

# ESP32-P4

Technical Reference Manual Pre-release v0.1

PRELIMINARY



ESPRESSIF

## About This Document

The **ESP32-P4 Technical Reference Manual** is targeted at developers working on low level software projects that use the ESP32-P4 SoC. It describes the hardware modules listed below for the ESP32-P4 SoC and other products in ESP32-P4 series. The modules detailed in this document provide an overview, list of features, hardware architecture details, any necessary programming procedures, as well as register descriptions.

## Navigation in This Document

Here are some tips on navigation through this extensive document:

- [Release Status at a Glance](#) on the very next page is a minimal list of all chapters from where you can directly jump to a specific chapter.
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## Release Status at a Glance

Note that this manual is still work in progress. See our release progress below:

| No.  | Chapter  | Progress  |
|--|--|-----------|
| <b>Part I. Microprocessor and Master</b>       |  |           |
| 1  | High-Performance CPU [to be added later]             | 95%       |
| 2  | RISC-V Trace Encoder (TRACE)                         | Published |
| 3  | Processor Instruction Extensions [to be added later] | 57%       |
| 4  | Low-Power CPU  | Published |
| <b>Part II. System DMA</b>                     |  |           |
| 5  | GDMA Controller (GDMA-AHB, GDMA-AXI)                 | Published |
| 6  | VDMA Controller (VDMA)                               | Published |
| 7  | 2D-DMA Controller (2D-DMA)                           | Published |
| <b>Part III. Memory Organization</b>           |  |           |
| 8  | System and Memory                                    | Published |
| 9  | eFuse Controller                                     | Published |
| <b>Part IV. System Component</b>               |  |           |
| 10   | GPIO Matrix and IO MUX                               | Published |
| 11   | Reset and Clock                                      | Published |
| 12   | Chip Boot Control                                    | Published |
| 13   | Interrupt Matrix                                     | Published |
| 14   | Event Task Matrix (ETM)                              | Published |
| 15   | Low-Power Management                                 | Published |
| 16   | System Timer   | Published |
| 17   | Timer Group (TIMG)                                   | Published |
| 18   | Watchdog Timers (WDT)                                | Published |
| 19   | RTC Timer  | Published |
| 20   | Permission Control (PMS)                             | Published |
| 21   | System Registers [to be added later]                 | 90%       |
| 22   | Debug Assistant                                      | Published |
| 23   | LP Mailbox   | Published |
| 24   | Brown-out Detector                                   | Published |
| <b>Part V. Cryptography/Security Component</b> |  |           |
| 25   | AES Accelerator (AES)                                | Published |
| 26   | ECC Accelerator (ECC)                                | Published |
| 27   | HMAC Accelerator (HMAC)                              | Published |
| 28   | RSA Accelerator (RSA)                                | Published |
| 29   | SHA Accelerator (SHA)                                | Published |
| 30   | Digital Signature Algorithm (DSA)                    | Published |
| 31   | Elliptic Curve Digital Signature Algorithm (ECDSA)   | Published |
| 32   | External Memory Encryption and Decryption (XTS_AES)  | Published |
| 33   | Random Number Generator (RNG)                        | Published |
| <b>Part VI. Image and Voice Processing</b>     |  |           |
| 34   | JPEG Codec   | Published |

| No.  | Chapter                                      | Progress  |
|--|--|-----------|
| 35   | Image Signal Processor (ISP)                 | Published |
| 36   | Pixel-Processing Accelerator (PPA)           | Published |
| 37   | LCD and Camera Controller (LCD_CAM)          | Published |
| 38   | H264 Encoder [to be added later]             | 81%       |
| 39   | MIPI CSI                                     | Published |
| 40   | MIPI DSI [to be added later]                 | 48%       |
| 41   | Voice Activity Detection (VAD)               | Published |
| <b>Part VII. Connectivity Interface</b>    |  |           |
| 42   | UART Controller (UART)                       | Published |
| 43   | SPI Controller (SPI)                         | Published |
| 44   | I2C Controller (I2C)                         | Published |
| 45   | Analog I2C Controller                        | Published |
| 46   | I3C Controller [to be added later]           | 48%       |
| 47   | I2S Controller (I2S)                         | Published |
| 48   | LP I2S Controller                            | Published |
| 49   | Pulse Count Controller (PCNT)                | Published |
| 50   | USB 2.0 High-Speed OTG                       | Published |
| 51   | USB 2.0 Full-Speed OTG                       | Published |
| 52   | USB Serial/JTAG Controller (USB_SERIAL_JTAG) | Published |
| 53   | Ethernet Media Access Controller (EMAC)      | Published |
| 54   | Two-Wire Automotive Interface (TWAI)         | Published |
| 55   | SD/MMC Host Controller (SDHOST)              | Published |
| 56   | LED PWM Controller (LEDC)                    | Published |
| 57   | Motor Control PWM (MCPWM)                    | Published |
| 58   | Remote Control Peripheral (RMT)              | Published |
| 59   | Parallel IO Controller (PARLIO)              | Published |
| 60   | BitScrambler                                 | Published |
| <b>Part VIII. Analog Signal Processing</b> |  |           |
| 61   | Touch Sensor (TOUCH)                         | Published |
| 62   | Temperature Sensor (TSENS)                   | Published |
| 63   | ADC Controller (ADC)                         | Published |
| 64   | Analog Voltage Comparator                    | Published |

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# Part I

## Microprocessor and Master

This part covers the essential processing elements of the system, diving into the microprocessor architecture with both high-performance and low-power CPUs. Details include CPU instruction extensions and trace encoding for debugging purposes.

## Chapter 1

### RISC-V Trace Encoder (TRACE)

The high-performance CPU (HP CPU) of ESP32-P4 supports the instruction trace interface through the trace encoder. The trace encoder connects to HP CPU's instruction trace interface, compresses the information into smaller packets, and then stores the packets into internal SRAM (see Chapter 6 *System and Memory*).

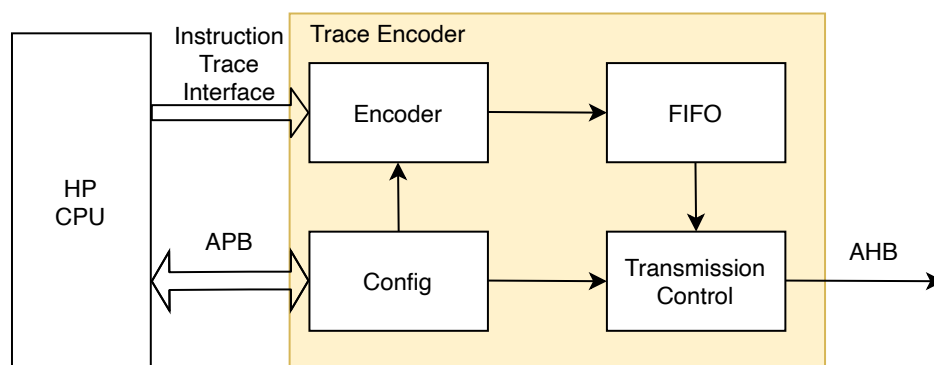


Figure 1.0-1. Trace Encoder Overview

## 1.1 Terminology

To better illustrate the functions of the RISC-V Trace Encoder, the following terms are used in this chapter.

|   |   |
|---|---|
| <b>hart</b>                                 | RISC-V hardware thread  |
| <b>branch</b>                               | an instruction which conditionally changes the execution flow   |
| <b>uninferable discontinuity (updiscon)</b> | a program counter change that can not be inferred from the program binary alone   |
| <b>delta</b>                                | a change in the program counter that is other than the difference between two instructions placed consecutively in memory |
| <b>trap</b>                                 | the transfer of control to a trap handler caused by either an exception or an interrupt                                   |
| <b>qualification</b>                        | an instruction that meets the filtering criteria passes the qualification, and will be traced                             |
| <b>te_inst</b>                              | the name of the packet type emitted by the encoder  |
| <b>retire</b>                               | the final stage of executing an instruction, when the machine state is updated  |
| <b>EPC</b>                                  | exception program counter   |

## 1.2 Introduction

In complex systems, understanding program execution flow is not straightforward. This may be due to a number of factors, for example, interactions with other cores, peripherals, real-time events, poor implementations, or some combination of all of the above.

It is hard to use a debugger to monitor the program execution flow of a running system in real time, as this is intrusive and might affect the running state. However, it is important to provide the visibility of program execution.

That is where instruction trace comes in, which provides trace of the program execution.

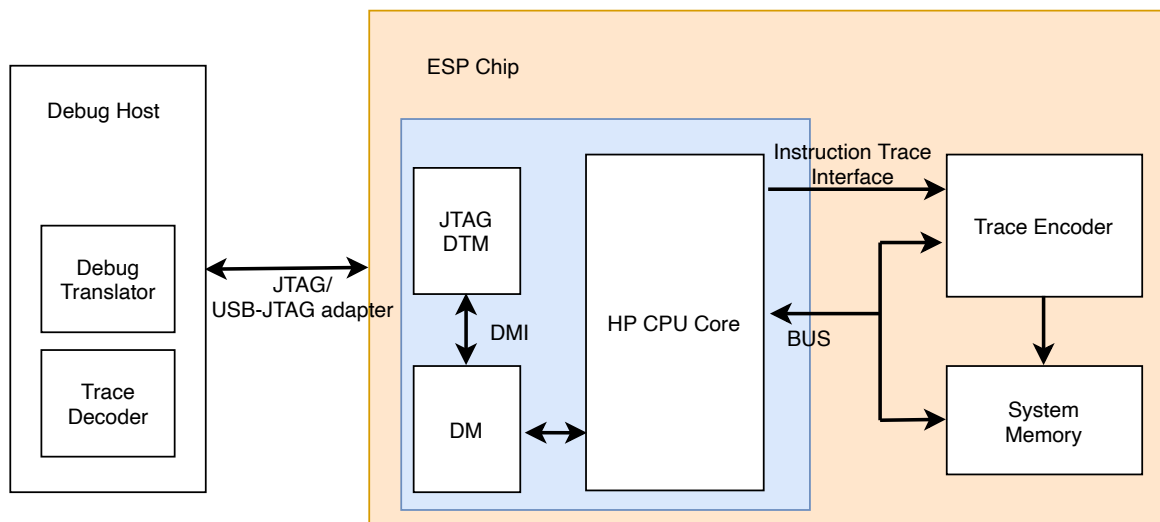


Figure 1.2-1. Trace Flow Overview

Figure 1.2-1 shows the instruction delta trace flow. Each HP Core has a private encoder that can work independently, and the trace flow of each core is the same:

- The HP CPU core provides an instruction trace interface that outputs the instruction information executed by the HP CPU. Such information includes instruction address, instruction type, etc. For more details about ESP32-P4 HP CPU's instruction trace interface, please refer to Chapter 1 [High-Performance CPU \[to be added later\]](#).
- The trace encoder collects the relevant instruction trace information from HP CPU's instruction trace interface, compresses the information into lower bandwidth packets, and then stores the packets in system memory.
- The debugger (debug host) can dump the trace packets from the system memory via JTAG or USB Serial/JTAG, and use a decoder to decompress and reconstruct the program execution flow. The trace decoder, usually software on an external PC, takes in the trace packets and reconstructs the program instruction flow with the program binary that runs on the originating hart. This decoding step can be done offline or in real time while the hart is executing.

## 1.3 Features

- Compatible with Efficient Trace for RISC-V Version 2.0. See Table 1.3-1 for the implemented parameters
- Support for delta address mode and full address mode
- Support for a filter unit
- Support for notifying an instruction address via debug trigger or filter unit
- Support for the following sideband signals to control trace data flow:
  - Support for debugging trigger to start or end encoder
  - When the hart is halted, the encoder can report the last packet and then stop
  - When the hart is reset, the encoder can report the last packet and then stop
  - Support for stalling the hart when FIFO is almost full
- Arbitrary address range of the trace memory size
- Configurable synchronization modes:
  - Synchronization counter counts by packet
  - Synchronization counter counts by cycle
  - Synchronization counter can be disabled
- Trace lost status to indicate packet loss
- Automatic restart after packet loss
- Memory writing in the loop or non-loop mode
- Support two interrupts:
  - Triggered when the packet size exceeds the configured memory space
  - Triggered when a packet is lost
- FIFO (128 × 8 bits) to buffer packets
- AHB burst transmission with configurable burst length

**Table 1.3-1. Trace Encoder Parameters**

| Parameter Name      | Value | Description                             |
|---------------------|-------|---|
| arch_p              | 0     | Initial version                         |
| bpred_size_p        | 0     | Branch prediction mode is not supported |
| cache_size_p        | 0     | Jump target cache mode is not supported |
| call_counter_size_p | 0     | Implicit return mode is not supported   |
| ctype_width_p       | 0     | Width of the ctype bus                  |
| context_width_p     | 0     | Width of context bus                    |
| ecause_width_p      | 6     | Width of exception cause                |
| ecause_choice_p     | 0     | Multiple choice is not supported        |
| f0s_width_p         | 0     | Format 0 packets are not supported      |
| filter_context_p    | 0     | Filtering on context is not supported   |

| Parameter Name      | Value | Description  |
|---------------------|-------|--|
| filter_excint_p     | 1     | Filtering on exception cause or interrupt is supported       |
| filter_privilege_p  | 1     | Filtering on privilege is supported                          |
| filter_tval_p       | 1     | Filtering on trap value is supported                         |
| iaddress_lsb_p      | 1     | Compressed instructions are supported                        |
| iaddress_width_p    | 32    | The instruction bus is 32-bit                                |
| iretire_width_p     | 1     | Width of the iretire bus                                     |
| ilastsize_width_p   | 0     | Width of the ilastsize                                       |
| itype_width_p       | 3     | Width of the itype bus                                       |
| nocontext_p         | 1     | Exclude context from te_inst packets                         |
| notime_p            | 1     | Exclude time from te_inst packets                            |
| privilege_width_p   | 1     | Only machine and user mode are supported                     |
| retires_p           | 1     | Maximum number of instructions that can be retired per block |
| return_stack_size_p | 0     | Implicit return mode is not supported                        |
| sijump_p            | 0     | Sequentially inferable jump mode is not supported            |
| taken_branches_p    | 1     | Only one instruction retired per cycle                       |
| impdef_width_p      | 0     | Not implemented  |

For detailed descriptions of the above parameters, please refer to the Efficient Trace for RISC-V Version 2.0 > Chapter Parameters and Discovery.

## 1.4 Architectural Overview

This chapter mainly introduces the implementation details of ESP32-P4's trace encoder.

As shown in Figure 1.0-1, the trace encoder contains an encoder, a FIFO, a register configuration module, and a transmission control module.

The encoder receives the HP CPU's instruction information via the instruction trace interface, compresses it into different packets, and writes it to the internal FIFO.

The transmission control module writes the data in the FIFO to the internal SRAM through the AHB bus.

The FIFO is 128 deep and 8-bit wide. When the memory bandwidth is insufficient, the FIFO may overflow, and packet loss occurs. If a packet is lost, the encoder will send a packet to tell that a packet is lost, stop working until the FIFO is empty, and also trigger an interrupt meanwhile if the interrupt is enabled.

## 1.5 Functional Description

### 1.5.1 Synchronization

In order to make the trace robust there must be regular synchronization points within the trace. Synchronization is accomplished by sending a full valued instruction address. When the synchronization counter value reaches the value of the [TRACE\\_RESYNC\\_PROLONGED](#) field of the [TRACE\\_RESYNC\\_PROLONGED\\_REG](#) register, the encoder will send a synchronization packet (format 3 subformat 0, see Section 1.6.3.1).

The synchronization counter is configured via [TRACE\\_RESYNC\\_MODE](#):

- 0: Disable the synchronization counter
- 1: Invalid. No effect
- 2: Synchronization counter counts by packet
- 3: Synchronization counter counts by cycle

You can adjust the trace bandwidth by increasing the value of [TRACE\\_RESYNC\\_PROLONGED](#) to reduce the frequency of sending synchronization packets, thereby reducing the bandwidth occupied by packets.

## 1.5.2 Address Mode

ESP32-P4 supports two address modes: delta address mode and full address mode.

- Delta address mode (default): In delta address mode, addresses are encoded as the difference between the actual address of the current instruction and the actual address of the instruction reported in the previous packet that contained an address. This differential encoding requires fewer bits than the full address, and thus results in more efficient trace compression.
- Full address mode: In full address mode, all addresses in the trace are encoded as absolute addresses instead of in differential form. This kind of encoding is always less efficient, but it can be a useful debugging aid for software decoder developers. This mode is enabled by setting [TRACE\\_FULL\\_ADDRESS](#).

## 1.5.3 Optional Sideband Signals

The Efficient Trace for RISC-V Version 2.0 > Chapter Optional Sideband Signals has provided some optional sideband signals for encoder control. ESP32-P4 has implemented the following functions:

**Table 1.5-1. Optional sideband signals**

| Signal       | Function   |
|--------------|--|
| trigger[2:0] | <ul style="list-style-type: none"> <li>• A pulse on bit 0 will cause the encoder to start tracing, and continue until further notice, subject to other filtering criteria also being met.</li> <li>• A pulse on bit 1 will cause the encoder to stop tracing until further notice.</li> <li>• A pulse on bit 2 will cause the encoder to report a specific address. This function is enabled by setting <a href="#">TRACE_DM_TRIGGER_ENA</a>. The trigger signal is asserted upon a trigger match. For example, if the <a href="#">action</a> field of <a href="#">mcontrol</a> is 2, while the trigger matched it will assert trigger bit0; if the <a href="#">action</a> is 3, while the trigger matched it will assert trigger bit1. For details, please refer to Table 1.8-1.</li> </ul> |
| halted       | <p>Hart is halted. Upon assertion, the encoder will output a packet to report the address of the last instruction retired before halting, followed by a support packet to indicate that tracing has stopped. Upon deassertion, the encoder will start tracing again, commencing with a synchronization packet. This function is enabled by setting <a href="#">TRACE_HALT_ENA</a>.</p>   |

| Signal | Function   |
|--------|--|
| reset  | Hart is in reset. Behavior is as described above for halted.   |
| stall  | Stall request to hart. Some applications may require lossless trace, which can be achieved by using this signal to stall the hart if the trace encoder is unable to output a trace packet (internal FIFO almost full). This function is enabled by setting <a href="#">TRACE_STALL_ENA</a> . |

### 1.5.4 Filtering

Filtering provides a mechanism to control the criteria for encoder to produce a trace. For example, it may be desirable to trace:

- When the instruction address is within a particular range
- Starting from one instruction address and continue until a second instruction address
- For one or more specified privilege levels
- Exception and/or interrupt handlers for specified exception causes

The filtering unit has a filter and a comparator unit.

Each comparator unit is actually a pair of comparators (Primary and Secondary, or P, S) allowing a bounded range to be matched with a signal unit if required, and offers:

- Input selected from iaddress and tval
- A range of arithmetic options (<, >, =, !=, etc.) independently selectable for each comparator
- Secondary match value may be used as a mask for the primary comparator
- The two comparators can be combined in several ways:  $P$ ,  $P \& \& S$ ,  $!(P \& \& S)$ , latch (set on P clear on S)
- Each comparator can also be used to explicitly report a particular instruction address

Each filter can specify filtering against instruction from the hart, and offers:

- 1 run-time selectable comparator units to match
- Multiple choice selection for priv and cause inputs
- Select matching for interrupt

### 1.5.5 Anchor Tag

Since the length of data packets is variable, in order to identify boundaries between data packets when packed packets are written to memory, the ESP32-P4 encoder inserts zero bytes between data packets:

- The maximum packet length is 13 bytes, so a sequence of at least 14 zero bytes cannot occur within a normal packet. Therefore, the first non-zero byte seen after a sequence of at least 14 zero bytes must be the first byte of a packet.
- Every time when 128 packets are transmitted, the encoder writes 14 zero bytes to the memory partition boundary as anchor tags.

## 1.5.6 Memory Writing Mode

When writing the trace memory, the size of the trace packets might exceed the capacity of the memory. In this case, you can choose whether to wrap around the trace memory or not by configuring the memory writing mode:

- Loop mode: When the size of the trace packets exceeds the capacity of the trace memory (namely when `TRACE_MEM_CURRENT_ADDR_REG` reaches the value of `TRACE_MEM_END_ADDR_REG`), the trace memory is wrapped around, so that the encoder loops back to the memory's starting address `TRACE_MEM_START_ADDR_REG`, and old data in the memory will be overwritten by new data.
- Non-loop mode: When the size of the trace packets exceeds the capacity of the trace memory, the trace memory is not wrapped around. The encoder stops at `TRACE_MEM_END_ADDR_REG`, and old data will be retained.

## 1.5.7 Automatic Restart

When packets are lost due to FIFO overflow, the encoder will stop working and need to be resumed by software manually or restarted by hardware automatically. If the `TRACE_RESTART_ENA` bit of `TRACE_TRIGGER_REG` is set, once the FIFO is empty, the encoder can automatically be restarted.

If the automatic restart feature is enabled, the encoder will be restarted in any case. Therefore, to disable the encoder, the automatic restart feature must be disabled first by clearing the `TRACE_RESTART_ENA` bit of the `TRACE_TRIGGER_REG` register.

## 1.6 Encoder Output Packets

This section mainly introduces ESP32-P4 trace encoder output packet format.



Figure 1.6-1. Trace packet Format

A packet includes header, index and payload. Header, index and payload are transmitted sequentially in bit stream form, from the fields listed at the top of tables below to the fields listed at the bottom. If a field consists of multiple bits, then the least significant bit is transmitted first.

### 1.6.1 Header

Header is 1-byte long. The format of header is shown in Table 1.6-1.



**Table 1.6-1. Header Format**

| Field     | Bits | Description            | Value  |
|-----------|------|------------------------|--------|
| length    | 5    | Length of whole packet | 4 ~ 13 |
| flow      | 2    | Reserved               | 0      |
| timestamp | 1    | Reserved               | 0      |

## 1.6.2 Index

Index has 2 bytes. The format of index is shown in Table 1.6-2.

**Table 1.6-2. Index Format**

| Field | Bits | Description              | Value   |
|-------|------|--------------------------|---------|
| index | 16   | The index of each packet | 0~65536 |

## 1.6.3 Payload

The length of payload ranges from 1 byte to 10 bytes.

### 1.6.3.1 Format 3 Packets

Format 3 packets are used for synchronization, and report supporting information. There are 4 subformats defined in the specification. ESP32-P4 only supports 3 of them.

#### Format 3 Subformat 0 - Synchronization

This packet contains all the information the decoder needs to fully identify an instruction. It is sent for the first traced instruction (unless that instruction also happens to be the first one in an exception handler), and when synchronization has been scheduled by expiry of the synchronization timer. The payload length is 5 bytes.

**Table 1.6-3. Packet format 3 subformat 0**

| Field name  | Bits | Description  |
|-------------|------|--|
| format      | 2    | 11 (sync): Synchronization   |
| subformat   | 2    | 00 (start): Start of tracing, or resync  |
| branch      | 1    | Set to 0 if the address points to a branch instruction, and the branch was taken. Set to 1 if the instruction is not a branch or if the branch is not taken. |
| privilege   | 1    | The privilege level of the reported instruction  |
| address     | 31   | Full instruction address. The address must be left shifted 1 bit in order to recreate the original byte address.   |
| sign_extend | 3    | Reserved   |

#### Format 3 Subformat 1 - Exception

This packet also contains all the information the decoder needs to fully identify an instruction. It is sent following an exception or interrupt, and includes the cause, the 'trap value' (for exceptions), and the address

of the trap handler or of the exception itself. The length is variable: if the interrupt field is 1, the tvalepc field is omitted and the length is 6 bytes, otherwise the length is 10 bytes.

**Table 1.6-4. Packet format 3 subformat 1**

| Field name  | Bits | Description   |
|-------------|------|---|
| format      | 2    | 11 (sync): Synchronization  |
| subformat   | 2    | 01 (exception): Exception cause and trap handler address  |
| branch      | 1    | Set to 0 if the address points to a branch instruction, and the branch was taken. Set to 1 if the instruction is not a branch or if the branch is not taken.  |
| privilege   | 1    | The privilege level of the reported instruction   |
| ecause      | 6    | Exception cause   |
| interrupt   | 1    | Interrupt   |
| theadr      | 1    | When set to 1, the address field points to the trap handler address. When set to 0, the address field points to the EPC (exception program counter) for an exception at the target for an updiscon, and is undefined for other exceptions and interrupts. |
| address     | 31   | Full instruction address. The value of this field must be left shifted 1 bit in order to recreate the original byte address.  |
| tvalepc     | 32   | Value from appropriate utval/stval/mtval CSR (control/status register). Omitted if the interrupt is 1   |
| sign_extend | 3    | Reserved  |

### Format 3 Subformat 3 - Support

This packet provides supporting information to aid the decoder. It is issued when the trace is ended, filter match is failed, or a packet is lost. The length is 2 bytes.

**Table 1.6-5. Packet format 3 subformat 3**

| Field name   | Bits | Description   |
|--------------|------|---|
| format       | 2    | 11 (sync): Synchronization  |
| subformat    | 2    | 11 (support): Supporting information for the decoder  |
| enable       | 1    | Indicates if the encoder is enabled   |
| encoder_mode | 1    | Always 0. Only supported by branch trace  |
| qual_status  | 2    | Indicates qualification status: <ul style="list-style-type: none"> <li>• 00 (no_change): No change to filter qualification</li> <li>• 01 (ended_rep): Qualification ended, preceding instruction sent explicitly to indicate last qualification instruction</li> <li>• 10 (trace lost): One or more packets lost</li> <li>• 11 (ended_upd): Qualification ended, preceding te_inst would have been sent anyway due to an updiscon, even if wasn't the last qualified instruction</li> </ul> |

| Field name  | Bits | Description  |
|-------------|------|--|
| ioptions    | 6    | <p>Indicates optional modes:</p> <ul style="list-style-type: none"> <li>sequentially inferred jumps (Bits 5): When set to 1, the targets of sequentially inferable jumps will not be reported. (This feature is not implemented, so bit 5 should always be 0)</li> <li>branch prediction (Bit 4): When set to 1, the branch prediction is enabled. (This feature is not implemented, so bit 4 should always be 0)</li> <li>jump target cache (Bit 3): When set to 1, the jump target cache is enabled. (This feature is not implemented, so bit 3 should always be 0)</li> <li>full address (Bit 2): <ul style="list-style-type: none"> <li>0: delta address mode</li> <li>1: full address mode</li> </ul> </li> <li>implicit exception (Bit 1): Exclude address from format 3 subformat 1 packet if trap vector can be determined from ecause. (This feature is not implemented, so bit 1 should always be 0)</li> <li>implicit return (Bit 0): When set to 1, function return addresses will not be reported. (This feature is not implemented, bit 0 should always be 0)</li> </ul> |
| sign_extend | 2    | Reserved   |

### 1.6.3.2 Format 2 Packets

This packet contains only an instruction address, and is used when the address of an instruction must be reported (for example if the instruction is the target for an updiscon, or is the last instruction before exception), and there is no reported branch information.

The length is variable if delta address mode is enabled, ranging from 5 bytes to 8 bytes. The address field can be 8/16/24/32 bits, inferred from the packet length. For example, if the header length is  $n$  bytes, the address bits are  $n - 4$  bytes. A sign bit is required to extend the address field to 32 bits.

**Table 1.6-6. Packet format 2**

| Field name | Bits | Description  |
|------------|------|--|
| format     | 2    | 10 (addr-only): No branch information  |
| notify     | 1    | If the value of this bit is different from the MSB of address, it indicates that this packet is reporting an instruction that is not the target of an uninferable discontinuity because a notification was requested via trigger[2] or a filter matched. |
| updiscon   | 1    | If the value of this bit is different from notify, it indicates that this packet is reporting the instruction following an uninferable discontinuity and is also the instruction before an exception, privilege change or resync.                        |

| Field name  | Bits     | Description  |
|-------------|----------|--|
| zero_extend | 4        | Reserved   |
| address     | Variable | Delta instruction address. These bits can be 8/16/24/32. |

### 1.6.3.3 Format 1 Packets

This packet includes branch information, and is used when either the branch information must be reported (for example because the branch map is full), or when the address of instruction must be reported, and there has been at least one branch since the previous packet.

The packet length is variable if delta address mode is enabled, ranging from 5 bytes to 12 bytes. The address field can be 8/16/24/32 bits, inferred from the packet length. For example:

- The header length is  $n$  bytes
- The value of the format field is 1
- The value of the branch field is:
  - 0: the packet is format 1 without address
  - 1: branch\_map is 1 bit wide, zero\_ext is 6 bits wide, and address is  $n - 5$  bits wide
  - 2 ~ 3: branch\_map is 3 bits wide, zero\_ext is 4 bits wide, and address is  $n - 5$  bits wide
  - 4 ~ 7: branch\_map is 7 bits wide, zero\_ext is 0 bits wide, and address is  $n - 5$  bits wide
  - 8 ~ 15: branch\_map is 15 bits wide, zero\_ext is 0 bits wide, and address is  $n - 6$  bits wide
  - 16 ~ 31: branch\_map is 31 bits wide, zero\_ext is 0 bits wide, and address is  $n - 8$  bits wide

#### Format 1 - address, branch\_map

The length is variable.

**Table 1.6-7. Packet format 1 with address**

| Field name | Bits | Description  |
|------------|------|--|
| format     | 2    | 01: Includes branch information  |
| branches   | 5    | Number of valid bits branch_map. The number of bits of branch_map is determined as follows: <ul style="list-style-type: none"> <li>• 0: (cannot occur for this format)</li> <li>• 1: 1 bit</li> <li>• 2 ~ 3: 3 bits</li> <li>• 4 ~ 7: 7 bits</li> <li>• 8 ~ 15: 15 bits</li> <li>• 16 ~ 31: 31 bits</li> </ul> For example if branches = 12, branch_map is 15-bit long, and the 12 LSBs are valid. |

| Field name | Bits     | Description   |
|------------|----------|---|
| branch_map | Variable | An array of bits indicating whether branches are taken or not. Bit 0 represents the oldest branch instruction executed. For each bit: <ul style="list-style-type: none"> <li>• 0: branch taken</li> <li>• 1: branch not taken</li> </ul> The field Bits is variable and determined by the branches field. |
| notify     | 1        | If the value of this bit is different from the MSB of address, it indicates that this packet is reporting an instruction that is not the target of an uninferable discontinuity because a notification was requested via trigger[2] or a filter matched.  |
| updiscon   | 1        | If the value of this bit is different from notify, it indicates that this packet is reporting the instruction following an uninferable discontinuity and is also the instruction before an exception, privilege change or resync.   |
| zero_ext   | Variable | The length of this field is determined by branches as follows: <ul style="list-style-type: none"> <li>• 1: 6 bits</li> <li>• 2 ~ 3: 4 bits</li> <li>• 4 ~ 31: 0 bits</li> </ul>   |
| address    | Variable | Delta instruction address. These bits can be 8/16/24/32   |

**Format 1 - no address, branch\_map**

The length is 5 bytes.

**Table 1.6-8. Packet format 1 without address**

| Field name  | Bits | Description  |
|-------------|------|--|
| format      | 2    | 01: includes branch information  |
| branches    | 5    | Number of valid bits in branch_map. The length of branch_map is 31 bits. Only 0 valid.   |
| branch_map  | 31   | An array of bits indicating whether branches are taken or not. Bit 0 represents the oldest branch instruction executed. For each bit: <ul style="list-style-type: none"> <li>• 0: branch taken</li> <li>• 1: branch not taken</li> </ul> |
| sign_extend | 2    | Reserved   |

## 1.7 Interrupt

ESP32-P4's CORE<sub>n</sub>\_TRACE (i.e., the trace encoder of core 0 or core 1) can generate the CORE<sub>n</sub>\_TRACE\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#).

There are several internal interrupt sources from CORE<sub>n</sub>\_TRACE that can generate the above interrupt signal. The interrupt sources from CORE<sub>n</sub>\_TRACE are listed with their trigger conditions and the resulted interrupt signals in Table 1.7-1.

Table 1.7-1. CORE<sub>n</sub>\_TRACE's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition  | Interrupt Signal              |
|---------------------------|--|-------------------------------|
| TRACE_MEM_FULL_INTR       | Triggered when the packet size exceeds the capacity of the trace memory, namely when <a href="#">TRACE_MEM_CURRENT_ADDR_REG</a> reaches the value of <a href="#">TRACE_MEM_END_ADDR_REG</a> . If necessary, this interrupt can be enabled to notify the HP CPU for processing, such as applying for a new memory space again | CORE <sub>n</sub> _TRACE_INTR |
| TRACE_FIFO_OVERFLOW_INTR  | Triggered when the internal FIFO overflows and one or more packets have been lost.   | CORE <sub>n</sub> _TRACE_INTR |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section 1.9 [Register Summary](#).

## 1.8 Programming Procedures

### 1.8.1 Encoder Option Configuration

The Encoder has some optional configuration options.

- Full address mode
  - The encoder uses delta address mode by default. Users can set [TRACE\\_FULL\\_ADDRESS](#) to enable full address mode for debugging.
- Restart after packet loss
  - Once the trace packet is lost due to FIFO overflow, the encoder will automatically stop if [TRACE\\_RESTART\\_ENA](#) is set. When the FIFO is empty, the encoder will restart to report packets.
- Stall CPU while FIFO is almost full
  - If [TRACE\\_STALL\\_ENA](#) is set, when the FIFO is almost full, a stall request will be asserted to the CPU, and the CPU will be stalled until the request is deasserted.
- Stop tracing when the CPU is halted
 

If [TRACE\\_HALT\\_ENA](#) is set, when the CPU is halted, the encoder will output a packet to report the address of the last instruction before halting, followed by a support packet to indicate that tracing has stopped. Upon the deassertion of the halted signal, the encoder will start tracing again, commencing with a synchronization packet.
- Stop tracing when the CPU is in reset

The encoder will be reset separately, if [TRACE\\_RESET\\_ENA](#) is set. When the CPU is in reset, the encoder will output a packet to report the address of the last instruction before reset, followed by a support packet to indicate that tracing has stopped. Once the CPU exits from reset, the encoder will start tracing again, commencing with a synchronization packet.

- Using trigger outputs from the Debug Module

The debug module of the RISC-V hart has a trigger unit. This defines a match control register ([mcontrol](#)) containing a 4-bit [action](#) field, and reserves codes 2 ~ 4 of this field for trace use. ESP32-P4 has implemented this feature. The values of the [action](#) field are listed in Table 1.8-1.

**Table 1.8-1. Debug module trigger support (the [action](#) field of the [mcontrol](#) register)**

| Value | Description   |
|-------|---|
| 2     | Trace-on: start trace                                 |
| 3     | Trace-off: end trace                                  |
| 4     | Trace-notify: notify the encoder to report an address |

For details about the debug module trigger unit, please refer to Chapter 1 [High-Performance CPU \[to be added later\]](#).

## 1.8.2 Filter Configuration

The filter unit described in Section 1.5.4 can be configured as follows:

1. Select one of the following match modes:
  - Set [TRACE\\_MATCH\\_PRIVILEGE](#) to enable privilege match mode:
    - Configure [TRACE\\_MATCH\\_CHOICE\\_PRIVILEGE](#) to specify the privilege level.
  - Set [TRACE\\_MATCH\\_ECAUSE](#) to enable ecause match mode:
    - Configure [TRACE\\_MATCH\\_CHOICE\\_ECAUSE](#) to specify the ecause value
  - Set [TRACE\\_MATCH\\_INTERRUPT](#) to enable interrupt match mode:
    - Configure [TRACE\\_MATCH\\_VALUE\\_INTERRUPT](#) to specify interrupt level
  - Set [TRACE\\_MATCH\\_COMP](#) to enable comparator match mode:
    - Configure the primary comparator:
      - \* Configure [TRACE\\_P\\_INPUT](#) to choose the input
      - \* Configure [TRACE\\_P\\_FUNCTION](#) to select the comparator function
      - \* Configure [TRACE\\_FILTER\\_P\\_COMPARATOR\\_MATCH\\_REG](#) to define match value
    - Configure the secondary comparator if needed:
      - \* Configure [TRACE\\_S\\_INPUT](#) to choose the input
      - \* Configure [TRACE\\_S\\_FUNCTION](#) to select the comparator function
      - \* Configure [TRACE\\_FILTER\\_S\\_COMPARATOR\\_MATCH\\_REG](#) to define match value
    - Choose which comparator to match via [TRACE\\_MATCH\\_MODE](#):

- \* 0: only the primary comparator matches, and the secondary comparator has no effect
- \* 1: both the primary comparator and the secondary comparator match ( $P \& \& S$ )
- \* 2: neither the primary comparator nor secondary comparator match ( $\neg(P \& \& S)$ )
- \* 3: start filtering when primary matches up until secondary matches

If [TRACE\\_P\\_NOTIFY](#) or [TRACE\\_S\\_NOTIFY](#) is set, the comparator will report the matched address as a notification, the instructions will not be filtered. For example:

- If the [TRACE\\_MATCH\\_MODE](#) is 0, and [TRACE\\_P\\_NOTIFY](#) is set, then all instructions will be traced, and the matched primary comparator will be notified.
- If the [TRACE\\_MATCH\\_MODE](#) is 0, and [TRACE\\_S\\_NOTIFY](#) is set, the instruction will be filtered by the primary comparator, and the instruction that matches the secondary comparator will be notified.

2. Set [TRACE\\_FILTER\\_EN](#) to enable filter unit.

### 1.8.3 Enable Encoder

- Configure the address space for the trace memory via [TRACE\\_MEM\\_START\\_ADDR\\_REG](#) and [TRACE\\_MEM\\_END\\_ADDR\\_REG](#). The encoder can access L2 MEM and PSRAM:
  - L2MEM: 0x4FF00000 ~ 0x4FFBFFFF
  - PSRAM: 0x48000000 ~ 0x4BFFFFFF
- Update the value of [TRACE\\_MEM\\_CURRENT\\_ADDR\\_REG](#) to the value of [TRACE\\_MEM\\_START\\_ADDR\\_REG](#) by setting [TRACE\\_MEM\\_CURRENT\\_ADDR\\_UPDATE](#)
- (Optional) Configure the memory writing mode via the [TRACE\\_MEM\\_LOOP](#) bit of [TRACE\\_TRIGGER\\_REG](#)
  - 0: Non-loop mode
  - 1: Loop mode (default)
- Configure the synchronization mode via the [TRACE\\_RESYNC\\_MODE](#) bit of [TRACE\\_RESYNC\\_PROLONGED\\_REG](#)
  - 0: Disable the synchronization counter
  - 1: Invalid. No effect
  - 2: Synchronization counter counts by packet
  - 3: Synchronization counter counts by cycle
- (Optional) Configures the threshold for the synchronization counter (default value is 128) via [TRACE\\_RESYNC\\_PROLONGED\\_REG](#)
- (Optional) Enable Interrupt
  - Set the corresponding bit of [TRACE\\_INTR\\_ENA\\_REG](#) to enable the corresponding interrupt
  - Set the corresponding bit of [TRACE\\_INTR\\_CLR\\_REG](#) to clear the corresponding interrupt
  - Read [TRACE\\_INTR\\_RAW\\_REG](#) to know which interrupt occurs



- (Optional) Enable automatic restart by setting the [TRACE\\_RESTART\\_ENA](#) bit of [TRACE\\_TRIGGER\\_REG](#). This function is enabled by default
- There are 2 ways to enable the trace encoder:
  - Setting the [TRACE\\_TRIGGER\\_ON](#) bit of [TRACE\\_TRIGGER\\_REG](#)
  - Through the Debug module Trace-on to start the encoder. When the trigger is matched and the [action](#) is 2, it will start the encoder. For trigger configurations, please refer to the RISC-V Debug Specification.

Once the encoder is enabled, it will keep tracing the HP CPU's instruction trace interface and writing packets to the trace memory.

### 1.8.4 Disable Encoder

There are two ways to end output trace packets:

1. Set [TRACE\\_TRIGGER\\_OFF](#) of [TRACE\\_TRIGGER\\_REG](#) to end the encoder
2. Through the Debug module Trace-off to end the encoder. When the trigger is matched and the [action](#) is 3, it will end the encoder. For trigger configurations, please refer to the RISC-V Debug Specification.

Due to the internal FIFO, the packets are not written to the memory immediately after the end of the trace. It is recommended to query the [TRACE\\_FIFO\\_STATUS\\_REG](#) to confirm that the data is all written to memory.

**Table 1.8-2. Trace Status**

| Field                             | Description  |
|-----------------------------------|--|
| <a href="#">TRACE_FIFO_EMPTY</a>  | If 1 indicates that the FIFO is empty, all data have been written to memory  |
| <a href="#">TRACE_WORK_STATUS</a> | Encoder's work status: <ul style="list-style-type: none"> <li>• 0: idle state, the encoder is not started</li> <li>• 1: the encoder is normally working that output packets</li> <li>• 2: the encoder is not outputting packets, the CPU is halted or in reset</li> <li>• 3: the encoder is not outputting packets, it occurs while a packet is lost, and is waiting for FIFO empty to restart.</li> </ul> |

### 1.8.5 Notify

Users may want to report a special address, even if it is not the target of an uninferable discontinuity. There are two ways to notify and report a special address:

1. The debug trigger unit matched, and the [action](#) is 4
2. The filter comparator matched

When a notification is requested, the encoder will report a format 2 or format 1 with an address packet, determined by the [branch\\_map](#). If [branch\\_map](#) is 0, report format 2, otherwise report format 1. The notify field shows whether the packet is reporting a notification address. If it is the target of an uninferable discontinuity,

even if it is a notification, the notify field will not be asserted, otherwise the decoder cannot reconstruct the instruction stream correctly.

### 1.8.6 Decode Data Packets

- Find the first address to decode
  - Read the [TRACE\\_MEM\\_FULL\\_INTR\\_RAW](#) bit of the [TRACE\\_INTR\\_RAW\\_REG](#) register to know if the trace memory is full
    - \* if read 0, read the trace packets from [TRACE\\_MEM\\_START\\_ADDR\\_REG](#)
    - \* if read 1, and the loop mode is enabled, then the old trace packets are overwritten. In this case, read the [TRACE\\_MEM\\_CURRENT\\_ADDR\\_REG](#) to know the last writing address, and use this address as the first address to decode
- Use the decoder to decode data packets
  - The decoder reads all data packets starting from the first address, and reconstructs the data stream with the binary file
  - As mentioned in [1.6](#), the encoder writes 14 zero bytes to the memory partition boundary every time when 128 packets are transmitted. Given this fact, the first non-zero byte after 14 zero bytes should be the header of a new packet

### 1.8.7 AHB Configuration

ESP32-P4 encoder supports the AHB bus. There are some optional configurations to control the transmission bandwidth of the encoder.

If there are many DMA masters, users can increase the bandwidth of Trace by setting AHB burst [TRACE\\_AHB\\_CONFIG\\_REG](#).

- The [TRACE\\_HBURST](#) supports the following configurations:
  - 0x0: SINGLE
  - 0x1: INCR (length not defined)
  - 0x2: INCR4
  - 0x4: INCR8
  - Others: reserved

Burst transfer means that once arbitration is successful, multiple words can be transferred continuously. For SINGLE, the length is 1; for INCR, the length is undefined; for INCR4, the length is 4; for INCR8, the length is 8. The longer the burst length, the better the bandwidth.

- When configured as INCR transfer, since INCR is a burst of indeterminate length, in order to avoid Trace occupying the bus for a long time, it will end the INCR transfer after the transfer length up to [TRACE\\_MAX\\_INCR](#), and restart bus arbitration.

This is the configuration used to adjust the bandwidth. When the bandwidth is sufficient, it's not required to do the configuration, and users can use the default configuration.

### 1.8.8 Software Retention

The `TRACE_WORK_STATUS` represents the state of the encoder. When the encoder is not in the IDLE state, it must backup and restore the configuration when the chip enters sleep.

## 1.9 Register Summary

The addresses in this section are relative to RISC-V Trace Encoder base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

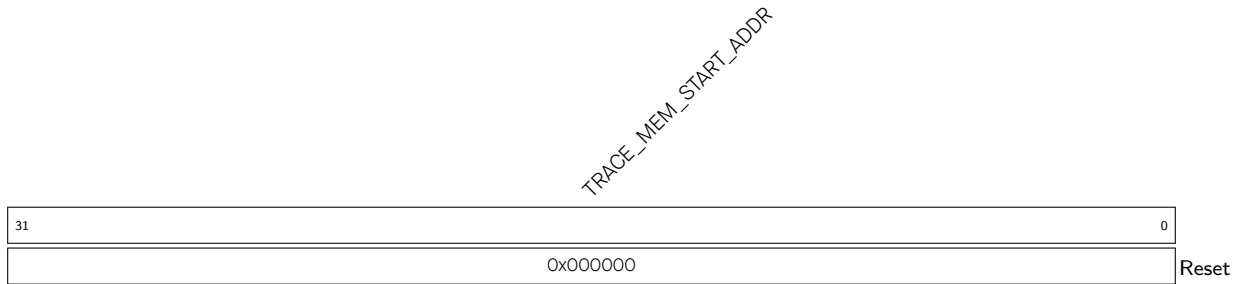
| Name   | Description                               | Address | Access |
|--|---|---------|--------|
| <b>Memory configuration registers</b>                  |   |         |        |
| <a href="#">TRACE_MEM_START_ADDR_REG</a>               | Memory start address                      | 0x0000  | R/W    |
| <a href="#">TRACE_MEM_END_ADDR_REG</a>                 | Memory end address                        | 0x0004  | R/W    |
| <a href="#">TRACE_MEM_CURRENT_ADDR_REG</a>             | Memory current address                    | 0x0008  | RO     |
| <a href="#">TRACE_MEM_ADDR_UPDATE_REG</a>              | Memory address update                     | 0x000C  | WT     |
| <b>FIFO status register</b>                            |   |         |        |
| <a href="#">TRACE_FIFO_STATUS_REG</a>                  | FIFO status register                      | 0x0010  | RO     |
| <b>Interrupt registers</b>                             |   |         |        |
| <a href="#">TRACE_INTR_ENA_REG</a>                     | Interrupt enable register                 | 0x0014  | R/W    |
| <a href="#">TRACE_INTR_RAW_REG</a>                     | Interrupt raw status register             | 0x0018  | RO     |
| <a href="#">TRACE_INTR_CLR_REG</a>                     | Interrupt clear register                  | 0x001C  | WT     |
| <b>Trace configuration registers</b>                   |   |         |        |
| <a href="#">TRACE_TRIGGER_REG</a>                      | Trace trigger register                    | 0x0020  | varies |
| <a href="#">TRACE_CONFIG_REG</a>                       | Trace configuration register              | 0x0024  | R/W    |
| <a href="#">TRACE_FILTER_CONTROL_REG</a>               | Filter control register                   | 0x0028  | R/W    |
| <a href="#">TRACE_FILTER_MATCH_CONTROL_REG</a>         | Filter match control register             | 0x002C  | R/W    |
| <a href="#">TRACE_FILTER_COMPARATOR_CONTROL_REG</a>    | Filter comparator match control register  | 0x0030  | R/W    |
| <a href="#">TRACE_FILTER_P_COMPARATOR_MATCH_REG</a>    | Primary comparator match value register   | 0x0034  | R/W    |
| <a href="#">TRACE_FILTER_S_COMPARATOR_MATCH_REG</a>    | Secondary comparator match value register | 0x0038  | R/W    |
| <a href="#">TRACE_RESYNC_PROLONGED_REG</a>             | Resynchronization configuration register  | 0x003C  | R/W    |
| <a href="#">TRACE_AHB_CONFIG_REG</a>                   | AHB configuration register                | 0x0040  | R/W    |
| <b>Clock gating control and configuration register</b> |   |         |        |
| <a href="#">TRACE_CLOCK_GATE_REG</a>                   | Clock gating control register             | 0x0044  | R/W    |
| <b>Version register</b>                                |   |         |        |
| <a href="#">TRACE_DATE_REG</a>                         | Version control register                  | 0x03FC  | R/W    |

## 1.10 Registers

The addresses in this section are relative to RISC-V Trace Encoder base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

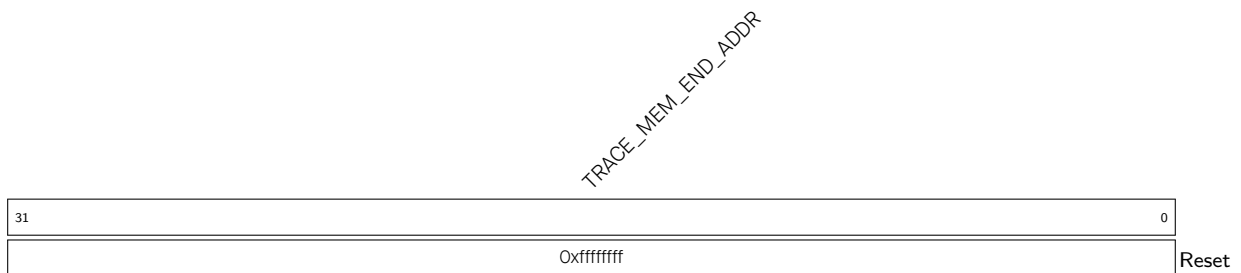
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 1.1. TRACE\_MEM\_START\_ADDR\_REG (0x0000)**



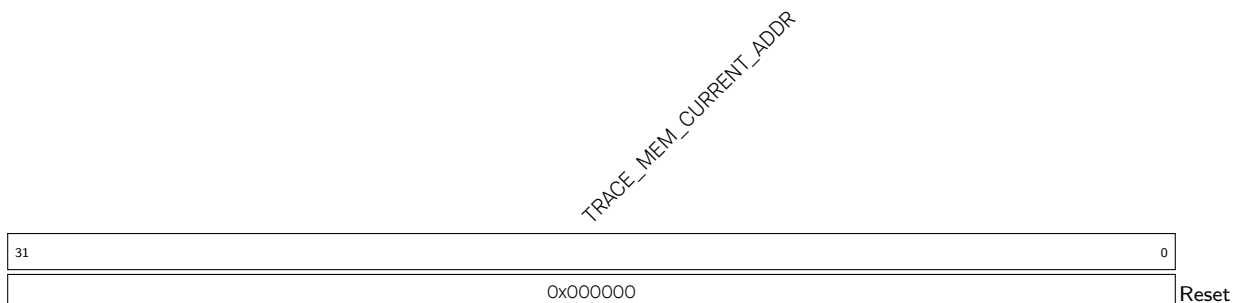
**TRACE\_MEM\_START\_ADDR** Configures the start address of the trace memory. (R/W)

**Register 1.2. TRACE\_MEM\_END\_ADDR\_REG (0x0004)**



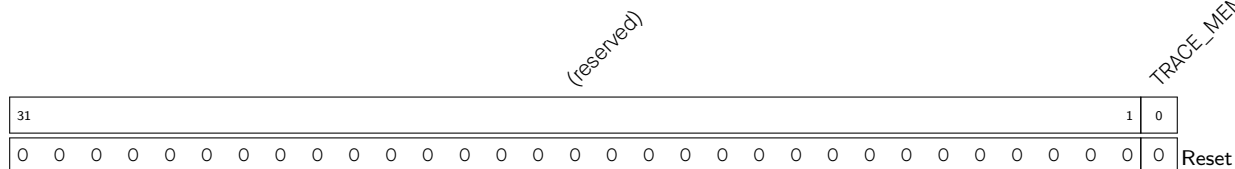
**TRACE\_MEM\_END\_ADDR** Configures the end address of the trace memory. (R/W)

**Register 1.3. TRACE\_MEM\_CURRENT\_ADDR\_REG (0x0008)**



**TRACE\_MEM\_CURRENT\_ADDR** Represents the current memory address for writing. (RO)

#### Register 1.4. TRACE\_MEM\_ADDR\_UPDATE\_REG (0x000C)



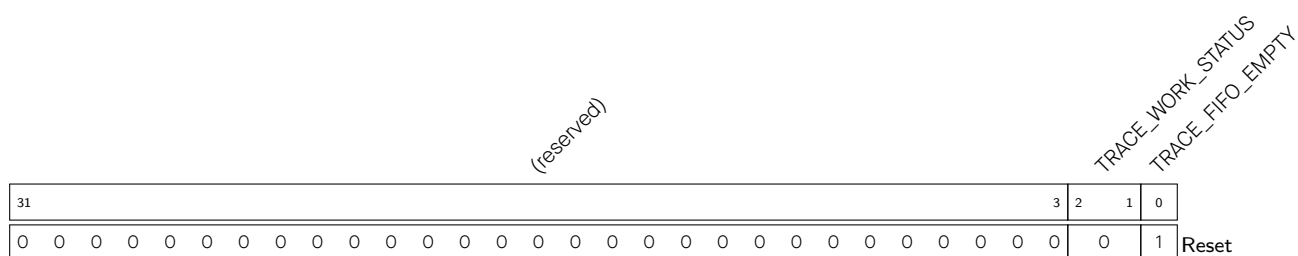
**TRACE\_MEM\_CURRENT\_ADDR\_UPDATE** Configures whether to update the value of **TRACE MEM CURRENT ADDR** to **TRACE MEM START ADDR**.

0: Not update

1: Update

(WT)

### Register 1.5. TRACE\_FIFO\_STATUS\_REG (0x0010)



**TRACE\_FIFO\_EMPTY** Represents whether the FIFO is empty.

1: Empty

0: Not empty (RO)

**TRACE\_WORK\_STATUS** Represents the state of the encoder:

0: Idle state

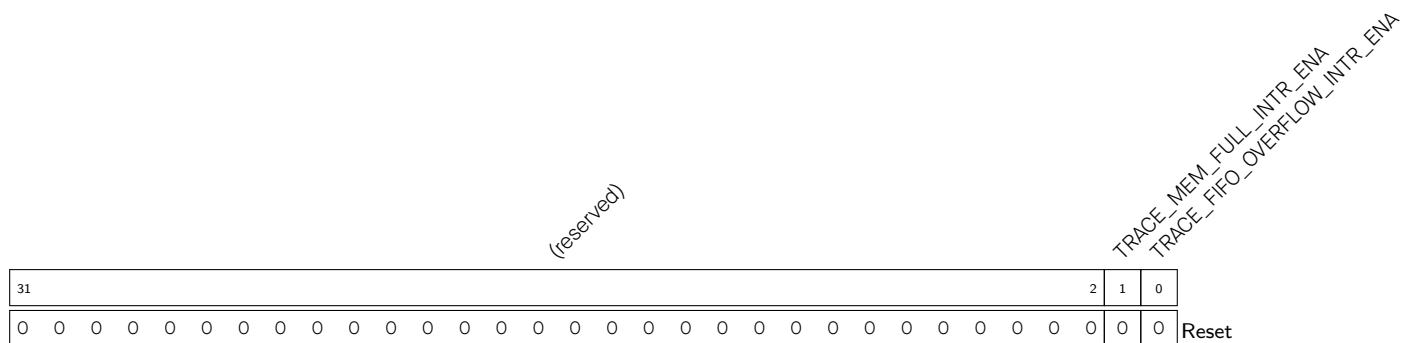
1: Working state

2: Wait state because the hart is halted or in reset

3: Lost state

(RO)

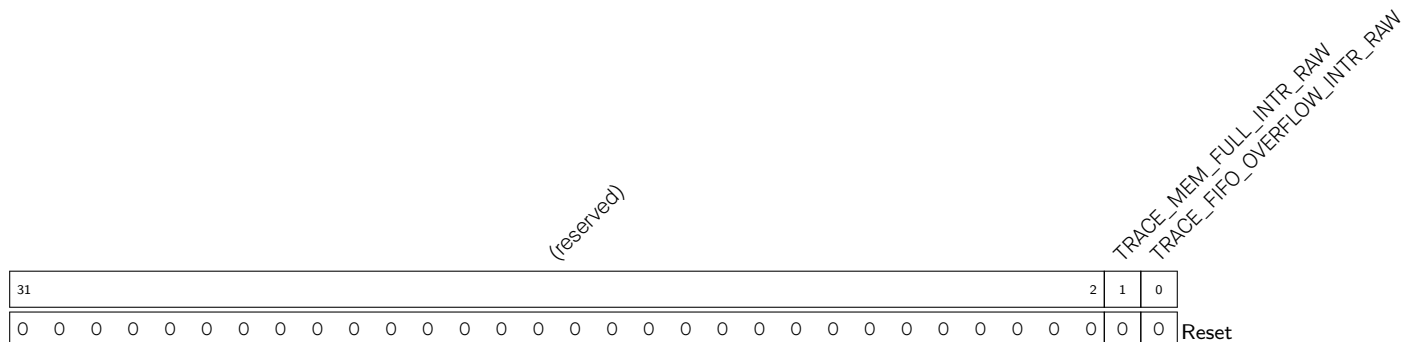
### Register 1.6. TRACE\_INTR\_ENA\_REG (0x0014)



**TRACE\_FIFO\_OVERFLOW\_INTR\_ENA** Write 1 to enable TRACE\_FIFO\_OVERFLOW\_INTR. (R/W)

**TRACE\_MEM\_FULL\_INTR\_ENA** Write 1 to enable TRACE\_MEM\_FULL\_INTR. (R/W)

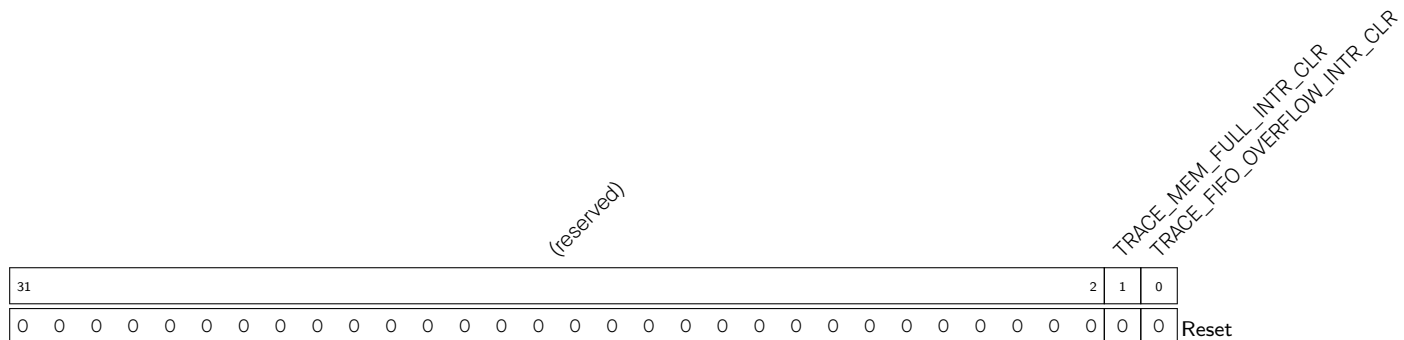
### Register 1.7. TRACE\_INTR\_RAW\_REG (0x0018)



**TRACE\_FIFO\_OVERFLOW\_INTR\_RAW** The raw interrupt status of TRACE\_FIFO\_OVERFLOW\_INTR.  
(RO)

|                                |   |
|--------------------------------|---|
| <b>TRACE_MEM_FULL_INTR_RAW</b> | The raw interrupt status of TRACE_MEM_FULL_INTR. (RO) |
|--------------------------------|---|

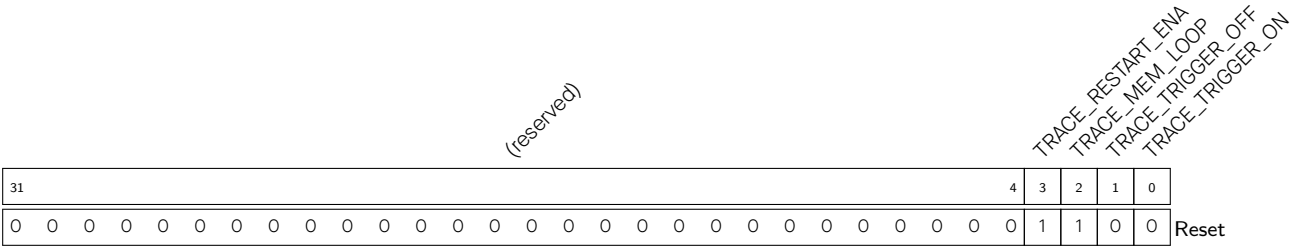
### Register 1.8. TRACE\_INTR\_CLR\_REG (0x001C)



**TRACE\_FIFO\_OVERFLOW\_INTR\_CLR** Write 1 to clear TRACE\_FIFO\_OVERFLOW\_INTR. (WT)

**TRACE\_MEM\_FULL\_INTR\_CLR** Write 1 to clear TRACE\_MEM\_FULL\_INTR. (WT)

Register 1.9. TRACE\_TRIGGER\_REG (0x0020)



- TRACE\_TRIGGER\_ON

Configures whether to enable the encoder.

0: Invalid

1: Enable

(WT)
- TRACE\_TRIGGER\_OFF

Configures whether to disable the encoder.

0: Invalid

1: Disable

(WT)
- TRACE\_MEM\_LOOP

Configures the memory writing mode.

0: Non-loop mode

1: Loop mode

(R/W)
- TRACE\_RESTART\_ENA

Configures whether to enable automatic restart.

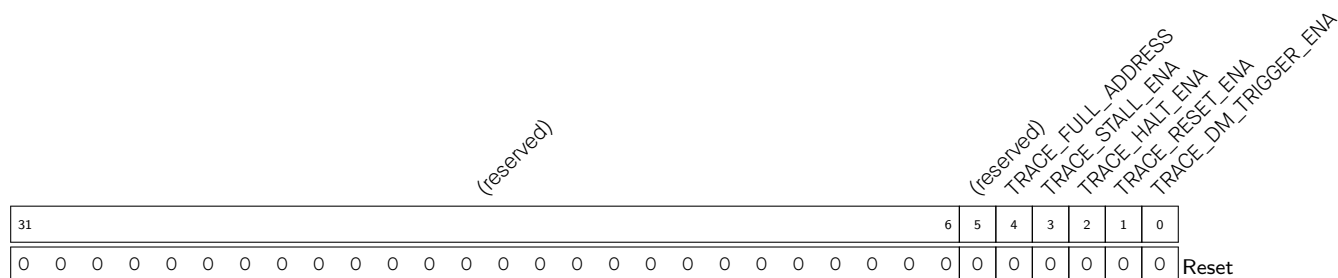
0: Disable

1: Enable

(R/W)



### Register 1.10. TRACE\_CONFIG\_REG (0x0024)



**TRACE\_DM\_TRIGGER\_ENA** Configure whether to enable the trigger signal.

0: Disable

1: Enable

(R/W)

**TRACE\_RESET\_ENA** Configures whether to enable the reset signal.

0: Disable

1: Enable

(R/W)

**TRACE\_HALT\_ENA** Configures whether to enable the halted signal.

0: Disable

1: Enable

(R/W)

**TRACE\_STALL\_ENA** Configures whether to enable the stall signal.

0: Disable

1: Enable

(R/W)

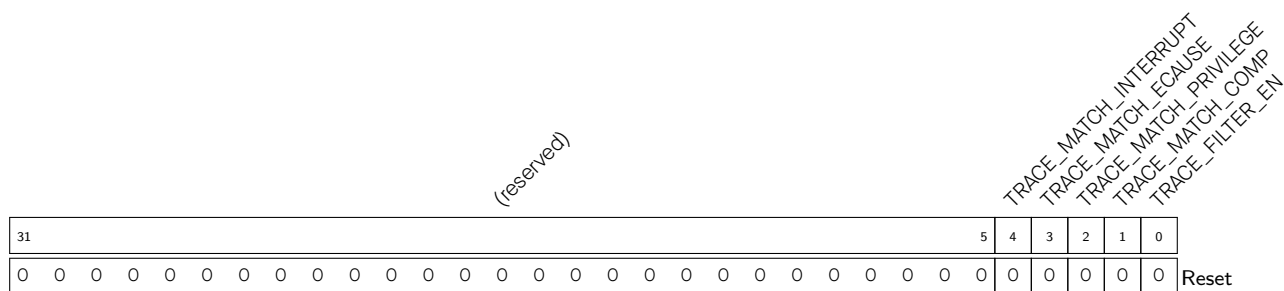
**TRACE\_FULL\_ADDRESS** Configure the address mode.

0: Delta address mode

### 1: Full address mode

(R/W)

### Register 1.11. TRACE\_FILTER\_CONTROL\_REG (0x0028)



**TRACE\_FILTER\_EN** Configure whether to enable filtering.

0: Disable

1: Enable

(R/W)

**TRACE\_MATCH\_COMP** Configures whether to enable the comparator match mode.

0: Disable

1: Enable

(R/W)

**TRACE\_MATCH\_PRIVILEGE** Configures whether to enable the privilege match mode.

0: Disable

1: Enable

(R/W)

**TRACE\_MATCH\_ECAUSE** Configures whether to enable the ecause match mode.

0: Disable

1: Enable

(R/W)

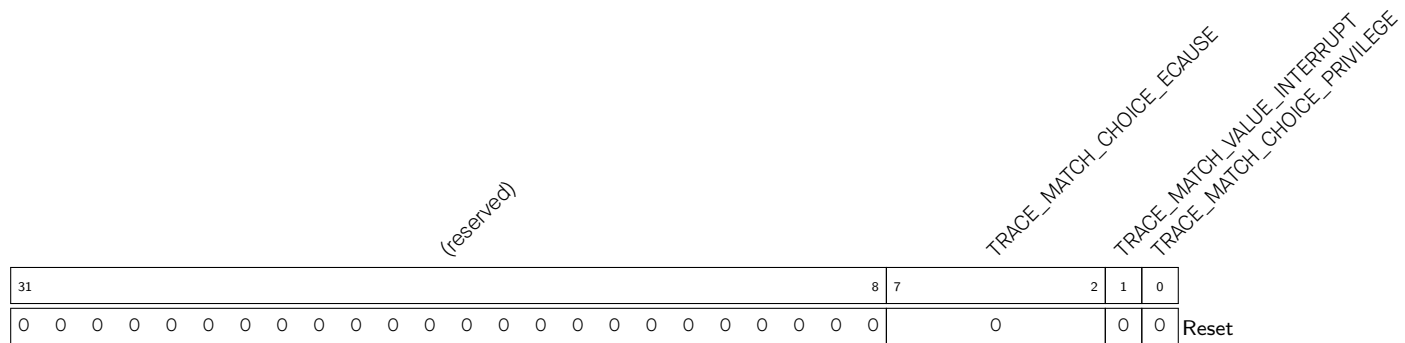
**TRACE\_MATCH\_INTERRUPT** Configures whether to enable the interrupt match mode.

0: Disable

1: Enable

(R/W)

### Register 1.12. TRACE\_FILTER\_MATCH\_CONTROL\_REG (0x002C)



**TRACE\_MATCH\_CHOICE\_PRIVILEGE** Configures the privilege level for matching.

0: User mode

## 1: Machine mode

(R/W)

**TRACE\_MATCH\_VALUE\_INTERRUPT** Configures the interrupt level for matching. Valid only when

TRACE\_MATCH\_INTERRUPT is set.

0: itype=1

1: itype=2

(R/W)

**TRACE\_MATCH\_CHOICE\_ECAUSE** Configures the ecause code for matching. (R/W)

**Register 1.13. TRACE\_FILTER\_COMPARATOR\_CONTROL\_REG (0x0030)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |       |            |    |                |    |                  |    |            |   |               |   |            |   |                |   |                  |   |            |  |               |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|-------|------------|----|----------------|----|------------------|----|------------|---|---------------|---|------------|---|----------------|---|------------------|---|------------|--|---------------|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TRACE_MATCH_MODE |       | (reserved) |    | TRACE_S_NOTIFY |    | TRACE_S_FUNCTION |    | (reserved) |   | TRACE_S_INPUT |   | (reserved) |   | TRACE_P_NOTIFY |   | TRACE_P_FUNCTION |   | (reserved) |  | TRACE_P_INPUT |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 18               | 17    | 16         | 15 | 14             | 13 | 12               | 10 |            | 9 | 8             | 7 | 6          | 5 | 4              | 2 |                  | 1 | 0          |  |               |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                | 0 0 0 |            | 0  |                | 0  |                  | 0  | 0          | 0 | 0             | 0 | 0          |   | 0 0 0          |   | Reset            |   |            |  |               |  |

**TRACE\_P\_INPUT** Configures the input of the primary comparator for matching.

0: iaddr

1: tval

(R/W)

**TRACE\_P\_FUNCTION** Configures the function for the primary comparator.

0: Equal

1: Not equal

2: Less than

3: Less than or equal

4: Greater than

5: Greater than or equal

Others: Always match

(R/W)

**TRACE\_P\_NOTIFY** Configures whether to explicitly report an instruction address matched against the primary comparator.

0: Not report

1: Report

(R/W)

**TRACE\_S\_INPUT** Configures the input of the secondary comparator for matching.

0: iaddr

1: tval

(R/W)

**TRACE\_S\_FUNCTION** Configures the function of for secondary comparator.

0: Equal

1: Not equal

2: Less than

3: Less than or equal

4: Greater than

5: Greater than or equal

6: The second comparator value is the masked value of the primary comparator

Others: Always match

(R/W)

Continued on the next page...

**Register 1.13. TRACE\_FILTER\_COMPARATOR\_CONTROL\_REG (0x0030)**

Continued from the previous page...

**TRACE\_S\_NOTIFY** Configures whether to explicitly report an instruction address matched against the secondary comparator.

0: Not report

1: Report

(R/W)

**TRACE\_MATCH\_MODE** Configures the comparator match condition.

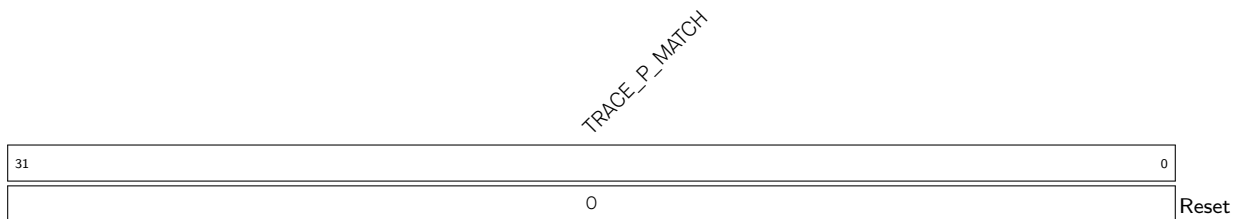
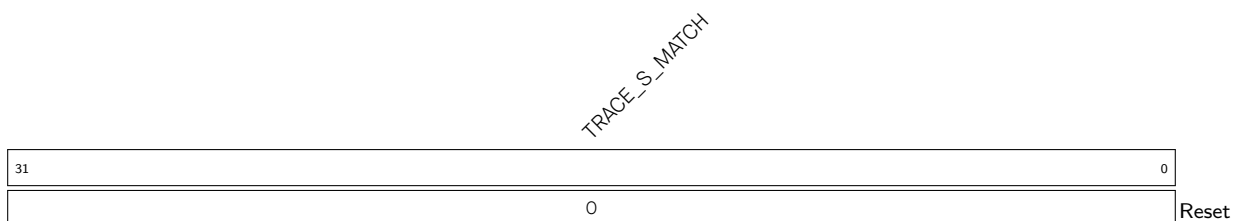
0: Only the primary comparator matches

1: Both primary and secondary comparators match (P&amp;&amp;S)

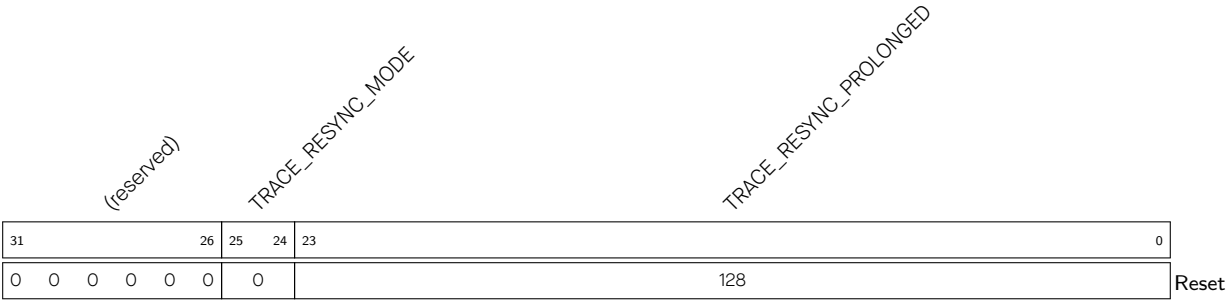
2: Neither primary nor secondary comparator match (!P&amp;&amp;S)

3: Start filtering when the primary comparator matches and stop filtering when the secondary comparator matches

(R/W)

**Register 1.14. TRACE\_FILTER\_P\_COMPARATOR\_MATCH\_REG (0x0034)****TRACE\_P\_MATCH** Configures the match value for the primary comparator. (R/W)**Register 1.15. TRACE\_FILTER\_S\_COMPARATOR\_MATCH\_REG (0x0038)****TRACE\_S\_MATCH** Configures the match value for the secondary comparator. (R/W)

Register 1.16. TRACE\_RESYNC\_PROLONGED\_REG (0x003C)

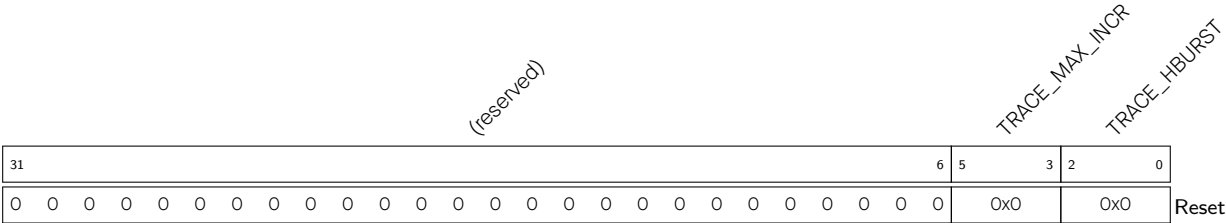


**TRACE\_RESYNC\_PROLONGED** Configures the threshold for the synchronization counter. (R/W)

**TRACE\_RESYNC\_MODE** Configures the synchronization mode.

- 0: Disable the synchronization counter
  - 1: Invalid
  - 2: Synchronization counter counts by packet
  - 3: Synchronization counter counts by cycle
- (R/W)

Register 1.17. TRACE\_AHB\_CONFIG\_REG (0x0040)



**TRACE\_HBURST** Configures the AHB burst mode.

- 0: SINGLE
  - 1: INCR (length not defined)
  - 2: INCR4
  - 4: INCR8
  - Others: Invalid
- (R/W)

**TRACE\_MAX\_INCR** Configures the maximum burst length for INCR mode. (R/W)

Register 1.18. TRACE\_CLOCK\_GATE\_REG (0x0044)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TRACE_CLK_EN |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0            |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 1 | Reset |

**TRACE\_CLK\_EN** Configures register clock gating. 0: Support clock only when the application writes registers to save power  
1: Always force the clock on for registers  
This bit doesn't affect register access  
(R/W)

Register 1.19. TRACE\_DATE\_REG (0x03FC)

|            |   |   |    |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|---|---|----|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |   |   |    | TRACE_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         |   |   | 28 | 27         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0 | 0 | 0  | 0x2211300  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**TRACE\_DATE** Version control register. (R/W)

## Chapter 2

## Low-Power CPU

### 2.1 Overview

The ESP32-P4 Low-Power CPU (LP CPU) is a 32-bit processor based upon RISC-V ISA comprising integer (I), multiplication/division (M), atomic (A), and compressed (C) standard extensions. It features ultra-low power consumption and has a 2-stage, in-order, and scalar pipeline. The LP CPU core complex has an interrupt controller (INTC), a debug module (DM), and system bus (SYS BUS) interfaces for memory and peripheral access.

The LP CPU is in sleep mode by default (see Section 2.10). It can stay powered on when the chip enters Deep-sleep mode (see Chapter 13 *Low-Power Management* for details) and can access most peripherals and memories (see Chapter 6 *System and Memory* for details). It has two application scenarios:

- Power insensitive scenario: When the High-Performance CPU (HP CPU) is active, the LP CPU can assist the it with some speed- and efficiency-insensitive controls and computations.
- Power sensitive scenario: When the HP CPU is in the power-down state to save power, the LP CPU can be woken up to handle some external wake-up events.

Figure 2.1-1 shows the resources accessible to the HP CPU and the LP CPU.

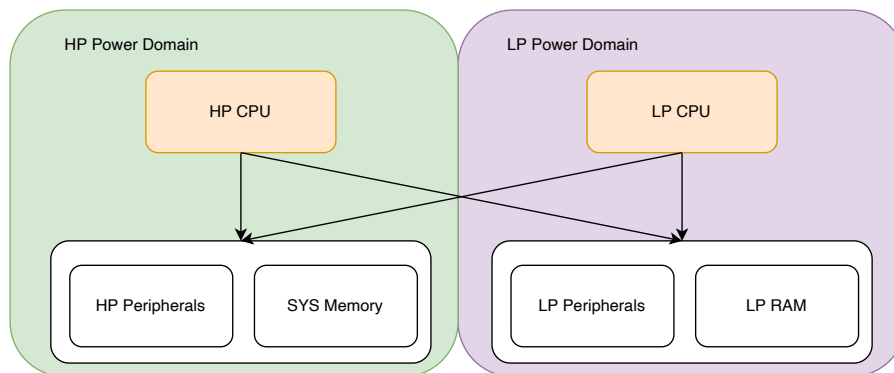


Figure 2.1-1. LP CPU Overview

In the figure above, the HP Power Domain and LP Power Domain can be powered on and off independently. When one domain is powered down, the CPU of the other domain cannot access the resources of that domain. In other words, only when the domain is powered on can its resources be accessed. For more information about power, please refer to the chapter 13 *Low-Power Management*.

### 2.2 Features

The LP CPU has the following features:



- Operating clock frequency of up to 40 MHz
- 18 vector interrupts
- Debug module compliant with RISC-V External Debug Support Version 0.13 with external debugger support over an industry-standard JTAG/USB port
- Hardware trigger compliant with RISC-V External Debug Support Version 0.13 with up to 2 breakpoints/watchpoints
- Core performance metric events
- Wake-up interrupt for HP CPU
- Access to HP memory and LP memory
- Access to the entire peripheral address space

## 2.3 Configuration and Status Registers (CSRs)

### 2.3.1 Register Summary

Below is a list of CSRs that are supported by the LP CPU. Except for the custom performance counter CSRs, all the implemented CSRs follow the standard mapping of bit fields as described in the RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10. It must be noted that even among the standard CSRs, not all bit fields have been implemented, limited by the subset of features implemented in the CPU. For a detailed description of the subset of fields implemented under each of these CSRs, please refer to Section 2.3.2.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description                  | Address | Access |
|---|------------------------------|---------|--------|
| <b>Machine Information CSR</b>                      |                              |         |        |
| <a href="#">mhartid</a>                             | Machine Hart ID              | 0xF14   | RO     |
| <b>Machine Trap Setup CSRs</b>                      |                              |         |        |
| <a href="#">mstatus</a>                             | Machine Mode Status          | 0x300   | R/W    |
| <a href="#">misa</a> <sup>1</sup>                   | Machine ISA                  | 0x301   | R/W    |
| <a href="#">mie</a>                                 | Machine Interrupt Enable     | 0x304   | R/W    |
| <a href="#">mtvec</a> <sup>2</sup>                  | Machine Trap Vector          | 0x305   | R/W    |
| <b>Machine Trap Handling CSRs</b>                   |                              |         |        |
| <a href="#">mscratch</a>                            | Machine Scratch              | 0x340   | R/W    |
| <a href="#">mepc</a>                                | Machine Trap Program Counter | 0x341   | R/W    |
| <a href="#">mcause</a> <sup>3</sup>                 | Machine Trap Cause           | 0x342   | R/W    |
| <a href="#">mtval</a>                               | Machine Trap Value           | 0x343   | R/W    |
| <a href="#">mip</a>                                 | Machine Interrupt Pending    | 0x344   | R/W    |
| <b>Trigger Module CSRs (shared with Debug Mode)</b> |                              |         |        |
| <a href="#">tselect</a>                             | Trigger Select Register      | 0x7A0   | R/W    |

<sup>1</sup>Although [misa](#) is specified as having both read and write access (R/W), its fields are hardwired and thus write has no effect. This is what would be termed WARL (Write Any Read Legal) in RISC-V terminology.

<sup>2</sup>[mtvec](#) only provides configuration for trap handling in vectored mode with the base address aligned to 256 bytes.

<sup>3</sup>External interrupt IDs reflected in [mcause](#) include even those IDs which have been reserved by RISC-V standard for core internal sources.

| Name                                     | Description   | Address    | Access |
|--|---|------------|--------|
| <a href="#">tdata1</a>                   | Trigger Abstract Data 1                                       | 0x7A1      | R/W    |
| <a href="#">tdata2</a>                   | Trigger Abstract Data 2                                       | 0x7A2      | R/W    |
| <b>Debug Mode CSRs</b>                   |   |            |        |
| <a href="#">dcsr</a>                     | Debug Control and Status                                      | 0x7B0      | R/W    |
| <a href="#">dpc</a>                      | Debug PC  | 0x7B1      | R/W    |
| <a href="#">dscratch0</a>                | Debug Scratch Register 0                                      | 0x7B2      | R/W    |
| <a href="#">dscratch1</a>                | Debug Scratch Register 1                                      | 0x7B3      | R/W    |
| <b>Machine Counter/Timer CSRs</b>        |   |            |        |
| <a href="#">mcycle</a>                   | Machine Clock Cycle Counter                                   | 0xB00      | R/W    |
| <a href="#">minstret</a>                 | Machine Retired Instruction Counter                           | 0xB02      | R/W    |
| <a href="#">mhpmcounter</a> $n(n:3-12)$  | Machine Performance Monitor Counter                           | 0xB00+ $n$ | R/W    |
| <a href="#">mcycleh</a>                  | The higher 32 bits of <a href="#">mcycle</a>                  | 0xB80      | R/W    |
| <a href="#">minstreth</a>                | The higher 32 bits of <a href="#">minstret</a>                | 0xB82      | R/W    |
| <a href="#">mhpmcounter</a> $nh(n:3-12)$ | The higher 32 bits of <a href="#">mhpmcounter</a> $n(n:3-12)$ | 0xB80+ $n$ | R/W    |
| <b>Machine Counter Setup CSR</b>         |   |            |        |
| <a href="#">mcountinhibit</a>            | Machine Counter Control                                       | 0x320      | R/W    |

Note that if write, set, or clear operation is attempted on any of the read-only (RO) CSRs indicated in the above table, the CPU will generate an illegal instruction exception.

## 2.3.2 Registers

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 2.1. mhartid (0xF14)**

|            |   |
|------------|---|
| MHARTID    |   |
| 31         | 0 |
| 0x00000000 |   |
| Reset      |   |

**MHARTID** Represents hart ID. The LP CPU hart ID is 0. (RO)

**Register 2.2. mstatus (0x300)**

|            |  |  |  |            |      |    |    |            |     |  |  |     |     |    |    |            |   |     |  |      |   |   |     |            |  |  |       |     |   |  |  |            |  |   |  |
|------------|--|--|--|------------|------|----|----|------------|-----|--|--|-----|-----|----|----|------------|---|-----|--|------|---|---|-----|------------|--|--|-------|-----|---|--|--|------------|--|---|--|
| (reserved) |  |  |  | (reserved) |      |    |    | (reserved) |     |  |  | MPP |     |    |    | (reserved) |   |     |  | MPIE |   |   |     | (reserved) |  |  |       | MIE |   |  |  | (reserved) |  |   |  |
| 31         |  |  |  |            | 22   | 21 | 20 |            |     |  |  | 13  | 12  | 11 | 10 |            |   |     |  | 8    | 7 | 6 |     |            |  |  | 4     | 3   | 2 |  |  |            |  | 0 |  |
| 0x000      |  |  |  | 0          | 0x00 |    |    |            | 0x0 |  |  |     | 0x0 |    |    |            | 0 | 0x0 |  |      |   | 0 | 0x0 |            |  |  | Reset |     |   |  |  |            |  |   |  |

**MIE** Write 1 to enable the global machine mode interrupt. (R/W)

**MPIE** Write 1 to enable the machine previous interrupt (before trap). (R/W)

**MPP** Configures machine previous privilege mode (before trap).

0x3: Machine mode

Other values: Invalid

Note: Only the lower bit is writable. Any write to the higher bit is ignored as it is directly tied to the lower bit.

(R/W)

Register 2.3. misa (0x301)

| MXL |    | (reserved) |    |    |    | Z  | Y  | X  | W  | V  | U  | T  | S  | R  | Q  | P  | O  | N  | M  | L  | K  | J | I | H | G | F | E | D | C | B | A |
|-----|----|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31  | 30 | 29         | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x1 |    | 0x0        |    |    |    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |

Reset

**MXL** Machine XLEN = 1 (32-bit). (RO)**Z** Reserved = 0. (RO)**Y** Reserved = 0. (RO)**X** Non-standard extensions present = 0. (RO)**W** Reserved = 0. (RO)**V** Reserved = 0. (RO)**U** User mode implemented = 0. (RO)**T** Reserved = 0. (RO)**S** Supervisor mode implemented = 0. (RO)**R** Reserved = 0. (RO)**Q** Quad-precision floating-point extension = 0. (RO)**P** Reserved = 0. (RO)**O** Reserved = 0. (RO)**N** User-level interrupts supported = 0. (RO)**M** Integer Multiply/Divide extension = 1. (RO)**L** Reserved = 0. (RO)**K** Reserved = 0. (RO)**J** Reserved = 0. (RO)**I** RV32I base ISA = 1. (RO)**H** Hypervisor extension = 0. (RO)**G** Additional standard extensions present = 0. (RO)**F** Single-precision floating-point extension = 0. (RO)**E** RV32E base ISA = 0. (RO)**D** Double-precision floating-point extension = 0. (RO)**C** Compressed Extension = 1. (RO)**B** Reserved = 0. (RO)**A** Atomic Standard Extension = 1. (RO)

**Register 2.4. mie (0x304)**

| (reserved)<br>HP_IE<br>LP_RTC_IE<br>LP_WDT_IE<br>LP_TIMER_IE<br>MB_LP_IE<br>PMU_LP_IE<br>LP_ANAPERI_IE<br>LP_SYSREG_IE<br>LP_EFUSE_IE<br>LP_TSENS_IE<br>LP_TOUCH_IE<br>LP_ADC_IE<br>LP_GPIO_IE<br>LP_I2C_IE<br>(reserved) |     |     |     |     |     |     |     |     |     |     |     |     |     |     | (reserved) |    | LP_SPI_IE |  | (reserved) |     | LP_UART_IE |     | (reserved) |   | LP_SW_IE |     | (reserved) |     |     |  |  |       |
|---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|------------|----|-----------|--|------------|-----|------------|-----|------------|---|----------|-----|------------|-----|-----|--|--|-------|
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16         | 15 | 12        |  | 11         | 10  | 8          |     | 7          | 6 | 4        |     | 3          | 2   | 0   |  |  |       |
| 0x0   | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | 0x0        |    | 0x0       |  | 0x0        | 0x0 |            | 0x0 | 0x0        |   | 0x0      | 0x0 |            | 0x0 | 0x0 |  |  |       |
|   |     |     |     |     |     |     |     |     |     |     |     |     |     |     |            |    |           |  |            |     |            |     |            |   |          |     |            |     |     |  |  | Reset |

**LP\_SW\_IE** Write 1 to enable LP software interrupt. (R/W)

**LP\_UART\_IE** Write 1 to enable LP UART interrupt. (R/W)

**LP\_SPI\_IE** Write 1 to enable LP SPI interrupt. (R/W)

**LP\_I2C\_IE** Write 1 to enable I2C interrupt. (R/W)

**LP\_GPIO\_IE** Write 1 to enable LP GPIO interrupt. (R/W)

**LP\_ADC\_IE** Write 1 to enable LP ADC interrupt. (R/W)

**LP\_TOUCH\_IE** Write 1 to enable LP TOUCH interrupt. (R/W)

**LP\_TSENS\_IE** Write 1 to enable LP TSENS interrupt. (R/W)

**LP\_EFUSE\_IE** Write 1 to enable LP eFuse interrupt. (R/W)

**LP\_SYSREG\_IE** Write 1 to enable SYSREG interrupt. (R/W)

**LP\_ANAPERI\_IE** Write 1 to enable ANAPERI interrupt. (R/W)

**LP\_PMU\_IE** Write 1 to enable PMU interrupt. (R/W)

**LP\_MB\_IE** Write 1 to enable Mailbox interrupt. (R/W)

**LP\_TIMER\_IE** Write 1 to enable LP Timer interrupt. (R/W)

**LP\_WDT\_IE** Write 1 to enable WDT interrupt. (R/W)

**LP\_RTC\_IE** Write 1 to enable RTC interrupt. (R/W)

**HP\_IE** Write 1 to enable HP interrupt. (R/W)

**Register 2.5. mtvec (0x305)**

|          |   |   |   |   |   |  |  |            |  |  |  |      |  |       |
|----------|---|---|---|---|---|--|--|------------|--|--|--|------|--|-------|
| BASE     |   |   |   |   |   |  |  | (reserved) |  |  |  | MODE |  |       |
| 31       | 8 | 7 | 2 | 1 | 0 |  |  |            |  |  |  |      |  |       |
| 0x000000 |   |   |   |   |   |  |  | 0x00       |  |  |  | 0x1  |  | Reset |

**MODE** Represents whether machine mode interrupts are vectored. Only vectored mode **0x1** is available. (RO)

**BASE** Configures the higher 24 bits of trap vector base address aligned to 256 bytes. (R/W)

**Register 2.6. mscratch (0x340)**

|                 |   |
|-----------------|---|
| <i>MSCRATCH</i> |   |
| 31              | 0 |
| 0x00000000      |   |
| Reset           |   |

**MSCRATCH** Contains machine scratch information for custom use. (R/W)

**Register 2.7. mepc (0x341)**

|             |   |
|-------------|---|
| <i>MEPC</i> |   |
| 31          | 0 |
| 0x00000000  |   |
| Reset       |   |

**MEPC** Configures the machine trap/exception program counter. This is automatically updated with address of the instruction which was about to be executed while CPU encountered the most recent trap. (R/W)

**Register 2.8. mcause (0x342)**

|                |            |            |   |                |       |
|----------------|------------|------------|---|----------------|-------|
| Interrupt Flag |            | (reserved) |   | Exception Code |       |
| 31             | 30         | 5          | 4 | 0              |       |
| 0              | 0x00000000 |            |   | 0x00           |       |
|                |            |            |   |                | Reset |

**Exception Code** This field is automatically updated with unique ID of the most recent exception or interrupt due to which CPU entered trap. Possible exception IDs are:

0x2: Illegal instruction

0x3: Hardware breakpoint/watchpoint or EBREAK

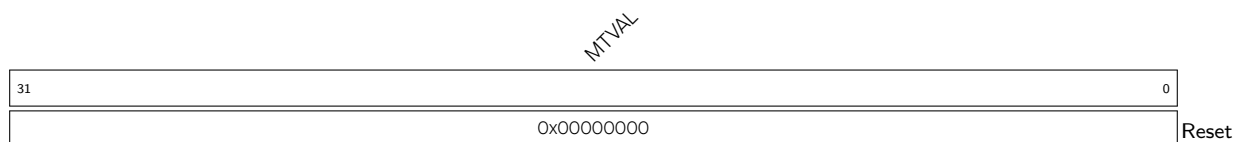
0x6: Misaligned atomic instructions

Note: Exception ID 0x0 (instruction access misaligned) is not present because CPU always masks the lowest bit of the address during instruction fetch.

(R/W)

**Interrupt Flag** This flag is automatically updated when CPU enters trap. If this is found to be set, it indicates that the latest trap occurred due to an interrupt. For exceptions it remains unset.

(R/W)

**Register 2.9. mtval (0x343)**

**MTVAL** Configures machine trap value. This is automatically updated with an exception dependent data which may be useful for handling that exception. Data is to be interpreted depending upon exception IDs:

0x1: Faulting address of instruction

0x2: Faulting instruction opcode

0x5: Faulting data address of load operation

0x7: Faulting data address of store operation

Note: The value of this register is not valid for other exception IDs and interrupts.

(R/W)

Register 2.10. mip (0x344)

|            |     |       |     |           |     |           |     |             |     |          |     |        |     |     |     |            |  |              |     |             |     |             |     |             |     |           |     |            |     |           |  |            |  |            |  |           |  |            |  |            |  |            |  |          |  |            |  |
|------------|-----|-------|-----|-----------|-----|-----------|-----|-------------|-----|----------|-----|--------|-----|-----|-----|------------|--|--------------|-----|-------------|-----|-------------|-----|-------------|-----|-----------|-----|------------|-----|-----------|--|------------|--|------------|--|-----------|--|------------|--|------------|--|------------|--|----------|--|------------|--|
| (reserved) |     | HP_IP |     | LP_RTC_IP |     | LP_WDT_IP |     | LP_TIMER_IP |     | MB_LP_IP |     | PMU_IP |     | LP  |     | ANAPERL_IP |  | LP_SYSREG_IP |     | LP_EFUSE_IP |     | LP_TSENS_IP |     | LP_TOUCH_IP |     | LP_ADC_IP |     | LP_GPIO_IP |     | LP_I2C_IP |  | (reserved) |  | (reserved) |  | LP_SPI_IP |  | (reserved) |  | LP_UART_IP |  | (reserved) |  | LP_SW_IP |  | (reserved) |  |
| 31         | 30  | 29    | 28  | 27        | 26  | 25        | 24  | 23          | 22  | 21       | 20  | 19     | 18  | 17  | 16  | 15         |  |              | 12  | 11          | 10  | 8           |     | 7           | 6   | 4         |     | 3          | 2   | 0         |  |            |  |            |  |           |  |            |  |            |  |            |  |          |  |            |  |
| 0x0        | 0x0 | 0x0   | 0x0 | 0x0       | 0x0 | 0x0       | 0x0 | 0x0         | 0x0 | 0x0      | 0x0 | 0x0    | 0x0 | 0x0 | 0x0 | 0x0        |  | 0x0          | 0x0 | 0x0         | 0x0 | 0x0         | 0x0 | 0x0         | 0x0 | 0x0       | 0x0 | 0x0        | 0x0 | Reset     |  |            |  |            |  |           |  |            |  |            |  |            |  |          |  |            |  |

Reset

**LP\_SW\_IP** Configures the pending status of the LP software interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_UART\_IP** Configures the pending status of the LP UART interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_SPI\_IP** Configures the pending status of the LP SPI interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_I2C\_IP** Configures the pending status of the LP I2C interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_GPIO\_IP** Configures the pending status of the LP GPIO interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_ADC\_IP** Configures the pending status of the LP ADC interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_TOUCH\_IP** Configures the pending status of the LP TOUCH interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_TSENS\_IP** Configures the pending status of the LP TSENS interrupt.

0 Not pending

1 Pending

(R/W)

**LP\_EFUSE\_IP** Configures the pending status of the LP eFuse interrupt.

0 Not pending

1 Pending

(R/W)

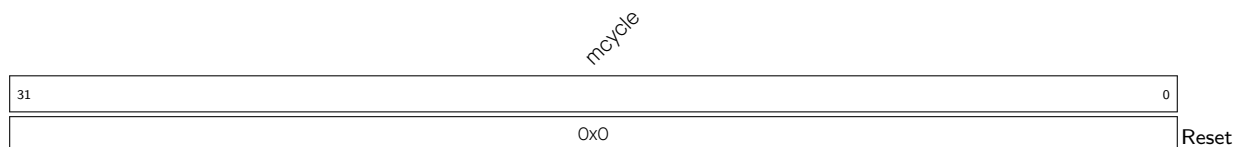
**LP\_SYSREG\_IP** Configures the pending status of the LP SYSREG interrupt.

0 Not pending

1 Pending

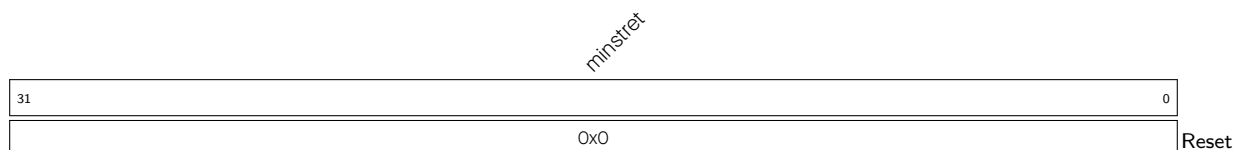


## Register 2.11. mcycle (0xB00)

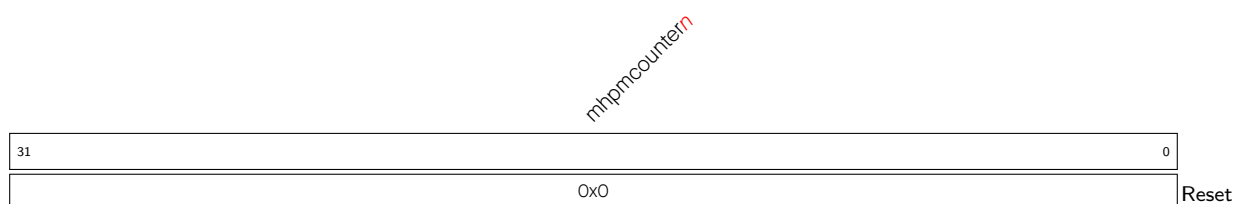


**MCYCLE** Configures the lower 32 bits of the clock cycle counter. (R/W)

## Register 2.12. minstret (0xB02)

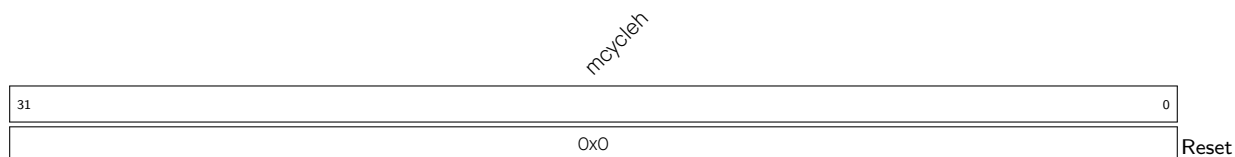


**MINSTRET** Configures the lower 32 bits of the instruction counter. (R/W)

Register 2.13. mhpmpcounter<sub>*n*</sub> (*n*: 3-12) (0xB00+*n*)

**MHPMCOUNTER<sub>*n*</sub>** Configures the lower 32 bits of the performance counter *n*. (R/W)

## Register 2.14. mcycleh (0xB80)



**MCYCLEH** Configures the higher 32 bits of the clock cycle counter. (R/W)

Register 2.15. minstreth (0xB82)

|           |   |
|-----------|---|
| minstreth |   |
| 31        | 0 |
| 0x0       |   |
| Reset     |   |

**MINSTRETH** Configures the higher 32 bits of the instruction counter. (R/W)

Register 2.16. mhpmpcounter $n$ ( $n$ : 3-12)h (0xB80+ $n$ )

|                  |   |
|------------------|---|
| mhpmpcounter $n$ |   |
| 31               | 0 |
| 0x0              |   |
| Reset            |   |

**MHPMCOUNTER $n$ h** Configures the higher 32 bits of the performance counter  $n$ . (R/W)

Register 2.17. mcountinhibit (0x320)

|     |   |                     |     |     |
|-----|---|---------------------|-----|-----|
| HPM |   | IR (reserved)<br>CY |     |     |
|     |   | 3                   | 2   | 1 0 |
| 31  | 0 | 0x0                 | 0x0 | 0x0 |
| 0x0 |   | Reset               |     |     |

**HPM** Configures whether the performance counter  $n$ ( $n$ :3-12) increments.

0: The counter does not count

1: The counter increments

(R/W)

**IR** Configure whether the instruction counter increments.

0: The counter does not count

1: The counter increments

(R/W)

**CY** Configure whether the clock cycle counter increments.

0: The counter does not count

1: The counter increments

(R/W)

## 2.4 Interrupts and Exceptions

The LP CPU handles interrupts and exceptions according to RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10. After entering an interrupt/exception handler, the CPU:

- Saves the current program counter (PC) value to the [mepc](#) CSR
- Copies the state of [MIE](#) of [mstatus](#) to [MPIE](#) of [mstatus](#)
- Saves the current privileged mode to [MPP](#) of [mstatus](#)
- Clears [MIE](#) of [mstatus](#)
- Toggles the privileged mode to machine mode (M mode)
- Jumps to the handler address
  - For exceptions, the handler address is the base address of the vector table in the [mtvec](#) CSR
  - For interrupts, the handler address is  $mtvec + 4 * ID$ , where ID is the interrupt ID. For more information, see Section 2.4.1
- After the mret instruction is executed, the core jumps to the PC saved in the [mepc](#) CSR, restores the value of [MPIE](#) of [mstatus](#) to [MIE](#) of [mstatus](#), and restores the privileged mode to that indicated by [MPP](#) of [mstatus](#)

When the core starts up, the base address of the vector table is initialized to the boot address 0x50000000. After startup, the base address can be changed by writing to the [mtvec](#) CSR. For more information about CSRs, see Section 2.3.1.

After a reset, the core starts to fetch instructions from the memory address specified by the LP\_SYS\_LP\_CORE\_BOOT\_ADDR\_REG register with an offset of 0x80. The default value for this register is 0x50100000, which corresponds to the starting address of the LP ROM.

### 2.4.1 Interrupts

The LP CPU in the ESP32-P4 supports 18 interrupt inputs. Each interrupt corresponds to an ID, which is denoted as *n* (where *n* = 3, 7, 11, 16 to 30), and has a specific entry address of  $mtvec + 4 * n$ . These interrupts are associated with specific peripheral sources. For the mapping between peripheral sources and interrupt IDs, please refer to 2.4-1.

**Table 2.4-1. LP CPU Interrupt Mapping**

| Interrupt ID | Peripheral Source |
|--------------|-------------------|
| 3            | LP_SW_INTR        |
| 7            | LP_UART_INTR      |
| 11           | LP_SPI_INTR       |
| 17           | LP_I2C_INTR       |
| 18           | LP_GPIO_INTR      |
| 19           | LP_ADC_INTR       |
| 20           | LP_TOUCH_INTR     |
| 21           | LP_TSENS_INTR     |
| 22           | LP_EFUSE_INTR     |

| Interrupt ID | Peripheral Source                        |
|--------------|--|
| 23           | LP_SYSREG_INTR                           |
| 24           | LP_ANAPERI_INTR                          |
| 25           | PMU_REG_O_INTR, PMU_REG_1_INTR           |
| 26           | MB_HP_INTR, MB_LP_INTR                   |
| 27           | LP_TIMER_REG_O_INTR, LP_TIMER_REG_1_INTR |
| 28           | LP_WDT_INTR                              |
| 29           | LP_RTC_INTR                              |
| 30           | HP_INTR                                  |

The read-only register LPINTR\_STATUS\_REG indicates the current status of the LP CPU external interrupt sources. For the mapping between this register and the interrupt sources, please refer to the description of this register.

## 2.4.2 Interrupt Handling

By default, interrupts are disabled globally because the MIE bit in `mstatus` has a reset value of 0. Software must set this bit to enable global interrupts.

Assuming the interrupt to enable is Interrupt `n`:

1. Enable Interrupt `n`:
  - To enable interrupts globally, write 1 to the MIE bit of `mstatus`.
  - To enable Interrupt `n`, write 1 to the `n`th bit of `mie` CSR.
2. After Interrupt `n` is enabled, the LP CPU can respond to it. Meanwhile, the corresponding peripheral interrupt should be configured to send an interrupt signal to the LP CPU.
3. After the interrupt is triggered, the LP CPU jumps to the  $mtvec + 4 * n$  address.
4. To clear Interrupt `n`, the peripheral needs to clear the interrupt signal.

## 2.4.3 Exceptions

The LP CPU supports the RISC-V standard exceptions and can trigger the following exceptions:

**Table 2.4-2. LP CPU Exception Causes**

| Exception ID | Description                    |
|--------------|--------------------------------|
| 1            | Instruction access fault       |
| 2            | Illegal instructions           |
| 3            | Breakpoints (EBREAK)           |
| 5            | Load access fault              |
| 6            | Misaligned atomic instructions |
| 7            | Store access fault             |

## 2.5 Debugging

This section describes how to debug and test the LP CPU. Debug support is provided through standard JTAG pins and complies with RISC-V External Debug Support Version 0.13.

For ESP32-P4 system debugging overview, please refer to Chapter 1 *High-Performance CPU [to be added later]* > Figure 1.1 *Debug System Overview [to be added later]*.

The user interacts with the Debug Host (e.g., laptop), which is running a debugger (e.g., gdb). The debugger communicates with a Debug Translator (e.g., OpenOCD, which may include a hardware driver) to communicate with Debug Transport Hardware (e.g., ESP-Prog adapter). The Debug Transport Hardware connects the Debug Host to the CPU's Debug Transport Module (DTM) through a standard JTAG interface. The DTM provides access to the debug module (DM) using the Debug Module Interface (DMI).

ESP32-P4 features two DTMs interconnected in a daisy-chain configuration. Specifically, TAP0 connects to the HP CPU, while TAP1 is dedicated to the LP CPU.

The HP DM supports multicore debugging according to the specification RISC-V External Debug Support Version 0.13. It can simultaneously control both cores of the HP CPU. In contrast, the LP DM is designed for debugging the single-core LP CPU.

The LP CPU implements four registers for core debugging: [dcsr](#), [dpc](#), [dscratch0](#), and [dscratch1](#). All of those registers can only be accessed from debug mode. If software attempts to access them when the LP CPU is not in debug mode, an illegal instruction exception will be triggered.

### 2.5.1 Features

The Low-Power CPU debug module has the following debugging features:

- Access to necessary information about the implementation
- CPU core halt and resume
- Read and write of CPU core registers (including CSRs)
- CPU core reset
- CPU halted on software breakpoint (planted breakpoint instruction)
- Hardware single-stepping
- Two hardware triggers (which can be used as breakpoints/watchpoints). See Section 2.6 for details

### 2.5.2 Functional Description

The debugging mechanism adheres to the specification RISC-V External Debug Support Version 0.13. For a detailed description of the debugging features, refer to the specification.

According to the specification, a hart has the following states: nonexistent, unavail, running, and halted. By default, the LP CPU is in the unavail state. To connect the LP CPU for debugging, users need to clear that state by configuring the [LPPERI\\_CPU\\_REG](#) register.

## 2.5.3 Register Summary

The following table lists the debug CSRs supported for the LP CPU.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name                      | Description              | Address | Access |
|---------------------------|--------------------------|---------|--------|
| <a href="#">dcsr</a>      | Debug Control and Status | 0x7B0   | R/W    |
| <a href="#">dpc</a>       | Debug PC                 | 0x7B1   | R/W    |
| <a href="#">dscratch0</a> | Debug Scratch Register 0 | 0x7B2   | R/W    |
| <a href="#">dscratch1</a> | Debug Scratch Register 1 | 0x7B3   | R/W    |

All debug module registers are implemented in accordance with the specification RISC-V External Debug Support Version 0.13. For more information, refer to the specification.

## 2.5.4 Registers

The following is a detailed description of the debug CSR supported by the LP CPU.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 2.18. dcsr (0x7B0)

| xdebugver |   |   |   | (reserved) |   |   |   |    |   |   |   |   |   |   |   | ebreakm |   |   |   | (reserved) |   |    |   | ebreaku |   |    |   | (reserved) |   |   |   | cause |   |   |   | (reserved) |   |       |  | step |  | prv |  |   |  |
|-----------|---|---|---|------------|---|---|---|----|---|---|---|---|---|---|---|---------|---|---|---|------------|---|----|---|---------|---|----|---|------------|---|---|---|-------|---|---|---|------------|---|-------|--|------|--|-----|--|---|--|
| 31        |   |   |   | 28         |   |   |   | 27 |   |   |   |   |   |   |   | 16      |   |   |   | 15         |   | 14 |   | 13      |   | 12 |   | 11         |   | 9 |   | 8     |   | 6 |   | 5          |   | 3     |  | 2    |  | 1   |  | 0 |  |
| 0         | 1 | 0 | 0 | 0          | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0 | 0 | 0 | 0          | 0 | 0  | 0 | 0       | 0 | 0  | 0 | 0          | 0 | 0 | 0 | 0     | 0 | 0 | 0 | 1          | 1 | Reset |  |      |  |     |  |   |  |

**xdebugver** Represents the debug version.

4: External debug support exists  
(RO)

**ebreakm** Configures execution of the EBREAK instruction in machine mode.

0: Trigger an exception with mcause = 3  
1: Enter debug mode  
(R/W)

**ebreaku** Configures execution of the EBREAK instruction in user mode.

0: Trigger an exception with mcause = 3 as described in privileged mode  
1: Enter debug mode  
(R/W)

**cause** Represents the reason why debug mode was entered. When there are multiple reasons to enter debug mode in a single cycle, the cause with the highest priority number is the one written.

1: An EBREAK instruction was executed. (priority 3)  
2: The Trigger Module caused a halt. (priority 4)  
3: haltreq was set. (priority 2)  
4: The CPU core single stepped because step was set. (priority 1)  
Other values: reserved for future use  
(RO)

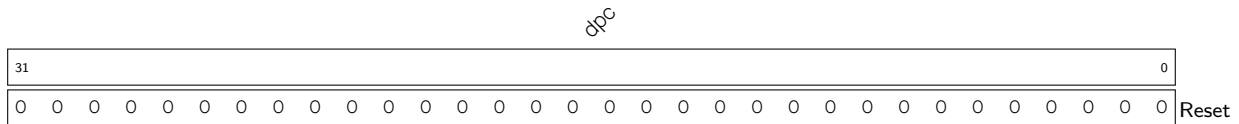
**step** When set and not in Debug Mode, the core will only execute a single instruction and then enter Debug Mode.

If the instruction does not complete due to an exception, the core will immediately enter Debug Mode before executing the trap handler, with appropriate exception registers set.

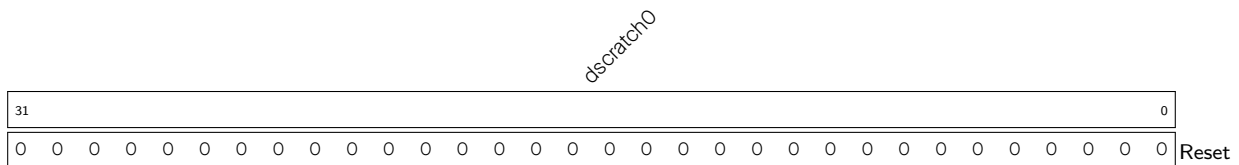
Setting this bit does not mask interrupts. This is a deviation from the RISC-V External Debug Support Specification Version 0.13.

(R/W)

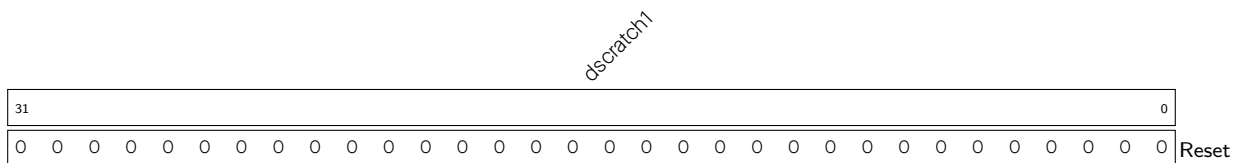
**prv** Contains the privilege level the core is operating in when debug mode is entered. A debugger can change this value to change the core's privilege level when exiting debug mode. Only **0x3** (machine mode) and **0x0** (user mode) are supported. (RO)

**Register 2.19. dpc (0x7B1)**

**dpc** Upon entry to debug mode, dpc is written with the address of the next instruction that will be executed. When resuming, the CPU core's PC is updated to the address stored in dpc. In debug mode, dpc can be modified. This field can be accessed in debug mode. (R/W)

**Register 2.20. dscratch0 (0x7B2)**

**dscratch0** Used by the debug module internally. (R/W)

**Register 2.21. dscratch1 (0x7B3)**

**dscratch1** Used by the debug module internally. (R/W)

## 2.6 Hardware Trigger

### 2.6.1 Features

Hardware Trigger module provides breakpoint and watchpoint capability for debugging. It has the following features:

- Two independent trigger units
- Configurable unit to match the address of the program counter
- Able to halt execution and transfer control to the debugger

### 2.6.2 Functional Description

The hardware trigger module provides three CSRs. See Section 2.6 for details. Among them, `tdata1` and `tdata2` are abstract CSRs, which means they are shadow registers for accessing internal registers in the trigger units, one at a time.



To select a specific trigger unit, the corresponding number (0-1) needs to be written to the [tselect](#) CSR. When a valid value is written, the abstract CSRs, [tdata1](#) and [tdata2](#), automatically match the internal registers of the trigger unit. Each trigger unit has two internal registers, namely [mcontrol](#) and [maddress](#), which are mapped to [tdata1](#) and [tdata2](#), respectively.

Writing a value more than 1 to [tselect](#) will set [tselect](#) to 1.

Since software or debugger may need to know the type of the selected trigger to correctly interpret [tdata1](#) and [tdata2](#), the 4-bit field (31-28) of [tdata1](#) encodes the type of the selected trigger. This type field is read-only and always provides a value of 0x2 for every trigger, which stands for support for address and data matching. Hence, it is inferred that [tdata1](#) and [tdata2](#) are to be interpreted as fields of [mcontrol](#) and [maddress](#), respectively. The specification RISC-V External Debug Support Version 0.13 provides information on other possible values, but the trigger module only supports the 0x2 type.

Once a trigger unit has been chosen by writing its index to [tselect](#), it will become possible to configure it by setting the appropriate bits in [mcontrol](#) CSR ([tdata1](#)) and writing the target address to [maddress](#) CSR ([tdata2](#)).

### 2.6.3 Trigger Execution Flow

When a hart is halted and enters debug mode due to the firing of a trigger ([action](#) = 1):

- [dpc](#) is set to the current PC in the decoding phase
- The cause field in [dcsr](#) is set to 2, which means halt due to trigger

### 2.6.4 Register Summary

Below is a list of Trigger Module CSRs supported by the CPU. These are only accessible from machine mode.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

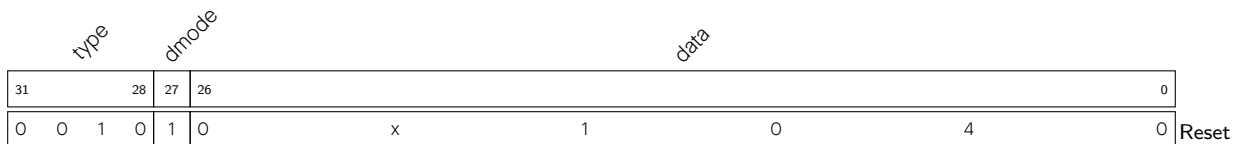
| Name                     | Description                            | Address | Access |
|--------------------------|--|---------|--------|
| <a href="#">tselect</a>  | Trigger Select Register                | 0x7A0   | R/W    |
| <a href="#">tdata1</a>   | Trigger Abstract Data 1                | 0x7A1   | R/W    |
| <a href="#">mcontrol</a> | <a href="#">tdata1</a> Shadow Register | 0x7A1   | R/W    |
| <a href="#">tdata2</a>   | Trigger Abstract Data 2                | 0x7A2   | R/W    |
| <a href="#">maddress</a> | <a href="#">tdata2</a> Shadow Register | 0x7A2   | R/W    |

### 2.6.5 Registers

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 2.22. tselect (0x7A0)**

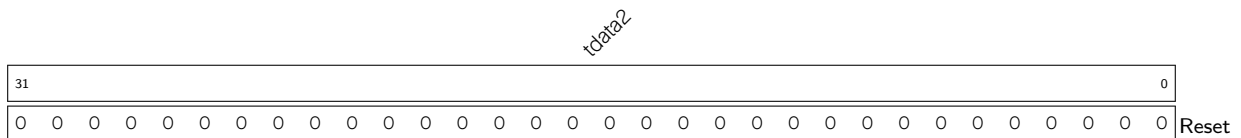
**tselect** Configures the index of the selected trigger unit. (R/W)

**Register 2.23. tdata1 (0x7A1)**

**type** Represents the trigger type. This field is reserved since only match type (0x2) triggers are supported. (RO)

**dmode** This is set to 1 if a trigger is being used by the debugger. This field is reserved since it is only supported in debug mode. (RO)

**data** Configures the abstract tdata1 content. This will always be interpreted as fields of [mcontrol](#) since only match type (0x2) triggers are supported. (R/W)

**Register 2.24. tdata2 (0x7A2)**

**tdata2** Configures the abstract tdata2 content. This will always be interpreted as [maddress](#) since only match type (0x2) triggers are supported. (R/W)

Register 2.25. mcontrol (0x7A1)

| (reserved) |    |    |    | dmode | maskmax |    |    |    | hit | select | timing | sizelo | action |    | chain | match | m | (reserved) |   |   | s | u | execute | store | load |  |  |
|------------|----|----|----|-------|---------|----|----|----|-----|--------|--------|--------|--------|----|-------|-------|---|------------|---|---|---|---|---------|-------|------|--|--|
| 31         | 28 | 27 | 26 |       |         | 21 | 20 | 19 | 18  | 17     | 16     | 15     |        | 12 | 11    | 10    |   | 7          | 6 | 5 | 4 | 3 | 2       | 1     | 0    |  |  |
| 0x2        |    |    |    | 0     | 0x0     |    |    |    | 0   | 0      | 0      | 0      | 0001   |    | 0     | 0     | 0 | 0          | 0 | 0 | 0 | 0 | 0       | 0     | 0    |  |  |
| Reset      |    |    |    |       |         |    |    |    |     |        |        |        |        |    |       |       |   |            |   |   |   |   |         |       |      |  |  |

Reset

**dmode** Same as [dmode](#) in [tdata1](#). (RO)

**maskmax** Represents the maximum NAPOT range.

0: A byte. Only exact match is supported.

Other values: Not supported.

(RO)

**hit** Not implemented in hardware. This field remains 0. (RO)

**select** Configures to select between an address match or a data match.

0: Perform a match on the virtual address

1: Perform a match on the data value loaded or stored, or the instruction executed

Note: Only address match is implemented. This field remains 0.

(RO)

**timing** Configures when the trigger will take action.

0: Take action before the instruction is executed

1: Take action after the instruction is executed

Note: The field remains 0.

(RO)

**sizelo** Only match of any size is supported. This field remains 0. (RO)

**action** Configure action of the selected trigger after it is triggered.

0x0: Cause a breakpoint exception

0x1: Enter debug mode (Valid only when dmode = 1)

Note: Only entering debug mode is supported. This field remains 1.

(RO)

**CHAIN** Not implemented in hardware. This field remains 0. (RO)

**match** Configures the trigger to perform the matching operation of the lower data/instruction address.

0x0: Exact match. Namely, the address corresponding to a certain byte during the access must exactly match the value of [maddress](#).

0x1: NAPOT match. Namely, at least one byte during the access is in the NAPOT region specified in [maddress](#).

Note: Only exact byte match is supported. This field remains 0.

(R/W)

**m** Set this field to make the selected trigger operate in machine mode. (RO)

**s** Set this field to make the selected trigger operate in supervisor mode. Operation in supervisor mode is not supported. This field is always 0. (RO)

Continued on the next page...

**Register 2.25. mcontrol (0x7A1)****Continued from the previous page...**

**u** Set this field to make the selected trigger operate in user mode. Operation in user mode is not supported. This field is always 0. (RO)

**execute** Configures whether to enable the selected trigger to match the virtual address of instructions.

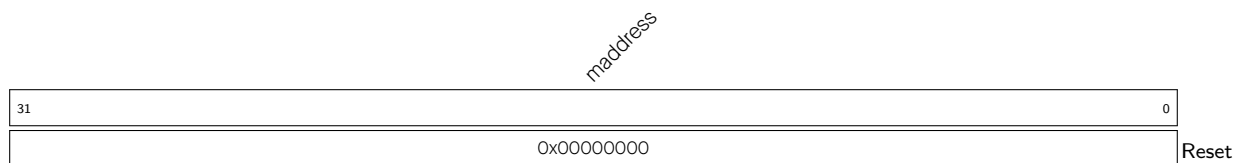
0: Not enable

1: Enable

(R/W)

**store** Set this field to make the selected trigger match the virtual address of the memory write operation. Not supported by hardware. This field is always 0. (RO)

**load** Set this field to make the selected trigger match the virtual address of a memory read operation. Not supported by hardware. This field is always 0. (RO)

**Register 2.26. maddress (0x7A2)**

**maddress** Configures the address used by the selected trigger when performing match operation. (R/W)

## 2.7 Performance Counter

The LP CPU implements one clock cycle counter [mcycle\(h\)](#), one instruction counter [minstret\(h\)](#), and ten event counters [mhpmcounter\(n:3-12\)](#). The clock cycle counter and instruction counter are always available and each is 64-bit wide. The performance counters are 40-bit wide each.

By default, all counters are enabled after reset. A counter can be enabled or disabled individually via the corresponding bit in the [mcountinhibit](#) CSR.

As shown in Table 2.7-1, each counter is dedicated to counting a particular event.

**Table 2.7-1. Performance Counter**

| Counter      | Counted Event                 |
|--------------|-------------------------------|
| mcycle       | Clock cycles                  |
| minstret     | The number of instructions    |
| mhpmcounter3 | Wait cycles for memory access |

| Counter       | Counted Event  |
|---------------|--|
| mhpmcounter4  | Wait cycles for fetching instructions  |
| mhpmcounter5  | The number of memory read operations. An unaligned read is counted as two.   |
| mhpmcounter6  | The number of memory write operations. An unaligned write is counted as two. |
| mhpmcounter7  | The number of unconditional jump instructions (jal, jr, jalr)                |
| mhpmcounter8  | The number of branch instructions  |
| mhpmcounter9  | The number of taken branch instructions                                      |
| mhpmcounter10 | The number of compressed instructions  |
| mhpmcounter11 | Wait cycles for multiplication instructions                                  |
| mhpmcounter12 | Wait cycles for division instructions  |

## 2.8 System Access

The LP CPU has access to both memory and peripherals. When accessing an illegal address, i.e., outside the memory's or peripherals' address space, it will trigger the corresponding access error exception based on the type of access.

### 2.8.1 Memory Access

The ESP32-P4 LP CPU can access LP ROM, LP SRAM, and L2 SRAM. For more information, please refer to Section 6 *System and Memory*.

- LP ROM: 16 KB region starting from 0x5010\_0000 to 0x5010\_3FFF. It is used for instruction fetch, data read, etc.
- LP SRAM: 32 KB region starting from 0x5010\_8000 ~ 0x5010\_FFFF. It is used for instruction fetch, data read, data write, etc.
- L2 SRAM: 768 KB region starting from 0x4FF0\_0000 to 0x4FFB\_FFFF. It is used for instruction fetch, data read, data write, etc.

**Note:**

The LP CPU experiences significant latency when accessing L2 SRAM, with each access taking approximately 20 LP CPU clock cycles. However, it can access LP ROM and LP SRAM with no latency.

The LP CPU supports the atomic instruction set. Both the LP CPU and the HP CPU can access memory through atomic instructions, thus achieving atomicity of memory access. For details on the atomic instruction set, please refer to RISC-V Instruction Set Manual Volume I: Unprivileged ISA, Version 2.2.

### 2.8.2 Peripheral Access

Table 6.3-2 in Chapter 6 *System and Memory* lists the peripherals accessible by the LP CPU and their base addresses.

## 2.9 Event Task Matrix Feature

The LP CPU on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows LP CPU's ETM tasks to be triggered by any peripherals' ETM events, or LP CPU's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to the LP CPU. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

LP CPU can receive the following ETM task:

- ULP\_TASK\_WAKEUP\_CPU: Wakes up the LP CPU.
- ULP\_TASK\_INT\_CPU: Triggers an LP CPU interrupt.

LP CPU can generate the following ETM events:

- ULP\_EVT\_ERR\_INTR: Indicates that an LP CPU exception occurs.
- ULP\_EVT\_START\_INTR: Indicates that the LP CPU clock is turned on.
- ULP\_EVT\_HALT: Indicates that the LP CPU enters the sleep state

## 2.10 Sleep and Wake-Up Process

### 2.10.1 Features

Here are the sleep and wake-up features supported by the LP CPU.

- Independent operation, sleeping, and waking-up in the low-power system when the HP CPU is sleeping
- Actively configuring registers to enter the sleep state based on software operating status
- Multiple wake-up sources
- Sleep entry rejection by peripherals

### 2.10.2 Process

The LP CPU is in sleep by default and its wake-up module follows the process below to wake it up for work and make it sleep.

To configure wake-up sources, please refer to Table [2.10-1](#).

The first startup of the LP CPU after power-up depends on the wake-up enable and wake-up source configuration by the HP CPU.

- Initialization of the LP CPU
  - Initialize the LP memory.
  - Start the LP CPU. Since the startup of the LP CPU depends on the wake-up process, it is recommended to use the [PMU\\_HP\\_TRIGGER\\_LP](#) register to start the initialization of the LP CPU in the following way:
    - \* Set [PMU\\_LP\\_CPU\\_WAKEUP\\_EN](#) to 0x400000
    - \* Set [PMU\\_HP\\_TRIGGER\\_LP](#) to 0x1

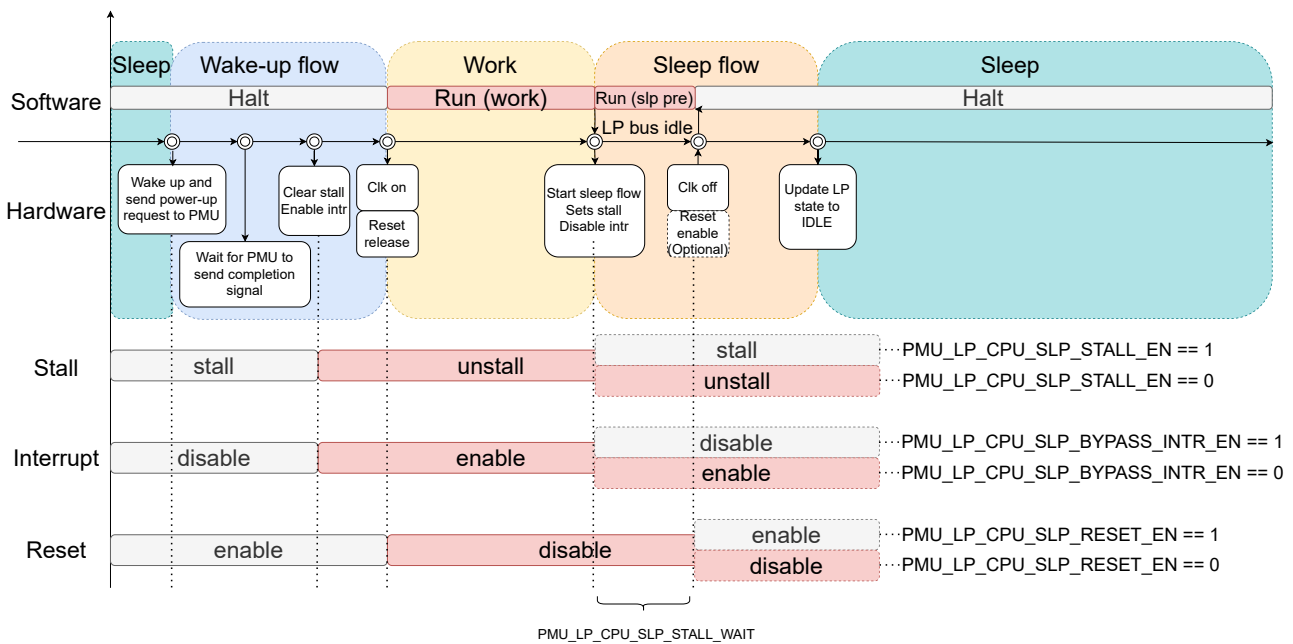


Figure 2.10-1. Wake-Up and Sleep Flow of LP CPU

\* The LP CPU will go through the wake-up process to start running

- Wake-up process:

- The wake-up module receives a wake-up signal and sends a power-up request to the PMU.
- If the current power consumption state (clock, power supply, etc.) meets the requirements of the LP CPU, the PMU will immediately reply with the completion signal. Otherwise, it will adjust the power consumption state before replying with the completion signal.
- The wake-up module disables the STALL state of the LP CPU and enables interrupt receiving.
- The wake-up module starts the clock, releases reset (ignore this step if reset is not enabled for sleep), and starts working.

- Sleep process:

- The LP CPU configures the `PMU_LP_CPU_SLEEP_REQ` register to enable the wake-up module to start the sleep process.
- If `PMU_LP_CPU_SLP_STALL_EN` is 1, the wake-up module enables the STALL state of the LP CPU. If it is 0, the module does not enable that state. If `PMU_LP_CPU_SLP_BYPASS_INTR_EN` is 1, the module masks all the LP CPU's interrupts. If it is 0, the module does not mask them.
- The wake-up module waits for `PMU_LP_CPU_SLP_STALL_WAIT` LP CPU clock cycles, and then turns off the LP CPU clock. If `PMU_LP_CPU_SLP_RESET_EN` is 1, the module enables reset of the LP CPU.
- The wake-up module changes the state of the LP CPU to IDLE and the PMU can enter a deeper level of sleep state.

## 2.10.3 Wake-Up Sources

Table 2.10-1. Wake Sources

| Register Value <sup>1</sup> | Wake-Up Source             | Description  |
|-----------------------------|----------------------------|--|
| BIT(9)                      | LP IO                      | The LP CPU can be waken up by the LP IO interrupt status register signal. For more information, please refer to Chapter 8 <i>GPIO Matrix and IO MUX</i> .  |
| BIT(10)                     | LP UART                    | The LP CPU can be waken up when the LP UART receives a certain number of RX pulses. REG_UART_WAKEUP_EN needs to be enabled. For more information, please refer to Chapter 37 <i>UART Controller (UART)</i> . |
| BIT(13)                     | RTC timer                  | The LP CPU can be waken up by the RTC timer target 0 timeout interrupt. For more information, please refer to Chapter 13 <i>Low-Power Management</i> .   |
| BIT(14)                     | Brownout detection         | The LP CPU can be waken up when a brownout occurs. For more information, please refer to Chapter 21 <i>Brown-out Detector</i> .  |
| BIT(17)                     | ETM                        | The LP CPU can be waken up by the ETM task. For more information, please refer to Chapter 12 <i>Event Task Matrix (ETM)</i> .  |
| BIT(18)                     | RTC timer                  | The LP CPU can be waken up by the RTC timer target 0 timeout interrupt. For more information, please refer to Chapter 13 <i>Low-Power Management</i> .   |
| BIT(19)                     | LP I2S audio               | The LP CPU can be waken up when the predefined audio is received via I2S. For more details, please refer to Chapter 41 <i>I2S Controller (I2S)</i> .   |
| BIT(22)                     | PMU_HP_TRIGGER_LP register | The HP CPU sets the register PMU_HP_TRIGGER_LP to wake up the LP CPU, and sets REG_HP_SW_TRIGGER_INT_CLR to clear this wake-up source.   |

<sup>1</sup> Value of the PMU\_LP\_CPU\_WAKEUP\_EN register

## 2.10.4 Sleep Rejection

When the LP CPU is preparing to enter the sleep state, it can be rejected by peripheral events. In other words, peripheral events have the capability to prevent the LP CPU from entering sleep mode. Below is the configuration process for the rejection:

1. The LP CPU configures PMU\_SLP\_REJECT\_EN to enable the functionality that allows peripherals to reject the LP CPU from entering the sleep mode.
2. The LP CPU configures PMU\_SLEEP\_REJECT\_ENA to enable the corresponding peripheral event to prevent the LP CPU from entering the sleep state.

The peripheral sources that can prevent the LP CPU from sleeping are the same as the wake-up sources.



## Part II

# System DMA

Focused on managing and transferring data within the system, this part explores controllers for Direct Memory Access (DMA), providing guidelines for efficient data movement supporting various peripherals and devices.

## Chapter 3

# GDMA Controller (GDMA-AHB, GDMA-AXI)

## 3.1 Overview

General Direct Memory Access (GDMA) is a feature that allows peripheral-to-memory, memory-to-peripheral, and memory-to-memory data transfer at high speed. The CPU is not involved in the GDMA transfer and therefore is more efficient with less workload.

ESP32-P4 has two types of general-purpose DMA controllers, namely GDMA-AHB and GDMA-AXI, to directly access the AHB bus or the AXI bus respectively. Both GDMA-AHB and GDMA-AXI have six independent channels, i.e., three transmit channels and three receive channels.

The GDMA-AHB channels are shared and can be assigned to I3C, UHCI, I2S, ADC, or RMT to access internal memory.

The GDMA-AXI channels are also shared and can be assigned to LCD, CAM, two general-purpose SPIs, PARLIO, AES, or SHA to access both internal and external memory.

GDMA-AHB and GDMA-AXI use configurable priority and weight arbitration schemes to manage peripherals' needs for bandwidth.

Unless otherwise specified, the term "GDMA controller" refers to both GDMA-AHB and GDMA-AXI in the following text.

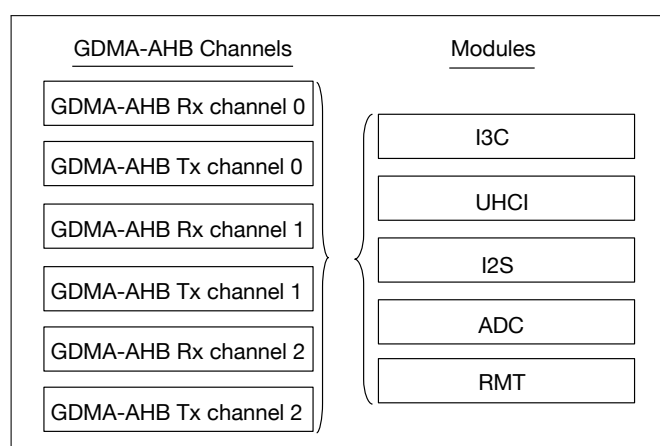


Figure 3.1-1. Modules that Share GDMA-AHB Channels

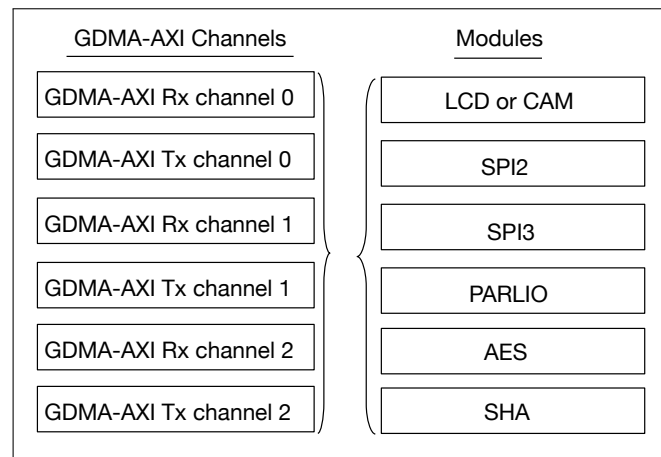


Figure 3.1-2. Modules that Share GDMA-AXI Channels

## 3.2 Features

GDMA-AHB and GDMA-AXI have the following features:

- Architecture:
  - GDMA-AHB: AHB bus architecture
  - GDMA-AXI: AXI bus architecture, which gives the possibility to complete up to 8 transactions out of order and up to 8 outstanding transactions
- Programmable length of data to be transferred in bytes
- Access via any address and size
- Alignment:
  - GDMA-AHB:
    - \* Descriptor address: 1-word aligned
    - \* Data address and length (only internal memory is accessible): no requirements
  - GDMA-AXI:
    - \* Descriptor address: 2-word aligned
    - \* Data address and length:
      - Internal memory and non-encrypted external memory address space: no requirements
      - Encrypted external memory address space: 16-byte aligned
- Linked list of descriptors
- INCR burst transfer when accessing memory
- Three transmit channels and three receive channels for each controller
- Software-configurable selection of peripheral requesting its service
- Configurable channel priority and weight arbitration
- Support for memory transfer

- CRC calculation of data

### 3.3 Architecture

In ESP32-P4, all modules that need high-speed data transfer support GDMA. The GDMA controller and CPU data bus have access to the same address space in memory. Figure 3.3-1 shows the basic architecture of the GDMA controller.

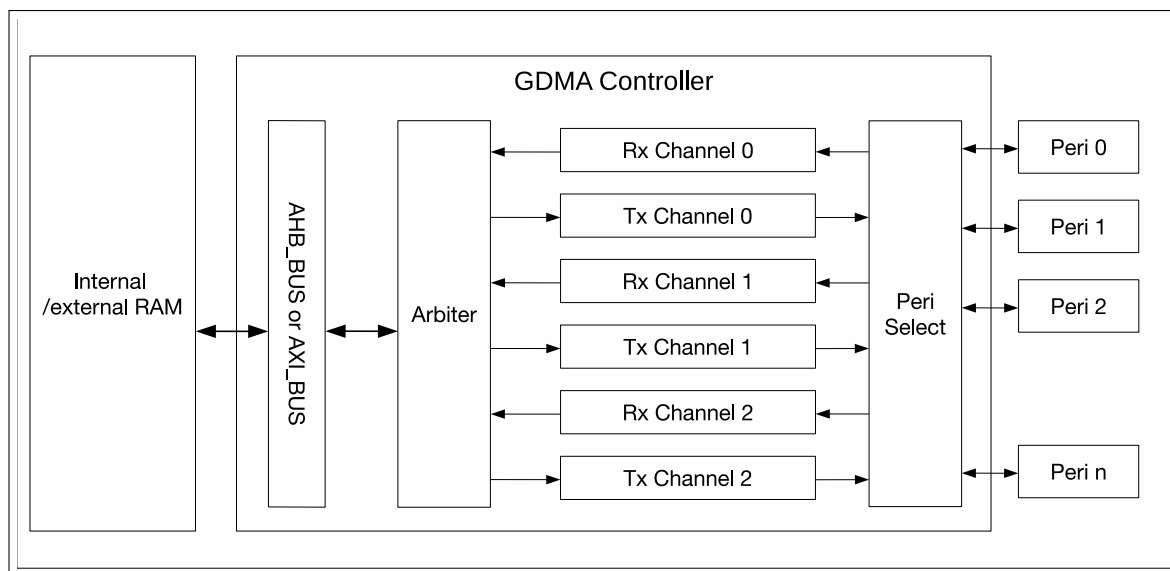


Figure 3.3-1. GDMA controller Architecture

GDMA-AHB and GDMA-AXI have six independent channels respectively, i.e., three transmit channels and three receive channels. Every channel can be connected to different peripherals. In other words, channels are general-purpose, and shared by peripherals.

GDMA-AHB and GDMA-AXI read data from or write data to internal memory or internal and external memory via AHB\_BUS or AXI\_BUS respectively. Before this, GDMA uses configurable arbitration schemes for channels requesting read or write access. For the available address range of internal and external memory, please see Chapter 6 [System and Memory](#).

Software can use the GDMA through linked lists. GDMA-AHB linked lists are stored in internal memory, while GDMA-AXI linked lists are stored in internal or external memory. These linked lists consist of outlink<sub>*n*</sub> and inlink<sub>*n*</sub>, where *n* indicates the channel number (ranging from 0 to 2). The GDMA reads an outlink<sub>*n*</sub> (i.e., a linked list of transmit descriptors) from memory and transmit data in corresponding memory according to the outlink<sub>*n*</sub>, or read an inlink<sub>*n*</sub> (i.e., a linked list of receive descriptors) and store received data into specific address space in memory according to the inlink<sub>*n*</sub>.

### 3.4 Functional Description

#### 3.4.1 Linked List

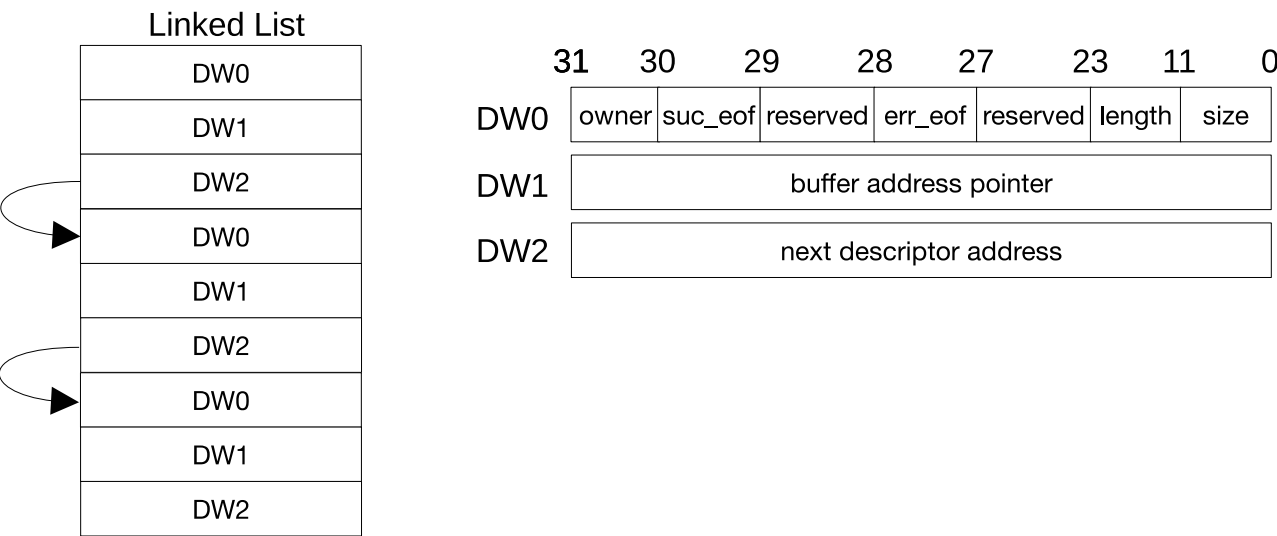


Figure 3.4-1. Structure of a Linked List

Figure 3.4-1 shows the structure of a linked list. An outlink and an inlink have the same structure. A linked list is formed by one or more descriptors, and each descriptor consists of three words. Linked lists should be stored in the memory for the GDMA to be able to use them. The meanings of a descriptor’s fields are as follows:

- owner (DW0) [31]: Specifies who is allowed to access the buffer that this descriptor points to.  
0: CPU can access the buffer.  
1: The GDMA controller can access the buffer.  
When the GDMA controller stops using the buffer, this bit in a receive descriptor is automatically cleared by hardware, while this bit in a transmit descriptor can only be automatically cleared by hardware if [AHB/AXI\\_DMA\\_OUT\\_AUTO\\_WRBACK\\_CHn](#) is set to 1. Software can disable automatic clearing by hardware by setting the [AHB/AXI\\_DMA\\_OUT\\_LOOP\\_TEST\\_CHn](#) or [AHB/AXI\\_DMA\\_IN\\_LOOP\\_TEST\\_CHn](#) bit. When software loads a linked list, this bit should be set to 1.  
**Note:** AHB/AXI\_DMA\_OUT is the prefix of transmit channel registers, and AHB/AXI\_DMA\_IN is the prefix of receive channel registers.
- suc\_eof (DW0) [30]: Specifies whether the [AHB/AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#) or [AHB/AXI\\_DMA\\_OUT\\_EOF\\_CHn\\_INT](#) interrupt will be triggered when the data corresponding to this descriptor has been received or transmitted.  
0: No interrupt will be triggered after the current descriptor’s successful transfer;  
1: An interrupt will be triggered after the current descriptor’s successful transfer.  
For receive descriptors, software needs to clear this bit to 0, and hardware will set it to 1 after receiving data containing the EOF flag.  
For transmit descriptors, software needs to set this bit to 1 as needed.  
If software configures this bit to 1 in a descriptor, the GDMA will include the EOF flag in the data sent to the corresponding peripheral, indicating to the peripheral that this data segment marks the end of one

transfer phase.

- reserved (DWO) [29]: Reserved. The value of this bit does not matter.
- err\_eof (DWO) [28]: Specifies whether the received data has errors.  
0: The received data does not have errors.  
1: The received data has errors.  
This bit is used only when UHCI or PARLIO uses the GDMA to receive data. When an error is detected in the received data segment corresponding to a descriptor, this bit in the receive descriptor is set to 1 by hardware.
- reserved (DWO) [27:24]: Reserved.
- length (DWO) [23:12]: Specifies the number of valid bytes in the buffer that this descriptor points to. This field in a transmit descriptor is written by software and indicates how many bytes can be read from the buffer; this field in a receive descriptor is written by hardware automatically and indicates how many valid bytes have been stored in the buffer.
- size (DWO) [11:0]: Specifies the size of the buffer that this descriptor points to.
- buffer address pointer (DW1): Address of the buffer.
- next descriptor address (DW2): Address of the next descriptor. If the current descriptor is the last one, this value is 0. For GDMA-AHB, this field can only point to the internal memory space; for GDMA-AXI, this field can point to the internal or external memory space.

**Note:**

Please note that addresses of GDMA-AHB descriptors should be 4-byte aligned, and addresses of GDMA-AXI descriptors should be 8-byte aligned.

If the length of data received is smaller than the size of the buffer, the GDMA controller will not use the available space of the buffer in the next transaction.

### 3.4.2 Peripheral-to-Memory and Memory-to-Peripheral Data Transfer

The GDMA controller can transfer data from memory to peripheral (transmit) and from peripheral to memory (receive). A transmit channel transfers data in the specified memory location to a peripheral's transmitter via an outlink<sub>*n*</sub>, whereas a receive channel transfers data received by a peripheral to the specified memory location via an inlink<sub>*n*</sub>.

Every transmit and receive channel can be connected to any peripheral with the GDMA feature. Table 3.4-1 and Table 3.4-2 illustrate how to select the peripheral to be connected via registers. “Dummy-*n*” corresponds to register values for memory-to-memory data transfer. When a channel is connected to a peripheral, the rest of the channels cannot be connected to that peripheral.

**Table 3.4-1. GDMA-AHB Selecting Peripherals via Register Configuration**

| AHB_DMA_PERI_IN_SEL_CH <sub><i>n</i></sub><br>AHB_DMA_PERI_OUT_SEL_CH <sub><i>n</i></sub> | Peripheral |
|---|------------|
| 0   | I3C        |
| 1   | Dummy-1    |

|         |               |
|---------|---------------|
| 2       | UHCI          |
| 3       | I2S0          |
| 4       | I2S1          |
| 5       | I2S2          |
| 6 ~ 7   | Dummy-6 ~ 7   |
| 8       | ADC           |
| 9       | Dummy-9       |
| 10      | RMT           |
| 11 ~ 15 | Dummy-11 ~ 15 |
| 16 ~ 63 | Invalid       |

Table 3.4-2. GDMA-AXI Selecting Peripherals via Register Configuration

| AXI_DMA_PERI_IN_SEL_CH $n$<br>AXI_DMA_PERI_OUT_SEL_CH $n$ | Peripheral   |
|---|--------------|
| 0   | LCD or CAM   |
| 1   | SPI2         |
| 2   | SPI3         |
| 3   | PARLIO       |
| 4   | AES          |
| 5   | SHA          |
| 6 ~ 15  | Dummy-6 ~ 15 |
| 16 ~ 63   | Invalid      |

### 3.4.3 Memory-to-Memory Data Transfer

The GDMA controller also allows memory-to-memory data transfer. Such data transfer can be enabled by setting `AHB/AXI_DMA_MEM_TRANS_EN_CH $n$` , which connects the output of transmit channel  $n$  to the input of receive channel  $n$ . Note that a transmit channel is only connected to the receive channel with the same number ( $n$ ), and `AHB/AXI_DMA_PERI_IN_SEL_CH $n$`  and `AHB/AXI_DMA_PERI_OUT_SEL_CH $n$`  should be configured to the same value corresponding to “Dummy”.

To access external memory, please use GDMA-AXI.

### 3.4.4 Enabling GDMA

The software uses the GDMA controller through linked lists. When the GDMA controller receives data, software loads an inlink, configures the `AHB/AXI_DMA_INLINK_ADDR_CH $n$`  field with the address of the first receive descriptor, and sets the `AHB/AXI_DMA_INLINK_START_CH $n$`  bit to enable GDMA. When the GDMA controller transmits data, software loads an outlink, prepares data to be transmitted, configures the `AHB/AXI_DMA_OUTLINK_ADDR_CH $n$`  field with address of the first transmit descriptor, and sets the `AHB/AXI_DMA_OUTLINK_START_CH $n$`  bit to enable GDMA. The `AHB/AXI_DMA_INLINK_START_CH $n$`  bit and `AHB/AXI_DMA_OUTLINK_START_CH $n$`  bit are cleared automatically by hardware.

In some cases, you may want to append more descriptors to a DMA transfer that is already started. Naively, it would seem to be possible to do this by clearing the EOF bit of the final descriptor in the existing list and

setting its next descriptor address pointer field (DW2) to the first descriptor of the to-be-added list. However, this strategy fails if the existing DMA transfer is almost or entirely finished. Instead, the GDMA controller has specialized logic to make sure a DMA transfer can be continued or restarted: if the transfer is ongoing, the controller will make sure to take the appended descriptors into account; if the transfer has already finished, the controller will restart with the new descriptors. This is implemented by the Restart function.

When using the Restart function, software needs to rewrite the address of the first descriptor in the new list to DW2 of the last descriptor in the loaded list, and set [AHB/AXI\\_DMA\\_INLINK\\_RESTART\\_CH<sub>n</sub>](#) bit or [AHB/AXI\\_DMA\\_OUTLINK\\_RESTART\\_CH<sub>n</sub>](#) bit (these two bits are cleared automatically by hardware). As shown in Figure 3.4-2, by doing so hardware can obtain the address of the first descriptor in the new list when reading the last descriptor in the loaded list, and then read the new list.

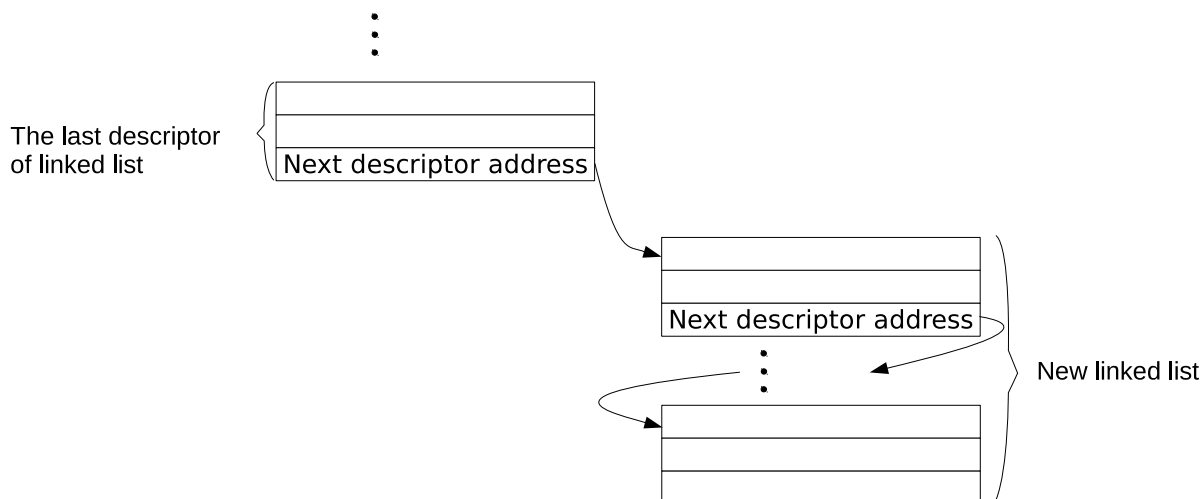


Figure 3.4-2. Relationship among Linked Lists

### 3.4.5 Linked List Reading Process

Once configured and enabled by software, the GDMA controller starts to read the linked list from memory. The GDMA performs checks on descriptors in the linked list. Only if descriptors pass the checks, the corresponding GDMA channel will start data transfer. If the descriptors fail any of the checks, hardware will trigger descriptor error interrupt (either [AHB/AXI\\_DMA\\_IN\\_DSCR\\_ERR\\_CH<sub>n</sub>\\_INT](#) or [AHB/AXI\\_DMA\\_OUT\\_DSCR\\_ERR\\_CH<sub>n</sub>\\_INT](#)), and the channel will halt.

The checks performed on descriptors are:

- Owner bit check when [AHB/AXI\\_DMA\\_IN\\_CHECK\\_OWNER\\_CH<sub>n</sub>](#) or [AHB/AXI\\_DMA\\_OUT\\_CHECK\\_OWNER\\_CH<sub>n</sub>](#) is set to 1. If the owner bit is 0, the buffer is accessed by the CPU. In this case, the owner bit fails the check. The owner bit will not be checked if [AHB/AXI\\_DMA\\_IN\\_CHECK\\_OWNER\\_CH<sub>n</sub>](#) or [AHB/AXI\\_DMA\\_OUT\\_CHECK\\_OWNER\\_CH<sub>n</sub>](#) is 0.
- Descriptor address check, which checks if the descriptor address is located in configured internal memory space for GDMA-AHB, and configured internal or external memory space for GDMA-AXI. If a GDMA-AHB descriptor points to [AHB\\_DMA\\_ACCESS\\_INTR\\_MEM\\_START\\_ADDR](#) ~ [AHB\\_DMA\\_ACCESS\\_INTR\\_MEM\\_END\\_ADDR](#) (the value should be located in internal memory), it passes the check. If a GDMA-AXI descriptor points to [AXI\\_DMA\\_ACCESS\\_INTR\\_MEM\\_START\\_ADDR](#) ~ [AXI\\_DMA\\_ACCESS\\_INTR\\_MEM\\_END\\_ADDR](#) (the value should be located in internal memory), or [AXI\\_DMA\\_ACCESS\\_EXTR\\_MEM\\_START\\_ADDR](#) ~ [AXI\\_DMA\\_ACCESS\\_EXTR\\_MEM\\_END\\_ADDR](#) (the value



should be located in external memory), it passes the check. For details, please refer to Section 3.4.7.

After the software detects a descriptor error interrupt, it must reset the corresponding channel, and enable GDMA by setting [AHB/AXI\\_DMA\\_OUTLINK\\_START\\_CHn](#) or [AHB/AXI\\_DMA\\_INLINK\\_START\\_CHn](#) bit.

### 3.4.6 EOF

**Note:** In this chapter, EOF of transmit descriptors refers to `suc_eof` (i.e., bit 30 of DWO), while EOF of receive descriptors refers to both `suc_eof` and `err_eof` (i.e., bit 28 of DWO).

The GDMA controller uses EOF (end of frame) flags to indicate the end of data segment transfer corresponding to a specific descriptor.

For data transmission, the GDMA generates two types of EOF interrupts:

- [AHB/AXI\\_DMA\\_OUT\\_EOF\\_CHn\\_INT](#), generated when the `suc_eof` bit of any descriptor in the linked list is set, and the data corresponding to this descriptor has been transmitted. This interrupt is enabled by setting the [AHB/AXI\\_DMA\\_OUT\\_EOF\\_CHn\\_INT\\_ENA](#) bit.
- [AHB/AXI\\_DMA\\_OUT\\_TOTAL\\_EOF\\_CHn\\_INT](#), generated when the `suc_eof` bit of the last descriptor in the linked list is set, and the data corresponding to the last descriptor has been transmitted. This interrupt is enabled by setting the [AHB/AXI\\_DMA\\_OUT\\_TOTAL\\_EOF\\_CHn\\_INT\\_ENA](#) bit.

For data reception, the GDMA also generates two types of EOF interrupts:

- [AHB/AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#), generated when a data segment with an EOF flag has been received. This interrupt is enabled by setting the [AHB/AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT\\_ENA](#) bit.
- (UHCI and PARLIO only) [AHB/AXI\\_DMA\\_IN\\_ERR\\_EOF\\_CHn\\_EOF\\_INT](#), generated when a data segment corresponding to a descriptor has been received with errors. This interrupt is enabled by setting the [AHB/AXI\\_DMA\\_IN\\_ERR\\_EOF\\_CHn\\_INT\\_ENA](#) bit, and is valid only when the channel is connected to UHCI or PARLIO.

When detecting an [AHB/AXI\\_DMA\\_OUT\\_TOTAL\\_EOF\\_CHn\\_INT](#) or [AHB/AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#) interrupt, software can read the value of the [AHB/AXI\\_DMA\\_OUT\\_EOF\\_DES\\_ADDR\\_CHn](#) or

[AHB/AXI\\_DMA\\_IN\\_SUC\\_EOF\\_DES\\_ADDR\\_CHn](#) field, which stores the address of the finished descriptor.

Therefore, the software can tell which descriptors have been used and reclaim them as needed. For RX, the address of the descriptor can also be stored to the [AHB/AXI\\_DMA\\_IN\\_ERR\\_EOF\\_DES\\_ADDR\\_CHn](#) field when an [AHB/AXI\\_DMA\\_IN\\_ERR\\_EOF\\_CHn\\_INT](#) interrupt is triggered.

### 3.4.7 Accessing Memory

Any transmit and receive channels of GDMA-AHB and GDMA-AXI can access the internal memory address space configured by [AHB/AXI\\_DMA\\_ACCESS\\_INTR\\_MEM\\_START\\_ADDR](#) and

[AHB/AXI\\_DMA\\_ACCESS\\_INTR\\_MEM\\_END\\_ADDR](#). Moreover, the transmit and receive channels of GDMA-AXI can access the external memory address space configured by [AXI\\_DMA\\_ACCESS\\_EXTR\\_MEM\\_START\\_ADDR](#) and [AXI\\_DMA\\_ACCESS\\_EXTR\\_MEM\\_END\\_ADDR](#).

To improve data transfer efficiency, GDMA can send data in burst mode. For GDMA-AHB, this mode is disabled by default, and can be enabled for receive channels by setting [AHB\\_DMA\\_IN\\_DATA\\_BURST\\_EN\\_CHn](#), and enabled for transmit channels by setting [AHB\\_DMA\\_OUT\\_DATA\\_BURST\\_EN\\_CHn](#). For GDMA-AXI, this mode is enabled by default, and cannot be disabled. Users can configure the number of data bytes in a single AXI

burst (burst length) to 8, 16, 32, 64, or 128 bytes via [AXI\\_DMA\\_IN\\_BURST\\_SIZE\\_SEL\\_CHn](#) and [AXI\\_DMA\\_OUT\\_BURST\\_SIZE\\_SEL\\_CHn](#).

When GDMA-AHB accesses the configured internal memory space, there are no requirements for descriptor field alignment. When GDMA-AXI accesses the configured internal memory and non-encrypted external memory space, there are no requirements for descriptor field alignment; when it accesses the encrypted external memory space (see Chapter [29 External Memory Encryption and Decryption \(XTS\\_AES\)](#)), buffer address pointer and data should be 16-byte aligned, and other fields are not required to be aligned.

### 3.4.8 Arbitration

To ensure timely response to peripherals running at a high speed with low latency (such as SPI), the GDMA controller implements two arbitration schemes, based on channel priority and channel weight respectively.

- Priority arbitration: Each channel can be assigned a priority from 0 ~ 5 (in total 6 levels). The larger the number, the higher the priority. When several channels perform data transfers at the same time, the GDMA would respond to the transfer requests according to priority levels, and the channel with higher priority would get a response more timely.
- Weight arbitration:
  - Each channel is assigned a weight (i.e., the number of tokens) from 0 ~ 15. The GDMA divides the AHB or AXI bus clock period into multiple time slots, and in each time slot, the number of transfers performed by a channel is determined by the number of its tokens. Every time a channel performs a data transfer, one of its tokens is spent. If all of its tokens have been spent in a time slot, then this channel's transfer request will no longer be responded to until the time slot expires, or until tokens of all channels have been spent and the new time slot starts.
  - If the number of tokens assigned to a channel is not zero, the GDMA waits for this channel's tokens to be spent even if it does not have data transfer requests, and will not exit from this time slot ahead of expiration. This leads to a waste of bandwidth. Therefore, the GDMA provides weight arbitration optimization. When this feature is enabled, a channel without data transfer requests will not be involved in the arbitration and its tokens will be ignored. When all channels no longer have transfer requests, the GDMA arbiter exits from the current time slot before expiration. This way, the arbitration response is accelerated and the transfer efficiency is improved.

**Note:**

- If channels have the same weight but different priorities, on condition that the number of bytes to be transferred is the same and not large, channels with higher priorities would finish data transfers first.
- If channels have different priorities and weights, on condition that the number of bytes to be transferred is the same, channels with higher weights would be allocated more bandwidth and finish data transfers first.

### 3.4.9 CRC Calculation

The GDMA has a CRC calculation module for both TX and RX. This module supports arbitrary polynomials and 8-bit parallel computation, namely 8 bits at a time. The CRC result is up to 32-bit wide for GDMA-AHB, and up

to 16-bit for GDMA-AXI. It is calculated for each linked list descriptor by descriptor and becomes invalid when the Restart function is triggered during transfer.

For easier understanding of register configuration rules, assume:

- The 8-bit data to calculate each time is `data[7:0]`.
- The required CRC result is 5-bit wide, and the polynomial used is  $crc[4 : 0] = x \oplus 5 + x \oplus 2 + 1$ ;
- The initial CRC value is 0x1F, and the intermediate result calculated in each clock cycle is `crc_tmp[4:0]`.

Taking as an example the GDMA reading data from memory and transmitting the data to peripherals, the following fields are provided by hardware for CRC computation:

- **AHB/AXI\_DMA\_OUT\_CRC\_INIT\_DATA\_CH $n$** : Configures the initial CRC value, i.e., 0x1F in the above example. **AHB\_DMA\_OUT\_CRC\_INIT\_DATA\_CH $n$**  can be configured with a 32-bit value at the maximum, while **AXI\_DMA\_OUT\_CRC\_INIT\_DATA\_CH $n$**  can be configured with a 16-bit value at the maximum, meaning that the CRC result could be 32 bits or 16 bits at most.
- **AHB/AXI\_DMA\_OUT\_CRC\_FINAL\_RESULT\_CH $n$** : Stores the computation result of all data in a DMA transfer (until data pointed by the last descriptor in the linked list has been transferred). The computation result could be 32 bits at most.
- **AHB/AXI\_DMA\_TX\_CRC\_WIDTH\_CH $n$** : Configures the CRC result length.
- **AHB/AXI\_DMA\_TX\_CRC\_LAUTCH\_FLGA\_CH $n$** , which latches the CRC result.
- **AHB/AXI\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$** : Indicates which bits in `crc_tmp[4:0]` are used to compute `crc[x]` ( $x$  is configured via **AHB/AXI\_DMA\_TX\_CRC\_EN\_ADDR\_CH $n$** ). If **AHB/AXI\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$**  is configured as 0xF, it means that only `crc_tmp[3]`, `crc_tmp[2]`, `crc_tmp[1]`, and `crc_tmp[0]` are used for computation, and other bits are not used (in this case `crc_tmp[4]`).
- **AHB/AXI\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$** : Indicates which bits in `data[7:0]` are used to compute `crc[x]` ( $x$  is configured via **AHB/AXI\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH $n$** ). GDMA calculates the CRC in the unit of byte, so only the lower 8 bits of this field needs to be configured. If **AHB/AXI\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$**  is configured as 0xF, it means that only `data[3]`, `data[2]`, `data[1]`, and `data[0]` are used for computation.

CRC calculation is achieved in the GDMA by configuring a parallel calculation matrix derived from the polynomial. If the expected CRC result is  $n$  bits, then the matrix has  $n$  rows and  $n + 8$  columns.

Based on the assumptions at the beginning of this section, the calculation matrix would be 5 rows and 13 columns, and the actual hardware CRC calculation formulas would be as follows ( $\oplus$  represents the XOR operation):

$$\begin{aligned} crc[0] &= crc\_tmp[0] \oplus crc\_tmp[2] \oplus crc\_tmp[3] \oplus data[0] \oplus data[3] \oplus data[5] \oplus data[6] \\ crc[1] &= crc\_tmp[1] \oplus crc\_tmp[3] \oplus crc\_tmp[4] \oplus data[1] \oplus data[4] \oplus data[6] \oplus data[7] \\ crc[2] &= crc\_tmp[0] \oplus crc\_tmp[3] \oplus crc\_tmp[4] \oplus data[0] \oplus data[2] \oplus data[3] \oplus data[6] \oplus data[7] \\ crc[3] &= crc\_tmp[0] \oplus crc\_tmp[1] \oplus crc\_tmp[4] \oplus data[1] \oplus data[4] \oplus data[3] \oplus data[7] \\ crc[4] &= crc\_tmp[1] \oplus crc\_tmp[2] \oplus data[2] \oplus data[4] \oplus data[5] \end{aligned}$$

The above calculation formula can be abstracted as a switch matrix shown in Figure 3.4-3:

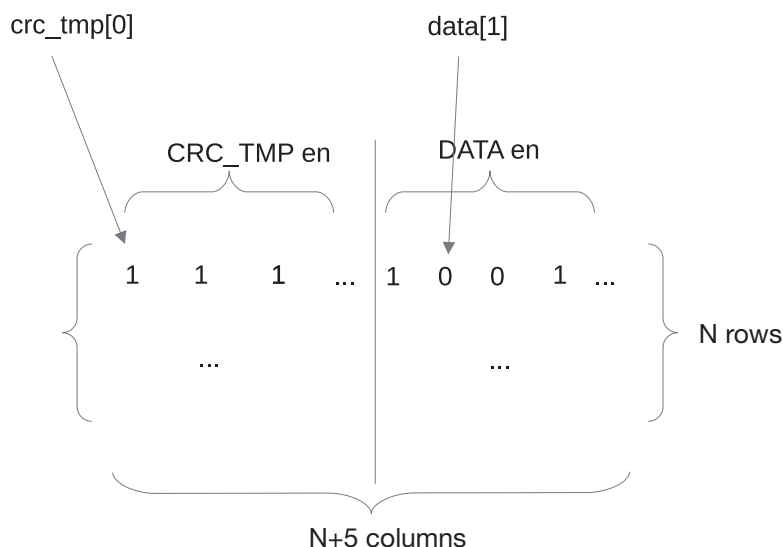


Figure 3.4-3. CRC Calculation Matrix

**Note:**

The CRC calculation described above is a Linear Feedback Shift Register (LFSR) implementation of the bitwise CRC algorithm. The formulas can be generated with some online tools according to the polynomial and the data width for parallel computation (always 8 bits for ESP32-P4).

## 3.5 Event Task Matrix Feature

The GDMA controller on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows GDMA's ETM tasks to be triggered by any peripherals' ETM events, or GDMA's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to GDMA. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

GDMA can receive the following ETM tasks:

- GDMA\_AHB/AXI\_TASK\_IN\_START\_CH $n$ : Enables the corresponding RX channel  $n$  for data transfer.
- GDMA\_AHB/AXI\_TASK\_OUT\_START\_CH $n$ : Enables the corresponding TX channel  $n$  for data transfer.

**Note:**

Above ETM tasks can achieve the same functions as CPU configuring [AHB/AXI\\_DMA\\_INLINK\\_START\\_CH \$n\$](#)  and [AHB/AXI\\_DMA\\_OUTLINK\\_START\\_CH \$n\$](#) . When [AHB/AXI\\_DMA\\_IN\\_ETM\\_EN\\_CH \$n\$](#)  or [AHB/AXI\\_DMA\\_OUT\\_ETM\\_EN\\_CH \$n\$](#)  is 1, only ETM tasks can be used to configure the transfer direction and enable the corresponding GDMA channel. When [AHB/AXI\\_DMA\\_IN\\_ETM\\_EN\\_CH \$n\$](#)  or [AHB\\_DMA\\_OUT\\_ETM\\_EN\\_CH \$n\$](#)  is 0, only CPU can be used to enable the corresponding GDMA channel.

GDMA can generate the following ETM events:

- GDMA\_AHB/AXI\_EVT\_IN\_DONE\_CH $n$ : Indicates that the data has been received according to the receive descriptor via channel  $n$ .

- GDMA\_AHB/AXI\_EVT\_IN\_SUC\_EOF\_CH $n$ : Indicates that the data corresponding to a receive descriptor has been received via channel  $n$  and the EOF bit of this descriptor is 1.
- GDMA\_AHB/AXI\_EVT\_IN\_FIFO\_EMPTY\_CH $n$ : Indicates that the RX FIFO has become empty.
- GDMA\_AHB/AXI\_EVT\_IN\_FIFO\_FULL\_CH $n$ : Indicates that the RX FIFO has become full.
- GDMA\_AHB/AXI\_EVT\_OUT\_DONE\_CH $n$ : Indicates that the data has been transmitted according to the transmit descriptor via channel  $n$ .
- GDMA\_AHB/AXI\_EVT\_OUT\_SUC\_EOF\_CH $n$ : Indicates that the data corresponding to a transmit descriptor has been transmitted or received via channel  $n$  and the EOF bit of this descriptor is 1.
- GDMA\_AHB/AXI\_EVT\_OUT\_TOTAL\_EOF\_CH $n$ : Indicates that the data corresponding to the last transmit descriptors has been sent via transmit channel  $n$  and the EOF bit of this descriptor is 1.
- GDMA\_AHB/AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH $n$ : Indicates that the TX FIFO has become empty.
- GDMA\_AHB/AXI\_EVT\_OUT\_FIFO\_FULL\_CH $n$ : Indicates that the TX FIFO has become full.

In practical applications, GDMA's ETM events can trigger its own ETM tasks. For example, the GDMA\_AHB/AXI\_EVT\_OUT\_TOTAL\_EOF\_CH0 event can trigger the GDMA\_AHB/AXI\_TASK\_IN\_START\_CH1 task, and in this way trigger a new round of GDMA operations.

## 3.6 Interrupts

ESP32-P4's GDMA module can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- AHB/AXI\_PDMA\_IN\_CH0\_INTR
- AHB/AXI\_PDMA\_IN\_CH1\_INTR
- AHB/AXI\_PDMA\_IN\_CH2\_INTR
- AHB/AXI\_PDMA\_OUT\_CH0\_INTR
- AHB/AXI\_PDMA\_OUT\_CH1\_INTR
- AHB/AXI\_PDMA\_OUT\_CH2\_INTR

There are several internal interrupt sources from GDMA that can generate the above interrupt signals.

The AHB/AXI\_PDMA\_IN\_CH $n$ \_INTR ( $n$  is 0 ~ 2) signals are generated by the following interrupt sources:

- AHB/AXI\_DMA\_IN\_DONE\_CH $n$ \_INT: Triggered when all data corresponding to a receive descriptor has been received via receive channel  $n$ .
- AHB/AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT: Triggered when the suc\_eof bit in a receive descriptor is 1 and the data corresponding to this receive descriptor has been received via receive channel  $n$ .
- AHB/AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT: Triggered when an error is detected in the data segment corresponding to a descriptor received via receive channel  $n$ . This interrupt is used only for UHCI (UART0 or UART1) or PARLIO.
- AHB/AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT: Triggered when the size of the buffer pointed by receive descriptors is smaller than the length of data to be received via receive channel  $n$ .

- AHB/AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT: Triggered when a receive descriptor on receive channel  $n$  fails any of the two descriptor checks.
- AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT or AXI\_DMA\_INFIFO\_L1/L2/L3\_OVF\_CH $n$ \_INT: Triggered when the RX FIFO of GDMA-AHB or the L1/L2/L3 RX FIFO of GDMA-AXI overflows.
- AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT or AXI\_DMA\_INFIFO\_L1/L2/L3\_UDF\_CH $n$ \_INT: Triggered when the RX FIFO of GDMA-AHB or the L1/L2/L3 RX FIFO of GDMA-AXI underflows.

The AHB/AXI\_PDMA\_OUT\_CH $n$ \_INTR ( $n$  is 0 ~ 2) signals are generated by the following interrupt sources:

- AHB/AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT: Triggered when all data corresponding to a transmit descriptor has been sent via transmit channel  $n$ .
- AHB/AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT: Triggered when the suc\_eof bit in a transmit descriptor is 1 and data corresponding to this descriptor has been sent via transmit channel  $n$ . If [AHB/AXI\\_DMA\\_OUT\\_EOF\\_MODE\\_CH \$n\$](#)  is 0, this interrupt will be triggered when the last byte of data corresponding to this descriptor enters GDMA's transmit channel; if [AHB/AXI\\_DMA\\_OUT\\_EOF\\_MODE\\_CH \$n\$](#)  is 1, this interrupt is triggered when the last byte of data is taken from GDMA's transmit channel.
- AHB/AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT: Triggered when a transmit descriptor on transmit channel  $n$  fails any of the two descriptor checks.
- AHB/AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT: Triggered when all data corresponding to a linked list (including multiple descriptors) has been sent via transmit channel  $n$ .
- AHB\_DMA\_OUTFIFO\_OVF\_CH $n$ \_INT or AXI\_DMA\_OUTFIFO\_L1/L2/L3\_OVF\_CH $n$ \_INT: Triggered when the TX FIFO of GDMA-AHB or the L1/L2/L3 TX FIFO of GDMA-AXI overflows.
- AHB\_DMA\_OUTFIFO\_UDF\_CH $n$ \_INT or AXI\_DMA\_OUTFIFO\_L1/L2/L3\_UDF\_CH $n$ \_INT: Triggered when the TX FIFO of GDMA-AHB or the L1/L2/L3 TX FIFO of GDMA-AXI underflows.

## 3.7 Programming Procedures

The clock gating for GDMA can be configured via [HP\\_SYS\\_CLKRST\\_AHB/AXI\\_PDMA\\_SYS\\_CLK\\_EN](#), and is enabled by default. GDMA can be reset by configuring [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_AHB/AXI\\_PDMA](#).

### 3.7.1 Programming Procedures for GDMA's Transmit Channel

To transmit data, GDMA's transmit channel should be configured by software as follows:

1. Set [AHB/AXI\\_DMA\\_OUT\\_RST\\_CH \$n\$](#)  first to 1 and then to 0, to reset the state machine of GDMA's transmit channel and FIFO pointer.
2. Load an outlink, and configure [AHB/AXI\\_DMA\\_OUTLINK\\_ADDR\\_CH \$n\$](#)  with address of the first transmit descriptor.
3. Configure [AHB/AXI\\_DMA\\_PERI\\_OUT\\_SEL\\_CH \$n\$](#)  with the value corresponding to the peripheral to be connected, as shown in Table 3.4-1 and Table 3.4-2.
4. Set [AHB/AXI\\_DMA\\_OUTLINK\\_START\\_CH \$n\$](#)  to enable GDMA's transmit channel for data transfer.

5. Configure and enable the corresponding peripheral (SPI2, UHCI (UART0 or UART1), I2S, AES, SHA, and ADC). See details in individual chapters of these peripherals.
6. Wait for the AHB/AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT interrupt, which indicates the completion of data transfer.

### 3.7.2 Programming Procedures for GDMA's Receive Channel

To receive data, GDMA's receive channel should be configured by software as follows:

1. Set AHB/AXI\_DMA\_IN\_RST\_CH $n$  first to 1 and then to 0, to reset the state machine of GDMA's receive channel and FIFO pointer.
2. Load an inlink, and configure AHB/AXI\_DMA\_INLINK\_ADDR\_CH $n$  with address of the first receive descriptor.
3. Configure AHB/AXI\_DMA\_PERI\_IN\_SEL\_CH $n$  with the value corresponding to the peripheral to be connected, as shown in Table 3.4-1 and Table 3.4-2.
4. Set AHB/AXI\_DMA\_INLINK\_START\_CH $n$  to enable GDMA's receive channel for data transfer.
5. Configure and enable the corresponding peripheral (SPI2, UHCI (UART0 or UART1), I2S, AES, SHA, and ADC). See details in individual chapters of these peripherals.

### 3.7.3 Programming Procedures for Memory-to-Memory Transfer

To transfer data from one memory location to another, GDMA should be configured by software as follows:

1. Set AHB/AXI\_DMA\_OUT\_RST\_CH $n$  first to 1 and then to 0, to reset the state machine of GDMA's transmit channel and FIFO pointer.
2. Set AHB/AXI\_DMA\_IN\_RST\_CH $n$  first to 1 and then to 0, to reset the state machine of GDMA's receive channel and FIFO pointer.
3. Load an outlink, and configure AHB/AXI\_DMA\_OUTLINK\_ADDR\_CH $n$  with address of the first transmit descriptor.
4. Load an inlink, and configure AHB/AXI\_DMA\_INLINK\_ADDR\_CH $n$  with address of the first receive descriptor.
5. Set AHB/AXI\_DMA\_MEM\_TRANS\_EN\_CH $n$  to enable memory-to-memory transfer.
6. Set AHB/AXI\_DMA\_OUTLINK\_START\_CH $n$  to enable GDMA's transmit channel for data transfer.
7. Set AHB/AXI\_DMA\_INLINK\_START\_CH $n$  to enable GDMA's receive channel for data transfer.
8. If the suc\_eof bit is set in a transmit descriptor, an AHB/AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT interrupt will be triggered when the data segment corresponding to this descriptor has been transmitted.

### 3.7.4 Programming Procedures for Channel Priority and Weight

The priority arbitration can be configured as follows:

1. Configure the channel priority for TX and RX respectively via AHB/AXI\_DMA\_TX\_PRI\_CH $n$  and AHB/AXI\_DMA\_RX\_PRI\_CH $n$ .

The weight arbitration can be configured as follows:

1. Configure the time slot for TX and RX respectively via [AHB/AXI\\_DMA\\_ARB\\_TIMEOUT\\_TX](#) and [AHB/AXI\\_DMA\\_ARB\\_TIMEOUT\\_RX](#).
2. Configure the number of tokens for TX and RX respectively via [AHB/AXI\\_DMA\\_TX\\_CH\\_ARB\\_WEIGHT\\_CHn](#) and [AHB/AXI\\_DMA\\_RX\\_CH\\_ARB\\_WEIGHT\\_CHn](#).
3. Enable weight arbitration optimization for TX and RX respectively by clearing [AHB/AXI\\_DMA\\_TX\\_ARB\\_WEIGHT\\_OPT\\_DIR\\_CHn](#) and [AHB/AXI\\_DMA\\_RX\\_ARB\\_WEIGHT\\_OPT\\_DIR\\_CHn](#).
4. Enable the arbitration for TX and RX respectively by setting [AHB/AXI\\_DMA\\_WEIGHT\\_EN\\_TX](#) and [AHB/AXI\\_DMA\\_WEIGHT\\_EN\\_RX](#).

### 3.7.5 Programming Procedures for CRC Calculation

The CRC calculation registers can be configured as follows:

1. Configure which bits in `crc_tmp` and data are used in the matrix via [AHB/AXI\\_DMA\\_TX\\_CRC\\_EN\\_ADDR\\_CHn](#), [AHB/AXI\\_DMA\\_TX\\_CRC\\_DATA\\_EN\\_ADDR\\_CHn](#), [AHB/AXI\\_DMA\\_TX\\_CRC\\_EN\\_WR\\_DATA\\_CHn](#), and [AHB/AXI\\_DMA\\_TX\\_CRC\\_DATA\\_EN\\_WR\\_DATA\\_CHn](#).
2. Latch the values of the above four fields by first writing 1 and then 0 to [AHB/AXI\\_DMA\\_TX\\_CRC\\_LAUTCH\\_FLGA\\_CHn](#). Then the configuration for a row is complete.
3. Repeat Step 1 and Step 2 until all rows in the matrix are set up, and then start DMA transfer.



## 3.8 Register Summary

### 3.8.1 GDMA-AHB Register Summary

The addresses in this section are relative to GDMA-AHB base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description                                   | Address | Access   |
|---|---|---------|----------|
| <b>Interrupt Registers</b>                  |   |         |          |
| <a href="#">AHB_DMA_IN_INT_RAW_CHO_REG</a>  | RX channel 0 raw interrupt status register    | 0x0000  | R/WTC/SS |
| <a href="#">AHB_DMA_IN_INT_ST_CHO_REG</a>   | RX channel 0 masked interrupt status register | 0x0004  | RO       |
| <a href="#">AHB_DMA_IN_INT_ENA_CHO_REG</a>  | RX channel 0 interrupt enable register        | 0x0008  | R/W      |
| <a href="#">AHB_DMA_IN_INT_CLR_CHO_REG</a>  | RX channel 0 interrupt clear register         | 0x000C  | WT       |
| <a href="#">AHB_DMA_IN_INT_RAW_CH1_REG</a>  | RX channel 1 raw interrupt status register    | 0x0010  | R/WTC/SS |
| <a href="#">AHB_DMA_IN_INT_ST_CH1_REG</a>   | RX channel 1 masked interrupt status register | 0x0014  | RO       |
| <a href="#">AHB_DMA_IN_INT_ENA_CH1_REG</a>  | RX channel 1 interrupt enable register        | 0x0018  | R/W      |
| <a href="#">AHB_DMA_IN_INT_CLR_CH1_REG</a>  | RX channel 1 interrupt clear register         | 0x001C  | WT       |
| <a href="#">AHB_DMA_IN_INT_RAW_CH2_REG</a>  | RX channel 2 raw interrupt status register    | 0x0020  | R/WTC/SS |
| <a href="#">AHB_DMA_IN_INT_ST_CH2_REG</a>   | RX channel 2 masked interrupt status register | 0x0024  | RO       |
| <a href="#">AHB_DMA_IN_INT_ENA_CH2_REG</a>  | RX channel 2 interrupt enable register        | 0x0028  | R/W      |
| <a href="#">AHB_DMA_IN_INT_CLR_CH2_REG</a>  | RX channel 2 interrupt clear register         | 0x002C  | WT       |
| <a href="#">AHB_DMA_OUT_INT_RAW_CHO_REG</a> | TX channel 0 raw interrupt status register    | 0x0030  | R/WTC/SS |
| <a href="#">AHB_DMA_OUT_INT_ST_CHO_REG</a>  | TX channel 0 masked interrupt status register | 0x0034  | RO       |
| <a href="#">AHB_DMA_OUT_INT_ENA_CHO_REG</a> | TX channel 0 interrupt enable register        | 0x0038  | R/W      |
| <a href="#">AHB_DMA_OUT_INT_CLR_CHO_REG</a> | TX channel 0 interrupt clear register         | 0x003C  | WT       |
| <a href="#">AHB_DMA_OUT_INT_RAW_CH1_REG</a> | TX channel 1 raw interrupt status register    | 0x0040  | R/WTC/SS |
| <a href="#">AHB_DMA_OUT_INT_ST_CH1_REG</a>  | TX channel 1 masked interrupt status register | 0x0044  | RO       |
| <a href="#">AHB_DMA_OUT_INT_ENA_CH1_REG</a> | TX channel 1 interrupt enable register        | 0x0048  | R/W      |
| <a href="#">AHB_DMA_OUT_INT_CLR_CH1_REG</a> | TX channel 1 interrupt clear register         | 0x004C  | WT       |
| <a href="#">AHB_DMA_OUT_INT_RAW_CH2_REG</a> | TX channel 2 raw interrupt status register    | 0x0050  | R/WTC/SS |

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <a href="#">AHB_DMA_OUT_INT_ST_CH2_REG</a>  | TX channel 2 masked interrupt status register                             | 0x0054  | RO     |
| <a href="#">AHB_DMA_OUT_INT_ENA_CH2_REG</a> | TX channel 2 interrupt enable register                                    | 0x0058  | R/W    |
| <a href="#">AHB_DMA_OUT_INT_CLR_CH2_REG</a> | TX channel 2 interrupt clear register                                     | 0x005C  | WT     |
| <b>Debug Registers</b>                      |   |         |        |
| <a href="#">AHB_DMA_AHB_TEST_REG</a>        | Reserved  | 0x0060  | R/W    |
| <b>Configuration Registers</b>              |   |         |        |
| <a href="#">AHB_DMA_MISC_CONF_REG</a>       | Miscellaneous register  | 0x0064  | R/W    |
| <a href="#">AHB_DMA_IN_CONFO_CHO_REG</a>    | Configuration register 0 of RX channel 0                                  | 0x0070  | R/W    |
| <a href="#">AHB_DMA_IN_CONF1_CHO_REG</a>    | Configuration register 1 of Rx channel 0                                  | 0x0074  | R/W    |
| <a href="#">AHB_DMA_IN_POP_CHO_REG</a>      | Pop control register of RX channel 0                                      | 0x007C  | varies |
| <a href="#">AHB_DMA_IN_LINK_CHO_REG</a>     | Linked list descriptor configuration and control register of RX channel 0 | 0x0080  | varies |
| <a href="#">AHB_DMA_OUT_CONFO_CHO_REG</a>   | Configuration register 0 of TX channel 0                                  | 0x00D0  | R/W    |
| <a href="#">AHB_DMA_OUT_CONF1_CHO_REG</a>   | Configuration register 1 of TX channel 0                                  | 0x00D4  | R/W    |
| <a href="#">AHB_DMA_OUT_PUSH_CHO_REG</a>    | Push control register of TX channel 0                                     | 0x00DC  | varies |
| <a href="#">AHB_DMA_OUT_LINK_CHO_REG</a>    | Linked list descriptor configuration and control register of TX channel 0 | 0x00E0  | varies |
| <a href="#">AHB_DMA_IN_CONFO_CH1_REG</a>    | Configuration register 0 of RX channel 1                                  | 0x0130  | R/W    |
| <a href="#">AHB_DMA_IN_CONF1_CH1_REG</a>    | Configuration register 1 of RX channel 1                                  | 0x0134  | R/W    |
| <a href="#">AHB_DMA_IN_POP_CH1_REG</a>      | Pop control register of RX channel 1                                      | 0x013C  | varies |
| <a href="#">AHB_DMA_IN_LINK_CH1_REG</a>     | Linked list descriptor configuration and control register of RX channel 1 | 0x0140  | varies |
| <a href="#">AHB_DMA_OUT_CONFO_CH1_REG</a>   | Configuration register 0 of TX channel 1                                  | 0x0190  | R/W    |
| <a href="#">AHB_DMA_OUT_CONF1_CH1_REG</a>   | Configuration register 1 of TX channel 1                                  | 0x0194  | R/W    |
| <a href="#">AHB_DMA_OUT_PUSH_CH1_REG</a>    | Push control register of TX channel 1                                     | 0x019C  | varies |
| <a href="#">AHB_DMA_OUT_LINK_CH1_REG</a>    | Linked list descriptor configuration and control register of TX channel 1 | 0x01A0  | varies |
| <a href="#">AHB_DMA_IN_CONFO_CH2_REG</a>    | Configuration register 0 of RX channel 2                                  | 0x01F0  | R/W    |
| <a href="#">AHB_DMA_IN_CONF1_CH2_REG</a>    | Configuration register 1 of RX channel 2                                  | 0x01F4  | R/W    |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AHB_DMA_IN_POP_CH2_REG</a>                 | Pop control register of RX channel 2                                      | 0x01FC  | varies |
| <a href="#">AHB_DMA_IN_LINK_CH2_REG</a>                | Linked list descriptor configuration and control register of RX channel 2 | 0x0200  | varies |
| <a href="#">AHB_DMA_OUT_CONF0_CH2_REG</a>              | Configuration register 0 of TX channel 2                                  | 0x0250  | R/W    |
| <a href="#">AHB_DMA_OUT_CONF1_CH2_REG</a>              | Configuration register 1 of TX channel 2                                  | 0x0254  | R/W    |
| <a href="#">AHB_DMA_OUT_PUSH_CH2_REG</a>               | Push control register of TX channel 2                                     | 0x025C  | varies |
| <a href="#">AHB_DMA_OUT_LINK_CH2_REG</a>               | Linked list descriptor configuration and control register of TX channel 2 | 0x0260  | varies |
| <a href="#">AHB_DMA_OUT_CRC_INIT_DATA_CHO_REG</a>      | TX channel 0 CRC initial value configuration register                     | 0x02BC  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_WIDTH_CHO_REG</a>           | TX channel 0 CRC result width configuration register                      | 0x02C0  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_CLEAR_CHO_REG</a>          | TX channel 0 CRC result clear register                                    | 0x02C4  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_FINAL_RESULT_CHO_REG</a>   | TX channel 0 CRC result register  | 0x02C8  | RO     |
| <a href="#">AHB_DMA_TX_CRC_EN_WR_DATA_CHO_REG</a>      | CRC TX channel 0 CRC intermediate result mask register                    | 0x02CC  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_EN_ADDR_CHO_REG</a>         | TX channel 0 CRC intermediate result mask target register                 | 0x02D0  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_WR_DATA_CHO_REG</a> | TX channel 0 CRC data input mask register                                 | 0x02D4  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_ADDR_CHO_REG</a>    | TX channel 0 CRC data input mask target register                          | 0x02D8  | R/W    |
| <a href="#">AHB_DMA_TX_CH_ARB_WEIGHT_CHO_REG</a>       | TX channel 0 arbitration weight configuration register                    | 0x02DC  | R/W    |
| <a href="#">AHB_DMA_TX_ARB_WEIGHT_OPT_DIR_CHO_REG</a>  | TX channel 0 weight arbitration optimization enable register              | 0x02E0  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_INIT_DATA_CH1_REG</a>      | TX channel 1 CRC initial value configuration register                     | 0x02E4  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_WIDTH_CH1_REG</a>           | TX channel 1 CRC result width configuration register                      | R/W     |        |
| <a href="#">AHB_DMA_OUT_CRC_CLEAR_CH1_REG</a>          | TX channel 1 CRC result clear register                                    | 0x02EC  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_FINAL_RESULT_CH1_REG</a>   | TX channel 1 CRC result register  | 0x02F0  | RO     |
| <a href="#">AHB_DMA_TX_CRC_EN_WR_DATA_CH1_REG</a>      | TX channel 1 CRC intermediate result mask register                        | 0x02F4  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_EN_ADDR_CH1_REG</a>         | TX channel 1 CRC intermediate result mask target register                 | 0x02F8  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_WR_DATA_CH1_REG</a> | TX channel 1 CRC data input mask register                                 | 0x02FC  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_ADDR_CH1_REG</a>    | TX channel 1 CRC data input mask target register                          | 0x0300  | R/W    |
| <a href="#">AHB_DMA_TX_CH_ARB_WEIGHT_CH1_REG</a>       | TX channel 1 arbitration weight configuration register                    | 0x0304  | R/W    |
| <a href="#">AHB_DMA_TX_ARB_WEIGHT_OPT_DIR_CH1_REG</a>  | TX channel 1 weight arbitration optimization enable register              | 0x0308  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_INIT_DATA_CH2_REG</a>      | TX channel 2 CRC initial value configuration register                     | 0x030C  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">AHB_DMA_TX_CRC_WIDTH_CH2_REG</a>           | TX channel 2 CRC result width configuration register         | 0x0310  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_CLEAR_CH2_REG</a>          | TX channel 2 CRC result clear register                       | 0x0314  | R/W    |
| <a href="#">AHB_DMA_OUT_CRC_FINAL_RESULT_CH2_REG</a>   | TX channel 2 CRC result register                             | 0x0318  | RO     |
| <a href="#">AHB_DMA_TX_CRC_EN_WR_DATA_CH2_REG</a>      | TX channel 2 CRC intermediate result mask register           | 0x031C  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_EN_ADDR_CH2_REG</a>         | TX channel 2 CRC intermediate result mask target register    | 0x0320  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_WR_DATA_CH2_REG</a> | TX channel 2 CRC data input mask register                    | 0x0324  | R/W    |
| <a href="#">AHB_DMA_TX_CRC_DATA_EN_ADDR_CH2_REG</a>    | TX channel 2 CRC data input mask target register             | 0x0328  | R/W    |
| <a href="#">AHB_DMA_TX_CH_ARB_WEIGHT_CH2_REG</a>       | TX channel 2 arbitration weight configuration register       | 0x032C  | R/W    |
| <a href="#">AHB_DMA_TX_ARB_WEIGHT_OPT_DIR_CH2_REG</a>  | TX channel 2 weight arbitration optimization enable register | 0x0330  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_INIT_DATA_CHO_REG</a>       | RX channel 0 CRC initial value configuration register        | 0x0334  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_WIDTH_CHO_REG</a>           | RX channel 0 CRC result width configuration register         | 0x0338  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_CLEAR_CHO_REG</a>           | RX channel 0 CRC result clear register                       | 0x033C  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_FINAL_RESULT_CHO_REG</a>    | RX channel 0 CRC result register                             | 0x0340  | RO     |
| <a href="#">AHB_DMA_RX_CRC_EN_WR_DATA_CHO_REG</a>      | RX channel 0 CRC intermediate result mask register           | 0x0344  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_EN_ADDR_CHO_REG</a>         | RX channel 0 CRC data input mask target register             | 0x0348  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_WR_DATA_CHO_REG</a> | RX channel 0 CRC data input mask register                    | 0x034C  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_ADDR_CHO_REG</a>    | RX channel 0 CRC data input mask target register             | 0x0350  | R/W    |
| <a href="#">AHB_DMA_RX_CH_ARB_WEIGHT_CHO_REG</a>       | RX channel 0 arbitration weight configuration register       | 0x0354  | R/W    |
| <a href="#">AHB_DMA_RX_ARB_WEIGHT_OPT_DIR_CHO_REG</a>  | RX channel 0 weight arbitration optimization enable register | 0x0358  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_INIT_DATA_CH1_REG</a>       | RX channel 1 CRC initial value configuration register        | 0x035C  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_WIDTH_CH1_REG</a>           | RX channel 1 CRC result width configuration register         | 0x0360  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_CLEAR_CH1_REG</a>           | RX channel 1 CRC result clear register                       | 0x0364  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_FINAL_RESULT_CH1_REG</a>    | RX channel 1 CRC result register                             | 0x0368  | RO     |
| <a href="#">AHB_DMA_RX_CRC_EN_WR_DATA_CH1_REG</a>      | RX channel 1 CRC intermediate result mask register           | 0x036C  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_EN_ADDR_CH1_REG</a>         | RX channel 1 CRC data input mask target register             | 0x0370  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_WR_DATA_CH1_REG</a> | RX channel 1 CRC data input mask register                    | 0x0374  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_ADDR_CH1_REG</a>    | RX channel 1 CRC data input mask target register             | 0x0378  | R/W    |
| <a href="#">AHB_DMA_RX_CH_ARB_WEIGHT_CH1_REG</a>       | RX channel 1 arbitration weight configuration register       | 0x037C  | R/W    |
| <a href="#">AHB_DMA_RX_ARB_WEIGHT_OPT_DIR_CH1_REG</a>  | RX channel 1 weight arbitration optimization enable register | 0x0380  | R/W    |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AHB_DMA_IN_CRC_INIT_DATA_CH2_REG</a>       | RX channel 2 CRC initial value configuration register         | 0x0384  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_WIDTH_CH2_REG</a>           | RX channel 2 CRC result width configuration register          | 0x0388  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_CLEAR_CH2_REG</a>           | RX channel 2 CRC result clear register                        | 0x038C  | R/W    |
| <a href="#">AHB_DMA_IN_CRC_FINAL_RESULT_CH2_REG</a>    | RX channel 2 CRC result register                              | 0x0390  | RO     |
| <a href="#">AHB_DMA_RX_CRC_EN_WR_DATA_CH2_REG</a>      | RX channel 2 CRC intermediate result mask register            | 0x0394  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_EN_ADDR_CH2_REG</a>         | RX channel 2 CRC data input mask target register              | 0x0398  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_WR_DATA_CH2_REG</a> | RX channel 2 CRC data input mask register                     | 0x039C  | R/W    |
| <a href="#">AHB_DMA_RX_CRC_DATA_EN_ADDR_CH2_REG</a>    | RX channel 2 CRC data input mask target register              | 0x03A0  | R/W    |
| <a href="#">AHB_DMA_RX_CH_ARB_WEIGHT_CH2_REG</a>       | RX channel 2 arbitration weight configuration register        | 0x03A4  | R/W    |
| <a href="#">AHB_DMA_RX_ARB_WEIGHT_OPT_DIR_CH2_REG</a>  | RX channel 2 weight arbitration optimization enable register  | 0x03A8  | R/W    |
| <a href="#">AHB_DMA_IN_LINK_ADDR_CHO_REG</a>           | Linked list descriptor configuration register of RX channel 0 | 0x03AC  | R/W    |
| <a href="#">AHB_DMA_IN_LINK_ADDR_CH1_REG</a>           | Linked list descriptor configuration register of RX channel 1 | 0x03B0  | R/W    |
| <a href="#">AHB_DMA_IN_LINK_ADDR_CH2_REG</a>           | Linked list descriptor configuration register of RX channel 2 | 0x03B4  | R/W    |
| <a href="#">AHB_DMA_OUT_LINK_ADDR_CHO_REG</a>          | Linked list descriptor configuration register of TX channel 0 | 0x03B8  | R/W    |
| <a href="#">AHB_DMA_OUT_LINK_ADDR_CH1_REG</a>          | Linked list descriptor configuration register of TX channel 1 | 0x03BC  | R/W    |
| <a href="#">AHB_DMA_OUT_LINK_ADDR_CH2_REG</a>          | Linked list descriptor configuration register of TX channel 2 | 0x03C0  | R/W    |
| <a href="#">AHB_DMA_INTR_MEM_START_ADDR_REG</a>        | Accessible address space start address configuration register | 0x03C4  | R/W    |
| <a href="#">AHB_DMA_INTR_MEM_END_ADDR_REG</a>          | Accessible address space end address configuration register   | 0x03C8  | R/W    |
| <a href="#">AHB_DMA_ARB_TIMEOUT_TX_REG</a>             | TX Arbitration timeout configuration register                 | 0x03CC  | R/W    |
| <a href="#">AHB_DMA_ARB_TIMEOUT_RX_REG</a>             | RX Arbitration timeout configuration register                 | 0x03D0  | R/W    |
| <a href="#">AHB_DMA_WEIGHT_EN_TX_REG</a>               | TX weight arbitration enable register                         | 0x03D4  | R/W    |
| <a href="#">AHB_DMA_WEIGHT_EN_RX_REG</a>               | RX weight arbitration enable register                         | 0x03D8  | R/W    |
| <b>Version Register</b>                                |   |         |        |
| <a href="#">AHB_DMA_DATE_REG</a>                       | Version control register                                      | 0x0068  | R/W    |
| <b>Status Registers</b>                                |   |         |        |
| <a href="#">AHB_DMA_INFIFO_STATUS_CHO_REG</a>          | RX channel 0 FIFO status                                      | 0x0078  | RO     |
| <a href="#">AHB_DMA_IN_STATE_CHO_REG</a>               | RX channel 0 status   | 0x0084  | RO     |
| <a href="#">AHB_DMA_IN_SUC_EOF_DES_ADDR_CHO_REG</a>    | Receive descriptor address when EOF occurs on RX channel 0    | 0x0088  | RO     |
| <a href="#">AHB_DMA_IN_ERR_EOF_DES_ADDR_CHO_REG</a>    | Receive descriptor address when errors occur on RX channel 0  | 0x008C  | RO     |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AHB_DMA_IN_DSCR_CHO_REG</a>              | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 0   | 0x0090  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BFO_CHO_REG</a>          | Address of the current pre-read receive descriptor on RX channel 0  | 0x0094  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BF1_CHO_REG</a>          | Address of the previous pre-read receive descriptor on RX channel 0   | 0x0098  | RO     |
| <a href="#">AHB_DMA_OUTFIFO_STATUS_CHO_REG</a>       | TX channel 0 FIFO status  | 0x00D8  | RO     |
| <a href="#">AHB_DMA_OUT_STATE_CHO_REG</a>            | TX channel 0 status   | 0x00E4  | RO     |
| <a href="#">AHB_DMA_OUT_EOF_DES_ADDR_CHO_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 0   | 0x00E8  | RO     |
| <a href="#">AHB_DMA_OUT_EOF_BFR_DES_ADDR_CHO_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 0  | 0x00EC  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_CHO_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 0 | 0x00F0  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_BFO_CHO_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 0   | 0x00F4  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_BF1_CHO_REG</a>         | Address of the previous pre-read transmit descriptor on TX channel 0  | 0x00F8  | RO     |
| <a href="#">AHB_DMA_INFIFO_STATUS_CH1_REG</a>        | RX channel 1 FIFO status  | 0x0138  | RO     |
| <a href="#">AHB_DMA_IN_STATE_CH1_REG</a>             | RX channel 1 status   | 0x0144  | RO     |
| <a href="#">AHB_DMA_IN_SUC_EOF_DES_ADDR_CH1_REG</a>  | Receive descriptor address when EOF occurs on RX channel 1  | 0x0148  | RO     |
| <a href="#">AHB_DMA_IN_ERR_EOF_DES_ADDR_CH1_REG</a>  | Receive descriptor address when errors occur on RX channel 1  | 0x014C  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_CH1_REG</a>              | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 1   | 0x0150  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BFO_CH1_REG</a>          | Address of the current pre-read receive descriptor on RX channel 1  | 0x0154  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BF1_CH1_REG</a>          | Address of the previous pre-read receive descriptor on RX channel 1   | 0x0158  | RO     |
| <a href="#">AHB_DMA_OUTFIFO_STATUS_CH1_REG</a>       | TX channel 1 FIFO status  | 0x0198  | RO     |
| <a href="#">AHB_DMA_OUT_STATE_CH1_REG</a>            | TX channel 1 status   | 0x01A4  | RO     |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AHB_DMA_OUT_EOF_DES_ADDR_CH1_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 1   | 0x01A8  | RO     |
| <a href="#">AHB_DMA_OUT_EOF_BFR_DES_ADDR_CH1_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 1  | 0x01AC  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_CH1_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 1 | 0x01B0  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_BFO_CH1_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 1   | 0x01B4  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_BF1_CH1_REG</a>         | Address of the previous pre-read transmit descriptor on TX channel 1  | 0x01B8  | RO     |
| <a href="#">AHB_DMA_INFIFO_STATUS_CH2_REG</a>        | RX channel 2 FIFO status  | 0x01F8  | RO     |
| <a href="#">AHB_DMA_IN_STATE_CH2_REG</a>             | RX channel 2 status   | 0x0204  | RO     |
| <a href="#">AHB_DMA_IN_SUC_EOF_DES_ADDR_CH2_REG</a>  | Receive descriptor address when EOF occurs on RX channel 2  | 0x0208  | RO     |
| <a href="#">AHB_DMA_IN_ERR_EOF_DES_ADDR_CH2_REG</a>  | Receive descriptor address when errors occur on RX channel 2  | 0x020C  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_CH2_REG</a>              | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 2   | 0x0210  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BFO_CH2_REG</a>          | Address of the current pre-read receive descriptor on RX channel 2  | 0x0214  | RO     |
| <a href="#">AHB_DMA_IN_DSCR_BF1_CH2_REG</a>          | Address of the previous pre-read receive descriptor on RX channel 2   | 0x0218  | RO     |
| <a href="#">AHB_DMA_OUTFIFO_STATUS_CH2_REG</a>       | TX channel 2 FIFO status  | 0x0258  | RO     |
| <a href="#">AHB_DMA_OUT_STATE_CH2_REG</a>            | TX channel 2 status   | 0x0264  | RO     |
| <a href="#">AHB_DMA_OUT_EOF_DES_ADDR_CH2_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 2   | 0x0268  | RO     |
| <a href="#">AHB_DMA_OUT_EOF_BFR_DES_ADDR_CH2_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 2  | 0x026C  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_CH2_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 2 | 0x0270  | RO     |
| <a href="#">AHB_DMA_OUT_DSCR_BFO_CH2_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 2   | 0x0274  | RO     |



| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">AHB_DMA_OUT_DSCR_BF1_CH2_REG</a> | Address of the previous pre-read transmit descriptor on TX channel 2 | 0x0278  | RO     |
| <b>Priority Registers</b>                    |  |         |        |
| <a href="#">AHB_DMA_IN_PRI_CHO_REG</a>       | Priority register of RX channel 0                                    | 0x009C  | R/W    |
| <a href="#">AHB_DMA_OUT_PRI_CHO_REG</a>      | Priority register of TX channel 0                                    | 0x00FC  | R/W    |
| <a href="#">AHB_DMA_IN_PRI_CH1_REG</a>       | Priority register of RX channel 1                                    | 0x015C  | R/W    |
| <a href="#">AHB_DMA_OUT_PRI_CH1_REG</a>      | Priority register of TX channel 1                                    | 0x01BC  | R/W    |
| <a href="#">AHB_DMA_IN_PRI_CH2_REG</a>       | Priority register of RX channel 2                                    | 0x021C  | R/W    |
| <a href="#">AHB_DMA_OUT_PRI_CH2_REG</a>      | Priority register of TX channel 2                                    | 0x027C  | R/W    |
| <b>Peripheral Select Registers</b>           |  |         |        |
| <a href="#">AHB_DMA_IN_PERI_SEL_CHO_REG</a>  | Peripheral selection register of RX channel 0                        | 0x00A0  | R/W    |
| <a href="#">AHB_DMA_OUT_PERI_SEL_CHO_REG</a> | Peripheral selection register of TX channel 0                        | 0x0100  | R/W    |
| <a href="#">AHB_DMA_IN_PERI_SEL_CH1_REG</a>  | Peripheral selection register of RX channel 1                        | 0x0160  | R/W    |
| <a href="#">AHB_DMA_OUT_PERI_SEL_CH1_REG</a> | Peripheral selection register of TX channel 1                        | 0x01C0  | R/W    |
| <a href="#">AHB_DMA_IN_PERI_SEL_CH2_REG</a>  | Peripheral selection register of RX channel 2                        | 0x0220  | R/W    |
| <a href="#">AHB_DMA_OUT_PERI_SEL_CH2_REG</a> | Peripheral selection register of TX channel 2                        | 0x0280  | R/W    |

### 3.8.2 GDMA-AXI Register Summary

The addresses in this section are relative to GDMA-AXI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                       | Description                                   | Address | Access   |
|--|---|---------|----------|
| <b>Interrupt Registers</b>                 |   |         |          |
| <a href="#">AXI_DMA_IN_INT_RAW_CHO_REG</a> | RX channel 0 raw interrupt status register    | 0x0000  | R/WTC/SS |
| <a href="#">AXI_DMA_IN_INT_ST_CHO_REG</a>  | RX channel 0 masked interrupt status register | 0x0004  | RO       |
| <a href="#">AXI_DMA_IN_INT_ENA_CHO_REG</a> | RX channel 0 interrupt enable register        | 0x0008  | R/W      |
| <a href="#">AXI_DMA_IN_INT_CLR_CHO_REG</a> | RX channel 0 interrupt clear register         | 0x000C  | WT       |



| Name   | Description   | Address | Access   |
|--|---|---------|----------|
| <a href="#">AXI_DMA_IN_INT_RAW_CH1_REG</a>       | RX channel 1 raw interrupt status register                                  | 0x0068  | R/WTC/SS |
| <a href="#">AXI_DMA_IN_INT_ST_CH1_REG</a>        | RX channel 1 masked interrupt status register                               | 0x006C  | RO       |
| <a href="#">AXI_DMA_IN_INT_ENA_CH1_REG</a>       | RX channel 1 interrupt enable register                                      | 0x0070  | R/W      |
| <a href="#">AXI_DMA_IN_INT_CLR_CH1_REG</a>       | RX channel 1 interrupt clear register                                       | 0x0074  | WT       |
| <a href="#">AXI_DMA_IN_INT_RAW_CH2_REG</a>       | RX channel 2 raw interrupt status register                                  | 0x00D0  | R/WTC/SS |
| <a href="#">AXI_DMA_IN_INT_ST_CH2_REG</a>        | RX channel 2 masked interrupt status register                               | 0x00D4  | RO       |
| <a href="#">AXI_DMA_IN_INT_ENA_CH2_REG</a>       | RX channel 2 interrupt enable register                                      | 0x00D8  | R/W      |
| <a href="#">AXI_DMA_IN_INT_CLR_CH2_REG</a>       | RX channel 2 interrupt clear register                                       | 0x00DC  | WT       |
| <a href="#">AXI_DMA_OUT_INT_RAW_CHO_REG</a>      | TX channel 0 raw interrupt status register                                  | 0x0138  | R/WTC/SS |
| <a href="#">AXI_DMA_OUT_INT_ST_CHO_REG</a>       | TX channel 0 masked interrupt status register                               | 0x013C  | RO       |
| <a href="#">AXI_DMA_OUT_INT_ENA_CHO_REG</a>      | TX channel 0 interrupt enable register                                      | 0x0140  | R/W      |
| <a href="#">AXI_DMA_OUT_INT_CLR_CHO_REG</a>      | TX channel 0 interrupt clear register                                       | 0x0144  | WT       |
| <a href="#">AXI_DMA_OUT_INT_RAW_CH1_REG</a>      | TX channel 1 raw interrupt status register                                  | 0x01A0  | R/WTC/SS |
| <a href="#">AXI_DMA_OUT_INT_ST_CH1_REG</a>       | TX channel 1 masked interrupt status register                               | 0x01A4  | RO       |
| <a href="#">AXI_DMA_OUT_INT_ENA_CH1_REG</a>      | TX channel 1 interrupt enable register                                      | 0x01A8  | R/W      |
| <a href="#">AXI_DMA_OUT_INT_CLR_CH1_REG</a>      | TX channel 1 interrupt clear register                                       | 0x01AC  | WT       |
| <a href="#">AXI_DMA_OUT_INT_RAW_CH2_REG</a>      | TX channel 2 raw interrupt status register                                  | 0x0208  | R/WTC/SS |
| <a href="#">AXI_DMA_OUT_INT_ST_CH2_REG</a>       | TX channel 2 masked interrupt status register                               | 0x020C  | RO       |
| <a href="#">AXI_DMA_OUT_INT_ENA_CH2_REG</a>      | TX channel 2 interrupt enable register                                      | 0x0210  | R/W      |
| <a href="#">AXI_DMA_OUT_INT_CLR_CH2_REG</a>      | TX channel 2 interrupt clear register                                       | 0x0214  | WT       |
| <b>Configuration Registers</b>                   |   |         |          |
| <a href="#">AXI_DMA_IN_CONFO_CHO_REG</a>         | Configuration register 0 of RX channel 0                                    | 0x0010  | R/W      |
| <a href="#">AXI_DMA_IN_CONF1_CHO_REG</a>         | Configuration register 1 of RX channel 0                                    | 0x0014  | R/W      |
| <a href="#">AXI_DMA_IN_POP_CHO_REG</a>           | Pop control register of RX channel 0  | 0x001C  | varies   |
| <a href="#">AXI_DMA_IN_LINK1_CHO_REG</a>         | Linked list descriptor configuration and control register 1 of RX channel 0 | 0x0020  | varies   |
| <a href="#">AXI_DMA_IN_LINK2_CHO_REG</a>         | Linked list descriptor configuration and control register 2 of RX channel 0 | 0x0024  | R/W      |
| <a href="#">AXI_DMA_IN_CRC_INIT_DATA_CHO_REG</a> | RX channel 0 CRC initial value configuration register                       | 0x0048  | R/W      |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AXI_DMA_RX_CRC_WIDTH_CHO_REG</a>           | RX channel 0 CRC result width configuration register                        | 0x004C  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_CLEAR_CHO_REG</a>           | RX channel 0 CRC result clear register                                      | 0x0050  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_FINAL_RESULT_CHO_REG</a>    | RX channel 0 CRC result register  | 0x0054  | RO     |
| <a href="#">AXI_DMA_RX_CRC_EN_ADDR_CHO_REG</a>         | TX channel 0 CRC intermediate result mask target register                   | 0x005C  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_WR_DATA_CHO_REG</a> | CRC RX channel 0 CRC intermediate result mask register                      | 0x0060  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_ADDR_CHO_REG</a>    | RX channel 0 CRC data input mask target register                            | 0x0064  | R/W    |
| <a href="#">AXI_DMA_IN_CONFO_CH1_REG</a>               | Configuration register 0 of RX channel 1                                    | 0x0078  | R/W    |
| <a href="#">AXI_DMA_IN_CONF1_CH1_REG</a>               | Configuration register 1 of RX channel 1                                    | 0x007C  | R/W    |
| <a href="#">AXI_DMA_IN_POP_CH1_REG</a>                 | Pop control register of RX channel 1  | 0x0084  | varies |
| <a href="#">AXI_DMA_IN_LINK1_CH1_REG</a>               | Linked list descriptor configuration and control register 1 of RX channel 1 | 0x0088  | varies |
| <a href="#">AXI_DMA_IN_LINK2_CH1_REG</a>               | Linked list descriptor configuration and control register 2 of RX channel 1 | 0x008C  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_INIT_DATA_CH1_REG</a>       | RX channel 1 CRC initial value configuration register                       | 0x00B0  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_WIDTH_CH1_REG</a>           | RX channel 1 CRC result width configuration register                        | 0x00B4  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_CLEAR_CH1_REG</a>           | RX channel 1 CRC result clear register                                      | 0x00B8  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_FINAL_RESULT_CH1_REG</a>    | RX channel 1 CRC result register  | 0x00BC  | RO     |
| <a href="#">AXI_DMA_RX_CRC_EN_ADDR_CH1_REG</a>         | RX channel 1 CRC intermediate result mask target register                   | 0x00C4  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_WR_DATA_CH1_REG</a> | CRC RX channel 1 CRC intermediate result mask register                      | 0x00C8  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_ADDR_CH1_REG</a>    | RX channel 1 CRC data input mask target register                            | 0x00CC  | R/W    |
| <a href="#">AXI_DMA_IN_CONFO_CH2_REG</a>               | Configuration register 0 of RX channel 2                                    | 0x00E0  | R/W    |
| <a href="#">AXI_DMA_IN_CONF1_CH2_REG</a>               | Configuration register 1 of RX channel 2                                    | 0x00E4  | R/W    |
| <a href="#">AXI_DMA_IN_POP_CH2_REG</a>                 | Pop control register of RX channel 2  | 0x00EC  | varies |
| <a href="#">AXI_DMA_IN_LINK1_CH2_REG</a>               | Linked list descriptor configuration and control register 1 of RX channel 2 | 0x00F0  | varies |
| <a href="#">AXI_DMA_IN_LINK2_CH2_REG</a>               | Linked list descriptor configuration and control register 2 of RX channel 2 | 0x00F4  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_INIT_DATA_CH2_REG</a>       | RX channel 2 CRC initial value configuration register                       | 0x0118  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_WIDTH_CH2_REG</a>           | RX channel 2 CRC result width configuration register                        | 0x011C  | R/W    |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AXI_DMA_IN_CRC_CLEAR_CH2_REG</a>           | RX channel 2 CRC result clear register                                      | 0x0120  | R/W    |
| <a href="#">AXI_DMA_IN_CRC_FINAL_RESULT_CH2_REG</a>    | RX channel 2 CRC result register  | 0x0124  | RO     |
| <a href="#">AXI_DMA_RX_CRC_EN_ADDR_CH2_REG</a>         | RX channel 2 CRC intermediate result mask target register                   | 0x012C  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_WR_DATA_CH2_REG</a> | CRC RX channel 2 CRC intermediate result mask register                      | 0x0130  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_DATA_EN_ADDR_CH2_REG</a>    | RX channel 2 CRC data input mask target register                            | 0x0134  | R/W    |
| <a href="#">AXI_DMA_OUT_CONFO_CHO_REG</a>              | Configuration register 0 of TX channel 0                                    | 0x0148  | R/W    |
| <a href="#">AXI_DMA_OUT_CONF1_CHO_REG</a>              | Configuration register 1 of TX channel 0                                    | 0x014C  | R/W    |
| <a href="#">AXI_DMA_OUT_PUSH_CHO_REG</a>               | Push control register of TX channel 0                                       | 0x0154  | varies |
| <a href="#">AXI_DMA_OUT_LINK1_CHO_REG</a>              | Linked list descriptor configuration and control register 1 of TX channel 0 | 0x0158  | varies |
| <a href="#">AXI_DMA_OUT_LINK2_CHO_REG</a>              | Linked list descriptor configuration and control register 2 of TX channel 0 | 0x015C  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_INIT_DATA_CHO_REG</a>      | TX channel 0 CRC initial value configuration register                       | 0x0180  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_WIDTH_CHO_REG</a>           | TX channel 0 CRC result width configuration register                        | 0x0184  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_CLEAR_CHO_REG</a>          | TX channel 0 CRC result clear register                                      | 0x0188  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_FINAL_RESULT_CHO_REG</a>   | TX channel 0 CRC result register  | 0x018C  | RO     |
| <a href="#">AXI_DMA_TX_CRC_EN_WR_DATA_CHO_REG</a>      | CRC TX channel 0 CRC intermediate result mask register                      | 0x0190  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_EN_ADDR_CHO_REG</a>         | TX channel 0 CRC intermediate result mask target register                   | 0x0194  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_WR_DATA_CHO_REG</a> | TX channel 0 CRC data input mask register                                   | 0x0198  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_ADDR_CHO_REG</a>    | TX channel 0 CRC data input mask target register                            | 0x019C  | R/W    |
| <a href="#">AXI_DMA_OUT_CONFO_CH1_REG</a>              | Configuration register 0 of TX channel 1                                    | 0x01B0  | R/W    |
| <a href="#">AXI_DMA_OUT_CONF1_CH1_REG</a>              | Configuration register 1 of TX channel 1                                    | 0x01B4  | R/W    |
| <a href="#">AXI_DMA_OUT_PUSH_CH1_REG</a>               | Push control register of TX channel 1                                       | 0x01BC  | varies |
| <a href="#">AXI_DMA_OUT_LINK1_CH1_REG</a>              | Linked list descriptor configuration and control register 1 of TX channel 1 | 0x01C0  | varies |
| <a href="#">AXI_DMA_OUT_LINK2_CH1_REG</a>              | Linked list descriptor configuration and control register 2 of TX channel 1 | 0x01C4  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_INIT_DATA_CH1_REG</a>      | TX channel 1 CRC initial value configuration register                       | 0x01E8  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_WIDTH_CH1_REG</a>           | TX channel 1 CRC result width configuration register                        | 0x01EC  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">AXI_DMA_OUT_CRC_CLEAR_CH1_REG</a>          | TX channel 1 CRC result clear register                                       | 0x01F0  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_FINAL_RESULT_CH1_REG</a>   | TX channel 1 CRC result register   | 0x01F4  | RO     |
| <a href="#">AXI_DMA_TX_CRC_EN_WR_DATA_CH1_REG</a>      | CRC TX channel 1 CRC intermediate result mask register                       | 0x01F8  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_EN_ADDR_CH1_REG</a>         | TX channel 1 CRC intermediate result mask target register                    | 0x01FC  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_WR_DATA_CH1_REG</a> | TX channel 1 CRC data input mask target register                             | 0x0200  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_ADDR_CH1_REG</a>    | TX channel 1 CRC data input mask target register                             | 0x0204  | R/W    |
| <a href="#">AXI_DMA_OUT_CONFO_CH2_REG</a>              | Configuration register 0 of TX channel 2                                     | 0x0218  | R/W    |
| <a href="#">AXI_DMA_OUT_CONF1_CH2_REG</a>              | Configuration register 1 of TX channel 2                                     | 0x021C  | R/W    |
| <a href="#">AXI_DMA_OUT_PUSH_CH2_REG</a>               | Push control register of TX channel 2  | 0x0224  | varies |
| <a href="#">AXI_DMA_OUT_LINK1_CH2_REG</a>              | Linked list descriptor configuration and control register of TX channel 2    | 0x0228  | varies |
| <a href="#">AXI_DMA_OUT_LINK2_CH2_REG</a>              | Linked list descriptor configuration and control register 2 1of TX channel 2 | 0x022C  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_INIT_DATA_CH2_REG</a>      | TX channel 2 CRC initial value configuration register                        | 0x0250  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_WIDTH_CH2_REG</a>           | TX channel 2 CRC result width configuration register                         | 0x0254  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_CLEAR_CH2_REG</a>          | TX channel 2 CRC result clear register                                       | 0x0258  | R/W    |
| <a href="#">AXI_DMA_OUT_CRC_FINAL_RESULT_CH2_REG</a>   | TX channel 2 CRC result register   | 0x025C  | RO     |
| <a href="#">AXI_DMA_TX_CRC_EN_WR_DATA_CH2_REG</a>      | CRC TX channel 2 CRC intermediate result mask register                       | 0x0260  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_EN_ADDR_CH2_REG</a>         | TX channel 2 CRC intermediate result mask target register                    | 0x0264  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_WR_DATA_CH2_REG</a> | TX channel 2 CRC data input mask target register                             | 0x0268  | R/W    |
| <a href="#">AXI_DMA_TX_CRC_DATA_EN_ADDR_CH2_REG</a>    | TX channel 2 CRC data input mask target register                             | 0x026C  | R/W    |
| <a href="#">AXI_DMA_ARB_TIMEOUT_REG</a>                | Arbitration timeout configuration register                                   | 0x0270  | R/W    |
| <a href="#">AXI_DMA_WEIGHT_EN_REG</a>                  | Weight arbitration enable register   | 0x0274  | R/W    |
| <a href="#">AXI_DMA_IN_MEM_CONF_REG</a>                | Internal memory power configuration register for RX channel                  | 0x0278  | R/W    |
| <a href="#">AXI_DMA_INTR_MEM_START_ADDR_REG</a>        | Accessible internal memory start address configuration register              | 0x027C  | R/W    |
| <a href="#">AXI_DMA_INTR_MEM_END_ADDR_REG</a>          | Accessible internal memory end address configuration register                | 0x0280  | R/W    |
| <a href="#">AXI_DMA_EXTR_MEM_START_ADDR_REG</a>        | Accessible external memory start address configuration register              | 0x0284  | R/W    |
| <a href="#">AXI_DMA_EXTR_MEM_END_ADDR_REG</a>          | Accessible external memory end address configuration register                | 0x0288  | R/W    |
| <a href="#">AXI_DMA_IN_RESET_AVAIL_CHO_REG</a>         | RX channel 0 reset status register   | 0x028C  | RO     |

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <a href="#">AXI_DMA_IN_RESET_AVAIL_CH1_REG</a>      | RX channel 1 reset status register  | 0x0290  | RO     |
| <a href="#">AXI_DMA_IN_RESET_AVAIL_CH2_REG</a>      | RX channel 2 reset status register  | 0x0294  | RO     |
| <a href="#">AXI_DMA_OUT_RESET_AVAIL_CHO_REG</a>     | TX channel 0 reset status register  | 0x0298  | RO     |
| <a href="#">AXI_DMA_OUT_RESET_AVAIL_CH1_REG</a>     | TX channel 1 reset status register  | 0x029C  | RO     |
| <a href="#">AXI_DMA_OUT_RESET_AVAIL_CH2_REG</a>     | TX channel 2 reset status register  | 0x02A0  | RO     |
| <a href="#">AXI_DMA_MISC_CONF_REG</a>               | Miscellaneous register  | 0x02A8  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_EN_WR_DATA_CHO_REG</a>   | CRC RX channel 0 CRC intermediate result mask register  | 0x0058  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_EN_WR_DATA_CH1_REG</a>   | CRC RX channel 1 CRC intermediate result mask register  | 0x00C0  | R/W    |
| <a href="#">AXI_DMA_RX_CRC_EN_WR_DATA_CH2_REG</a>   | CRC RX channel 2 CRC intermediate result mask register  | 0x0128  | R/W    |
| <b>Status Registers</b>                             |   |         |        |
| <a href="#">AXI_DMA_INFIFO_STATUS_CHO_REG</a>       | RX channel 0 FIFO status register   | 0x0018  | RO     |
| <a href="#">AXI_DMA_IN_STATE_CHO_REG</a>            | RX channel 0 status register  | 0x0028  | RO     |
| <a href="#">AXI_DMA_IN_SUC_EOF_DES_ADDR_CHO_REG</a> | Receive descriptor address when EOF occurs on RX channel 0  | 0x002C  | RO     |
| <a href="#">AXI_DMA_IN_ERR_EOF_DES_ADDR_CHO_REG</a> | Receive descriptor address when errors occur on RX channel 0  | 0x0030  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_CHO_REG</a>             | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 0 | 0x0034  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_BFO_CHO_REG</a>         | Address of the current pre-read receive descriptor on RX channel 0  | 0x0038  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_BF1_CHO_REG</a>         | Address of the previous pre-read receive descriptor on RX channel 0                                       | 0x003C  | RO     |
| <a href="#">AXI_DMA_INFIFO_STATUS_CH1_REG</a>       | RX channel 1 FIFO status register   | 0x0080  | RO     |
| <a href="#">AXI_DMA_IN_STATE_CH1_REG</a>            | RX channel 1 status register  | 0x0090  | RO     |
| <a href="#">AXI_DMA_IN_SUC_EOF_DES_ADDR_CH1_REG</a> | Receive descriptor address when EOF occurs on RX channel 1  | 0x0094  | RO     |
| <a href="#">AXI_DMA_IN_ERR_EOF_DES_ADDR_CH1_REG</a> | Receive descriptor address when errors occur on RX channel 1  | 0x0098  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_CH1_REG</a>             | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 1 | 0x009C  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_BFO_CH1_REG</a>         | Address of the current pre-read receive descriptor on RX channel 1  | 0x00A0  | RO     |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AXI_DMA_IN_DSCR_BF1_CH1_REG</a>          | Address of the previous pre-read receive descriptor on RX channel 1   | 0x00A4  | RO     |
| <a href="#">AXI_DMA_INFIFO_STATUS_CH2_REG</a>        | RX channel 2 FIFO status register   | 0x00E8  | RO     |
| <a href="#">AXI_DMA_IN_STATE_CH2_REG</a>             | RX channel 2 status register  | 0x00F8  | RO     |
| <a href="#">AXI_DMA_IN_SUC_EOF_DES_ADDR_CH2_REG</a>  | Receive descriptor address when EOF occurs on RX channel 2  | 0x00FC  | RO     |
| <a href="#">AXI_DMA_IN_ERR_EOF_DES_ADDR_CH2_REG</a>  | Receive descriptor address when errors occur on RX channel 2  | 0x0100  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_CH2_REG</a>              | Address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 2   | 0x0104  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_BFO_CH2_REG</a>          | Address of the current pre-read receive descriptor on RX channel 2  | 0x0108  | RO     |
| <a href="#">AXI_DMA_IN_DSCR_BF1_CH2_REG</a>          | Address of the previous pre-read receive descriptor on RX channel 2   | 0x010C  | RO     |
| <a href="#">AXI_DMA_OUTFIFO_STATUS_CHO_REG</a>       | TX channel 0 FIFO status  | 0x0150  | RO     |
| <a href="#">AXI_DMA_OUT_STATE_CHO_REG</a>            | TX channel 0 status   | 0x0160  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_DES_ADDR_CHO_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 0   | 0x0164  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_BFR_DES_ADDR_CHO_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 0  | 0x0168  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_CHO_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 0 | 0x016C  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BFO_CHO_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 0   | 0x0170  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BF1_CHO_REG</a>         | Address of the previous pre-read transmit descriptor on TX channel 0  | 0x0174  | RO     |
| <a href="#">AXI_DMA_OUTFIFO_STATUS_CH1_REG</a>       | TX channel 0 FIFO status  | 0x01B8  | RO     |
| <a href="#">AXI_DMA_OUT_STATE_CH1_REG</a>            | TX channel 1 status   | 0x01C8  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_DES_ADDR_CH1_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 1   | 0x01CC  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_BFR_DES_ADDR_CH1_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 1  | 0x01D0  | RO     |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">AXI_DMA_OUT_DSCR_CH1_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 1 | 0x01D4  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BFO_CH1_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 1   | 0x01D8  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BF1_CH1_REG</a>         | Address of the previous pre-read transmit descriptor on TX channel 1  | 0x01DC  | RO     |
| <a href="#">AXI_DMA_OUTFIFO_STATUS_CH2_REG</a>       | TX channel 2 FIFO status  | 0x0220  | RO     |
| <a href="#">AXI_DMA_OUT_STATE_CH2_REG</a>            | TX channel 2 status   | 0x0230  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_DES_ADDR_CH2_REG</a>     | Transmit descriptor address when EOF occurs on TX channel 2   | 0x0234  | RO     |
| <a href="#">AXI_DMA_OUT_EOF_BFR_DES_ADDR_CH2_REG</a> | The last transmit descriptor address when EOF occurs on TX channel 2  | 0x0238  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_CH2_REG</a>             | Address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 2 | 0x023C  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BFO_CH2_REG</a>         | Address of the current pre-read transmit descriptor on TX channel 2   | 0x0240  | RO     |
| <a href="#">AXI_DMA_OUT_DSCR_BF1_CH2_REG</a>         | Address of the previous pre-read transmit descriptor on TX channel 2  | 0x0244  | RO     |
| <b>Priority Registers</b>                            |   |         |        |
| <a href="#">AXI_DMA_IN_PRI_CHO_REG</a>               | Priority register of RX channel 0   | 0x0040  | R/W    |
| <a href="#">AXI_DMA_IN_PRI_CH1_REG</a>               | Priority register of RX channel 1   | 0x00A8  | R/W    |
| <a href="#">AXI_DMA_IN_PRI_CH2_REG</a>               | Priority register of RX channel 2   | 0x0110  | R/W    |
| <a href="#">AXI_DMA_OUT_PRI_CHO_REG</a>              | Priority register of TX channel 0   | 0x0178  | R/W    |
| <a href="#">AXI_DMA_OUT_PRI_CH1_REG</a>              | Priority register of TX channel 1   | 0x01E0  | R/W    |
| <a href="#">AXI_DMA_OUT_PRI_CH2_REG</a>              | Priority register of TX channel 2   | 0x0248  | R/W    |
| <b>Peripheral Select Registers</b>                   |   |         |        |
| <a href="#">AXI_DMA_IN_PERI_SEL_CHO_REG</a>          | Peripheral selection register of RX channel 0   | 0x0044  | R/W    |
| <a href="#">AXI_DMA_IN_PERI_SEL_CH1_REG</a>          | Peripheral selection register of RX channel 1   | 0x00AC  | R/W    |
| <a href="#">AXI_DMA_IN_PERI_SEL_CH2_REG</a>          | Peripheral selection register of RX channel 2   | 0x0114  | R/W    |
| <a href="#">AXI_DMA_OUT_PERI_SEL_CHO_REG</a>         | Peripheral selection register of TX channel 0   | 0x017C  | R/W    |



| Name   | Description                                   | Address | Access |
|--|---|---------|--------|
| <a href="#">AXI_DMA_OUT_PERI_SEL_CH1_REG</a> | Peripheral selection register of TX channel 1 | 0x01E4  | R/W    |
| <a href="#">AXI_DMA_OUT_PERI_SEL_CH2_REG</a> | Peripheral selection register of TX channel 2 | 0x024C  | R/W    |
| <b>Version Register</b>                      |   |         |        |
| <a href="#">AXI_DMA_DATE_REG</a>             | Version control register                      | 0x02D8  | R/W    |



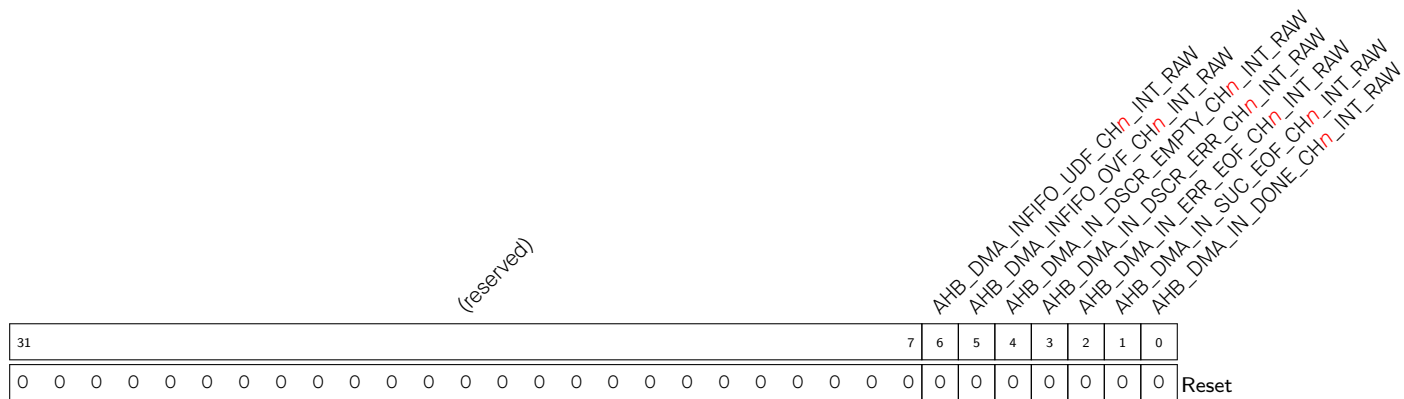
## 3.9 Registers

### 3.9.1 GDMA-AHB Registers

The addresses in this section are relative to GDMA-AHB base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 3.1. AHB\_DMA\_IN\_INT\_RAW\_CH $n$ \_REG ( $n$ : 0-2) (0x0000+0x10\* $n$ )



**AHB\_DMA\_IN\_DONE\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_IN\_DONE\_CH $n$ \_INT. (R/WTC/SS)

**AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT. For UHCI, this bit turns to 1 when the last data byte pointed by one receive descriptor has been received and no data error is detected for RX channel  $n$ . (R/WTC/SS)

**AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. Valid only for UHCI. (R/WTC/SS)

**AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT. (R/WTC/SS)

**AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (R/WTC/SS)

**AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT. (R/WTC/SS)

Register 3.2. AHB\_DMA\_IN\_INT\_ST\_CH $n$ \_REG ( $n$ : 0-2) (0x0004+0x10\* $n$ )

**AHB\_DMA\_IN\_DONE\_CH $n$ \_INT\_ST** The masked interrupt status of AHB\_DMA\_IN\_DONE\_CH $n$ \_INT.  
(RO)

**AHB\_DMA\_IN\_SUC\_EOF\_CH<sub>n</sub>INT\_ST** The masked interrupt status of AHB DMA IN SUC EOF CH<sub>n</sub> INT. (RO)

**AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. (RO)

**AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_ST** The masked interrupt status of AHB DMA IN DSCR ERR CH $n$  INT. (RO)

**AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_ST** The masked interrupt status of AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (RO)

**AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT. (RO)

**AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT. (RO)

Register 3.3. AHB\_DMA\_IN\_INT\_ENA\_CH $n$ \_REG ( $n$ : 0-2) (0x0008+0x10\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_INFIFO_UDF_CH <sub>n</sub> _INT_ENA<br>AHB_DMA_INFIFO_OVF_CH <sub>n</sub> _INT_ENA<br>AHB_DMA_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_ENA<br>AHB_DMA_IN_DSCR_ERR_CH <sub>n</sub> _INT_ENA<br>AHB_DMA_IN_SUC_EOF_CH <sub>n</sub> _INT_ENA<br>AHB_DMA_IN_DONE_CH <sub>n</sub> _INT_ENA |   |   |   |   |       |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 7 | 6 | 5 | 4   | 3 | 2 | 1 | 0 | Reset |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |       |  |  |

**AHB\_DMA\_IN\_DONE\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_IN\_DONE\_CH $n$ \_INT. (R/W)

**AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT.  
(R/W)

**AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT.  
(R/W)

**AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT.  
(R/W)

**AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT.  
(R/W)

**AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT. (R/W)

**AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT. (R/W)

Register 3.4. AHB\_DMA\_IN\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-2) (0x000C+0x10\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AHB_DMA_IN_FIFO_UDF_CHn_INT_CLR<br>AHB_DMA_IN_FIFO_OVF_CHn_INT_CLR<br>AHB_DMA_IN_DSCR_EMPTY_CHn_INT_CLR<br>AHB_DMA_IN_DSCR_ERR_CHn_INT_CLR<br>AHB_DMA_IN_EOF_CHn_INT_CLR<br>AHB_DMA_IN_SUC_EOF_CHn_INT_CLR<br>AHB_DMA_IN_DONE_CHn_INT_CLR |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |

**AHB\_DMA\_IN\_DONE\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_IN\_DONE\_CH $n$ \_INT. (WT)

**AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT. (WT)

**AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. (WT)

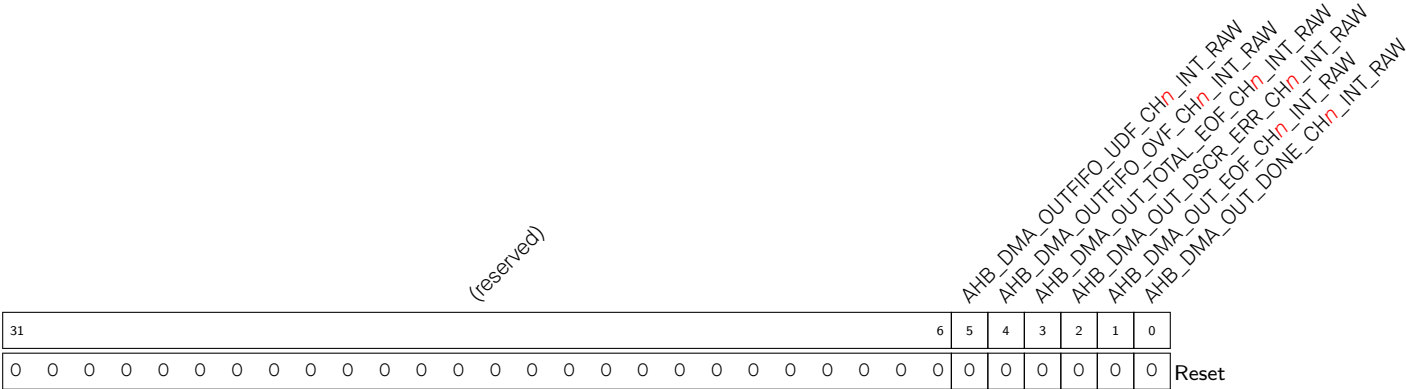
**AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT.  
(WT)

**AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT.  
(WT)

**AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_INFIFO\_OVF\_CH $n$ \_INT. (WT)

**AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_INFIFO\_UDF\_CH $n$ \_INT. (WT)

Register 3.5. AHB\_DMA\_OUT\_INT\_RAW\_CHn\_REG (n: 0-2) (0x0030+0x10\*n)



- AHB\_DMA\_OUT\_DONE\_CHn\_INT\_RAW

The raw interrupt status of AHB\_DMA\_OUT\_DONE\_CHn\_INT. (R/WTC/SS)
- AHB\_DMA\_OUT\_EOF\_CHn\_INT\_RAW

The raw interrupt status of AHB\_DMA\_OUT\_EOF\_CHn\_INT. (R/WTC/SS)
- AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT\_RAW

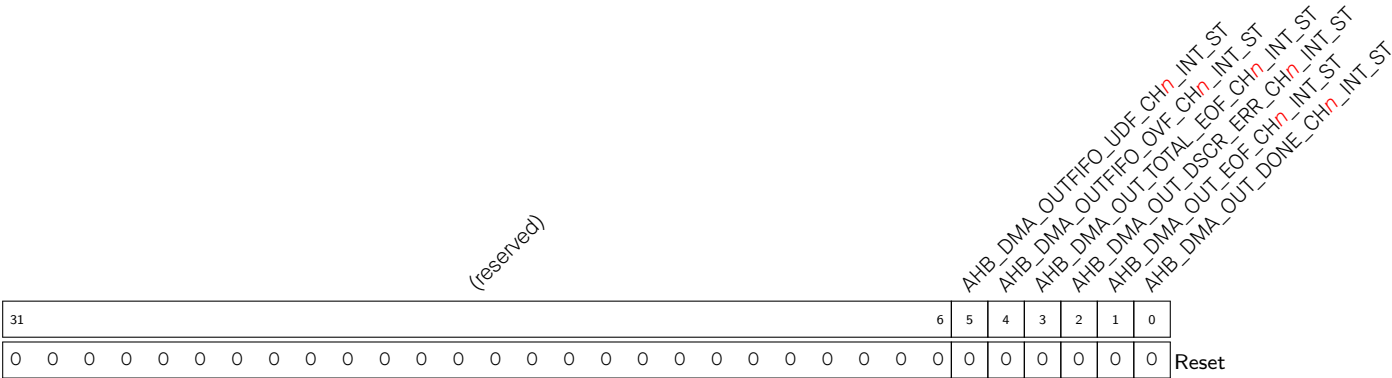
The raw interrupt status of AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT. (R/WTC/SS)
- AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT\_RAW

The raw interrupt status of AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT. (R/WTC/SS)
- AHB\_DMA\_OUTFIFO\_OVF\_CHn\_INT\_RAW

The raw interrupt status of AHB\_DMA\_OUTFIFO\_OVF\_CHn\_INT. (R/WTC/SS)
- AHB\_DMA\_OUTFIFO\_UDF\_CHn\_INT\_RAW

The raw interrupt status of AHB\_DMA\_OUTFIFO\_UDF\_CHn\_INT. (R/WTC/SS)

Register 3.6. AHB\_DMA\_OUT\_INT\_ST\_CHn\_REG (n: 0-2) (0x0034+0x10\*n)



**AHB\_DMA\_OUT\_DONE\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_DONE\_CHn\_INT. (RO)

**AHB\_DMA\_OUT\_EOF\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_EOF\_CHn\_INT. (RO)

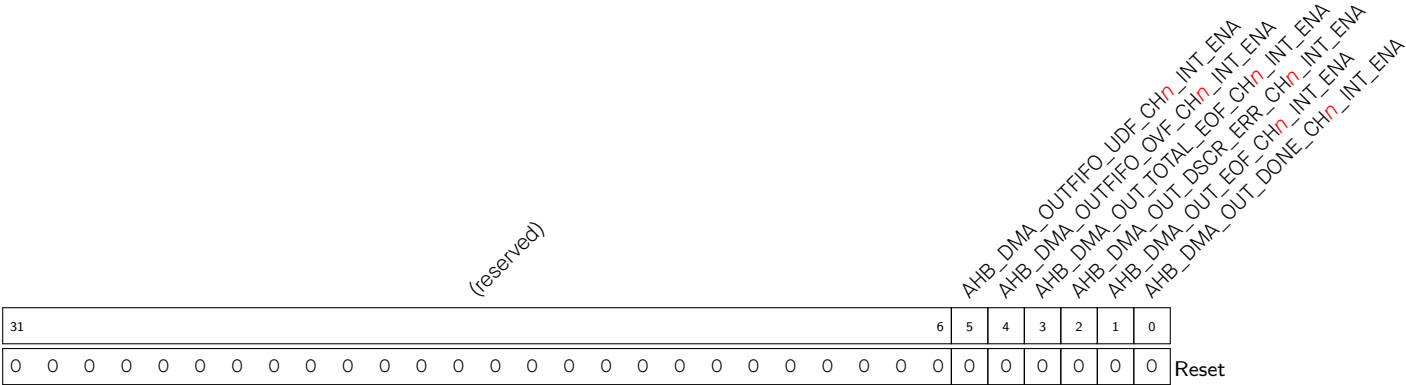
**AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT. (RO)

**AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT. (RO)

**AHB\_DMA\_OUT\_FIFO\_OVF\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_FIFO\_OVF\_CHn\_INT. (RO)

**AHB\_DMA\_OUT\_FIFO\_UDF\_CHn\_INT\_ST** The masked interrupt status of AHB\_DMA\_OUT\_FIFO\_UDF\_CHn\_INT. (RO)

Register 3.7. AHB\_DMA\_OUT\_INT\_ENA\_CHn\_REG (n: 0-2) (0x0038+0x10\*n)



**AHB\_DMA\_OUT\_DONE\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_DONE\_CHn\_INT. (R/W)

**AHB\_DMA\_OUT\_EOF\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_EOF\_CHn\_INT. (R/W)

**AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_DSCR\_ERR\_CHn\_INT.  
(R/W)

**AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_TOTAL\_EOF\_CHn\_INT.  
(R/W)

**AHB\_DMA\_OUT\_FIFO\_OVF\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_FIFO\_OVF\_CHn\_INT.  
(R/W)

**AHB\_DMA\_OUT\_FIFO\_UDF\_CHn\_INT\_ENA** Write 1 to enable AHB\_DMA\_OUT\_FIFO\_UDF\_CHn\_INT.  
(R/W)

Register 3.8. AHB\_DMA\_OUT\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-2) (0x003C+0x10\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |       |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|-------|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_FIFO_UDF_CH <sub>n</sub> _INT_CLR  |   |       |   |   |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_FIFO_OVF_CH <sub>n</sub> _INT_CLR  |   |       |   |   |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_CLR |   |       |   |   |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_DSCR_ERR_CH <sub>n</sub> _INT_CLR  |   |       |   |   |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_DONE_CH <sub>n</sub> _INT_CLR      |   |       |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5 | 4 | 3 | 2 | 1  | 0 | Reset |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 |       | 0 | 0 |  |

**AHB\_DMA\_OUT\_DONE\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_DONE\_CH $n$ \_INT. (WT)

**AHB\_DMA\_OUT\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_EOF\_CH $n$ \_INT. (WT)

**AHB\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (WT)

**AHB\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (WT)

**AHB\_DMA\_OUT\_FIFO\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_FIFO\_OVF\_CH $n$ \_INT. (WT)

**AHB\_DMA\_OUT\_FIFO\_UDF\_CH $n$ \_INT\_CLR** Write 1 to clear AHB\_DMA\_OUT\_FIFO\_UDF\_CH $n$ \_INT. (WT)

Register 3.9. AHB\_DMA\_AHB\_TEST\_REG (0x0060)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |   |   |   |            |   |                      |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|---|---|---|------------|---|----------------------|-------|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AHB_DMA_AHB_TESTADDR |   |   |   | (reserved) |   | AHB_DMA_AHB_TESTMODE |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6                    | 5 | 4 | 3 | 2          | 0 |                      | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    | 0 | 0 |   |            |   |                      |       |

**AHB\_DMA\_AHB\_TESTMODE** Reserved. (R/W)

**AHB\_DMA\_AHB\_TESTADDR** Reserved. (R/W)



### Register 3.10. AHB\_DMA\_MISC\_CONF\_REG (0x0064)

[illegible]

**AHB\_DMA\_AHBM\_RST\_INTER** Write 1 and then 0 to reset the internal AHB FSM. (R/W)

**AHB\_DMA\_ARB\_PRI\_DIS** Configures whether to disable the priority arbitration.

0: Enable

1: Disable

(R/W)

**AHB\_DMA\_CLK\_EN** Configures AHB DMA clock gating.

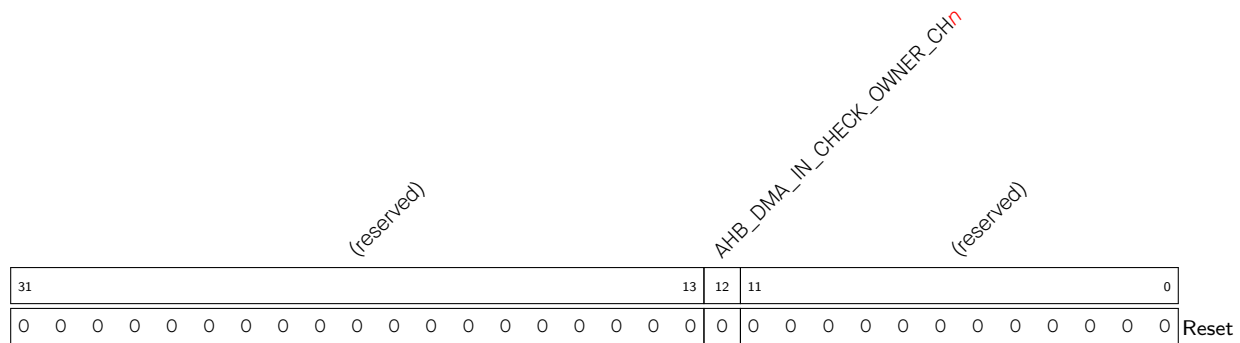
0: Support clock only when the application writes registers

1: Always force the clock on for registers

(R/W)



**Register 3.12. AHB\_DMA\_IN\_CONF1\_CH $n$ \_REG ( $n$ : 0-2) (0x0074+0xC0\* $n$ )**



**AHB\_DMA\_IN\_CHECK\_OWNER\_CH**n Configures whether to enable owner bit check for RX channel

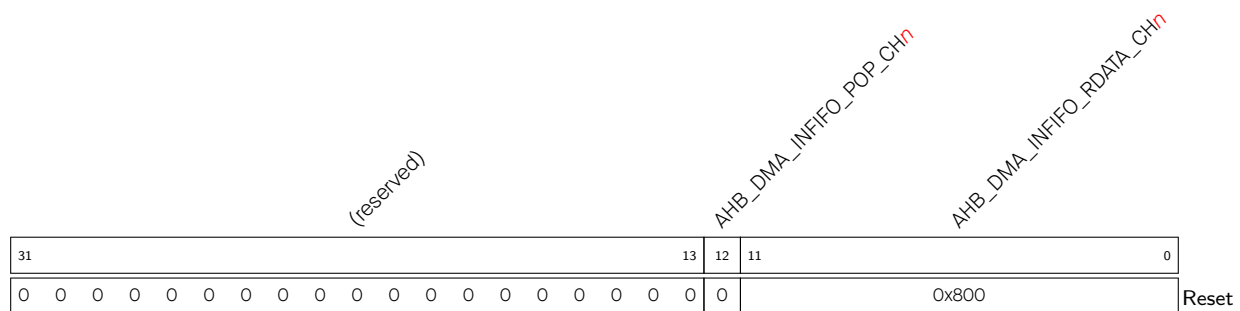
 $n.$ 

0: Disable

1: Enable

(R/W)

**Register 3.13. AHB\_DMA\_IN\_POP\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x007C+0xC0\**n*)**



**AHB\_DMA\_INFIFO\_RDATA\_CH<sub>n</sub>** Represents the data popped from AHB DMA RX FIFO. (RO)

**AHB\_DMA\_INFIFO\_POP\_CH $n$**  Configures whether to pop data from AHB DMA RX FIFO.

0: Invalid. No effect

1: Pop

(WT)



Register 3.15. AHB\_DMA\_OUT\_CONFO\_CH $n$ \_REG ( $n$ : 0-2) (0x00D0+0xC0\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AHB_DMA_OUT_ETM_EN_CH <sub>n</sub><br>AHB_DMA_OUT_DATA_BURST_EN_CH <sub>n</sub><br>AHB_DMA_OUTDSCR_BURST_EN_CH <sub>n</sub><br>AHB_DMA_OUT_EOF_MODE_CH <sub>n</sub><br>AHB_DMA_OUT_AUTO_WRBACK_CH <sub>n</sub><br>AHB_DMA_OUT_LOOP_TEST_CH <sub>n</sub><br>AHB_DMA_OUT_RST_CH <sub>n</sub> |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 1 | 0 | 0 | 0 |   |       |

**AHB\_DMA\_OUT\_RST\_CH $n$**  Configures the reset state of TX channel  $n$  FSM and TX FIFO pointer.

0: Release reset

1: Reset

(R/W)

**AHB\_DMA\_OUT\_LOOP\_TEST\_CH $n$**  Reserved. (R/W)

**AHB\_DMA\_OUT\_AUTO\_WRBK\_CH $n$**  Configures whether to enable automatic outlink write-back when all the data in TX FIFO has been transmitted.

0: Disable

1: Enable

(R/W)

**AHB\_DMA\_OUT\_EOF\_MODE\_CH $n$**  Configures when to generate EOF flag.

0: EOF flag for TX channel  $n$  is generated when data to be transmitted has been pushed into FIFO in AHB DMA.

1: EOF flag for TX channel  $n$  is generated when data to be transmitted has been popped from FIFO in AHB DMA.

(R/W)

**AHB\_DMA\_OUTDSCR\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for TX channel  $n$  reading descriptors.

0: Disable

1: Enable

(R/W)

**AHB\_DMA\_OUT\_DATA\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for TX channel  $n$ .

0: Disable

1: Enable

(R/W)

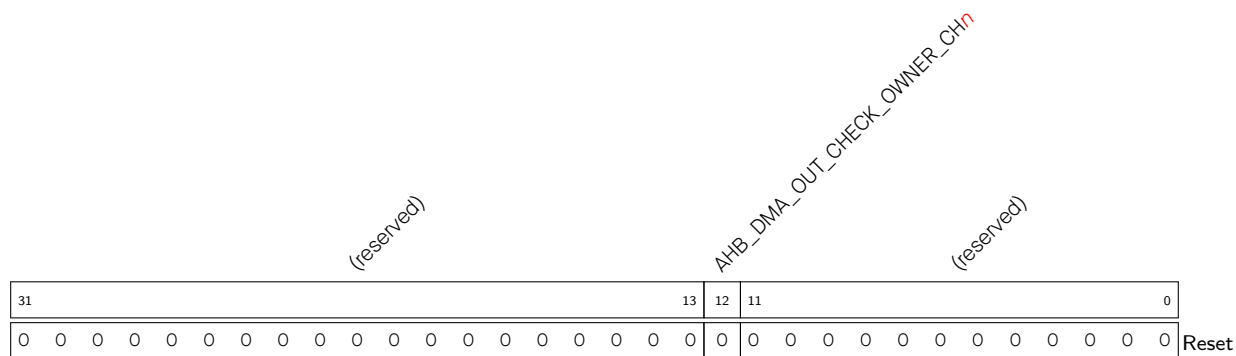
**AHB\_DMA\_OUT\_ETM\_EN\_CH $n$**  Configures whether to enable ETM control for TX channel  $n$ .

0: Disable

1: Enable

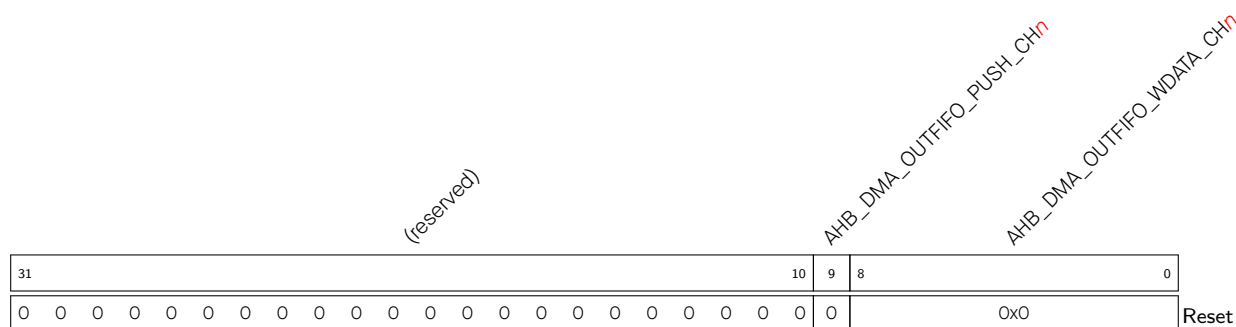
(R/W)

**Register 3.16. AHB\_DMA\_OUT\_CONF1\_CH $n$ \_REG ( $n$ : 0-2) (0x00D4+0xC0\* $n$ )**



**AHB\_DMA\_OUT\_CHECK\_OWNER\_CH***n* Configures whether to enable owner bit check for TX channel *n*.  
0: Disable  
1: Enable  
(R/W)

Register 3.17. AHB\_DMA\_OUT\_PUSH\_CH $n$ \_REG ( $n$ : 0-2) (0x00DC+0xC0\* $n$ )



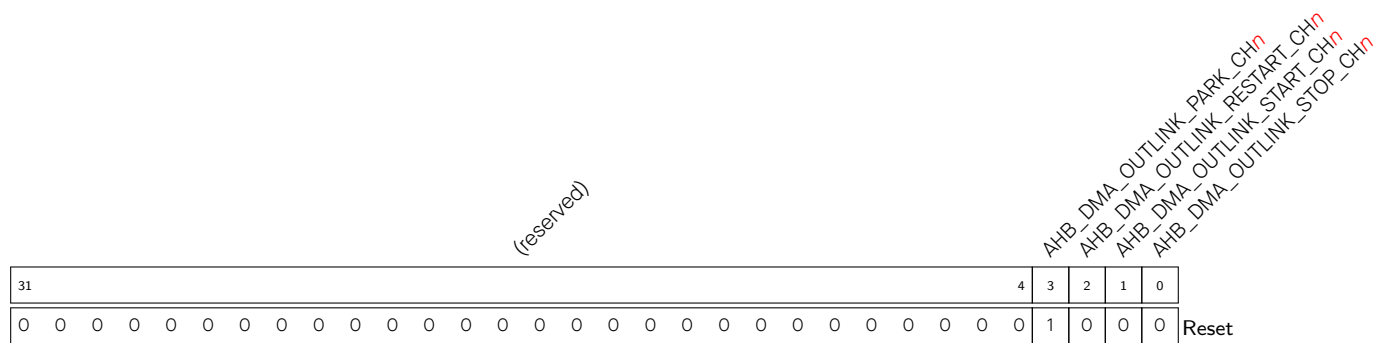
**AHB\_DMA\_OUTFIFO\_WDATA\_CH $n$**  Represents the data that need to be pushed into AHB DMA TX FIFO. (R/W)

**AHB\_DMA\_OUTFIFO\_PUSH\_CH**n Configures whether to push data into AHB DMA TX FIFO.

- 0: Invalid. No effect
- 1: Push

(WT)

**Register 3.18. AHB\_DMA\_OUT\_LINK\_CH $n$ \_REG ( $n$ : 0-2) (0x00E0+0xC0\* $n$ )**



**AHB\_DMA\_OUTLINK\_STOP\_CH***n* Configures whether to stop TX channel *n* from transmitting data.

0: Invalid. No effect

1: Stop

(WT)

**AHB\_DMA\_OUTLINK\_START\_CH***n* Configures whether to enable TX channel *n* for data transfer.

0: Disable

1: Enable

(WT)

**AHB\_DMA\_OUTLINK\_RESTART\_CH $n$**  Configures whether to restart TX channel  $n$  for AHB DMA transfer.

0: Invalid. No effect

1: Restart

(WT)

**AHB\_DMA\_OUTLINK\_PARK\_CH<sub>n</sub>** Represents the status of the transmit descriptor's FSM.

0: Running

1: Idle

(RO)

Register 3.19. AHB\_DMA\_OUT\_CRC\_INIT\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x02BC+0x28\* $n$ )



**AHB\_DMA\_OUT\_CRC\_INIT\_DATA\_CH $n$**  Configures the CRC initial value for TX channel  $n$ . (R/W)

Register 3.20. AHB\_DMA\_TX\_CRC\_WIDTH\_CH $n$ \_REG ( $n$ : 0-2) (0x02C0+0x28\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_TX_CRC_LAUTCH_FLGA_CHn |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_TX_CRC_WIDTH_CHn       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3 | 2 | 1                              | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**AHB\_DMA\_TX\_CRC\_WIDTH\_CH $n$**  Configures the CRC result width for TX channel  $n$ . 0:  $\leq 8$  bits

1:  $\leq 16$  bits

2:  $\leq 24$  bits

3:  $\leq 32$  bits

(R/W)

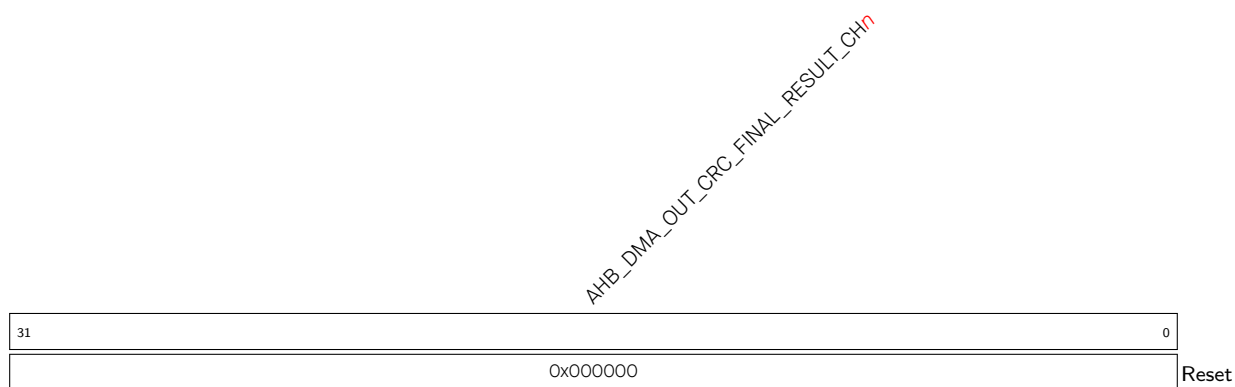
**AHB\_DMA\_TX\_CRC\_LAUTCH\_FLGA\_CH $n$**  Write 1 and then 0 to latch the values of AHB\_DMA\_TX\_CRC\_EN\_ADDR\_CH $n$ , AHB\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH $n$ , AHB\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$ , and AHB\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ . (R/W)

Register 3.21. AHB\_DMA\_OUT\_CRC\_CLEAR\_CH $n$ \_REG ( $n$ : 0-2) (0x02C4+0x28\* $n$ )

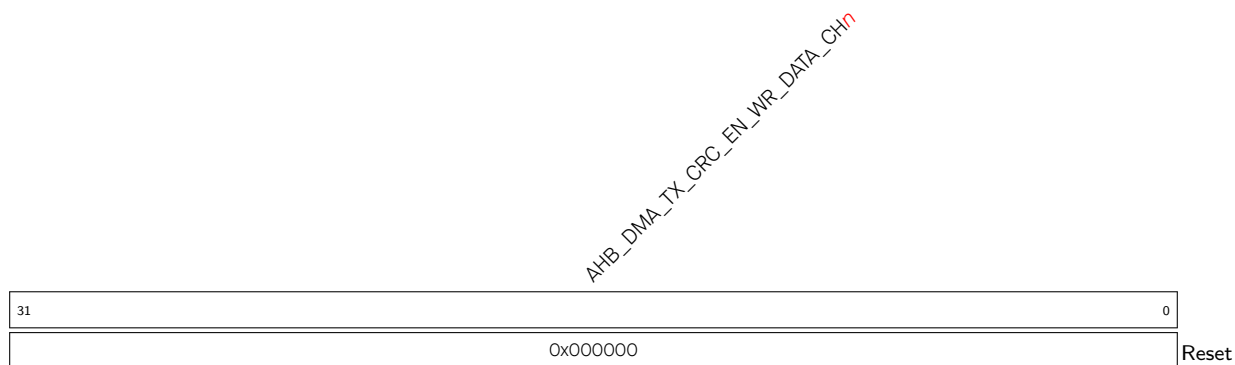
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_OUT_CRC_CLEAR_CH <sub>n</sub> _REG |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0  | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  |       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**AHB\_DMA\_OUT\_CRC\_CLEAR\_CH $n$ \_REG** Reserved. (R/W)



**Register 3.22. AHB\_DMA\_OUT\_CRC\_FINAL\_RESULT\_CH $n$ \_REG ( $n$ : 0-2) (0x02C8+0x28\* $n$ )**

**AHB\_DMA\_OUT\_CRC\_FINAL\_RESULT\_CH $n$**  Represents the CRC result for TX channel  $n$ . (RO)

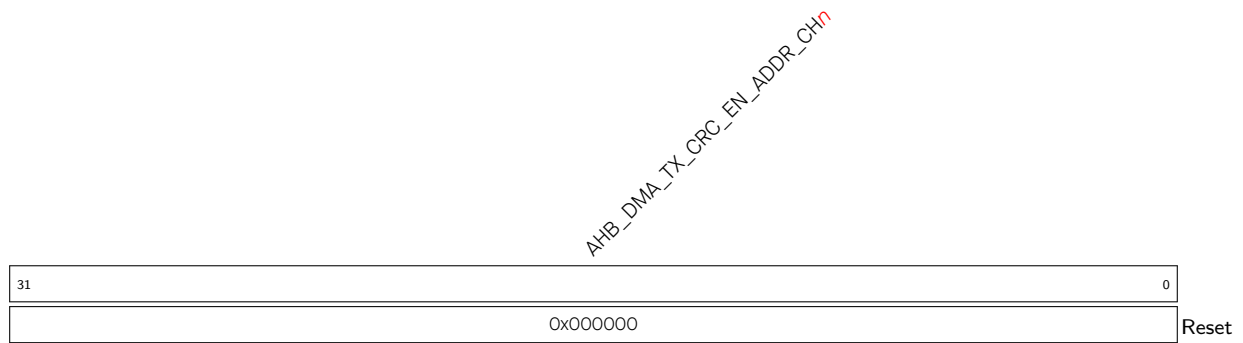
**Register 3.23. AHB\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x02CC+0x28\* $n$ )**

**AHB\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$**  Configures whether to include each bit of the intermediate result in the CRC calculation matrix for TX channel  $n$ .

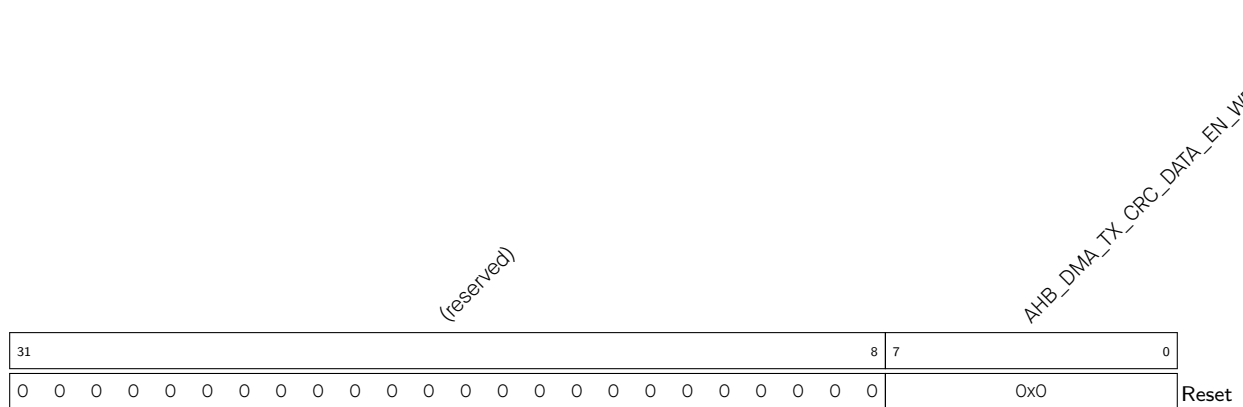
0: Not include

1: Include

(R/W)

**Register 3.24. AHB\_DMA\_TX\_CRC\_EN\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x02D0+0x28\* $n$ )**

**AHB\_DMA\_TX\_CRC\_EN\_ADDR\_CH $n$**  Configures at which bit of the CRC result the AHB\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH $n$ \_REG register targets for TX channel  $n$ . (R/W)

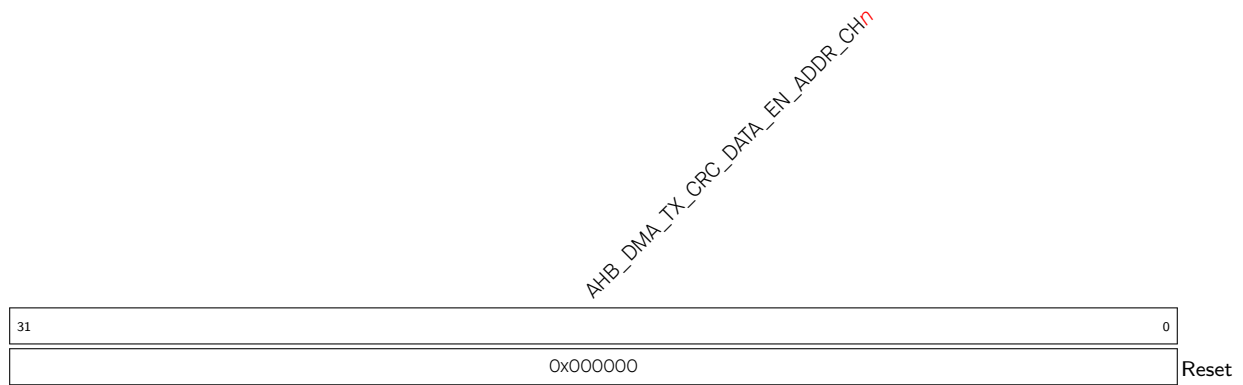
**Register 3.25. AHB\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x02D4+0x28\* $n$ )**

**AHB\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$**  Configures whether to include each bit of the data in the CRC calculation matrix for TX channel  $n$ .

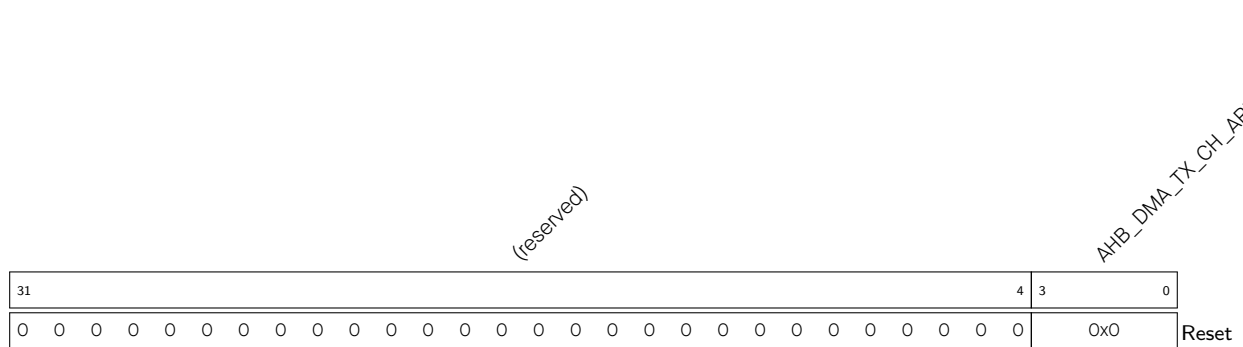
0: Not include

1: Include

(R/W)

**Register 3.26. AHB\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x02D8+0x28\* $n$ )**

**AHB\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH $n$**  Configures at which bit of the CRC result the AHB\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ \_REG register targets for TX channel  $n$ . (R/W)

**Register 3.27. AHB\_DMA\_TX\_CH\_ARB\_WEIGHT\_CH $n$ \_REG ( $n$ : 0-2) (0x02DC+0x28\* $n$ )**

**AHB\_DMA\_TX\_CH\_ARB\_WEIGHT\_CH $n$**  Configures the weight (i.e the number of tokens) of TX channel  $n$ .

Value range: 0 ~ 15. (R/W)

Register 3.28. AHB\_DMA\_TX\_ARB\_WEIGH\_OPT\_DIR\_CH $n$ \_REG ( $n$ : 0-2) (0x02E0+0x28\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_TX_ARB_WEIGHT_OPT_DIR_0 |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                               | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               |       |

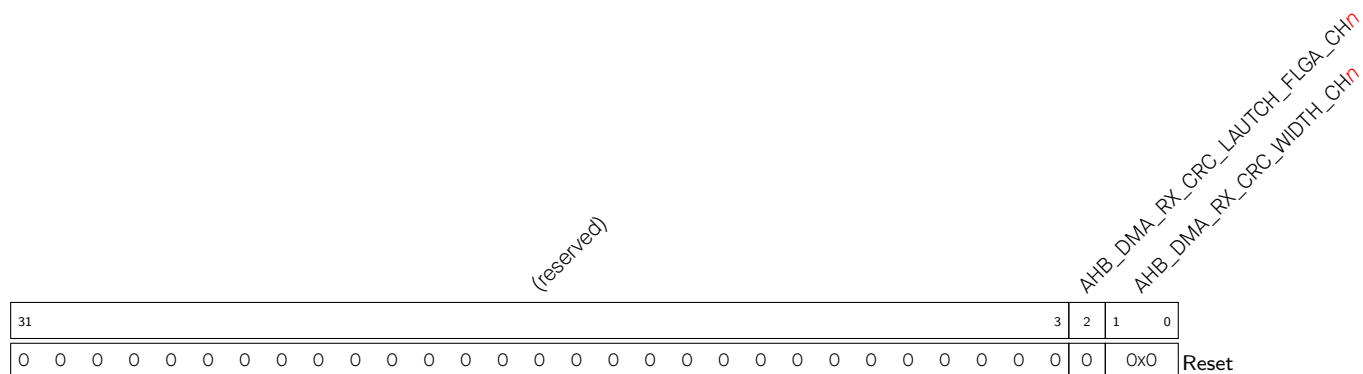
**AHB\_DMA\_TX\_ARB\_WEIGH\_OPT\_DIR\_CH $n$**  Configures whether to enable weight optimization for TX channel  $n$ .  
0: Enable  
1: Disable (R/W)

Register 3.29. AHB\_DMA\_IN\_CRC\_INIT\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x0334+0x28\* $n$ )

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| AHB_DMA_IN_CRC_INIT_DATA_CH <sup>n</sup> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0xffffffff                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**AHB\_DMA\_IN\_CRC\_INIT\_DATA\_CH $n$**  Configures the CRC initial value for RX channel  $n$ . (R/W)

Register 3.30. AHB\_DMA\_RX\_CRC\_WIDTH\_CH $n$ \_REG ( $n$ : 0-2) (0x0338+0x28\* $n$ )



**AHB\_DMA\_RX\_CRC\_WIDTH\_CH $n$**  Configures the CRC result width for RX channel  $n$ .

0: < 8 bits

1:  $< 16$  bits

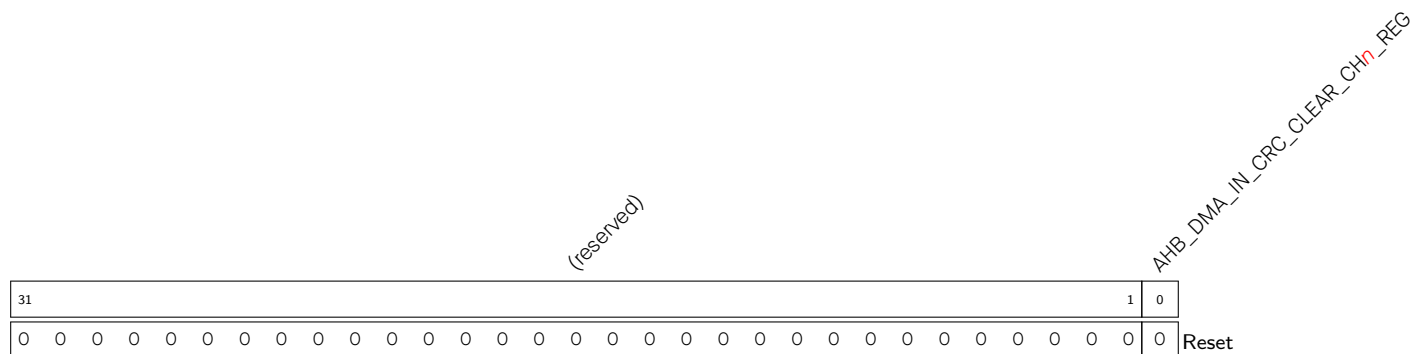
2:  $\leq 24$  bits

3:  $\leq 32$  bits

(R/W)

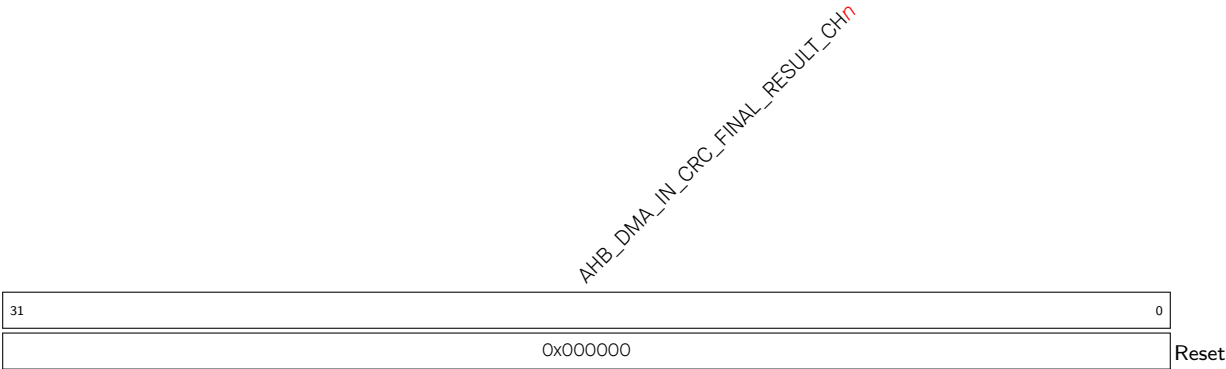
**AHB\_DMA\_RX\_CRC\_LAUTCH\_FLGA\_CH***n* Write 1 and then 0 to latch the values of  
**AHB\_DMA\_RX\_CRC\_EN\_ADDR\_CH***n*, **AHB\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH***n*,  
**AHB\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH***n*, and **AHB\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH***n*.  
 (R/W)

**Register 3.31. AHB\_DMA\_IN\_CRC\_CLEAR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x033C+0x28\**n*)**



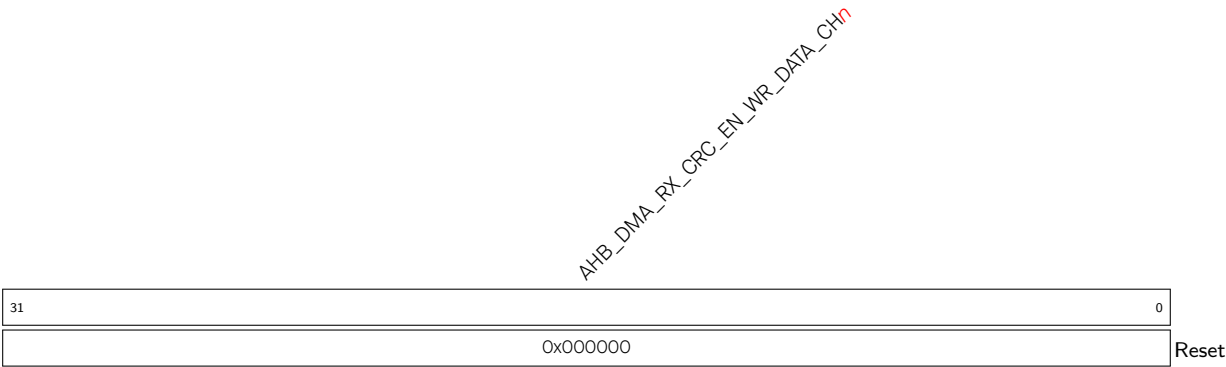
AHB\_DMA\_IN\_CRC\_CLEAR\_CH<sub>n</sub> REG Reserved. (R/W)

Register 3.32. AHB\_DMA\_IN\_CRC\_FINAL\_RESULT\_CH $n$ \_REG ( $n$ : 0-2) (0x0340+0x28\* $n$ )



AHB\_DMA\_IN\_CRC\_FINAL\_RESULT\_CH $n$  Represents the CRC result for RX channel  $n$ . (RO)

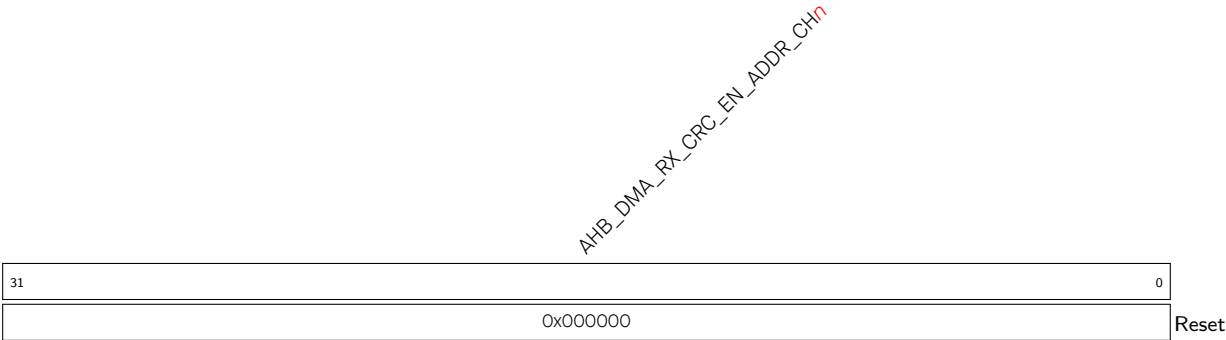
Register 3.33. AHB\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x0344+0x28\* $n$ )



AHB\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$  Configures whether to include each bit of the intermediate result in the CRC calculation matrix for RX channel  $n$ .

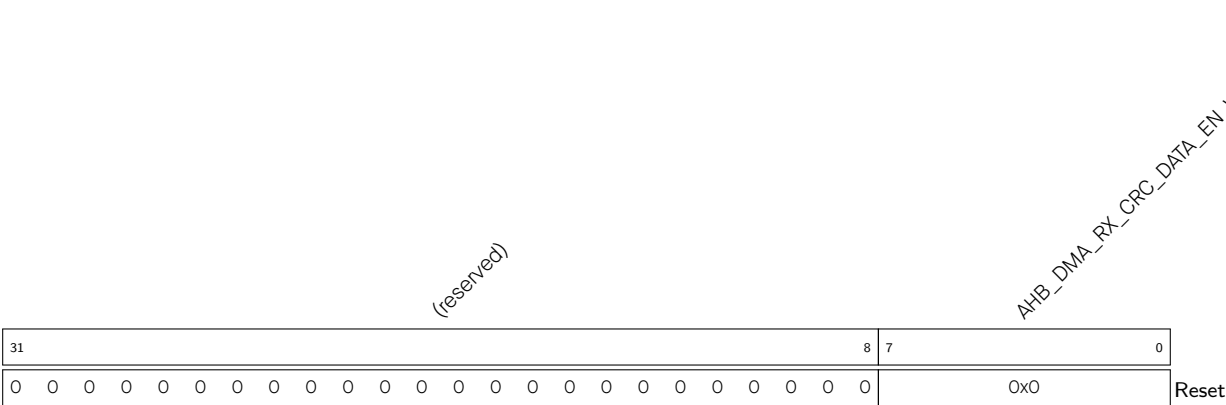
- 0: Not include
  - 1: Include
- (R/W)

Register 3.34. AHB\_DMA\_RX\_CRC\_EN\_ADDR\_CHn\_REG (n: 0-2) (0x0348+0x28\*n)



AHB\_DMA\_RX\_CRC\_EN\_ADDR\_CHn Configures at which bit of the CRC result the AHB\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CHn\_REG register targets for RX channel n. (R/W)

Register 3.35. AHB\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CHn\_REG (n: 0-2) (0x034C+0x28\*n)

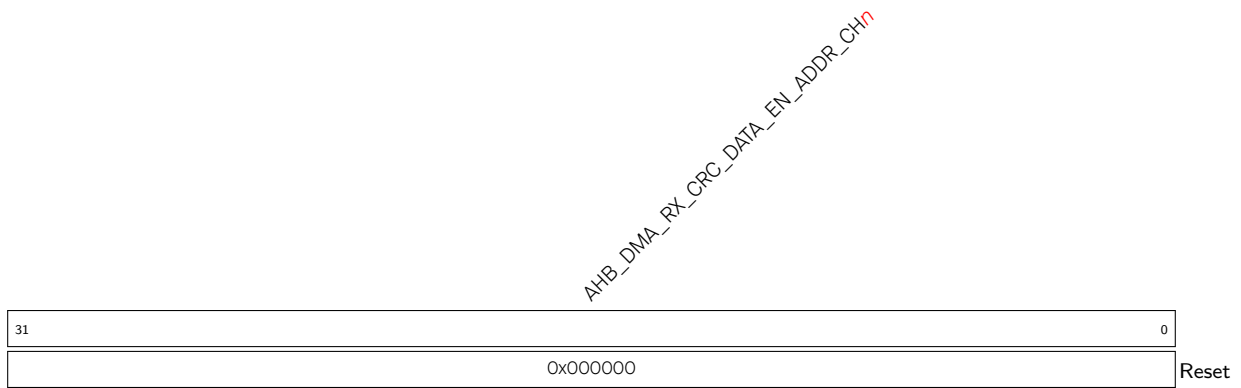


AHB\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CHn Configures whether to include each bit of the data in the CRC calculation matrix for RX channel n.

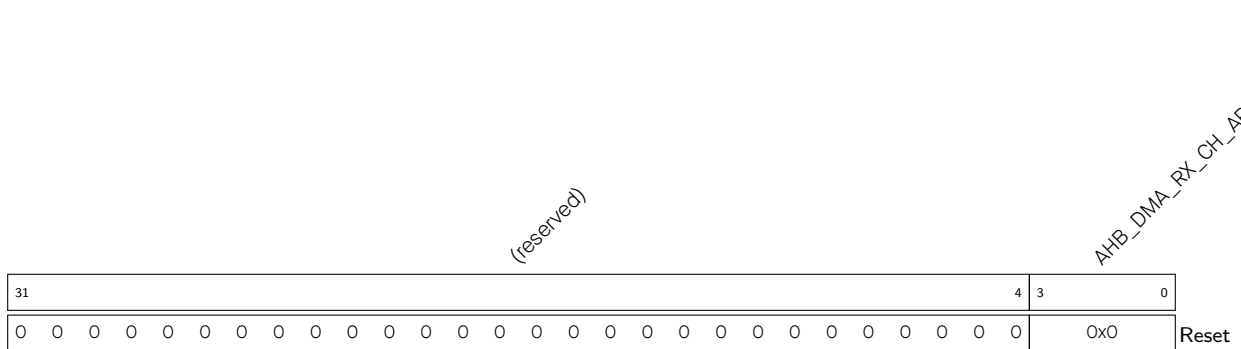
0: Not include

1: Include

(R/W)

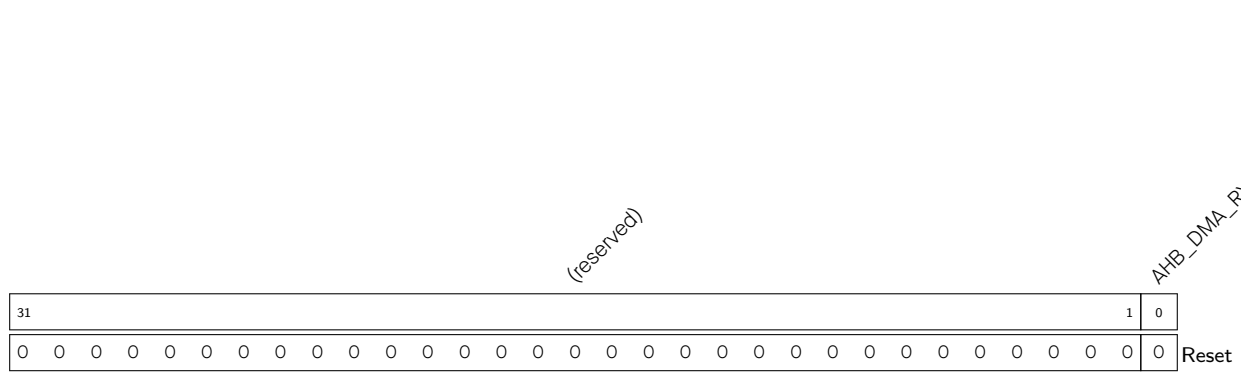
**Register 3.36. AHB\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0350+0x28\* $n$ )**

**AHB\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH $n$**  Configures at which bit of the CRC result the AHB\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ \_REG register targets for RX channel  $n$ . (R/W)

**Register 3.37. AHB\_DMA\_RX\_CH\_ARB\_WEIGHT\_CH $n$ \_REG ( $n$ : 0-2) (0x0354+0x28\* $n$ )**

**AHB\_DMA\_RX\_CH\_ARB\_WEIGHT\_CH $n$**  Configures the weight (i.e the number of tokens) of RX channel  $n$ .  
Value range: 0 ~ 15. (R/W)

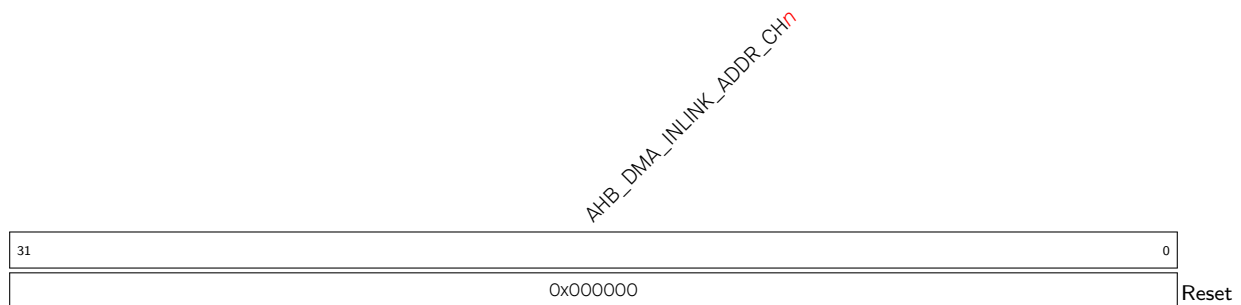


**Register 3.38. AHB\_DMA\_RX\_ARB\_WEIGH\_OPT\_DIR\_CH $n$ \_REG ( $n$ : 0-2) (0x0358+0x28\* $n$ )**

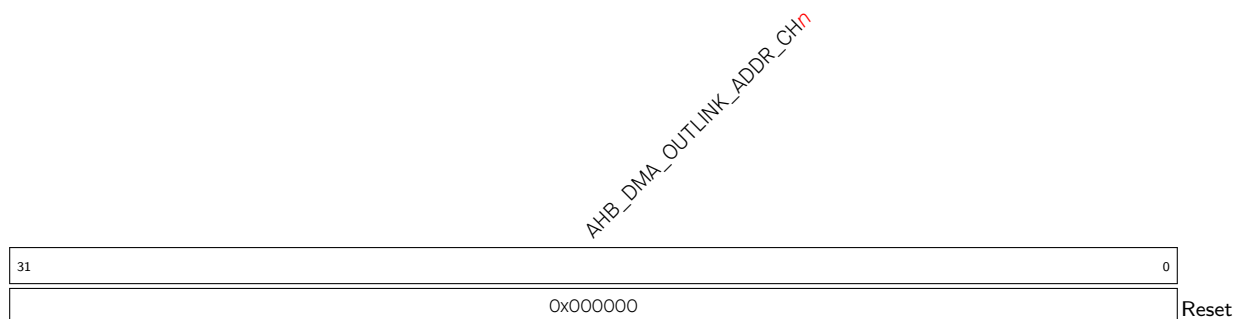
**AHB\_DMA\_RX\_ARB\_WEIGH\_OPT\_DIR\_CH $n$**  Configures whether to enable weight optimization for RX channel  $n$ .

0: Enable

1: Disable (R/W)

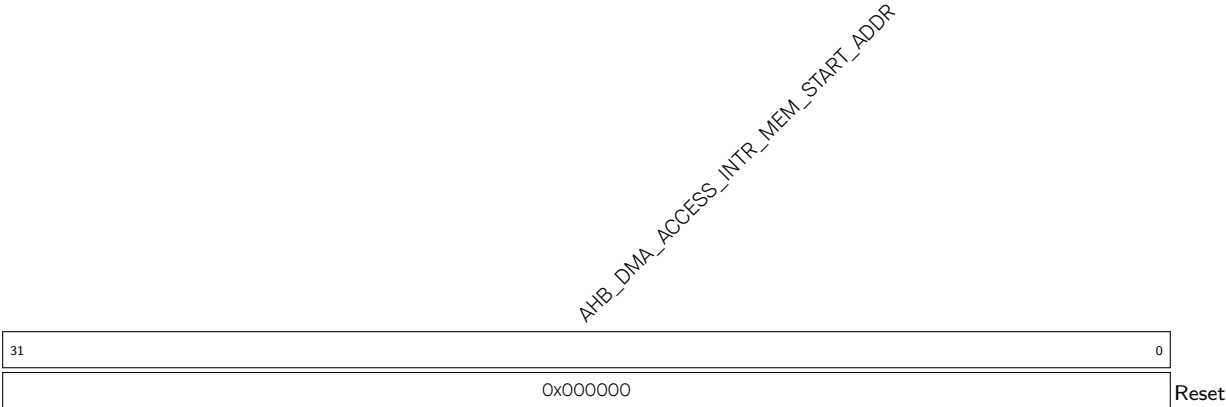
**Register 3.39. AHB\_DMA\_IN\_LINK\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x03AC+0x4\* $n$ )**

**AHB\_DMA\_INLINK\_ADDR\_CH $n$**  Represents the first receive descriptor's address. (R/W)

**Register 3.40. AHB\_DMA\_OUT\_LINK\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x03B8+0x4\* $n$ )**

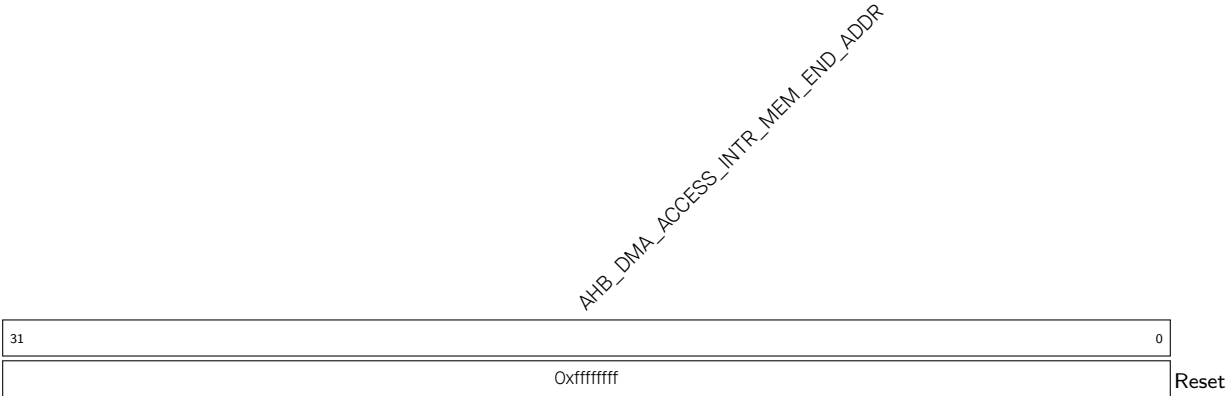
**AHB\_DMA\_OUTLINK\_ADDR\_CH $n$**  Represents the first transmit descriptor's address. (R/W)

Register 3.41. AHB\_DMA\_INTR\_MEM\_START\_ADDR\_REG (0x03C4)



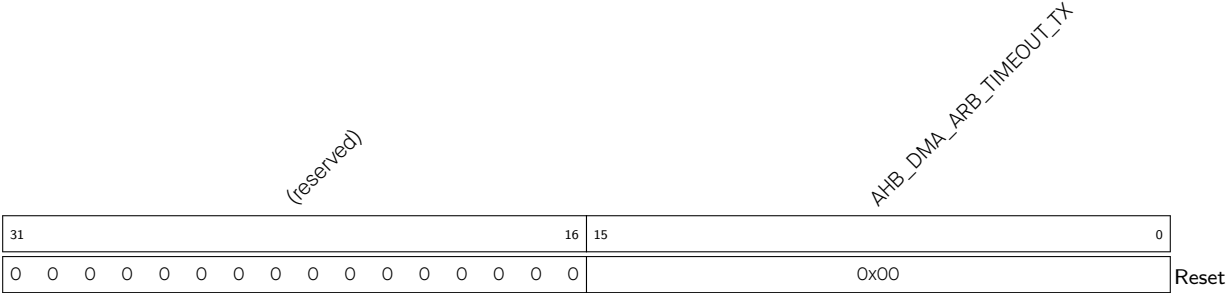
**AHB\_DMA\_ACCESS\_INTR\_MEM\_START\_ADDR** Configures the start address of accessible address space. (R/W)

Register 3.42. AHB\_DMA\_INTR\_MEM\_END\_ADDR\_REG (0x03C8)



**AHB\_DMA\_ACCESS\_INTR\_MEM\_END\_ADDR** Configures the end address of accessible address space. (R/W)

Register 3.43. AHB\_DMA\_ARB\_TIMEOUT\_TX\_REG (0x03CC)



**AHB\_DMA\_ARB\_TIMEOUT\_TX** Configures the time slot for TX. Measurement unit: AHB bus clock cycle. (R/W)

**Register 3.44. AHB\_DMA\_ARB\_TIMEOUT\_RX\_REG (0x03D0)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AHB_DMA_ARB_TIMEOUT_RX |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**AHB\_DMA\_ARB\_TIMEOUT\_RX** Configures the time slot for RX. Measurement unit: AHB bus clock cycle. (R/W)

**Register 3.45. AHB\_DMA\_WEIGHT\_EN\_TX\_REG (0x03D4)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_WEIGHT_EN_TX |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                    | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | Reset |

**AHB\_DMA\_WEIGHT\_EN\_TX** Configures whether to enable weight arbitration for TX.  
 0: Disable  
 1: Enable  
 (R/W)

**Register 3.46. AHB\_DMA\_WEIGHT\_EN\_RX\_REG (0x03D8)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_DMA_WEIGHT_EN_RX |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                    | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | Reset |

**AHB\_DMA\_WEIGHT\_EN\_RX** Configures whether to enable weight arbitration for RX.  
 0: Disable  
 1: Enable  
 (R/W)

### Register 3.47. AHB\_DMA\_DATE\_REG (0x0068)

Diagram of the AHB-DMA\_DATE register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value 0x2303140 is shown in the center, and the word "Reset" is at the bottom right.

**AHB\_DMA\_DATE** Version control register. (R/W)

**Register 3.48. AHB\_DMA\_INFIFO\_STATUS\_CH $n$ \_REG ( $n$ : 0-2) (0x0078+0xC0\* $n$ )**

Diagram illustrating the structure of the AHB\_DMA\_INFIFO\_CNT register (32 bits wide). The register is divided into three main sections:

- Top Section (Bits 31-22):** Contains fields for DMA channel status and counts:
  - (reserved) [31:28]
  - AHB\_DMA\_IN\_BUF\_HUNGRY\_CHn [27]
  - AHB\_DMA\_IN\_REMAIN\_UNDER\_4B\_CHn [26]
  - AHB\_DMA\_IN\_REMAIN\_UNDER\_3B\_CHn [25]
  - AHB\_DMA\_IN\_REMAIN\_UNDER\_2B\_CHn [24]
  - AHB\_DMA\_IN\_REMAIN\_UNDER\_1B\_CHn [23]
- Middle Section (Bits 7-0):** (reserved)
- Bottom Section (Bits 1-0):** Contains the AHB\_DMA\_INFIFO\_CNT\_CHn field, split into two bits:
  - 1 [1]
  - 0 [0]

Reset values are indicated for the bottom section: 1 for bit 1 and 1 for bit 0.

**AHB\_DMA\_INFIFO\_FULL\_CH<sub>n</sub>** Represents whether L1 RX FIFO is full.

0: Not Full

1: Full

(RO)

**AHB\_DMA\_INFIFO\_EMPTY\_CH<sub>n</sub>** Represents whether L1 RX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AHB\_DMA\_INFIFO\_CNT\_CH $n$**  Represents the number of data bytes in L1 RX FIFO for RX channel  $n$ .

(RO)

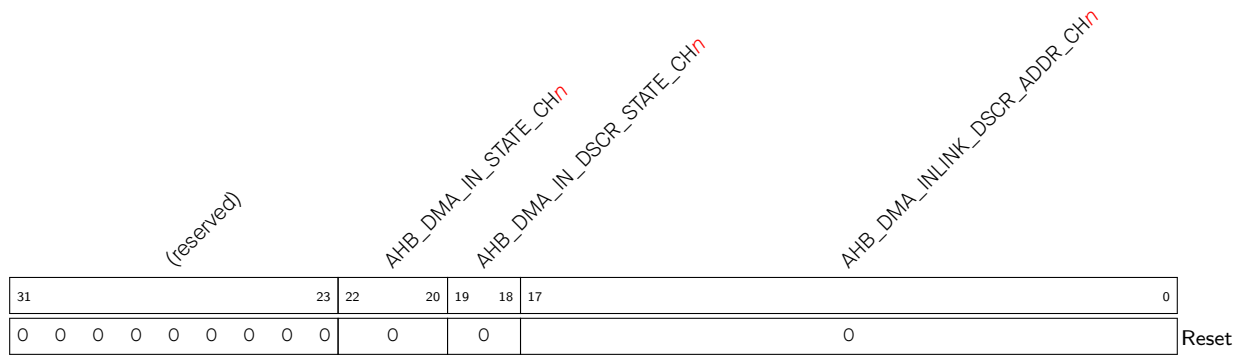
AHB\_DMA\_IN\_REMAIN\_UNDER\_1B\_CHn Reserved. (RO)

AHB\_DMA\_IN\_REMAIN\_UNDER\_2B\_CH<sub>n</sub> Reserved. (RO)

AHB DMA IN REMAIN UNDER 3B CH Reserved. (RO)

AHB\_DMA\_IN\_REMAIN\_UNDER\_4B\_CH<sub>n</sub> Reserved. (RO)

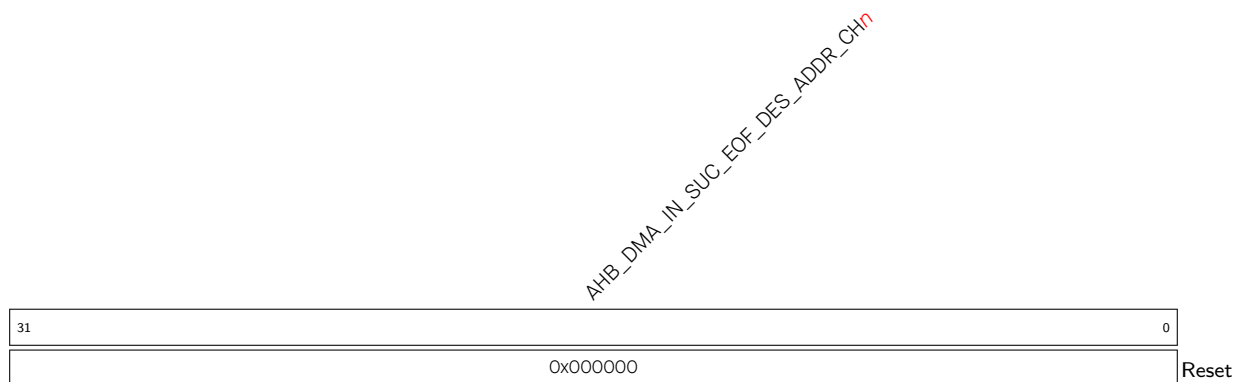
AHB\_DMA\_IN\_BUF\_HUNGRY\_CH<sub>n</sub> Reserved. (RO)

**Register 3.49. AHB\_DMA\_IN\_STATE\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0084+0xC0\**n*)**

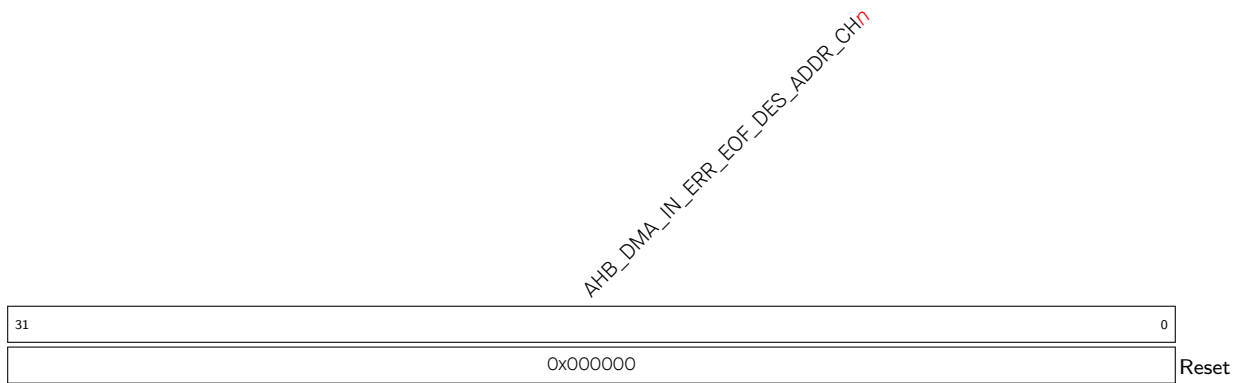
**AHB\_DMA\_INLINK\_DSCR\_ADDR\_CH<sub>*n*</sub>** Represents the lower 18 bits of the next receive descriptor address that is pre-read (but not processed yet). If the current receive descriptor is the last descriptor, then this field represents the address of the current receive descriptor. (RO)

**AHB\_DMA\_IN\_DSCR\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

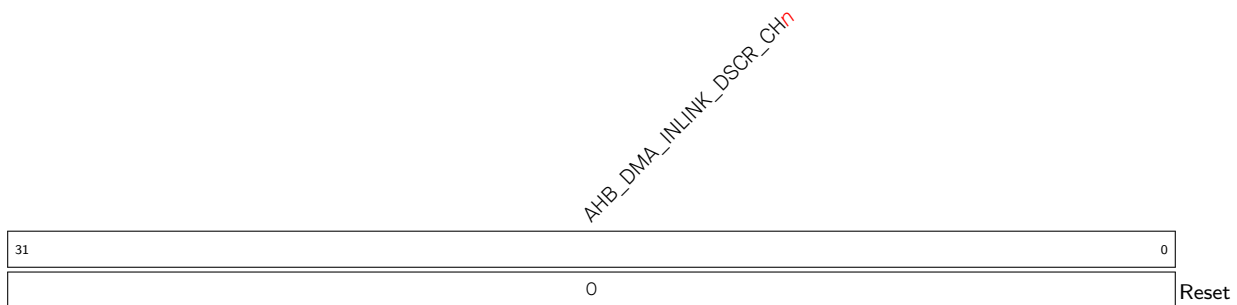
**AHB\_DMA\_IN\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

**Register 3.50. AHB\_DMA\_IN\_SUC\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0088+0xC0\**n*)**

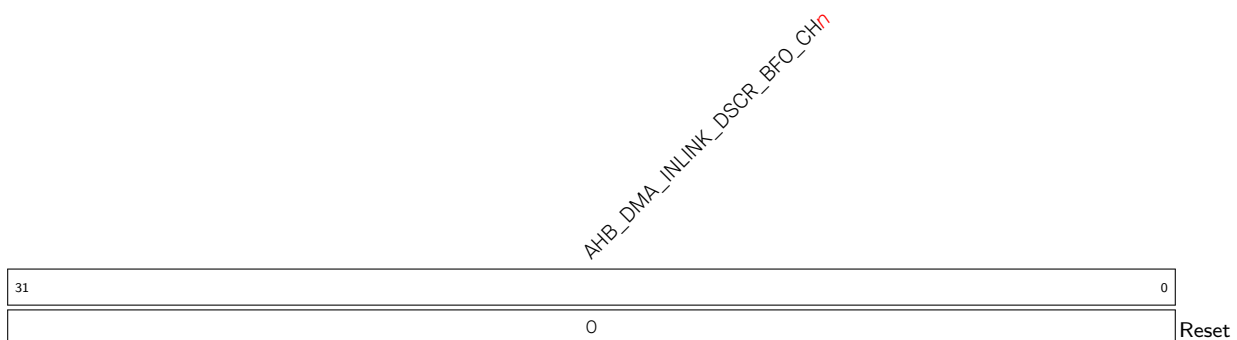
**AHB\_DMA\_IN\_SUC\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>** Represents the address of the receive descriptor when the EOF bit in this descriptor is 1. (RO)

**Register 3.51. AHB\_DMA\_IN\_ERR\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x008C+0xC0\**n*)**

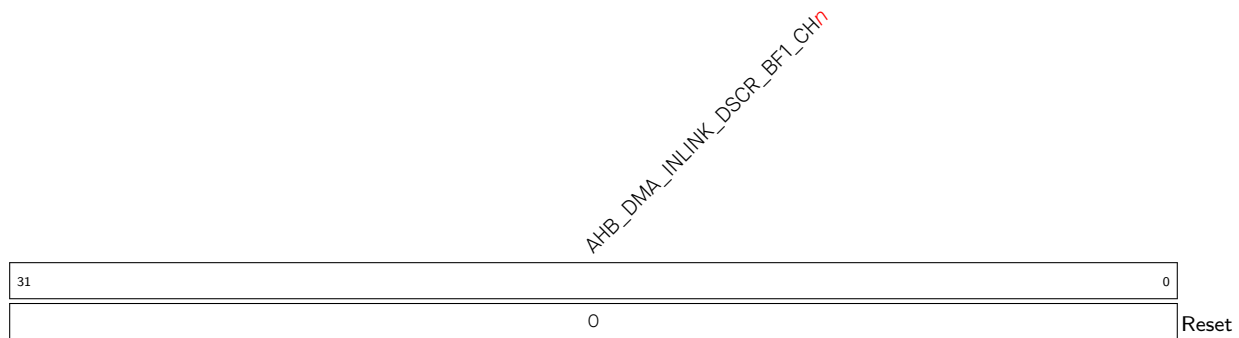
**AHB\_DMA\_IN\_ERR\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>** Represents the address of the receive descriptor when there are some errors in the currently received data. Valid only for UHCI. (RO)

**Register 3.52. AHB\_DMA\_INLINK\_DSCR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0090+0xC0\**n*)**

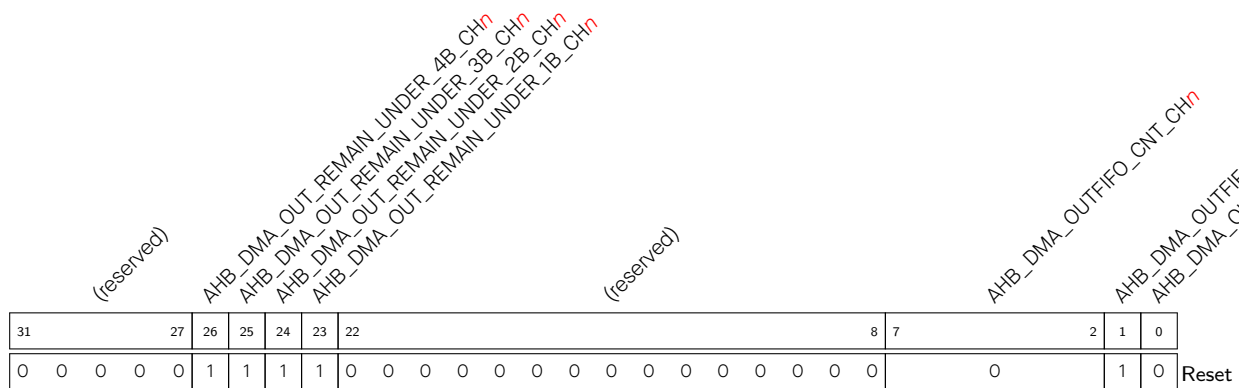
**AHB\_DMA\_INLINK\_DSCR\_CH<sub>*n*</sub>** Represents the address of the next receive descriptor x+1 pointed by the current receive descriptor that is pre-read. (RO)

**Register 3.53. AHB\_DMA\_IN\_DSCR\_BFO\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0094+0xC0\**n*)**

**AHB\_DMA\_INLINK\_DSCR\_BFO\_CH<sub>*n*</sub>** Represents the address of the current receive descriptor x that is pre-read. (RO)

**Register 3.54. AHB\_DMA\_IN\_DSCR\_BF1\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0098+0xC0\**n*)**

**AHB\_DMA\_INLINK\_DSCR\_BF1\_CH<sub>*n*</sub>** Represents the address of the previous receive descriptor x-1 that is pre-read. (RO)

**Register 3.55. AHB\_DMA\_OUTFIFO\_STATUS\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x00D8+0xC0\**n*)**

**AHB\_DMA\_OUTFIFO\_FULL\_CH<sub>*n*</sub>** Represents whether L1 TX FIFO is full.

0: Not Full

1: Full

(RO)

**AHB\_DMA\_OUTFIFO\_EMPTY\_CH<sub>*n*</sub>** Represents whether L1 TX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AHB\_DMA\_OUTFIFO\_CNT\_CH<sub>*n*</sub>** Represents the number of data bytes in L1 TX FIFO for TX channel *n*. (RO)

**AHB\_DMA\_OUT\_REMAIN\_UNDER\_1B\_CH<sub>*n*</sub>** Reserved. (RO)

**AHB\_DMA\_OUT\_REMAIN\_UNDER\_2B\_CH<sub>*n*</sub>** Reserved. (RO)

**AHB\_DMA\_OUT\_REMAIN\_UNDER\_3B\_CH<sub>*n*</sub>** Reserved. (RO)

**AHB\_DMA\_OUT\_REMAIN\_UNDER\_4B\_CH<sub>*n*</sub>** Reserved. (RO)

**Register 3.56. AHB\_DMA\_OUT\_STATE\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x00E4+0xC0\**n*)**

|            |   |   |   |   |   |   |   |   |    |  |   |   |    |   |    |    |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
|------------|---|---|---|---|---|---|---|---|----|--|---|---|----|---|----|----|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| (reserved) |   |   |   |   |   |   |   |   |    | AHB_DMA_OUT_STATE_CH <sub><i>n</i></sub> |   |   |    | AHB_DMA_OUT_DSCR_STATE_CH <sub><i>n</i></sub> |    |    |   | AHB_DMA_OUTLINK_DSCR_ADDR_CH <sub><i>n</i></sub> |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31         |   |   |   |   |   |   |   |   | 23 | 22                                       |   |   | 20 | 19  | 18 | 17 |   |  |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0 | 0 | 0  | 0   | 0  | 0  | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

Reset

**AHB\_DMA\_OUTLINK\_DSCR\_ADDR\_CH<sub>*n*</sub>** Represents the lower 18 bits of the next transmit descriptor address that is pre-read (but not processed yet). If the current transmit descriptor is the last descriptor, then this field represents the address of the current transmit descriptor. (RO)

**AHB\_DMA\_OUT\_DSCR\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

**AHB\_DMA\_OUT\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

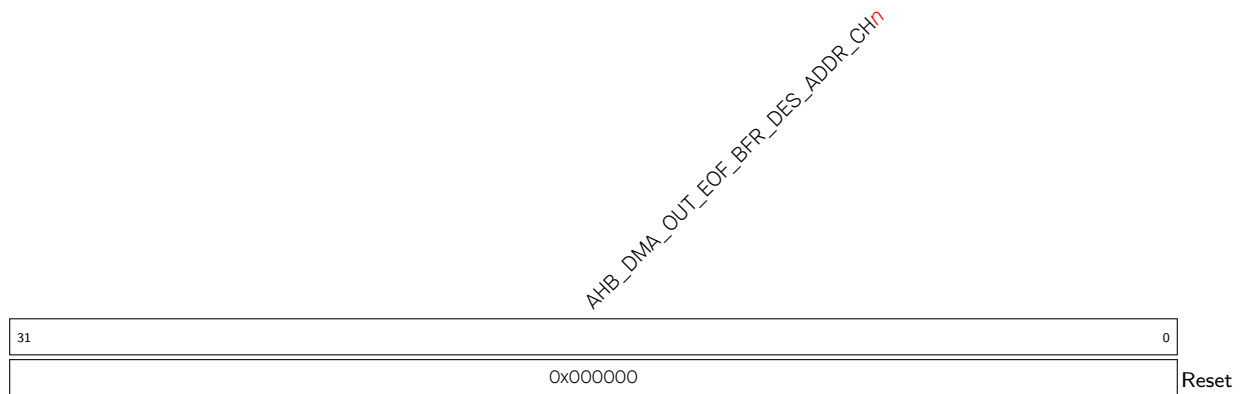
**Register 3.57. AHB\_DMA\_OUT\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x00E8+0xC0\**n*)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| AHB_DMA_OUT_EOF_DES_ADDR_CH <sup>n</sup> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

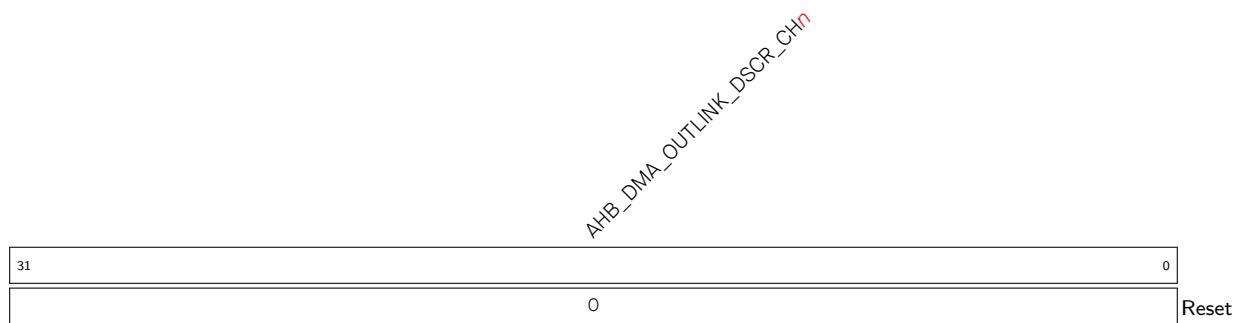
Reset

**AHB\_DMA\_OUT\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>** Represents the address of the transmit descriptor when the EOF bit in this descriptor is 1. (RO)

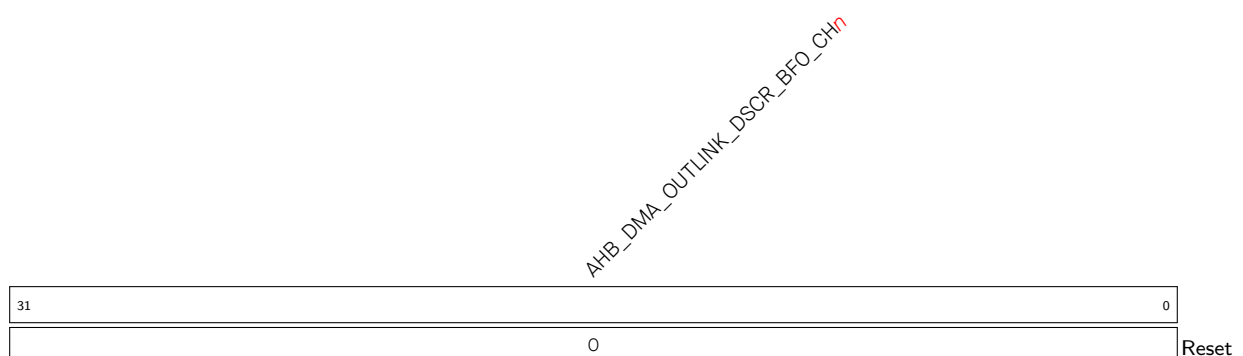


**Register 3.58. AHB\_DMA\_OUT\_EOF\_BFR\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x00EC+0xC0\* $n$ )**

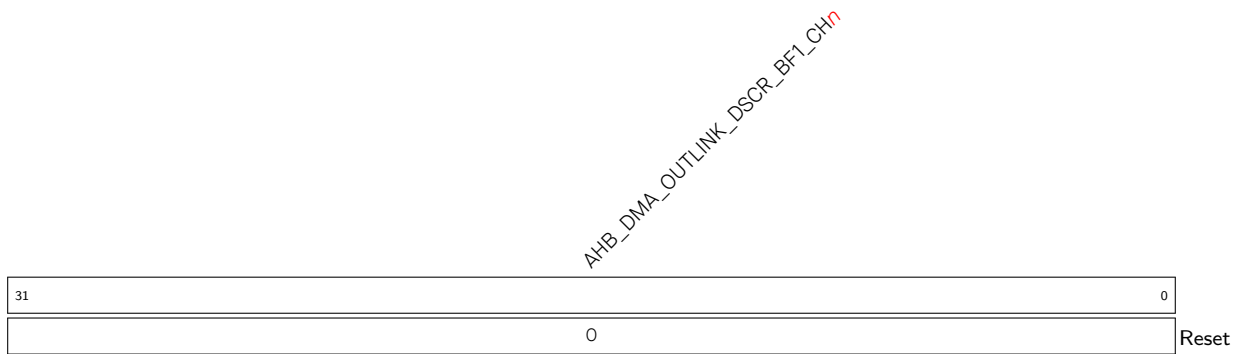
**AHB\_DMA\_OUT\_EOF\_BFR\_DES\_ADDR\_CH $n$**  Represents the address of the transmit descriptor before the last transmit descriptor. (RO)

**Register 3.59. AHB\_DMA\_OUT\_DSCR\_CH $n$ \_REG ( $n$ : 0-2) (0x00F0+0xC0\* $n$ )**

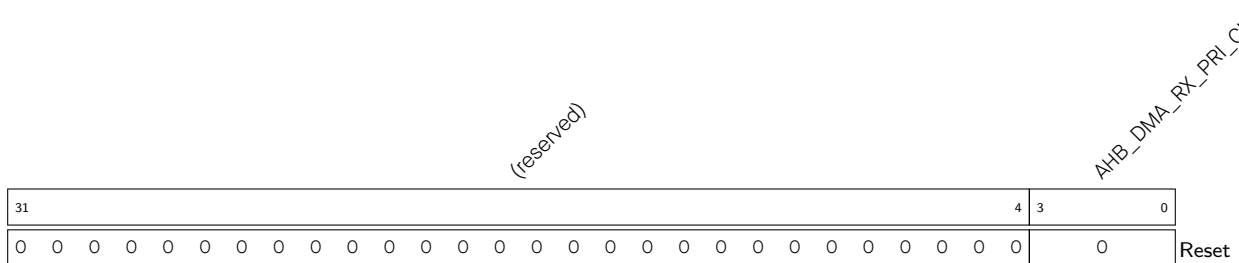
**AHB\_DMA\_OUTLINK\_DSCR\_CH $n$**  Represents the address of the next transmit descriptor  $y+1$  pointed by the current transmit descriptor that is pre-read. (RO)

**Register 3.60. AHB\_DMA\_OUT\_DSCR\_BFO\_CH $n$ \_REG ( $n$ : 0-2) (0x00F4+0xC0\* $n$ )**

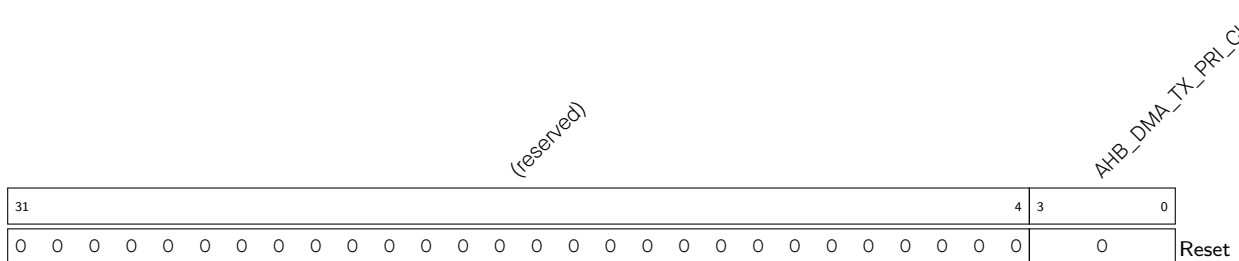
**AHB\_DMA\_OUTLINK\_DSCR\_BFO\_CH $n$**  Represents the address of the current transmit descriptor  $y$  that is pre-read. (RO)

**Register 3.61. AHB\_DMA\_OUT\_DSCR\_BF1\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x00F8+0xC0\**n*)**

**AHB\_DMA\_OUTLINK\_DSCR\_BF1\_CH<sub>*n*</sub>** Represents the address of the previous transmit descriptor y-1 that is pre-read. (RO)

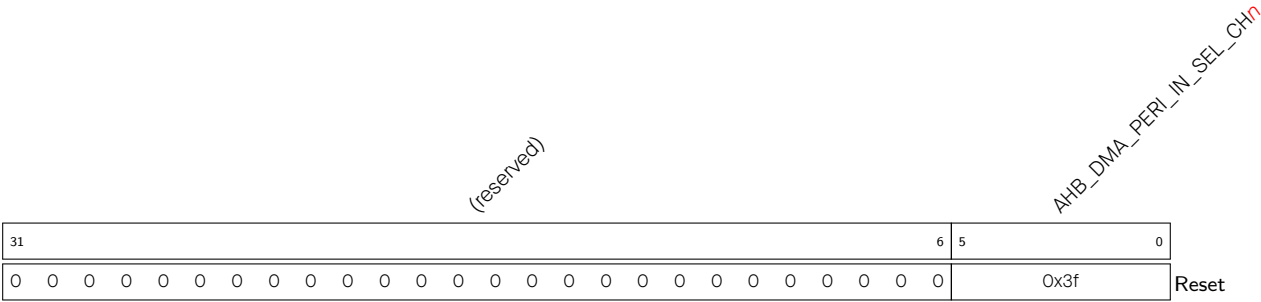
**Register 3.62. AHB\_DMA\_IN\_PRI\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x009C+0xC0\**n*)**

**AHB\_DMA\_RX\_PRI\_CH<sub>*n*</sub>** Configures the priority of RX channel *n*. The larger the value, the higher the priority.  
Value range: 0 ~ 5 (R/W)

**Register 3.63. AHB\_DMA\_OUT\_PRI\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x00FC+0xC0\**n*)**

**AHB\_DMA\_TX\_PRI\_CH<sub>*n*</sub>** Configures the priority of TX channel *n*. The larger the value, the higher the priority.  
Value range: 0 ~ 5 (R/W)

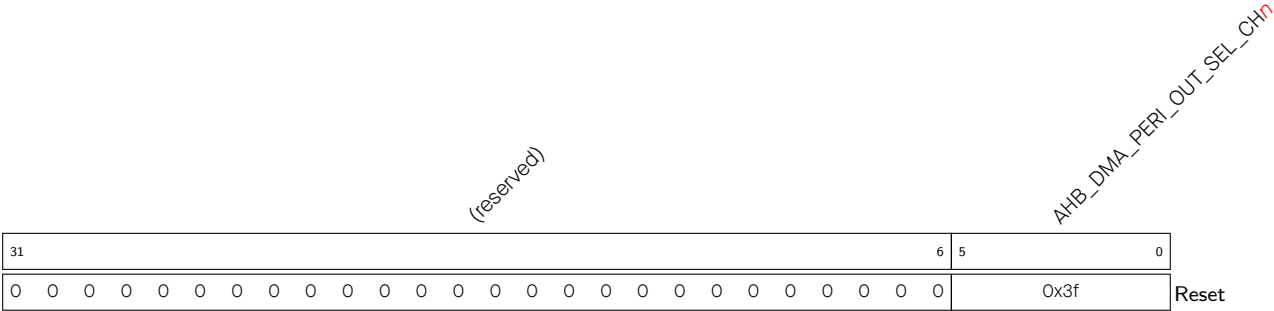
Register 3.64. AHB\_DMA\_IN\_PERI\_SEL\_CHn\_REG (n: 0-2) (0x00A0+0xC0\*n)



AHB\_DMA\_PERI\_IN\_SEL\_CHn Configures the peripheral connected to RX channel n.

- 0: I3C
  - 1: Dummy-1
  - 2: UHCI
  - 3: I2S0
  - 4: I2S1
  - 5: I2S2
  - 6: Dummy-6
  - 7: Dummy-7
  - 8: ADC
  - 9: Dummy-9
  - 10: RMT
  - 11 ~ 15: Dummy-11 ~ Dummy-15
  - 16 ~ 63: Invalid
- (R/W)

Register 3.65. AHB\_DMA\_OUT\_PERI\_SEL\_CHn\_REG (n: 0-2) (0x0100+0xC0\*n)



AHB\_DMA\_OUT\_PERI\_SEL\_CHn Configures the peripheral connected to TX channel n.

- 0: I3C
  - 1: Dummy-1
  - 2: UHCI
  - 3: I2S0
  - 4: I2S1
  - 5: I2S2
  - 6: Dummy-6
  - 7: Dummy-7
  - 8: ADC
  - 9: Dummy-9
  - 10: RMT
  - 11 ~ 15: Dummy-11 ~ Dummy-15
  - 16 ~ 63: Invalid
- (R/W)

3.9.2 GDMA-AXI Registers

The addresses in this section are relative to GDMA-AXI base address provided in Table 6.3-2 in Chapter 6 System and Memory.

For how to program reserved fields, please refer to Section Programming Reserved Register Field.

**Register 3.66. AXI\_DMA\_IN\_INT\_RAW\_CH $n$ \_REG ( $n$ : 0-2) (0x0000+0x68\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   | AXI_DMA_INFIFO_L3_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_INFIFO_L3_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_INFIFO_L2_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_INFIFO_L2_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_INFIFO_L1_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_INFIFO_L1_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_IN_ERR_EOF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_IN_SUC_EOF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_IN_DONE_CH <sub>n</sub> _INT_RAW |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 11 |   |   |   |   |   |   |   |   |   |   |   | 10   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset  |   |   |   |   |   |   |   |   |   |   |

**AXI\_DMA\_IN\_DONE\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_IN\_DONE\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT. For UHCI this bit turns to 1 when the last data byte pointed by one receive descriptor has been received and no data error is detected for RX channel 0. (R/WTC/SS)

**AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. Valid only for UHCI. (R/WTC/SS)

**AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L1\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L1\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L1\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L1\_UDF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L2\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L2\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L2\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L2\_UDF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L3\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L3\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_INFIFO\_L3\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_INFIFO\_L3\_UDF\_CH $n$ \_INT. (R/WTC/SS)

Register 3.67. AXI\_DMA\_IN\_INT\_ST\_CH $n$ \_REG ( $n$ : 0-2) (0x0004+0x68\* $n$ )

|            |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  | AXI_DMA_IN_FIFO_L3_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_FIFO_L3_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_FIFO_L2_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_FIFO_L2_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_FIFO_L1_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_FIFO_L1_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_DSCR_ERR_EOF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_SUC_EOF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_IN_DONE_CH <sub>n</sub> _INT_ST |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  |  |  |  |  | 10  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**AXI\_DMA\_IN\_DONE\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_DONE\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_FIFO\_L2\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L2\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_FIFO\_L2\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L2\_UDF\_CH $n$ \_INT. (RO)

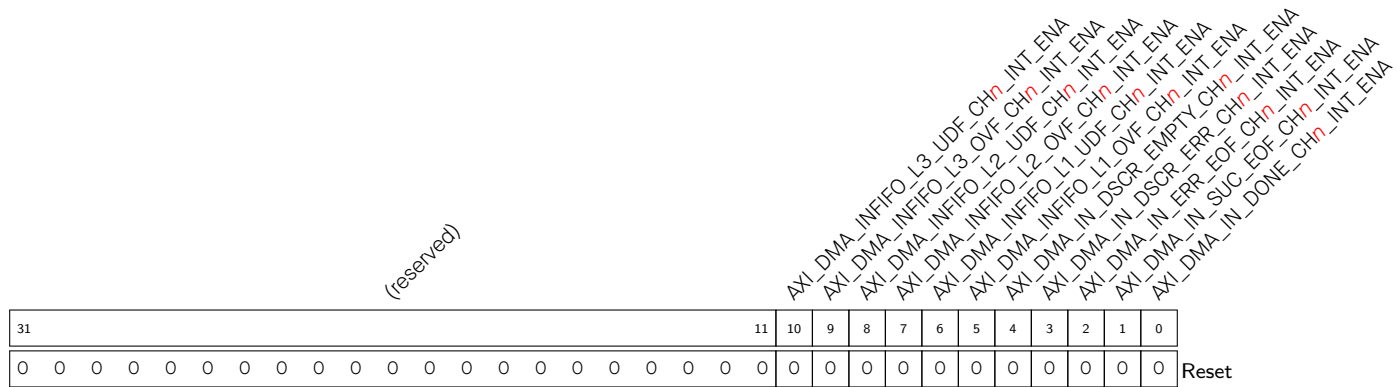
**AXI\_DMA\_IN\_FIFO\_L1\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L1\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_FIFO\_L1\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L1\_UDF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_FIFO\_L3\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L3\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_IN\_FIFO\_L3\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_IN\_FIFO\_L3\_UDF\_CH $n$ \_INT. (RO)

Register 3.68. AXI\_DMA\_IN\_INT\_ENA\_CH $n$ \_REG ( $n$ : 0-2) (0x0008+0x68\* $n$ )



**AXI\_DMA\_IN\_DONE\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable AXI\_DMA\_IN\_DONE\_CH<sub>n</sub>\_INT. (R/W)

**AXI\_DMA\_IN\_SUC\_EOF\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable AXI\_DMA\_IN\_SUC\_EOF\_CH<sub>n</sub>\_INT. (R/W)

**AXI\_DMA\_IN\_ERR\_EOF\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable AXI\_DMA\_IN\_ERR\_EOF\_CH<sub>n</sub>\_INT. (R/W)

**AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_IN\_DSCR\_EMPTY\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable AXI\_DMA\_IN\_DSCR\_EMPTY\_CH<sub>n</sub>\_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L1\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L1\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L1\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L1\_UDF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L2\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L2\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L2\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L2\_UDF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L3\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L3\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_INFIFO\_L3\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_INFIFO\_L3\_UDF\_CH $n$ \_INT.  
(R/W)

Register 3.69. AXI\_DMA\_IN\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-2) (0x000C+0x68\* $n$ )

|            |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  | AXI_DMA_IN_FIFO_L3_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_FIFO_L3_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_FIFO_L2_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_FIFO_L2_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_FIFO_L1_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_FIFO_L1_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_DSCR_ERR_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_SUC_EOF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_IN_DONE_CH <sub>n</sub> _INT_CLR |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  |  |  |  | 10  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0          |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

AXI\_DMA\_IN\_DONE\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_DONE\_CH $n$ \_INT. (WT)

AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_SUC\_EOF\_CH $n$ \_INT. (WT)

AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_ERR\_EOF\_CH $n$ \_INT. (WT)

AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_DSCR\_ERR\_CH $n$ \_INT. (WT)

AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_DSCR\_EMPTY\_CH $n$ \_INT.  
(WT)

AXI\_DMA\_IN\_FIFO\_L1\_OVF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L1\_OVF\_CH $n$ \_INT. (WT)

AXI\_DMA\_IN\_FIFO\_L1\_UDF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L1\_UDF\_CH $n$ \_INT.  
(WT)

AXI\_DMA\_IN\_FIFO\_L2\_OVF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L2\_OVF\_CH $n$ \_INT.  
(WT)

AXI\_DMA\_IN\_FIFO\_L2\_UDF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L2\_UDF\_CH $n$ \_INT.  
(WT)

AXI\_DMA\_IN\_FIFO\_L3\_OVF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L3\_OVF\_CH $n$ \_INT.  
(WT)

AXI\_DMA\_IN\_FIFO\_L3\_UDF\_CH $n$ \_INT\_CLR Write 1 to clear AXI\_DMA\_IN\_FIFO\_L3\_UDF\_CH $n$ \_INT.  
(WT)



Register 3.70. AXI\_DMA\_OUT\_INT\_RAW\_CH $n$ \_REG ( $n$ : 0-2) (0x0138+0x68\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AXI_DMA_OUTFIFO_L3_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUTFIFO_L3_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUTFIFO_L2_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUTFIFO_L2_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUTFIFO_L1_UDF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUTFIFO_L1_OVF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUT_DSCR_ERR_CH <sub>n</sub> _INT_RAW<br>AXI_DMA_OUT_DONE_CH <sub>n</sub> _INT_RAW |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |       |

**AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT. (R/WTC/SS)

**AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT\_RAW** The raw interrupt status of AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT. (R/WTC/SS)

Register 3.71. AXI\_DMA\_OUT\_INT\_ST\_CH $n$ \_REG ( $n$ : 0-2) (0x013C+0x68\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |       |   |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|-------|---|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   | AXI_DMA_OUTFIFO_L3_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUTFIFO_L3_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUTFIFO_L2_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUTFIFO_L2_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUTFIFO_L1_UDF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUTFIFO_L1_OVF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUT_DSCR_ERR_CH <sub>n</sub> _INT_ST<br>AXI_DMA_OUT_DONE_CH <sub>n</sub> _INT_ST |   |   |   |       |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10 | 9 | 8   | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0   | 0 | 0 | 0 | Reset |   |   |   |   |  |

**AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT. (RO)

**AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT\_ST** The masked interrupt status of AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT. (RO)

Register 3.72. AXI\_DMA\_OUT\_INT\_ENA\_CH $n$ \_REG ( $n$ : 0-2) (0x0140+0x68\* $n$ )

|            |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |       |  |
|------------|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   | AXI_DMA_OUTFIFO_L3_UDF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUTFIFO_L3_OVF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUTFIFO_L2_UDF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUTFIFO_L2_OVF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUTFIFO_L1_UDF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUTFIFO_L1_OVF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUT_DSCR_ERR_CH <sub>n</sub> _INT_ENA<br>AXI_DMA_OUT_DONE_CH <sub>n</sub> _INT_ENA |   |   |   |   |   |   |   |       |  |
| 31         |   |   |   |   |   |   |   |   |   | 10 |   |   |   |   |   |   |   |   |   | 9 | 8 | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  |   |   |   |   |   |   |   |       |  |

**AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT. (R/W)

**AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT. (R/W)

**AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT.  
(R/W)

**AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT\_ENA** Write 1 to enable AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT.  
(R/W)

Register 3.73. AXI\_DMA\_OUT\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-2) (0x0144+0x68\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |   |   |   |   |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|--|---|---|---|---|---|---|---|---|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AXI_DMA_OUTFIFO_L3_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUTFIFO_L3_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUTFIFO_L2_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUTFIFO_L2_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUTFIFO_L1_UDF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUTFIFO_L1_OVF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUT_DSCR_ERR_CH <sub>n</sub> _INT_CLR<br>AXI_DMA_OUT_DONE_CH <sub>n</sub> _INT_CLR |  |   |   |   |   |   |   |   |   |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10   |  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset  |  |   |   |   |   |   |   |   |   |   |   |  |  |

**AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUT\_DONE\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUT\_EOF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$ \_INT. (WT)

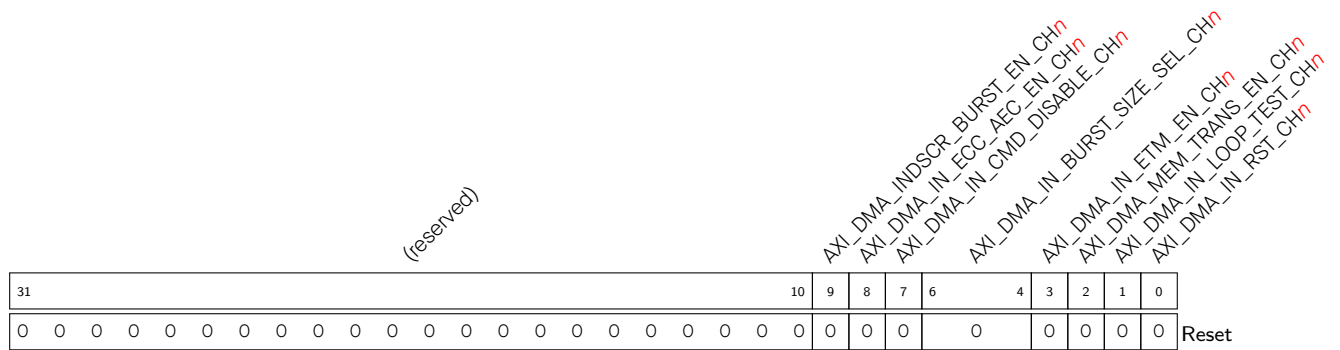
**AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH $n$ \_INT. (WT)

**AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT\_CLR** Write 1 to clear AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH $n$ \_INT. (WT)

**Register 3.74. AXI\_DMA\_IN\_CONFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0010+0x68\* $n$ )**

**AXI\_DMA\_IN\_RST\_CH $n$**  Write 1 and then 0 to reset RX channel  $n$  FSM and RX FIFO pointer.(R/W)

**AXI\_DMA\_IN\_LOOP\_TEST\_CH $n$**  Reserved. (R/W)

**AXI\_DMA\_MEM\_TRANS\_EN\_CH $n$**  Configures whether to enable memory-to-memory data transfer.

0: Disable

1: Enable

(R/W)

**AXI\_DMA\_IN\_ETM\_EN\_CH $n$**  Configures whether to enable ETM control for RX channel  $n$ .

0: Disable

1: Enable

(R/W)

**AXI\_DMA\_IN\_BURST\_SIZE\_SEL\_CH $n$**  Configures the burst length for RX channel  $n$ .

0: 8 bytes

1: 16 bytes

2: 32 bytes

3: 64 bytes

4: 128 bytes

5 ~ 7: Invalid

(R/W)

**AXI\_DMA\_IN\_CMD\_DISABLE\_CH $n$**  Configures whether to disable command on RX channel  $n$ .

0: Enable

1: Disable

(R/W)

**AXI\_DMA\_IN\_ECC\_AEC\_EN\_CH $n$**  Configures whether AXI DMA can access external memory space for ECC and AES via RX channel  $n$ .

0: Not access

1: Access

(R/W)

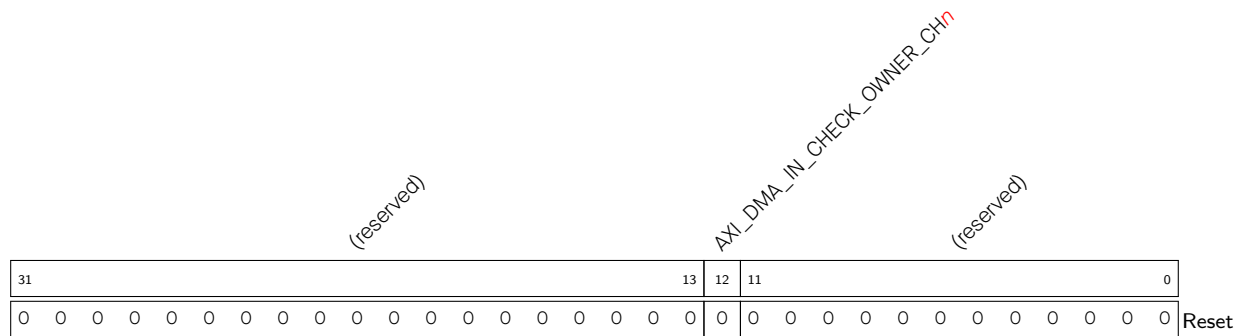
**AXI\_DMA\_INDCR\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for RX channel  $n$  to read descriptors when accessing internal memory.

0: Disable

1: Enable

(R/W)

Register 3.75. AXI\_DMA\_IN\_CONF1\_CH $n$ \_REG ( $n$ : 0-2) (0x0014+0x68\* $n$ )



**AXI\_DMA\_IN\_CHECK\_OWNER\_CH<sub>n</sub>** Configures whether to enable owner bit check for RX channel

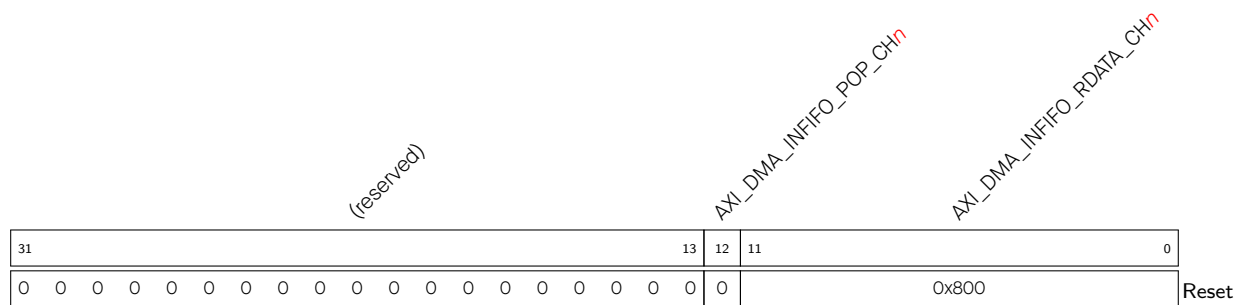
 $n.$ 

0: Disable

1: Enable

(R/W)

Register 3.76. AXI\_DMA\_IN\_POP\_CH $n$ \_REG ( $n$ : 0-2) (0x001C+0x68\* $n$ )



**AXI\_DMA\_INFIFO\_RDATA\_CH<sub>n</sub>** Represents the data popped from AXI DMA RX FIFO. (RO)

**AXI\_DMA\_INFIFO\_POP\_CHn** Configures whether to pop data from AXI DMA RX FIFO.

0: Invalid. No effect

1: Pop

(WT)

Register 3.77. AXI\_DMA\_IN\_LINK1\_CH $n$ \_REG ( $n$ : 0-2) (0x0020+0x68\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AXI_DMA_INLINK_PARK_CH <sub>n</sub><br>AXI_DMA_INLINK_RESTART_CH <sub>n</sub><br>AXI_DMA_INLINK_START_CH <sub>n</sub><br>AXI_DMA_INLINK_STOP_CH <sub>n</sub><br>AXI_DMA_INLINK_AUTO_RET_CH <sub>n</sub> |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5   | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1   | 0 | 0 | 0 | 1 |   |       |

**AXI\_DMA\_INLINK\_AUTO\_RET\_CH $n$**  Configures whether to return to the current receive descriptor's address when there are some errors in current receiving data.

0: Not return

1: Return

(R/W)

**AXI\_DMA\_INLINK\_STOP\_CH $n$**  Configures whether to stop RX channel  $n$  from receiving data.

0: Invalid. No effect

1: Stop

(WT)

**AXI\_DMA\_INLINK\_START\_CH $n$**  Configures whether to enable RX channel  $n$  for data transfer.

0: Disable

1: Enable

(WT)

**AXI\_DMA\_INLINK\_RESTART\_CH $n$**  Configures whether to restart RX channel  $n$  for AXI DMA transfer.

0: Invalid. No effect

1: Restart

(WT)

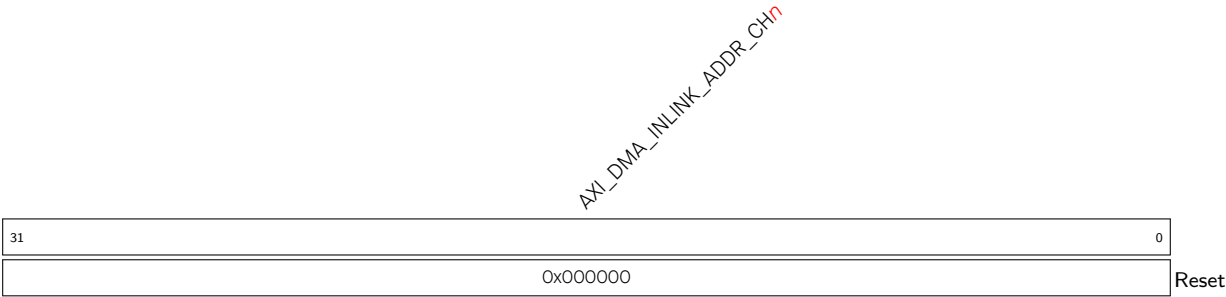
**AXI\_DMA\_INLINK\_PARK\_CH $n$**  Represents the status of the receive descriptor's FSM.

0: Running

1: Idle

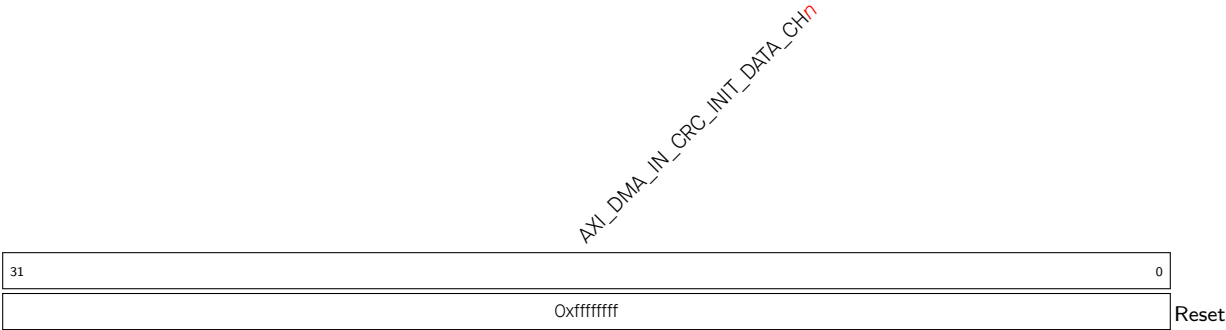
(RO)

Register 3.78. AXI\_DMA\_IN\_LINK2\_CHn\_REG (n: 0-2) (0x0024+0x68\*n)



AXI\_DMA\_INLINK\_ADDR\_CHn Represents the first receive descriptor’s address. (R/W)

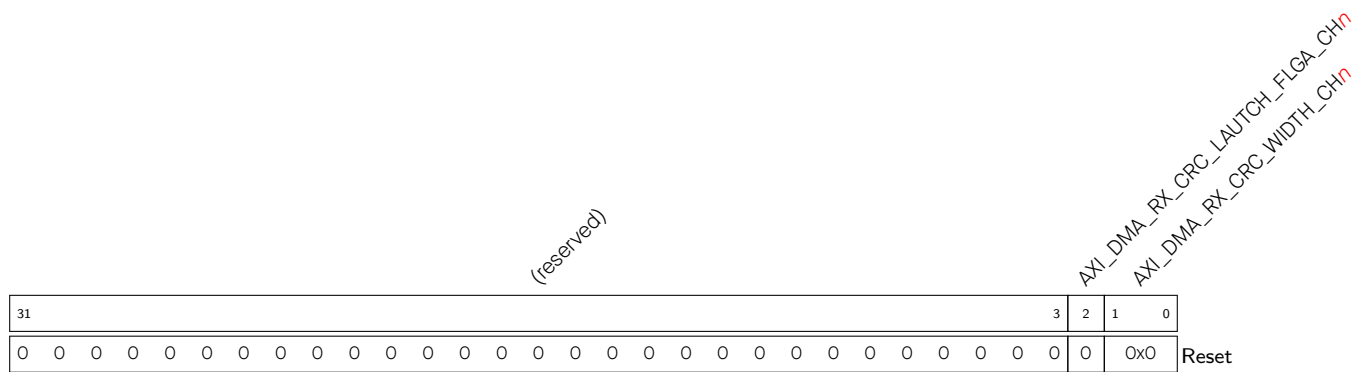
Register 3.79. AXI\_DMA\_IN\_CRC\_INIT\_DATA\_CHn\_REG (n: 0-2) (0x0048+0x68\*n)



AXI\_DMA\_IN\_CRC\_INIT\_DATA\_CHn Configures the CRC initial value for RX channel n. (R/W)



Register 3.80. AXI\_DMA\_RX\_CRC\_WIDTH\_CH $n$ \_REG ( $n$ : 0-2) (0x004C+0x68\* $n$ )



**AXI\_DMA\_RX\_CRC\_WIDTH\_CH $n$**  Configures the CRC result width for RX channel  $n$ . 0:  $\leq 8$  bits

1:  $\leq 16$  bits

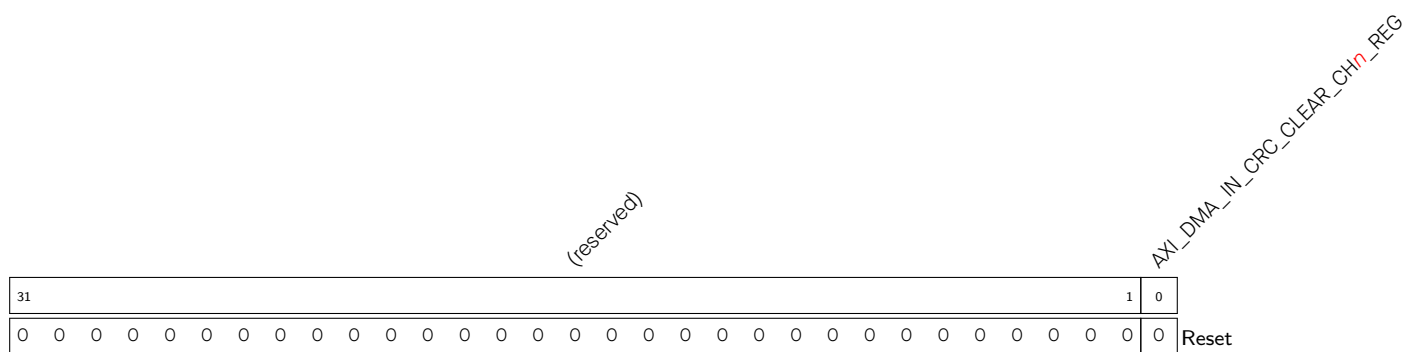
2:  $\leq 24$  bits

3:  $\leq 32$  bits

(R/W)

**AXI\_DMA\_RX\_CRC\_LAUTCH\_FLGA\_CH $n$**  Write 1 and then 0 to latch the values of AXI\_DMA\_RX\_CRC\_EN\_ADDR\_CH $n$ , AXI\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH $n$ , AXI\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$ , and AXI\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ . (R/W)

**Register 3.81. AXI\_DMA\_IN\_CRC\_CLEAR\_CH $n$ \_REG ( $n$ : 0-2) (0x0050+0x68\* $n$ )**

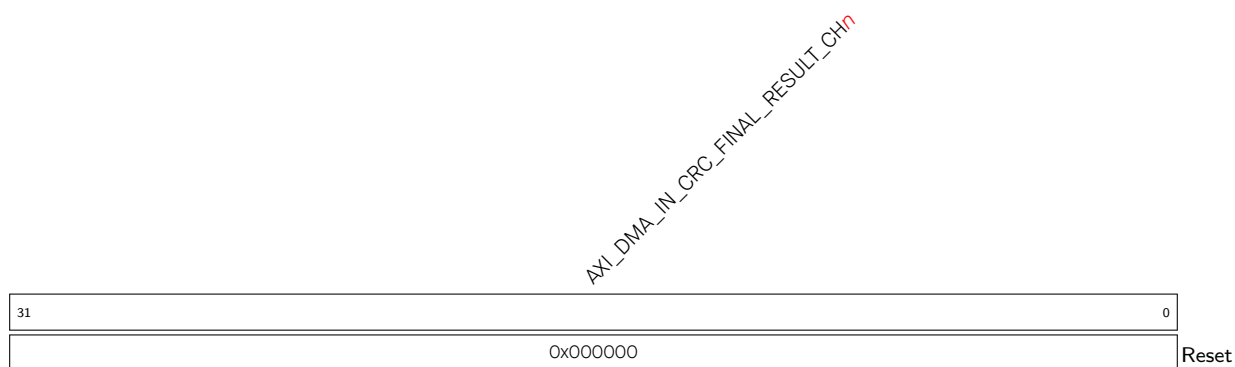


**AXI\_DMA\_IN\_CRC\_CLEAR\_CH $n$ \_REG** Configures whether to clear the CRC result for RX channel  $n$ .

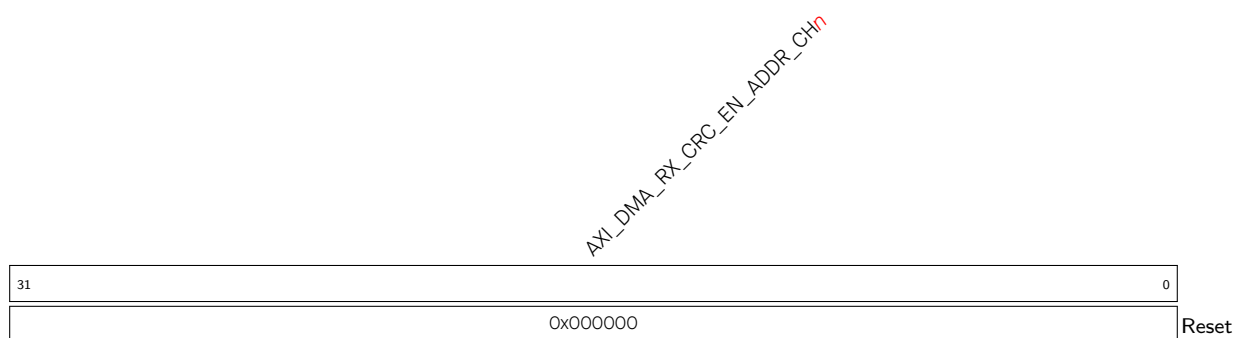
0: Not clear

1: Clear

(R/W)

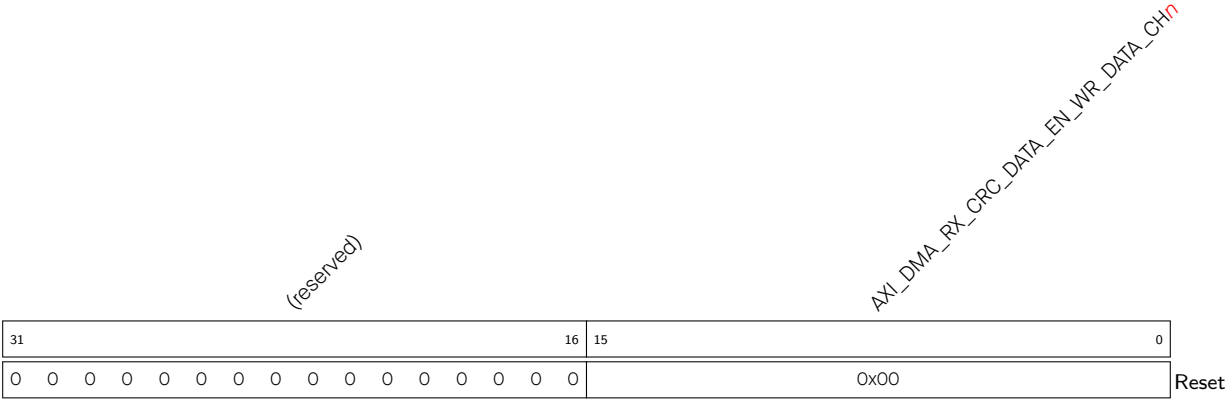
Register 3.82. AXI\_DMA\_IN\_CRC\_FINAL\_RESULT\_CH $n$ \_REG ( $n$ : 0-2) (0x0054+0x68\* $n$ )

AXI\_DMA\_IN\_CRC\_FINAL\_RESULT\_CH $n$  Represents the CRC result for RX channel  $n$ . (RO)

Register 3.83. AXI\_DMA\_RX\_CRC\_EN\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x005C+0x68\* $n$ )

AXI\_DMA\_RX\_CRC\_EN\_ADDR\_CH $n$  Configures at which bit of the CRC result the AXI\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$ \_REG register targets for TX channel  $n$ . (R/W)

Register 3.84. AXI\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x0060+0x68\* $n$ )

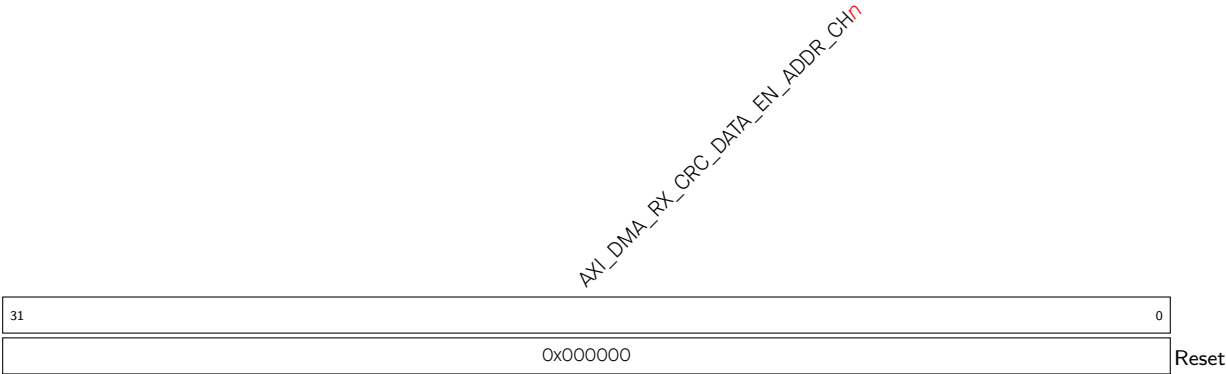


AXI\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$  Configures whether to include each bit of the data in the CRC calculation matrix for TX channel  $n$ .

- 0: Not include
- 1: Include

(R/W)

Register 3.85. AXI\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0064+0x68\* $n$ )



AXI\_DMA\_RX\_CRC\_DATA\_EN\_ADDR\_CH $n$  Configures at which bit of the CRC result the AXI\_DMA\_RX\_CRC\_DATA\_EN\_WR\_DATA\_CH $n$ \_REG register targets for TX channel  $n$ . (R/W)

Register 3.86. AXI\_DMA\_OUT\_CONFO\_CH $n$ \_REG( $n$ : 0-2) (0x0148+0x68\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    | AXI_DMA_OUTDSCR_BURST_EN_CHn<br>AXI_DMA_OUT_ECC_AEC_EN_CHn<br>AXI_DMA_OUT_CMD_DISABLE_CHn<br>AXI_DMA_OUT_BURST_SIZE_SEL_CHn<br>AXI_DMA_OUT_ETM_EN_CHn<br>AXI_DMA_OUT_EOF_MODE_CHn<br>AXI_DMA_OUT_AUTO_WB_CHn<br>AXI_DMA_OUT_LOOP_TEST_CHn |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 11 | 10 | 9   | 8 | 7 | 5 |   | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**AXI\_DMA\_OUT\_RST\_CH $n$**  Configures the reset state of TX channel  $n$  FSM and TX FIFO pointer.

0: Release reset

1: Reset

(R/W)

**AXI\_DMA\_OUT\_LOOP\_TEST\_CH $n$**  Reserved. (R/W)

**AXI\_DMA\_OUT\_AUTO\_WRBACK\_CH $n$**  Configures whether to enable automatic outlink write-back when all the data in TX FIFO has been transmitted.

0: Disable

1: Enable

(R/W)

**AXI\_DMA\_OUT\_EOF\_MODE\_CH $n$**  Configures when to generate EOF flag.

0: EOF flag for TX channel  $n$  is generated when data to be transmitted has been pushed into FIFO in AXI DMA.

1: EOF flag for TX channel  $n$  is generated when data to be transmitted has been popped from FIFO in AXI DMA.

(R/W)

**AXI\_DMA\_OUT\_ETM\_EN\_CH $n$**  Configures whether to enable ETM control for TX channel  $n$ .

0: Disable

1: Enable

(R/W)

**AXI\_DMA\_OUT\_BURST\_SIZE\_SEL\_CH $n$**  Configures the burst length for TX channel  $n$ .

0: 8 bytes

1: 16 bytes

2: 32 bytes

3: 64 bytes

4: 128 bytes

5 ~ 7: Invalid

(R/W)

**AXI\_DMA\_OUT\_CMD\_DISABLE\_CH $n$**  Configures whether to disable command on TX channel  $n$ .

0: Enable

1: Disable

(R/W)

Continued on the next page...

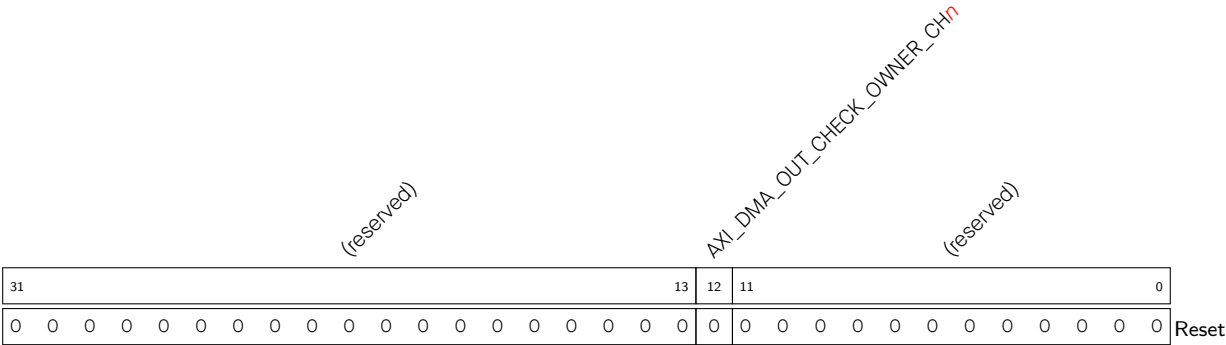
Register 3.86. AXI\_DMA\_OUT\_CONFO\_CH $n$ \_REG( $n$ : 0-2) (0x0148+0x68\* $n$ )

Continued from the previous page...

**AXI\_DMA\_OUT\_ECC\_AEC\_EN\_CH $n$**  Configures whether AXI DMA can access external memory space for ECC and AES via TX channel  $n$ .  
0: Not access  
1: Access  
(R/W)

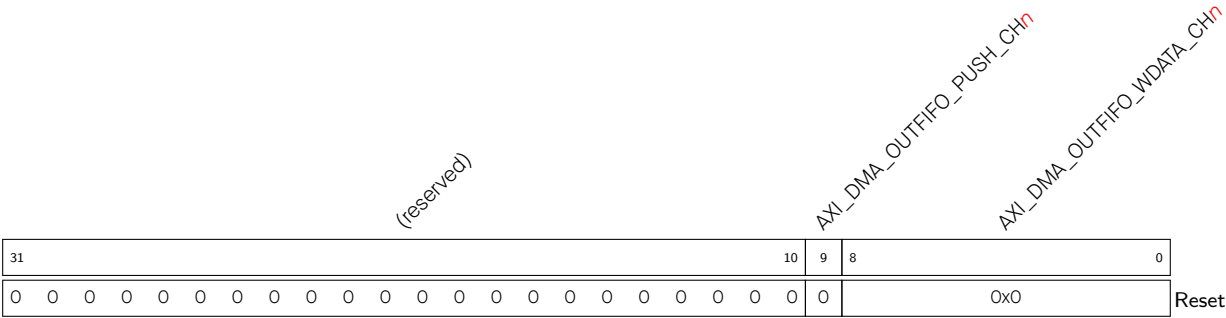
**AXI\_DMA\_OUTDSCR\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for TX channel  $n$  reading descriptors when accessing internal memory.  
0: Disable  
1: Enable  
(R/W)

Register 3.87. AXI\_DMA\_OUT\_CONF1\_CH $n$ \_REG ( $n$ : 0-2) (0x014C+0x68\* $n$ )



**AXI\_DMA\_OUT\_CHECK\_OWNER\_CH $n$**  Configures whether to enable owner bit check for TX channel  $n$ .  
0: Disable  
1: Enable  
(R/W)

Register 3.88. AXI\_DMA\_OUT\_PUSH\_CHn\_REG (n: 0-2) (0x0154+0x68\*n)



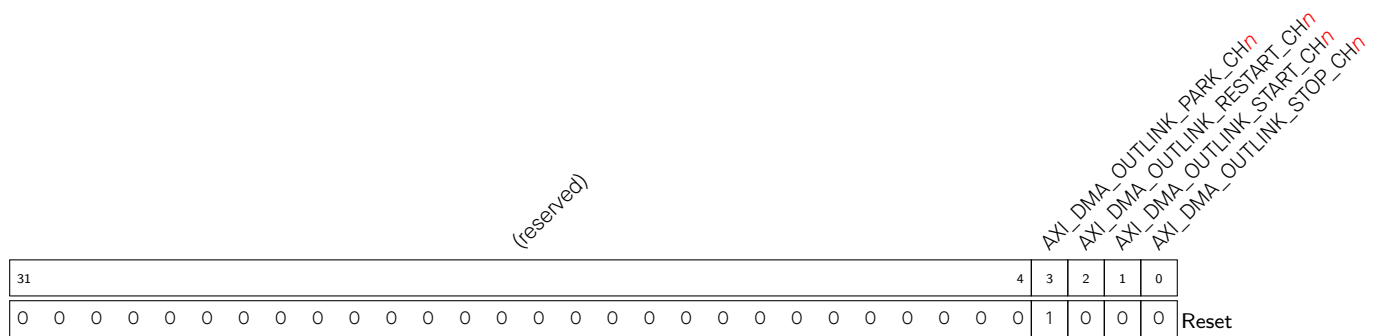
**AXI\_DMA\_OUTFIFO\_WDATA\_CHn** Represents the data that need to be pushed into AXI DMA TX FIFO. (R/W)

**AXI\_DMA\_OUTFIFO\_PUSH\_CHn** Configures whether to push data into AXI DMA TX FIFO.

0: Invalid. No effect

1: Push

(WT)

Register 3.89. AXI\_DMA\_OUT\_LINK1\_CH $n$ \_REG ( $n$ : 0-2) (0x0158+0x68\* $n$ )

**AXI\_DMA\_OUTLINK\_STOP\_CH $n$**  Configures whether to stop TX channel  $n$  from transmitting data.

- 0: Invalid. No effect
- 1: Stop (WT)

**AXI\_DMA\_OUTLINK\_START\_CH $n$**  Configures whether to enable TX channel  $n$  for data transfer.

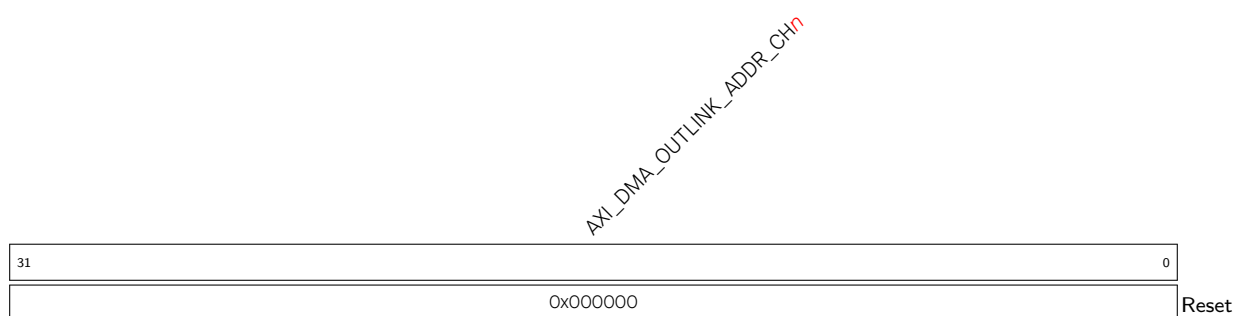
- 0: Disable
- 1: Enable (WT)

**AXI\_DMA\_OUTLINK\_RESTART\_CH $n$**  Configures whether to restart TX channel  $n$  for AXI DMA transfer.

- 0: Invalid. No effect
- 1: Restart (WT)

**AXI\_DMA\_OUTLINK\_PARK\_CH $n$**  Represents the status of the transmit descriptor's FSM.

- 0: Running
- 1: Idle (RO)

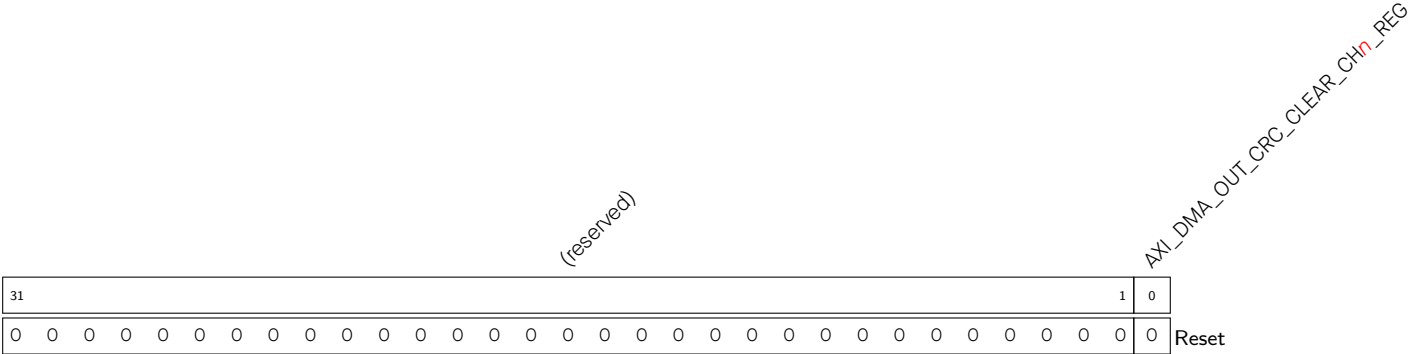
Register 3.90. AXI\_DMA\_OUT\_LINK2\_CH $n$ \_REG ( $n$ : 0-2) (0x015C+0x68\* $n$ )

**AXI\_DMA\_OUTLINK\_ADDR\_CH $n$**  Represents the first transmit descriptor's address. (R/W)





Register 3.93. AXI\_DMA\_OUT\_CRC\_CLEAR\_CH $n$ \_REG ( $n$ : 0-2) (0x0188+0x68\* $n$ )



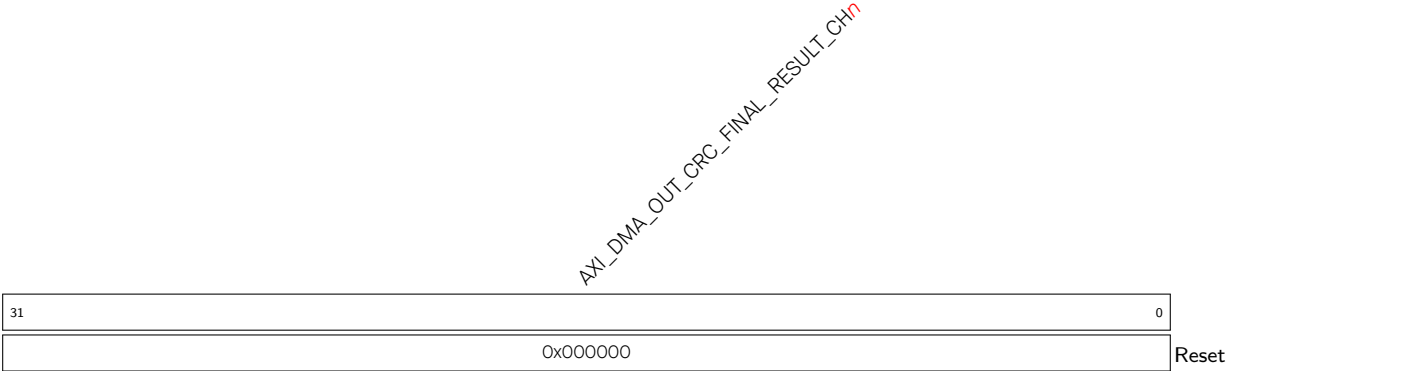
**AXI\_DMA\_OUT\_CRC\_CLEAR\_CH $n$ \_REG** Configures whether to clear the CRC result for TX channel  $n$ .

0: Not clear

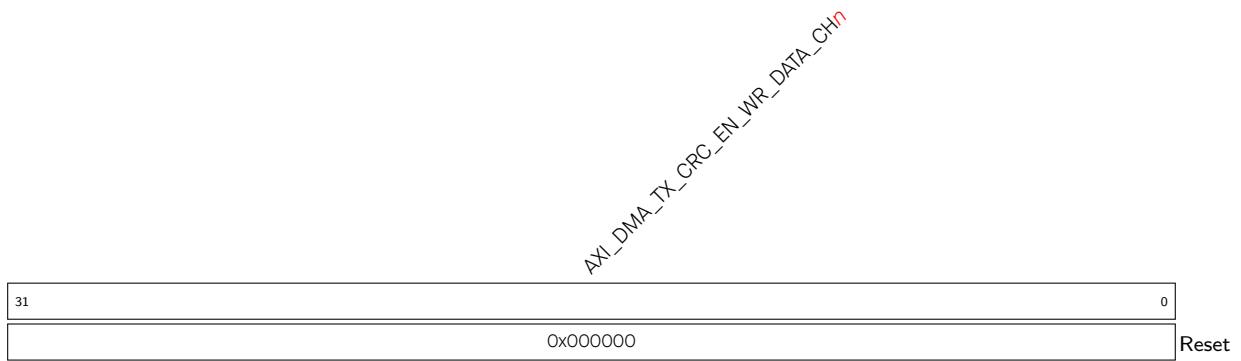
1: Clear

(R/W)

Register 3.94. AXI\_DMA\_OUT\_CRC\_FINAL\_RESULT\_CH $n$ \_REG ( $n$ : 0-2) (0x018C+0x68\* $n$ )



**AXI\_DMA\_OUT\_CRC\_FINAL\_RESULT\_CH $n$**  Represents the CRC result for TX channel  $n$ . (RO)

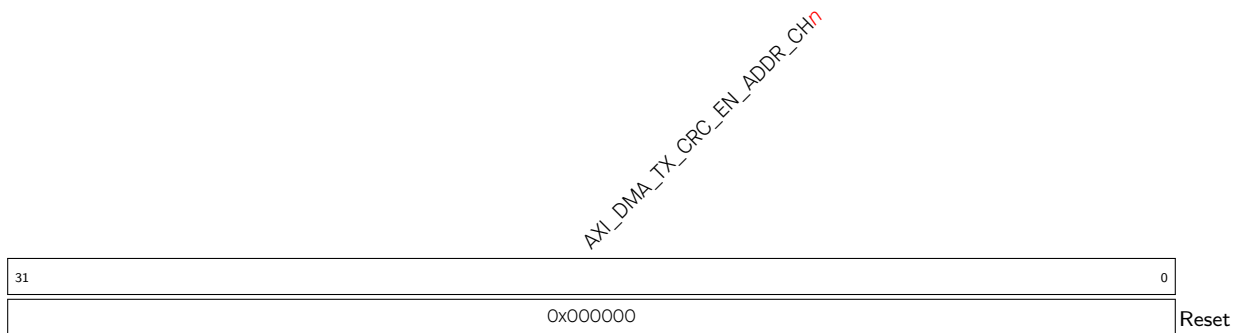
**Register 3.95. AXI\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0190+0x68\**n*)**

**AXI\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH<sub>*n*</sub>** Configures whether to include each bit of the intermediate result in the CRC calculation matrix for TX channel *n*.

0: Not include

1: Include

(R/W)

**Register 3.96. AXI\_DMA\_TX\_CRC\_EN\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0194+0x68\**n*)**

**AXI\_DMA\_TX\_CRC\_EN\_ADDR\_CH<sub>*n*</sub>** Configures at which bit of the CRC result the AXI\_DMA\_TX\_CRC\_EN\_WR\_DATA\_CH<sub>*n*</sub>\_REG register targets for TX channel *n*. (R/W)

(reserved)

AXI\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH<sup>n</sup>

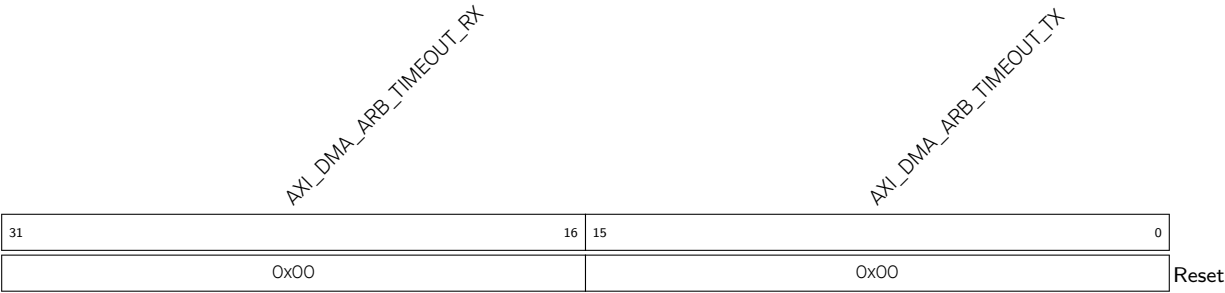
(R/W)

AXI\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH1

AXI\_DMA\_TX\_CRC\_DATA\_EN\_ADDR\_CH1

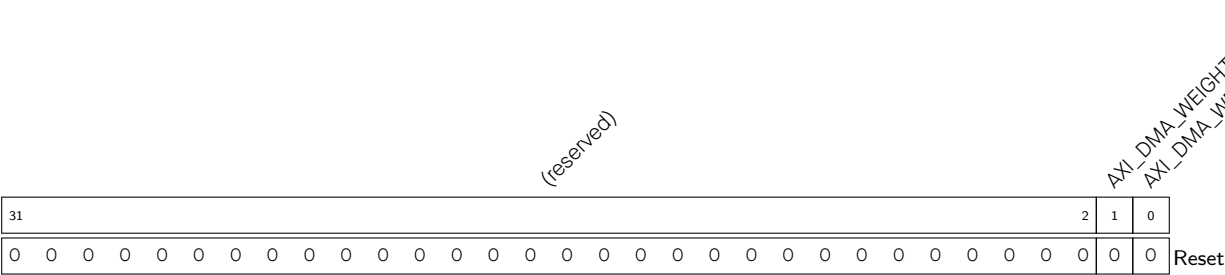
AAXI\_DMA\_TX\_CRC\_DATA\_EN\_WR\_DATA\_CH*n*\_REG register targets for TX channel *n*.(R/W)

Register 3.99. AXI\_DMA\_ARB\_TIMEOUT\_REG (0x0270)



- AXI\_DMA\_ARB\_TIMEOUT\_TX Configures the time slot for TX. Measurement unit: AXI bus clock cycle. (R/W)
- AXI\_DMA\_ARB\_TIMEOUT\_RX Configures the time slot for RX. Measurement unit: AXI bus clock cycle. (R/W)

Register 3.100. AXI\_DMA\_WEIGHT\_EN\_REG (0x0274)



- AXI\_DMA\_WEIGHT\_EN\_TX Configures whether to enable weight arbitration for TX.  
0: Disable  
1: Enable  
(R/W)
- AXI\_DMA\_WEIGHT\_EN\_RX Configures whether to enable weight arbitration for RX.  
0: Disable  
1: Enable  
(R/W)

**Register 3.101. AXI\_DMA\_IN\_MEM\_CONF\_REG (0x0278)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AXI_DMA_OUT_MEM_FORCE_PD<br>AXI_DMA_OUT_MEM_FORCE_PU<br>AXI_DMA_IN_MEM_FORCE_PD<br>AXI_DMA_IN_MEM_FORCE_PU |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6  | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**AXI\_DMA\_IN\_MEM\_CLK\_FORCE\_EN** Configures memory clock gating for RX.

0: Support clock only when AXI DMA accesses memory

1: Always force the clock on

(R/W)

**AXI\_DMA\_IN\_MEM\_FORCE\_PU** Configures whether to force power up memory for RX.

0: Not force power up

1: Force power up

(R/W)

**AXI\_DMA\_IN\_MEM\_FORCE\_PD** Configures whether to force power down memory for RX.

0: Not force power down

1: Force power down

(R/W)

**AXI\_DMA\_OUT\_MEM\_CLK\_FORCE\_EN** Configures memory clock gating for TX.

0: Support clock only when AXI DMA accesses memory

1: Always force the clock on

(R/W)

**AXI\_DMA\_OUT\_MEM\_FORCE\_PU** Configures whether to force power up memory for TX.

0: Not force power up

1: Force power up

(R/W)

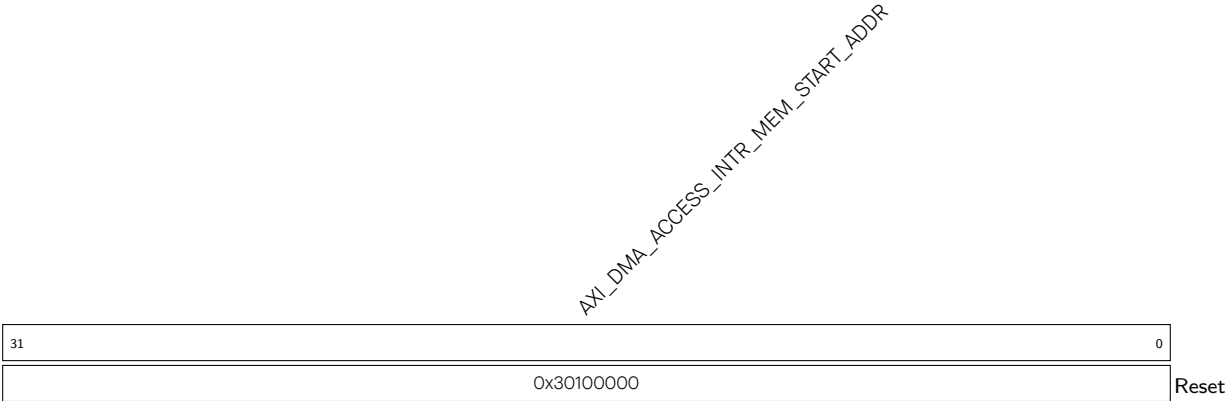
**AXI\_DMA\_OUT\_MEM\_FORCE\_PD** Configures whether to force power down memory for TX.

0: Not force power down

1: Force power down

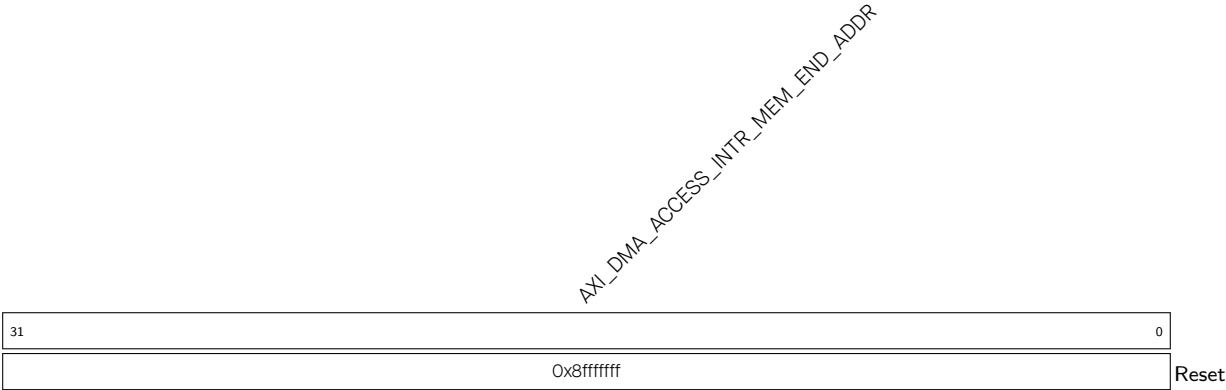
(R/W)

Register 3.102. AXI\_DMA\_INTR\_MEM\_START\_ADDR\_REG (0x027C)



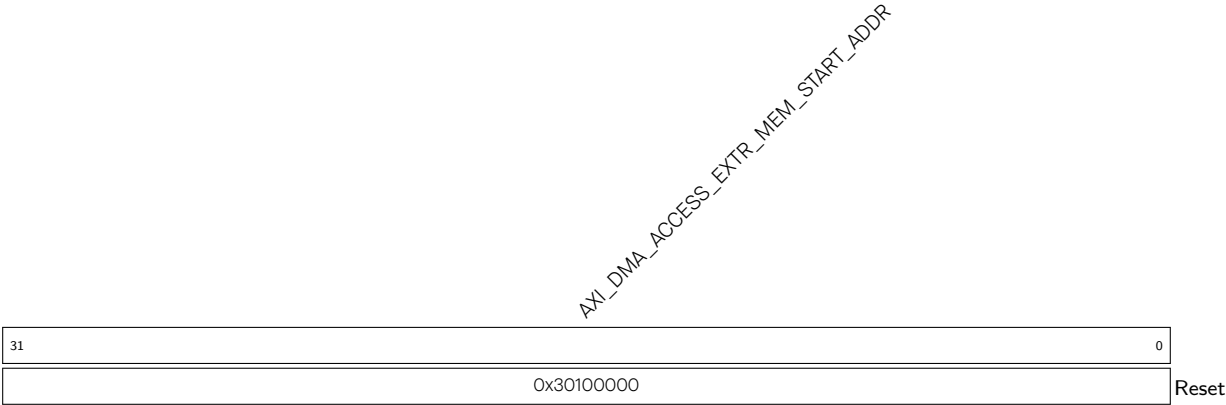
**AXI\_DMA\_ACCESS\_INTR\_MEM\_START\_ADDR** Configures the start address of the accessible internal memory address space. (R/W)

Register 3.103. AXI\_DMA\_INTR\_MEM\_END\_ADDR\_REG (0x0280)



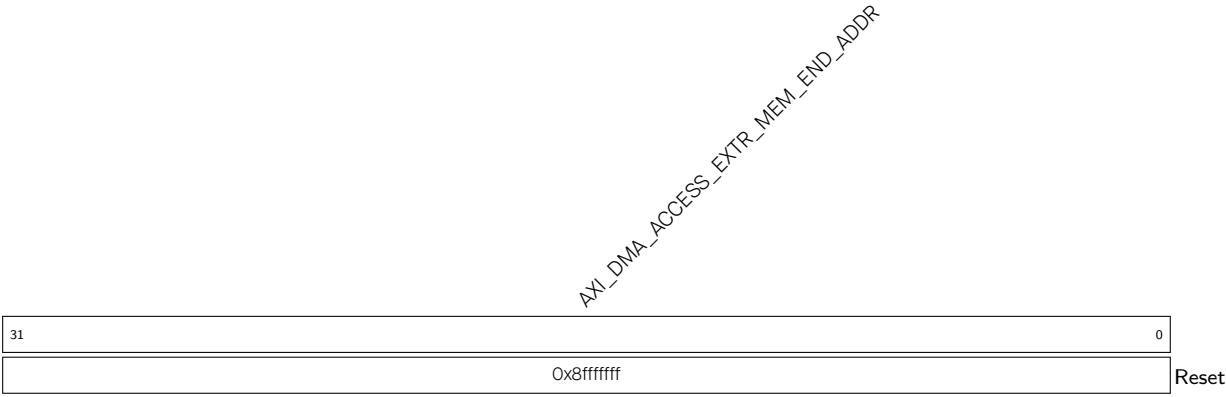
**AXI\_DMA\_ACCESS\_INTR\_MEM\_END\_ADDR** Configures the end address of the accessible internal memory address space. (R/W)

Register 3.104. AXI\_DMA\_EXTR\_MEM\_START\_ADDR\_REG (0x0284)



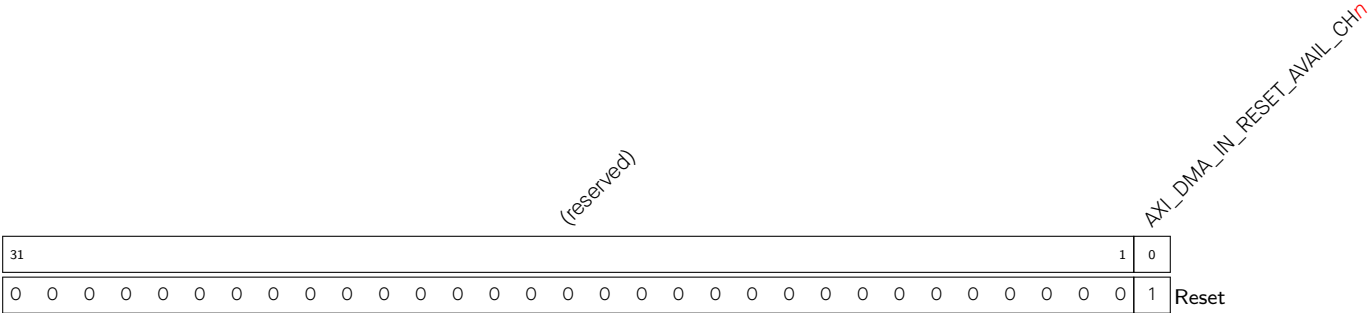
**AXI\_DMA\_ACCESS\_EXTR\_MEM\_START\_ADDR** Configures the start address of the accessible external memory address space. (R/W)

Register 3.105. AXI\_DMA\_EXTR\_MEM\_END\_ADDR\_REG (0x0288)



**AXI\_DMA\_ACCESS\_EXTR\_MEM\_END\_ADDR** Configures the end address of the accessible external memory address space. (R/W)

Register 3.106. AXI\_DMA\_IN\_RESET\_AVAIL\_CH $n$ \_REG ( $n$ : 0-2) (0x028C+0x4\* $n$ )



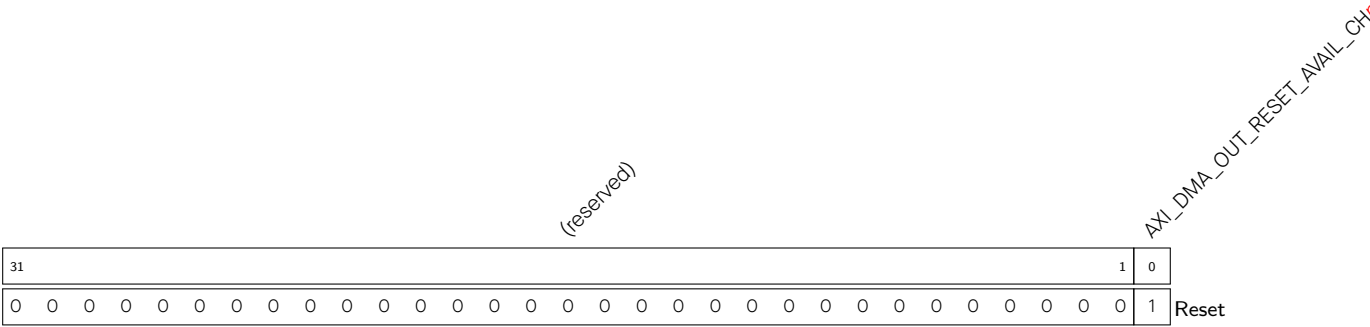
AXI\_DMA\_IN\_RESET\_AVAIL\_CH $n$  Represents whether RX channel  $n$  can be reset.

0: Cannot be reset by software

1: Can be reset

(RO)

Register 3.107. AXI\_DMA\_OUT\_RESET\_AVAIL\_CH $n$ \_REG ( $n$ : 0-2) (0x0298+0x4\* $n$ )



AXI\_DMA\_OUT\_RESET\_AVAIL\_CH $n$  Represents whether TX channel  $n$  can be reset.

0: Cannot be reset by software

1: Can be reset

. (RO)



Register 3.108. AXI\_DMA\_MISC\_CONF\_REG (0x02A8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AXI_DMA_CLK_EN<br>AXI_DMA_ARB_PRI_DIS<br>(reserved)<br>AXI_DMA_AXIM_RST_RD_INTER<br>AXI_DMA_AXIM_RST_WR_INTER |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 4 | 3 | 2 | 1 | 0   | Reset |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0     | 0 | 0 | 0 | 0 |

**AXI\_DMA\_AXIM\_RST\_WR\_INTER** Write 1 and then 0 to reset the internal AXI write FSM. (R/W)

**AXI\_DMA\_AXIM\_RST\_RD\_INTER** Write 1 and then 0 to reset the internal AXI read FSM. (R/W)

**AXI\_DMA\_ARB\_PRI\_DIS** Configures whether to disable the priority arbitration.

0: Enable

1: Disable

(R/W)

**AXI\_DMA\_CLK\_EN** Configures AXI DMA clock gating.

0: Support clock only when the application writes registers.

1: Always force the clock on for registers.

(R/W)

**Register 3.109. AXI\_DMA\_INFIFO\_STATUS\_CH<sub>n</sub>\_REG (*n*: 0-2) (0x0018+0x68\**n*)**

|  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|
| AXI_DMA_IN_BUF_HUNGRY_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L2_OVF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_CNT_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_EMPTY_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_8B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L2_UDF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_OVF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_FULL_CH <sub>n</sub>  |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_7B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L2_EMPTY_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L1_OVF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L1_FULL_CH <sub>n</sub>  |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_6B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L1_UDF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L1_EMPTY_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_OVF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_5B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_FULL_CH <sub>n</sub>  |  |  |  |  |  |  |  |  |  | AXI_DMA_INFIFO_L3_UDF_CH <sub>n</sub>   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_4B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_3B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_2B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_IN_REMAIN_UNDER_1B_CH <sub>n</sub> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| (reserved)                                 |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L2_OVF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L2_UDF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L2_EMPTY_CH <sub>n</sub>    |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L1_OVF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L1_UDF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L1_EMPTY_CH <sub>n</sub>    |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_OVF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_FULL_CH <sub>n</sub>     |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_UDF_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_CNT_CH <sub>n</sub>      |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_EMPTY_CH <sub>n</sub>    |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| AXI_DMA_INFIFO_L3_FULL_CH <sub>n</sub>     |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |

|    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |   |   |   |   |       |  |   |   |   |
|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|---|---|---|---|-------|--|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 |   |   |   |   |   |   |   |   |   |   | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 |   |       |  | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0  | 0  | 1  | 0  | 0  | 0  | 0  |    |    | 1 |   |   | 1 | Reset |  |   |   |   |

Reset

**AXI\_DMA\_INFIFO\_L3\_FULL\_CH<sub>n</sub>** Represents whether L3 RX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_INFIFO\_L3\_EMPTY\_CH<sub>n</sub>** Represents whether L3 RX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_INFIFO\_L3\_CNT\_CH<sub>n</sub>** Represents the number of data bytes in L3 RX FIFO for RX channel ***n***. (RO)**AXI\_DMA\_INFIFO\_L3\_UDF\_CH<sub>n</sub>** Represents whether L3 RX FIFO underflows.

0: No underflow

1: Underflow

(RO)

**AXI\_DMA\_INFIFO\_L3\_OVF\_CH<sub>n</sub>** Represents whether L3 RX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_INFIFO\_L1\_FULL\_CH<sub>n</sub>** Represents whether L1 RX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_INFIFO\_L1\_EMPTY\_CH<sub>n</sub>** Represents whether L1 RX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_INFIFO\_L1\_UDF\_CH<sub>n</sub>** Represents whether L1 RX FIFO underflows.

0: No underflow

1: Underflow

(RO)

Continued on the next page...

**Register 3.109. AXI\_DMA\_INFIFO\_STATUS\_CH $n$ \_REG ( $n$ : 0-2) (0x0018+0x68\* $n$ )**

Continued from the previous page...

**AXI\_DMA\_INFIFO\_L1\_OVF\_CH $n$**  Represents whether L1 RX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_INFIFO\_L2\_FULL\_CH $n$**  Represents whether L2 RX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_INFIFO\_L2\_EMPTY\_CH $n$**  Represents whether L1 RX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_INFIFO\_L2\_UDF\_CH $n$**  Represents whether L2 RX FIFO underflows.

0: No underflow

1: Underflow

(RO)

**AXI\_DMA\_INFIFO\_L2\_OVF\_CH $n$**  Represents whether L2 RX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_1B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_2B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_3B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_4B\_CH $n$**  Reserved.(RO)

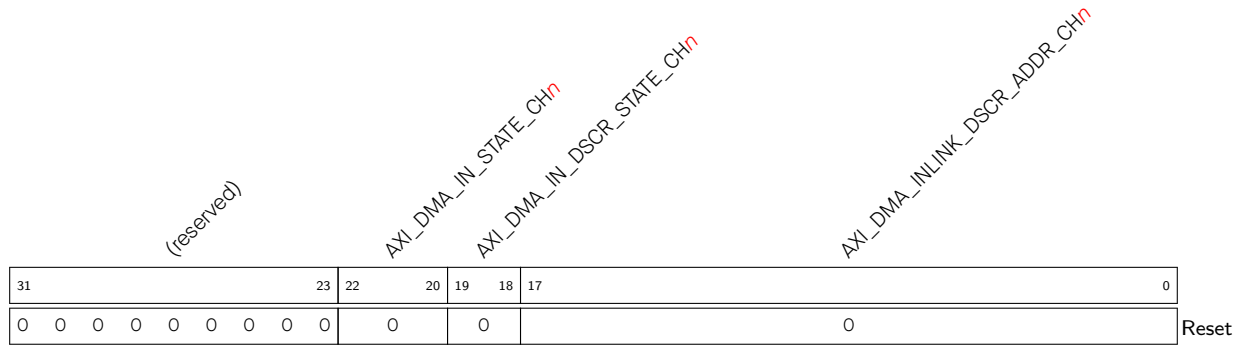
**AXI\_DMA\_IN\_REMAIN\_UNDER\_5B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_6B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_7B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_IN\_REMAIN\_UNDER\_8B\_CH $n$**  Reserved.(RO)

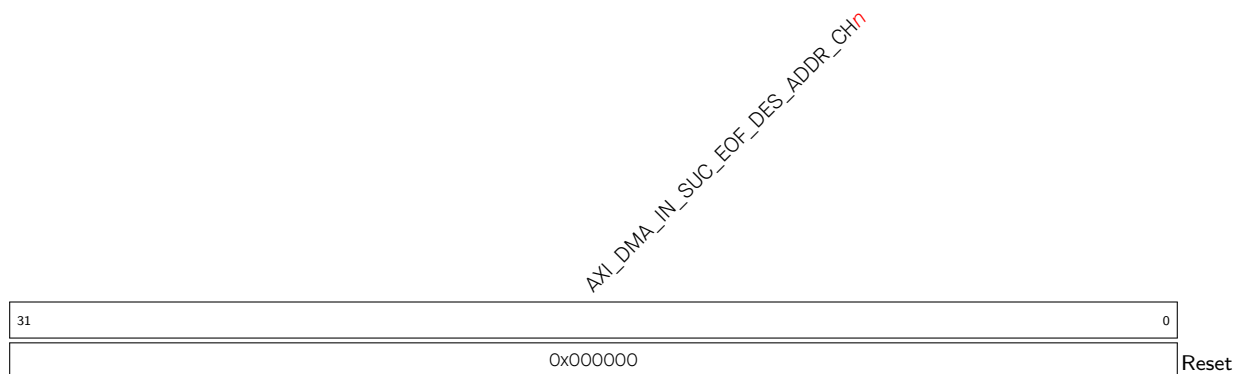
**AXI\_DMA\_IN\_BUF\_HUNGRY\_CH $n$**  Reserved.(RO)

**Register 3.110. AXI\_DMA\_IN\_STATE\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0028+0x68\**n*)**

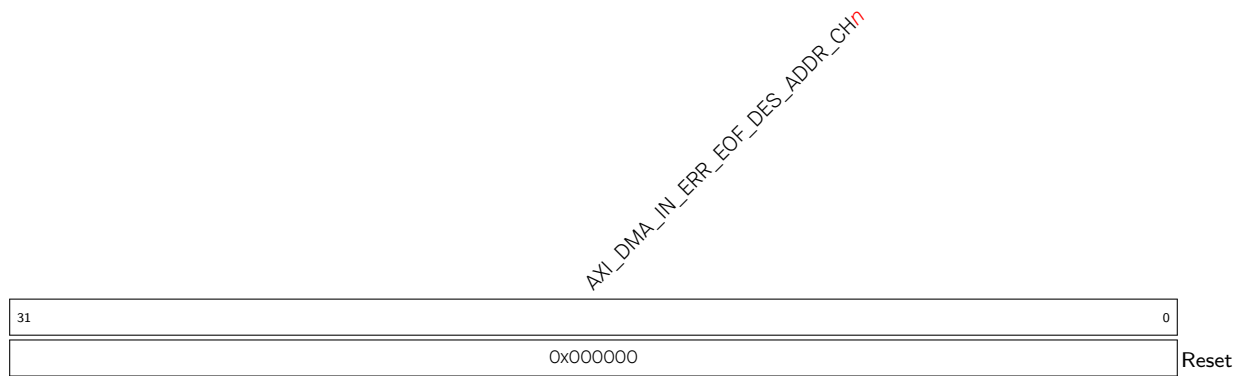
**AXI\_DMA\_INLINK\_DSCR\_ADDR\_CH<sub>*n*</sub>** Represents the lower 18 bits of the next receive descriptor address that is pre-read (but not processed yet). If the current receive descriptor is the last descriptor, then this field represents the address of the current receive descriptor. (RO)

**AXI\_DMA\_IN\_DSCR\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

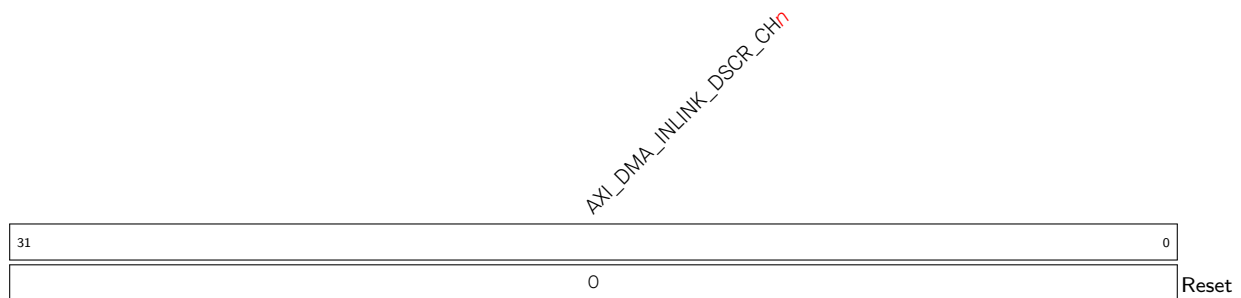
**AXI\_DMA\_IN\_STATE\_CH<sub>*n*</sub>** Reserved. (RO)

**Register 3.111. AXI\_DMA\_IN\_SUC\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x002C+0x68\**n*)**

**AXI\_DMA\_IN\_SUC\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>** Represents the address of the receive descriptor when the EOF bit in this descriptor is 1. (RO)

**Register 3.112. AXI\_DMA\_IN\_ERR\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0030+0x68\**n*)**

**AXI\_DMA\_IN\_ERR\_EOF\_DES\_ADDR\_CH<sub>*n*</sub>** Represents the address of the receive descriptor when there are some errors in the currently received data. Valid only for UHCI. (RO)

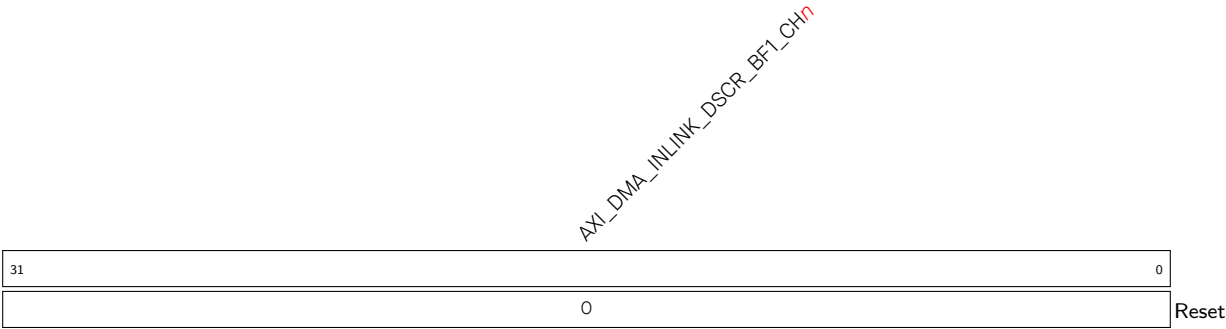
**Register 3.113. AXI\_DMA\_IN\_DSCR\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0034+0x68\**n*)**

**AXI\_DMA\_INLINK\_DSCR\_CH<sub>*n*</sub>** Represents the address of the next receive descriptor x+1 pointed by the current receive descriptor that is pre-read. (RO)

**Register 3.114. AXI\_DMA\_IN\_DSCR\_BFO\_CH<sub>*n*</sub>\_REG (*n*: 0-2) (0x0038+0x68\**n*)**

**AXI\_DMA\_INLINK\_DSCR\_BFO\_CH<sub>*n*</sub>** Represents the address of the current receive descriptor x that is pre-read. (RO)

Register 3.115. AXI\_DMA\_IN\_DSCR\_BF1\_CHn\_REG (n: 0-2) (0x003C+0x68\*n)



AXI\_DMA\_INLINK\_DSCR\_BF1\_CHn Represents the address of the previous receive descriptor x-1 that is pre-read. (RO)

**Register 3.116. AXI\_DMA\_OUTFIFO\_STATUS\_CH<sub>n</sub>\_REG (*n*: 0-2) (0x0150+0x68\**n*)**

|            |    |    |    |    |    |    |    |    |    |            |   |    |    |    |    |    |    |    |    |  |   |   |   |   |  |   |   |       |  |   |  |  |  |  |  |  |  |  |  |
|------------|----|----|----|----|----|----|----|----|----|------------|---|----|----|----|----|----|----|----|----|--|---|---|---|---|--|---|---|-------|--|---|--|--|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |    |    |    |    |    | (reserved) |   |    |    |    |    |    |    |    |    | AXI_DMA_OUTFIFO_L2_OVF_CHn<br>AXI_DMA_OUTFIFO_L2_UDF_CHn<br>AXI_DMA_OUTFIFO_L2_EMPTY_CHn<br>AXI_DMA_OUTFIFO_L1_FULL_CHn<br>AXI_DMA_OUTFIFO_L1_OVF_CHn<br>AXI_DMA_OUTFIFO_L1_UDF_CHn<br>AXI_DMA_OUTFIFO_L1_EMPTY_CHn<br>AXI_DMA_OUTFIFO_L3_FULL_CHn<br>AXI_DMA_OUTFIFO_L3_OVF_CHn<br>AXI_DMA_OUTFIFO_L3_UDF_CHn |   |   |   |   |  |   |   |       |  | AXI_DMA_OUTFIFO_L3_CNT_CHn<br>AXI_DMA_OUTFIFO_L3_EMPTY_CHn<br>AXI_DMA_OUTFIFO_L3_FULL_CHn |  |  |  |  |  |  |  |  |  |
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 |            |   | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10   | 9 | 8 | 7 |   |  | 2 | 1 | 0     |  |   |  |  |  |  |  |  |  |  |  |
| 0          | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0          | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0 | 0 | 0 | 0 |  | 1 | 0 | Reset |  |   |  |  |  |  |  |  |  |  |  |

**AXI\_DMA\_OUTFIFO\_L3\_FULL\_CH<sub>n</sub>** Represents whether L3 TX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_OUTFIFO\_L3\_EMPTY\_CH<sub>n</sub>** Represents whether L3 TX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_OUTFIFO\_L3\_CNT\_CH<sub>n</sub>** Represents the number of data bytes in L3 TX FIFO for TX channel *n*. (RO)

**AXI\_DMA\_OUTFIFO\_L3\_UDF\_CH<sub>n</sub>** Represents whether L3 TX FIFO underflows.

0: No underflow

1: Underflow

(RO)

**AXI\_DMA\_OUTFIFO\_L3\_OVF\_CH<sub>n</sub>** Represents whether L3 TX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_OUTFIFO\_L1\_FULL\_CH<sub>n</sub>** Represents whether L1 TX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_OUTFIFO\_L1\_EMPTY\_CH<sub>n</sub>** Represents whether L1 TX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_OUTFIFO\_L1\_UDF\_CH<sub>n</sub>** Represents whether L1 TX FIFO underflows.

0: No underflow

1: Underflow

(RO)

Continued on the next page...

**Register 3.116. AXI\_DMA\_OUTFIFO\_STATUS\_CH $n$ \_REG ( $n$ : 0-2) (0x0150+0x68\* $n$ )**

Continued from the previous page...

**AXI\_DMA\_OUTFIFO\_L1\_OVF\_CH $n$**  Represents whether L1 TX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_OUTFIFO\_L2\_FULL\_CH $n$**  Represents whether L2 TX FIFO is full.

0: Not Full

1: Full

(RO)

**AXI\_DMA\_OUTFIFO\_L2\_EMPTY\_CH $n$**  Represents whether L2 TX FIFO is empty.

0: Not empty

1: Empty

(RO)

**AXI\_DMA\_OUTFIFO\_L2\_UDF\_CH $n$**  Represents whether L2 TX FIFO underflows.

0: No underflow

1: Underflow

(RO)

**AXI\_DMA\_OUTFIFO\_L2\_OVF\_CH $n$**  Represents whether L2 TX FIFO overflows.

0: No overflow

1: Overflow

(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_1B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_2B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_3B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_4B\_CH $n$**  Reserved.(RO)

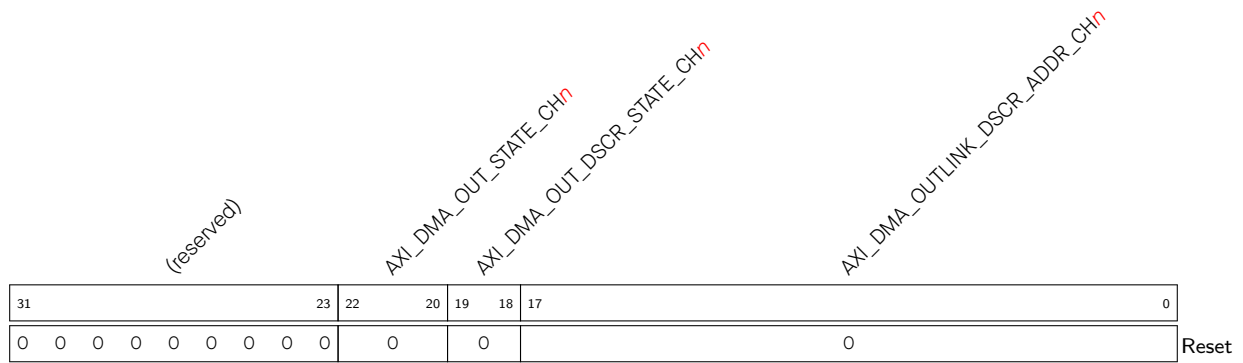
**AXI\_DMA\_OUT\_REMAIN\_UNDER\_5B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_6B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_7B\_CH $n$**  Reserved.(RO)

**AXI\_DMA\_OUT\_REMAIN\_UNDER\_8B\_CH $n$**  Reserved.(RO)

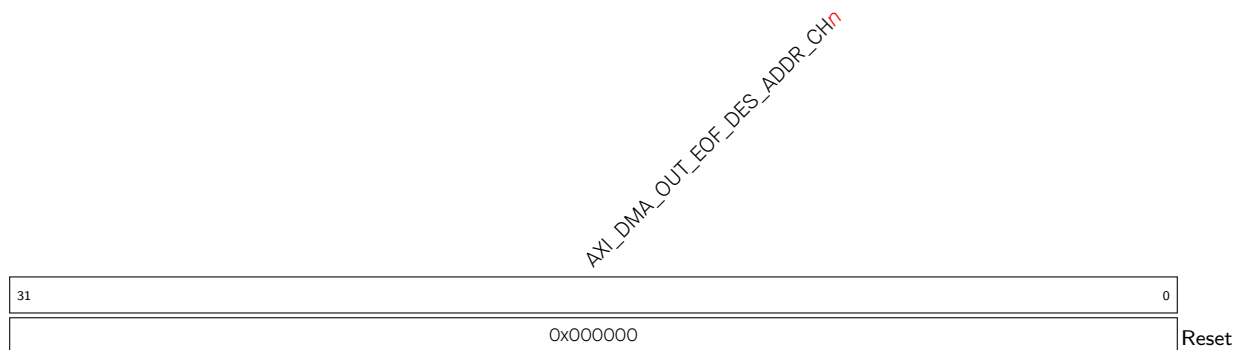


**Register 3.117. AXI\_DMA\_OUT\_STATE\_CH $n$ \_REG ( $n$ : 0-2) (0x0160+0x68\* $n$ )**

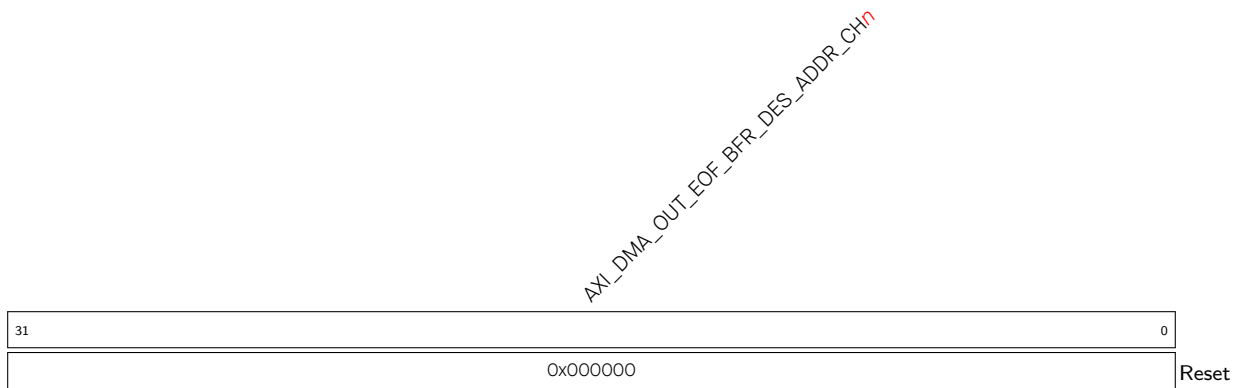
**AXI\_DMA\_OUTLINK\_DSCR\_ADDR\_CH $n$**  Represents the lower 18 bits of the next transmit descriptor address that is pre-read (but not processed yet). If the current transmit descriptor is the last descriptor, then this field represents the address of the current transmit descriptor. (RO)

**AXI\_DMA\_OUT\_DSCR\_STATE\_CH $n$**  Reserved. (RO)

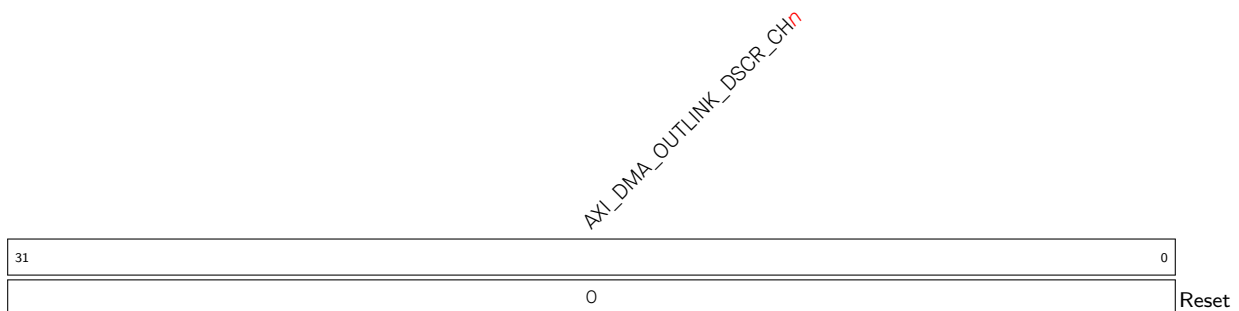
**AXI\_DMA\_OUT\_STATE\_CH $n$**  Reserved. (RO)

**Register 3.118. AXI\_DMA\_OUT\_EOF\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0164+0x68\* $n$ )**

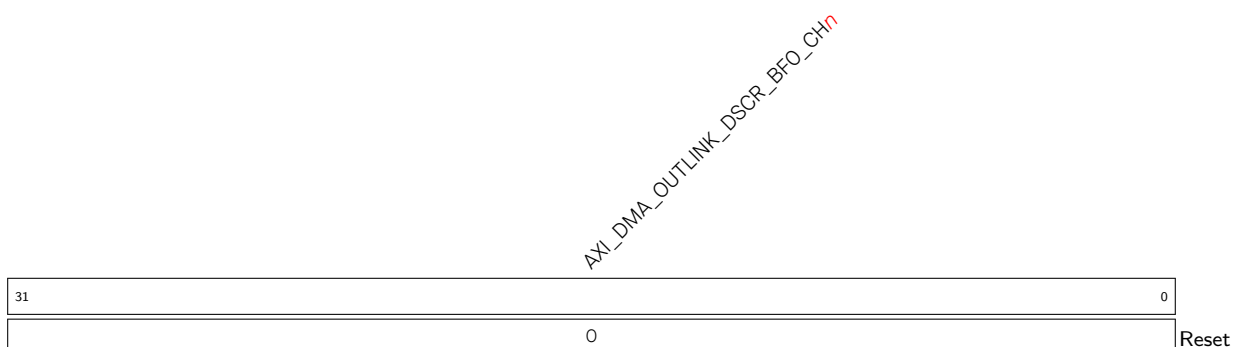
**AXI\_DMA\_OUT\_EOF\_DES\_ADDR\_CH $n$**  Represents the address of the transmit descriptor when the EOF bit in this descriptor is 1. (RO)

**Register 3.119. AXI\_DMA\_OUT\_EOF\_BFR\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0168+0x68\* $n$ )**

**AXI\_DMA\_OUT\_EOF\_BFR\_DES\_ADDR\_CH $n$**  Represents the address of the transmit descriptor before the last transmit descriptor. (RO)

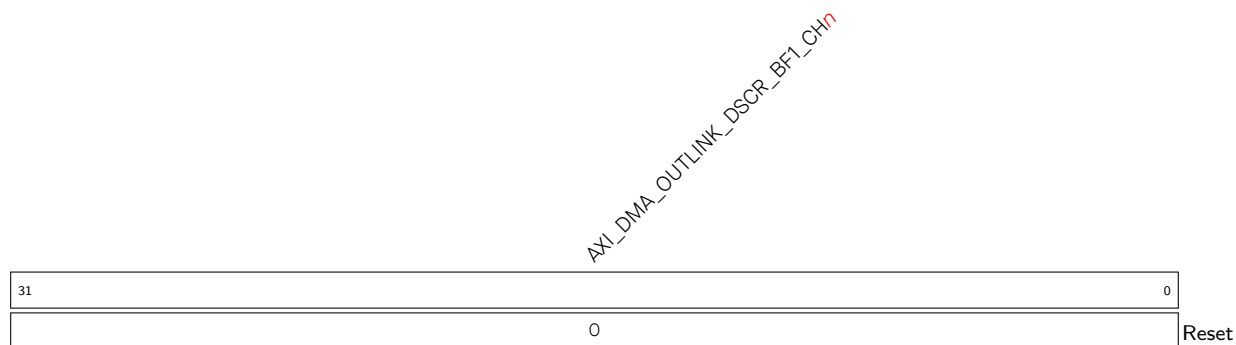
**Register 3.120. AXI\_DMA\_OUT\_DSCR\_CH $n$ \_REG ( $n$ : 0-2) (0x016C+0x68\* $n$ )**

**AXI\_DMA\_OUTLINK\_DSCR\_CH $n$**  Represents the address of the next transmit descriptor  $y+1$  pointed by the current transmit descriptor that is pre-read. (RO)

**Register 3.121. AXI\_DMA\_OUT\_DSCR\_BFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0170+0x68\* $n$ )**

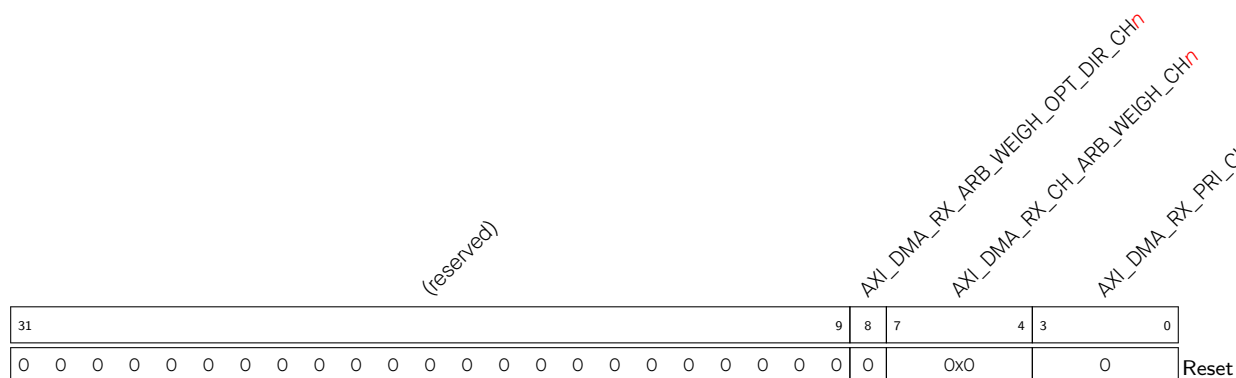
**AXI\_DMA\_OUTLINK\_DSCR\_BFO\_CH $n$**  Represents the address of the current transmit descriptor  $y$  that is pre-read. (RO)

Register 3.122. AXI\_DMA\_OUT\_DSCR\_BF1\_CH $n$ \_REG ( $n$ : 0-2) (0x0174+0x68\* $n$ )



**AXI\_DMA\_OUTLINK\_DSCR\_BF1\_CH<sub>n</sub>** Represents the address of the previous transmit descriptor y-1 that is pre-read. (RO)

**Register 3.123. AXI\_DMA\_IN\_PRI\_CH $n$ \_REG ( $n$ : 0-2) (0x0040+0x68\* $n$ )**



**AXI\_DMA\_RX\_PRI\_CH $n$**  Configures the priority of RX channel  $n$ . The larger the value, the higher the priority.

Value range: 0 ~ 5. (R/W)

**AXI\_DMA\_RX\_CH\_ARB\_WEIGHT\_CH***n* Configures the weight (i.e the number of tokens) of RX channel *n*.

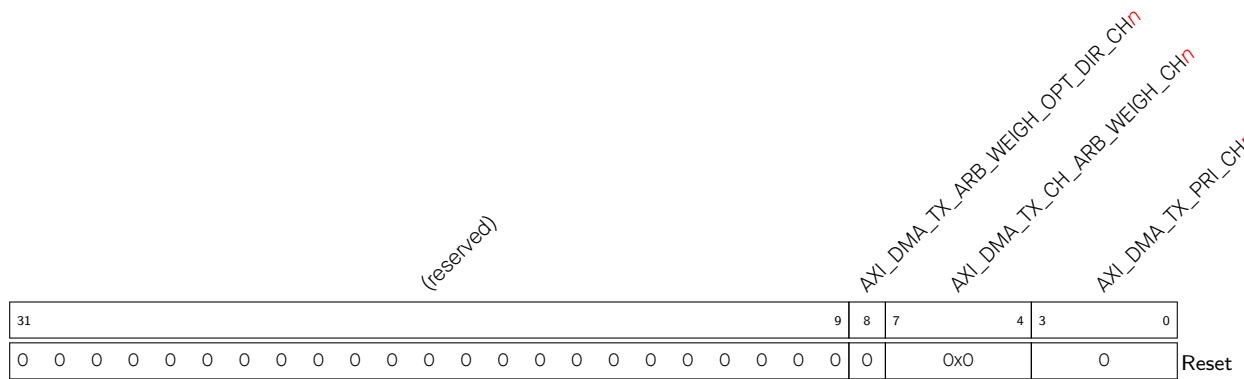
Value range: 0 ~ 15. (R/W)

**AXI\_DMA\_RX\_ARB\_WEIGHT\_OPT\_DIR\_CH $n$**  Configures whether to enable weight optimization for RX channel  $n$ .

0: Enable

1: Disable

(R/W)

Register 3.124. AXI\_DMA\_OUT\_PRI\_CH $n$ \_REG ( $n$ : 0-2) (0x0178+0x68\* $n$ )

**AXI\_DMA\_TX\_PRI\_CH $n$**  Configures the priority of RX channel  $n$ . The larger the value, the higher the priority.

Value range: 0 ~ 5. (R/W)

**AXI\_DMA\_TX\_CH\_ARB\_WEIGHT\_CH $n$**  Configures the weight (i.e the number of tokens) of TX channel  $n$ .

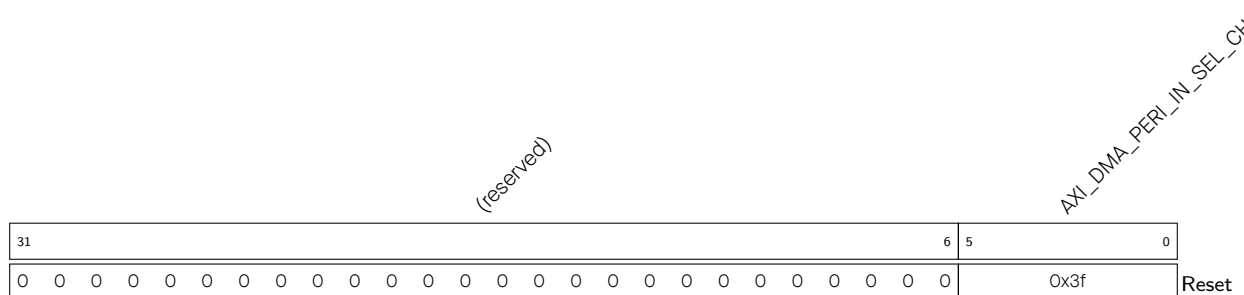
Value range: 0 ~ 15. (R/W)

**AXI\_DMA\_TX\_ARB\_WEIGHT\_OPT\_DIR\_CH $n$**  Configures whether to enable weight optimization for RX channel  $n$ .

0: Enable

1: Disable

(R/W)

Register 3.125. AXI\_DMA\_IN\_PERI\_SEL\_CH $n$ \_REG ( $n$ : 0-2) (0x0044+0x68\* $n$ )

**AXI\_DMA\_PERI\_IN\_SEL\_CH $n$**  Configures the peripheral connected to RX channel  $n$ .

0: LCD\_CAM

1: SPI2

2: SPI3

3: PARLIO

4: AES

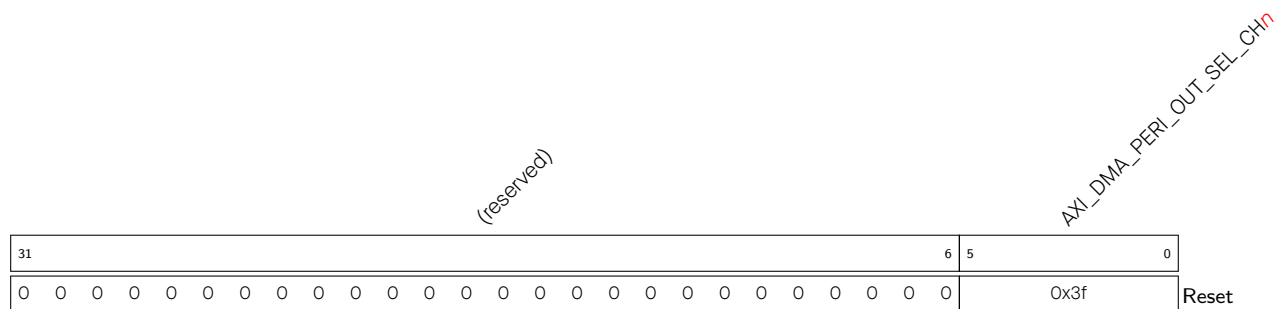
5: SHA

6 ~ 15: Dummy-6 ~ Dummy-15

16 ~ 63: Invalid

(R/W)

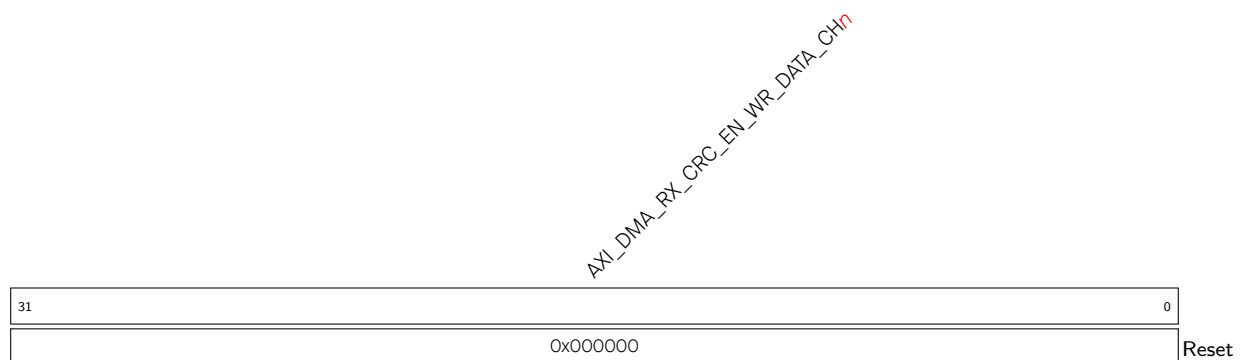
Register 3.126. AXI\_DMA\_OUT\_PERI\_SEL\_CH*n*\_REG (*n*: 0-2) (0x017C+0x68\**n*)



**AXI\_DMA\_PERI\_OUT\_SEL\_CH $n$**  Configures the peripheral connected to TX channel  $n$ .

- 0: LCD\_CAM  
1: SPI2  
2: SPI3  
3: PARLIO  
4: AES  
5: SHA  
6 ~ 15: Dummy-6 ~ Dummy-15  
16 ~ 63: Invalid  
(R/W)

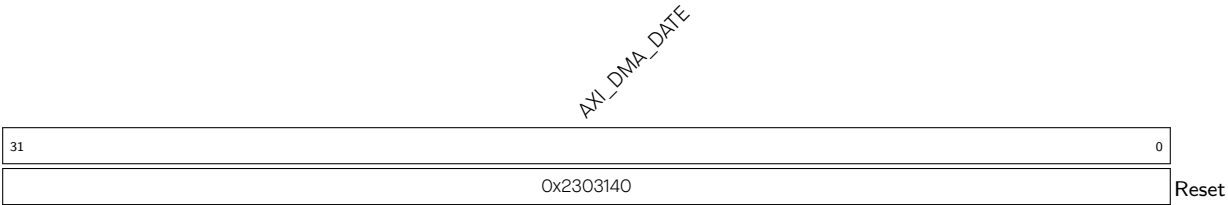
Register 3.127. AXI\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$ \_REG ( $n$ : 0-2) (0x0058+0x68\* $n$ )



**AXI\_DMA\_RX\_CRC\_EN\_WR\_DATA\_CH $n$**  Configures whether to include each bit of the intermediate result in the CRC calculation matrix for RX channel  $n$ .

- 0: Not include  
1: Include  
(R/W)

Register 3.128. AXI\_DMA\_DATE\_REG (0x02D8)



AXI\_DMA\_DATE Version control register. (R/W)

## Chapter 4

# VDMA Controller (VDMA)

## 4.1 Overview

DMA (Direct Memory Access) enables direct access to system memory or peripherals without CPU involvement. The VDMA controller on ESP32-P4 is a general-purpose DMA that performs high-speed data transfer from memory to memory, from memory to peripheral, and from peripheral to memory. The VDMA complies with the AXI3 protocol and includes two AXI master interfaces. This design allows users to select between the two interfaces for data transfer dynamically.

## 4.2 Terminology

The following terms are defined in the context of the VDMA controller on ESP32-P4:

- **AXI:** Advanced eXtensible Interface, a part of AMBA 3 (Advanced Microcontroller Bus Architecture) specification, designed to facilitate high bandwidth and low latency communication between memory and peripheral, and between memory and memory.
- **Peripheral:** A system component that has a handshake interface with VDMA, as listed in Table 4.4-1.
- **Memory:** A system component that is always ready for DMA transfer, which means there is no handshaking interface between VDMA and memory. The memory that supports VDMA data transfer includes HP L2MEM, external flash, and external RAM.
- **Source:** Source memory or peripheral from which VDMA reads data via the AXI interface. VDMA then stores data in channel FIFO.
- **Source transfer:** Transfer from the source to VDMA.
- **Destination:** Destination peripheral or memory to which VDMA writes the data stored in channel FIFO.
- **Destination transfer:** Transfer from VDMA to the destination.
- **Channel:** Data path between source and destination.
- **Master interface:** Refers to the two AXI master interfaces of VDMA.
- **Slave interface:** The APB3 slave interface for programming registers.
- **Handshaking interface:** The handshaking interface performs a handshake between VDMA and the source or destination peripheral. The handshaking interface requests, acknowledges, and controls an VDMA transfer.
- **Flow controller:** The flow controller defines the length of a DMA block transfer and terminates the transfer. The flow controller can be VDMA, a source peripheral, or a destination peripheral, but it cannot be memory.

## 4.3 Features

VDMA supports the following features:

- Four channels for unidirectional data transfer from source to destination
- Two AXI master interfaces
- Handshake with MIPI DSI (Display Serial Interface) and ISP (Image Signal Processor)
- Memory-to-memory, ISP-to-memory, and MIPI DSI-to-memory transfer types
- Multiple levels of DMA transfer hierarchy
- Configurable transfer type, transfer length, and transfer size for each channel
- Single-block transfer
- Multi-block transfer based on contiguous address, automatic reloading register configuration, shadow registers, and linked lists
- Independent configuration of multi-block transfer type for source transfer and destination transfer
- Channel disabling without data loss
- Channel suspension, resume, and abortion
- Configurable priorities among arbitration channels
- Flow control using VDMA or peripherals
- Programmable mapping between peripherals and channels

## 4.4 Architectural Overview

Figure [4.4-1](#) shows the architecture of VDMA and its connection with other system components.



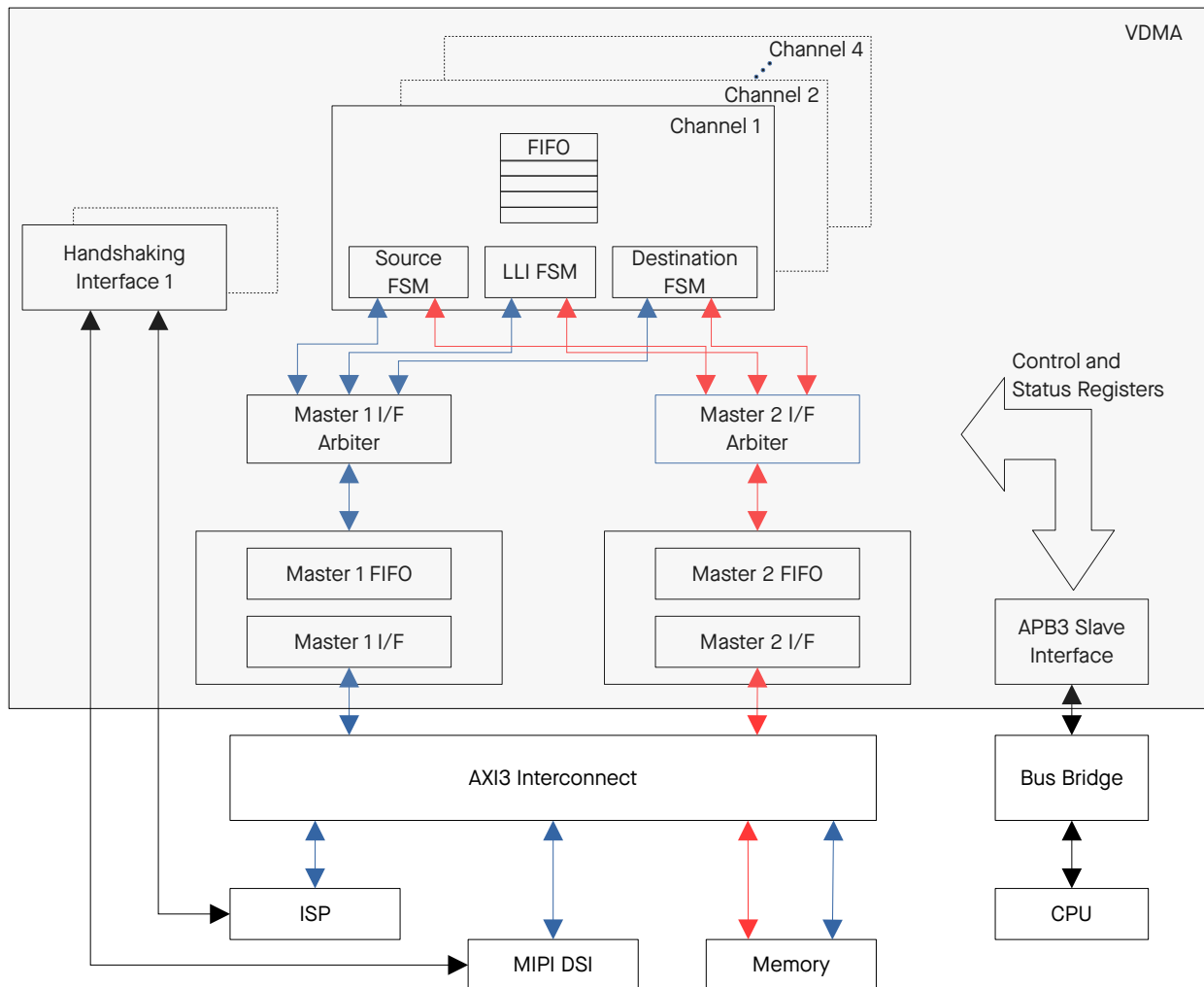


Figure 4.4-1. VDMA Architecture

It can be seen from the figure that:

- The CPU accesses VDMA registers via the APB3 slave interface.
- VDMA has four channels (Channel 1 to Channel 4). Each channel has a data FIFO with a depth of 64 and a width of 64 bits.
- VDMA has two AXI master interfaces (Master 1 and Master 2).
  - Master 1 can access ISP, MIPI DSI, and memory, as blue arrows indicate.
  - Master 2 can only access memory, as red arrows indicate.
  - Master 1 and Master 2 each have an arbiter that arbitrates read and write requests on all channels.
- VDMA has three hardware handshaking interfaces. Table 4.4-1 shows the mapping between the handshaking interfaces and peripherals.

Table 4.4-1. Hardware Handshaking Interface and Peripherals Mapping Table

| Handshaking Interface Number | Peripheral |
|------------------------------|------------|
| 0                            | MIPI DSI   |

|   |                     |
|---|---------------------|
| 1 | ISP (ISP-to-memory) |
| 2 | ISP (memory-to-ISP) |

For more information about ISP and MIPI DSI, please refer to Chapter [32 Image Signal Processor \(ISP\)](#) and Chapter [5 MIPI DSI \[to be added later\]](#).

## 4.5 Functional Description

This section provides a detailed description of the key features and operations of the module.

### 4.5.1 Transfer Hierarchy

Transfers are organized into a maximum of four levels: DMA transfer level, block transfer level, transaction level, and AXI transfer level.

Figure [4.5-1](#) shows four transfer levels between VDMA and peripherals.

Figure [4.5-2](#) shows three transfer levels between VDMA and memory. There is no transaction level because memory is assumed to be always ready for data transfer.

The following descriptions of DMA, block, and AXI transfers apply to the transfer between VDMA and memory, VDMA and peripherals. **The description of the transaction level applies only to transfers between VDMA and peripherals.**

- **DMA transfer:** Software defines the number of blocks in a DMA transfer. Once a DMA transfer has finished, VDMA disables the channel and generates an interrupt. The channel can then be reprogrammed for a new DMA transfer. A DMA transfer can consist of either a single-block or a multi-block transfer.
- **Block transfer:** A block transfer moves a specified data block through the VDMA. The flow controller controls the block length. There are two types of block transfer: single-block transfer and multi-block transfer. As shown in Figure [4.5-1](#), a block transfer may consist of multiple transactions.
- **Transaction:** A peripheral request may trigger either a single or burst transaction, corresponding to an AXI single transfer or multiple AXI burst transfers, respectively.
  - Single transaction: The length of a single transaction is always 1, in the unit of `DMAC_CHn_SRC_TR_WIDTH`.
  - Burst transaction: The length of a burst transaction is programmed into the VDMA through `DMAC_CHn_SRC_MSIZE` for the source or `DMAC_CHn_DST_MSIZE` for the destination. The burst length typically relates to the FIFO sizes in the source or destination peripherals. For more information, please refer to the chapter on each peripheral.
- **AXI transfer:** Refers to the AXI protocol transfer, which is divided into AXI single transfer and AXI burst transfer.

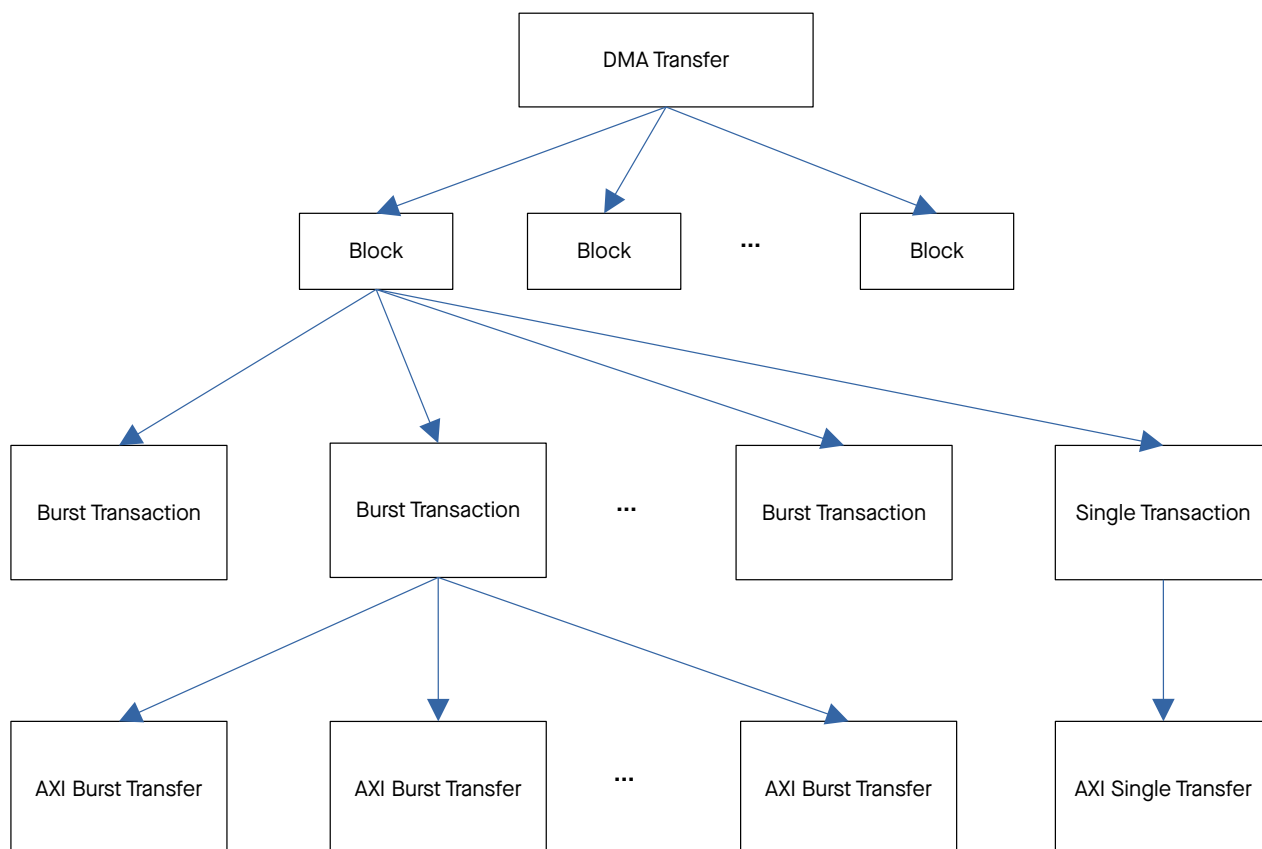


Figure 4.5-1. VDMA Transfer Hierarchy for Peripherals

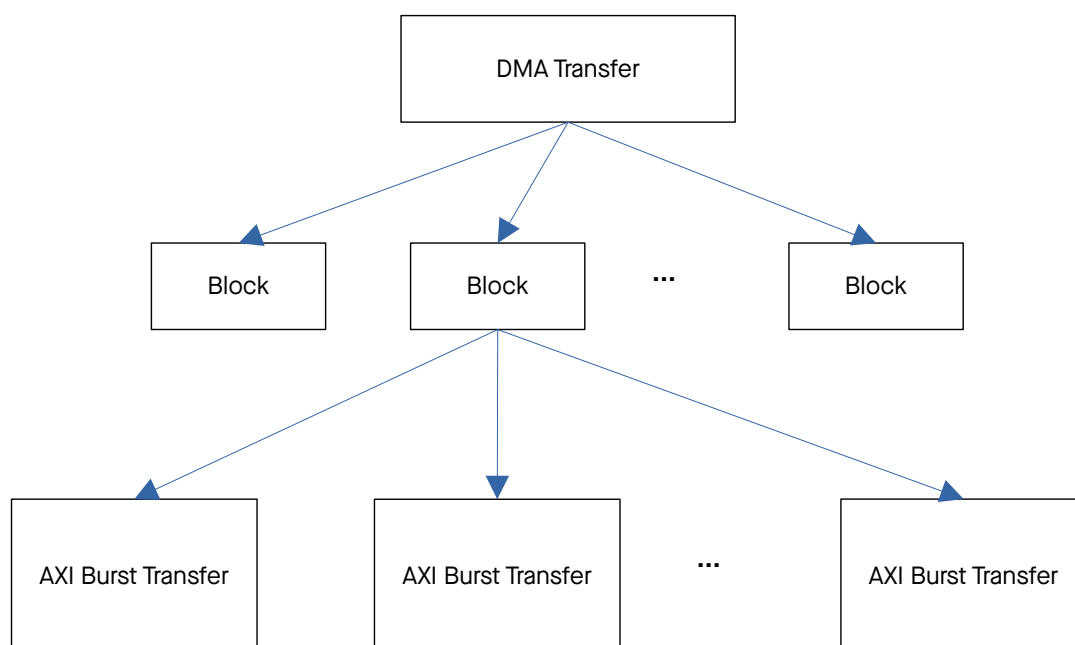


Figure 4.5-2. VDMA Transfer Hierarchy for Memory

## 4.5.2 Arbitration Scheme

The arbitration mechanism arbitrates read and write requests for all channels.

VDMA uses a priority and fair-among-equals arbitration mechanism. The priority for each channel is defined in the channel configuration register `DMAC_CH $n$ _CFG1_REG`.

A priority of 3 is the highest, while 0 is the lowest. Multiple channels can share the same priority level.

The arbitration mechanism works as follows:

- The arbitration mechanism determines which request client to grant the authorization signal based on the priority of the request. The request with the highest priority will be granted access to the channel.
- When two or more requests have the same priority, request clients will gain access randomly.

### 4.5.2.1 Read Arbiter

The read arbiter arbitrates read requests, including:

- VDMA's read requests to obtain data or status from the source
- VDMA's read requests to obtain status from the destination
- VDMA's read requests to obtain LLI descriptors

The block diagram of the read arbiter is shown in Figure 4.5-3:

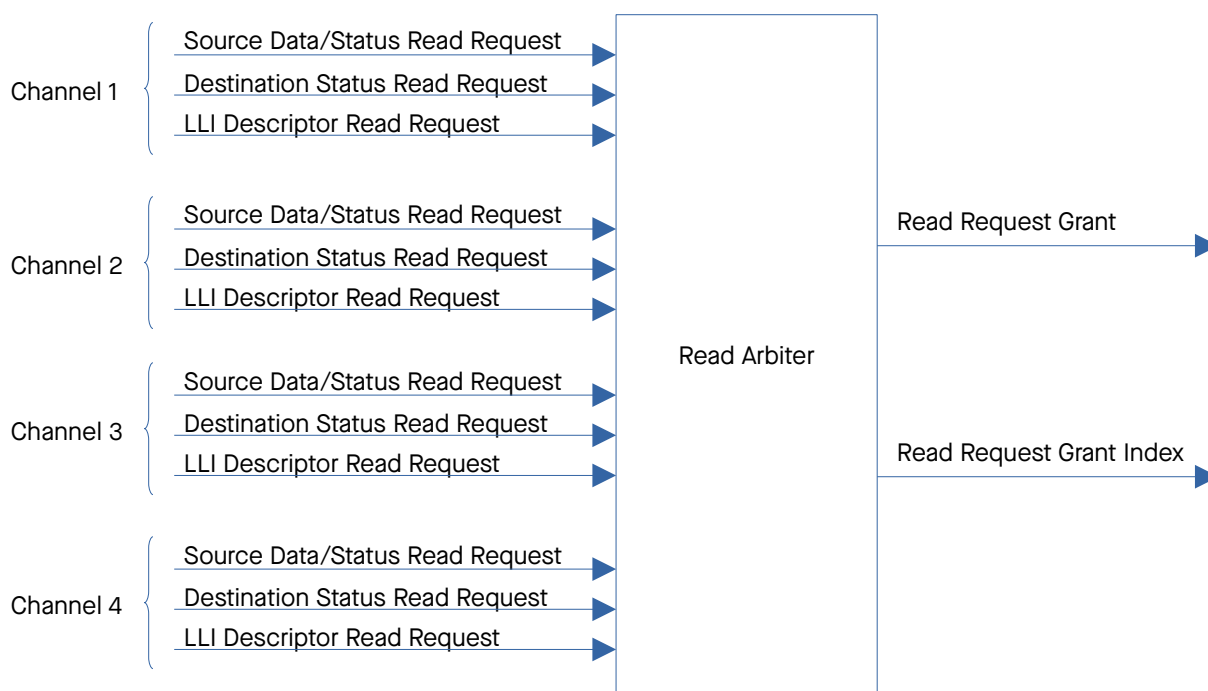


Figure 4.5-3. VDMA Read Arbiter

Read requests to obtain linked list descriptors will be granted the highest priority, regardless of the channels' priority settings.

### 4.5.2.2 Write Arbiter

The write arbiter arbitrates write requests, including:

- Destination Data Write Request
- LLI Descriptor Write-Back Request

The block diagram of the write arbiter is shown in Figure 4.5-4:

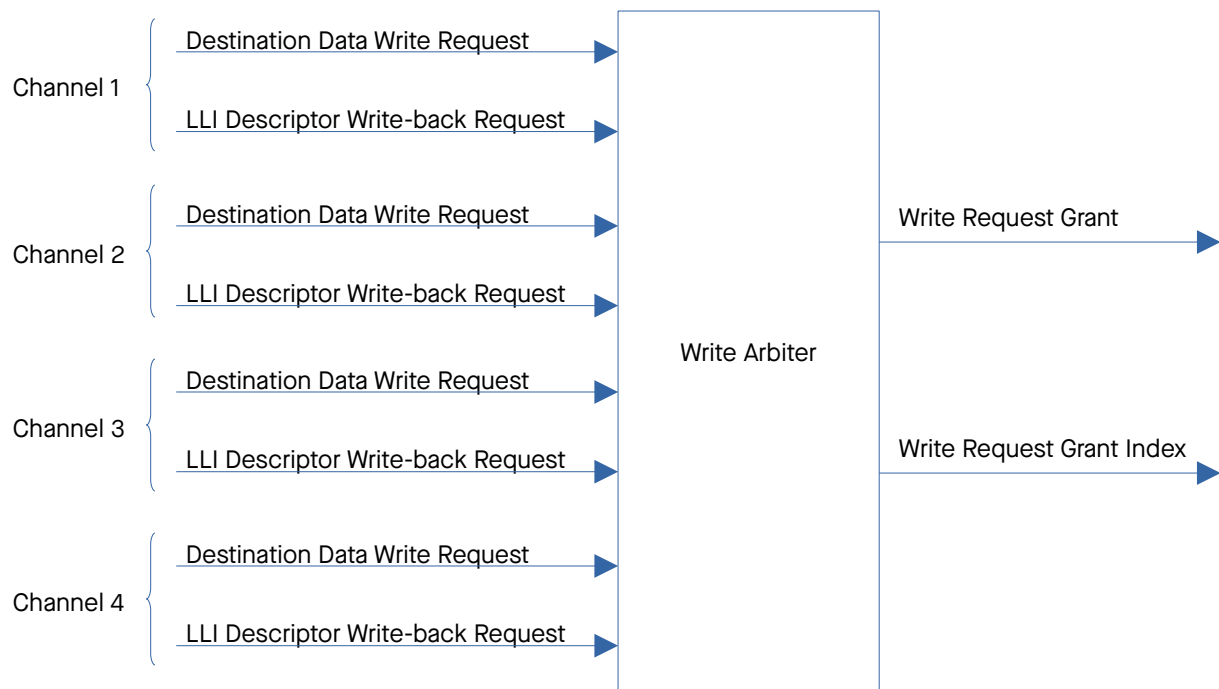


Figure 4.5-4. VDMA Write Arbiter

Within the same channel, Destination Data Write Request has higher priority than LLI Descriptor Write-Back Request. If different channels have the same priority, then Data Write Requests have the highest priority.

### 4.5.3 Handshaking Interface

A peripheral uses a handshaking interface to inform VDMA that it is ready to transmit or receive data via AXI bus. The operation of the handshaking interface depends on whether the flow controller is the peripheral or VDMA.

VDMA performs a single transaction or a burst transaction per handshake. In some cases, a block transfer cannot be completed using only burst transactions. This situation typically occurs when the block size is not a multiple of the burst transaction length. In this case, the block transfer uses burst transactions until the remaining size of the block is less than the amount of data in the burst transaction. At this point, a single transaction is used to complete the block transfer.

A source's burst transaction size is determined by `DMAC_CHn_SRC_MSIZ`. A destination's burst transaction size is determined by `DMAC_CHn_DST_MSIZ`. The transaction size also corresponds to the burst transaction size used for handshaking. The value of `DMAC_CHn_SRC_MSIZ` or `DMAC_CHn_DST_MSIZ` should match the peripheral configuration. For detailed information, please refer to the chapter on related peripherals.

VDMA has three hardware handshaking interfaces with MIPI DSI, ISP (ISP-to-memory), and ISP (memory-to-ISP). For the mapping relationship please see Table 4.4-1.

## 4.5.4 Transfer Control

Transfer control logic facilitates the data transfer from a source to a destination. Data from the source is temporarily stored in the channel FIFO before being sent to the destination. If source and destination peripherals use different transfer sizes, VDMA will pack and unpack the data to fit the FIFO configuration.

For a specific DMA transfer, the transfer type and flow control configurations are determined by `DMAC_CHn_TT_FC`.

### 4.5.4.1 Single-Block Transfer

If a DMA transfer consists of a single block, the software can set `DMAC_CHn_SRC_MULTBLK_TYPE` and `DMAC_CHn_DST_MULTBLK_TYPE` to 0 to enable contiguous-address-based single-block transfer. In this case, VDMA disables the channel once the block transfer of size `DMAC_CHn_BLOCK_TS` is completed.

**Note:**

Single-block transfer is a special case of multi-block transfer, and there is no strict distinction between the two. In this chapter, single-block transfer refers to the transfer consisting of only one block, while multi-block transfer refers to the transfer consisting of at least two blocks.

### 4.5.4.2 Multi-Block Transfer

If a DMA transfer consists of multiple blocks, the software can configure `DMAC_CHn_SRC_MULTBLK_TYPE` and `DMAC_CHn_DST_MULTBLK_TYPE` to choose a multi-block transfer type. There are four types of multi-block transfers, depending on how the transfer control registers (`DMAC_CHn_SARO_REG`, `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO/1_REG`) are updated:

1. **Contiguous address**
2. **Auto reloading:** Register values reload from initial values
3. **Shadow register:** Register values load from shadow registers
4. **Linked list** Register values load from the next linked list (LLI)

Table 4.5-1 lists all the cases of register update methods for multi-block transfer.

Table 4.5-1. Register Update Methods for Multi-Block Transfer

| DMAC_CH $n$ _CFG0_REG         |                               | Registers Update Method   |                           |                                  |                           | Comment                                   |
|-------------------------------|-------------------------------|---------------------------|---------------------------|----------------------------------|---------------------------|---|
| DMAC_CH $n$ _SRC_MULTBLK_TYPE | DMAC_CH $n$ _DST_MULTBLK_TYPE | DMAC_CH $n$ _SARO_REG     | DMAC_CH $n$ _DARO_REG     | DMAC_CH $n$ _CTLO_REG / CTL1_REG | DMAC_CH $n$ _BLOCK_TS     |   |
| 00                            | 00                            | Contiguous address        | Contiguous address        | No update                        | No update                 | Single block or last block of multi-block |
| 00                            | 01                            | Contiguous address        | Reload from initial value | Reload from initial value        | Reload from initial value | -   |
| 00                            | 10                            | Contiguous address        | Load from shadow register | Load from shadow register        | Load from shadow register | -   |
| 01                            | 00                            | Reload from initial value | Contiguous address        | Reload from initial value        | Reload from initial value | -   |
| 01                            | 01                            | Reload from initial value | Reload from initial value | Reload from initial value        | Reload from initial value | -   |
| 01                            | 10                            | Reload from initial value | Load from shadow register | Load from shadow register        | Load from shadow register | -   |
| 10                            | 00                            | Load from shadow register | Contiguous address        | Load from shadow register        | Load from shadow register | -   |
| 10                            | 01                            | Load from shadow register | Reload from initial value | Load from shadow register        | Load from shadow register | -   |
| 10                            | 10                            | Load from shadow register | Load from shadow register | Load from shadow register        | Load from shadow register | -   |
| 00                            | 11                            | Contiguous address        | Load from next LLI        | Load from next LLI               | Load from next LLI        | -   |
| 01                            | 11                            | Reload from initial value | Load from next LLI        | Load from next LLI               | Load from next LLI        | -   |
| 11                            | 00                            | Load from next LLI        | Contiguous address        | Load from next LLI               | Load from next LLI        | -   |
| 11                            | 01                            | Load from next LLI        | Reload from initial value | Load from next LLI               | Load from next LLI        | -   |
| 11                            | 11                            | Load from next LLI        | Load from next LLI        | Load from next LLI               | Load from next LLI        | -   |
| 10                            | 11                            | -                         | -                         | -                                | -                         | Invalid. Interrupt* is generated.         |
| 11                            | 10                            | -                         | -                         | -                                | -                         | Invalid. Interrupt* is generated.         |

\*Note: The interrupt is [DMAC\\_CH \$n\$ \\_SLVIF\\_MULTIBLKTYPE\\_ERR\\_INT](#).

## Contiguous Address

In this scenario, the address for each subsequent block continues from the end of the preceding block. To achieve this contiguity, configure `DMAC_CHn_SRC_MULTBLK_TYPE` or `DMAC_CHn_DST_MULTBLK_TYPE` to 0 for the source address or destination address to remain continuous across the blocks.

In the case of multi-block transfer, the values of `DMAC_CHn_SRC_MULTBLK_TYPE` and `DMAC_CHn_DST_MULTBLK_TYPE` cannot both be selected as contiguous addresses, meaning they cannot both be configured to 0 at the same time. If both are configured to 0 during a multi-block transfer, then the current block will be considered as the last block.

During a multi-block transfer, if `DMAC_CHn_SARO_REG` and `DMAC_CHn_DARO_REG` need to have contiguous addresses between blocks, you can indirectly achieve this functionality using linked-list or shadow-register-based multi-block transfer.

### Note:

If you have enabled contiguous-address-based multi-block transfer (i.e., `DMAC_CHn_SRC_MULTBLK_TYPE` or `DMAC_CHn_DST_MULTBLK_TYPE` is 0), ensure there are at least two blocks in the DMA transfer. Otherwise, it will result in unpredictable behavior.

## Auto Reloading

In this scenario, `DMAC_CHn_SARO_REG` and `DMAC_CHn_DARO_REG` are reloaded with their initial values at the end of each block. VDMA does not proceed to the next block transfer until software clears the corresponding channel's block transfer complete interrupt by writing 1 to `DMAC_CHn_CLEAR_SRC_TRANSCOMP_INTSTAT` and `DMAC_CHn_CLEAR_DST_TRANSCOMP_INTSTAT`.

### Note:

If you have enabled auto-reloading-based multi-block transfer, please ensure there are at least two blocks in the DMA transfer. Otherwise, it will result in unpredictable behavior.

## Shadow Register

In this scenario, `DMAC_CHn_SARO_REG`, `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG` synchronize with their corresponding shadow registers when each block finishes. The values of the shadow registers are then used for the subsequent block.

Software writes the block configurations to the corresponding shadow registers. VDMA copies the shadow register contents to `DMAC_CHn_SARO_REG`, `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG` before starting the subsequent block transfer.

Read operations to the `DMAC_CHn_SARO_REG`, `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG` always return the data corresponding to the current block transfer, not the shadow register contents that correspond to the next block.

`DMAC_CHn_SHADOWREG_OR_LLI_VALID` indicates whether the shadow register contents are valid (1) or not (0). If this bit reads as 0 during a shadow register fetch phase, VDMA discards the shadow register contents and generates a `DMAC_CHn_SHADOWREG_OR_LLI_INVALID_ERR_INT` interrupt. VDMA waits until the software



writes 1 to [DMAC\\_CHn\\_BLK\\_TFR\\_RESUMEREQ](#), indicating that the shadow registers are available. After this, VDMA attempts to read the shadow registers again and continues with the next block transfer.

**Note:**

In a shadow-register-based multi-block transfer, the values in [DMAC\\_CHn\\_SARO\\_REG](#), [DMAC\\_CHn\\_DARO\\_REG](#), [DMAC\\_CHn\\_BLOCK\\_TS](#), [DMAC\\_CHn\\_CTLO\\_REG](#), and [DMAC\\_CHn\\_CTL1\\_REG](#) correspond to the current transfer configurations. When software writes to these registers, it is actually writing to the corresponding shadow registers.

## Linked List

In this scenario, VDMA retrieves a block descriptor for a specific block from memory to update [DMAC\\_CHn\\_SARO\\_REG](#), [DMAC\\_CHn\\_DARO\\_REG](#), [DMAC\\_CHn\\_BLOCK\\_TS](#), [DMAC\\_CHn\\_CTLO\\_REG](#), and [DMAC\\_CHn\\_CTL1\\_REG](#), and then initiates the block transfer. This process is called LLI (Linked List Item) update. The block chaining feature of VDMA uses the linked list pointer register [DMAC\\_CHn\\_LOCO](#) to store the address of the next linked list item in memory, thereby achieving seamless continuity of data transfer.

Figure 4.5-5 shows the VDMA linked list item:

|                          |  |               |
|--------------------------|--|---------------|
| 31                       |  | 0             |
| Reserved                 |  |               |
| Reserved                 |  |               |
| CHn_LL_P_STATUS[63:32]   |  |               |
| CHn_LL_P_STATUS[31:0]    |  |               |
| Write Back for CHn_DSTAT |  |               |
| Write Back for CHn_SSTAT |  |               |
| CHn_CTL1[31:0]           |  |               |
| CHn_CTLO[31:0]           |  |               |
| Reserved                 |  |               |
| CHn_LLPO[31:6]           |  | Reserved[5:0] |
| Reserved                 |  |               |
| CHn_BLOCK_TS[31:0]       |  |               |
| Reserved                 |  |               |
| CHn_DAR[31:0]            |  |               |
| Reserved                 |  |               |
| CHn_SAR[31:0]            |  |               |

**Figure 4.5-5. VDMA Linked List Item (Descriptor)**

VDMA can dynamically extend linked lists, which means you do not need to pre-create the entire linked list in system memory. To enable this feature, set [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) to 1. If the linked list item is the last one, then also configure [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_LAST](#) to 1.

**DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** indicates whether the linked list item fetched from memory is valid (1) or not (0). If the LLI is invalid, VDMA discards the LLI and generates a **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INT** interrupt. This interrupt causes VDMA to halt the corresponding channel and wait until the software writes 1 to **DMAC\_CH $n$ \_BLK\_TFR\_RESUMEREQ** to indicate that the LLI is available. After this, VDMA will attempt to read the LLI again.

**Note:**

For pre-fetched LLIs, if **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** is 0, then the **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INTSTAT** interrupt will not be generated. VDMA re-attempts to fetch the LLI again after completing the current block transfer and generates a **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INTSTAT** interrupt only if **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** still reads as 0.

The following fields in LLI are prepared by software:

- CH $n$ \_SAR: The field definition is the same as **DMAC\_CH $n$ \_SARO\_REG**
- CH $n$ \_DAR: The field definition is the same as **DMAC\_CH $n$ \_DARO\_REG**
- CH $n$ \_BLOCK\_TS: The field definition is the same as **DMAC\_CH $n$ \_BLOCK\_TS**
- CH $n$ \_LLPO[31:6]: The field definition is the same as **DMAC\_CH $n$ \_LLPO\_REG**[31:6]
- CH $n$ \_CTLO: The field definition is the same as **DMAC\_CH $n$ \_CTLO\_REG**
- CH $n$ \_CTL1: The field definition is the same as **DMAC\_CH $n$ \_CTL1\_REG**

If the status write-back option is enabled, VDMA writes back CH $n$ \_CTLO, CH $n$ \_CTL1, CH $n$ \_LLP\_STATUS, CH $n$ \_SSTAT, and CH $n$ \_DSTAT information to the location defined for this field, which is from address [CH $n$ \_LLP] + 0x20 to [CH $n$ \_LLP] + 0x34. The write-back of CH $n$ \_SSTAT and CH $n$ \_DSTAT can be independently enabled or disabled by programming **DMAC\_CH $n$ \_SRC\_STAT\_EN** and **DMAC\_CH $n$ \_DST\_STAT\_EN**.

**Note:**

- If CH $n$ \_SSTAT and CH $n$ \_DSTAT write-back is not enabled, do not use PSRAM to store LLI.
- **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** will be 0 after the LLI write-back operation.

Figure 4.5-6 shows CH $n$ \_LLP\_STATUS write-back field of LLI:

|    |                 |  |                 |   |
|----|-----------------|--|-----------------|---|
| 63 |                 |  |                 | 0   |
| *  | Reserved[61:47] | Data Left in Channel FIFO<br>(CH $n$ _Status[46:32]) | Reserved[31:22] | Completed Block Transfer Size<br>(CH $n$ _Status[21:0]) |

Note: \* denotes Status Indication (CH $n$ \_IntStatus[1:0])

**Figure 4.5-6. CH $n$ \_LLP\_STATUS Write-Back Field of LLI**

CH $n$ \_LLP\_STATUS[63] and CH $n$ \_LLP\_STATUS[62] indicate DMA\_TFR\_DONE and BLOCK\_TFR\_DONE status respectively. These two fields are the last to be updated during LLI write-back. Software should ensure that BLOCK\_TFR\_DONE bit is set to 1 before using CH $n$ \_SSTAT and CH $n$ \_DSTAT information. DMA\_TFR\_DONE and BLOCK\_TFR\_DONE bits will be set to 1 after transferring the last block.

CH $n$ \_STATUS[21:0] corresponds to [DMAC\\_CH \$n\$ \\_CMPLTD\\_BLK\\_TFR\\_SIZE](#), and CH $n$ \_STATUS[46:32] corresponds to [DMAC\\_CH \$n\$ \\_DATA\\_LEFT\\_IN\\_FIFO\[14:0\]](#).

### Suspension of Transfers Between Blocks

At the end of every block transfer, a block transfer completion interrupt [DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INT](#) is generated if:

- Global interrupt is enabled ([DMAC\\_INT\\_EN](#) = 1)
- The channel block transfer completion interrupt is enabled  
([DMAC\\_CH \$n\$ \\_ENABLE\\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#) = 1,  
[DMAC\\_CH \$n\$ \\_ENABLE\\_BLOCK\\_TFR\\_DONE\\_INTSIGNAL](#) = 1, [DMAC\\_CH \$n\$ \\_IOC\\_BLK\\_TFR](#) = 1)

For contiguous-address and auto-reloading-based multi-block transfers (neither source nor destination peripheral uses shadow-register or linked-list-based multi-block transfers), the DMA transfer automatically stalls after the [DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INT](#) interrupt is generated. VDMA does not proceed to the next block transfer until software writes 1 to [DMAC\\_CH \$n\$ \\_CLEAR\\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#) to clear the interrupt.

Channel suspension between blocks ensures that the block transfer done ISR (Interrupt Service Routine) of the next-to-last block is serviced before the final block transfer starts. This ensures that the ISR has cleared [DMAC\\_CH \$n\$ \\_SRC\\_MULTBLK\\_TYPE](#) and [DMAC\\_CH \$n\$ \\_DST\\_MULTBLK\\_TYPE](#) before the final block transfer is completed.

### End of Multi-Block Transfers

If either source or destination peripheral uses shadow-register or linked-list-based multi-block transfers, then [DMAC\\_CH \$n\$ \\_SHADOWREG\\_OR\\_LLI\\_LAST](#) indicates whether the current block is the last in the transfer. If this bit is 1, VDMA recognizes that the current block is the final block in the transfer and completes the DMA transfer operation at the end of the current block transfer.

For contiguous-address and auto-reloading-based multi-block transfers (when neither source nor destination peripheral uses shadow-register or linked-list-based multi-block transfers), if the corresponding multi-block type selection fields [DMAC\\_CH \$n\$ \\_SRC\\_MULTBLK\\_TYPE](#) and/or [DMAC\\_CH \$n\$ \\_DST\\_MULTBLK\\_TYPE](#) are 0 at the end of a block transfer, VDMA understands that the previous block was the final block in the transfer and completes the DMA transfer operation.

## 4.5.5 Flow Controller

The flow controller determines the length of the DMA block transfer. The flow controller can be VDMA, the source peripheral, or the destination peripheral; memory cannot serve as a flow controller.

If the block length is known before enabling the channel, configure VDMA as the flow controller. If the block length is unknown before enabling the channel, use the source or destination peripheral as the flow controller to determine when to terminate the DMA block transfer.

## 4.5.6 Channel Suspend and Resume

Software can suspend and resume a channel during DMA transfer. To suspend a channel during DMA transfer:

1. Software writes 1 to `DMAC_CHn_SUSP`.
2. VDMA halts all transfers from the source, after completing all AXI transfers initiated from the source.
3. VDMA sets `DMAC_CHn_CH_SRC_SUSPENDED_INT` to 1 to indicate that source transfer is suspended.
4. VDMA transfers all the data in channel FIFO to the destination. If `DMAC_CHn_SRC_TR_WIDTH < DMAC_CHn_DST_TR_WIDTH` and `DMAC_CHn_SUSP` is 1, there may still be data in the channel FIFO, but not enough to form a single transfer of `DMAC_CHn_DST_TR_WIDTH`. The remaining data in the channel FIFO will be transferred to the destination if the channel is resumed.
5. VDMA sets `DMAC_CHn_CH_SUSPENDED_INT` to 1 to indicate that the channel is suspended.

After a channel suspend, software can resume the channel by setting `DMAC_CHn_SUSP` to 0. Then, VDMA resumes the DMA transfer from the point where it was suspended.

### 4.5.7 Channel Disable

Under normal operation, software enables a channel by writing 1 to `DMAC_CHn_EN`, and VDMA clears `DMAC_CHn_EN` after channel transfer completion. Software can disable a channel before a transfer completes.

#### 4.5.7.1 Disabling a Suspended Channel Before Transfer Completion

To disable a suspended channel before transfer completion:

- Write 0 to `DMAC_CHn_EN` after `DMAC_CHn_CH_SUSPENDED_INTSTAT` is set to 1. If `DMAC_CHn_SRC_TR_WIDTH < DMAC_CHn_DST_TR_WIDTH` and `DMAC_CHn_SUSP` is 1, there may still be data in the channel FIFO, but not enough to form a single transfer of `DMAC_CHn_DST_TR_WIDTH`. In this case, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.
- VDMA sets `DMAC_CHn_CH_DISABLED_INTSTAT` to 1 to indicate that the channel is disabled and generates an interrupt.

#### 4.5.7.2 Disabling a Non-suspended Channel Before Transfer Completion

To disable a non-suspended channel before transfer completion:

- Software writes 0 to `DMAC_CHn_EN` during DMA transfer.
- VDMA halts all transfers from the source, after completing all AXI transfers initiated on the source.
- VDMA transfers all the data in the channel FIFO to the destination. When `DMAC_CHn_SRC_TR_WIDTH < DMAC_CHn_DST_TR_WIDTH` and `DMAC_CHn_EN` is 0, there may still be data in the channel FIFO, but not enough to form a single transfer of `DMAC_CHn_DST_TR_WIDTH`. In this scenario, once the channel is disabled, the remaining data in the channel FIFO is not transferred to the destination peripheral and is lost.
- VDMA sets `DMAC_CHn_CH_DISABLED_INTSTAT` to 1 to indicate that the channel is disabled and generates an interrupt.

**Note:**

Once software initiates a channel disable procedure by writing 0 to `DMAC_CHn_EN`, before `DMAC_CHn_CH_DISABLED_INT` is set to 1, you cannot re-enable the channel by writing 1 to `DMAC_CHn_EN`. VDMA will ignore this write operation.

## 4.5.8 Low-Power Technique

VDMA implements a low-power technique that intelligently monitors idle periods across multiple DMA channels, the slave bus interface, and AXI master interface channels in various scenarios. By detecting inactivity, this feature can turn off the clock for these modules, significantly reducing overall power consumption.

When activity is detected, the logic quickly restores the clocks to these modules, ensuring that performance remains uncompromised.

Configure `DMAC_LOWPOWER_CFGO_REG` to enable the low-power feature and manage the low-power counters.

### 4.5.8.1 Low-Power Technique for DMA Channels

DMA channels occupy a significant portion of the chip area in the VDMA module, resulting in higher power consumption compared to other components. Therefore, optimizing power usage in this module is essential.

The low-power technique for DMA channels employs a **DMA channel low-power state machine** to monitor activities. When the state machine detects a low-power condition, it activates a **DMA channel low-power delay counter**. This counter runs until it expires. Once the counter expires, the DMA channels enter a low-power state by gating the `AXI_DMAC_CORE_CLK`.

The DMA channels will remain in this low-power state until any activity is detected. If activity is detected while the delay counter is still running, the counter is reset and paused until the low-power condition is detected again.

### 4.5.8.2 Low-Power Technique for Slave Bus Interface

The slave bus interface unit (SBIU) accesses the internal registers of VDMA via the APB3 slave interface. The low-power technique can optimize the power consumption in SBIU.

The low-power technique for the slave bus interface employs a **SBIU state machine** to monitor activities. When a low-power condition is detected (i.e., when there are no ongoing APB reads or writes and the SBIU state machine is idle), the **SBIU low power delay counter** is activated. Once the delay counter expires, SBIU enters the low-power state by gating `PCLK` or `AXI_DMAC_CORE_CLK` (based on the clock mode configuration).

SBIU remains in the low-power state until an active read or write transaction is detected on the slave bus interface. If an active transaction is detected while the SBIU low-power delay counter running, the delay counter is reset and paused until the low-power condition is detected again.

If a read or write transaction occurs while SBIU is in a low-power state, the low-power logic immediately exits the low-power state by un-gating `PCLK` or `AXI_DMAC_CORE_CLK`.

### 4.5.8.3 Low-Power Technique for AXI Master Interface Channels

The AXI master interface module implements the AXI bus to transfer data between memory and peripheral.

Whenever a low-power condition is detected on the AXI master interface channels, the **AXI master interface channel low-power delay counter** starts. The AXI low-power logic waits until the delay counter expires. After the delay counter expires, the AXI master interface channel enters the low-power state by gating the clock of AXI master interface and AXI\_DMAC\_CORE\_CLK. It remains in this state until any activity is detected. If an activity is detected while the AXI master interface channel low-power delay counter is running, the delay counter is reset and paused until the low-power condition is detected again.

### 4.5.8.4 Global Low-Power Technique

The global low-power technique implements the low-power option based on the idle condition of the DMA channel, slave bus interface, and AXI master interface channels. If all the mentioned modules indicate that the VDMA is idle, the **global low-power delay counter** is activated.

The global low-power logic waits until the low-power delay counter expires. After the counter expires, VDMA enters the low-power state by gating the clocks of all modules. It remains in the low-power state until any activity is detected on any of the modules. If an activity is detected while the global low-power delay counter is running, the global delay counter is reset and paused until the low-power condition is again detected.

## 4.6 Interrupts

ESP32-P4's VDMA can generate the interrupt signal AXI\_DMAC\_INTR that will be sent to the [Interrupt Matrix](#).

The interrupt signal is generated by the internal interrupt sources from VDMA.

- Common interrupts:
  - DMAC\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INT: Slave interface undefined register decode error interrupt
  - DMAC\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INT: Slave interface common register read to write-only error interrupt
  - DMAC\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INT: Slave interface common register write to read-only error Interrupt
  - DMAC\_SLVIF\_COMMONREG\_DEC\_ERR\_INT: Slave interface common register decode error interrupt
- Channel interrupts ( $n = 1 \sim 4$ ):
  - DMAC\_CH $n$ \_CH\_ABORTED\_INT: Channel aborted interrupt
  - DMAC\_CH $n$ \_CH\_DISABLED\_INT: Channel disabled interrupt
  - DMAC\_CH $n$ \_CH\_SUSPENDED\_INT: Channel suspended interrupt
  - DMAC\_CH $n$ \_CH\_SRC\_SUSPENDED\_INT: Channel source suspended interrupt
  - DMAC\_CH $n$ \_SLVIF\_SHADOWREG\_WRON\_VALID\_ERR\_INT: Shadow register write on valid error interrupt

- DMAC\_CH $n$ \_SLVIF\_WRONCHEN\_ERR\_INT: Slave interface write on enabled channel error interrupt
- DMAC\_CH $n$ \_SLVIF\_RD2RWO\_ERR\_INT: Slave interface read to write-only error interrupt
- DMAC\_CH $n$ \_SLVIF\_WR2RO\_ERR\_INT: Slave interface write to read-only error interrupt
- DMAC\_CH $n$ \_SLVIF\_DEC\_ERR\_INT: Slave interface decode error interrupt
- DMAC\_CH $n$ \_SLVIF\_MULTIBLKTYPE\_ERR\_INT: Slave interface multi-block type error interrupt
- DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INT: Shadow register or LLI invalid error interrupt
- DMAC\_CH $n$ \_LLI\_WR\_SLV\_ERR\_INT: LLI write slave error interrupt
- DMAC\_CH $n$ \_LLI\_RD\_SLV\_ERR\_INT: LLI read slave error interrupt
- DMAC\_CH $n$ \_LLI\_WR\_DEC\_ERR\_INT: LLI write decode error interrupt
- DMAC\_CH $n$ \_LLI\_RD\_DEC\_ERR\_INT: LLI read decode error interrupt
- DMAC\_CH $n$ \_DST\_SLV\_ERR\_INT: Destination slave error interrupt
- DMAC\_CH $n$ \_SRC\_SLV\_ERR\_INT: Source slave error interrupt
- DMAC\_CH $n$ \_DST\_DEC\_ERR\_INT: Destination decode error interrupt
- DMAC\_CH $n$ \_SRC\_DEC\_ERR\_INT: Source decode error interrupt
- DMAC\_CH $n$ \_DST\_TRANSCOMP\_INT: Destination transfer completed interrupt
- DMAC\_CH $n$ \_SRC\_TRANSCOMP\_INT: Source transfer completed interrupt
- DMAC\_CH $n$ \_DMA\_TFR\_DONE\_INT: DMA transfer done interrupt
- DMAC\_CH $n$ \_BLOCK\_TFR\_DONE\_INT: Block transfer done interrupt

## 4.7 Programming Procedures

This section outlines the programming steps for different types of transfers.

### 4.7.1 Common Programming Procedures

The following two steps are common and should be performed before other programming procedures.

1. Set [HP\\_SYS\\_CLKRST\\_GDMA\\_SYS\\_CLK\\_EN](#) to 1 to enable VDMA bus clock.
2. Configure [TEE\\_DMA\\_GDMA\\_CH \$n\$ \\_W\\_PMS](#) and [TEE\\_DMA\\_GDMA\\_CH \$n\$ \\_R\\_PMS](#) to define the access permission of VDMA. For more details please refer to Chapter [18 Permission Control \(PMS\)](#).

### 4.7.2 Programming Procedures for Shadow-Register-Based Multi-Block Transfer

1. Read [DMAC\\_CH \$n\$ \\_EN](#) to select an available (unused) channel.
2. Configure [DMAC\\_CH \$n\$ \\_SRC\\_MULTBLK\\_TYPE](#) and/or [DMAC\\_CH \$n\$ \\_DST\\_MULTBLK\\_TYPE](#) to 2 to enable shadow-register-based multi-block transfer for source transfer and/or destination transfer.

3. Configure [DMAC\\_CHn\\_SARO\\_REG](#) and/or [DMAC\\_CHn\\_DARO\\_REG](#), [DMAC\\_CHn\\_BLOCK\\_TS](#), [DMAC\\_CHn\\_CTLO\\_REG](#), and [DMAC\\_CHn\\_CTL1\\_REG](#) for the first block. VDMA loads the configured values to the corresponding shadow registers.

**Notice:** The [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) field in [DMAC\\_CHn\\_CTL1\\_REG](#) must be the last one to be set to 1.

4. Set [DMAC\\_CHn\\_EN](#) to 1 to enable the corresponding channel.
5. VDMA initiates the DMA block transfer operation based on the configurations.
  - The block transfer might start immediately or after the handshaking request, depending on [DMAC\\_CHn\\_TT\\_FC](#). Specifically,
    - When the source is memory, the source transfer starts immediately; when the destination is memory, the destination transfer starts immediately.
    - When the source is a peripheral, obtaining data from the source requires waiting for a handshake with the source. When the destination is a peripheral, writing data to the destination requires waiting for a handshake with the destination.
  - VDMA checks [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) and if it is seen as 0, VDMA waits until software writes 1 to [DMAC\\_CHn\\_BLK\\_TFR\\_RESUMEREQ](#) to indicate valid shadow registers availability. Then VDMA re-attempts shadow register fetch operation. In this case, VDMA may generate a [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_INVALID\\_ERR\\_INT](#) interrupt.
  - VDMA checks [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) and if it is seen as 1, VDMA copies the shadow register contents to the registers used for executing the DMA block transfer (i.e., [DMAC\\_CHn\\_SARO\\_REG](#) and/or [DMAC\\_CHn\\_DARO\\_REG](#), [DMAC\\_CHn\\_BLOCK\\_TS](#), [DMAC\\_CHn\\_CTLO\\_REG](#), and [DMAC\\_CHn\\_CTL1\\_REG](#)) and clears [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#).
    - If VDMA sees [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_LAST](#) as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of current block transfer.
    - If VDMA sees [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_LAST](#) as 0, it understands that there are one or more blocks to be transferred and checks [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) again at the end of current block transfer.

6. Software waits [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) to be cleared to 0.
7. Configure [DMAC\\_CHn\\_SARO\\_REG](#) and/or [DMAC\\_CHn\\_DARO\\_REG](#), [DMAC\\_CHn\\_BLOCK\\_TS](#), [DMAC\\_CHn\\_CTLO\\_REG](#), and [DMAC\\_CHn\\_CTL1\\_REG](#) for the next block. If the next block is the last block, set [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_LAST](#) to 1.

**Notice:** [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_VALID](#) must be the last to be set to 1.

8. Software waits for a [DMAC\\_CHn\\_BLOCK\\_TFR\\_DONE\\_INT](#) interrupt or polls [DMAC\\_CHn\\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#) until it reads as 1 and goes back to Step 6.

**Note:**

In cases where a [DMAC\\_CHn\\_SHADOWREG\\_OR\\_LLI\\_INVALID\\_ERR\\_INT](#) interrupt is generated, follow the recommended flow to resume transfer:



- Configure `DMAC_CHn_SARO_REG` and/or `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG` for the next block.
- Set `DMAC_CHn_CLEAR_SHADOWREG_OR_LLI_INVALID_ERR_INTSTAT` to 1 to clear the interrupt.
- Set `DMAC_CHn_BLK_TFR_RESUMEREQ` to 1 to request for resuming block transfer.

### 4.7.3 Programming Procedures for Linked-List-Based Multi-Block Transfer

1. Reads `DMAC_CHn_EN` to select an available (unused) channel.
2. Configure `DMAC_CHn_SRC_MULTBLK_TYPE` and/or `DMAC_CHn_DST_MULTBLK_TYPE` to 3 to enable linked-list-based transfer for source transfer and/or destination transfer.
3. Configure `DMAC_CHn_LLPO_REG` to define the base address of the first linked list item and the master interface on which the linked list item is available.
4. Create one or more linked list items in the system memory. You can create the entire linked list item in advance or dynamically extend it using `DMAC_CHn_SHADOWREG_OR_LLI_VALID` and `DMAC_CHn_SHADOWREG_OR_LLI_LAST` fields of the LLI. Follow the steps below to dynamically extend the linked list.
  - During the DMA transfer process, when the linked list is not ready, configure `DMAC_CHn_SHADOWREG_OR_LLI_VALID` in the linked list to 0 and wait until the linked list is prepared. Then set `DMAC_CHn_SHADOWREG_OR_LLI_VALID` to 1 to extend the linked list.
  - When it is time to end the DMA transfer, set `DMAC_CHn_SHADOWREG_OR_LLI_LAST` of the last linked list to 1 to indicate the end of the transfer.
5. Set `DMAC_CHn_EN` to 1 to enable the channel.

**Note:**

You can swap the sequence of Step 4 and Step 5. However, if Step 5 is performed before Step 4, or if the linked list item for the next block transfer is not available in system memory during the multi-block transfer (i.e., `DMAC_CHn_SHADOWREG_OR_LLI_VALID` of the fetched LLI is 0), VDMA may generate a `DMAC_CHn_SHADOWREG_OR_LLI_INVALID_ERR_INT` interrupt.

6. VDMA initiates the DMA block transfer operation based on the configurations. The block transfer might start immediately or after the handshaking request, depending on `DMAC_CHn_TT_FC`. VDMA copies the linked list contents to the registers used for executing the DMA block transfer (i.e., `DMAC_CHn_SARO_REG` and/or `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG`) and initiates the DMA block transfer.
7. During the linked list fetch phase:
  - If VDMA reads `DMAC_CHn_SHADOWREG_OR_LLI_LAST` as 1, it understands that the current block is the final block in the transfer and completes the DMA transfer operation at the end of the current block transfer.
  - If VDMA reads `DMAC_CHn_SHADOWREG_OR_LLI_LAST` as 0, it understands that there are one or more blocks to be transferred and goes to Step 6.

- If VDMA reads `DMAC_CHn_SHADOWREG_OR_LLI_VALID` as 0, it may generate a `DMAC_CHn_SHADOWREG_OR_LLI_INVALID_ERR_INT` interrupt. VDMA waits until software writes 1 to `DMAC_CHn_BLK_TFR_RESUMEREQ` to indicate valid LLI availability before re-attempting the LLI read operation.

#### 4.7.4 Programming Procedures for Single-Block Transfer

1. Read `DMAC_CHn_EN` to choose a free (unused) channel.
2. Configure `DMAC_CHn_SRC_MULTBLK_TYPE` and `DMAC_CHn_DST_MULTBLK_TYPE` to 0 to enable contiguous-address-based single-block transfer.
3. Configure `DMAC_CHn_SARO_REG` and/or `DMAC_CHn_DARO_REG`, `DMAC_CHn_BLOCK_TS`, `DMAC_CHn_CTLO_REG`, and `DMAC_CHn_CTL1_REG` for the block.
4. Set `DMAC_CHn_EN` to 1 to enable the channel.
5. Software waits for the `DMAC_CHn_BLOCK_TFR_DONE_INT` interrupt or polls `DMAC_CHn_BLOCK_TFR_DONE_INTSTAT` until it is 1.

## 4.8 Register Summary

The addresses in this section are relative to the VDMA base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Version Control Registers</b>                |   |         |        |
| <a href="#">DMAC_IDO_REG</a>                    | VDMA ID number  | 0x0000  | RO     |
| <a href="#">DMAC_COMPVERO_REG</a>               | VDMA version number                                   | 0x0008  | RO     |
| <b>Configuration Registers</b>                  |   |         |        |
| <a href="#">DMAC_CFGO_REG</a>                   | VDMA Configuration register                           | 0x0010  | R/W    |
| <a href="#">DMAC_CHENO_REG</a>                  | VDMA channel enable register                          | 0x0018  | varies |
| <a href="#">DMAC_RESETO_REG</a>                 | VDMA reset control register                           | 0x0058  | R/W    |
| <a href="#">DMAC_LOWPOWER_CFGO_REG</a>          | VDMA low power configuration register 0               | 0x0060  | R/W    |
| <a href="#">DMAC_LOWPOWER_CFG1_REG</a>          | VDMA low power configuration register 1               | 0x0064  | R/W    |
| <a href="#">DMAC_CH1_SARO_REG</a>               | VDMA channel 1 source address register                | 0x0100  | R/W    |
| <a href="#">DMAC_CH1_DARO_REG</a>               | VDMA channel 1 destination address register           | 0x0108  | R/W    |
| <a href="#">DMAC_CH1_BLOCK_TSO_REG</a>          | VDMA channel 1 block transfer size register           | 0x0110  | R/W    |
| <a href="#">DMAC_CH1_CTLO_REG</a>               | VDMA channel 1 control register 0                     | 0x0118  | R/W    |
| <a href="#">DMAC_CH1_CTL1_REG</a>               | VDMA channel 1 control register 1                     | 0x011C  | R/W    |
| <a href="#">DMAC_CH1_CFGO_REG</a>               | VDMA channel 1 configuration register 0               | 0x0120  | varies |
| <a href="#">DMAC_CH1_CFG1_REG</a>               | VDMA channel 1 configuration register 1               | 0x0124  | varies |
| <a href="#">DMAC_CH1_LLPO_REG</a>               | VDMA channel 1 linked list pointer register           | 0x0128  | R/W    |
| <a href="#">DMAC_CH1_BLK_TFR_RESUMEREQO_REG</a> | VDMA channel 1 block transfer resume request register | 0x0148  | WO     |
| <a href="#">DMAC_CH1_AXI_IDO_REG</a>            | VDMA channel 1 AXI ID register                        | 0x0150  | R/W    |
| <a href="#">DMAC_CH2_SARO_REG</a>               | VDMA channel 2 source address register                | 0x0200  | R/W    |
| <a href="#">DMAC_CH2_DARO_REG</a>               | VDMA channel 2 destination address register           | 0x0208  | R/W    |
| <a href="#">DMAC_CH2_BLOCK_TSO_REG</a>          | VDMA channel 2 block transfer size register           | 0x0210  | R/W    |
| <a href="#">DMAC_CH2_CTLO_REG</a>               | VDMA channel 2 control register 0                     | 0x0218  | R/W    |
| <a href="#">DMAC_CH2_CTL1_REG</a>               | VDMA channel 2 control register 1                     | 0x021C  | R/W    |

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <a href="#">DMAC_CH2_CFG0_REG</a>               | VDMA channel 2 configuration register 0               | 0x0220  | varies |
| <a href="#">DMAC_CH2_CFG1_REG</a>               | VDMA channel 2 configuration register 1               | 0x0224  | varies |
| <a href="#">DMAC_CH2_LLPO_REG</a>               | VDMA channel 2 linked list pointer register           | 0x0228  | R/W    |
| <a href="#">DMAC_CH2_BLK_TFR_RESUMEREQO_REG</a> | VDMA channel 2 block transfer resume request register | 0x0248  | WO     |
| <a href="#">DMAC_CH2_AXI_IDO_REG</a>            | VDMA channel 2 AXI ID register                        | 0x0250  | R/W    |
| <a href="#">DMAC_CH3_SARO_REG</a>               | VDMA channel 3 source address register                | 0x0300  | R/W    |
| <a href="#">DMAC_CH3_DARO_REG</a>               | VDMA channel 3 destination address register           | 0x0308  | R/W    |
| <a href="#">DMAC_CH3_BLOCK_TSO_REG</a>          | VDMA channel 3 block transfer size register           | 0x0310  | R/W    |
| <a href="#">DMAC_CH3_CTLO_REG</a>               | VDMA channel 3 control register 0                     | 0x0318  | R/W    |
| <a href="#">DMAC_CH3_CTL1_REG</a>               | VDMA channel 3 control register 1                     | 0x031C  | R/W    |
| <a href="#">DMAC_CH3_CFG0_REG</a>               | VDMA channel 3 configuration register 0               | 0x0320  | varies |
| <a href="#">DMAC_CH3_CFG1_REG</a>               | VDMA channel 3 configuration register 1               | 0x0324  | varies |
| <a href="#">DMAC_CH3_LLPO_REG</a>               | VDMA channel 3 linked list pointer register           | 0x0328  | R/W    |
| <a href="#">DMAC_CH3_BLK_TFR_RESUMEREQO_REG</a> | VDMA channel 3 block transfer resume request register | 0x0348  | WO     |
| <a href="#">DMAC_CH3_AXI_IDO_REG</a>            | VDMA channel 3 AXI ID register                        | 0x0350  | R/W    |
| <a href="#">DMAC_CH4_SARO_REG</a>               | VDMA channel 4 source address register                | 0x0400  | R/W    |
| <a href="#">DMAC_CH4_DARO_REG</a>               | VDMA channel 4 destination address register           | 0x0408  | R/W    |
| <a href="#">DMAC_CH4_BLOCK_TSO_REG</a>          | VDMA channel 4 block transfer size register           | 0x0410  | R/W    |
| <a href="#">DMAC_CH4_CTLO_REG</a>               | VDMA channel 4 control register 0                     | 0x0418  | R/W    |
| <a href="#">DMAC_CH4_CTL1_REG</a>               | VDMA channel 4 control register 1                     | 0x041C  | R/W    |
| <a href="#">DMAC_CH4_CFG0_REG</a>               | VDMA channel 4 configuration register 0               | 0x0420  | varies |
| <a href="#">DMAC_CH4_CFG1_REG</a>               | VDMA channel 4 configuration register 1               | 0x0424  | varies |
| <a href="#">DMAC_CH4_LLPO_REG</a>               | VDMA channel 4 linked list pointer register           | 0x0428  | R/W    |
| <a href="#">DMAC_CH4_BLK_TFR_RESUMEREQO_REG</a> | VDMA channel 4 block transfer resume request register | 0x0448  | WO     |
| <a href="#">DMAC_CH4_AXI_IDO_REG</a>            | VDMA channel 4 AXI ID register                        | 0x0450  | R/W    |
| <b>Interrupt Registers</b>                      |   |         |        |

| Name   | Description                                     | Address | Access |
|--|---|---------|--------|
| <a href="#">DMAC_INTSTATUSO_REG</a>                  | VDMA interrupt status register                  | 0x0030  | RO     |
| <a href="#">DMAC_COMMONREG_INTCLEARO_REG</a>         | VDMA common interrupt clear register            | 0x0038  | WO     |
| <a href="#">DMAC_COMMONREG_INTSTATUS_ENABLEO_REG</a> | VDMA common interrupt status enable register    | 0x0040  | varies |
| <a href="#">DMAC_COMMONREG_INTSIGNAL_ENABLEO_REG</a> | VDMA common interrupt signal enable register    | 0x0048  | varies |
| <a href="#">DMAC_COMMONREG_INTSTATUSO_REG</a>        | VDMA common interrupt status register           | 0x0050  | RO     |
| <a href="#">DMAC_CH1_INTSTATUS_ENABLEO_REG</a>       | VDMA channel 1 interrupt status enable register | 0x0180  | varies |
| <a href="#">DMAC_CH1_INTSTATUSO_REG</a>              | VDMA channel 1 interrupt status register        | 0x0188  | RO     |
| <a href="#">DMAC_CH1_INTSIGNAL_ENABLEO_REG</a>       | VDMA channel 1 interrupt signal enable register | 0x0190  | varies |
| <a href="#">DMAC_CH1_INTCLEARO_REG</a>               | VDMA channel 1 interrupt clear register         | 0x0198  | WO     |
| <a href="#">DMAC_CH2_INTSTATUS_ENABLEO_REG</a>       | VDMA channel 2 interrupt status enable register | 0x0280  | varies |
| <a href="#">DMAC_CH2_INTSTATUSO_REG</a>              | VDMA channel 2 interrupt status register        | 0x0288  | RO     |
| <a href="#">DMAC_CH2_INTSIGNAL_ENABLEO_REG</a>       | VDMA channel 2 interrupt signal enable register | 0x0290  | varies |
| <a href="#">DMAC_CH2_INTCLEARO_REG</a>               | VDMA channel 2 interrupt clear register         | 0x0298  | WO     |
| <a href="#">DMAC_CH3_INTSTATUS_ENABLEO_REG</a>       | VDMA channel 3 interrupt status enable register | 0x0380  | varies |
| <a href="#">DMAC_CH3_INTSTATUSO_REG</a>              | VDMA channel 3 interrupt status register        | 0x0388  | RO     |
| <a href="#">DMAC_CH3_INTSIGNAL_ENABLEO_REG</a>       | VDMA channel 3 interrupt signal enable register | 0x0390  | varies |
| <a href="#">DMAC_CH3_INTCLEARO_REG</a>               | VDMA channel 3 interrupt clear register         | 0x0398  | WO     |
| <a href="#">DMAC_CH4_INTSTATUS_ENABLEO_REG</a>       | VDMA channel 4 interrupt status enable register | 0x0480  | varies |
| <a href="#">DMAC_CH4_INTSTATUSO_REG</a>              | VDMA channel 4 interrupt status register        | 0x0488  | RO     |
| <a href="#">DMAC_CH4_INTSIGNAL_ENABLEO_REG</a>       | VDMA channel 4 interrupt signal enable register | 0x0490  | varies |
| <a href="#">DMAC_CH4_INTCLEARO_REG</a>               | VDMA channel 4 interrupt clear register         | 0x0498  | WO     |
| <b>status registers</b>                              |   |         |        |
| <a href="#">DMAC_CH1_STATUSO_REG</a>                 | VDMA channel 1 status register 0                | 0x0130  | RO     |
| <a href="#">DMAC_CH1_STATUS1_REG</a>                 | VDMA channel 1 status register 1                | 0x0134  | RO     |
| <a href="#">DMAC_CH1_SSTATO_REG</a>                  | VDMA channel 1 source status register           | 0x0160  | RO     |
| <a href="#">DMAC_CH1_DSTATO_REG</a>                  | VDMA channel 1 destination status register      | 0x0168  | RO     |
| <a href="#">DMAC_CH1_SSTATARO_REG</a>                | VDMA channel 1 source status address register   | 0x0170  | R/W    |

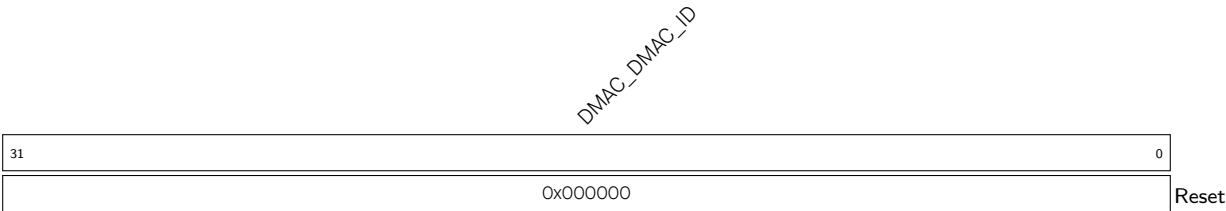
| Name                                  | Description  | Address | Access |
|---------------------------------------|--|---------|--------|
| <a href="#">DMAC_CH1_DSTATARO_REG</a> | VDMA channel 1 destination status address register | 0x0178  | R/W    |
| <a href="#">DMAC_CH2_STATUSO_REG</a>  | VDMA channel 2 status register 0                   | 0x0230  | RO     |
| <a href="#">DMAC_CH2_STATUS1_REG</a>  | VDMA channel 2 status register 1                   | 0x0234  | RO     |
| <a href="#">DMAC_CH2_SSTATO_REG</a>   | VDMA channel 2 source status register              | 0x0260  | RO     |
| <a href="#">DMAC_CH2_DSTATO_REG</a>   | VDMA channel 2 destination status register         | 0x0268  | RO     |
| <a href="#">DMAC_CH2_SSTATARO_REG</a> | VDMA channel 2 source status address register      | 0x0270  | R/W    |
| <a href="#">DMAC_CH2_DSTATARO_REG</a> | VDMA channel 2 destination status address register | 0x0278  | R/W    |
| <a href="#">DMAC_CH3_STATUSO_REG</a>  | VDMA channel 3 status register 0                   | 0x0330  | RO     |
| <a href="#">DMAC_CH3_STATUS1_REG</a>  | VDMA channel 3 status register 1                   | 0x0334  | RO     |
| <a href="#">DMAC_CH3_SSTATO_REG</a>   | VDMA channel 3 source status register              | 0x0360  | RO     |
| <a href="#">DMAC_CH3_DSTATO_REG</a>   | VDMA channel 3 destination status register         | 0x0368  | RO     |
| <a href="#">DMAC_CH3_SSTATARO_REG</a> | VDMA channel 3 source status address register      | 0x0370  | R/W    |
| <a href="#">DMAC_CH3_DSTATARO_REG</a> | VDMA channel 3 destination status address register | 0x0378  | R/W    |
| <a href="#">DMAC_CH4_STATUSO_REG</a>  | VDMA channel 4 status register 0                   | 0x0430  | RO     |
| <a href="#">DMAC_CH4_STATUS1_REG</a>  | VDMA channel 4 status register 1                   | 0x0434  | RO     |
| <a href="#">DMAC_CH4_SSTATO_REG</a>   | VDMA channel 4 source status register              | 0x0460  | RO     |
| <a href="#">DMAC_CH4_DSTATO_REG</a>   | VDMA channel 4 destination status register         | 0x0468  | RO     |
| <a href="#">DMAC_CH4_SSTATARO_REG</a> | VDMA channel 4 source status address register      | 0x0470  | R/W    |
| <a href="#">DMAC_CH4_DSTATARO_REG</a> | VDMA channel 4 destination status address register | 0x0478  | R/W    |

## 4.9 Registers

The addresses in this section are relative to the VDMA base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

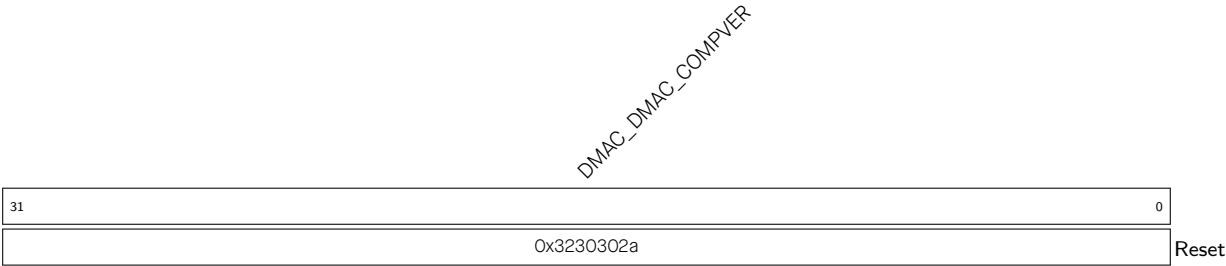
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 4.1. DMAC\_IDO\_REG (0x0000)



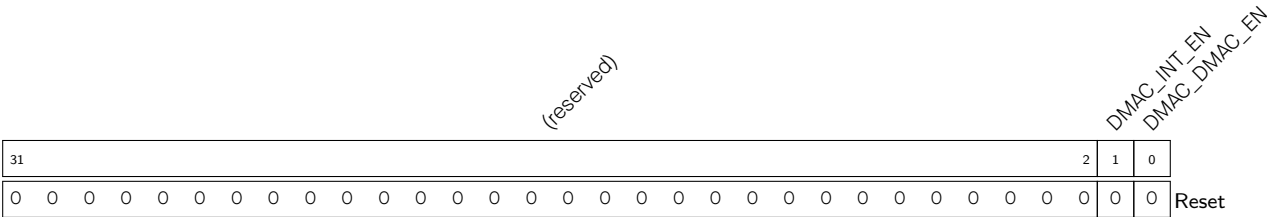
**DMAC\_DMID** Represents VDMA ID number. (RO)

Register 4.2. DMAC\_COMPVERO\_REG (0x0008)



**DMAC\_DMCOMPVER** Represents VDMA version number. (RO)

Register 4.3. DMAC\_CFG0\_REG (0x0010)



**DMAC\_DMEN** Configures whether to enable VDMA.

0: Disable

1: Enable

**Note:** If this field is cleared but a channel is still active, this field will still return 1. When hardware has terminated activity on all channels, this field will return 0.

(R/W)

**DMAC\_INT\_EN** Configures whether to enable global interrupt.

0: Disable

1: Enable

(R/W)



#### Register 4.4. DMAC\_CHENO\_REG (0x0018)

[illegible]

**DMAC\_CH $n$ \_EN ( $n$ : 1-4)** Configures whether to enable VDMA channel  $n$ . Hardware automatically clears this bit after the last AXI transfer of the DMA transfer has been completed. Software can poll this field to determine when this channel is free for a new DMA transfer.

0: Disable channel *n*

1: Enable channel  $n$

(R/W)

**DMAC\_CH*n*\_EN\_WE (*n*: 1-4)** Configures whether to enable write to **DMAC\_CH*n*\_EN**. This field always reads as 0.

0: Disable write to `DMAC_CHn_EN`

1: Enable write to DMAC\_CHn\_EN

(WO)

**DMAC\_CH $n$ \_SUSP** ( $n$ : 1-4) Configures whether to suspend channel  $n$ .

0: Do not suspend channel  $n$

1: Suspend channel  $n$

Software can clear this field to 0 after VDMA sets `DMAC_CHn_CH_SUSPENDED_INTSTAT` to 1, to exit the channel suspend mode.

**Note:** This field is cleared when channel *n* is disabled.

(R/W)

**DMAC\_CHn\_SUSP\_WE** (*n*: 1-4) Configures whether to enable write to **DMAC\_CHn\_SUSP**. This field always reads as 0.

0: Disable write to DMAC\_CHn\_SUSP

1: Enable write to DMAC CH<sub>n</sub> SUSP

(WO)

**Register 4.5. DMAC\_RESETO\_REG (0x0058)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|-------|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | DMAC_DMAR_RST |       |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0             | Reset |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             |       | 0 | 0 |

**DMAC\_DMAC\_RST** Configures whether to reset VDMA. Software writes 1 to this field to reset VDMA and polls this field to see if it is 0. VDMA resets all the modules except the APB slave interface module and clears this field to 0.

**Note:** Software is not allowed to write 0 to this field.

(R/W)

**Register 4.6. DMAC\_LOWPOWER\_CFGO\_REG (0x0060)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                   |   |   |       |                   |  |  |  |                   |  |  |  |                  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------|---|---|-------|-------------------|--|--|--|-------------------|--|--|--|------------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | DMAC_MXIF_CSLP_EN |   |   |       | DMAC_SBIU_CSLP_EN |  |  |  | DMAC_CHNL_CSLP_EN |  |  |  | DMAC_GBL_CSLP_EN |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4                 | 3 | 2 | 1     | 0                 |  |  |  |                   |  |  |  |                  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1                 | 1 | 1 | Reset |                   |  |  |  |                   |  |  |  |                  |  |  |  |

**DMAC\_GBL\_CSLP\_EN** Configures whether to enable global low-power feature.

0: Disable

1: Enable

(R/W)

**DMAC\_CHNL\_CSLP\_EN** Configures whether to enable low-power feature for DMA channels.

0: Disable

1: Enable

(R/W)

**DMAC\_SBIU\_CSLP\_EN** SBIU Configures whether to enable low-power feature for slave bus interface.

0: Disable

1: Enable

(R/W)

**DMAC\_MXIF\_CSLP\_EN** Configures whether to enable low-power feature for AXI master interface.

0: Disable

1: Enable

(R/W)

Register 4.7. DMAC\_LOWPOWER\_CFG1\_REG (0x0064)

|            |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  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| 31         |  |  |  |  |  |  |  | 24              |  |  |  |  |  |  |  | 23              |  |  |  |  |  |  |  | 16              |  |  |  |  |  |  |  | 15 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  | 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| 0          |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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| 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

**DMAC\_GLCH\_LPDLY** Configures the value of the AXI master interface low-power delay counter. The programmed value must be greater than or equal to 0x4. If it is less than 0x4, the field will reset to 0x40. (R/W)

**DMAC\_SBIU\_LPDLY** Configures the value of the SBIU low-power delay counter. The programmed value must be greater than or equal to 0x4. If it is less than 0x4, the field will reset to 0x40. (R/W)

**DMAC\_MXIF\_LPDLY** Configures the value of the global low-power delay counter and the DMA channel low-power delay counter. The programmed value must be greater than or equal to 0x4. If it is less than 0x4, the field will reset to 0x40. (R/W)

Register 4.8. DMAC\_CH $n$ \_SARO\_REG ( $n$ : 1-4) (0x0100\* $n$ )

|                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|
| DMAC_CH <sub>n</sub> _SAR0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
| 31                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |
| 0x000000                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
| Reset                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |

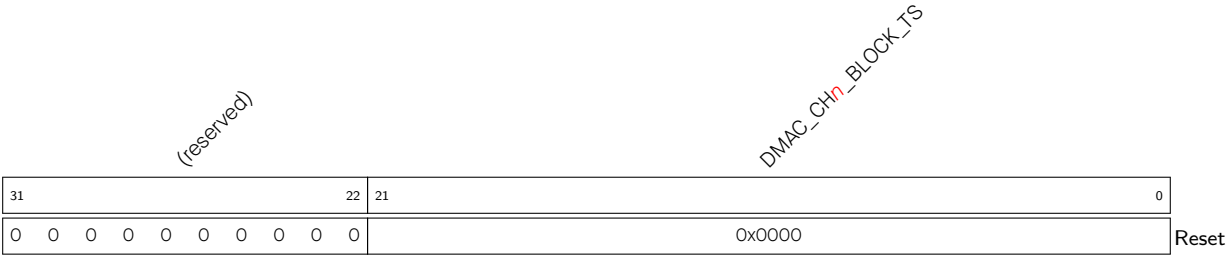
**DMAC\_CH $n$ \_SARO** Configures the source address of DMA transfer. This field is updated after each source transfer. **DMAC\_CH $n$ \_SINC** determines whether the address increments or remains unchanged on every source transfer throughout the block transfer. (R/W)

Register 4.9. DMAC\_CH $n$ \_DARO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0008)

|                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|
| DMAC_CH <sub>n</sub> _DAR0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
| 31                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |
| 0x000000                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
| Reset                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |

**DMAC\_CH $n$ \_DARO** Configures the destination address of DMA transfer. This field is updated after each source transfer. **DMAC\_CH $n$ \_DINC** determines whether the address increments or remains unchanged on every destination transfer throughout the block transfer. (R/W)

Register 4.10. DMAC\_CHn\_BLOCK\_TSO\_REG (n: 1-4) (0x0100\*n + 0x0010)



**DMAC\_CHn\_BLOCK\_TS** Configures the total number of **DMAC\_CHn\_SRC\_TR\_WIDTH** in a DMA transfer. The programming range of this field is 0 ~ 4,194,303.  
Block transfer size = Programmed value + 1  
(R/W)

Register 4.11. DMAC\_CH $n$ \_CTLO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0018)

|            |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |    |     |  |     |    |     |  |   |    |    |   |   |    |    |   |   |   |   |   |   |   |   |       |   |   |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|----|-----|--|-----|----|-----|--|---|----|----|---|---|----|----|---|---|---|---|---|---|---|---|-------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |    |     |  |     |    |     | DMAC_CH <sub>n</sub> _NONPOSTED_LASTWRITE_EN |   |    |    |   |   |    |    |   |   |   |   |   |   |   |   |       |   |   |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _DST_MSIZ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _SRC_MSIZ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _DST_TR_WIDTH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _SRC_TR_WIDTH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _DINC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _SINC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _DMS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _SMS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30 | 29 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     | 22 | 21  |  |     | 18 | 17  |  |   | 14 | 13 |   |   | 11 | 10 |   |   | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0  | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0 |    | 0x0 |  | 0x2 |    | 0x2 |  | 0 | 0  | 0  | 0 | 0 | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**DMAC\_CH $n$ \_SMS** Configures which AXI master to access the source.

0: AXI Master 1

1: AXI Master 2

(R/W)

**DMAC\_CH $n$ \_DMS** Configures which AXI master to access the destination.

0: AXI Master 1

1: AXI Master 2

(R/W)

**DMAC\_CH $n$ \_SINC** Configures whether to increment the source address on every source transfer.

If VDMA is fetching data from a source peripheral's FIFO at a fixed address, then set this field to 1.

0: Increment

1: No change

(R/W)

**DMAC\_CH $n$ \_DINC** Configures whether to increment the destination address on every destination transfer. If VDMA is writing data to a source peripheral's FIFO at a fixed address, then set this field to 1.

0: Increment

1: No change

(R/W)

**DMAC\_CH $n$ \_SRC\_TR\_WIDTH** Configures source transfer width.

0x0: 8 bits

0x1: 16 bits

0x2: 32 bits

0x3: 64 bits

(R/W)

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**Register 4.11. DMAC\_CH $n$ \_CTLO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0018)**

Continued from the previous page...

**DMAC\_CH $n$ \_DST\_TR\_WIDTH** Configures destination transfer width.

0x0: 8 bits  
0x1: 16 bits  
0x2: 32 bits  
0x3: 64 bits  
(R/W)

**DMAC\_CH $n$ \_SRC\_MSIZ** Configures the length of the source burst transaction. Every time the handshaking interface requests for a source burst transaction, the read value of this field from the source is the number of data items, each of width **DMAC\_CH $n$ \_SRC\_TR\_WIDTH**.

0x0: 1 data item  
0x1: 4 data items  
0x2: 8 data items  
0x3: 16 data items  
0x4: 32 data items  
0x5: 64 data items  
0x6: 128 data items  
0x7: 256 data items  
0x8: 512 data items  
0x9: 1024 data items  
(R/W)

**DMAC\_CH $n$ \_DST\_MSIZ** Configures the length of the destination burst transaction. Every time the handshaking interface requests for a destination burst transaction, the read value of this field from the destination is the number of data items, each of width **DMAC\_CH $n$ \_SRC\_TR\_WIDTH**.

0x0: 1 data item  
0x1: 4 data items  
0x2: 8 data items  
0x3: 16 data items  
0x4: 32 data items  
0x5: 64 data items  
0x6: 128 data items  
0x7: 256 data items  
0x8: 512 data items  
0x9: 1024 data items  
(R/W)

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**Register 4.11. DMAC\_CH $n$ \_CTLO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0018)**

Continued from the previous page...

**DMAC\_CH $n$ \_NONPOSTED\_LASTWRITE\_EN** Configures whether to enable non-posted writes throughout the block transfer.

Posted writes refers to sending data without the need to write the data into the destination (the data may still be in transit); VDMA can consider this write request to be complete. Non-posted writes refers to sending data that needs to be written into the destination and requires a response, only then can VDMA consider this write request to be complete.

0: Posted writes can be used throughout the block transfer.

1: Posted writes can be used at the end of the block transfer (within the block). The last write must be non-posted to ensure synchronization between the generation of the block completion interrupt and the final written data reaching the destination.

(R/W)

Register 4.12. DMAC\_CH $n$ \_CTL1\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x001C)

|  |    |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |     |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |   |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|--|----|----|----|----|----|----|----|----|-----|----|----|----|----|----|----|----|-----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|---|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| DMAC_CH <sub>n</sub> _SHADOWREG_OR_LLI_VALID |    |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |     |    |    |    |    |   | DMAC_CH <sub>n</sub> _SHADOWREG_OR_LLI_LAST |   |   |   |   |   |   |   |   |       |   |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _IOC_BLKTRF |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _DST_STAT_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _SRC_STAT_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _AWLEN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _AWLEN_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _ARLEN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_CH <sub>n</sub> _ARLEN_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22  | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14  | 13 | 12 | 11 | 10 | 9 | 8   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |   |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x0 |    |    |    |    |    |    | 0  | 0x0 |    |    |    |    |   |   | 0 | 0 | x |   |   |   |   |   |       | 0 |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |    |    |    |    |    |    |    |    |     |    |    |    |    |    |    |    |     |    |    |    |    |   |   |   |   |   |   |   |   |   |   | Reset |   |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**DMAC\_CH $n$ \_ARLEN\_EN** Configures whether to enable the length of the source burst transfer.

0: VDMA uses any possible value that is less than or equal to 16 as the length of the source burst transfer.

1: VDMA uses the value of **DMAC\_CH $n$ \_ARLEN** as the length of the source burst transfer till the extent possible. The remaining transfers use the maximum possible burst transfer length. For example, if the data size is 192 bytes and the source burst transfer length **DMAC\_CH $n$ \_ARLEN** is set to 128 bytes, then after transmitting 128 bytes, the remaining 64 bytes is the maximum possible burst transfer length.

(R/W)

**DMAC\_CH $n$ \_ARLEN** Configures the length of the source burst transfer. The specified burst length is used for source data transfer till the extent possible. The remaining transfers use the maximum possible value that is less than or equal to 16.

(R/W)

**DMAC\_CH $n$ \_AWLEN\_EN** Configures whether to enable the length of the destination burst transfer.

0: VDMA uses any possible value that is less than or equal to 16 as the length of the destination burst transfer.

1: VDMA uses the value of **DMAC\_CH $n$ \_AWLEN** as the length of the destination burst transfer till the extent possible. The remaining transfers use the maximum possible burst transfer length.

(R/W)

**DMAC\_CH $n$ \_AWLEN** Configures the length of the destination burst transfer. The specified burst length is used for destination data transfer till the extent possible. The remaining transfers use the maximum possible value that is less than or equal to 16.

(R/W)

**DMAC\_CH $n$ \_SRC\_STAT\_EN** Configures whether to enable fetch of source status.

This logic enables the fetch of the status from the source peripheral of channel  $n$  pointed to by **DMAC\_CH $n$ \_SSTATARO**. The value is subsequently stored in **DMAC\_CH $n$ \_SSTAT**. At the end of each block transfer, the status value is written back to the **DMAC\_CH $n$ \_SSTAT** register of the linked list, if either source or destination peripheral uses linked-list-based multi-block transfer.

0: Do not fetch source status

1: Fetch source status and store the value in **DMAC\_CH $n$ \_SSTAT**

(R/W)

Continued on the next page...



**Register 4.12. DMAC\_CH $n$ \_CTL1\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x001C)**

Continued from the previous page...

**DMAC\_CH $n$ \_DST\_STAT\_EN** Configures whether to enable fetch of destination status.

This logic enables the fetch of the status from the destination peripheral of channel  $n$  pointed to by [DMAC\\_CH \$n\$ \\_DSTATARO](#). The value is subsequently stored in [DMAC\\_CH \$n\$ \\_DSTAT](#). At the end of each block transfer, the status value is written back to the [DMAC\\_CH \$n\$ \\_DSTAT](#) register of the linked list, if either source or destination peripheral uses linked-list-based multi-block transfer.

0: Do not fetch destination status

1: Fetch destination status and store the value in [DMAC\\_CH \$n\$ \\_DSTAT](#)

(R/W)

**DMAC\_CH $n$ \_IOC\_BLKTRF** Configures whether to enable the interrupt on completion of multi-block transfer based on shadow register or linked list.

**Note:** If the source and destination uses contiguous-address or auto-reloading-based multi-block transfer, this field cannot be modified on a block by block basis. In addition, the programmed value before enabling the channel will be used for all the blocks in DMA transfer.

0: Disable [DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#)

1: Enable [DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#), valid when

[DMAC\\_CH \$n\$ \\_ENABLE\\_BLOCK\\_TFR\\_DONE\\_INTSTAT](#) is 1. To output a [DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INT](#) interrupt, set [DMAC\\_CH \$n\$ \\_ENABLE\\_BLOCK\\_TFR\\_DONE\\_INTSIGNAL](#) to 1.

(R/W)

**DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_LAST** Configures whether the shadow register or linked list item is the last one.

0: Not the last one

1: The last one

(R/W)

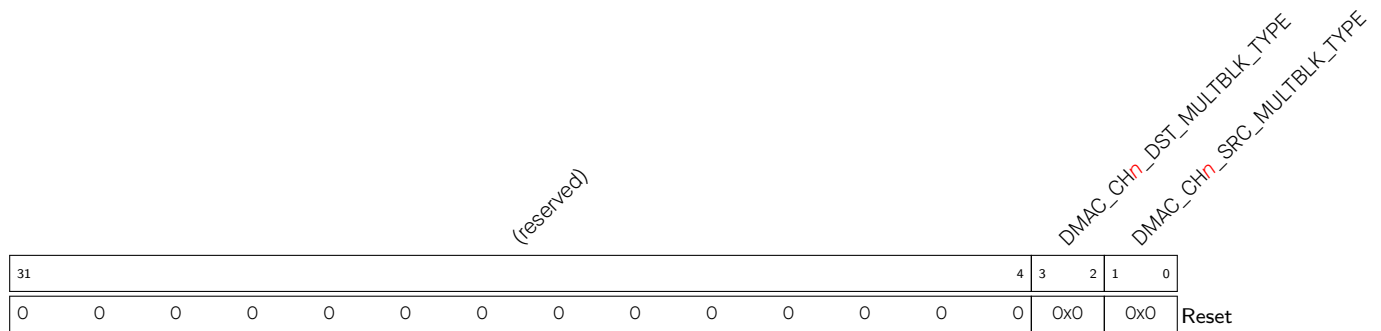
**DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** Configures whether the contents of shadow register or the linked list item are valid.

0: Invalid

1: Valid

(R/W)

**Register 4.13. DMAC\_CH*n*\_CFG0\_REG (*n*: 1-4) (0x0100\**n* + 0x0120)**



**DMAC\_CHn\_SRC\_MULTBLK\_TYPE** Configures the source multi-block transfer type.

- 0: Contiguous address
- 1: Auto reloading
- 2: Shadow register
- 3: Linked list

(R/W)

**DMAC\_CHn\_DST\_MULTBLK\_TYPE** Configures the destination multi-block transfer type.

- 0: Contiguous address
- 1: Auto reloading
- 2: Shadow register
- 3: Linked list

If both `DMAC_CHn_SRC_MULTBLK_TYPE` and `DMAC_CHn_DST_MULTBLK_TYPE` are 0, then the transfer type is single-block transfer based on contiguous address.

(R/W)

**Register 4.14. DMAC\_CH $n$ \_CFG1\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0124)**

|            |     |                                   |     |                                   |     |                                 |    |                               |    |                                |    |            |     |                               |   |            |     |                               |   |            |   |                             |       |
|------------|-----|-----------------------------------|-----|-----------------------------------|-----|---------------------------------|----|-------------------------------|----|--------------------------------|----|------------|-----|-------------------------------|---|------------|-----|-------------------------------|---|------------|---|-----------------------------|-------|
| (reserved) |     | DMAC_CH <sub>n</sub> _DST_OSR_LMT |     | DMAC_CH <sub>n</sub> _SRC_OSR_LMT |     | DMAC_CH <sub>n</sub> _LOCK_CH_L |    | DMAC_CH <sub>n</sub> _LOCK_CH |    | DMAC_CH <sub>n</sub> _CH_PRIOR |    | (reserved) |     | DMAC_CH <sub>n</sub> _DST_PER |   | (reserved) |     | DMAC_CH <sub>n</sub> _SRC_PER |   | (reserved) |   | DMAC_CH <sub>n</sub> _TT_FC |       |
| 31         | 30  | 27                                | 26  | 23                                | 22  | 21                              | 20 | 19                            | 17 | 16                             | 14 | 13         | 12  | 11                            | 9 | 8          | 7   | 6                             | 3 | 2          | 0 |                             |       |
| 0          | 0x0 |                                   | 0x0 |                                   | 0x0 |                                 | 0  | 0x3                           |    | 0                              | 0  | 0          | 0x0 | 0                             | 0 | 0          | 0x0 | 0                             | 0 | 0          | 0 | 0x3                         | Reset |

**DMAC\_CHn\_TT\_FC** Configures transfer type and flow controller.

0x0: Transfer type is memory to memory and flow controller is VDMA

Ox1: Transfer type is memory to peripheral and flow controller is VDMA

0x2: Transfer type is peripheral to memory and flow controller is VDMA

0x3: Invalid

Ox4: Transfer type is peripheral to memory and flow controller is source peripheral

0x5: Invalid

0x6: Transfer type is memory to peripheral and flow controller is destination peripheral

0x7: Invalid

(R/W)

**DMAC\_CH $n$ \_SRC\_PER** Assigns a handshaking interface (0 ~ 2) to the source of channel  $n$ . (R/W)

**DMAC\_CH $n$ \_DST\_PER** Assigns a handshaking interface (0 ~ 2) to the destination of channel  $n$ .  
(R/W)

**DMAC\_CHn\_CH\_PRIOR** Assigns channel priority (0 ~ 3). A priority of 3 is the highest priority, and 0 is the lowest. A programmed value outside this range will cause erroneous behavior. (R/W)

**DMAC\_CH<sub>n</sub>\_LOCK\_CH** VDMA does not support lock feature. Reads of this field always return 0.  
(RO)

**DMAC\_CH<sub>n</sub>\_LOCK\_CH\_L** VDMA does not support lock feature. Reads of this field always return 0.  
(RO)

**DMAC\_CHn\_SRC\_OSR\_LMT** Configures the limit of the source AXI Outstanding request. The maximum number of AXI Outstanding request is 16.

Source AXI Outstanding request limit = Programmed value + 1.

AXI Outstanding is a feature in the AXI protocol that allows to send request before the previous request response is received, thereby increasing the bandwidth of the bus interface.

(R/W)

**DMAC\_CHn\_DST\_OSR\_LMT** Configures the limit of the destination AXI Outstanding request. The maximum number of AXI Outstanding request is 16.

Destination AXI Outstanding request limit = Programmed value + 1.

(R/W)

Register 4.15. DMAC\_CHn\_LLPO\_REG (n: 1-4) (0x0100\*n + 0x0128)



**DMAC\_CHn\_LMS** Selects the AXI master for accessing LLI.

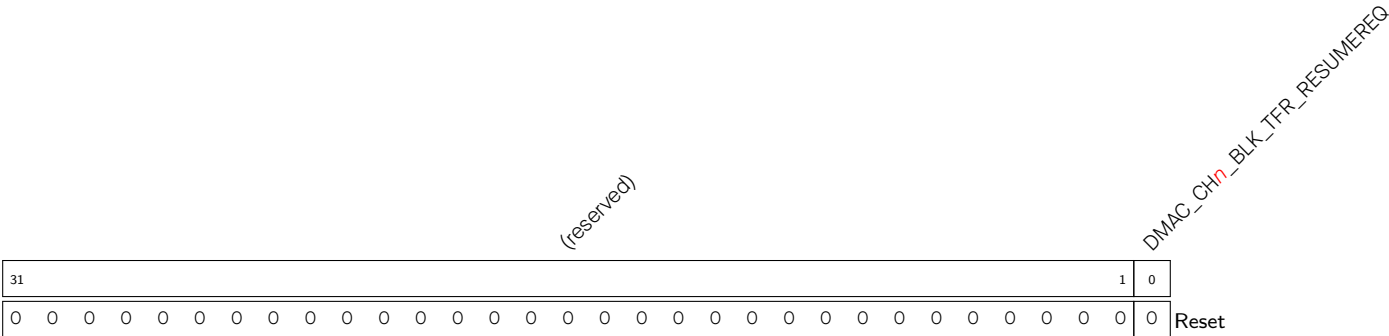
0: AXI Master 1

1: AXI Master 2

(R/W)

**DMAC\_CHn\_LOCO** Configures the starting address of the first linked list item in memory. The six least significant bits (LSB) of the starting address are not stored because it is assumed that the address is 64-byte aligned. (R/W)

Register 4.16. DMAC\_CHn\_BLK\_TFR\_RESUMEREQ0\_REG (n: 1-4) (0x0100\*n + 0x0148)

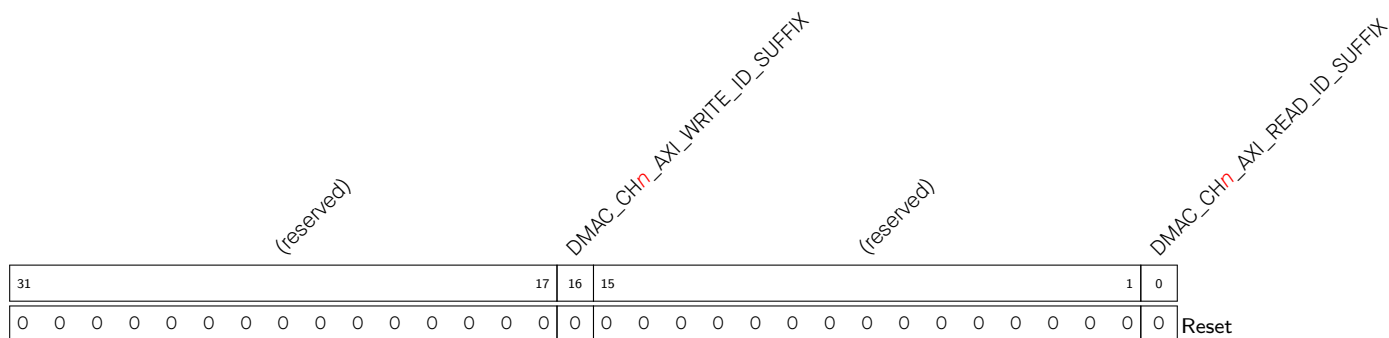


**DMAC\_CHn\_BLK\_TFR\_RESUMEREQ** Configures whether to request to resume block transfer during linked-list or shadow-register-based multi-block transfer.

0: Do not request to resume block transfer

1: Request to resume block transfer

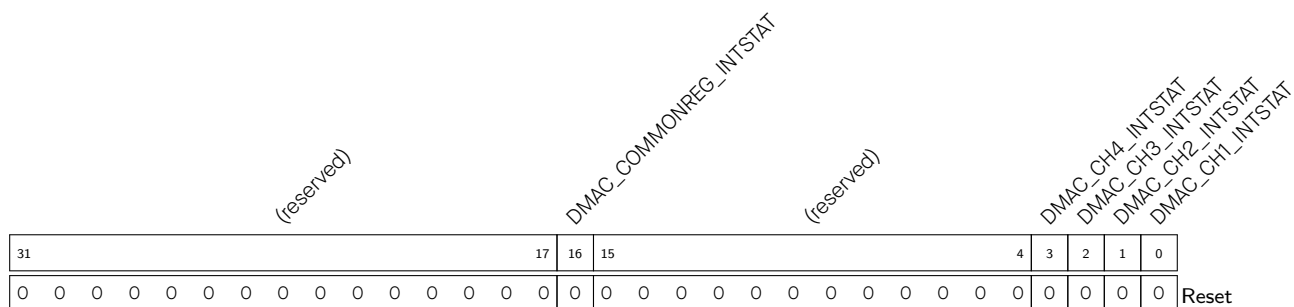
(WO)

Register 4.17. DMAC\_CH $n$ \_AXI\_ID0\_REG (0x0150)

**DMAC\_CH $n$ \_AXI\_READ\_ID\_SUFFIX** Configure the least significant bit of AXI read ID. (R/W)

**DMAC\_CH $n$ \_AXI\_WRITE\_ID\_SUFFIX** Configure the least significant bit of AXI write ID. (R/W)

Register 4.18. DMAC\_INTSTATUS0\_REG (0x0030)



**DMAC\_CH $n$ \_INTSTAT ( $n$ : 1-4)** Indicates the interrupt status for channel  $n$ .

1: Interrupt is active

0: Interrupt is inactive

(RO)

**DMAC\_COMMONREG\_INTSTAT** Indicates the common register interrupt status.

1: Interrupt is active

0: Interrupt is inactive

(RO)

#### Register 4.19. DMAC\_COMMONREG\_INTCLEAR0\_REG (0x0038)

|    |   |   |   |   |   |   |   |   |   |   |
|----|---|---|---|---|---|---|---|---|---|---|
| 31 |   | 9 | 8 | 7 |   | 3 | 2 | 1 | 0 |   |
| 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(reserved)

DMAC\_CLEAR\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT

(reserved)

DMAC\_CLEAR\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT  
DMAC\_CLEAR\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSTAT  
DMAC\_CLEAR\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT

Reset

DMAC\_CLEAR\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT Write 1 to clear  
DMAC\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT. (WO)

**DMAC\_CLEAR\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSTAT** Write 1 to clear [DMAC\\_SLVIF\\_COMMONREG\\_WR2RO\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CLEAR\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT** Write 1 to clear  
DMAC\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT. (WO)

DMAC\_CLEAR\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT Write 1 to clear  
DMAC\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT. (WO)

Register 4.20. DMAC\_COMMONREG\_INTSTATUS\_ENABLE0\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |            |   |   |   |   |   |       |  |   |  |  |  |   |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|------------|---|---|---|---|---|-------|--|---|--|--|--|---|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | DMAC_ENABLE_SLVIF_UNDEFINEDREG_DEC_ERR_INTSTAT |   |   |   | (reserved) |   |   |   | DMAC_ENABLE_SLVIF_COMMONREG_RD2WO_ERR_INTSTAT |   |       |  | DMAC_ENABLE_SLVIF_COMMONREG_WR2RO_ERR_INTSTAT |  |  |  | DMAC_ENABLE_SLVIF_COMMONREG_DEC_ERR_INTSTAT |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9  | 8 | 7 | 3 |            |   |   | 2 | 1   | 0 | Reset |  |   |  |  |  |   |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0 | 0 | 0 | 0          | 0 | 1 | 1 | 1   |   |       |  |   |  |  |  |   |  |  |  |

- DMAC\_ENABLE\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT. (R/W)
- DMAC\_ENABLE\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSTAT

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSTAT. (R/W)
- DMAC\_ENABLE\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT. (R/W)
- DMAC\_ENABLE\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT

Write

1

to

enable

DMAC\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT. (R/W)

Register 4.21. DMAC\_COMMONREG\_INTSIGNAL\_ENABLE0\_REG (0x0048)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |           |   |   |            |   |   |   |   |   |  |  |   |  |  |  |   |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------|---|---|------------|---|---|---|---|---|--|--|---|--|--|--|---|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMAC_ENABLE_SLVIF_UNDEFINEDREG_DEC_ERR_INTSIGNAL |           |   |   | (reserved) |   |   |   | DMAC_ENABLE_SLVIF_COMMONREG_RD2WO_ERR_INTSIGNAL |   |  |  | DMAC_ENABLE_SLVIF_COMMONREG_WR2RO_ERR_INTSIGNAL |  |  |  | DMAC_ENABLE_SLVIF_COMMONREG_DEC_ERR_INTSIGNAL |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9  | 8         | 7 | 3 |            |   |   | 2 | 1   | 0 |  |  |   |  |  |  |   |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1  | 0 0 0 0 0 |   |   |            | 1 | 1 | 1 | Reset   |   |  |  |   |  |  |  |   |  |  |  |

- DMAC\_ENABLE\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSIGNAL

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_DEC\_ERR\_INT at port level. (R/W)
- DMAC\_ENABLE\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSIGNAL

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INT at port level. (R/W)
- DMAC\_ENABLE\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSIGNAL

Write

1

to

enable

DMAC\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INT at port level. (R/W)
- DMAC\_ENABLE\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSIGNAL

Write

1

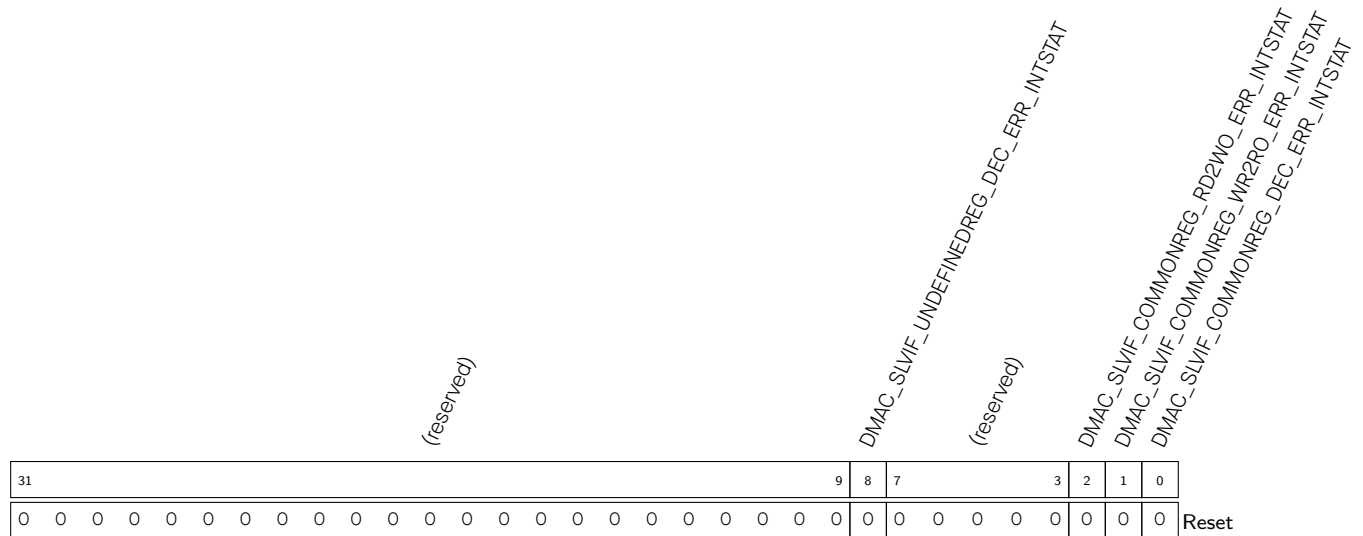
to

enable

DMAC\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INT at port level. (R/W)



#### Register 4.22. DMAC\_COMMONREG\_INTSTATUS0\_REG (0x0050)



**DMAC\_SLVIF\_COMMONREG\_DEC\_ERR\_INTSTAT** Slave interface common register decode error interrupt status bit. This error occurs when VDMA accesses an invalid address in the common register space (0x000 to 0x0FF).

0: No error occurs

1: Error occurs

(RO)

**DMAC\_SLVIF\_COMMONREG\_WR2RO\_ERR\_INTSTAT** Slave interface common register write to read-only error interrupt status bit. This error occurs when a write operation is performed to a read-only register in the common register space (0x000 to 0xFF).

0: No error occurs

1: Error occurs

(RO)

**DMAC\_SLVIF\_COMMONREG\_RD2WO\_ERR\_INTSTAT** Slave interface common register read to write-only error interrupt status bit. This error occurs when a read operation is performed to a write-only register in the common register space (0x000 to 0xFF).

0: No error occurs

1: Error occurs

(RO)

**DMAC\_SLVIF\_UNDEFINEDREG\_DEC\_ERR\_INTSTAT** Slave interface undefined register decode error interrupt signal enable bit. This error occurs when the register access is to undefined address range (>0x4FF).

0: No error occurs

1: Error occurs

(RO)

Register 4.23. DMAC\_CH $n$ \_INTSTATUS\_ENABLE0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0180)

|  |    |    |    |    |  |    |    |    |    |  |    |    |    |    |   |    |    |    |    |  |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|--|----|----|----|----|--|----|----|----|----|---|----|----|----|----|--|----|---|---|---|---|---|---|---|---|---|---|-------|
| DMAC_CH $n$ _ENABLE_CH_ABORTED_INTSTAT   |    |    |    |    | DMAC_CH $n$ _ENABLE_SLVIF_SHADOWREG_WRON_VALID_ERR_INTSTAT |    |    |    |    | DMAC_CH $n$ _ENABLE_SLVIF_SHADOWREG_OR_LLI_INVALID_ERR_INTSTAT |    |    |    |    | DMAC_CH $n$ _ENABLE_SRC_TRANSCOMP_INTSTAT |    |    |    |    | DMAC_CH $n$ _ENABLE_DMA_TFR_DONE_INTSTAT   |    |   |   |   |   |   |   |   |   |   |   |       |
| DMAC_CH $n$ _ENABLE_CH_DISABLED_INTSTAT  |    |    |    |    | DMAC_CH $n$ _ENABLE_SLVIF_WRONCHEN_ERR_INTSTAT             |    |    |    |    | DMAC_CH $n$ _ENABLE_LLI_WR_SLV_ERR_INTSTAT                     |    |    |    |    | DMAC_CH $n$ _ENABLE_DST_TRANSCOMP_INTSTAT |    |    |    |    | DMAC_CH $n$ _ENABLE_BLOCK_TFR_DONE_INTSTAT |    |   |   |   |   |   |   |   |   |   |   |       |
| DMAC_CH $n$ _ENABLE_CH_SUSPENDED_INTSTAT |    |    |    |    | DMAC_CH $n$ _ENABLE_RD2RWO_ERR_INTSTAT                     |    |    |    |    | DMAC_CH $n$ _ENABLE_LLI_RD_SLV_ERR_INTSTAT                     |    |    |    |    | DMAC_CH $n$ _ENABLE_SRC_DEC_ERR_INTSTAT   |    |    |    |    | DMAC_CH $n$ _ENABLE_BLOCK_TFR_DONE_INTSTAT |    |   |   |   |   |   |   |   |   |   |   |       |
| (reserved)                               |    |    |    |    | (reserved)   |    |    |    |    | DMAC_CH $n$ _ENABLE_LLI_WR_DEC_ERR_INTSTAT                     |    |    |    |    | (reserved)                                |    |    |    |    | DMAC_CH $n$ _ENABLE_DMA_TFR_DONE_INTSTAT   |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                                       | 30 | 29 | 28 | 27 | 26   | 25 | 24 | 23 | 22 | 21   | 20 | 19 | 18 | 17 | 16  | 15 | 14 | 13 | 12 | 11   | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1   | 0  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | Reset |

Reset

DMAC\_CH $n$ \_ENABLE\_BLOCK\_TFR\_DONE\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_BLOCK\_TFR\_DONE\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_DMA\_TFR\_DONE\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_DMA\_TFR\_DONE\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_TRANSCOMP\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_SRC\_TRANSCOMP\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_TRANSCOMP\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_DST\_TRANSCOMP\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_DEC\_ERR\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_SRC\_DEC\_ERR\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_DEC\_ERR\_INTSTAT Write 1 to enable DMAC\_CH $n$ \_DST\_DEC\_ERR\_INTSTAT.  
(R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_SLV\_ERR\_INTSTAT Write 1 to enable DMAC\_CH $n$ \_SRC\_SLV\_ERR\_INTSTAT.  
(R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_SLV\_ERR\_INTSTAT Write 1 to enable DMAC\_CH $n$ \_DST\_SLV\_ERR\_INTSTAT.  
(R/W)

DMAC\_CH $n$ \_ENABLE\_LLI\_RD\_DEC\_ERR\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_LLI\_RD\_DEC\_ERR\_INTSTAT. (R/W)

DMAC\_CH $n$ \_ENABLE\_LLI\_WR\_DEC\_ERR\_INTSTAT Write 1 to enable  
DMAC\_CH $n$ \_LLI\_WR\_DEC\_ERR\_INTSTAT. (R/W)

Continued on the next page...

Register 4.23. DMAC\_CH $n$ \_INTSTATUS\_ENABLE0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0180)

Continued from the previous page...

DMAC\_CH $n$ \_ENABLE\_LLI\_RD\_SLV\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_LLI\\_RD\\_SLV\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_LLI\_WR\_SLV\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_LLI\\_WR\\_SLV\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SHADOWREG\\_OR\\_LLI\\_INVALID\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_MULTIBLKTYPE\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_MULTIBLKTYPE\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_DEC\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_DEC\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_WR2RO\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_WR2RO\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_RD2RWO\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_RD2RWO\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_WRONCHEN\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_WRONCHEN\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_SLVIF\_SHADOWREG\_WRON\_VALID\_ERR\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SLVIF\\_SHADOWREG\\_WRON\\_VALID\\_ERR\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_CH\_SRC\_SUSPENDED\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_CH\\_SRC\\_SUSPENDED\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_CH\_SUSPENDED\_INTSTAT Write 1 to enable  
[DMAC\\_CH \$n\$ \\_CH\\_SUSPENDED\\_INTSTAT](#). (R/W)

DMAC\_CH $n$ \_ENABLE\_CH\_DISABLED\_INTSTAT Write 1 to enable [DMAC\\_CH \$n\$ \\_CH\\_DISABLED\\_INTSTAT](#).  
 (R/W)

DMAC\_CH $n$ \_ENABLE\_CH\_ABORTED\_INTSTAT Write 1 to enable [DMAC\\_CH \$n\$ \\_CH\\_ABORTED\\_INTSTAT](#).  
 (R/W)

Register 4.24. DMAC\_CH $n$ \_INTSTATUSO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0188)

|   |    |    |    |    |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|---|----|----|----|----|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| <div>DMAC_CH<sub>n</sub>_CH_ABORTED_INTSTAT<br/>DMAC_CH<sub>n</sub>_CH_DISABLED_INTSTAT<br/>DMAC_CH<sub>n</sub>_CH_SUSPENDED_INTSTAT<br/>DMAC_CH<sub>n</sub>_CH_SRC_SUSPENDED_INTSTAT<br/><br/>(reserved)<br/><br/>DMAC_CH<sub>n</sub>_SLVIF_SHADOWREG_WRON_VALID_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_SLVIF_WRONCHEN_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_SLVIF_RD2RWO_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_SLVIF_WR2RO_ERR_INTSTAT<br/>(reserved)<br/>DMAC_CH<sub>n</sub>_SLVIF_DEC_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_SLVIF_MULTIBLKTYPE_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_LLI_WR_SLV_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_LLI_RD_SLV_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_LLI_WR_DEC_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_DST_DEC_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_SRC_SLV_ERR_INTSTAT<br/>DMAC_CH<sub>n</sub>_DST_DEC_ERR_INTSTAT<br/>(reserved)<br/>DMAC_CH<sub>n</sub>_SRC_TRANSCOMP_INTSTAT<br/>DMAC_CH<sub>n</sub>_DMA_TFR_DONE_INTSTAT<br/>DMAC_CH<sub>n</sub>_BLOCK_TFR_DONE_INTSTAT</div> |    |    |    |    |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| 31  | 30 | 29 | 28 | 27 |   |   |   |   |   |   |   | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| 0   | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset   |    |    |    |    |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

Reset

**DMAC\_CH $n$ \_BLOCK\_TFR\_DONE\_INTSTAT** Block transfer done status bit. (RO)

**DMAC\_CH $n$ \_DMA\_TFR\_DONE\_INTSTAT** DMA transfer done status bit. (RO)

**DMAC\_CH $n$ \_SRC\_TRANSCOMP\_INTSTAT** Source DMA transfer completed status bit. (RO)

**DMAC\_CH $n$ \_DST\_TRANSCOMP\_INTSTAT** Destination DMA transfer completed status bit. (RO)

**DMAC\_CH $n$ \_SRC\_DEC\_ERR\_INTSTAT** Source decode error status bit. The decode error is detected by the master interface during source transfer. (RO)

**DMAC\_CH $n$ \_DST\_DEC\_ERR\_INTSTAT** Destination decode error status bit. The decode error is detected by the master interface during destination transfer. (RO)

**DMAC\_CH $n$ \_SRC\_SLV\_ERR\_INTSTAT** Source slave error status bit. The slave error is detected by the master interface during source transfer. This error occurs if the slave interface that reads data issues a slave error. (RO)

**DMAC\_CH $n$ \_DST\_SLV\_ERR\_INTSTAT** Destination slave error status bit. The slave error is detected by the master interface during source transfer. This error occurs if the slave interface that writes data issues a slave error. (RO)

**DMAC\_CH $n$ \_LLI\_RD\_DEC\_ERR\_INTSTAT** LLI read decode error status bit. The decode error is detected by the master interface during LLI read operation. (RO)

**DMAC\_CH $n$ \_LLI\_WR\_DEC\_ERR\_INTSTAT** LLI write decode error status bit. The decode error is detected by the master interface during LLI write-back operation. (RO)

**DMAC\_CH $n$ \_LLI\_RD\_SLV\_ERR\_INTSTAT** LLI read slave error status bit. The slave error is detected by the master interface during LLI read operation. (RO)

**DMAC\_CH $n$ \_LLI\_WR\_SLV\_ERR\_INTSTAT** LLI write slave error status bit. The slave error is detected by the master interface during LLI write-back operation. (RO)

Continued on the next page...

**Register 4.24. DMAC\_CH $n$ \_INTSTATUSO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0188)**

Continued from the previous page...

**DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INTSTAT** Shadow register or LLI invalid error status bit. This error occurs if **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** is 0 during VDMA shadow register/LLI fetch phase. (RO)

**DMAC\_CH $n$ \_SLVIF\_MULTIBLKTYPE\_ERR\_INTSTAT** Slave interface multi-block type error status bit. This error occurs if multi-block transfer type programmed in **DMAC\_CH $n$ \_SRC\_MULTBLK\_TYPE** and **DMAC\_CH $n$ \_DST\_MULTBLK\_TYPE** is invalid. (RO)

**DMAC\_CH $n$ \_SLVIF\_DEC\_ERR\_INTSTAT** Slave interface decode error status bit. The decode error is generated by VDMA during register access. This error occurs if the register access is to invalid address in channel  $n$ . (RO)

**DMAC\_CH $n$ \_SLVIF\_WR2RO\_ERR\_INTSTAT** Slave interface write to read-only error status bit. This error occurs if write operation is performed to a read-only register. (RO)

**DMAC\_CH $n$ \_SLVIF\_RD2RWO\_ERR\_INTSTAT** Slave interface read to write-only error status bit. This error occurs if read operation is performed to a write-only register. (RO)

**DMAC\_CH $n$ \_SLVIF\_WRONCHEN\_ERR\_INTSTAT** Slave interface write to enable channel error status bit. This error occurs if an illegal write operation is performed on a register as per the VDMA specification. (RO)

**DMAC\_CH $n$ \_SLVIF\_SHADOWREG\_WRON\_VALID\_ERR\_INTSTAT** Shadow register write on valid error status bit. This error occurs if shadow register based multi-block transfer is enabled and software tries to write to the shadow register when **DMAC\_CH $n$ \_SHADOWREG\_OR\_LLI\_VALID** bit is 1. (RO)

**DMAC\_CH $n$ \_CH\_SRC\_SUSPENDED\_INTSTAT** Channel source suspended status bit.  
 0: Channel source is not suspended.  
 1: Channel Source is suspended.  
 (RO)

**DMAC\_CH $n$ \_CH\_SUSPENDED\_INTSTAT** Channel suspended status bit.  
 0: Channel is not suspended.  
 1: Channel is suspended.  
 (RO)

**DMAC\_CH $n$ \_CH\_DISABLED\_INTSTAT** Channel disabled status bit.  
 0: Channel is not disabled.  
 1: Channel is disabled.  
 (RO)

**DMAC\_CH $n$ \_CH\_ABORTED\_INTSTAT** Channel aborted status bit.  
 0: Channel is not aborted.  
 1: Channel is aborted.  
 (RO)

Register 4.25. DMAC\_CH $n$ \_INTSIGNAL\_ENABLE0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0190)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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| DMAC_CH $n$ _ENABLE_CH_SRC_SUSPENDED_INTSIGNAL |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_SLVIF_WR2RO_ERR_INTSIGNAL                |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_SRC_SLV_ERR_INTSIGNAL |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_BLOCK_TFR_DONE_INTSIGNAL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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| (reserved)                                     |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_SLVIF_DEC_ERR_INTSIGNAL                  |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_SRC_SLV_ERR_INTSIGNAL |  |  |  |  |  |  |  |  |  | DMAC_CH $n$ _ENABLE_BLOCK_TFR_DONE_INTSIGNAL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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DMAC\_CH $n$ \_ENABLE\_BLOCK\_TFR\_DONE\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_BLOCK\\_TFR\\_DONE\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_DMA\_TFR\_DONE\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_DMA\\_TFR\\_DONE\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_TRANSCOMP\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SRC\\_TRANSCOMP\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_TRANSCOMP\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_DST\\_TRANSCOMP\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_DEC\_ERR\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_SRC\\_DEC\\_ERR\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_DEC\_ERR\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_DST\\_DEC\\_ERR\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_SRC\_SLV\_ERR\_INTSIGNAL Write 1 to enable [DMAC\\_CH \$n\$ \\_SRC\\_SLV\\_ERR\\_INT](#)  
 at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_DST\_SLV\_ERR\_INTSIGNAL Write 1 to enable [DMAC\\_CH \$n\$ \\_DST\\_SLV\\_ERR\\_INT](#)  
 at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_LLI\_RD\_DEC\_ERR\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_LLI\\_RD\\_DEC\\_ERR\\_INT](#) at port level. (R/W)

DMAC\_CH $n$ \_ENABLE\_LLI\_WR\_DEC\_ERR\_INTSIGNAL Write 1 to enable  
[DMAC\\_CH \$n\$ \\_LLI\\_WR\\_DEC\\_ERR\\_INT](#) at port level. (R/W)

Continued on the next page...

**Register 4.25. DMAC\_CH $n$ \_INTSIGNAL\_ENABLE0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0190)**

Continued from the previous page...

|  |  |   |    |        |
|--|--|---|----|--------|
| DMAC_CH $n$ _ENABLE_LLI_RD_SLV_ERR_INTSIGNAL                         | Write  | 1 | to | enable |
| DMAC_CH $n$ _LLI_RD_SLV_ERR_INT at port level. (R/W)                 |  |   |    |        |
| DMAC_CH $n$ _ENABLE_LLI_WR_SLV_ERR_INTSIGNAL                         | Write  | 1 | to | enable |
| DMAC_CH $n$ _LLI_WR_SLV_ERR_INT at port level. (R/W)                 |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SHADOWREG_OR_LLI_INVALID_ERR_INTSIGNAL           | Write  | 1 | to | enable |
| DMAC_CH $n$ _SHADOWREG_OR_LLI_INVALID_ERR_INT at port level. (R/W)   |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_MULTIBLKTYPE_ERR_INTSIGNAL                 | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_MULTIBLKTYPE_ERR_INT at port level. (R/W)         |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_DEC_ERR_INTSIGNAL                          | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_DEC_ERR_INT at port level. (R/W)                  |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_WR2RO_ERR_INTSIGNAL                        | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_WR2RO_ERR_INT at port level. (R/W)                |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_RD2RWO_ERR_INTSIGNAL                       | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_RD2RWO_ERR_INT at port level. (R/W)               |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_WRONCHEN_ERR_INTSIGNAL                     | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_WRONCHEN_ERR_INT at port level. (R/W)             |  |   |    |        |
| DMAC_CH $n$ _ENABLE_SLVIF_SHADOWREG_WRON_VALID_ERR_INTSIGNAL         | Write  | 1 | to | enable |
| DMAC_CH $n$ _SLVIF_SHADOWREG_WRON_VALID_ERR_INT at port level. (R/W) |  |   |    |        |
| DMAC_CH $n$ _ENABLE_CH_SRC_SUSPENDED_INTSIGNAL                       | Write  | 1 | to | enable |
| DMAC_CH $n$ _CH_SRC_SUSPENDED_INT at port level. (R/W)               |  |   |    |        |
| DMAC_CH $n$ _ENABLE_CH_SUSPENDED_INTSIGNAL                           | Write  | 1 | to | enable |
| DMAC_CH $n$ _CH_SUSPENDED_INT at port level. (R/W)                   |  |   |    |        |
| DMAC_CH $n$ _ENABLE_CH_DISABLED_INTSIGNAL                            | Write  | 1 | to | enable |
| DMAC_CH $n$ _CH_DISABLED_INT at port level. (R/W)                    |  |   |    |        |
| DMAC_CH $n$ _ENABLE_CH_ABORTED_INTSIGNAL                             | Write 1 to enable DMAC_CH $n$ _CH_ABORTED_INT at port level. (R/W) |   |    |        |

Register 4.26. DMAC\_CH*n*\_INTCLEARO\_REG (*n*: 1-4) (0x0100\**n* + 0x0198)

[illegible]

DMAC\_CHn\_CLEAR\_BLOCK\_TFR\_DONE\_INTSTAT Write 1 to clear  
DMAC\_CHn\_BLOCK\_TFR\_DONE\_INTSTAT. (WO)

**DMAC\_CHn\_CLEAR\_DMA\_TFR\_DONE\_INTSTAT** Write 1 to clear **DMAC\_CHn\_DMA\_TFR\_DONE\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_SRC\_TRANSCOMP\_INTSTAT** Write 1 to clear **DMAC\_CHn\_SRC\_TRANSCOMP\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_DST\_TRANSCOMP\_INTSTAT** Write 1 to clear **DMAC\_CHn\_DST\_TRANSCOMP\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_SRC\_DEC\_ERR\_INTSTAT** Write 1 to clear **DMAC\_CHn\_SRC\_DEC\_ERR\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_DST\_DEC\_ERR\_INTSTAT** Write 1 to clear **DMAC\_CHn\_DST\_DEC\_ERR\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_SRC\_SLV\_ERR\_INTSTAT** Write 1 to clear **DMAC\_CHn\_SRC\_SLV\_ERR\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_DST\_SLV\_ERR\_INTSTAT** Write 1 to clear **DMAC\_CHn\_DST\_SLV\_ERR\_INTSTAT**.  
(WO)

**DMAC\_CHn\_CLEAR\_LLI\_RD\_DEC\_ERR\_INTSTAT** Write 1 to clear **DMAC\_CHn\_LLI\_RD\_DEC\_ERR\_INTSTAT**.  
(WO)

DMAC\_CHn\_CLEAR\_LLI\_WR\_DEC\_ERR\_INTSTAT Write 1 to clear DMAC\_CHn\_LLI\_WR\_DEC\_ERR\_INTSTAT.  
(WO)

Continued on the next page...



**Register 4.26. DMAC\_CH $n$ \_INTCLEAR0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0198 )**

Continued from the previous page...

**DMAC\_CH $n$ \_CLEAR\_LLI\_RD\_SLV\_ERR\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_LLI\\_RD\\_SLV\\_ERR\\_INTSTAT](#).  
(WO)

**DMAC\_CH $n$ \_CLEAR\_LLI\_WR\_SLV\_ERR\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_LLI\\_WR\\_SLV\\_ERR\\_INTSTAT](#).  
(WO)

**DMAC\_CH $n$ \_CLEAR\_SHADOWREG\_OR\_LLI\_INVALID\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SHADOWREG\\_OR\\_LLI\\_INVALID\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_MULTIBLKTYPE\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SLVIF\\_MULTIBLKTYPE\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_DEC\_ERR\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_SLVIF\\_DEC\\_ERR\\_INTSTAT](#).  
(WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_WR2RO\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SLVIF\\_WR2RO\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_RD2RWO\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SLVIF\\_RD2RWO\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_WRONCHEN\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SLVIF\\_WRONCHEN\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_SLVIF\_SHADOWREG\_WRON\_VALID\_ERR\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_SLVIF\\_SHADOWREG\\_WRON\\_VALID\\_ERR\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_CH\_SRC\_SUSPENDED\_INTSTAT** Write 1 to clear  
[DMAC\\_CH \$n\$ \\_CH\\_SRC\\_SUSPENDED\\_INTSTAT](#). (WO)

**DMAC\_CH $n$ \_CLEAR\_CH\_SUSPENDED\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_CH\\_SUSPENDED\\_INTSTAT](#).  
(WO)

**DMAC\_CH $n$ \_CLEAR\_CH\_DISABLED\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_CH\\_DISABLED\\_INTSTAT](#).  
(WO)

**DMAC\_CH $n$ \_CLEAR\_CH\_ABORTED\_INTSTAT** Write 1 to clear [DMAC\\_CH \$n\$ \\_CH\\_ABORTED\\_INTSTAT](#).  
(WO)

**Register 4.27. DMAC\_CH $n$ \_STATUS0\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0130)**

|            |   |   |   |   |   |   |   |   |   |   |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   | DMAC_CH <sub>n</sub> _CMPLTD_BLK_TFR_SIZE |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   | 22  | 21 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000                                    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**DMAC\_CH $n$ \_CMPLTD\_BLK\_TFR\_SIZE** Indicates the total number of data of width **DMAC\_CH $n$ \_SRC\_TR\_WIDTH** transferred during the previous block transfer.

If any error occurs during DMA transfer, the block transfer might be terminated early. In such case, the value of this field indicates the actual data transferred without error in the current block.

This field is cleared to 0 when the channel is enabled.

(RO)

**Register 4.28. DMAC\_CH $n$ \_STATUS1\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0134)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  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 |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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 |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0</ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**DMAC\_CH $n$ \_DATA\_LEFT\_IN\_FIFO** Indicates the total number of remaining data in the VDMA channel FIFO after completing the current block transfer.

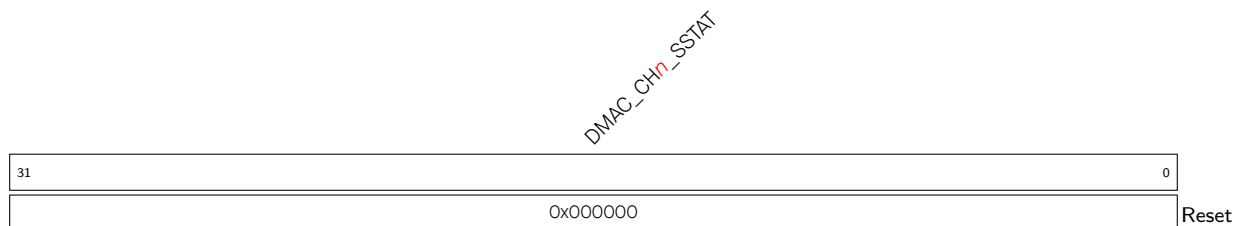
The data width in the channel FIFO is **DMAC\_CH $n$ \_SRC\_TR\_WIDTH**.

For a normal block transfer completion without errors, the value of this field is 0. If any errors occur during DMA transfer, the block transfer may be terminated early; in this case, this field indicates the remaining data in the channel FIFO that cannot be transferred to the target peripheral.

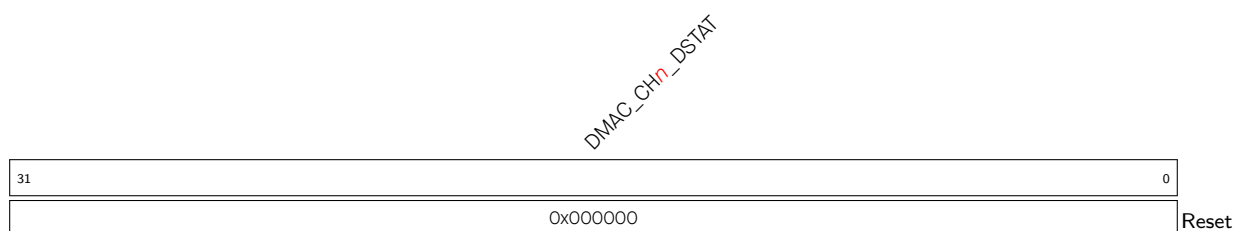
This field will be cleared when the channel is enabled.

If **DMAC\_CH $n$ \_DST\_TR\_WIDTH** > **DMAC\_CH $n$ \_SRC\_TR\_WIDTH**, there may be remaining data in the FIFO that is not enough to form a single transfer of **DMAC\_CH $n$ \_SRC\_TR\_WIDTH** width; in this case, this field will return 0.

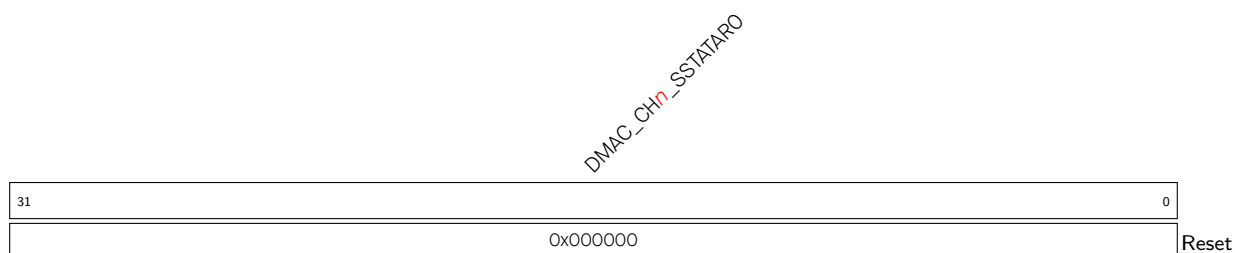
(RO)

**Register 4.29. DMAC\_CH $n$ \_SSTATO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0160)**

**DMAC\_CH $n$ \_SSTAT** Indicates the source status information retrieved by hardware from the address pointed to by [DMAC\\_CH \$n\$ \\_SSTATARO\\_REG](#). (RO)

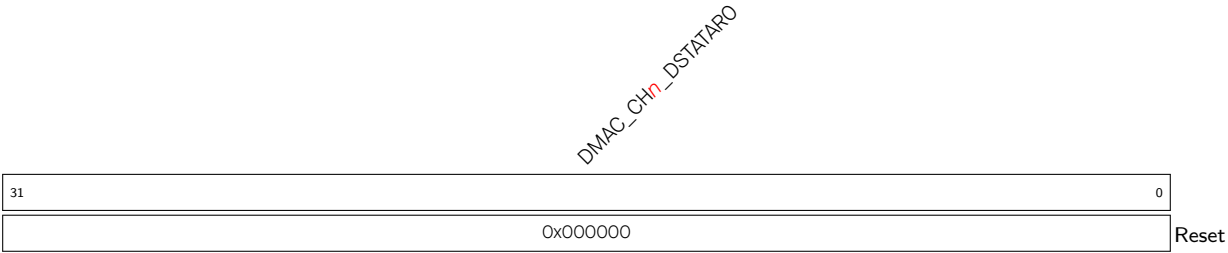
**Register 4.30. DMAC\_CH $n$ \_DSTATO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0168)**

**DMAC\_CH $n$ \_DSTAT** Indicates the destination status information retrieved by hardware from the address pointed to by [DMAC\\_CH \$n\$ \\_DSTATARO\\_REG](#). (RO)

**Register 4.31. DMAC\_CH $n$ \_SSTATARO\_REG ( $n$ : 1-4) (0x0100\* $n$  + 0x0170)**

**DMAC\_CH $n$ \_SSTATARO** Configures the address from where the hardware obtains the source status information. (R/W)

Register 4.32. DMAC\_CHn\_DSTATARO\_REG (n: 1-4) (0x0100\*n + 0x0178)



**DMAC\_CHn\_DSTATARO** Configures the address from where the hardware obtains the destination status information. (R/W)

## Chapter 5

### 2D-DMA Controller (2D-DMA)

#### 5.1 Overview

The 2D-DMA controller is a DMA (Direct Memory Access) dedicated to two-dimensional image processing. In addition to all the features of GDMA-AXI, it includes support for macroblock reordering and color space conversion (CSC) to better meet the data transfer requirements from JPEG and PPA. Notably, the 2D-DMA facilitates memory-to-memory transfers, enabling the movement of macroblocks between different segments of memory address space while concurrently performing color space conversion.

#### 5.2 Features

- One AXI master interface
- Data transfer with unaligned starting addresses
- Memory-to-memory, peripheral-to-memory (RX), and memory-to-peripheral (TX) data transfer
- Three memory-to-peripheral channels, and two peripheral-to-memory channels
- Support for PPA and JPEG Codec
- Macroblock reordering
- Color space conversion
- Configurable channel priority and weight

#### 5.3 Architecture

In ESP32-P4, only JPEG Codec and PPA support 2D-DMA. The 2D-DMA controller and CPU data bus have access to the same address space in memory. Figure 5.3-1 shows the basic architecture of the 2D-DMA controller.

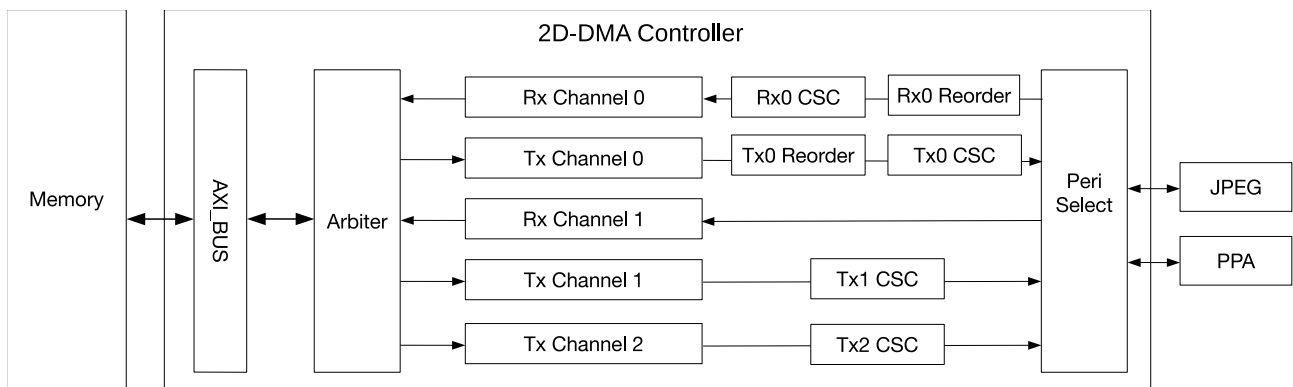


Figure 5.3-1. 2D-DMA Architecture

The 2D-DMA has five independent channels: three transmit channels and two receive channels. Every channel can be connected to different peripherals, or in other words shared by peripherals.

The macroblock reordering and color space conversion features of the 2D-DMA are not supported by all channels. Among the five channels, transmit channel 0 and receive channel 0 support macroblock reordering, while transmit channel 0 ~ 2 and receive channel 0 support color space conversion.

The 2D-DMA reads data from or writes data to the internal or external memory via AXI\_BUS. Before the data transfer, the 2D-DMA uses configurable arbitration schemes for channels requesting read or write access. For the available address range of internal and external memory, please see Chapter 6 [System and Memory](#).

The software can use the 2D-DMA through linked lists stored in internal or external memory. These linked lists consist of `outlinkn` and `inlinkn`, where `n` indicates the channel number. For `outlinkn`, `n` ranges from 0 to 2; for `inlinkn`, `n` is 0 or 1. The 2D-DMA reads an `outlinkn` (i.e., a linked list of transmit descriptors) from memory and transmit data in corresponding memory according to the `outlinkn`, or read an `inlinkn` (i.e., a linked list of receive descriptors) and store received data into specific address space in memory according to the `inlinkn`.

## 5.4 Functional Description

### 5.4.1 Transfer Mode

The 2D-DMA supports four transfer modes:

- 1D mode: enabled by setting the 2DEN field of DW0 and the mod field of DW2 to 0. In this mode, the 2D-DMA has the same functionalities as GDMA-AXI: it performs memory read/write operations based on the data length and memory space configured in the linked list, and the operation addresses are contiguous.
- 2D-MOD0 mode: enabled by setting the 2DEN field of DW0 to 1 and the mod field of DW2 to 0. In this mode, the 2D-DMA reads or writes a `hb*vb` macroblock starting from the (X, Y) coordinates of the HA\*VA image. After the last data in each row has been read or written, the address jumps to the address of the first data in the next row to be read or written.
- 2D-MOD1 mode: enabled by setting the 2DEN field of DW0 to 1 and the mod field of DW2 to 1. In this mode, the 2D-DMA reads or writes multiple macroblocks from the starting address of the HA\*VA image until the HA\*VA image has been fully read or written. For JPEG, it is necessary to configure `DMA2D_IN_MACRO_BLOCK_SIZE_CHn` or `DMA2D_OUT_MACRO_BLOCK_SIZE_CHn` to choose a

macroblock size out of the three available options (horizontal × vertical): 8 pixels × 8 pixels, 8 pixels × 16 pixels, and 16 pixels × 16 pixels. For more information about macroblock size, see Chapter 31 [JPEG Codec](#). For correspondence between macroblock size, hb, and vb of descriptors, see Table 5.4-4 and Table 5.4-5.

- DSCR-PORT mode: enabled by setting the 2DEN field of DW0 to 1, the mod field of DW2 to 0, and the [DMA2D\\_OUT\\_DSCR\\_PORT\\_EN\\_CHn](#) bit or the [DMA2D\\_IN\\_DSCR\\_PORT\\_EN\\_CHn](#) bit to 1. This mode is specifically designed for PPA. For details, see Chapter 33 [Pixel-Processing Accelerator \(PPA\)](#).

1D Mode, 2D-MOD0 Mode, 2D-MOD1 Mode, and DSCR-PORT support both peripheral-to-memory and memory-to-peripheral data transfers. Only 1D Mode and 2D-MOD0 Mode support memory-to-memory data transfers.

5.4.2 Linked List

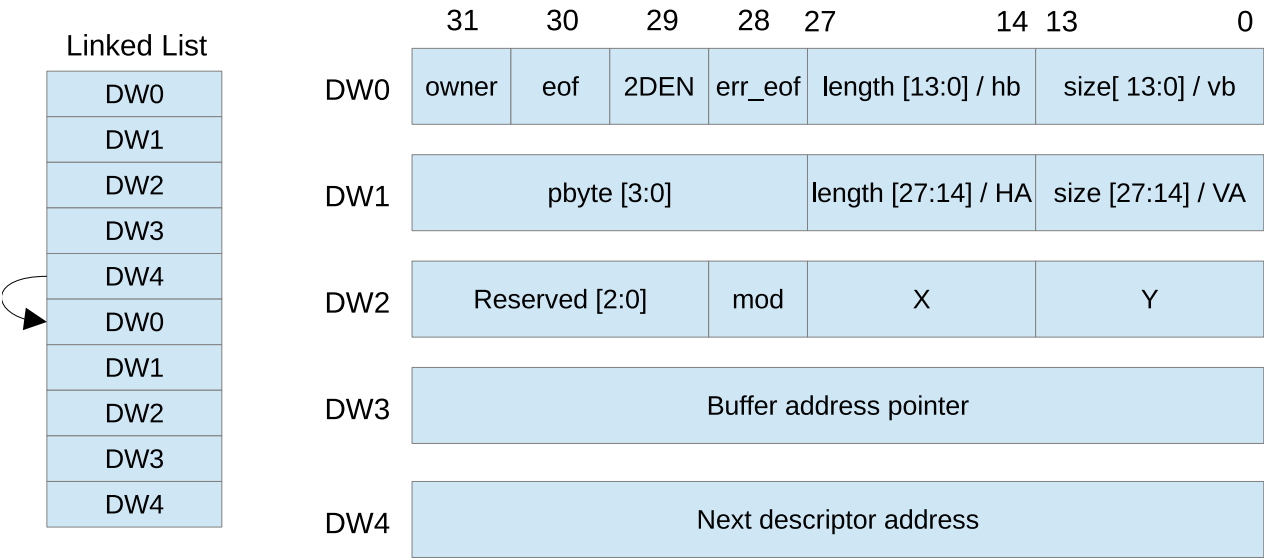


Figure 5.4-1. Structure of a Linked List

Figure 5.4-1 shows the structure of a linked list. An outlink and an inlink have the same structure. A linked list is formed by one or more descriptors, and each descriptor consists of five words. Linked lists should be stored in the memory for the 2D-DMA to be able to use them. The meanings of a descriptor’s fields are shown in Table 5.4-1.

**Note:** DMA2D\_OUT is the prefix of transmit channel registers, and DMA2D\_IN is the prefix of receive channel registers.

Table 5.4-1. Descriptor Field Description

| Bits       | Name            | Description  |
|------------|-----------------|--|
| DWO[31]    | owner           | <p>Specifies who is allowed to access the buffer that this descriptor points to.</p> <ul style="list-style-type: none"> <li>• 0: CPU can access the buffer</li> <li>• 1: The 2D-DMA controller can access the buffer</li> </ul> <p>When the 2D-DMA controller stops using the buffer, this bit in a receive descriptor is automatically cleared by hardware, while this bit in a transmit descriptor can only be automatically cleared by hardware if <code>DMA2D_OUT_AUTO_WRBCK_CHn</code> is set to 1. When software loads a linked list, this bit should be set to 1.</p> |
| DWO[30]    | eof             | <p>Specifies the end of frame.</p> <ul style="list-style-type: none"> <li>• 0: The current descriptor is not the last descriptor of an image</li> <li>• 1: The current descriptor is the last descriptor of an image</li> </ul> <p>For receive descriptors, software needs to write 0 to this bit first, and hardware would set this bit to 1 after receiving a complete image. For transmit descriptors, software should set this bit in the last descriptor of an image to 1.</p>  |
| DWO[29]    | 2DEN            | <p>Specifies whether to enable 2D functions.</p> <ul style="list-style-type: none"> <li>• 0: 2D-DMA operates in 1D mode</li> <li>• 1: 2D-DMA operates in 2D mode</li> </ul>  |
| DWO[28]    | err_eof         | <p>Specifies whether the received data has errors (JPEG only).</p> <ul style="list-style-type: none"> <li>• 0: The received data does not have errors</li> <li>• 1: The received data has errors</li> </ul> <p>For receive descriptors, the hardware sets this bit to 1 after receiving a complete image and detecting errors in the received data.</p>  |
| DWO[27:14] | length[13:0]/hb | <p><b>hb</b> in 2D mode – Specifies the horizontal width of the macroblocks to be moved in the unit of pixels.</p> <p><b>length[13:0]</b> in 1D mode – Specifies the lower 14 bits of length, which is the number of valid bytes in the buffer that this descriptor points to. This field in a transmit descriptor is written by software and indicates how many bytes can be read from the buffer; this field in a receive descriptor is written by hardware automatically and indicates how many valid bytes have been stored in the buffer.</p>                           |
| DWO[13:0]  | size[13:0]/vb   | <p><b>vb</b> in 2D mode – Specifies the vertical height of the macroblocks to be moved in the unit of pixels.</p> <p><b>size[13:0]</b> in 1D mode – Specifies the lower 14 bits of size, which is the capacity of the buffer that this descriptor points to in the unit of bytes.</p>  |



| Bits       | Name                   | Description  |
|------------|------------------------|--|
| DW1[31:28] | pbyte                  | <p>In 2D mode, specifies the number of bytes per pixel of the image to be transferred to/from the memory. (If color space conversion is applied, this field represents the number of bytes per pixel of the image stored in the memory.)</p> <ul style="list-style-type: none"> <li>• 0: 0.5 byte/pixel</li> <li>• 1: 1 byte/pixel</li> <li>• 2: 1.5 bytes/pixel</li> <li>• 3: 2 bytes/pixel</li> <li>• 4: 3 bytes/pixel</li> <li>• 5: 4 bytes/pixel</li> </ul> <p>In 1D mode, this field is not used and can be any value.</p>  |
| DW1[27:14] | length[27:14]/HA       | <p><b>HA</b> in 2D mode – Specifies the horizontal width of the original image corresponding to the macroblocks to be moved in the unit of pixels.</p> <p><b>length[27:14]</b> in 1D mode – Specifies the higher 14 bits of length.</p>  |
| DW1[13:0]  | size[27:14]/VA         | <p><b>VA</b> in 2D mode – Specifies the vertical height of the original image corresponding to the macroblocks to be moved in the unit of pixels.</p> <p><b>size[27:14]</b> in 1D mode – Specifies the higher 14 bits of size.</p>   |
| DW2[31:29] | Reserved               | Reserved. Irrelevant.  |
| DW2[28]    | mod                    | <p>Specifies the macroblock read mode.</p> <ul style="list-style-type: none"> <li>• 0: 2D-DMA reads or writes a single macroblock with horizontal width hb and vertical height vb only once</li> <li>• 1: 2D-DMA reads or writes multiple macroblocks with horizontal width hb and vertical height vb until the image data with horizontal width HA and vertical height VA is fully read or written</li> </ul> <p>In 1D mode, this bit must be 0.</p> <div style="border: 1px solid black; padding: 5px; margin-top: 10px;"> <p><b>Note:</b><br/>hb/vb/HA/VA are in the unit of pixels.</p> </div> |
| DW2[27:14] | X                      | <p>In 2D mode, specifies the X coordinate of the hb*vb image block within the HA*VA image in the unit of pixels.</p> <p>In 1D mode, this field is not used and can be any value.</p>   |
| DW2[13:0]  | Y                      | <p>In 2D mode, specifies the Y coordinate of the hb*vb image block within the HA*VA image in the unit of pixels.</p> <p>In 1D mode, this field is not used and can be any value.</p>   |
| DW3        | Buffer address pointer | <p>In 2D mode, specifies the address of the HA*VA image block origin in the buffer (the address of the original image's first byte in the memory).</p> <p>In 1D mode, specifies the starting address of the buffer.</p>  |

| Bits | Name                    | Description  |
|------|-------------------------|--|
| DW4  | Next descriptor address | <p>Address of the next descriptor. If the current descriptor is the last descriptor in the linked list, this value can be 0. This address can point to the address space of internal or external memory.</p> <div style="border: 1px solid black; padding: 5px;"> <p><b>Note:</b><br/>The starting address for storing 2D-DMA descriptors must be 8-byte aligned.</p> </div> |

### 5.4.3 Padding in 2D-MOD1 Mode and DSCR-PORT Mode

This section only applies to the TX direction of 2D-DMA transfers in 2D-MOD1 and DSCR-PORT mode.

For JPEG decoding, the basic unit of image data input is a block of 8x8, 8x16, or 16x16 (pixels). In 2D-MOD1 mode, when the length and width of the image are not integer multiples of the basic unit, the image needs to pad out to integer multiples of the basic unit based on the previous or the current macroblock.

For PPA, the basic unit for transmit channels in DSCR-PORT mode is 20x20 (YUV420) or 18x18. The width and height of a basic unit for different transmit channels are configured using

[DMA2D\\_OUT\\_DSCR\\_PORT\\_BLK\\_H\\_CH \$n\$](#)  and [DMA2D\\_OUT\\_DSCR\\_PORT\\_BLK\\_V\\_CH \$n\$](#) . When the length and width of the image are not integer multiples of the basic unit, the image needs to pad out.

Below are the padding rules rules:

- Horizontally, the padding depends on the pbyte field of DW1.
  - When pbyte is 0 (0.5 byte/pixel), the remaining pixels must be even, and the padding is the last 0.5 byte.
  - When pbyte is 1 (1 byte/pixel), the padding is the last 1 byte.
  - When pbyte is 2 (1.5 bytes/pixel), the remaining pixels must be even, and the padding is the last 3 bytes.
  - When pbyte is 3 (2 bytes/pixel), the padding is the last 2 bytes.
  - When pbyte is 4 (3 bytes/pixel), the padding is the last 3 bytes.
  - When pbyte is 5 (4 bytes/pixel), the padding is the last 4 bytes.
- Vertically, the padding is the last row.

Figure 5.4-2 and Figure 5.4-3 illustrate the padding method.

In Figure 5.4-2, a blue grid represents a basic unit (a block of 8x8, 8x16, or 16x16 pixels), and a yellow box (incomplete basic unit) along with a green box (padding) forms a basic unit.

In Figure 5.4-3, a grid represents one pixel, and the numbers inside each grid represent pixel values.

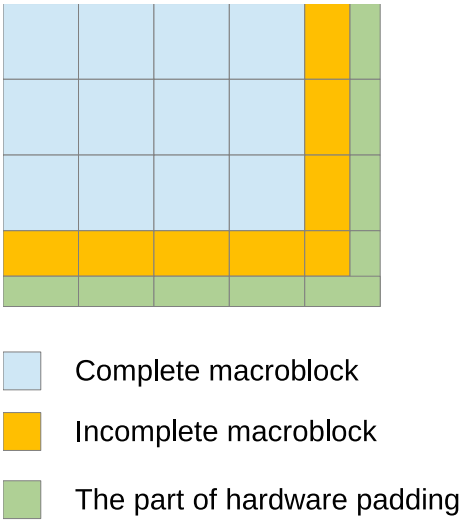


Figure 5.4-2. Padding Illustration (Overall)

|   |   |   |   |   |   |   |   |
|---|---|---|---|---|---|---|---|
| 1 | 2 | 3 | 3 | 3 | 3 | 3 | 3 |
| 4 | 5 | 6 | 6 | 6 | 6 | 6 | 6 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |
| 7 | 8 | 9 | 9 | 9 | 9 | 9 | 9 |

Figure 5.4-3. Padding Illustration (Detail)

5.4.4 Peripheral-to-Memory and Memory-to-Peripheral Data Transfer

When `DMA2D_MEM_TRANS_EN_CHn` is 0, the 2D-DMA controller enters peripheral transfer mode. The transmit channel reads data from the memory and transmits it to peripherals, while the receive channel receives data from peripherals and stores it into the memory.

The transmit direction refers to data transfer from memory to peripheral, and the receive direction refers data transfer from peripheral to memory. A transmit channel transfers data in the specified memory location to a peripheral’s transmitter via an outlink`n`, whereas a receive channel transfers data received by a peripheral to the specified memory location via an inlink`n`.

Every transmit and receive channel can be connected to any peripheral that supports 2D-DMA. Table 5.4-2 and Table 5.4-3 illustrate how to select the peripheral to be connected via registers. “Dummy-`n`” corresponds to register values for memory-to-memory data transfer. When a channel is connected to a peripheral, the rest

of the channels cannot be connected to that peripheral.

**Table 5.4-2. Selecting Peripherals via Register Configuration in TX Direction**

| DMA2D_PERI_OUT_SEL_CH $n$ | Peripheral         |
|---------------------------|--------------------|
| 0                         | JPEG               |
| 1                         | PPA's SRM module   |
| 2                         | PPA's BLEND module |
| 3 ~ 7                     | Dummy-3 ~ 7        |

**Table 5.4-3. Selecting Peripherals via Register Configuration in RX Direction**

| DMA2D_PERI_IN_SEL_CH $n$ | Peripheral           |
|--------------------------|----------------------|
| 0                        | JPEG                 |
| 1                        | PPA's SRM module     |
| 2                        | PPA's BLEND0 channel |
| 3                        | PPA's BLEND1 channel |
| 4 ~ 7                    | Dummy-4 ~ 7          |

## 5.4.5 Memory-to-Memory Data Transfer

The 2D-DMA controller allows memory-to-memory data transfer only in 1D mode and 2D-MOD0 mode. Such data transfer can be enabled by setting `DMA2D_IN_MEM_TRANS_EN_CH $n$` , which connects the output of transmit channel  $n$  to the input of receive channel  $n$ . Note that a transmit channel can only be connected to the receive channel with the same number ( $n$ ), and `DMA2D_IN_PERI_SEL_CH $n$`  and `DMA2D_OUT_PERI_SEL_CH $n$`  should be configured to any value corresponding to "Dummy".

Memory-to-memory data transfer can be used in combination with color space conversion so that a macroblock can be moved from one segment of memory address space to another with its color space converted.

## 5.4.6 Macroblock Reordering

### 5.4.6.1 Macroblock Reordering in TX Direction

When the 2D-DMA accesses external memory via SPI, in order to improve the bandwidth utilization of SPI, it is necessary to initiate AXI transfers with a larger burst length. In 2D-MOD1 mode, the 2D-DMA can increase the burst length of AXI transfers by fetching multiple macroblocks at once. For example, the 2D-DMA can fetch five macroblocks of 8x8 pixels in one operation, and in this case, the `hb` field in the descriptor should be 40 and `vb` should be 8. However, the JPEG requires the 2D-DMA to send data in the order of macroblocks. This means that the 2D-DMA needs to reorder the fetched macroblocks to meet the requirements of JPEG.

Recommended configurations for macroblock reordering are listed in Table 5.4-4.

**Table 5.4-4. Recommended Configurations for Macroblock Reordering in TX Direction**

| Byte/Pixel | Macroblock Size (Pixel) | Optimal Macroblock Count | hb  | vb |
|------------|-------------------------|--------------------------|-----|----|
| 3          | 8×8                     | 5                        | 40  | 8  |
| 3          | 16×8                    | 2                        | 32  | 8  |
| 3          | 16×16                   | 2                        | 32  | 16 |
| 2          | 8×8                     | 8                        | 64  | 8  |
| 2          | 16×8                    | 4                        | 64  | 8  |
| 2          | 16×16                   | 3                        | 48  | 16 |
| 1          | 8×8                     | 16                       | 128 | 8  |

The macroblock size in TX direction should be configured via the [DMA2D\\_OUT\\_MACRO\\_BLOCK\\_SIZE\\_CHn](#) field.

#### 5.4.6.2 Macroblock Reordering in RX Direction

Currently, in RX direction the 2D-DMA can only reorder the data decoded by JPEG (the bitstream is 1 scan, see Chapter [31 JPEG Codec](#)). The 2D-DMA breaks down color component data decoded by JPEG into pixels, assembles them into larger macroblocks, and writes these blocks into the memory.

The data formats decoded by JPEG include GRAY, YUV444, YUV422, and YUV420. Recommended configurations for macroblock reordering are listed in Table [5.4-5](#).

**Table 5.4-5. Recommended Configuration Table for Macroblock Reordering in 2D-DMA Receive Direction (Without Color Format Conversion)**

| Format | Macroblock Size (pixels) | Optimal Macroblock Count | hb | vb |
|--------|--------------------------|--------------------------|----|----|
| GRAY   | 8×8                      | 12                       | 96 | 8  |
| YUV444 | 8×8                      | 5                        | 40 | 8  |
| YUV422 | 16×8                     | 4                        | 64 | 8  |
| YUV420 | 16×16                    | 3                        | 48 | 16 |

The macroblock size in TX direction should be configured via the [DMA2D\\_IN\\_MACRO\\_BLOCK\\_SIZE\\_CHn](#) field.

Figure [5.4-4](#) shows the layout of macroblocks outputted by the JPEG decoder. Each blue grid in this figure represents 8x8 bytes of continuous data, and for each color format the figure displays four macroblocks of 8×8 pixels.

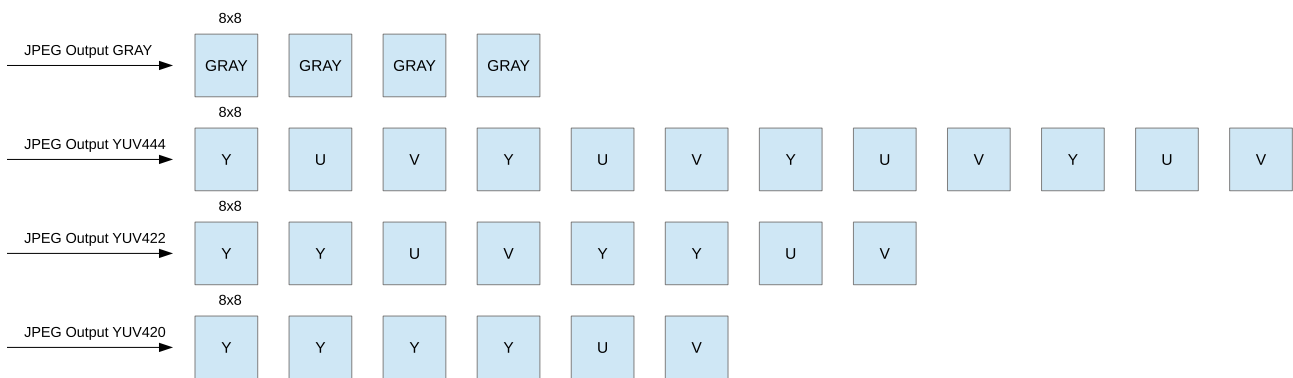


Figure 5.4-4. Macroblock Layout of JPEG Decoder Output Data

### 5.4.7 Color Space Conversion

On the transmit side, the 2D-DMA converts the color space after assembling the data read from memory into pixels. The 2D-DMA supports the following conversion except YUV420:

- RGB888 to RGB565
- RGB565 to RGB888
- RGB888 to YUV444
- RGB888 to YUV422 (the number of pixels per row in RGB format must be even)
- YUV444 to RGB888
- YUV422 to RGB888

On the receive side, only pixels received from JPEG requires color space conversion. The 2D-DMA supports the following conversion:

- YUV444 to RGB888/RGB565
- YUV422 to YUV444 to RGB888/RGB565
- YUV420 to YUV444 to RGB888/RGB565

**Note:**

- For JPEG decoding, i.e., the receive side of 2D-DMA, the hardware will forcibly convert YUV422 and YUV420 to the YUV444 format. Software can optionally further convert the format to RGB888/RGB565 with the color space conversion feature.

Figure 5.4-5 shows the structure of the color space conversion module.

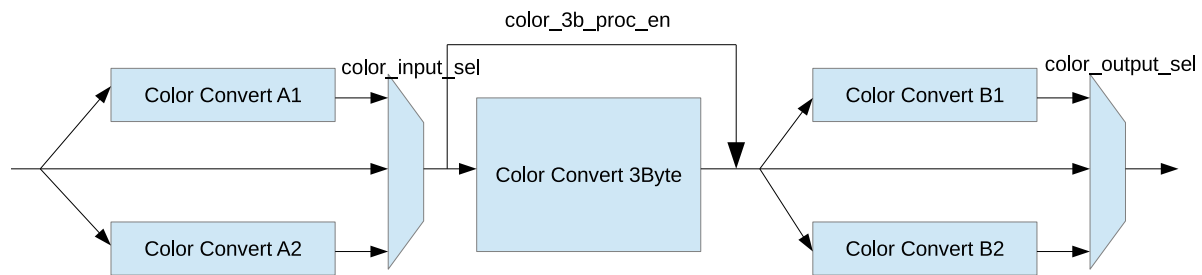


Figure 5.4-5. Color Space Conversion

Color space conversion is performed in 3 stages. The first stage converts a specific 16-bit color format (2 bytes/pixel) to a 24-bit color format (3 bytes/pixel). The source color formats can be configured via the [DMA2D\\_OUT\\_COLOR\\_INPUT\\_SEL\\_CHn](#) or [DMA2D\\_IN\\_COLOR\\_INPUT\\_SEL\\_CHO](#) field. (See the supported color format conversion in the first stage by clicking the fields)

The second stage further converts the output data of the first stage using the following formula:

$$256 * Q = A[9 : 0] * x + B[10 : 0] * y + C[9 : 0] * z + D[17 : 0]$$

In this formula, Q is the output data; x, y, and z are the most significant, middle, and the least significant byte of the input data respectively; A, B, C, and D are the corresponding multiplication or addition coefficients, which are signed numbers. At most 3 bytes of data can be processed in one go, and therefore  $3 * 4 = 12$  coefficients need to be configured via the following fields:

- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_HO\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_HO\\_CHO](#)
- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_H1\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_H1\\_CHO](#)
- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_MO\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_MO\\_CHO](#)
- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_M1\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_M1\\_CHO](#)
- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_LO\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_LO\\_CHO](#)
- [DMA2D\\_OUT\\_COLOR\\_PARAM\\_L1\\_CHn](#)/[DMA2D\\_IN\\_COLOR\\_PARAM\\_L1\\_CHO](#)

PARAM\_Hx, PARAM\_Mx, and PARAM\_Lx (x is 0 or 1) in field names represent the parameters for the three bytes of data respectively. Take PARAM\_Hx as examples, the lower 10 bits of the 21-bit PARAM\_H0 is coefficient A, the higher 11 bits of PARAM\_H0 is coefficient B, the lower 10 bits of the 28-bit PARAM\_H1 is coefficient C, and the higher 18 bits of PARAM\_H1 is coefficient D.

The third stage, similar to the first stage, outputs the color format converted in the second stage directly, or further converts the 24-bit color format (3 bytes/pixel) to a 16-bit color format. This is configured using [DMA2D\\_OUT\\_COLOR\\_OUTPUT\\_SEL\\_CHn](#) or [DMA2D\\_IN\\_COLOR\\_OUTPUT\\_SEL\\_CHO](#).

The following table lists the parameter configurations for commonly used color space conversions:

Table 5.4-6. Parameter Configuration for Color Space Conversion in TX Direction

| Conversion          | input_sel | proc_en | output_sel | param_h0 | param_h1 | param_m0 | param_m1 | param_l0 | param_l1 |
|---------------------|-----------|---------|------------|----------|----------|----------|----------|----------|----------|
| No conversion       | 7         | N/A     | N/A        | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| Only scramble order | 2/3       | 0       | 2          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |

Cont'd on next page

Table 5.4-6 – cont'd from previous page

| Conversion                 | input_sel | proc_en | output_sel | param_h0 | param_h1 | param_m0 | param_m1 | param_I0 | param_I1 |
|----------------------------|-----------|---------|------------|----------|----------|----------|----------|----------|----------|
| RGB888 → RGB565            | 3         | 0       | 0          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| RGB565 → RGB888            | 0         | 0       | 2          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| RGB888 → (601) YUV444      | 3         | 1       | 2          | 20442    | 400019   | 1EDBDA   | 2000070  | 1E8870   | 20003EE  |
| RGB888 → (709) YUV444      | 3         | 1       | 2          | 2742F    | 400010   | 1EABE6   | 2000070  | 1E6870   | 20003F6  |
| RGB888 → (601) YUV422-MIPI | 3         | 1       | 1          | 20442    | 400019   | 1EDBDA   | 2000070  | 1E8870   | 20003EE  |
| RGB888 → (709) YUV422-MIPI | 3         | 1       | 1          | 2742F    | 400010   | 1EABE6   | 2000070  | 1E6870   | 20003F6  |
| YUV444 → (601) RGB888      | 3         | 1       | 2          | 12A      | C86D999  | 1E712A   | 21E4F30  | 8112A    | BAD3000  |
| YUV444 → (709) RGB888      | 3         | 1       | 2          | 12A      | C21E5CB  | 1F252A   | 1338778  | 8752A    | B7D0800  |
| YUV422-MIPI → (601) RGB888 | 1         | 1       | 2          | 12A      | C86D999  | 1E712A   | 21E4F30  | 8112A    | BAD3000  |
| YUV422-MIPI → (709) RGB888 | 1         | 1       | 2          | 12A      | C21E5CB  | 1F252A   | 1338778  | 8752A    | B7D0800  |

Table 5.4-7. Parameter Configuration for Color Space Conversion in RX Direction

| Conversion                   | input_sel | proc_en | output_sel | param_h0 | param_h1 | param_m0 | param_m1 | param_I0 | param_I1 |
|------------------------------|-----------|---------|------------|----------|----------|----------|----------|----------|----------|
| No conversion                | 7         | N/A     | N/A        | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| Only scramble order          | 1/2       | 0       | 1          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| YUV422 → YUV444              | 0         | 0       | 1          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| YUV420 → YUV444              | 0         | 0       | 1          | N/A      | N/A      | N/A      | N/A      | N/A      | N/A      |
| YUV420 → (601) RGB888/RGB565 | 0         | 1       | 1/0        | 12A      | C86D999  | 1E712A   | 21E4F30  | 8112A    | BAD3000  |
| YUV422 → (601) RGB888/RGB565 | 0         | 1       | 1/0        | 12A      | C86D999  | 1E712A   | 21E4F30  | 8112A    | BAD3000  |
| YUV444 → (601) RGB888/RGB565 | 2         | 1       | 1/0        | 12A      | C86D999  | 1E712A   | 21E4F30  | 8112A    | BAD3000  |
| YUV420 → (709) RGB888/RGB565 | 0         | 1       | 1/0        | 12A      | C21E5CB  | 1F252A   | 1338778  | 8752A    | B7D0800  |
| YUV422 → (709) RGB888/RGB565 | 0         | 1       | 1/0        | 12A      | C21E5CB  | 1F252A   | 1338778  | 8752A    | B7D0800  |
| YUV444 → (709) RGB888/RGB565 | 2         | 1       | 1/0        | 12A      | C21E5CB  | 1F252A   | 1338778  | 8752A    | B7D0800  |

Additionally, the color space conversion module can scramble the order of at most three bytes per pixel. This can be done before the color space conversion in TX direction, and before or after the color space



conversion in RX direction. Table 5.4-8, Table 5.4-9, and Table 5.4-10 show the byte order per pixel required by the color space conversion module. For the JPEG decoder, if the byte order per pixel is not scrambled after the macroblock reordering in RX direction, it will conform to the requirements of color space conversion. Assuming that the order of an input pixel is represented from MSB to LSD as 2, 1, 0, the order can be scrambled and outputted as 210 (default), 201, 102, 120, 021, or 012. In RX direction, this feature can be configured before or after the color space conversion via [DMA2D\\_IN\\_SCRAMBLE\\_SEL\\_PRE\\_CHO](#) or [DMA2D\\_IN\\_SCRAMBLE\\_SEL\\_POST\\_CHO](#) respectively; in TX direction, this feature can be configured before the color space conversion via [DMA2D\\_OUT\\_SCRAMBLE\\_SEL\\_PRE\\_CHn](#).

**Table 5.4-8. RGBB888 Storage Format**

|      |     |    |    |    |    |    |    |    |     |
|------|-----|----|----|----|----|----|----|----|-----|
|      | LSB |    |    |    |    |    |    |    | MSB |
| LINE | B1  | G1 | R1 | B2 | G2 | R2 | B3 | G3 | R3  |

**Table 5.4-9. YUV444 Storage Format**

|      |     |    |    |    |    |    |    |    |     |
|------|-----|----|----|----|----|----|----|----|-----|
|      | LSB |    |    |    |    |    |    |    | MSB |
| LINE | V1  | U1 | Y1 | V2 | U2 | Y2 | V3 | U3 | Y3  |

**Table 5.4-10. YUV422 Storage Format**

|      |     |    |    |    |    |    |    |     |
|------|-----|----|----|----|----|----|----|-----|
|      | LSB |    |    |    |    |    |    | MSB |
| LINE | U1  | Y1 | V1 | Y2 | U3 | Y3 | V3 | Y4  |

## 5.4.8 Enabling 2D-DMA

The software uses the 2D-DMA controller through linked lists. For receive channels, software loads an inlink, configures the [DMA2D\\_INLINK\\_ADDR\\_CHn](#) field with the address of the first receive descriptor, and sets the [DMA2D\\_INLINK\\_START\\_CHn](#) bit to enable the 2D-DMA. For transmit channels, software loads an outlink, prepares data to be transmitted, configures the [DMA2D\\_OUTLINK\\_ADDR\\_CHn](#) field with address of the first transmit descriptor, and sets the [DMA2D\\_OUTLINK\\_START\\_CHn](#) bit to enable the 2D-DMA. The [DMA2D\\_INLINK\\_START\\_CHn](#) bit and [DMA2D\\_OUTLINK\\_START\\_CHn](#) bit are cleared automatically by hardware.

In some cases, you may want to append more descriptors to a 2D-DMA transfer that is already started. Naively, it would seem to be possible to do this by clearing the eof bit of the final descriptor in the existing list and setting its next descriptor address pointer field (DW4) to the first descriptor of the to-be-added list. However, this strategy fails if the existing 2D-DMA transfer is almost or entirely finished. Instead, the 2D-DMA controller has specialized logic to make sure a transfer can be continued or restarted: if the transfer is ongoing, the controller will make sure to take the appended descriptors into account; if the transfer has already finished, the controller will restart with the new descriptors. This is implemented by the Restart function.

When using the Restart function, software needs to

1. Set [DMA2D\\_INLINK\\_STOP\\_CHn](#) or [DMA2D\\_OUTLINK\\_STOP\\_CHn](#) to stop the 2D-DMA when it finishes processing the current descriptor
2. Rewrite the address of the first descriptor in the new list to DW4 of the last descriptor in the loaded list

3. Set `DMA2D_INLINK_RESTART_CHn` or `DMA2D_OUTLINK_RESTART_CHn` (these two bits are cleared automatically by hardware)

By doing so, hardware can obtain the address of the first descriptor in the new list when reading the last descriptor in the loaded list, and then read the new list.

### 5.4.9 Linked List Reading Process

Once configured and enabled by software, the 2D-DMA controller starts to read the linked list from the memory. The 2D-DMA performs checks on descriptors in the linked list. Only if descriptors pass the checks, the corresponding 2D-DMA channel will start data transfer. If the descriptors fail any of the checks, hardware will trigger descriptor error interrupt (either `DMA2D_IN_DSCR_ERR_CHn_INT` or `DMA2D_OUT_DSCR_ERR_CHn_INT`), and the channel will remain idle. This channel can be restarted by setting `DMA2D_OUTLINK_START_CHn` or `DMA2D_INLINK_START_CHn` again.

The checks performed on descriptors are:

- Owner bit check when `DMA2D_IN_CHECK_OWNER_CHn` or `DMA2D_OUT_CHECK_OWNER_CHn` is set to 1. If the owner bit is 0, the buffer is accessed by the CPU. In this case, the owner bit fails the check. The owner bit will not be checked if `DMA2D_IN_CHECK_OWNER_CHn` or `DMA2D_OUT_CHECK_OWNER_CHn` is 0.
- Descriptor address check, which checks if the descriptor address is located in configured memory space. If a 2D-DMA descriptor points to `DMA2D_ACCESS_INTR_MEM_START_ADDR ~ DMA2D_ACCESS_INTR_MEM_END_ADDR` (the value should be located in internal memory) or `DMA2D_ACCESS_EXTR_MEM_START_ADDR ~ DMA2D_ACCESS_EXTR_MEM_END_ADDR` (the value should be located in external memory), it passes the check. For details, please refer to Section 5.4.11).
- HA/VA/hb/vb/SIZE check, which checks if any of these fields is 0. If any field is 0, it fails the check. HA/VA/hb/vb fields are not checked in 1D mode, while SIZE is checked only in 1D mode.

After the software detects a descriptor error interrupt, it must reset the corresponding channel, and restart the 2D-DMA DMA by setting the `DMA2D_OUTLINK_START_CHn` or `DMA2D_INLINK_START_CHn` bit.

To quickly obtain receive or transmit descriptors from the memory, AXI burst transfers for 2D-DMA can be enabled by setting `DMA2D_INDSCR_BURST_EN_CHn` or `DMA2D_OUTDSCR_BURST_EN_CHn`.

### 5.4.10 EOF

**Note:** In this chapter, EOF of transmit descriptors refers to eof (i.e., bit 30 of DW0), while EOF of receive descriptors refers to both eof and err\_eof (i.e., bit 28 of DW0).

The 2D-DMA controller uses EOF (end of frame) flags to indicate the end of the image transmission.

For data transmission, the 2D-DMA generates two types of EOF interrupts:

- `DMA2D_OUT_EOF_CHn_INT`, generated when the eof bit of any descriptor in the linked list is set, and the data corresponding to this descriptor has been transmitted. Usually, the eof bit is set in the last descriptor for the transmission of an image. This interrupt is enabled by setting the `DMA2D_OUT_EOF_CHn_INT_ENA` bit.
- `DMA2D_OUT_TOTAL_EOF_CHn_INT`, generated when the eof bit of the last descriptor in the linked list is set, and the data corresponding to the last descriptor has been transmitted. This interrupt is enabled by

setting the [DMA2D\\_OUT\\_TOTAL\\_EOF\\_CH \$n\$ \\_INT\\_ENA](#) bit.

For data reception, the 2D-DMA also generates two types of EOF interrupts:

- [DMA2D\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#), generated when an image has been received. This interrupt is enabled by setting the [DMA2D\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT\\_ENA](#) bit.
- (JPEG only) [DMA2D\\_IN\\_ERR\\_EOF\\_CH \$n\$ \\_EOF\\_INT](#), generated when an image has been received with errors. This interrupt is enabled by setting the [DMA2D\\_IN\\_ERR\\_EOF\\_CH \$n\$ \\_INT\\_ENA](#) bit, and is valid only when the channel is connected to JPEG.

When detecting an [DMA2D\\_OUT\\_TOTAL\\_EOF\\_CH \$n\$ \\_INT](#) or [DMA2D\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#) interrupt, software can read the value of the [DMA2D\\_OUT\\_EOF\\_DES\\_ADDR\\_CH \$n\$](#)  or [DMA2D\\_IN\\_SUC\\_EOF\\_DES\\_ADDR\\_CH \$n\$](#)  field, which stores the address of the finished descriptor. Therefore, the software can tell which descriptors have been used and reclaim them as needed. In RX direction, the address of the descriptor can also be stored to the [DMA2D\\_IN\\_ERR\\_EOF\\_DES\\_ADDR\\_CH \$n\$](#)  field when an [DMA2D\\_IN\\_ERR\\_EOF\\_CH \$n\$ \\_INT](#) interrupt is triggered.

### 5.4.11 Accessing Memory

Any transmit and receive channels of the 2D-DMA can access the internal memory address space configured by [DMA2D\\_ACCESS\\_INTR\\_MEM\\_START\\_ADDR](#) and [DMA2D\\_ACCESS\\_INTR\\_MEM\\_END\\_ADDR](#), and the external memory address space configured by [DMA2D\\_ACCESS\\_EXTR\\_MEM\\_START\\_ADDR](#) and [DMA2D\\_ACCESS\\_EXTR\\_MEM\\_END\\_ADDR](#).

The 2D-DMA can send data in the internal memory in burst mode via the AXI bus. Burst transfer on the AXI bus is enabled by default, and cannot be disabled. Users can configure the number of data bytes in a single AXI burst (burst length) to 8, 16, 32, 64, or 128 bytes via [DMA2D\\_IN\\_MEM\\_BURST\\_LENGTH\\_CH \$n\$](#)  and [DMA2D\\_OUT\\_MEM\\_BURST\\_LENGTH\\_CH \$n\$](#) .

When the 2D-DMA accesses the encrypted external memory space (see Chapter [29 External Memory Encryption and Decryption \(XTS\\_AES\)](#)), buffer address pointer and corresponding data should be 16-byte aligned; when it accesses the configured internal memory and non-encrypted external memory space, there are no requirements for descriptor field alignment.

### 5.4.12 Arbitration

To ensure timely response to peripherals running at a high speed with low latency, the 2D-DMA controller implements two arbitration schemes, based on channel priority and channel weight respectively.

- Priority arbitration: Each channel can be assigned a priority from 0 ~ 3 (in total 4 levels). The larger the number, the higher the priority. When several channels perform data transfers at the same time, the 2D-DMA would respond to the transfer requests according to priority levels, and the channel with higher priority would get a response more timely.
- Weight arbitration:
  - Each channel is assigned a weight (i.e., the number of tokens) from 0 ~ 15. The 2D-DMA divides the AXI bus clock period into multiple time slots, and in each time slot, the number of transfers performed by a channel is determined by the number of its tokens. Every time a channel performs a data transfer, one of its tokens is spent. If all of its tokens have been spent in a time slot, then this

channel's transfer request will no longer be responded to until the time slot expires, or until tokens of all channels have been spent and the new time slot starts.

- If the number of tokens assigned to a channel is not zero, the 2D-DMA waits for this channel's tokens to be spent even if it does not have data transfer requests, and will not exit from this time slot ahead of expiration. This leads to a waste of bandwidth. Therefore, the 2D-DMA provides weight arbitration optimization. When this feature is enabled, a channel without data transfer requests will not be involved in the arbitration and its tokens will be ignored. When all channels no longer have transfer requests, the 2D-DMA arbiter exits from the current time slot before expiration. This way, the arbitration response is accelerated and the transfer efficiency is improved.

**Note:**

- If channels have the same weight but different priorities, on condition that the number of bytes to be transferred is the same and not large, channels with higher priorities would finish data transfers first.
- If channels have different priorities and weights, on condition that the number of bytes to be transferred is the same, channels with higher weights would be allocated more bandwidth and finish data transfers first.

## 5.5 Event Task Matrix Feature

The 2D-DMA controller on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows 2D-DMA's ETM tasks to be triggered by any peripherals' ETM events, or 2D-DMA's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to 2D-DMA. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

2D-DMA can receive the following ETM tasks:

- `DMA2D_TASK_IN_START_CH $n$` : Enables the corresponding receive channel  $n$  for data transfer.
- `DMA2D_TASK_OUT_START_CH $n$` : Enables the corresponding transmit channel  $n$  for data transfer.

**Note:**

Above ETM tasks can achieve the same functions as CPU configuring `DMA2D_INLINK_START_CH $n$`  and `DMA2D_OUTLINK_START_CH $n$` . When `DMA2D_IN_ETM_EN_CH $n$`  or `DMA2D_OUT_ETM_EN_CH $n$`  is 1, only ETM tasks can be used to configure the transfer direction and enable the corresponding 2D-DMA channel. When `DMA2D_IN_ETM_EN_CH $n$`  or `DMA2D_OUT_ETM_EN_CH $n$`  is 0, only CPU can be used to enable the corresponding 2D-DMA channel.

- `DMA2D_TASK_IN_DSCR_READY_CH $n$` : Allows receive channel  $n$  to process the next descriptor.
- `DMA2D_TASK_OUT_DSCR_READY_CH $n$` : Allows transmit channel  $n$  to process the next descriptor.

**Note:**

In normal conditions, after finishing with the current descriptor if the next descriptor is available (i.e., the next descriptor address field is not zero), the 2D-DMA would process the next descriptor directly and reads/writes to the memory according to the descriptor's configuration until all descriptors are processed. When `DMA2D_IN_ETM_LOOP_EN_CH $n$`  or `DMA2D_OUT_ETM_LOOP_EN_CH $n$`  is set, after finishing with the current descriptor, the 2D-DMA would not start processing the next descriptor until receiving the `DMA2D_TASK_IN_DSCR_READY_CH $n$`  or

DMA2D\_TASK\_OUT\_DSCR\_READY\_CH $n$  task.

The DMA2D\_TASK\_IN\_DSCR\_READY\_CH $n$  or DMA2D\_TASK\_OUT\_DSCR\_READY\_CH $n$  task can be stored in the task buffer, which can cache at most four tasks. When the 2D-DMA receives this task but the current descriptor is not yet processed, it can cache the task. The depth of the task buffer is determined by

[DMA2D\\_IN\\_DSCR\\_TASK\\_MAX\\_CH \$n\$](#)  or [DMA2D\\_OUT\\_DSCR\\_TASK\\_MAX\\_CH \$n\$](#) .

When the task buffer exceeds its maximum capacity, it will trigger an [DMA2D\\_IN\\_DSCR\\_TASK\\_OVF\\_CH \$n\$ \\_INT](#) or [DMA2D\\_OUT\\_DSCR\\_TASK\\_OVF\\_CH \$n\$ \\_INT](#) interrupt.

2D-DMA can generate the following ETM events:

- DMA2D\_EVT\_IN\_DONE\_CH $n$ : Indicates that the data has been received according to the receive descriptor via channel  $n$ .
- DMA2D\_EVT\_IN\_SUC\_EOF\_CH $n$ : Indicates that the data corresponding to a receive descriptor has been received via channel  $n$  and the Eof bit of this descriptor is 1.
- DMA2D\_EVT\_OUT\_DONE\_CH $n$ : Indicates that the data has been transmitted according to the transmit descriptor via channel  $n$ .
- DMA2D\_EVT\_OUT\_SUC\_EOF\_CH $n$ : Indicates that the data corresponding to a transmit descriptor has been transmitted or received via channel  $n$  and the eof bit of this descriptor is 1.
- DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH $n$ : Indicates that the data corresponding to the last transmit descriptors has been sent via transmit channel  $n$  and the eof bit of this descriptor is 1.

In practical applications, 2D-DMA's ETM events can trigger its own ETM tasks. For example, the DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH0 event can trigger the DMA2D\_TASK\_IN\_START\_CH1 task, and in this way trigger a new round of 2D-DMA operations.

## 5.6 Interrupts

ESP32-P4's 2D-DMA module can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- DMA2D\_IN\_CHO\_INTR
- DMA2D\_IN\_CH1\_INTR
- DMA2D\_OUT\_CHO\_INTR
- DMA2D\_OUT\_CH1\_INTR
- DMA2D\_OUT\_CH2\_INTR

There are several internal interrupt sources from 2D-DMA that can generate the above interrupt signals.

The DMA2D\_IN\_CH $n$ \_INTR ( $n$  is 0 ~ 1) signals are generated by the following interrupt sources:

- DMA2D\_IN\_DONE\_CH $n$ \_INT: Triggered when all data corresponding to a receive descriptor has been received via receive channel  $n$ .
- DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT: Triggered when the eof bit in a receive descriptor is 1 and the data corresponding to this receive descriptor has been received (i.e., when an image corresponding to an inlink has been received) via receive channel  $n$ .

- DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT: Triggered when an error is detected in the image received via receive channel  $n$ . This interrupt is used only for JPEG.
- DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT: Triggered when the size of the buffer pointed by receive descriptors is smaller than the length of data to be received via receive channel  $n$ .
- DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT: Triggered when a receive descriptor on receive channel  $n$  fails any of the two descriptor checks.
- DMA2D\_INFIFO\_OVF\_CH $n$ \_INT: Triggered when the RX FIFO of 2D-DMA overflows.
- DMA2D\_INFIFO\_UDF\_CH $n$ \_INT or AXI\_DMA\_INFIFO\_L1/L2/L3\_UDF\_CH $n$ \_INT: Triggered when the RX FIFO of 2D-DMA underflows.
- DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT: Triggered when the number of cached DMA2D\_TASK\_IN\_DSCR\_READY\_CH $n$  task exceeds the maximum capacity of the task buffer.
- DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT (only channel 0): Triggered when the buffer for macroblock reordering in RX direction overflows.
- DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT (only channel 0): Triggered when the buffer for macroblock reordering in RX direction underflows.

The DMA2D\_OUT\_CH $n$ \_INTR ( $n$  is 0 ~ 2) signals are generated by the following interrupt sources:

- DMA2D\_OUT\_DONE\_CH $n$ \_INT: Triggered when all data corresponding to a transmit descriptor has been sent via transmit channel  $n$ .
- DMA2D\_OUT\_EOF\_CH $n$ \_INT: Triggered when the eof bit in a transmit descriptor is 1 and data corresponding to this descriptor has been sent via transmit channel  $n$ . If DMA2D\_OUT\_EOF\_MODE\_CH $n$  is 0, this interrupt will be triggered when the last byte of data corresponding to this descriptor enters 2D-DMA's transmit channel via the bus; if DMA2D\_OUT\_EOF\_MODE\_CH $n$  is 1, this interrupt is triggered when the last byte of data is taken from 2D-DMA's transmit channel.
- DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT: Triggered when a transmit descriptor on transmit channel  $n$  fails any of the two descriptor checks.
- DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT: Triggered when all data corresponding to a linked list (including multiple descriptors) has been sent via transmit channel  $n$ .
- DMA2D\_OUTFIFO\_L1/L2/L3\_OVF\_CH $n$ \_INT: Triggered when the TX FIFO of 2D-DMA overflows.
- DMA2D\_OUTFIFO\_L1/L2/L3\_UDF\_CH $n$ \_INT: Triggered when the TX FIFO of 2D-DMA underflows.
- DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT: Triggered when the number of cached DMA2D\_TASK\_OUT\_DSCR\_READY\_CH $n$  task exceeds the maximum capacity of the task buffer.
- DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT (only channel 0): Triggered when the buffer for macroblock reordering or color space conversion in TX direction overflows.
- DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT (only channel 0): Triggered when the buffer for macroblock reordering or color space conversion in TX direction underflows.

## 5.7 Programming Procedures

The clock gating for the 2D-DMA can be configured via [HP\\_SYS\\_CLKRST\\_DMA2D\\_SYS\\_CLK\\_EN](#), and is enabled by default. The 2D-DMA can be reset globally by configuring [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_AHB/AXI\\_PDMA](#).

### 5.7.1 General Configurations for 2D-DMA

Configure the accessible address space of internal and external memory and burst length according to Section [5.4.11](#).

### 5.7.2 Mode-Specific Configurations for 2D-DMA

- 1D Mode: No specific configuration required.
- 2D-MOD0 Mode: No specific configuration required.
- 2D-MOD1 Mode: For JPEG, configure [DMA2D\\_IN\\_MACRO\\_BLOCK\\_SIZE\\_CHn](#) or [DMA2D\\_OUT\\_MACRO\\_BLOCK\\_SIZE\\_CHn](#) to choose a macroblock size out of the three available options (horizontal × vertical): 8 pixels × 8 pixels, 8 pixels × 16 pixels, and 16 pixels × 16 pixels. For more information about macroblock size, see Chapter [31 JPEG Codec](#). For correspondence between macroblock size, hb, and vb of descriptors, see Table [5.4-4](#) and Table [5.4-5](#).
- DSCR-PORT Mode: Set [DMA2D\\_OUT\\_DSCR\\_PORT\\_EN\\_CHn](#) to enter this mode. This mode is specifically designed for PPA. For details, see Chapter [33 Pixel-Processing Accelerator \(PPA\)](#).

### 5.7.3 Configurations for 2D-DMA's Transmit Channel

To transmit data, 2D-DMA's transmit channel should be configured by software as follows:

1. Set [DMA2D\\_OUT\\_RST\\_CHn](#) first to 1 and then to 0, to reset the state machine of 2D-DMA's transmit channel and FIFO pointer.
2. Load an outlink, and configure [DMA2D\\_OUTLINK\\_ADDR\\_CHn](#) with address of the first transmit descriptor.
3. Configure [DMA2D\\_OUT\\_PERI\\_SEL\\_CHn](#) with the value corresponding to the peripheral to be connected, as shown in Table [5.4-2](#).
4. Set [DMA2D\\_OUTLINK\\_START\\_CHn](#) to enable 2D-DMA's transmit channel for data transfer.
5. Configure and enable the corresponding peripheral. See details in individual chapters of these peripherals.
6. Wait for the [DMA2D\\_OUT\\_EOF\\_CHn\\_INT](#) interrupt, which indicates the completion of data transfer.

### 5.7.4 Configurations for 2D-DMA's Receive Channel

To receive data, 2D-DMA's receive channel should be configured by software as follows:

1. Set [DMA2D\\_IN\\_RST\\_CHn](#) first to 1 and then to 0, to reset the state machine of 2D-DMA's receive channel and FIFO pointer.
2. Load an inlink, and configure [DMA2D\\_INLINK\\_ADDR\\_CHn](#) with address of the first receive descriptor.



3. Configure `DMA2D_IN_PERI_SEL_CHn` with the value corresponding to the peripheral to be connected, as shown in Table 5.4-3.
4. Set `DMA2D_INLINK_START_CHn` to enable 2D-DMA's receive channel for data transfer.
5. Configure and enable the corresponding peripheral. See details in individual chapters of these peripherals.
6. Wait for `DMA2D_IN_SUC_EOF_CHn_INT` interrupt, which indicates that an image has been received.

## 5.7.5 Configurations for Memory-to-Memory Transfer

To transfer data from one memory location to another, 2D-DMA should be configured by software as follows:

1. Set `DMA2D_OUT_RST_CHn` first to 1 and then to 0, to reset the state machine of 2D-DMA's transmit channel and FIFO pointer.
2. Set `DMA2D_IN_RST_CHn` first to 1 and then to 0, to reset the state machine of 2D-DMA's receive channel and FIFO pointer.
3. Load an outlink, and configure `DMA2D_OUTLINK_ADDR_CHn` with address of the first transmit descriptor.
4. Load an inlink, and configure `DMA2D_INLINK_ADDR_CHn` with address of the first receive descriptor.
5. Configure `DMA2D_PERI_OUT_SEL_CHn` with any value corresponding to Dummy-*n* (see Table 5.4-2).
6. Configure `DMA2D_PERI_IN_SEL_CHn` with any value corresponding to Dummy-*n* (see Table 5.4-3).
7. Set `DMA2D_IN_MEM_TRANS_EN_CHn` to enable memory-to-memory transfer.
8. Set `DMA2D_OUTLINK_START_CHn` to enable 2D-DMA's transmit channel for data transfer.
9. Set `DMA2D_INLINK_START_CHn` to enable 2D-DMA's receive channel for data transfer.
10. Wait for `DMA2D_IN_SUC_EOF_CHn_INT` interrupt, which indicates that a data transaction has been completed.

## 5.7.6 Configurations for Channel Priority and Weight

The priority arbitration can be configured as follows:

1. Configure the channel priority for TX and RX respectively via `DMA2D_OUT_ARB_PRIORITY_CHn` and `DMA2D_IN_ARB_PRIORITY_CHn`.

The weight arbitration can be configured as follows:

1. Configure the time slot for TX and RX respectively via `DMA2D_OUT_ARB_TIMEOUT_NUM` and `DMA2D_IN_ARB_TIMEOUT_NUM`.
2. Configure the number of tokens for TX and RX respectively via `DMA2D_OUT_ARB_TOKEN_NUM_CHn` and `DMA2D_IN_ARB_TOKEN_NUM_CHn`.
3. Enable weight arbitration optimization for TX and RX respectively by clearing `DMA2D_OUT_ARB_WEIGHT_OPT_DIS_CHn` and `DMA2D_IN_ARB_WEIGHT_OPT_DIS_CHn`.
4. Enable the arbitration for TX and RX respectively via `DMA2D_OUT_WEIGHT_EN` and `DMA2D_IN_WEIGHT_EN`.



## 5.7.7 Resetting 2D-DMA While it Runs

When the 2D-DMA is running, namely when it is still processing descriptors, it must be stopped first before being reset fully via [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_DMA2D](#) or partially (only reset AXI functions) via [DMA2D\\_AXIM\\_RD\\_RST](#) and [DMA2D\\_AXIM\\_WR\\_RST](#). The procedures are as follows:

1. Set [DMA2D\\_IN\\_CMD\\_DISABLE\\_CHn](#) and [DMA2D\\_OUT\\_CMD\\_DISABLE\\_CHn](#) to stop the 2D-DMA.
2. Reset the 2D-DMA when [DMA2D\\_OUT\\_RESET\\_AVAIL\\_CHn](#) and [DMA2D\\_IN\\_RESET\\_AVAIL\\_CHn](#) turn to 1.
3. Clear [DMA2D\\_IN\\_CMD\\_DISABLE\\_CHn](#) and [DMA2D\\_OUT\\_CMD\\_DISABLE\\_CHn](#) to 0 after the 2D-DMA is reset.

## 5.8 Register Summary

The addresses in this section are relative to 2D-DMA base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Configuration Registers</b>                  |   |         |        |
| <a href="#">DMA2D_OUT_CONFO_CHO_REG</a>         | Configures the TX channel 0                                     | 0x0000  | R/W    |
| <a href="#">DMA2D_OUT_PUSH_CHO_REG</a>          | Configures the FIFO of TX channel 0                             | 0x0018  | varies |
| <a href="#">DMA2D_OUT_LINK_CONF_CHO_REG</a>     | Configures the transmit descriptor operations of TX channel 0   | 0x001C  | varies |
| <a href="#">DMA2D_OUT_LINK_ADDR_CHO_REG</a>     | Configures the transmit descriptor address of TX channel 0      | 0x0020  | R/W    |
| <a href="#">DMA2D_OUT_ARB_CHO_REG</a>           | Configures the arbitration of TX channel 0                      | 0x003C  | R/W    |
| <a href="#">DMA2D_OUT_RO_PD_CONF_CHO_REG</a>    | Configures the macroblock reordering memory of TX channel 0     | 0x0044  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_CONVERT_CHO_REG</a> | Configures the color space conversion of TX channel 0           | 0x0048  | R/W    |
| <a href="#">DMA2D_OUT_SCRAMBLE_CHO_REG</a>      | Configures the byte scrambling of TX channel 0                  | 0x004C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM0_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x0050  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM1_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x0054  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM2_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x0058  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM3_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x005C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM4_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x0060  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM5_CHO_REG</a>  | Configures the color space conversion parameter of TX channel 0 | 0x0064  | R/W    |
| <a href="#">DMA2D_OUT_ETM_CONF_CHO_REG</a>      | Configures the ETM of TX channel 0                              | 0x0068  | R/W    |
| <a href="#">DMA2D_OUT_DSCR_PORT_BLK_CHO_REG</a> | Configures the block size for TX channel 0 in DSCR-PORT mode    | 0x006C  | R/W    |
| <a href="#">DMA2D_OUT_CONFO_CH1_REG</a>         | Configures the TX channel 1                                     | 0x0100  | R/W    |
| <a href="#">DMA2D_OUT_PUSH_CH1_REG</a>          | Configures the FIFO of TX channel 1                             | 0x0118  | varies |
| <a href="#">DMA2D_OUT_LINK_CONF_CH1_REG</a>     | Configures the transmit descriptor operations of TX channel 1   | 0x011C  | varies |
| <a href="#">DMA2D_OUT_LINK_ADDR_CH1_REG</a>     | Configures the transmit descriptor address of TX channel 1      | 0x0120  | R/W    |
| <a href="#">DMA2D_OUT_ARB_CH1_REG</a>           | Configures the arbitration of TX channel 1                      | 0x013C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_CONVERT_CH1_REG</a> | Configures the color space conversion of TX channel 1           | 0x0148  | R/W    |
| <a href="#">DMA2D_OUT_SCRAMBLE_CH1_REG</a>      | Configures the byte scrambling of TX channel 1                  | 0x014C  | R/W    |

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <a href="#">DMA2D_OUT_COLOR_PARAM0_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x0150  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM1_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x0154  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM2_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x0158  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM3_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x015C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM4_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x0160  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM5_CH1_REG</a>  | Configures the color space conversion parameter of TX channel 1 | 0x0164  | R/W    |
| <a href="#">DMA2D_OUT_ETM_CONF_CH1_REG</a>      | Configures the ETM of TX channel 1                              | 0x0168  | R/W    |
| <a href="#">DMA2D_OUT_DSCR_PORT_BLK_CH1_REG</a> | Configures the block size for TX channel 1 in DSCR-PORT mode    | 0x016C  | R/W    |
| <a href="#">DMA2D_OUT_CONFO_CH2_REG</a>         | Configures the TX channel 2                                     | 0x0200  | R/W    |
| <a href="#">DMA2D_OUT_PUSH_CH2_REG</a>          | Configures the FIFO of TX channel 2                             | 0x0218  | varies |
| <a href="#">DMA2D_OUT_LINK_CONF_CH2_REG</a>     | Configures the transmit descriptor operations of TX channel 2   | 0x021C  | varies |
| <a href="#">DMA2D_OUT_LINK_ADDR_CH2_REG</a>     | Configures the transmit descriptor address of TX channel 2      | 0x0220  | R/W    |
| <a href="#">DMA2D_OUT_ARB_CH2_REG</a>           | Configures the arbitration of TX channel 2                      | 0x023C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_CONVERT_CH2_REG</a> | Configures the color space conversion of TX channel 2           | 0x0248  | R/W    |
| <a href="#">DMA2D_OUT_SCRAMBLE_CH2_REG</a>      | Configures the byte scrambling of TX channel 2                  | 0x024C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM0_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x0250  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM1_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x0254  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM2_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x0258  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM3_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x025C  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM4_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x0260  | R/W    |
| <a href="#">DMA2D_OUT_COLOR_PARAM5_CH2_REG</a>  | Configures the color space conversion parameter of TX channel 2 | 0x0264  | R/W    |
| <a href="#">DMA2D_OUT_ETM_CONF_CH2_REG</a>      | Configures the ETM of TX channel 2                              | 0x0268  | R/W    |
| <a href="#">DMA2D_OUT_DSCR_PORT_BLK_CH2_REG</a> | Configures the block size for TX channel 2 in DSCR-PORT mode    | 0x026C  | R/W    |
| <a href="#">DMA2D_IN_CONFO_CHO_REG</a>          | Configures the RX channel 0                                     | 0x0500  | R/W    |
| <a href="#">DMA2D_IN_POP_CHO_REG</a>            | Configures the FIFO of RX channel 0                             | 0x0518  | varies |
| <a href="#">DMA2D_IN_LINK_CONF_CHO_REG</a>      | Configures the receive descriptor operations of RX channel 0    | 0x051C  | varies |
| <a href="#">DMA2D_IN_LINK_ADDR_CHO_REG</a>      | Configures the receive descriptor address of RX channel 0       | 0x0520  | R/W    |
| <a href="#">DMA2D_IN_ARB_CHO_REG</a>            | Configures the arbitration of RX channel 0                      | 0x0540  | R/W    |
| <a href="#">DMA2D_IN_RO_PD_CONF_CHO_REG</a>     | Configures the macroblock reordering memory of RX channel 0     | 0x0548  | R/W    |

| Name   | Description   | Address | Access   |
|--|---|---------|----------|
| <a href="#">DMA2D_IN_COLOR_CONVERT_CHO_REG</a> | Configures the color space conversion of RX channel 0           | 0x054C  | R/W      |
| <a href="#">DMA2D_IN_SCRAMBLE_CHO_REG</a>      | Configures the byte scrambling of RX channel 0                  | 0x0550  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM0_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x0554  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM1_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x0558  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM2_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x055C  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM3_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x0560  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM4_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x0564  | R/W      |
| <a href="#">DMA2D_IN_COLOR_PARAM5_CHO_REG</a>  | Configures the color space conversion parameter of RX channel 0 | 0x0568  | R/W      |
| <a href="#">DMA2D_IN_ETM_CONF_CHO_REG</a>      | Configures the ETM of RX channel 0                              | 0x056C  | R/W      |
| <a href="#">DMA2D_IN_CONFO_CH1_REG</a>         | Configures the RX channel 1                                     | 0x0600  | R/W      |
| <a href="#">DMA2D_IN_POP_CH1_REG</a>           | Configures the FIFO of RX channel 1                             | 0x0618  | varies   |
| <a href="#">DMA2D_IN_LINK_CONF_CH1_REG</a>     | Configures the receive descriptor operations of RX channel 1    | 0x061C  | varies   |
| <a href="#">DMA2D_IN_LINK_ADDR_CH1_REG</a>     | Configures the receive descriptor address of RX channel 1       | 0x0620  | R/W      |
| <a href="#">DMA2D_IN_ARB_CH1_REG</a>           | Configures the arbitration of RX channel 1                      | 0x0640  | R/W      |
| <a href="#">DMA2D_IN_ETM_CONF_CH1_REG</a>      | Configures the ETM of RX channel 1                              | 0x0648  | R/W      |
| <a href="#">DMA2D_RST_CONF_REG</a>             | Configures the reset of AXI                                     | 0x0A04  | R/W      |
| <a href="#">DMA2D_INTR_MEM_START_ADDR_REG</a>  | The start address of accessible internal memory address space   | 0x0A08  | R/W      |
| <a href="#">DMA2D_INTR_MEM_END_ADDR_REG</a>    | The end address of accessible internal memory address space     | 0x0A0C  | R/W      |
| <a href="#">DMA2D_EXTR_MEM_START_ADDR_REG</a>  | The start address of accessible external memory address space   | 0x0A10  | R/W      |
| <a href="#">DMA2D_EXTR_MEM_END_ADDR_REG</a>    | The end address of accessible external memory address space     | 0x0A14  | R/W      |
| <a href="#">DMA2D_OUT_ARB_CONFIG_REG</a>       | Configures the arbitration in TX direction                      | 0x0A18  | R/W      |
| <a href="#">DMA2D_IN_ARB_CONFIG_REG</a>        | Configures the arbitration in RX direction                      | 0x0A1C  | R/W      |
| <b>Interrupt Registers</b>                     |   |         |          |
| <a href="#">DMA2D_OUT_INT_RAW_CHO_REG</a>      | Raw interrupt status of TX channel 0                            | 0x0004  | R/WTC/SS |
| <a href="#">DMA2D_OUT_INT_ENA_CHO_REG</a>      | Interrupt enable bits of TX channel 0                           | 0x0008  | R/W      |
| <a href="#">DMA2D_OUT_INT_ST_CHO_REG</a>       | Masked interrupt status of TX channel 0                         | 0x000C  | RO       |
| <a href="#">DMA2D_OUT_INT_CLR_CHO_REG</a>      | Interrupt clear bits of TX channel 0                            | 0x0010  | WT       |
| <a href="#">DMA2D_OUT_INT_RAW_CH1_REG</a>      | Raw interrupt status of TX channel 1                            | 0x0104  | R/WTC/SS |
| <a href="#">DMA2D_OUT_INT_ENA_CH1_REG</a>      | Interrupt enable bits of TX channel 1                           | 0x0108  | R/W      |

| Name   | Description  | Address | Access   |
|--|--|---------|----------|
| <a href="#">DMA2D_OUT_INT_ST_CH1_REG</a>       | Masked interrupt status of TX channel 1  | 0x010C  | RO       |
| <a href="#">DMA2D_OUT_INT_CLR_CH1_REG</a>      | Interrupt clear bits of TX channel 1   | 0x0110  | WT       |
| <a href="#">DMA2D_OUT_INT_RAW_CH2_REG</a>      | Raw interrupt status of TX channel 2   | 0x0204  | R/WTC/SS |
| <a href="#">DMA2D_OUT_INT_ENA_CH2_REG</a>      | Interrupt enable bits of TX channel 2  | 0x0208  | R/W      |
| <a href="#">DMA2D_OUT_INT_ST_CH2_REG</a>       | Masked interrupt status of TX channel 2  | 0x020C  | RO       |
| <a href="#">DMA2D_OUT_INT_CLR_CH2_REG</a>      | Interrupt clear bits of TX channel 2   | 0x0210  | WT       |
| <a href="#">DMA2D_IN_INT_RAW_CHO_REG</a>       | Raw interrupt status of RX channel 0   | 0x0504  | R/WTC/SS |
| <a href="#">DMA2D_IN_INT_ENA_CHO_REG</a>       | Interrupt enable bits of RX channel 0  | 0x0508  | R/W      |
| <a href="#">DMA2D_IN_INT_ST_CHO_REG</a>        | Masked interrupt status of RX channel 0  | 0x050C  | RO       |
| <a href="#">DMA2D_IN_INT_CLR_CHO_REG</a>       | Interrupt clear bits of RX channel 0   | 0x0510  | WT       |
| <a href="#">DMA2D_IN_INT_RAW_CH1_REG</a>       | Raw interrupt status of RX channel 1   | 0x0604  | R/WTC/SS |
| <a href="#">DMA2D_IN_INT_ENA_CH1_REG</a>       | Interrupt enable bits of RX channel 1  | 0x0608  | R/W      |
| <a href="#">DMA2D_IN_INT_ST_CH1_REG</a>        | Masked interrupt status of RX channel 1  | 0x060C  | RO       |
| <a href="#">DMA2D_IN_INT_CLR_CH1_REG</a>       | Interrupt clear bits of RX channel 1   | 0x0610  | WT       |
| <b>Status Registers</b>                        |  |         |          |
| <a href="#">DMA2D_OUTFIFO_STATUS_CHO_REG</a>   | Represents the status of the FIFO of TX channel 0  | 0x0014  | RO       |
| <a href="#">DMA2D_OUT_STATE_CHO_REG</a>        | Represents the working status of the transmit descriptor of TX channel 0   | 0x0024  | RO       |
| <a href="#">DMA2D_OUT_EOF_DES_ADDR_CHO_REG</a> | Represents the transmit descriptor address when EOF occurs on TX channel 0   | 0x0028  | RO       |
| <a href="#">DMA2D_OUT_DSCR_CHO_REG</a>         | Represents the address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 0 | 0x002C  | RO       |
| <a href="#">DMA2D_OUT_DSCR_BFO_CHO_REG</a>     | Represents the address of the current pre-read transmit descriptor on TX channel 0   | 0x0030  | RO       |
| <a href="#">DMA2D_OUT_DSCR_BF1_CHO_REG</a>     | Represents the address of the previous pre-read transmit descriptor on TX channel 0  | 0x0034  | RO       |
| <a href="#">DMA2D_OUTFIFO_STATUS_CH1_REG</a>   | Represents the status of the FIFO of TX channel 1  | 0x0114  | RO       |
| <a href="#">DMA2D_OUT_STATE_CH1_REG</a>        | Represents the working status of the transmit descriptor of TX channel 1   | 0x0124  | RO       |
| <a href="#">DMA2D_OUT_EOF_DES_ADDR_CH1_REG</a> | Represents the transmit descriptor address when EOF occurs on TX channel 1   | 0x0128  | RO       |

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">DMA2D_OUT_DSCR_CH1_REG</a>            | Represents the address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 1 | 0x012C  | RO     |
| <a href="#">DMA2D_OUT_DSCR_BFO_CH1_REG</a>        | Represents the address of the current pre-read transmit descriptor on TX channel 1   | 0x0130  | RO     |
| <a href="#">DMA2D_OUT_DSCR_BF1_CH1_REG</a>        | Represents the address of the previous pre-read transmit descriptor on TX channel 1  | 0x0134  | RO     |
| <a href="#">DMA2D_OUTFIFO_STATUS_CH2_REG</a>      | Represents the status of the FIFO of TX channel 2  | 0x0214  | RO     |
| <a href="#">DMA2D_OUT_STATE_CH2_REG</a>           | Represents the working status of the transmit descriptor of TX channel 2   | 0x0224  | RO     |
| <a href="#">DMA2D_OUT_EOF_DES_ADDR_CH2_REG</a>    | Represents the transmit descriptor address when EOF occurs on TX channel 2   | 0x0228  | RO     |
| <a href="#">DMA2D_OUT_DSCR_CH2_REG</a>            | Represents the address of the next transmit descriptor pointed by the current pre-read transmit descriptor on TX channel 2 | 0x022C  | RO     |
| <a href="#">DMA2D_OUT_DSCR_BFO_CH2_REG</a>        | Represents the address of the current pre-read transmit descriptor on TX channel 2   | 0x0230  | RO     |
| <a href="#">DMA2D_OUT_DSCR_BF1_CH2_REG</a>        | Represents the address of the previous pre-read transmit descriptor on TX channel 2  | 0x0234  | RO     |
| <a href="#">DMA2D_INFIFO_STATUS_CHO_REG</a>       | Represents the status of the FIFO of RX channel 0  | 0x0514  | RO     |
| <a href="#">DMA2D_IN_STATE_CHO_REG</a>            | Represents the working status of the receive descriptor of RX channel 0  | 0x0524  | RO     |
| <a href="#">DMA2D_IN_SUC_EOF_DES_ADDR_CHO_REG</a> | Represents the receive descriptor address when EOF occurs on RX channel 0  | 0x0528  | RO     |
| <a href="#">DMA2D_IN_ERR_EOF_DES_ADDR_CHO_REG</a> | Represents the receive descriptor address when errors occur on RX channel 0  | 0x052C  | RO     |
| <a href="#">DMA2D_IN_DSCR_CHO_REG</a>             | Represents the address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 0   | 0x0530  | RO     |
| <a href="#">DMA2D_IN_DSCR_BFO_CHO_REG</a>         | Represents address of the current pre-read receive descriptor on RX channel 0  | 0x0534  | RO     |
| <a href="#">DMA2D_IN_DSCR_BF1_CHO_REG</a>         | Represents the address of the previous pre-read receive descriptor on RX channel 0   | 0x0538  | RO     |
| <a href="#">DMA2D_INFIFO_STATUS_CH1_REG</a>       | Represents the status of the FIFO of RX channel 1  | 0x0614  | RO     |

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">DMA2D_IN_STATE_CH1_REG</a>            | Represents the working status of the receive descriptor of RX channel 1  | 0x0624  | RO     |
| <a href="#">DMA2D_IN_SUC_EOF_DES_ADDR_CH1_REG</a> | Represents the receive descriptor address when EOF occurs on RX channel 1  | 0x0628  | RO     |
| <a href="#">DMA2D_IN_ERR_EOF_DES_ADDR_CH1_REG</a> | Represents the receive descriptor address when errors occur on RX channel 1  | 0x062C  | RO     |
| <a href="#">DMA2D_IN_DSCR_CH1_REG</a>             | Represents the address of the next receive descriptor pointed by the current pre-read receive descriptor on RX channel 1 | 0x0630  | RO     |
| <a href="#">DMA2D_IN_DSCR_BFO_CH1_REG</a>         | Represents address of the current pre-read receive descriptor on RX channel 1  | 0x0634  | RO     |
| <a href="#">DMA2D_IN_DSCR_BF1_CH1_REG</a>         | Represents the address of the previous pre-read receive descriptor on RX channel 1                                       | 0x0638  | RO     |
| <a href="#">DMA2D_AXI_ERR_REG</a>                 | Represents the status of the AXI bus   | 0x0A00  | RO     |
| <a href="#">DMA2D_DATE_REG</a>                    | Version register   | 0x0A2C  | R/W    |
| <b>Peripheral Select Registers</b>                |  |         |        |
| <a href="#">DMA2D_OUT_PERI_SEL_CHO_REG</a>        | Configures the peripheral connected to TX channel 0  | 0x0038  | R/W    |
| <a href="#">DMA2D_OUT_PERI_SEL_CH1_REG</a>        | Configures the peripheral connected to TX channel 1  | 0x0138  | R/W    |
| <a href="#">DMA2D_OUT_PERI_SEL_CH2_REG</a>        | Configures the peripheral connected to TX channel 2  | 0x0238  | R/W    |
| <a href="#">DMA2D_IN_PERI_SEL_CHO_REG</a>         | Configures the peripheral connected to RX channel 0  | 0x053C  | R/W    |
| <a href="#">DMA2D_IN_PERI_SEL_CH1_REG</a>         | Configures the peripheral connected to RX channel 1  | 0x063C  | R/W    |

## 5.9 Registers

The addresses in this section are relative to 2D-DMA base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

Register 5.1. DMA2D\_OUT\_CONFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0000+0x100\* $n$ )

|   |    |   |   |   |    |    |    |    |   |   |   |    |   |   |   |    |    |    |   |   |     |     |    |   |   |   |   |   |   |   |       |   |   |
|---|----|---|---|---|----|----|----|----|---|---|---|----|---|---|---|----|----|----|---|---|-----|-----|----|---|---|---|---|---|---|---|-------|---|---|
| <div>(reserved)</div> <div>DMA2D_OUT_ARB_WEIGHT_OPT_DIS_CH<sup>n</sup></div> <div>DMA2D_OUT_CMD_DISABLE_CH<sup>n</sup></div> <div>DMA2D_OUT_RST_CH<sup>n</sup></div> <div>(reserved)</div> <div>DMA2D_OUT_REORDER_EN_CHO</div> <div>(reserved)</div> <div>DMA2D_OUT_DSCR_PORT_EN_CH<sup>n</sup></div> <div>DMA2D_OUT_MACRO_BLOCK_SIZE_CH<sup>n</sup></div> <div>DMA2D_OUT_MEM_BURST_LENGTH_CH<sup>n</sup></div> <div>(reserved)</div> <div>DMA2D_OUT_CHECK_OWNER_CH<sup>n</sup></div> <div>DMA2D_OUT_ECC_AES_EN_CH<sup>n</sup></div> <div>DMA2D_OUTDSCR_BURST_EN_CH<sup>n</sup></div> <div>DMA2D_OUT_EOF_MODE_CH<sup>n</sup></div> <div>DMA2D_OUT_AUTO_WBACK_CH<sup>n</sup></div> |    |   |   |   |    |    |    |    |   |   |   |    |   |   |   |    |    |    |   |   |     |     |    |   |   |   |   |   |   |   |       |   |   |
| 31  | 27 |   |   |   | 26 | 25 | 24 | 23 |   |   |   | 17 |   |   |   | 16 | 15 | 12 |   |   |     | 11  | 10 | 9 | 8 | 6 |   | 5 | 4 | 3 | 2     | 1 | 0 |
| 0   | 0  | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0  | 0  | 0  | 0 | 0 | 0x0 | 0x0 |    | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Reset |   |   |
|   |    |   |   |   |    |    |    |    |   |   |   |    |   |   |   |    |    |    |   |   |     |     |    |   |   |   |   |   |   |   |       |   |   |

**DMA2D\_OUT\_AUTO\_WRBACK\_CH<sub>n</sub>** Configures whether to enable automatic outlink write-back when all the data in TX FIFO has been transmitted.

0: Disable

1: Enable

(R/W)

**DMA2D\_OUT\_EOF\_MODE\_CH $n$**  Configures when to generate EOF flag.

0: EOF flag for TX channel *n* is generated when data need to read has been pushed into FIFO of 2DDMA

1: EOF flag for TX channel  $n$  is generated when data need to read has been popped from FIFO of 2DDMA

(R/W)

**DMA2D\_OUTDSCR\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for TX channel  $n$  reading descriptors.

0: Disable

1: Enable

(R/W)

**DMA2D\_OUT\_ECC\_AES\_EN\_CH***n* Configures to enable the access to external memory space for ECC and AES (encrypted) via TX channel *n*.

0: Disable

1: Enable

In this case, the starting address of the space and the corresponding data should be 16-byte aligned.

(R/W)

Continued on the next page...



**Register 5.1. DMA2D\_OUT\_CONFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0000+0x100\* $n$ )**

Continued from the previous page...

**DMA2D\_OUT\_CHECK\_OWNER\_CH $n$**  Configures whether to enable the owner bit check for TX channel  $n$ .

0: Disable

1: Enable

(R/W)

**DMA2D\_OUT\_MEM\_BURST\_LENGTH\_CH $n$**  Configures the burst length for TX channel  $n$ .

0: 8 bytes

1: 16 bytes

2: 32 bytes

3: 64 bytes

4: 128 bytes

Others: Invalid

(R/W)

**DMA2D\_OUT\_MACRO\_BLOCK\_SIZE\_CH $n$**  Configures macroblock size for TX channel  $n$ . Used only in 2D-MOD1 mode.

0: 8 \* 8 pixels

1: 8 \* 16 pixels

2: 16 \* 16 pixels

3: No macroblock

(R/W)

**DMA2D\_OUT\_DSCR\_PORT\_EN\_CH $n$**  Configures whether to enable the DSCR-PORT mode for TX channel  $n$ .

0: Disable

1: Enable

(R/W)

**DMA2D\_OUT\_REORDER\_EN\_CHO** Configures whether to enable macroblock reordering for TX channel 0.

0: Disable

1: Enable

(R/W)

**DMA2D\_OUT\_RST\_CH $n$**  Configures whether to reset TX channel  $n$ .

0: Reset release

1: Reset

(R/W)

Continued on the next page...

**Register 5.1. DMA2D\_OUT\_CONFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0000+0x100\* $n$ )**

Continued from the previous page...

**DMA2D\_OUT\_CMD\_DISABLE\_CH***n* Configures reset command for TX channel *n*.

0: Set 0 after reset release

1: Pause transfers before reset

(R/W)

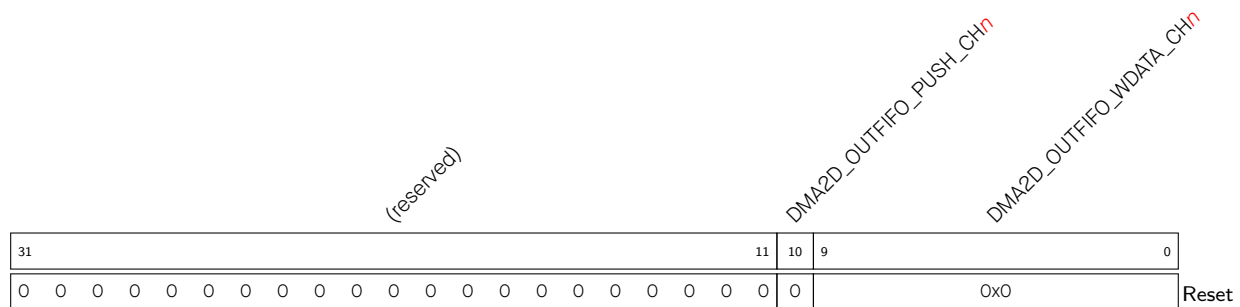
**DMA2D\_OUT\_ARB\_WEIGHT\_OPT\_DIS\_CH $n$**  Configures whether to enable weight optimization for TX channel  $n$ .

0: Enable

1: Disable

(R/W)

**Register 5.2. DMA2D\_OUT\_PUSH\_CH $n$ \_REG ( $n$ : 0-2) (0x0018+0x100\* $n$ )**



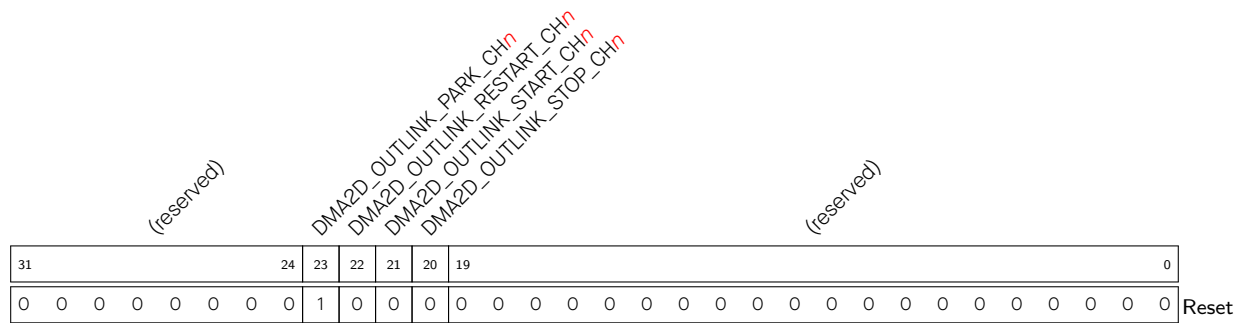
**DMA2D\_OUTFIFO\_WDATA\_CHn** Configures the data to be pushed into the 2D-DMA TX FIFO. (R/W)

**DMA2D\_OUTFIFO\_PUSH\_CH<sub>n</sub>** Configures whether to push data into the 2D-DMA TX FIFO.

0: Not push 1: Push

(R/W/SC)

**Register 5.3. DMA2D\_OUT\_LINK\_CONF\_CH $n$ \_REG ( $n$ : 0-2) (0x001C+0x100\* $n$ )**



**DMA2D\_OUTLINK\_STOP\_CH***n* Configures whether to stop TX channel *n* from transmitting data.

0: Invalid. No effect

1: Stop

(R/W/SC)

**DMA2D\_OUTLINK\_START\_CH***n* Configures whether to enable TX channel *n* for data transfer.

0: Disable

1: Enable

(R/W/SC)

**DMA2D\_OUTLINK\_RESTART\_CH***n* Configures whether to restart TX channel *n* for AXI DMA transfer.

0: Invalid. No effect

1: Restart

(R/W/SC)

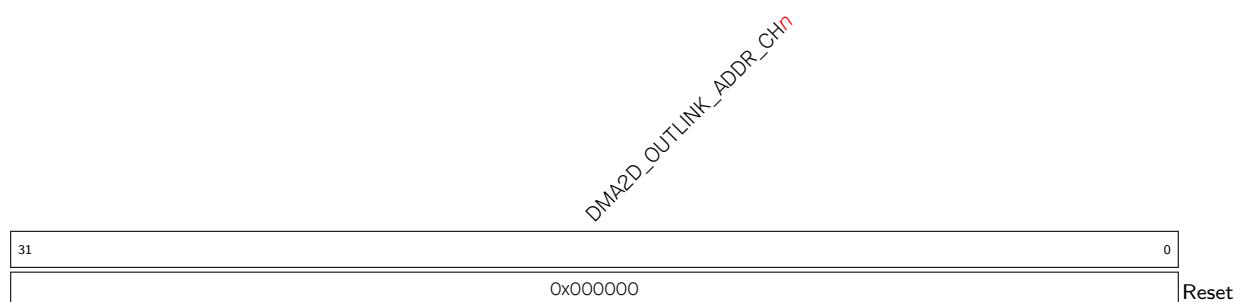
**DMA2D\_OUTLINK\_PARK\_CH<sub>n</sub>** Represents the status of the transmit descriptor's FSM.

0: Running

1: Idle

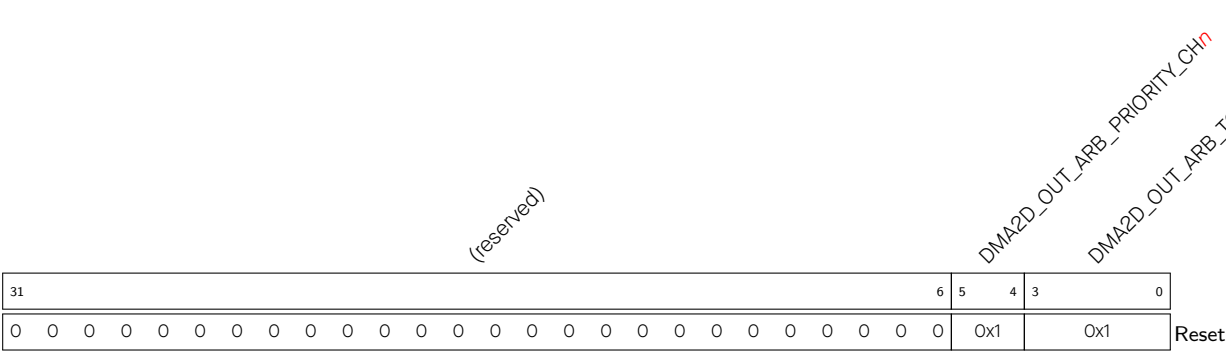
(RO)

Register 5.4. DMA2D\_OUT\_LINK\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0020+0x100\* $n$ )



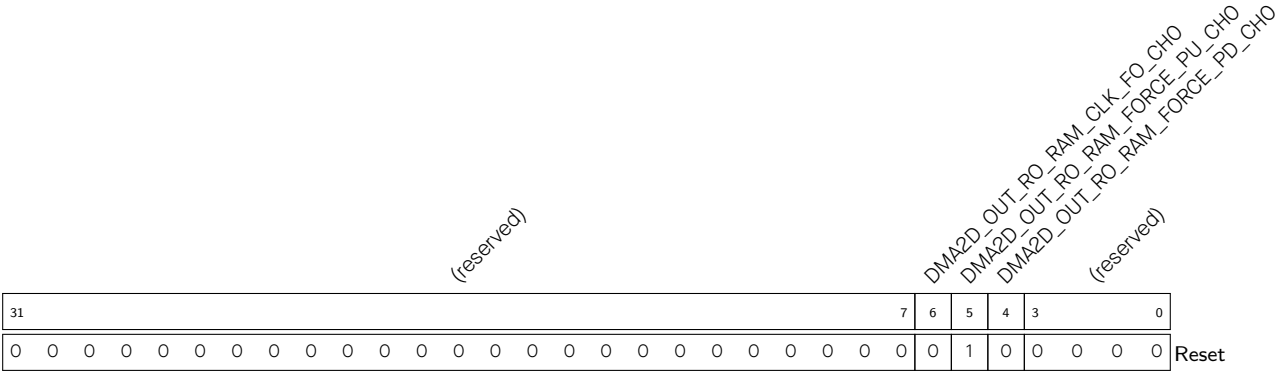
**DMA2D\_OUTLINK\_ADDR\_CH<sub>n</sub>** Represents the first transmit descriptor's address. (R/W)

Register 5.5. DMA2D\_OUT\_ARB\_CHn\_REG (n: 0-2) (0x003C+0x100\*n)



- DMA2D\_OUT\_ARB\_TOKEN\_NUM\_CHn Configures the weight (i.e the number of tokens) of TX channel n.  
Value range: 0 ~ 15. (R/W)
- DMA2D\_OUT\_ARB\_PRIORITY\_CHn Configures the priority of TX channel n. The larger the value, the higher the priority.  
Value range: 0 ~ 3. (R/W)

Register 5.6. DMA2D\_OUT\_RO\_PD\_CONF\_CHO\_REG (0x0044)



**DMA2D\_OUT\_RO\_RAM\_FORCE\_PD\_CHO** Configures whether to force power down the macroblock reordering RAM for TX channel 0.

0: Not force power down

1: Force power down

(R/W)

**DMA2D\_OUT\_RO\_RAM\_FORCE\_PU\_CHO** Configures whether to force power up the macroblock reordering RAM for TX channel 0.

0: Not force power up

1: Force power up

(R/W)

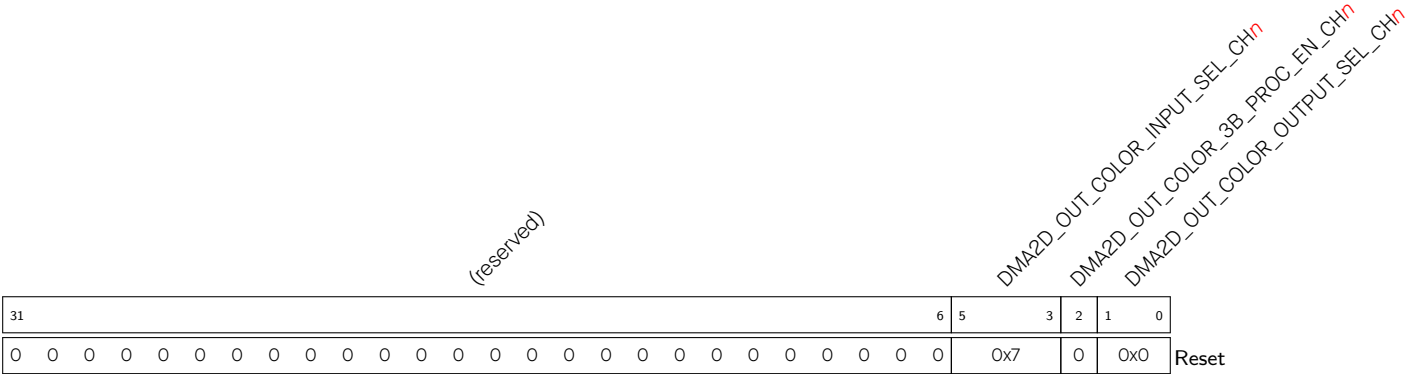
**DMA2D\_OUT\_RO\_RAM\_CLK\_FO\_CHO** Configures the clock gating when TX channel 0 accessing the 2D-DMA RAM.

0: Use the clock gate

1: Force the clock on and bypass the clock gate

(R/W)

Register 5.7. DMA2D\_OUT\_COLOR\_CONVERT\_CHn\_REG (n: 0-2) (0x0048+0x100\*n)

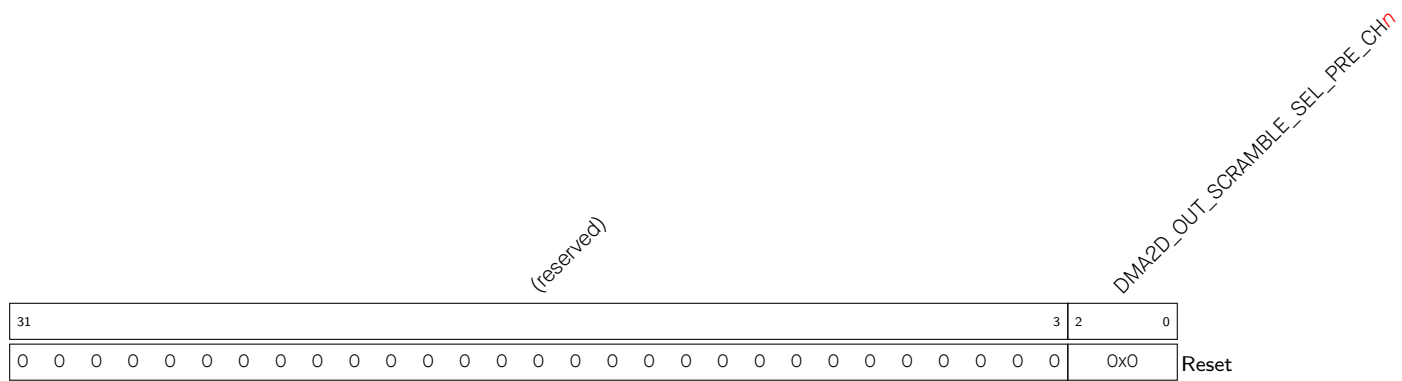


**DMA2D\_OUT\_COLOR\_OUTPUT\_SEL\_CHn** Configures the third stage output of color space conversion for TX channel *n*.  
0: RGB888 to RGB565  
1: YUV444 to YUV422  
2: Output directly  
Others: Invalid  
(R/W)

**DMA2D\_OUT\_COLOR\_3B\_PROC\_EN\_CHn** Configures whether to enable the second stage of color space conversion for TX channel *n*.  
0: Disable  
1: Enable  
(R/W)

**DMA2D\_OUT\_COLOR\_INPUT\_SEL\_CHn** Configures the first stage output of color space conversion for TX channel *n*.  
0: RGB565 to RGB888  
1: YUV422 to YUV444  
2: Other 2 bytes/pixel color format  
3: Other 3 bytes/pixel color format  
7: Disable color space conversion  
Others: Invalid  
(R/W)

Register 5.8. DMA2D\_OUT\_SCRAMBLE\_CH $n$ \_REG ( $n$ : 0-2) (0x004C+0x100\* $n$ )



**DMA2D\_OUT\_SCRAMBLE\_SEL\_PRE\_CH $n$**  Configures the byte order scrambling before the color space conversion for TX channel  $n$ .

- 0: BYTE2-1-0  
1: BYTE2-0-1  
2: BYTE1-0-2  
3: BYTE1-2-0  
4: BYTE0-2-1  
5: BYTE0-1-2  
Others: Invalid  
(R/W)

**Register 5.9. DMA2D\_OUT\_COLOR\_PARAM0\_CH $n$ \_REG ( $n$ : 0-2) (0x0050+0x100\* $n$ )**



**DMA2D\_OUT\_COLOR\_PARAM\_HO\_CH $n$**  Configures the coefficient A and B for the most significant byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

Register 5.10. DMA2D\_OUT\_COLOR\_PARAM1\_CH $n$ \_REG ( $n$ : 0-2) (0x0054+0x100\* $n$ )

|            |    |    |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | DMA2D_OUT_COLOR_PARAM_H1_CH <sup>n</sup> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0 | 0xc86d999                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

Reset

**DMA2D\_OUT\_COLOR\_PARAM\_H1\_CH $n$**  Configures the coefficient C and D for the most significant byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

Register 5.11. DMA2D\_OUT\_COLOR\_PARAM2\_CH $n$ \_REG ( $n$ : 0-2) (0x0058+0x100\* $n$ )

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |          |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|----------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  | DMA2D_OUT_COLOR_PARAM_MO_CH <sup>n</sup> |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |          |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  | 21                                       |  |  |  |  |  |  |  |  |  |  |  | 20 |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | 0 |  |  |  |          |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  | 0x1e712a |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |

Reset

**DMA2D\_OUT\_COLOR\_PARAM\_MO\_CH $n$**  Configures the coefficient A and B for the middle byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

Register 5.12. DMA2D\_OUT\_COLOR\_PARAM3\_CH $n$ \_REG ( $n$ : 0-2) (0x005C+0x100\* $n$ )

|            |    |    |   |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|----|----|---|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |    |    |   | DMA2D_OUT_COLOR_PARAM_M1_CH $n$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         | 28 | 27 |   |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0  | 0  | 0 | 0x21e4f30                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

**DMA2D\_OUT\_COLOR\_PARAM\_M1\_CH $n$**  Configures the coefficient C and D for the middle byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

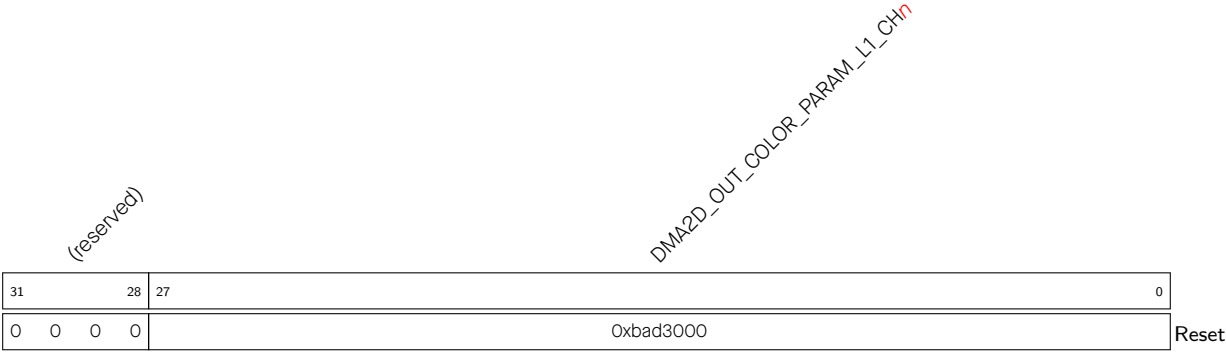


Register 5.13. DMA2D\_OUT\_COLOR\_PARAM4\_CH $n$ \_REG ( $n$ : 0-2) (0x0060+0x100\* $n$ )

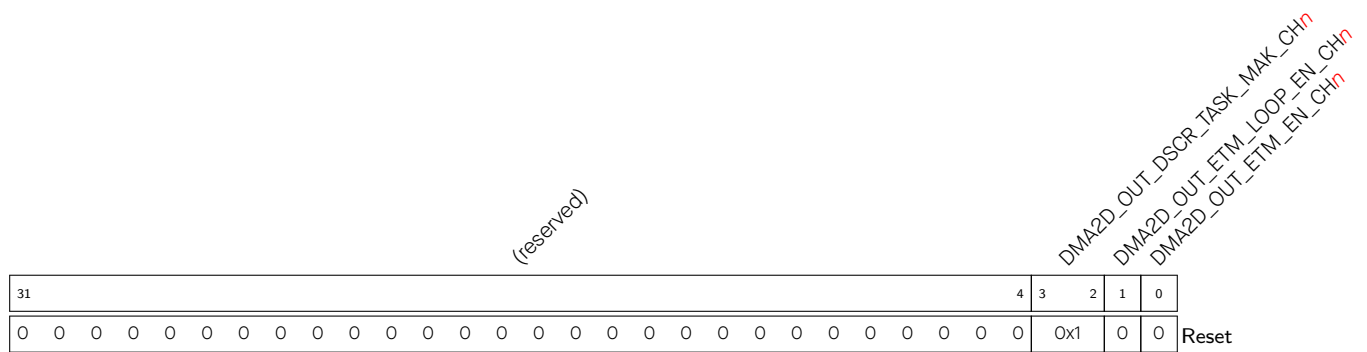


DMA2D\_OUT\_COLOR\_PARAM\_LO\_CH $n$  Configures the coefficient A and B for the least significant byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

Register 5.14. DMA2D\_OUT\_COLOR\_PARAM5\_CH $n$ \_REG ( $n$ : 0-2) (0x0064+0x100\* $n$ )



DMA2D\_OUT\_COLOR\_PARAM\_L1\_CH $n$  Configures the coefficient C and D for the least significant byte of the input of color space conversion's second stage for TX channel  $n$ . (R/W)

Register 5.15. DMA2D\_OUT\_ETM\_CONF\_CH $n$ \_REG ( $n$ : 0-2) (0x0068+0x100\* $n$ )

**DMA2D\_OUT\_ETM\_EN\_CH $n$**  Configures whether to enable the ETM function for TX channel  $n$ .

0: Disable

1: Enable

(R/W)

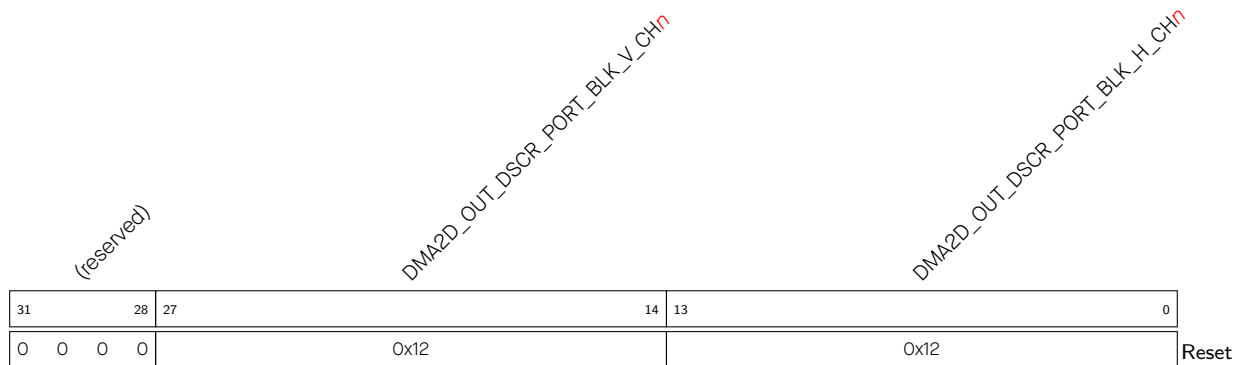
**DMA2D\_OUT\_ETM\_LOOP\_EN\_CH $n$**  Configures whether to use the ETM task to indicate the processing of the next descriptor for TX channel  $n$ .

0: Not use ETM task

1: Use ETM task

(R/W)

**DMA2D\_OUT\_DSCR\_TASK\_MAK\_CH $n$**  Configures the maximum number of tasks that can be cached for TX channel  $n$ . (R/W)

Register 5.16. DMA2D\_OUT\_DSCR\_PORT\_BLK\_CH $n$ \_REG ( $n$ : 0-2) (0x006C+0x100\* $n$ )

**DMA2D\_OUT\_DSCR\_PORT\_BLK\_H\_CH $n$**  Configures the horizontal width of the basic unit for TX channel  $n$  in DSCR-PORT mode.

Measurement unit: pixels. (R/W)

**DMA2D\_OUT\_DSCR\_PORT\_BLK\_V\_CH $n$**  Configures the vertical height of the basic unit for TX channel  $n$  in DSCR-PORT mode.

Measurement unit: pixels. (R/W)

Register 5.17. DMA2D\_IN\_CONFO\_CH $n$ \_REG ( $n$ : 0-1) (0x0500+0x100\* $n$ )

|            |  |   |  |  |  |                                 |  |    |    |    |    |                          |  |  |  |  |   |            |  |  |  |  |    |                         |    |   |  |  |  |            |     |    |     |   |  |                           |   |  |   |   |   |                               |   |   |       |  |  |          |  |  |  |  |  |                               |  |  |  |  |  |                          |  |  |  |  |  |                         |  |  |  |  |  |            |  |  |  |  |  |                              |  |  |  |  |  |                           |  |  |  |  |  |
|------------|--|---|--|--|--|---------------------------------|--|----|----|----|----|--------------------------|--|--|--|--|---|------------|--|--|--|--|----|-------------------------|----|---|--|--|--|------------|-----|----|-----|---|--|---------------------------|---|--|---|---|---|-------------------------------|---|---|-------|--|--|----------|--|--|--|--|--|-------------------------------|--|--|--|--|--|--------------------------|--|--|--|--|--|-------------------------|--|--|--|--|--|------------|--|--|--|--|--|------------------------------|--|--|--|--|--|---------------------------|--|--|--|--|--|
| (reserved) |  |   |  |  |  | DMA2D_IN_ARB_WEIGHT_OPT_DIS_CHn |  |    |    |    |    | DMA2D_IN_CMD_DISABLE_CHn |  |  |  |  |   | (reserved) |  |  |  |  |    | DMA2D_IN_REORDER_EN_CHO |    |   |  |  |  | (reserved) |     |    |     |   |  | DMA2D_IN_DSCR_PORT_EN_CHn |   |  |   |   |   | DMA2D_IN_MACRO_BLOCK_SIZE_CHn |   |   |       |  |  | reserved |  |  |  |  |  | DMA2D_IN_MEM_BURST_LENGTH_CHn |  |  |  |  |  | DMA2D_IN_CHECK_OWNEN_CHn |  |  |  |  |  | DMA2D_IN_ECC_AES_EN_CHn |  |  |  |  |  | (reserved) |  |  |  |  |  | DMA2D_IN_INDSCR_BURST_EN_CHn |  |  |  |  |  | DMA2D_IN_MEM_TRANS_EN_CHn |  |  |  |  |  |
| 31         |  |   |  |  |  | 27                              |  | 26 | 25 | 24 | 23 |                          |  |  |  |  |   |            |  |  |  |  | 17 | 16                      | 15 |   |  |  |  | 12         | 11  | 10 | 9   | 8 |  |                           |   |  | 6 | 5 | 4 | 3                             | 2 | 1 | 0     |  |  |          |  |  |  |  |  |                               |  |  |  |  |  |                          |  |  |  |  |  |                         |  |  |  |  |  |            |  |  |  |  |  |                              |  |  |  |  |  |                           |  |  |  |  |  |
| 0          |  | 0 |  |  |  | 0                               |  | 0  | 0  | 0  | 0  |                          |  |  |  |  | 0 |            |  |  |  |  | 0  | 0                       | 0  | 0 |  |  |  | 0          | 0x0 |    | 0x0 |   |  |                           | 0 |  | 0 | 0 | 0 | 0                             | 0 | 0 | Reset |  |  |          |  |  |  |  |  |                               |  |  |  |  |  |                          |  |  |  |  |  |                         |  |  |  |  |  |            |  |  |  |  |  |                              |  |  |  |  |  |                           |  |  |  |  |  |

**DMA2D\_IN\_MEM\_TRANS\_EN\_CH $n$**  Configures whether to enable memory-to-memory data transfer for TX and RX channel  $n$ .

0: Disable

1: Enable

(R/W)

**DMA2D\_INDSR\_BURST\_EN\_CH $n$**  Configures whether to enable INCR burst transfer for RX channel  $n$  to read descriptors when accessing internal memory.

0: Disable

1: Enable

(R/W)

**DMA2D\_IN\_ECC\_AES\_EN\_CH $n$**  Configures whether to enable the access to external memory space for ECC and AES (encrypted) via RX channel  $n$ .

0: Disable

1: Enable. In this case, the starting address of the space and the corresponding data should be 16-byte aligned.

(R/W)

**DMA2D\_IN\_CHECK\_OWNER\_CH***n* Configures whether to enable the owner bit check for RX channel *n*.

0: Disable

1: Enable

(R/W)

**DMA2D\_IN\_MEM\_BURST\_LENGTH\_CH $n$**  Configures the burst length for RX channel  $n$ .

0: 8 bytes

1: 16 bytes

2: 32 bytes

3: 64 bytes

4: 128 bytes

Others: Invalid

(R/W)

Continued on the next page...

**Register 5.17. DMA2D\_IN\_CONFO\_CH $n$ \_REG ( $n$ : 0-1) (0x0500+0x100\* $n$ )**

Continued from the previous page...

**DMA2D\_IN\_MACRO\_BLOCK\_SIZE\_CH $n$**  Configures macroblock size for RX channel  $n$ . Used only in 2D-MOD1 mode.

0: 8 \* 8 pixels

1: 8 \* 16 pixels

2: 16 \* 16 pixels

3: No macroblock

(R/W)

**DMA2D\_IN\_DSCR\_PORT\_EN\_CH $n$**  Configures whether to enable the DSCR-PORT mode for RX channel  $n$ .

0: Disable

1: Enable

(R/W)

**DMA2D\_IN\_REORDER\_EN\_CHO** Configures whether to enable macroblock reordering for RX channel 0.

0: Disable

1: Enable

(R/W)

**DMA2D\_IN\_RST\_CH $n$**  Configures whether to reset RX channel  $n$ .

0: Invalid

1: Reset

(R/W)

**DMA2D\_IN\_CMD\_DISABLE\_CH $n$**  Configures reset command for RX channel  $n$ .

0: Set 0 after reset release

1: Pause transfers before reset

(R/W)

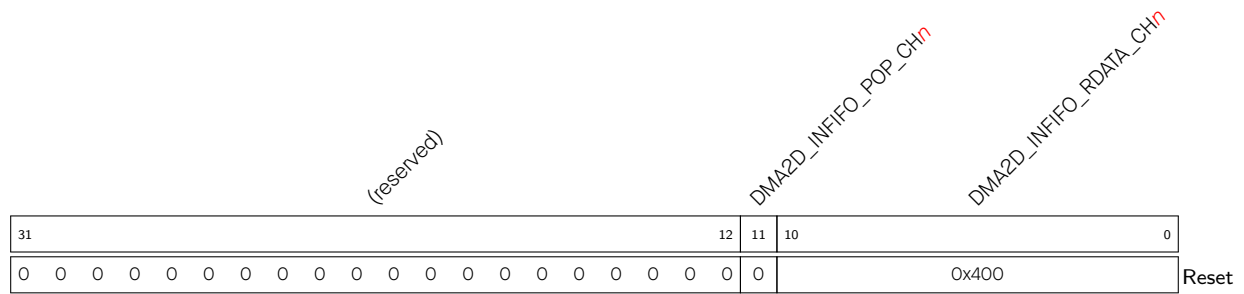
**DMA2D\_IN\_ARB\_WEIGHT\_OPT\_DIS\_CH $n$**  Configures whether to enable weight optimization for RX channel  $n$ .

0: Enable

1: Disable

(R/W)

Register 5.18. DMA2D\_IN\_POP\_CH $n$ \_REG ( $n$ : 0-1) (0x0518+0x100\* $n$ )



**DMA2D\_INFIFO\_RDATA\_CH<sub>n</sub>** Represents the data popped from 2D-DMA RX FIFO. (RO)

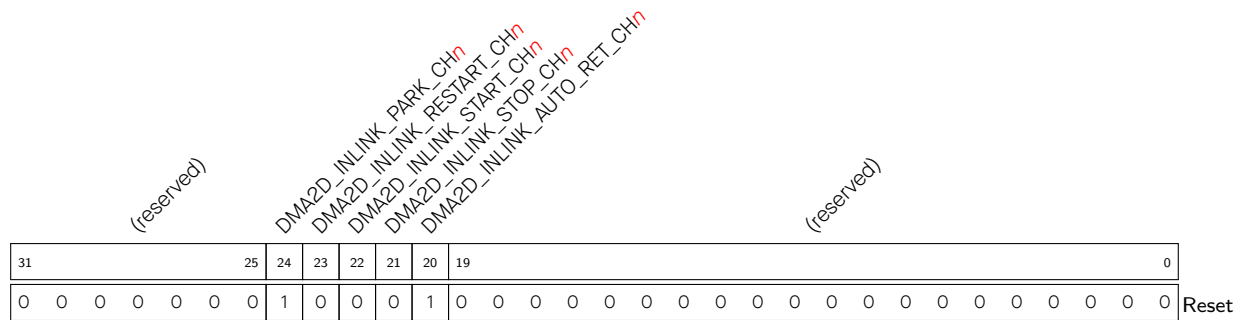
**DMA2D\_INFIFO\_POP\_CH**n Configures whether to pop data from 2D-DMA RX FIFO.

0: Not pop

1: Pop

(R/W/SC)

**Register 5.19. DMA2D\_IN\_LINK\_CONF\_CH $n$ \_REG ( $n$ : 0-1) (0x051C+0x100\* $n$ )**



**DMA2D\_INLINK\_AUTO\_RET\_CH**n Configure the value of the owner bit written back to the receive descriptor.

0: Write back 0

1: Write back 1

(R/W)

**DMA2D\_INLINK\_STOP\_CH***n* Configures whether to stop RX channel *n* from receiving data.

0: Invalid. No effect

1: Stop

(R/W/SC)

**DMA2D\_INLINK\_START\_CH $n$**  Configures whether to enable RX channel  $n$  for data transfer.

0: Disable

1: Enable

(R/W/SC)

**DMA2D\_INLINK\_RESTART\_CH $n$**  Configures whether to restart RX channel  $n$  for 2D-DMA transfer.

0: Invalid. No effect

1: Restart

(R/W/SC)

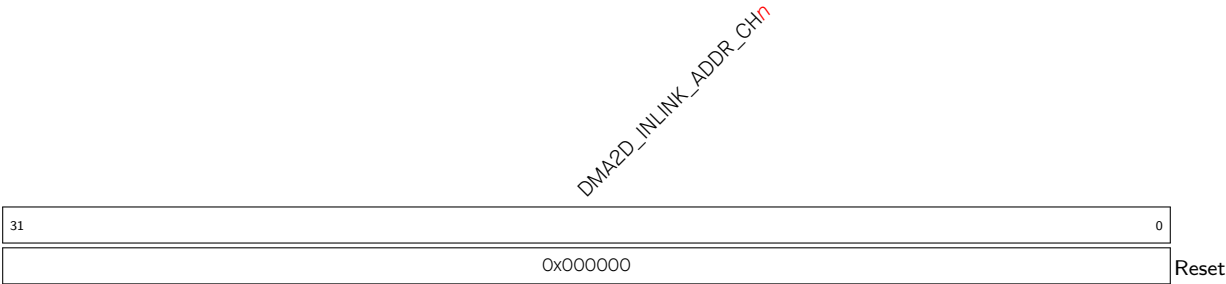
**DMA2D\_INLINK\_PARK\_CH $n$**  Represents the status of the receive descriptor's FSM.

0: Running

1: Idle

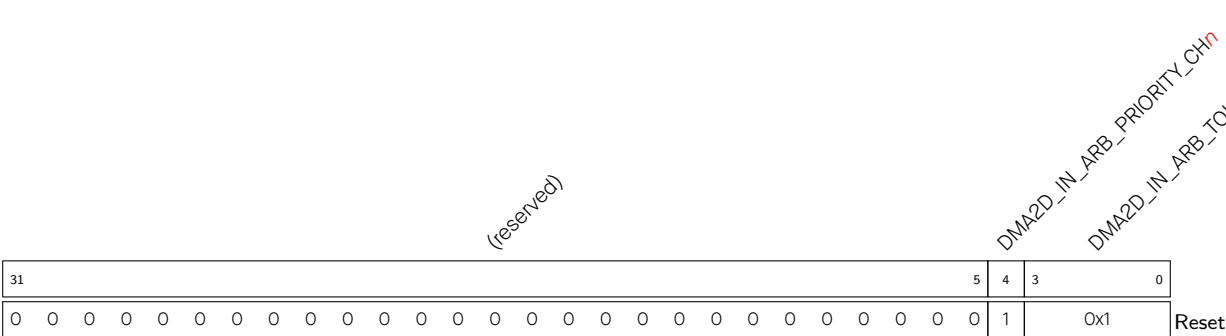
(RO)

Register 5.20. DMA2D\_IN\_LINK\_ADDR\_CH $n$ \_REG ( $n$ : 0-1) (0x0520+0x100\* $n$ )



DMA2D\_INLINK\_ADDR\_CH $n$  Represents the first receive descriptor’s address. (R/W)

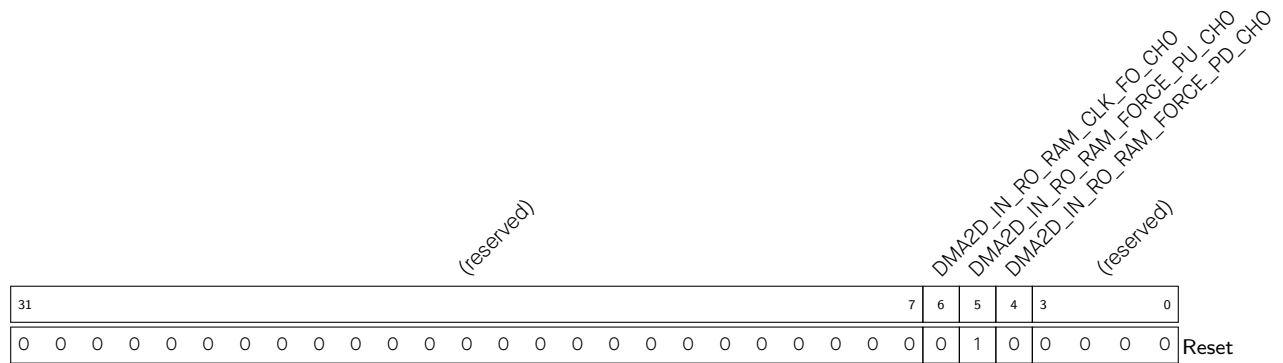
Register 5.21. DMA2D\_IN\_ARB\_CH $n$ \_REG ( $n$ : 0-1) (0x0540+0x100\* $n$ )



DMA2D\_IN\_ARB\_TOKEN\_NUM\_CH $n$  Configures the weight (i.e the number of tokens) of RX channel  $n$ .  
Value range: 0 ~ 15. (R/W)

DMA2D\_IN\_ARB\_PRIORITY\_CH $n$  Configures the priority of RX channel  $n$ . The larger the value, the higher the priority.  
Value range: 0 ~ 3. (R/W)

### Register 5.22. DMA2D\_IN\_RO\_PD\_CONF\_CH0\_REG (0x0548)



|                                     |  |
|-------------------------------------|--|
| <b>DMA2D_IN_RO_RAM_FORCE_PD_CHO</b> | Configures whether to force power down the macroblock reordering RAM for RX channel 0. |
|-------------------------------------|--|

0: Not force power down

1: Force power down

(R/W)

|                                     |   |
|-------------------------------------|---|
| <b>DMA2D_IN_RO_RAM_FORCE_PU_CHO</b> | Configures whether to force power up the macroblock re-ordering RAM for RX channel 0. |
|-------------------------------------|---|

0: Not force power up

1: Force power up

(R/W)

**DMA2D\_IN\_RO\_RAM\_CLK\_FO\_CHO** Configures the clock gating when RX channel 0 accessing the 2D-DMA RAM.

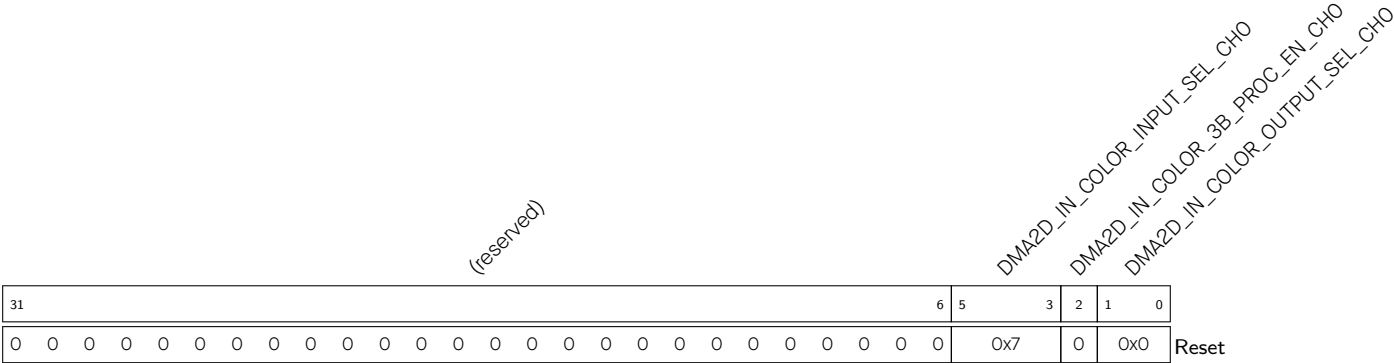
0: Use the clock gate

1: Force the clock on and bypass the clock gate

(R/W)



Register 5.23. DMA2D\_IN\_COLOR\_CONVERT\_CHO\_REG (0x054C)



**DMA2D\_IN\_COLOR\_OUTPUT\_SEL\_CHO** Configures the third stage output of color space conversion for RX channel 0.

0: RGB888 to RGB565

1: Output directly

(R/W)

**DMA2D\_IN\_COLOR\_3B\_PROC\_EN\_CHO** Configures whether to enable the second stage of color space conversion for RX channel 0.

0: Disable

1: Enable

(R/W)

**DMA2D\_IN\_COLOR\_INPUT\_SEL\_CHO** Configures the first stage output of color space conversion for RX channel 0.

0: YUV422/420 to YUV444

1: YUV422

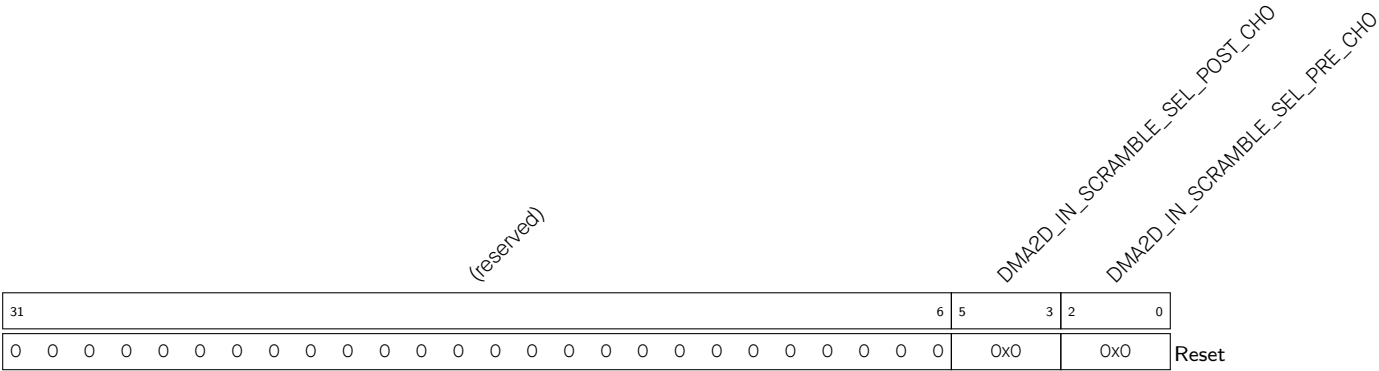
2: YUV444/420

7: Disable color space conversion

Others: Invalid

(R/W)

Register 5.24. DMA2D\_IN\_SCRAMBLE\_CHO\_REG (0x0550)



**DMA2D\_IN\_SCRAMBLE\_SEL\_PRE\_CHO** Configures the byte order scrambling before the color space conversion for RX channel 0.

- 0: BYTE2-1-0
- 1: BYTE2-0-1
- 2: BYTE1-0-2
- 3: BYTE1-2-0
- 4: BYTE0-2-1
- 5: BYTE0-1-2
- Others: Invalid

(R/W)

**DMA2D\_IN\_SCRAMBLE\_SEL\_POST\_CHO** Configures the byte order scrambling after the color space conversion for RX channel 0.

- 0: BYTE2-1-0
- 1: BYTE2-0-1
- 2: BYTE1-0-2
- 3: BYTE1-2-0
- 4: BYTE0-2-1
- 5: BYTE0-1-2
- Others: Invalid

(R/W)

### Register 5.25. DMA2D\_IN\_COLOR\_PARAM0\_CHO\_REG (0x0554)

Diagram illustrating the structure of the `DMA2D_IN_COLOR_PARAM_HO_CH0` register. The register is 32 bits wide, divided into a 12-bit reserved field (bits 31-20) and a 20-bit data field (bits 19-0). The data field contains the value `0x012a`. The register is labeled `DMA2D_IN_COLOR_PARAM_HO_CH0` and has a `Reset` value of `0x012a`.

**DMA2D\_IN\_COLOR\_PARAM\_HO\_CHO** Configures the coefficient A and B for the most significant byte of the input of color space conversion's second stage for RX channel 0. (R/W)

### Register 5.26. DMA2D\_IN\_COLOR\_PARAM1\_CHO\_REG (0x0558)

|            |    |    |   |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | DMA2D_IN_COLOR_PARAM_H1_CH0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 | 0 |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0 | 0xc86d999                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**DMA2D\_IN\_COLOR\_PARAM\_H1\_CHO** Configures the coefficient C and D for the most significant byte of the input of color space conversion's second stage for RX channel 0. (R/W)

### Register 5.27. DMA2D\_IN\_COLOR\_PARAM2\_CHO\_REG (0x055C)

|            |    |                             |   |
|------------|----|-----------------------------|---|
| 31         | 21 | 20                          | 0 |
| (reserved) |    | DMA2D_IN_COLOR_PARAM_MO_CHO |   |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0          | 0  | 0                           | 0 |
| 0x1e712a   |    |                             |   |
| Reset      |    |                             |   |

**DMA2D\_IN\_COLOR\_PARAM\_MO\_CHO** Configures the coefficient A and B for the middle byte of the input of color space conversion's second stage for RX channel 0. (R/W)

Register 5.28. DMA2D\_IN\_COLOR\_PARAM3\_CHO\_REG (0x0560)

|            |    |    |   |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|----|----|---|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | DMA2D_IN_COLOR_PARAM_M1_CHO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 0x21e4f30                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**DMA2D\_IN\_COLOR\_PARAM\_M1\_CHO** Configures the coefficient C and D for the middle byte of the input of color space conversion's second stage for RX channel 0. (R/W)

**Register 5.29. DMA2D\_IN\_COLOR\_PARAM4\_CHO\_REG (0x0564)**

|                     |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |
|---------------------|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|---|--|
| (reserved)          |  |  |  |  |  |  |  |  |  | DMA2D_IN_COLOR_PARAM_LO_CHO |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |
| 31                  |  |  |  |  |  |  |  |  |  | 21                          |  |  |  |  |  |  |  |  |  | 20 |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  | 0 |  |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  | 0x8112a                     |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |   |  |

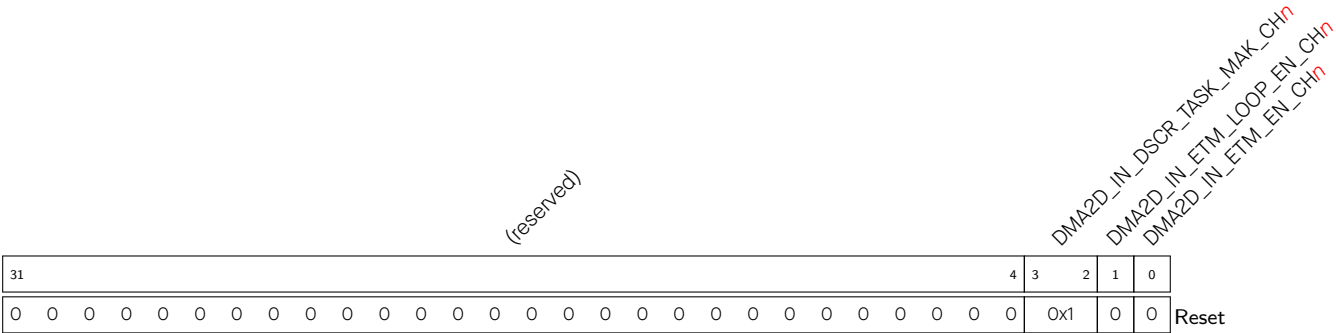
**DMA2D\_IN\_COLOR\_PARAM\_LO\_CHO** Configures the coefficient A and B for the least significant byte of the input of color space conversion's second stage for RX channel 0. (R/W)

### Register 5.30. DMA2D\_IN\_COLOR\_PARAM5\_CHO\_REG (0x0568)

|            |    |    |   |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | DMA2D_IN_COLOR_PARAM_L1_CHO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 | 0 |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0 | 0xbad3000                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**DMA2D\_IN\_COLOR\_PARAM\_L1\_CHO** Configures the coefficient C and D for the least significant byte of the input of color space conversion's second stage for RX channel 0. (R/W)

Register 5.31. DMA2D\_IN\_ETM\_CONF\_CHn\_REG (n: 0-1) (0x056C+0x100\*n)



**DMA2D\_IN\_ETM\_EN\_CHn** Configures whether to enable the ETM function for RX channel *n*.  
0: Disable  
1: Enable  
(R/W)

**DMA2D\_IN\_ETM\_LOOP\_EN\_CHn** Configures whether to use the ETM task to indicate the processing of the next descriptor for RX channel *n*.  
0: Not use ETM task  
1: Use ETM task  
(R/W)

**DMA2D\_IN\_DSCR\_TASK\_MAK\_CHn** Configures the maximum number of tasks that can be cached for RX channel *n*. (R/W)

### Register 5.32. DMA2D\_RST\_CONF\_REG (0x0A04)

[illegible]

**DMA2D\_AXIM\_RD\_RST** Configures whether to reset the AXI master read data FIFO.

0: No effect

1: Reset

(R/W)

**DMA2D\_AXIM\_WR\_RST** Configures whether to reset the AXI master write data FIFO.

0: No effect

1: Reset

(R/W)

**DMA2D\_CLK\_EN** Configures the clock for registers.

0: Support clock only when application writes registers

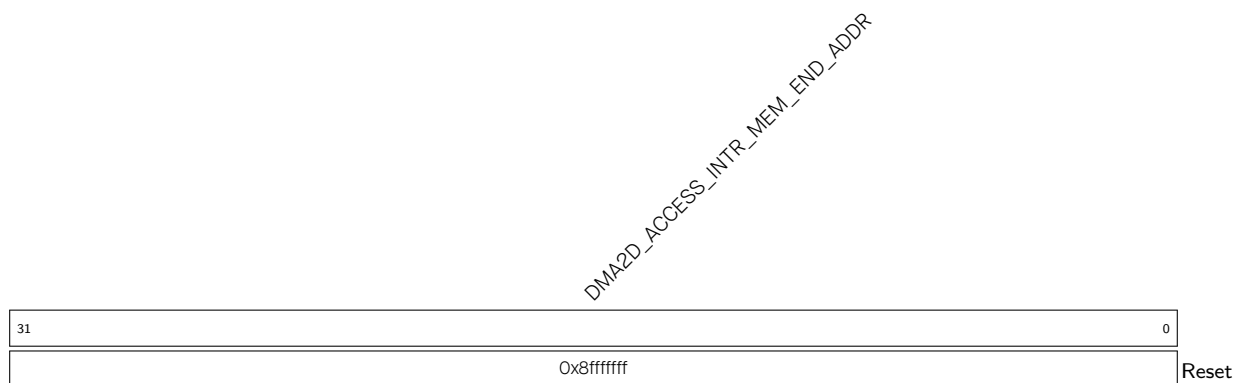
1: Force clock on for register

(R/W)

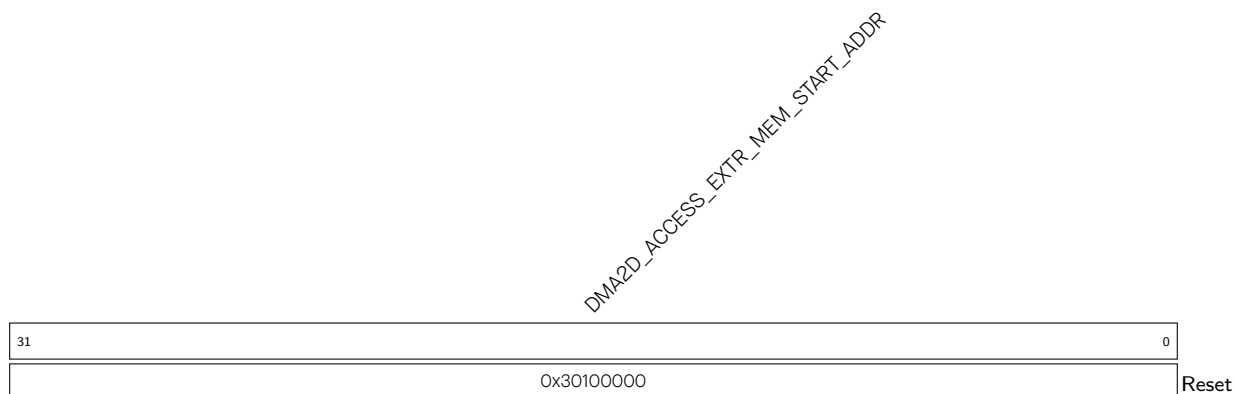
### Register 5.33. DMA2D\_INTR\_MEM\_START\_ADDR\_REG (0x0A08)

Diagram of the DMA2D\_ACCESS\_INTR\_MEM\_START\_ADDR register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value 0x30100000 is shown in the center. The label 'DMA2D\_ACCESS\_INTR\_MEM\_START\_ADDR' is written diagonally across the register.

|   |  |
|---|--|
| <b>DMA2D_ACCESS_INTR_MEM_START_ADDR</b> | Configures the start address of the accessible internal address space. (R/W) |
|---|--|

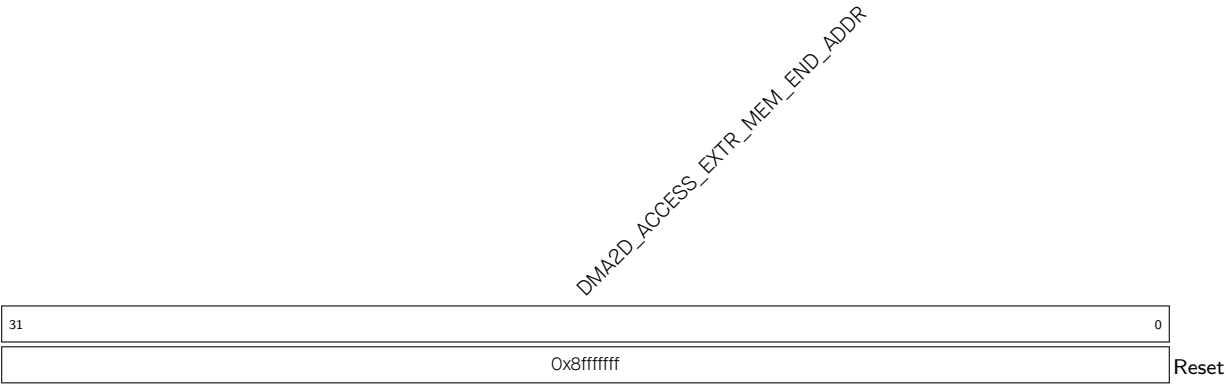
**Register 5.34. DMA2D\_INTR\_MEM\_END\_ADDR\_REG (0x0A0C)**

**DMA2D\_ACCESS\_INTR\_MEM\_END\_ADDR** Configures the end address of the accessible internal address space. Accessing an address beyond this range will result in a descriptor error. (R/W)

**Register 5.35. DMA2D\_EXTR\_MEM\_START\_ADDR\_REG (0x0A10)**

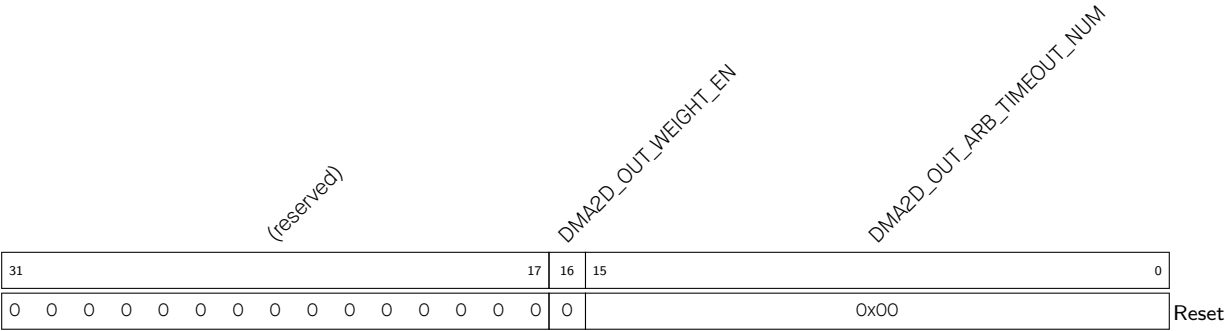
**DMA2D\_ACCESS\_EXTR\_MEM\_START\_ADDR** Configures the start address of the accessible external address space. (R/W)

Register 5.36. DMA2D\_EXTR\_MEM\_END\_ADDR\_REG (0x0A14)



**DMA2D\_ACCESS\_EXTR\_MEM\_END\_ADDR** Configures the end address of the accessible external address space. Accessing an address beyond this range will result in a descriptor error. (R/W)

Register 5.37. DMA2D\_OUT\_ARB\_CONFIG\_REG (0x0A18)



**DMA2D\_OUT\_ARB\_TIMEOUT\_NUM** Configures the time slot for TX. Measurement unit: AXI bus clock cycle. (R/W)

**DMA2D\_OUT\_WEIGHT\_EN** Configures whether to enable weight arbitration for TX.

- 0: Disable
- 1: Enable

(R/W)



### Register 5.38. DMA2D\_IN\_ARB\_CONFIG\_REG (0x0A1C)

Diagram of the DMA2D\_IN\_WEIGHT\_EN register structure:

|      |    |    |    |   |
|------|----|----|----|---|
| 31   | 17 | 16 | 15 | 0 |
| 0x00 |    |    |    |   |

Labels for fields:

- (reserved) [31:17]
- DMA2D\_IN\_WEIGHT\_EN [16]
- DMA2D\_IN\_ARB\_TIMEOUT\_NUM [15:0]

Reset value: 0x00

**DMA2D\_IN\_ARB\_TIMEOUT\_NUM** Configures the time slot for RX. Measurement unit: AXI bus clock cycle. (R/W)

**DMA2D\_IN\_WEIGHT\_EN** Configures whether to enable weight arbitration for RX.

0: Disable

1: Enable

(R/W)

Register 5.39. DMA2D\_OUT\_INT\_RAW\_CH $n$ \_REG ( $n$ : 0-2) (0x0004+0x100\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |   | DMA2D_OUT_DSCR_TASK_OVF_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_RO_UDF_CHO_INT_RAW<br>DMA2D_OUTFIFO_UDF_CHO_INT_RAW<br>DMA2D_OUTFIFO_OVF_L3_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_UDF_L3_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_OVF_L2_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_UDF_L2_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_OVF_L1_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUTFIFO_UDF_L1_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUT_DSCR_ERR_CH <sub>n</sub> _INT_RAW<br>DMA2D_OUT_DONE_CH <sub>n</sub> _INT_RAW |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   | 13 |   |   |   |   |   |   |   |   |   |   |   |   |   | 12  | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   |    |    |   |   |   |   |   |   |   |   |   |   |       |

**DMA2D\_OUT\_DONE\_CH $n$ \_INT\_RAW** The raw interrupt status bit of DMA2D\_OUT\_DONE\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUT\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUT\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT. (R/WTC/SS)

**DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT\_RAW** The raw interrupt status of DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT. (R/WTC/SS)

**DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (R/WTC/SS)

Register 5.40. DMA2D\_OUT\_INT\_ENA\_CH $n$ \_REG ( $n$ : 0-2) (0x0008+0x100\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |  |  |  |  |  |  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**DMA2D\_OUT\_DONE\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUT\_DONE\_CH $n$ \_INT. (R/W)

**DMA2D\_OUT\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUT\_EOF\_CH $n$ \_INT. (R/W)

**DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (R/W)

**DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT. (R/W)

**DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT. (R/W)

**DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT\_ENA** Write 1 to enable the DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT. (R/W)

**DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_ENA** Write 1 to enable the DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (R/W)

Register 5.41. DMA2D\_OUT\_INT\_ST\_CH $n$ \_REG ( $n$ : 0-2) (0x000C+0x100\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|--|--|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   |   | DMA2D_OUT_DSCR_TASK_OVF_CH <sub>n</sub> _INT_ST<br>DMA2D_OUTFIFO_RO_OVF_CHO_INT_ST<br>DMA2D_OUTFIFO_UDF_L3_CH <sub>n</sub> _INT_ST<br>DMA2D_OUTFIFO_UDF_L2_CH <sub>n</sub> _INT_ST<br>DMA2D_OUTFIFO_UDF_L1_CH <sub>n</sub> _INT_ST<br>DMA2D_OUT_TOTAL_EOF_CH <sub>n</sub> _INT_ST<br>DMA2D_OUT_DSCR_ERR_CH <sub>n</sub> _INT_ST<br>DMA2D_OUT_DONE_CH <sub>n</sub> _INT_ST |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5   | 4 | 3 | 2 | 1 | 0 | Reset |  |  |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0   |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |

**DMA2D\_OUT\_DONE\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUT\_DONE\_CH $n$ \_INT. (RO)

**DMA2D\_OUT\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUT\_EOF\_CH $n$ \_INT. (RO)

**DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT. (RO)

**DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_OVF\_L1\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT. (RO)

**DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT. (RO)

**DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT\_ST** The masked interrupt status of DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT. (RO)

**DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of DMA2D\_OUT\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (RO)

Register 5.42. DMA2D\_OUT\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-2) (0x0010+0x100\* $n$ )

Diagram illustrating the DMA2D\_OUT\_DONE register structure. The register is 32 bits wide, with bits 0-13 reserved and bits 12-31 containing 20 status flags. The flags are:

- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 31)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 30)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 29)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 28)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 27)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 26)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 25)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 24)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 23)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 22)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 21)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 20)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 19)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 18)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 17)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 16)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 15)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 14)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 13)
- DMA2D\_OUT\_DONE\_CHn\_INT\_CLR (bit 12)

**DMA2D\_OUT\_DONE\_CH<sub>n</sub>\_INT\_CLR** Write 1 to clear the DMA2D\_OUT\_DONE\_CH<sub>n</sub>\_INT. (WT)

**DMA2D\_OUT\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUT\_EOF\_CH $n$ \_INT. (WT)

**DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUT\_DSCR\_ERR\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUT\_TOTAL\_EOF\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_OVF\_L1\_CH<sub>n</sub>\_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_OVF\_L1\_CH<sub>n</sub>\_INT.  
(WT)

**DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_UDF\_L1\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_OVF\_L2\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_UDF\_L2\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_OVF\_L3\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_UDF\_L3\_CH $n$ \_INT.  
(WT)

**DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_RO\_OVF\_CHO\_INT.  
(WT)

**DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT\_CLR** Write 1 to clear the DMA2D\_OUTFIFO\_RO\_UDF\_CHO\_INT.  
(WT)

|   |   |
|---|---|
| DMA2D_OUT_DSCR_TASK_OVF_CH $n$ _INT_CLR | Write 1 to clear the DMA2D OUT DSCR TASK OVF CH $n$ INT. (WT) |
|---|---|

Register 5.43. DMA2D\_IN\_INT\_RAW\_CH $n$ \_REG ( $n$ : 0-1) (0x0504+0x100\* $n$ )

|                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMA2D_IN_DSCR_TASK_OVF_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_RO_OVF_CHO_INT_RAW<br>DMA2D_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_UDF_L3_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_OVF_L3_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_UDF_L2_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_OVF_L2_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_FIFO_UDF_L1_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_DSCR_ERR_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_SUC_EOF_CH <sub>n</sub> _INT_RAW<br>DMA2D_IN_DONE_CH <sub>n</sub> _INT_RAW |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 14  | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**DMA2D\_IN\_DONE\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_DONE\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT. (R/WTC/SS)

**DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT\_RAW** The raw interrupt status of DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT. (R/WTC/SS)

**DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_RAW** The raw interrupt status of DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (R/WTC/SS)

Register 5.44. DMA2D\_IN\_INT\_ENA\_CH<sub>n</sub>\_REG (*n*: 0-1) (0x0508+0x100\**n*)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | DMA2D_IN_DSCR_TASK_OVF_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_RO_UDF_CHO_INT_ENA<br>DMA2D_INFIFO_RO_UDF_CHO_INT_ENA<br>DMA2D_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_UDF_L3_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_OVF_L3_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_UDF_L2_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_OVF_L2_CH <sub>n</sub> _INT_ENA<br>DMA2D_INFIFO_UDF_L1_CH <sub>n</sub> _INT_ENA<br>DMA2D_IN_DSCR_ERR_CH <sub>n</sub> _INT_ENA<br>DMA2D_IN_ERR_EOF_CH <sub>n</sub> _INT_ENA<br>DMA2D_IN_SUC_EOF_CH <sub>n</sub> _INT_ENA<br>DMA2D_IN_DONE_CH <sub>n</sub> _INT_ENA |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 14  | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     |

**DMA2D\_IN\_DONE\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_DONE\_CH<sub>n</sub>\_INT. (R/W)

**DMA2D\_IN\_SUC\_EOF\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_SUC\_EOF\_CH<sub>n</sub>\_INT. (R/W)

**DMA2D\_IN\_ERR\_EOF\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_ERR\_EOF\_CH<sub>n</sub>\_INT. (R/W)

**DMA2D\_IN\_DSCR\_ERR\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_DSCR\_ERR\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_OVF\_L1\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_OVF\_L1\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_UDF\_L1\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_UDF\_L1\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_OVF\_L2\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_OVF\_L2\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_UDF\_L2\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_UDF\_L2\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_OVF\_L3\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_OVF\_L3\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_INFIFO\_UDF\_L3\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_UDF\_L3\_CH<sub>n</sub>\_INT.  
(R/W)

**DMA2D\_IN\_DSCR\_EMPTY\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_DSCR\_EMPTY\_CH<sub>n</sub>\_INT. (R/W)

**DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT.  
(R/W)

**DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT\_ENA** Write 1 to enable the DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT.  
(R/W)

**DMA2D\_IN\_DSCR\_TASK\_OVF\_CH<sub>n</sub>\_INT\_ENA** Write 1 to enable the DMA2D\_IN\_DSCR\_TASK\_OVF\_CH<sub>n</sub>\_INT. (R/W)

Register 5.45. DMA2D\_IN\_INT\_ST\_CH $n$ \_REG ( $n$ : 0-1) (0x050C+0x100\* $n$ )

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  | DMA2D_IN_DSCR_TASK_OVF_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_RO_OVF_CHO_INT_ST<br>DMA2D_INFIFO_UDF_CHO_INT_ST<br>DMA2D_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_UDF_L3_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_OVF_L3_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_UDF_L2_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_OVF_L2_CH <sub>n</sub> _INT_ST<br>DMA2D_INFIFO_UDF_L1_CH <sub>n</sub> _INT_ST<br>DMA2D_IN_DSCR_ERR_CH <sub>n</sub> _INT_ST<br>DMA2D_IN_ERR_EOF_CH <sub>n</sub> _INT_ST<br>DMA2D_IN_SUC_EOF_CH <sub>n</sub> _INT_ST<br>DMA2D_IN_DONE_CH <sub>n</sub> _INT_ST |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  | 14 |  |  |  |  |  |  |  |  |  |  |  |  |  | 13  | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**DMA2D\_IN\_DONE\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_DONE\_CH $n$ \_INT. (RO)

**DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT. (RO)

**DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT. (RO)

**DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT. (RO)

**DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (RO)

**DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT. (RO)

**DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT\_ST** The masked interrupt status of the DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT. (RO)

**DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_ST** The masked interrupt status of the DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (RO)



Register 5.46. DMA2D\_IN\_INT\_CLR\_CH $n$ \_REG ( $n$ : 0-1) (0x0510+0x100\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   |   |   |   |   |   |       |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | DMA2D_IN_DSCR_TASK_OVF_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_RO_UDF_CHO_INT_CLR<br>DMA2D_INFIFO_RO_UDF_CHO_INT_CLR<br>DMA2D_IN_DSCR_EMPTY_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_UDF_L3_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_UDF_L3_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_UDF_L2_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_UDF_L2_CH <sub>n</sub> _INT_CLR<br>DMA2D_INFIFO_UDF_L1_CH <sub>n</sub> _INT_CLR<br>DMA2D_IN_DSCR_ERR_CH <sub>n</sub> _INT_CLR<br>DMA2D_IN_ERR_EOF_CH <sub>n</sub> _INT_CLR<br>DMA2D_IN_SUC_EOF_CH <sub>n</sub> _INT_CLR<br>DMA2D_IN_DONE_CH <sub>n</sub> _INT_CLR |    |    |    |    |   |   |   |   |   |   |   |   |       |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 14  | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |  |

**DMA2D\_IN\_DONE\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_DONE\_CH $n$ \_INT. (WT)

**DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_SUC\_EOF\_CH $n$ \_INT. (WT)

**DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_ERR\_EOF\_CH $n$ \_INT. (WT)

**DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_DSCR\_ERR\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_OVF\_L1\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_UDF\_L1\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_OVF\_L2\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_UDF\_L2\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_OVF\_L3\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_UDF\_L3\_CH $n$ \_INT. (WT)

**DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_DSCR\_EMPTY\_CH $n$ \_INT. (WT)

**DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_RO\_OVF\_CHO\_INT. (WT)

**DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT\_CLR** Write 1 to clear the DMA2D\_INFIFO\_RO\_UDF\_CHO\_INT. (WT)

**DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT\_CLR** Write 1 to clear the DMA2D\_IN\_DSCR\_TASK\_OVF\_CH $n$ \_INT. (WT)

Register 5.47. DMA2D\_OUTFIFO\_STATUS\_CH $n$ \_REG ( $n$ : 0-2) (0x0014+0x100\* $n$ )

|            |    |    |                                      |    |  |     |                                       |    |                                      |    |  |    |                                       |    |   |   |   |   |   |   |   |   |   |  |   |  |   |  |                                      |  |  |  |                                       |  |
|------------|----|----|--------------------------------------|----|--|-----|---------------------------------------|----|--------------------------------------|----|--|----|---------------------------------------|----|---|---|---|---|---|---|---|---|---|--|---|--|---|--|--------------------------------------|--|--|--|---------------------------------------|--|
| (reserved) |    |    | DMA2D_OUTFIFO_CNT_L3_CH <sup>n</sup> |    | DMA2D_OUTFIFO_EMPTY_L3_CH <sup>n</sup> |     | DMA2D_OUTFIFO_FULL_L3_CH <sup>n</sup> |    | DMA2D_OUTFIFO_CNT_L1_CH <sup>n</sup> |    | DMA2D_OUTFIFO_EMPTY_L1_CH <sup>n</sup> |    | DMA2D_OUTFIFO_FULL_L1_CH <sup>n</sup> |    | DMA2D_OUT_REMAIN_UNDER_8B_CH <sup>n</sup> |   | DMA2D_OUT_REMAIN_UNDER_7B_CH <sup>n</sup> |   | DMA2D_OUT_REMAIN_UNDER_6B_CH <sup>n</sup> |   | DMA2D_OUT_REMAIN_UNDER_5B_CH <sup>n</sup> |   | DMA2D_OUT_REMAIN_UNDER_4B_CH <sup>n</sup> |  | DMA2D_OUT_REMAIN_UNDER_3B_CH <sup>n</sup> |  | DMA2D_OUT_REMAIN_UNDER_2B_CH <sup>n</sup> |  | DMA2D_OUTFIFO_CNT_L2_CH <sup>n</sup> |  | DMA2D_OUTFIFO_EMPTY_L2_CH <sup>n</sup> |  | DMA2D_OUTFIFO_FULL_L2_CH <sup>n</sup> |  |
| 31         | 29 | 28 | 24                                   | 23 | 22                                     | 21  | 17                                    | 16 | 15                                   | 14 | 13                                     | 12 | 11                                    | 10 | 9   | 8 | 7   | 6 | 5   | 2 | 1   | 0 | Reset                                     |  |   |  |   |  |                                      |  |  |  |                                       |  |
| 0          | 0  | 0  | 0x0                                  | 1  | 0                                      | 0x0 | 1                                     | 0  | 1                                    | 1  | 1                                      | 1  | 1                                     | 1  | 1   | 1 | 1   | 0 | 0x0                                       | 1 | 0   |   |   |  |   |  |   |  |                                      |  |  |  |                                       |  |

**DMA2D\_OUTFIFO\_FULL\_L2\_CH $n$**  Represents whether the L2 TX FIFO for TX channel  $n$  is full.

0: Not full

1: Full

(RO)

**DMA2D\_OUTFIFO\_EMPTY\_L2\_CH $n$**  Represents whether the L2 TX FIFO for TX channel  $n$  is empty.

0: Not empty

1: Empty

(RO)

**DMA2D\_OUTFIFO\_CNT\_L2\_CH $n$**  Represents the number of data bytes in L2 TX FIFO for TX channel  $n$ . (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_1B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_2B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_3B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_4B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_5B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_6B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_7B\_CHn Reserved. (RO)

DMA2D\_OUT\_REMAIN\_UNDER\_8B\_CHn Reserved. (RO)

**DMA2D\_OUTFIFO\_FULL\_L1\_CH $n$**  Represents whether the L1 TX FIFO for TX channel  $n$  is full.

0: Not full

1: Full

(RO)

**DMA2D\_OUTFIFO\_EMPTY\_L1\_CH $n$**  Represents whether the L1 TX FIFO for TX channel  $n$  is empty.

0: Not empty

1: Empty

(RO)

**DMA2D\_OUTFIFO\_CNT\_L1\_CH $n$**  Represents the number of data bytes in L1 TX FIFO for TX channel  $n$ . (RO)

Continued on the next page...

Register 5.47. DMA2D\_OUTFIFO\_STATUS\_CHn\_REG (n: 0-2) (0x0014+0x100\*n)

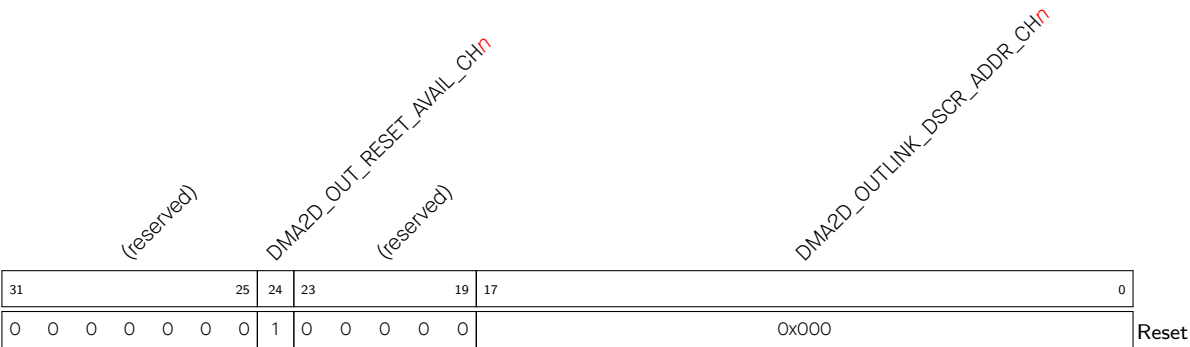
Continued from the previous page...

**DMA2D\_OUTFIFO\_FULL\_L3\_CHn** Represents whether the L3 TX FIFO for TX channel *n* is full.  
0: Not full  
1: Full  
(RO)

**DMA2D\_OUTFIFO\_EMPTY\_L3\_CHn** Represents whether the L3 TX FIFO for TX channel *n* is empty.  
0: Not empty  
1: Empty  
(RO)

**DMA2D\_OUTFIFO\_CNT\_L3\_CHn** Represents the number of data bytes in L3 TX FIFO for TX channel *n*. (RO)

Register 5.48. DMA2D\_OUT\_STATE\_CHn\_REG (n: 0-2) (0x0024+0x100\*n)



**DMA2D\_OUTLINK\_DSCR\_ADDR\_CHn** Represents the lower 18 bits of the next transmit descriptor address that is pre-read (but not processed yet). If the current transmit descriptor is the last descriptor, then this field represents the address of the current transmit descriptor. (RO)

**DMA2D\_OUT\_RESET\_AVAIL\_CHn** Represents whether it is safe to reset TX channel *n*.  
0: Not safe  
1: Safe  
(RO)

Register 5.49. DMA2D\_OUT\_EOF\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-2) (0x0028+0x100\* $n$ )

|                               |   |
|-------------------------------|---|
| DMA2D_OUT_EOF_DES_ADDR_CH $n$ |   |
| 31                            | 0 |
| 0x000000                      |   |
| Reset                         |   |

DMA2D\_OUT\_EOF\_DES\_ADDR\_CH $n$  Represents the address of the transmit descriptor when the eof bit in this descriptor is 1. (RO)

Register 5.50. DMA2D\_OUT\_DSCR\_CH $n$ \_REG ( $n$ : 0-2) (0x002C+0x100\* $n$ )

|                           |   |
|---------------------------|---|
| DMA2D_OUTLINK_DSCR_CH $n$ |   |
| 31                        | 0 |
| 0x000000                  |   |
| Reset                     |   |

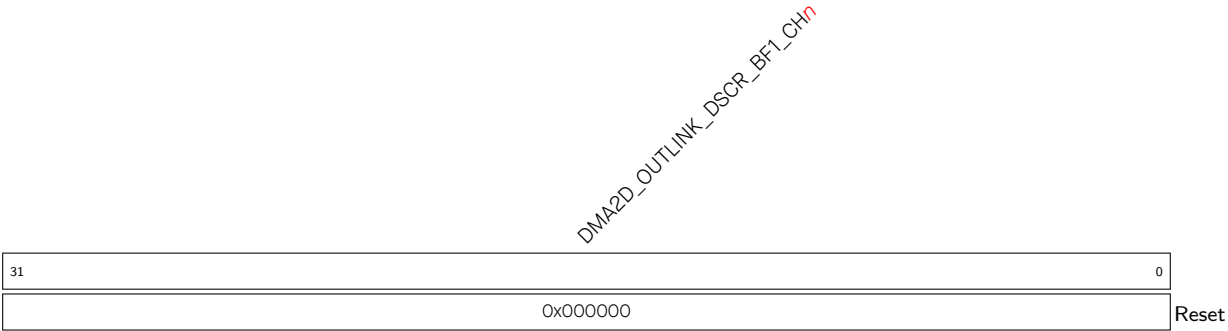
DMA2D\_OUTLINK\_DSCR\_CH $n$  Represents the address of the next transmit descriptor pointed by the current transmit descriptor that is pre-read. (RO)

Register 5.51. DMA2D\_OUT\_DSCR\_BFO\_CH $n$ \_REG ( $n$ : 0-2) (0x0030+0x100\* $n$ )

|                               |   |
|-------------------------------|---|
| DMA2D_OUTLINK_DSCR_BFO_CH $n$ |   |
| 31                            | 0 |
| 0x000000                      |   |
| Reset                         |   |

DMA2D\_OUTLINK\_DSCR\_BFO\_CH $n$  Represents the address of the current transmit descriptor that is pre-read. (RO)

Register 5.52. DMA2D\_OUT\_DSCR\_BF1\_CHn\_REG (n: 0-2) (0x0034+0x100\*n)



DMA2D\_OUTLINK\_DSCR\_BF1\_CHn Represents the address of the previous transmit descriptor that is pre-read. (RO)

**Register 5.53. DMA2D\_INFIFO\_STATUS\_CH $n$ \_REG ( $n$ : 0-1) (0x0514+0x100\* $n$ )**

|            |    |    |                                     |    |    |                                       |    |    |                                      |    |    |                                     |    |    |                                       |   |   |                                      |     |   |                                     |       |  |                                       |  |  |                                      |  |  |
|------------|----|----|-------------------------------------|----|----|---------------------------------------|----|----|--------------------------------------|----|----|-------------------------------------|----|----|---------------------------------------|---|---|--------------------------------------|-----|---|-------------------------------------|-------|--|---------------------------------------|--|--|--------------------------------------|--|--|
| (reserved) |    |    | DMA2D_INFIFO_CNT_L3_CH <sub>n</sub> |    |    | DMA2D_INFIFO_EMPTY_L3_CH <sub>n</sub> |    |    | DMA2D_INFIFO_FULL_L3_CH <sub>n</sub> |    |    | DMA2D_INFIFO_CNT_L1_CH <sub>n</sub> |    |    | DMA2D_INFIFO_EMPTY_L1_CH <sub>n</sub> |   |   | DMA2D_INFIFO_FULL_L1_CH <sub>n</sub> |     |   | DMA2D_INFIFO_CNT_L2_CH <sub>n</sub> |       |  | DMA2D_INFIFO_EMPTY_L2_CH <sub>n</sub> |  |  | DMA2D_INFIFO_FULL_L2_CH <sub>n</sub> |  |  |
| 31         | 29 | 28 | 24                                  | 23 | 22 | 21                                    | 17 | 16 | 15                                   | 14 | 13 | 12                                  | 11 | 10 | 9                                     | 8 | 7 | 6                                    | 5   | 1 | 0                                   |       |  |                                       |  |  |                                      |  |  |
| 0          | 0  | 0  | 0x0                                 | 1  | 0  | 0x0                                   | 1  | 0  | 0                                    | 0  | 0  | 0                                   | 0  | 0  | 0                                     | 0 | 0 | 0                                    | 0x0 | 1 | 0                                   | Reset |  |                                       |  |  |                                      |  |  |

**DMA2D\_INFIFO\_FULL\_L2\_CH $n$**  Represents whether the L2 RX FIFO for RX channel  $n$  is full.

0: Not full

1: Full

(RO)

**DMA2D\_INFIFO\_EMPTY\_L2\_CH $n$**  Represents whether the L2 RX FIFO for RX channel  $n$  is empty.

0: Not empty

1: Empty

(RO)

**DMA2D\_INFIFO\_CNT\_L2\_CH $n$**  Represents the number of data bytes in the L2 RX FIFO for RX channel  $n$ . (RO)

DMA2D\_IN\_REMAIN\_UNDER\_1B\_CHn Reserved. (RO)

DMA2D IN REMAIN UNDER 2B CH Reserved. (RO)

DMA2D\_IN\_REMAIN\_UNDER\_3B\_CHn Reserved. (RO)

DMA2D\_IN\_REMAIN\_UNDER\_4B\_CH<sub>n</sub> Reserved. (RO)

DMA2D IN REMAIN UNDER 5B\_CH Reserved. (RO)

DMA2D IN REMAIN UNDER 6B\_CHn Reserved. (RO)

DMA2D\_IN\_REMAIN\_UNDER\_7B\_CHn Reserved. (RO)

DMA2D IN REMAIN UNDER 8B CH Reserved. (RO)

**DMA2D\_INFIFO\_FULL\_L1\_CH $n$**  Represents whether the L1 RX FIFO for RX channel  $n$  is full.

0: Not full

1: Full

(RO)

**DMA2D\_INFIFO\_EMPTY\_L1\_CH $n$**  Represents whether the L1 RX FIFO for RX channel  $n$  is empty.

0: Not empty

1: Empty

(RO)

**DMA2D\_INFIFO\_CNT\_L1\_CH $n$**  Represents the number of data bytes in the L1 RX FIFO for RX channel  $n$ . (RO)

Continued on the next page...

**Register 5.53. DMA2D\_INFIFO\_STATUS\_CH*n*\_REG (*n*: 0-1) (0x0514+0x100\**n*)**

Continued from the previous page...

**DMA2D\_INFIFO\_FULL\_L3\_CH $n$**  Represents whether the L3 RX FIFO for RX channel  $n$  is full.

0: Not full

1: Full

(RO)

**DMA2D\_INFIFO\_EMPTY\_L3\_CH $n$**  Represents whether the L3 RX FIFO for RX channel  $n$  is empty.

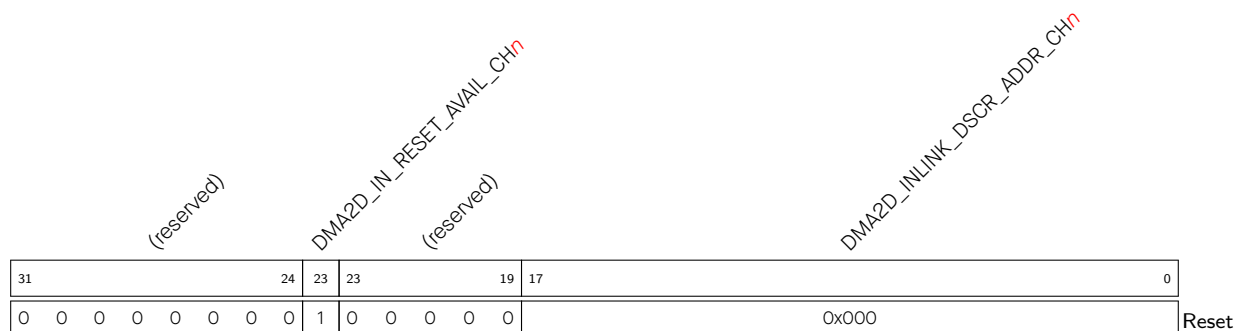
0: Not empty

1: Empty

(RO)

**DMA2D\_INFIFO\_CNT\_L3\_CH $n$**  Represents the number of data bytes in the L3 RX FIFO for RX channel  $n$ . (RO)

Register 5.54. DMA2D\_IN\_STATE\_CH $n$ \_REG ( $n$ : 0-1) (0x0524+0x100\* $n$ )



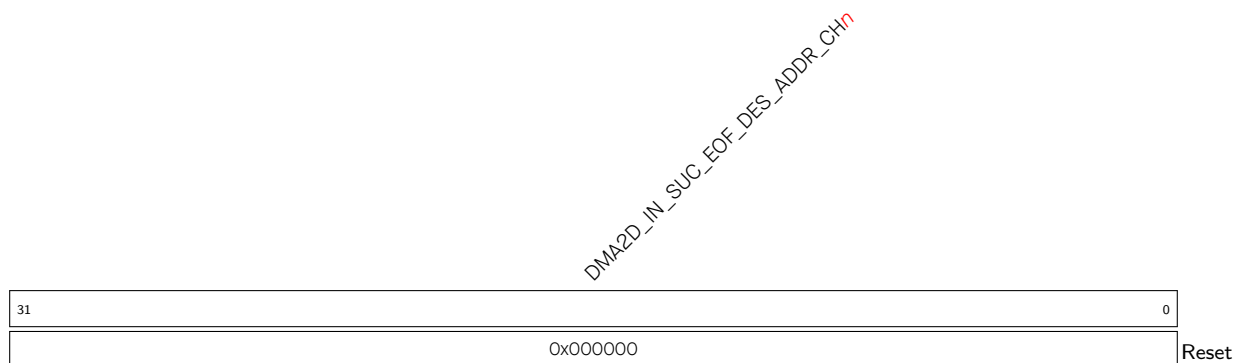
**DMA2D\_INLINK\_DSCR\_ADDR\_CH<sub>n</sub>** Represents the lower 18 bits of the next receive descriptor address that is pre-read (but not processed yet). If the current receive descriptor is the last descriptor, then this field represents the address of the current receive descriptor. (RO)

**DMA2D\_IN\_RESET\_AVAIL\_CH $n$**  Represents whether it is safe to reset RX channel  $n$ .

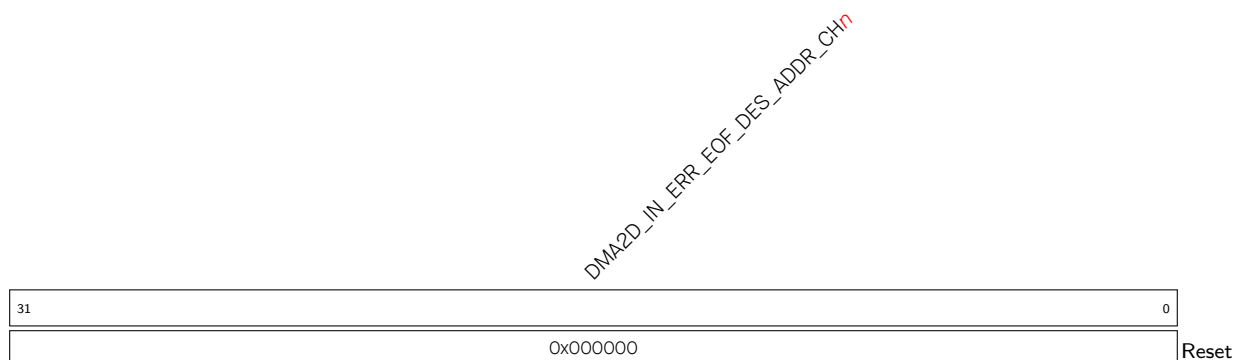
0: Not safe

1: Safe

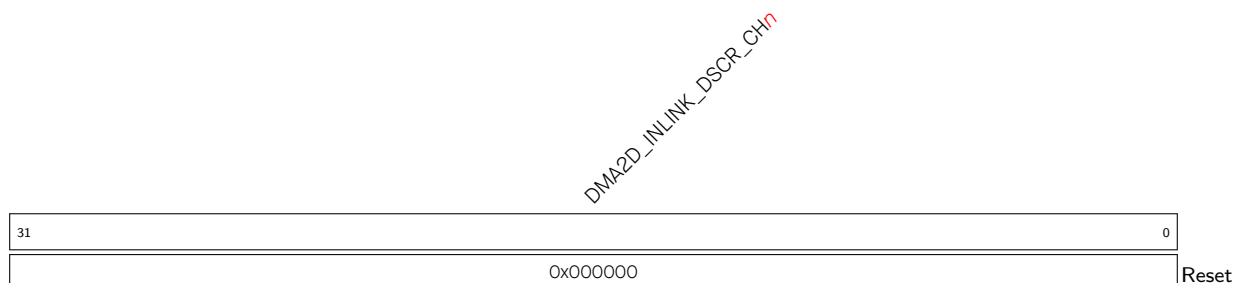
(RO)

**Register 5.55. DMA2D\_IN\_SUC\_EOF\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-1) (0x0528+0x100\* $n$ )**

**DMA2D\_IN\_SUC\_EOF\_DES\_ADDR\_CH $n$**  Represents the address of the receive descriptor when the eof bit in this descriptor is 1. (RO)

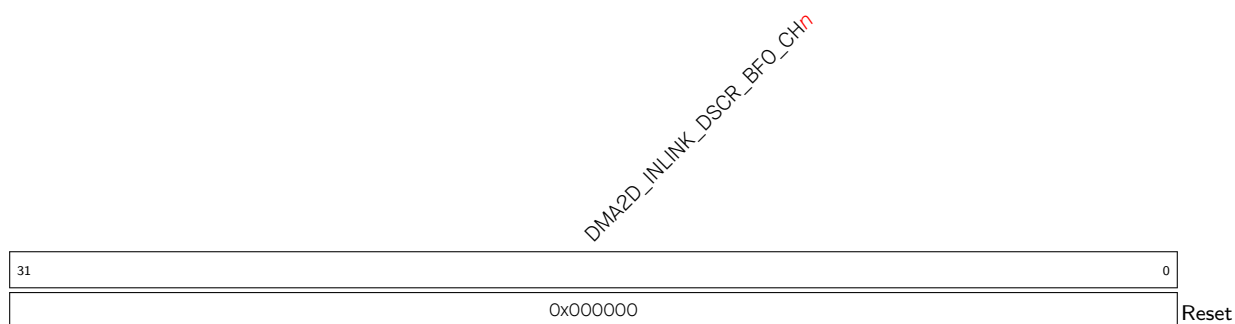
**Register 5.56. DMA2D\_IN\_ERR\_EOF\_DES\_ADDR\_CH $n$ \_REG ( $n$ : 0-1) (0x052C+0x100\* $n$ )**

**DMA2D\_IN\_ERR\_EOF\_DES\_ADDR\_CH $n$**  Represents the address of the receive descriptor when there are some errors in the currently received data. Valid only for JPEG. (RO)

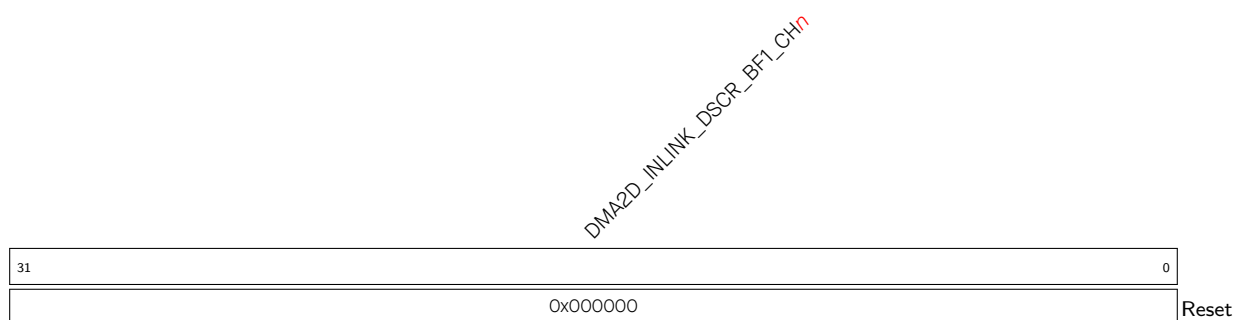
**Register 5.57. DMA2D\_IN\_DSCR\_CH $n$ \_REG ( $n$ : 0-1) (0x0530+0x100\* $n$ )**

**DMA2D\_INLINK\_DSCR\_CH $n$**  Represents the address of the next receive descriptor pointed by the current receive descriptor that is pre-read. (RO)



Register 5.58. DMA2D\_IN\_DSCR\_BFO\_CH $n$ \_REG ( $n$ : 0-1) (0x0534+0x100\* $n$ )

**DMA2D\_INLINK\_DSCR\_BFO\_CH $n$**  Represents the address of the current receive descriptor that is pre-read. (RO)

Register 5.59. DMA2D\_IN\_DSCR\_BF1\_CH $n$ \_REG ( $n$ : 0-1) (0x0538+0x100\* $n$ )

**DMA2D\_INLINK\_DSCR\_BF1\_CH $n$**  Represents the address of the previous receive descriptor that is pre-read. (RO)

### Register 5.60. DMA2D\_AXI\_ERR\_REG (0x0A00)

[illegible]

**DMA2D\_RID\_ERR\_CNT** Represents the number of AXI read ID errors. (RO)

**DMA2D\_RRESP\_ERR\_CNT** Represents the number of AXI read response errors. (RO)

**DMA2D\_WRESP\_ERR\_CNT** Represents the number of AXI write response errors. (RO)

**DMA2D\_RD\_FIFO\_CNT** Represents the number of remaining commands in the AXI read command FIFO. (RO)

**DMA2D\_RD\_BAK\_FIFO\_CNT** Represents the number of remaining commands in the AXI read backup command FIFO. (RO)

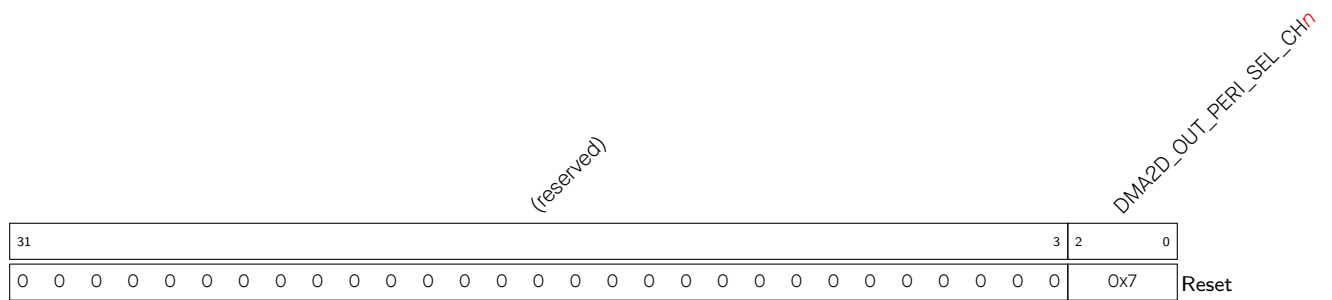
|                          |   |
|--------------------------|---|
| <b>DMA2D_WR_FIFO_CNT</b> | Represents the number of remaining commands in the AXI write command FIFO. (RO) |
|--------------------------|---|

**DMA2D\_WR\_BAK\_FIFO\_CNT** Represents the number of remaining commands in the AXI write backup command FIFO. (RO)

### Register 5.61. DMA2D\_DATE\_REG (0x0A2C)

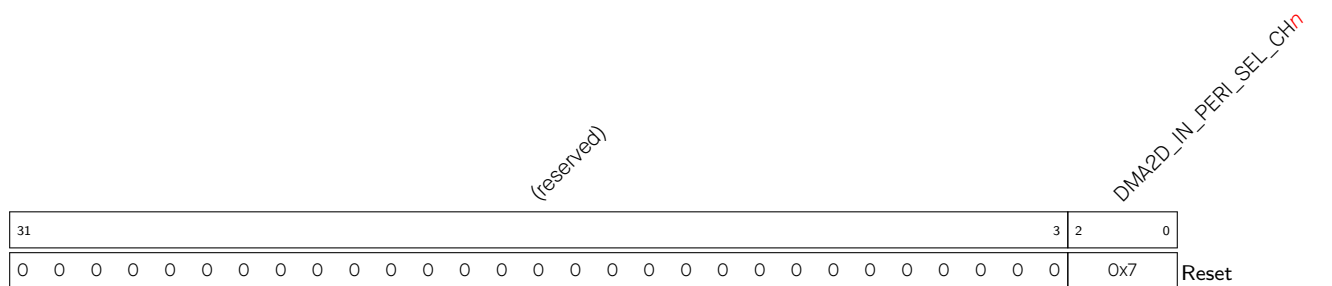
Diagram of DMA2D register DMA2D\_CR. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. Bit 31 is labeled 'DMA2D\_CR\_31'. Bit 0 is labeled 'DMA2D\_CR\_0'. The register value is 0x2304110. A 'Reset' label is at the bottom right.

**DMA2D\_DATE** Version control register. (R/W)

**Register 5.62. DMA2D\_OUT\_PERI\_SEL\_CH $n$ \_REG ( $n$ : 0-2) (0x0038+0x100\* $n$ )**

**DMA2D\_OUT\_PERI\_SEL\_CH $n$**  Configures the peripheral connected to TX channel  $n$ .

- 0: JPEG
  - 1: SRM module of PPA
  - 2: BLEND0 channel of PPA
  - 3: BLEND1 channel of PPA
  - 4 ~ 7: Dummy 4 ~ 7
- (R/W)

**Register 5.63. DMA2D\_IN\_PERI\_SEL\_CH $n$ \_REG ( $n$ : 0-1) (0x053C+0x100\* $n$ )**

**DMA2D\_IN\_PERI\_SEL\_CH $n$**  Configures the peripheral connected to RX channel  $n$ .

- 0: JPEG
  - 1: SRM module of PPA
  - 2: BLEND module of PPA
  - 3 ~ 7: Dummy 3 ~ 7
- (R/W)

## Part III

# Memory Organization

This part provides insights into the system's memory structure, discussing the organization and mapping of RAM, ROM, eFuse, and external memories, offering a framework for understanding memory-related subsystems.

## Chapter 6

# System and Memory

## 6.1 Overview

ESP32-P4 integrates two processors:

- a high-performance 32-bit RISC-V dual-core processor (HP CPU), five-stage pipeline, clock frequency up to 360 MHz.
- a low-power 32-bit RISC-V single-core processor (LP CPU), two-stage pipeline, clock frequency up to 40 MHz.

All internal memory, external memory, and peripherals are located on the HP CPU and LP CPU buses.

## 6.2 Features

- **Address Space**

- 896 KB of HP internal memory address space, accessible by the instruction bus or data bus of HP CPU via cache
- 8 KB of HP internal memory address space, accessible by the instruction bus or data bus of HP CPU
- 48 KB of LP internal memory address space, accessible by the instruction bus or data bus of LP CPU with zero latency
- 1256 KB of peripheral address space
- 64 MB of external flash virtual address space, accessible by the instruction bus or data bus
- 64 MB of external RAM virtual address space, accessible by the instruction bus or data bus
- 768 KB of internal DMA address space
- 128 MB of external DMA address space

- **Internal Memory**

- 128 KB of HP ROM
- 768 KB of HP L2MEM
- 8 KB of HP SPM (Scratchpad Memory)
- 16 KB of LP ROM
- 32 KB of LP SRAM

- **External Memory**

- Supports up to 64 MB of external flash and RAM
- **Peripheral Space**
  - 96 modules/peripherals in total
- **GDMA**
  - 7 GDMA-AHB supported modules/peripherals
  - 6 GDMA-AXI supported modules/peripherals

## 6.3 Functional Description

### 6.3.1 Address Mapping

Figure 6.3-1 illustrates the system structure and address mapping. All the non-reserved addresses are accessible via both the instruction bus and the data bus, meaning that the instruction bus and the data bus share the same address space.

Both the data bus and instruction bus of the HP CPU and LP CPU are little-endian. However, the HP CPU's data bus (DBUS) has a 128-bit data width, while other buses maintain a 32-bit data width.

The HP CPU can access data via the data bus using single-byte, double-byte, 4-byte alignment, and, in case of AI Instruction, up to 16-byte alignment. The LP CPU can access data via the data bus using single-byte, double-byte, and 4-byte alignment.

The HP CPU has the following access capabilities:

- Direct access to HP SPM via both the data bus and instruction bus.
- Access to internal memory and external memory mapped into the address space via cache, including:
  - 128 KB HP ROM (0x4FC0\_0000 ~ 0x4FC1\_FFFF)
  - 768 KB HP L2MEM (0x4FF0\_0000 ~ 0x4FFB\_FFFF)
  - 64 MB external flash (0x4000\_0000 ~ 0x43FF\_FFFF)
  - 64 MB external RAM (0x4800\_0000 ~ 0x4BFF\_FFFF)

**Note:**

Software can use the addresses starting with "0x4" in two ways: cache-able access or noncache-able access, depending on the control of CPU Physical Memory Attribution (PMA). Cache-able access is done via cache. Noncache-able access is done without cache, which is similar to the direct access to the addresses starting with "0x8", however, such direct access to "0x8" addresses is usually for debugging.

- Direct access to internal memory and external memory mapped into the following address space without cache. This access is slower than that via cache.
  - 128 KB HP ROM (0x8FC0\_0000 ~ 0x8FC1\_FFFF)
  - 768 KB HP L2MEM (0x8FF0\_0000 ~ 0x8FFB\_FFFF)
  - 32 KB LP SRAM (0x5010\_8000 ~ 0x5010\_FFFF)

- 64 MB external flash (0x8000\_0000 ~ 0x83FF\_FFFF)
- 64 MB external RAM (0x8800\_0000 ~ 0x8BFF\_FFFF)
- Direct access to modules/peripherals via the data bus, including:
  - HP CPU Peripherals
  - HP Peripherals
  - LP Peripherals

The LP CPU's access capabilities include:

- Direct access to LP SRAM and LP ROM via both the data bus and instruction bus.
- Access to internal memory and external memory, including:
  - 128 KB HP ROM (0x4FC0\_0000 ~ 0x4FC1\_FFFF)
  - 768 KB HP L2MEM (0x4FF0\_0000 ~ 0x4FFB\_FFFF)
  - 64 MB external flash (0x4000\_0000 ~ 0x43FF\_FFFF)
  - 64 MB external RAM (0x4800\_0000 ~ 0x4BFF\_FFFF)
- Direct access to modules/peripherals via the data bus, including:
  - HP CPU Peripherals
  - HP Peripherals
  - LP Peripherals

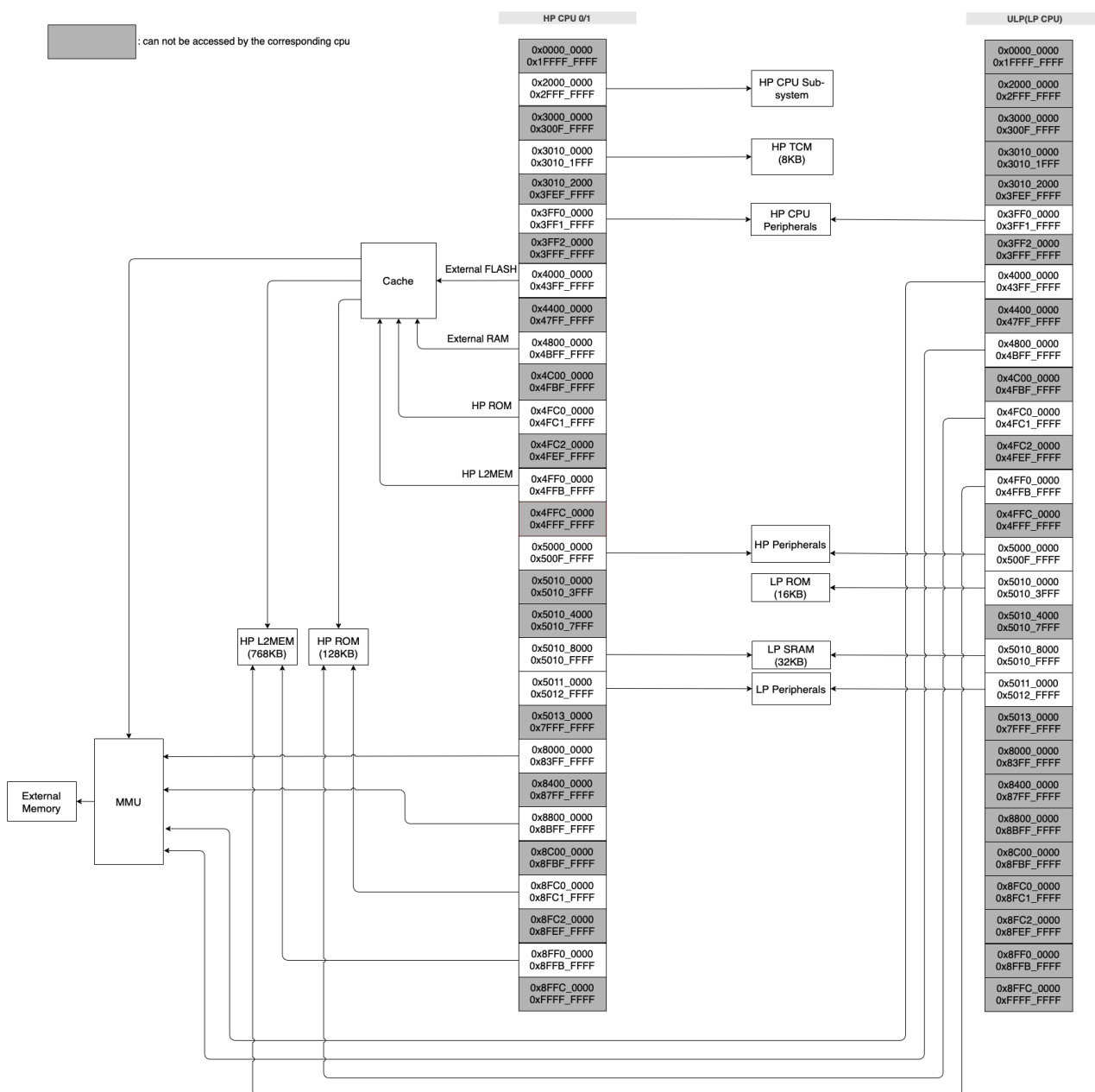


Figure 6.3-1. System Structure and Address Mapping

- The range of addresses available in the address space may be larger than the actual available memory of a particular type.
- For HP CPU sub-system, please refer to Chapter 1 *High-Performance CPU [to be added later]*.

Table 6.3-1 lists the address ranges on the data bus and instruction bus and their corresponding target memories.

Table 6.3-1. Memory Address Mapping

| Bus Type | Boundary Address |              | Size | Target*  |
|----------|------------------|--------------|------|----------|
|          | Low Address      | High Address |      |          |
|          | 0x0000_0000      | 0x300F_FFFF  |      | Reserved |

Cont'd on next page



Table 6.3-1 – cont'd from previous page

| Bus Type             | Boundary Address |              | Size   | Target *                              |
|----------------------|------------------|--------------|--------|---------------------------------------|
|                      | Low Address      | High Address |        |                                       |
| Data/Instruction bus | 0x3010_0000      | 0x3010_1FFF  | 8 KB   | HP SPM                                |
|                      | 0x3010_2000      | 0x3FEF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x3FF0_0000      | 0x3FF1_FFFF  | 128 KB | HP CPU peripherals                    |
|                      | 0x3FF2_0000      | 0x3FFF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x4000_0000      | 0x43FF_FFFF  | 64 MB  | External flash                        |
|                      | 0x4400_0000      | 0x47FF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x4800_0000      | 0x4BFF_FFFF  | 64 MB  | External RAM                          |
|                      | 0x4C00_0000      | 0x4FBF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x4FC0_0000      | 0x4FC1_FFFF  | 128 KB | HP ROM                                |
|                      | 0x4FC2_0000      | 0x4FEF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x4FF0_0000      | 0x4FFB_FFFF  | 768 KB | HP L2MEM                              |
|                      | 0x4FFC_0000      | 0x4FFF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x5000_0000      | 0x500F_FFFF  | 1 MB   | HP peripherals                        |
| Data/Instruction bus | 0x5010_0000      | 0x5010_3FFF  | 16 KB  | LP ROM                                |
|                      | 0x5010_4000      | 0x5010_7FFF  |        | Reserved                              |
| Data/Instruction bus | 0x5010_8000      | 0x5010_FFFF  | 32 KB  | LP SRAM                               |
| Data/Instruction bus | 0x5011_0000      | 0x5012_FFFF  | 128 KB | LP peripherals                        |
|                      | 0x5013_0000      | 0x7FFF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x8000_0000      | 0x83FF_FFFF  | 64 MB  | External flash (direct access by CPU) |
|                      | 0x8400_0000      | 0x87FF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x8800_0000      | 0x8BFF_FFFF  | 64 MB  | External RAM (direct access by CPU)   |
|                      | 0x8C00_0000      | 0x8FBF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x8FC0_0000      | 0x8FC1_FFFF  | 128 KB | HP ROM (direct access by CPU)         |
|                      | 0x8FC2_0000      | 0x8FEF_FFFF  |        | Reserved                              |
| Data/Instruction bus | 0x8FF0_0000      | 0x8FFB_FFFF  | 768 KB | HP L2MEM (direct access by CPU)       |
|                      | 0x8FFC_0000      | 0xFFFF_FFFF  |        | Reserved                              |

\* Address starting with 0x4xxx\_xxxx can be configured as noncache-able or cache-able, depending on CPU PMA, whereas address starting with 0x8xxx\_xxxx is accessed directly by CPU.

\* For the targets accessible by HP CPU or LP CPU, see Figure 6.3-1.

## 6.3.2 Internal Memory

ESP32-P4 has various types of internal memory:

- **HP ROM (128 KB):** This read-only memory is dedicated to the HP system and is not programmable. It contains the ROM code and read-only data of some low-level system software. The HP ROM is accessed by the HP CPU through the I2 cache at half the frequency of HP CPU.
- **HP L2MEM (768 KB):** A volatile memory accessible by the HP CPU, LP CPU, or DMA peripherals at half the frequency of the HP CPU. HP L2MEM can be configured to retain power during Light-sleep mode, making it suitable for data retention or register backup.
- **LP ROM (16 KB):** This read-only memory serves the LP system, containing the code for booting the LP CPU and some basic system functions. The LP ROM is accessed by the LP CPU with zero latency.

- **LP SRAM (32 KB):** A volatile memory accessible by both the HP CPU and LP CPU, operating at the same frequency as the LP CPU.
- **HP SPM (8 KB):** A volatile memory accessed by the HP CPU, finishing one access in two cycles.

### 1. Details for HP ROM

The 128 KB HP ROM is a read-only memory accessed by the HP CPU through the instruction bus or data bus via the following addresses as shown in Table 6.3-1:

- 0x4FC0\_0000 (cache-able or noncache-able, configuration-dependent) ~ 0x4FC1\_FFFF (cache-able or noncache-able, configuration-dependent).
- 0x8FC0\_0000 (direct access by CPU) ~ 0x8FC1\_FFFF (direct access by CPU).

### 2. Details for HP L2MEM

This 768 KB HP L2MEM is a read-and-write memory accessed by the HP CPU or LP CPU through the instruction bus or data bus, or by DMA master through AHB matrix or AXI matrix via the following addresses as shown in Table 6.3-1:

- 0x4FF0\_0000 (cache-able or noncache-able, configuration-dependent) ~ 0x4FFB\_FFFF (cache-able or noncache-able, configuration-dependent).
- 0x8FF0\_0000 (direct access by CPU) ~ 0x8FFB\_FFFF (direct access by CPU).

HP L2MEM can be accessed by various peripherals:

- by USB 2.0 High-speed, USB 2.0 Full-speed, GMAC, SDMMC, TRACE, GDMA-AHB, and SYSMON via AHB matrix.
- by GDMA, GDMA-AXI, 2D-DMA, and H264 Encoder via AXI matrix.

The HP L2MEM supports Error Correction Code (ECC) check to correct one-bit memory flip error. In the event of a one-bit flip error, the data in HP L2MEM still remains valid. Before ECC check, HP L2MEM itself must be initialized first.

HP L2MEM consists of six memory units, each occupying 128 KB. The initialization process allows individual configuration of each unit for power considerations. It is recommended to initialize memory units sequentially rather than simultaneously. This sequential approach helps prevent excessive power consumption and avoids triggering a brownout condition when initializing the entire 768 KB HP L2MEM.

#### Detailed Configuration Steps:

Take unit0 as an example, other units follow the same configuration steps.

- Set `HP_SYSTEM_L2_MEM_UNIT0_REFRESH_EN` and clear `HP_SYSTEM_L2_MEM_REFRESH_CNT_RESET` to start initializing HP L2MEM.
- Read the value of `HP_SYSTEM_L2_MEM_UNIT0_REFRESH_DONE`.
- Once `HP_SYSTEM_L2_MEM_UNIT0_REFRESH_DONE` reaches a value of 1, set `HP_SYSTEM_L2_RAM_UNIT0_ECC_EN` to start ECC check.
- (Recommended) clear `HP_SYSTEM_L2_MEM_UNIT0_REFRESH_EN` and set `HP_SYSTEM_L2_MEM_REFRESH_CNT_RESET` after `HP_SYSTEM_L2_MEM_UNIT0_REFRESH_DONE` reaches 1 to complete the initialization process.

During the initialization process, avoid any access to HP L2MEM unit being initialized.

### 3. Details for LP ROM

This 16 KB LP ROM is a read-only memory accessed by LP CPU through the instruction bus or data bus via their shared address 0x5010\_0000 ~ 0x5010\_3FFF as shown in Table 6.3-1.

### 4. Details for LP SRAM

This 32 KB LP SRAM is a read-and-write memory accessed by the HP CPU via AHB matrix and by the LP CPU through the instruction bus or data bus via their shared address 0x5010\_8000 ~ 0x5010\_FFFF as shown in Table 6.3-1. LP SRAM supports atomic operation.

### 5. Details for HP SPM

This 8 KB HP SPM is a read-and-write memory accessed by the HP CPU through the instruction bus or data bus via their shared address 0x3010\_0000 ~ 0x3010\_1FFF as shown in Table 6.3-1. Additionally, HP SPM supports atomic operation of the HP CPU.

HP SPM supports parity check to detect one-bit memory flip error. Before conducting the parity check, HP SPM itself must be initialized first.

#### Detailed Configuration Steps:

- Set HP\_SYSTEM\_SPM\_INIT\_EN and clear HP\_SYSTEM\_SPM\_INIT\_CNT\_RESET to start initializing HP SPM.
- Read the value of HP\_SYSTEM\_SPM\_INIT\_DONE.
- Once HP\_SYSTEM\_SPM\_INIT\_DONE reaches a value of 1, set HP\_SYSTEM\_HP\_SPM\_PARITY\_CHECK\_EN to start parity check.
- (Recommended) clear HP\_SYSTEM\_SPM\_INIT\_EN and set HP\_SYSTEM\_SPM\_INIT\_CNT\_RESET after HP\_SYSTEM\_SPM\_INIT\_CNT\_RESET reaches 1 to complete the initialization process.

During the above process, avoid any access to HP SPM.

## 6.3.3 External Memory

ESP32-P4 supports SPI, dual SPI, quad SPI and QPI interfaces for connecting to external flash, as well as OPI and HPI interfaces for connecting to external RAM.

ESP32-P4 provides the following security features to protect users' data in external flash and RAM:

- hardware manual encryption and automatic decryption based on XTS-AES algorithm to protect users' programs and data stored in the external flash.
- automatic encryption and decryption based on XTS-AES algorithm to protect users' data in the external RAM.

### 6.3.3.1 External Memory Address Mapping

HP CPU can access external flash or RAM via 0x4000\_0000 ~ 0x43FF\_FFFF or via 0x4800\_0000 ~ 0x4BFF\_FFFF using cache-able or noncache-able methods. HP CPU can also access external flash or RAM directly via 0x8000\_0000 ~ 0x83FF\_FFFF or via 0x8800\_0000 ~ 0x8BFF\_FFFF, which is slower than the access via cache and is therefore commonly used for debugging.

When the HP CPU accesses external memory, it maps the addresses to physical addresses based on the information in the Memory Management Unit (MMU).

- Range (0x4000\_0000 ~ 0x43FF\_FFFF) is mapped to the physical address of the external flash accessed by HP CPU via cache.
- Range (0x4800\_0000 ~ 0x4BFF\_FFFF) is mapped to the physical address of the external RAM accessed by HP CPU via cache.
- Range (0x8000\_0000 ~ 0x83FF\_FFFF) is mapped to the physical address of the external flash accessed by HP CPU directly.
- Range (0x8800\_0000 ~ 0x8BFF\_FFFF) is mapped to the physical address of the external RAM accessed by HP CPU directly.

This mapping allows ESP32-P4 to address up to 64 MB of external flash and 64 MB of external RAM. **Note that** the instruction bus shares the same address space (64 MB) with the data bus for accessing external memory.

### 6.3.3.2 Cache

As shown in Figure 6.3-2, ESP32-P4 has a two-level cache system, with the following features:

- L1 cache, including:
  - 16 KB of instruction cache (icache) with a 64 B block size, four-way set associative
  - 64 KB of data cache (dcache) with a 64 B block size, two-way set associative, supporting two writing strategies: write-through and write-back
- L2 cache: 128 KB/256 KB/512 KB with 64 B/128 B block sizes, eight-way set associative
- Cache-able and noncache-able access, depending on CPU PMA
- Preload operation
- Lock operation
- Critical word first and early restart

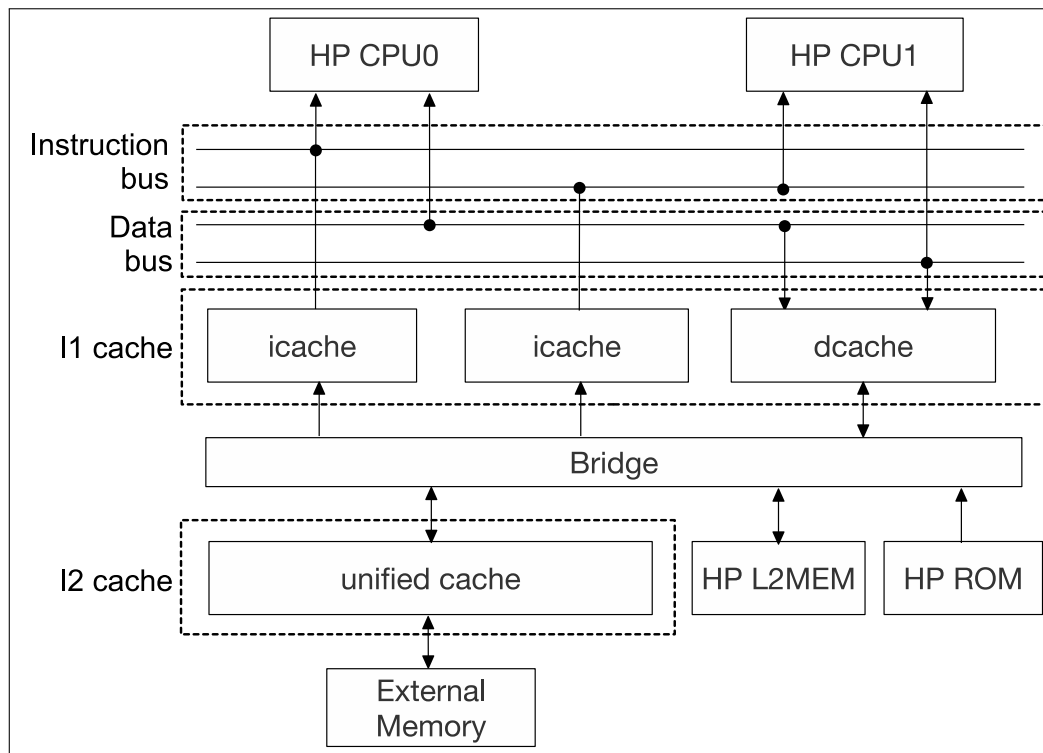


Figure 6.3-2. Cache Structure

### 6.3.3.3 Cache Operations

ESP32-P4 I1 cache and I2 cache supports the following operations:

1. **Write-back** (for dcache and I2 cache only):

- Clears dirty bits in the tag memory and updates new data to external memory.
- After the write-back operation, the new data is updated to external memory.
- Users can choose whether to invalidate the data in the cache.
- If the data is not invalidated, CPU will read/write data directly from/to the cache where data missing will not occur.

2. **Clean** (for dcache and I2 cache only):

- Clears dirty bits in the tag memory without updating data to external memory.
- After the clean operation, old data remains in external memory, while the cache holds the new one (unaware of it).
- CPU can then read/write the data directly from/to the cache, where data missing will not occur.

3. **Invalidate**:

- Removes valid data from the cache.
- Once this operation is done, the deleted data is stored only in external memory.
- HP CPU needs to access external memory if it wants to access the data again.
- Two types of invalidate operation:

- Manual-Invalidate: is performed only on data in the specified cache area.
- Invalidate-All: is performed on all data in the cache.

#### 4. Preload:

- Loads instructions and data into the cache in advance.
- Minimum unit of preload-operation is one block.
- Two types of preload operation:
  - Manual-Preload: involves the hardware prefetching continuous data based on the virtual address specified by the software.
  - Auto-Preload: involves the hardware prefetching continuous data based on the current address where the cache hits or misses (configuration-dependent).

#### 5. Lock/Unlock:

- Lock operation prevents easily replacing data in the cache.
- Two types of lock:
  - Prelock: locks data in the specified area when filling missing data to cache memory, leaving the data outside the specified area unlocked.
  - Manual Lock: checks data in the cache memory and locks data only if it falls in the specified area, leaving data outside the specified area unlocked.
- When there is missing data, the cache replaces the data in the unlocked way first, ensuring that the data in the locked way remains in the cache and will not be replaced.
- When all ways within the cache are locked, the cache will replace data, as if it was not locked.
- Unlocking is the reverse of locking and can only be done manually.
- Note: Manual-Invalidate operation only works on the unlocked data. If you plan to perform this operation on the locked data, please unlock them first.

### 6.3.4 DMA Address Space

ESP32-P4 includes AHB General Direct Memory Access (GDMA-AHB), AXI General Direct Memory Access (GDMA-AXI), and VDMA, all providing general direct memory access services.

In ESP32-P4, masters like USB 2.0 High-speed, USB 2.0 Full-speed, GDMAC, Trace0/1, VDMA, 2D-DMA, and H264 Encoder have built-in DMA function modules, providing direct memory access services.

All DMA-enabled master devices mentioned above can access:

- HP L2MEM (0x4FF0\_0000~0x4FFB\_FFFF).
- external flash (0x4000\_0000 ~ 0x43FF\_FFFF).
- external RAM (0x4800\_0000 ~ 0x4BFF\_FFFF).

Additionally, VDMA Master 1 can also access:

- MIPI CSI internal memory (0x5010\_4000 ~ 0x5010\_4FFF).
- MIPI DSI internal memory (0x5010\_5000 ~ 0x5010\_5FFF).

**Note:**

When accessing a memory via DMA, a corresponding access permission is needed, otherwise this access may fail. For more information about permission control, please refer to Chapter 18 [Permission Control \(PMS\)](#).

### 6.3.5 Modules/Peripherals Address Mapping

Table 6.3-2 lists all the modules/peripherals and their respective address ranges. Note that the address space of specific modules/peripherals is defined by “Boundary Address” (including both Low Address and High Address).

Table 6.3-2. Module/Peripheral Address Mapping

| Target                             | Boundary Address |              | Size (KB) |
|------------------------------------|------------------|--------------|-----------|
|                                    | Low Address      | High Address |           |
| HP CPU Peripherals (HP CPU PERI)   |                  |              |           |
| Reserved                           | 0x3FF0_0000      | 0x3FF0_3FFF  |           |
| RISC-V Trace Encoder 0             | 0x3FF0_4000      | 0x3FF0_4FFF  | 4         |
| RISC-V Trace Encoder 1             | 0x3FF0_5000      | 0x3FF0_5FFF  | 4         |
| Bus Monitor                        | 0x3FF0_6000      | 0x3FF0_6FFF  | 4         |
| Reserved                           | 0x3FF0_7000      | 0x3FF0_DFFF  |           |
| L2MEM Monitor                      | 0x3FF0_E000      | 0x3FF0_EFFF  | 4         |
| SPM Monitor                        | 0x3FF0_F000      | 0x3FF0_FFFF  | 4         |
| HP Peripherals 0 (HP PERIO)        |                  |              |           |
| USB 2.0 OTG High-Speed             | 0x5000_0000      | 0x5003_FFFF  | 256       |
| USB 2.0 OTG Full-Speed             | 0x5004_0000      | 0x5007_FFFF  | 256       |
| USB 2.0 OTG Full-Speed PHY         | 0x5008_0000      | 0x5008_0FFF  | 4         |
| VDMA Controller                    | 0x5008_1000      | 0x5008_1FFF  | 4         |
| Reserved                           | 0x5008_2000      | 0x5008_2FFF  |           |
| SD/MMC Host Controller             | 0x5008_3000      | 0x5008_3FFF  | 4         |
| H264 Encoder                       | 0x5008_4000      | 0x5008_4FFF  | 4         |
| GDMA-AHB                           | 0x5008_5000      | 0x5008_5FFF  | 4         |
| JPEG Codec                         | 0x5008_6000      | 0x5008_6FFF  | 4         |
| Pixel-Processing Accelerator (PPA) | 0x5008_7000      | 0x5008_7FFF  | 4         |
| 2D-DMA Controller                  | 0x5008_6000      | 0x5008_8FFF  | 4         |
| GDMA-AXI                           | 0x5008_A000      | 0x5008_BFFF  | 8         |
| AES Accelerator (AES)              | 0x5009_0000      | 0x5009_0FFF  | 4         |
| SHA Accelerator (SHA)              | 0x5009_1000      | 0x5009_1FFF  | 4         |
| RSA Accelerator (RSA)              | 0x5009_2000      | 0x5009_2FFF  | 4         |
| Digital Signature (DS)             | 0x5009_3000      | 0x5009_3FFF  | 4         |
| HMAC Accelerator (HMAC)            | 0x5009_4000      | 0x5009_4FFF  | 4         |
| ECC Accelerator (ECC)              | 0x5009_5000      | 0x5009_5FFF  | 4         |
| ECDSA                              | 0x5009_6000      | 0x5009_6FFF  | 4         |
| Reserved                           | 0x5009_7000      | 0x5009_7FFF  |           |
| GMAC                               | 0x5009_8000      | 0x5009_BFFF  | 16        |

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Table 6.3-2 – cont'd from previous page

| Target                                       | Boundary Address |              | Size (KB) |
|--|------------------|--------------|-----------|
|  | Low Address      | High Address |           |
| USB 2.0 OTG High-Speed PHY                   | 0x5009_C000      | 0x5009_CFFF  | 4         |
| Reserved                                     | 0x5009_D000      | 0x5009_DFFF  |           |
| CSI Host                                     | 0x5009_F000      | 0x500F_FFFF  | 4         |
| DSI Host                                     | 0x500A_0000      | 0x500A_0FFF  | 4         |
| Image Signal Processor (ISP)                 | 0x500A_1000      | 0x500A_1FFF  | 4         |
| Remote Control Peripheral (RMT)              | 0x500A_2000      | 0x500A_2FFF  | 4         |
| Bit-scrambler                                | 0x500A_3000      | 0x500A_3FFF  | 4         |
| AXI ICM                                      | 0x500A_4000      | 0x500A_4FFF  | 4         |
| HP Peripheral Permission (HP_PERI_PMS)       | 0x500A_5000      | 0x5009_57FF  | 2         |
| LP2HP Peripheral Permission (LP2HP_PERI_PMS) | 0x500A_5800      | 0x500A_5FFF  | 2         |
| HP DMA Permission (HP_DMA_PMS)               | 0x500A_6000      | 0x500A_6FFF  | 4         |
| H264 DMA                                     | 0x500A_7000      | 0x500A_7FFF  | 4         |
| Reserved                                     | 0x500A_8000      | 0x500B_FFFF  |           |
| <b>HP Peripherals 1 (HP PERI1)</b>           |                  |              |           |
| Motor Control PWM0 (MCPWM0)                  | 0x500C_0000      | 0x500C_0FFF  | 4         |
| Motor Control PWM1 (MCPWM1)                  | 0x500C_1000      | 0x500C_1FFF  | 4         |
| Timer Group 0 (TIMG0)                        | 0x500C_2000      | 0x500C_2FFF  | 4         |
| Timer Group 1 (TIMG1)                        | 0x500C_3000      | 0x500C_3FFF  | 4         |
| I2C Controller0 (I2C0)                       | 0x500C_4000      | 0x500C_4FFF  | 4         |
| I2C Controller1 (I2C1)                       | 0x500C_5000      | 0x500C_5FFF  | 4         |
| I2S Controller0 (I2S0)                       | 0x500C_6000      | 0x500C_6FFF  | 4         |
| I2S Controller1 (I2S1)                       | 0x500C_7000      | 0x500C_7FFF  | 4         |
| I2S Controller0 (I2S2)                       | 0x500C_8000      | 0x500C_8FFF  | 4         |
| Pulse Count Controller (PCNT)                | 0x500C_9000      | 0x500C_9FFF  | 4         |
| UART Controller 0 (UART0)                    | 0x500C_A000      | 0x500C_AFFF  | 4         |
| UART Controller 1 (UART1)                    | 0x500C_B000      | 0x500C_BFFF  | 4         |
| UART Controller 2 (UART2)                    | 0x500C_C000      | 0x500C_CFFF  | 4         |
| UART Controller 3 (UART3)                    | 0x500C_D000      | 0x500C_DFFF  | 4         |
| UART Controller 4 (UART4)                    | 0x500C_E000      | 0x500C_EFFF  | 4         |
| Parallel IO Controller (PARL_IO)             | 0x500C_F000      | 0x500C_FFFF  | 4         |
| General Purpose SPI2 (GP-SPI2)               | 0x500D_0000      | 0x500D_0FFF  | 4         |
| General Purpose SPI3 (GP-SPI3)               | 0x500D_1000      | 0x500D_1FFF  | 4         |
| USB Serial/JTAG Controller                   | 0x500D_2000      | 0x500D_2FFF  | 4         |
| LED PWM Controller (LEDC)                    | 0x500D_3000      | 0x500D_3FFF  | 4         |
| Reserved                                     | 0x500D_4000      | 0x500D_4FFF  |           |
| Event Task Matrix (SOC_ETM)                  | 0x500D_5000      | 0x500D_5FFF  | 4         |
| Interrupt Matrix (INTMTX)                    | 0x500D_6000      | 0x500D_6FFF  | 4         |
| Two-wire Automotive Interface 0 (TWAIO)      | 0x500D_7000      | 0x500D_7FFF  | 4         |
| Two-wire Automotive Interface 1 (TWA1)       | 0x500D_8000      | 0x500D_8FFF  | 4         |
| Two-wire Automotive Interface 2 (TWA2)       | 0x500D_9000      | 0x500D_9FFF  | 4         |

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Table 6.3-2 – cont'd from previous page

| Target   | Boundary Address |              | Size (KB) |
|--|------------------|--------------|-----------|
|  | Low Address      | High Address |           |
| I3C Master Controller                          | 0x500D_A000      | 0x500D_AFFF  | 4         |
| I3C Slave Controller                           | 0x500D_B000      | 0x500D_BFFF  | 4         |
| LCD and Camera Controller (LCD_CAM)            | 0x500D_C000      | 0x500D_CFFF  | 4         |
| Reserved                                       | 0x500D_D000      | 0x500D_DFFF  |           |
| ADC Controller                                 | 0x500D_E000      | 0x500D_EFFF  | 4         |
| UHCI Controller (UHCI)                         | 0x500D_F000      | 0x500D_FFFF  | 4         |
| GPIO Matrix                                    | 0x500E_0000      | 0x500E_0FFF  | 4         |
| IO MUX   | 0x500E_1000      | 0x500E_1FFF  | 4         |
| System Timer (SYSTIMER)                        | 0x500E_2000      | 0x500E_2FFF  | 4         |
| Reserved                                       | 0x500E_3000      | 0x500E_4FFF  |           |
| HP System Register (SYSREG)                    | 0x500E_5000      | 0x500D_5FFF  | 4         |
| Reset and Clock                                | 0x500E_6000      | 0x500E_6FFF  | 4         |
| Reserved                                       | 0x500E_7000      | 0x500F_FFFF  |           |
| <b>MIPI Camera and LCD Memory</b>              |                  |              |           |
| MIPI Camera Memory                             | 0x5010_4000      | 0x5010_4FFF  | 4         |
| MIPI LCD Memory                                | 0x5010_5000      | 0x5010_5FFF  | 4         |
| <b>LP Always On Peripherals (LP AON PERI)</b>  |                  |              |           |
| LP System Register                             | 0x5011_0000      | 0x5011_0FFF  | 4         |
| LP Always-on Clock and Reset                   | 0x5011_1000      | 0x5011_1FFF  | 4         |
| LP Timer                                       | 0x5011_2000      | 0x5011_2FFF  | 4         |
| LP Analog peripherals (LP ANAPERI)             | 0x5011_3000      | 0x5011_3FFF  | 4         |
| Power Management Unit (PMU)                    | 0x5011_5000      | 0x5011_5FFF  | 4         |
| LP Watch Dog Timer (LP WDT)                    | 0x5011_6000      | 0x5011_6FFF  | 4         |
| Reserved                                       | 0x5011_7000      | 0x5011_7FFF  |           |
| LP Mailbox (LP MB)                             | 0x5011_8000      | 0x5011_8FFF  | 4         |
| Reserved                                       | 0x5011_A000      | 0x5011_FFFF  |           |
| <b>LP Peripherals (LP PERI)</b>                |                  |              |           |
| LP Peripheral Clock and Reset (LP PERI-CLKRST) | 0x5012_0000      | 0x5012_0FFF  | 4         |
| LP UART  | 0x5012_1000      | 0x5012_1FFF  | 4         |
| LP I2C   | 0x5012_2000      | 0x5012_2FFF  | 4         |
| LP SPI   | 0x5012_3000      | 0x5012_3FFF  | 4         |
| LP Analog I2C                                  | 0x5012_4000      | 0x5012_4FFF  | 4         |
| LP I2S   | 0x5012_5000      | 0x5012_5FFF  | 4         |
| Reserved                                       | 0x5012_6000      | 0x5012_6FFF  | 4         |
| LP ADC   | 0x5012_7000      | 0x5012_7FFF  | 4         |
| Reserved                                       | 0x5012_8000      | 0x5012_9FFF  |           |
| LP GPIO Matrix                                 | 0x5012_A000      | 0x5012_AFFF  | 4         |
| LP IO MUX                                      | 0x5012_B000      | 0x5012_BFFF  | 4         |
| LP Interrupt (LP INTR)                         | 0x5012_C000      | 0x5012_CFFF  | 4         |
| LP eFuse                                       | 0x5012_D000      | 0x5012_DFFF  | 4         |

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Table 6.3-2 – cont'd from previous page

| Target   | Boundary Address |              | Size (KB) |
|--|------------------|--------------|-----------|
|  | Low Address      | High Address |           |
| <a href="#">LP Peripheral Permission (LP_PERI_PMS)</a>       | 0x5012_E000      | 0x5012_E7FF  | 2         |
| <a href="#">HP2LP Peripheral Permission (HP2LP_PERI_PMS)</a> | 0x5012_E800      | 0x5012_EFFF  | 2         |
| <a href="#">LP Temperature Sensor</a>                        | 0x5012_F000      | 0x5012_FFFF  | 4         |

**Note:**

As shown in Figure 6.3-1, HP CPU and LP CPU can access HP CPU PERI, HP PERIO, HP PERI1, LP AON PERI and LP PERI listed in Table 6.3-2.

## Chapter 7

### eFuse Controller

#### 7.1 Overview

ESP32-P4 contains a 4096-bit eFuse memory to store parameters and user data. The parameters include control parameters for some hardware modules, system data parameters and keys used for the encryption/decryption module. Once an eFuse bit is programmed to 1, it can never be reverted to 0. The eFuse controller programs individual bits of parameters in eFuse according to user configurations. From outside the chip, eFuse data can only be read via the eFuse controller. For some data, such as some keys stored in eFuse for internal use by hardware cryptography modules (e.g., digital signature, HMAC), if read protection is not enabled, the data can be read from outside the chip; if read protection is enabled, the data cannot be read from outside the chip.

#### 7.2 Features

- 4096-bit one-time programmable memory (including up to 1792 bits reserved for custom use depending on whether the EFUSE\_KEY\_PURPOSE\_*n* parameters are set to 0. For more information, see Table 7.3-2.)
- Configurable write protection
- Configurable read protection
- Various hardware encoding schemes against data corruption

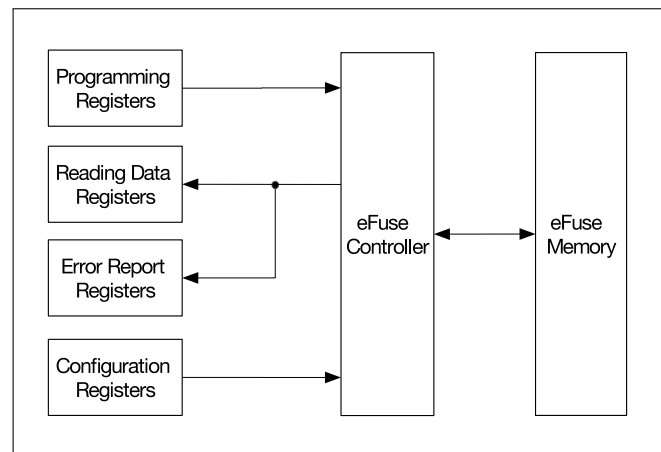
#### 7.3 Functional Description

##### 7.3.1 Structure

The eFuse system consists of the eFuse controller and eFuse memory. Data flow in this system is shown in Figure 7.3-1.

Users can program bits in the eFuse memory via the eFuse controller by writing the data to be programmed to the programming register and executing the programming instruction. For detailed programming steps, please refer to Section 7.3.2.

Users cannot directly read the data programmed in the eFuse memory, so they need to read the programmed data into the Reading Data Register of the corresponding address segment through the eFuse controller. During the reading process, if the data is inconsistent with that in the eFuse memory, the eFuse controller can automatically correct it through the hardware encoding mechanism (see Section 7.3.1.3 for details), and send the error message to the error report register. For detailed steps to read parameters, please refer to the Section 7.3.3.



**Figure 7.3-1. Data Flow in eFuse**

Data in eFuse memory is organized in 11 blocks (BLOCK0 ~ BLOCK10).

BLOCK0 holds most parameters for software and hardware uses.

Table [7.3-1](#) lists all the parameters accessible (readable and usable) to users in BLOCK0 and their offsets, bit widths, accessibility by hardware, write protection, and brief function description. For more description on the parameters, please click the link of the corresponding parameter in the table.

The [EFUSE\\_WR\\_DIS](#) parameter is used to disable write protection of other parameters. [EFUSE\\_RD\\_DIS](#) is used to disable read protection of BLOCK4 ~ BLOCK10. For more information on these two parameters, please see Section [7.3.1.1](#) and Section [7.3.1.2](#).

Table 7.3-1. Parameters in eFuse BLOCK0

| Parameters  | Bit Width | Accessible by Hardware | Write Protection by <a href="#">EFUSE_WR_DIS</a> Bit Number | Description  |
|---|-----------|------------------------|---|--|
| <a href="#">EFUSE_WR_DIS</a>                      | 32        | Y                      | N/A   | Represents whether writing of eFuse bits by eFuse controller is disabled.  |
| <a href="#">EFUSE_RD_DIS</a>                      | 7         | Y                      | 0   | Represents whether reading data from BLOCK4 ~ 10 in eFuse memory by users is disabled.   |
| <a href="#">EFUSE_USB_DEVICE_EXCHG_PINS</a>       | 1         | Y                      | 30  | Represents whether the USB Serial/JTAG pins D+ and D- are exchanged.   |
| <a href="#">EFUSE_USB_OTG11_EXCHG_PINS</a>        | 1         | Y                      | 30  | Represents whether the USB FS pins D+ and D- are exchanged.  |
| <a href="#">EFUSE_DIS_USB_JTAG</a>                | 1         | Y                      | 2   | Represents whether the USB-to-JTAG function in USB Serial/JTAG module is disabled.   |
| <a href="#">EFUSE_POWERGLITCH_EN</a>              | 1         | Y                      | 2   | Represents whether power glitch detection is enabled.  |
| <a href="#">EFUSE_DIS_FORCE_DOWNLOAD</a>          | 1         | Y                      | 2   | Represents whether the function to force the chip into Download mode is disabled.  |
| <a href="#">EFUSE_SPI_DOWNLOAD_MSPI_DIS</a>       | 1         | Y                      | 2   | Represents accessing MSPI flash/MSPI RAM by SYS AXI matrix is disabled during boot_mode_download.  |
| <a href="#">EFUSE_DIS_TWAI</a>                    | 1         | Y                      | 2   | Represents whether the TWAI controller is disabled.  |
| <a href="#">EFUSE_JTAG_SEL_ENABLE</a>             | 1         | Y                      | 2   | Represents whether the selection of a JTAG signal source through the strapping value is enabled when both <a href="#">EFUSE_DIS_PAD_JTAG</a> and <a href="#">EFUSE_DIS_USB_JTAG</a> are configured to 0. |
| <a href="#">EFUSE_SOFT_DIS_JTAG</a>               | 3         | Y                      | 31  | Represents whether PAD JTAG is disabled in the soft way.   |
| <a href="#">EFUSE_DIS_PAD_JTAG</a>                | 1         | Y                      | 2   | Represents whether PAD JTAG is disabled in the hard way (permanently).   |
| <a href="#">EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT</a> | 1         | Y                      | 2   | Represents whether flash encryption is disabled (except in SPI boot mode).   |

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Table 7.3-1 – cont'd from previous page

| Parameters  | Bit Width | Accessible by Hardware | Write Protection by <a href="#">EFUSE_WR_DIS</a> Bit Number | Description  |
|---|-----------|------------------------|---|--|
| <a href="#">EFUSE_USB_PHY_SEL</a>                   | 1         | Y                      | 30  | Represents the connection between USB Serial/JTAG Controller, OTG_FS and FS_PHY1, FS_PHY2. |
| <a href="#">EFUSE_XTS_KEY_LENGTH_256</a>            | 1         | N                      | 1   | Represents which key is used for flash encryption.   |
| <a href="#">EFUSE_WDT_DELAY_SEL</a>                 | 2         | Y                      | 2   | Represents RTC watchdog timeout threshold.   |
| <a href="#">EFUSE_SPI_BOOT_CRYPT_CNT</a>            | 3         | Y                      | 4   | Represents whether SPI boot encryption/decryption is enabled.                              |
| <a href="#">EFUSE_SECURE_BOOT_KEY_REVOKE0</a>       | 1         | N                      | 5   | Represents whether revoking the first Secure Boot key is enabled.                          |
| <a href="#">EFUSE_SECURE_BOOT_KEY_REVOKE1</a>       | 1         | N                      | 6   | Represents whether revoking the second Secure Boot key is enabled.                         |
| <a href="#">EFUSE_SECURE_BOOT_KEY_REVOKE2</a>       | 1         | N                      | 7   | Represents whether revoking the third Secure Boot key is enabled.                          |
| <a href="#">EFUSE_KEY_PURPOSE_0</a>                 | 4         | Y                      | 8   | Represents Key0 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_KEY_PURPOSE_1</a>                 | 4         | Y                      | 9   | Represents Key1 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_KEY_PURPOSE_2</a>                 | 4         | Y                      | 10  | Represents Key2 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_KEY_PURPOSE_3</a>                 | 4         | Y                      | 11  | Represents Key3 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_KEY_PURPOSE_4</a>                 | 4         | Y                      | 12  | Represents Key4 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_KEY_PURPOSE_5</a>                 | 4         | Y                      | 13  | Represents Key5 purpose. See Table <a href="#">7.3-2</a> .                                 |
| <a href="#">EFUSE_SEC_DPA_LEVEL</a>                 | 2         | Y                      | 14  | Represents the security level of anti-DPA (differential power analysis) attack.            |
| <a href="#">EFUSE_CRYPT_DPA_ENABLE</a>              | 1         | Y                      | 14  | Represents whether defense against DPA attack is enabled.                                  |
| <a href="#">EFUSE_SECURE_BOOT_EN</a>                | 1         | N                      | 15  | Represents whether Secure Boot is enabled.   |
| <a href="#">EFUSE_SECURE_BOOT_AGGRESSIVE_REVOKE</a> | 1         | N                      | 16  | Represents whether aggressive revocation of Secure Boot is enabled.                        |
| <a href="#">EFUSE_FLASH_TYPE</a>                    | 1         | N                      | 18  | Represents the type of the interfaced flash.   |

Cont'd on next page

Table 7.3-1 – cont'd from previous page

| Parameters  | Bit Width | Accessible by Hardware | Write Protection by EFUSE_WR_DIS Bit Number | Description  |
|---|-----------|------------------------|---|--|
| <a href="#">EFUSE_FLASH_PAGE_SIZE</a>                   | 2         | N                      | 18  | Represents flash page size.  |
| <a href="#">EFUSE_FLASH_ECC_EN</a>                      | 1         | N                      | 18  | Represents whether ECC is enabled during flash boot.                                       |
| <a href="#">EFUSE_DIS_USB_OTG_DOWNLOAD_MODE</a>         | 1         | N                      | 18  | Represents whether download via USB-OTG is disabled.                                       |
| <a href="#">EFUSE_FLASH_TPUW</a>                        | 4         | N                      | 18  | Represents the flash waiting time after power-up.  |
| <a href="#">EFUSE_DIS_DOWNLOAD_MODE</a>                 | 1         | N                      | 18  | Represents whether all Download modes are disabled.  |
| <a href="#">EFUSE_DIS_DIRECT_BOOT</a>                   | 1         | N                      | 18  | Represents whether direct boot mode is disabled.   |
| <a href="#">EFUSE_DIS_USB_SERIAL_JTAG_ROM_PRINT</a>     | 1         | N                      | 18  | Represents whether print from USB-Serial-JTAG during ROM boot is disabled.                 |
| <a href="#">EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE</a> | 1         | N                      | 18  | Represents whether the USB-Serial-JTAG download function is disabled.                      |
| <a href="#">EFUSE_ENABLE_SECURITY_DOWNLOAD</a>          | 1         | N                      | 18  | Represents whether security download is enabled.   |
| <a href="#">EFUSE_UART_PRINT_CONTROL</a>                | 2         | N                      | 18  | Represents the type of UART printing.  |
| <a href="#">EFUSE_FORCE_SEND_RESUME</a>                 | 1         | N                      | 18  | Represents whether ROM code is forced to send a resume command during SPI boot.            |
| <a href="#">EFUSE_SECURE_VERSION</a>                    | 16        | N                      | 18  | Represents the version used by ESP-IDF anti-rollback feature.                              |
| <a href="#">EFUSE_SECURE_BOOT_DISABLE_FAST_WAKE</a>     | 1         | N                      | 19  | Represents whether FAST VERIFY ON WAKE is disabled or enabled when Secure Boot is enabled. |
| <a href="#">EFUSE_HYS_EN_PAD</a>                        | 1         | Y                      | 2   | Represents whether the hysteresis function of PAD0 – PAD27 is enabled.                     |
| <a href="#">EFUSE_DCDC_VSET</a>                         | 5         | Y                      | N/A   | Represents the default DCDC voltage.   |
| <a href="#">EFUSE_OPXA_TIEH_SELO</a>                    | 2         | Y                      | 2   | Represents which output source is used for Extern Power (V01).                             |
| <a href="#">EFUSE_OPXA_TIEH_SEL1</a>                    | 2         | Y                      | 2   | Represents which output source is used for Extern Power (V02).                             |

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Table 7.3-1 – cont'd from previous page

| Parameters                           | Bit Width | Accessible by Hardware | Write Protection by <a href="#">EFUSE_WR_DIS</a> Bit Number | Description   |
|--------------------------------------|-----------|------------------------|---|---|
| <a href="#">EFUSE_OPXA_TIEH_SEL2</a> | 2         | Y                      | 2   | Represents which output source is used for Extern Power (VO3).                                |
| <a href="#">EFUSE_OPXA_TIEH_SEL3</a> | 2         | Y                      | 2   | Represents which output source is used for Extern Power (VO4).                                |
| <a href="#">EFUSE_HP_PWR_SRC_SEL</a> | 1         | Y                      | 3   | Represents the HP system power source.  |
| <a href="#">EFUSE_DCDC_VSET_EN</a>   | 1         | Y                      | N/A   | Represents whether to use the default voltage configured by <a href="#">EFUSE_DCDC_VSET</a> . |
| <a href="#">EFUSE_DIS_WDT</a>        | 1         | Y                      | 2   | Represents whether to disable the watchdog.   |
| <a href="#">EFUSE_DIS_SWD</a>        | 1         | Y                      | 2   | Represents whether to disable the super watchdog.   |



Table 7.3-2 lists all key purposes and their values. Setting the eFuse parameter EFUSE\_KEY\_PURPOSE\_*n* declares the purpose of KEY*n* (*n*: 0 ~ 5).

Table 7.3-2. Secure Key Purpose Values

| Key Purpose Values | Purposes   |
|--------------------|--|
| 0                  | User purposes  |
| 1                  | ECDSA_KEY  |
| 2                  | XTS_AES_256_KEY_1                                      |
| 3                  | XTS_AES_256_KEY_2                                      |
| 4                  | XTS_AES_128_KEY (flash/SRAM encryption and decryption) |
| 5                  | HMAC Downstream mode (both JTAG and DS)                |
| 6                  | JTAG in HMAC Downstream mode                           |
| 7                  | Digital Signature peripheral in HMAC Downstream mode   |
| 8                  | HMAC Upstream mode                                     |
| 9                  | SECURE_BOOT_DIGEST0 (secure boot key digest)           |
| 10                 | SECURE_BOOT_DIGEST1 (secure boot key digest)           |
| 11                 | SECURE_BOOT_DIGEST2 (secure boot key digest)           |

Table 7.3-3 provides the details of parameters in BLOCK1 ~ BLOCK10.

Table 7.3-3. Parameters in BLOCK1 to BLOCK10

| BLOCK   | Parameters           | Bit Width | Accessible<br>by Hardware | Write Protection by<br><a href="#">EFUSE_WR_DIS</a><br>Bit Number | Read Protection<br>by <a href="#">EFUSE_RD_DIS</a><br>Bit Number | Description          |
|---------|----------------------|-----------|---------------------------|---|--|----------------------|
| BLOCK1  | EFUSE_MAC            | 48        | N                         | 20  | N/A  | MAC address          |
|         | EFUSE_MAC_EXT        | 16        | N                         | 20  | N/A  | Extended MAC address |
|         | EFUSE_MAC_RESERVED   | 50        | N                         | 20  | N/A  | Reserved MAC address |
|         | EFUSE_SYS_DATA_PART0 | 78        | N                         | 20  | N/A  | System data          |
| BLOCK2  | EFUSE_SYS_DATA_PART1 | 256       | N                         | 21  | N/A  | System data          |
| BLOCK3  | EFUSE_USR_DATA       | 256       | N                         | 22  | N/A  | User data            |
| BLOCK4  | EFUSE_KEY0_DATA      | 256       | Y                         | 23  | 0  | KEY0 or user data    |
| BLOCK5  | EFUSE_KEY1_DATA      | 256       | Y                         | 24  | 1  | KEY1 or user data    |
| BLOCK6  | EFUSE_KEY2_DATA      | 256       | Y                         | 25  | 2  | KEY2 or user data    |
| BLOCK7  | EFUSE_KEY3_DATA      | 256       | Y                         | 26  | 3  | KEY3 or user data    |
| BLOCK8  | EFUSE_KEY4_DATA      | 256       | Y                         | 27  | 4  | KEY4 or user data    |
| BLOCK9  | EFUSE_KEY5_DATA      | 256       | Y                         | 28  | 5  | KEY5 or user data    |
| BLOCK10 | EFUSE_SYS_DATA_PART2 | 256       | N                         | 29  | 6  | System data          |

Among these blocks, BLOCK4 ~ 9 can be used to store KEY0 ~ 5. Up to six 256-bit keys can be written into eFuse. Whenever a key is written, its purpose value should also be written (see table 7.3-2). For example, when a key for the JTAG function in HMAC Downstream mode is written to KEY3 (i.e., BLOCK7), its key purpose value 6 should also be written to EFUSE\_KEY\_PURPOSE\_3.

**Note:**

Do not program the XTS-AES key into the KEY5 block, i.e., BLOCK9. Otherwise, the key may be unreadable. Instead, program it into the preceding blocks, i.e., BLOCK4 ~ BLOCK8. The last block, BLOCK9, is used to program other keys.

BLOCK1 ~ BLOCK10 use the RS coding scheme, so there are some limitations on writing to these parameters. For more detailed information, please refer to Section 7.3.1.3 and Section 7.3.2.

### 7.3.1.1 EFUSE\_WR\_DIS

Parameter EFUSE\_WR\_DIS determines whether individual eFuse parameters are write-protected. After EFUSE\_WR\_DIS has been programmed, execute an eFuse read operation so the new values would take effect.

Column “Write Protection by EFUSE\_WR\_DIS Bit Number” in Table 7.3-1 and Table 7.3-3 list the specific bits in EFUSE\_WR\_DIS that disable writing.

When the write protection bit of a parameter is set to 0, it means that this parameter is not write-protected and can be programmed, unless it has been programmed before.

When the write protection bit of a parameter is set to 1, it means that this parameter is write-protected and none of its bits can be modified, with non-programmed bits always remaining 0 and programmed bits always remaining 1. That is to say, if a parameter is write-protected, it will always remain in this state and cannot be changed.

### 7.3.1.2 EFUSE\_RD\_DIS

Only the parameters in BLOCK4 ~ BLOCK10 can be set to be read-protected from users, as shown in column “Read Protection by EFUSE\_RD\_DIS Bit Number” of Table 7.3-3. After EFUSE\_RD\_DIS has been programmed, execute an eFuse read operation so the new values would take effect.

If the corresponding EFUSE\_RD\_DIS bit is 0, the parameter controlled by this bit is not read-protected from users. If it is 1, the parameter controlled by it is read-protected from users.

Other parameters that are not in BLOCK4 ~ BLOCK10 can always be read by users.

When BLOCK4 ~ BLOCK10 are set to be read-protected, the data in them can still be read by hardware cryptography modules if the EFUSE\_KEY\_PURPOSE\_*n* bit is set accordingly.

### 7.3.1.3 Data Storage

Internally, eFuse uses the hardware encoding scheme to protect data from corruption. The scheme and the encoding process are invisible to users.

All BLOCK0 parameters except for EFUSE\_WR\_DIS are stored with four backups, meaning each bit is stored four times. This backup scheme is not visible to users.

In BLOCK0, `EFUSE_WR_DIS` occupies 32 bits, and other parameters takes 152 bits each. So, the eFuse memory space occupied by BLOCK0 is  $32 + 152 * 4 = 640$  bits.

BLOCK1 ~ BLOCK10 use RS (44, 32) coding scheme that supports up to 6 bytes of automatic error correction. The primitive polynomial of RS (44, 32) is  $p(x) = x^8 + x^4 + x^3 + x^2 + 1$ .

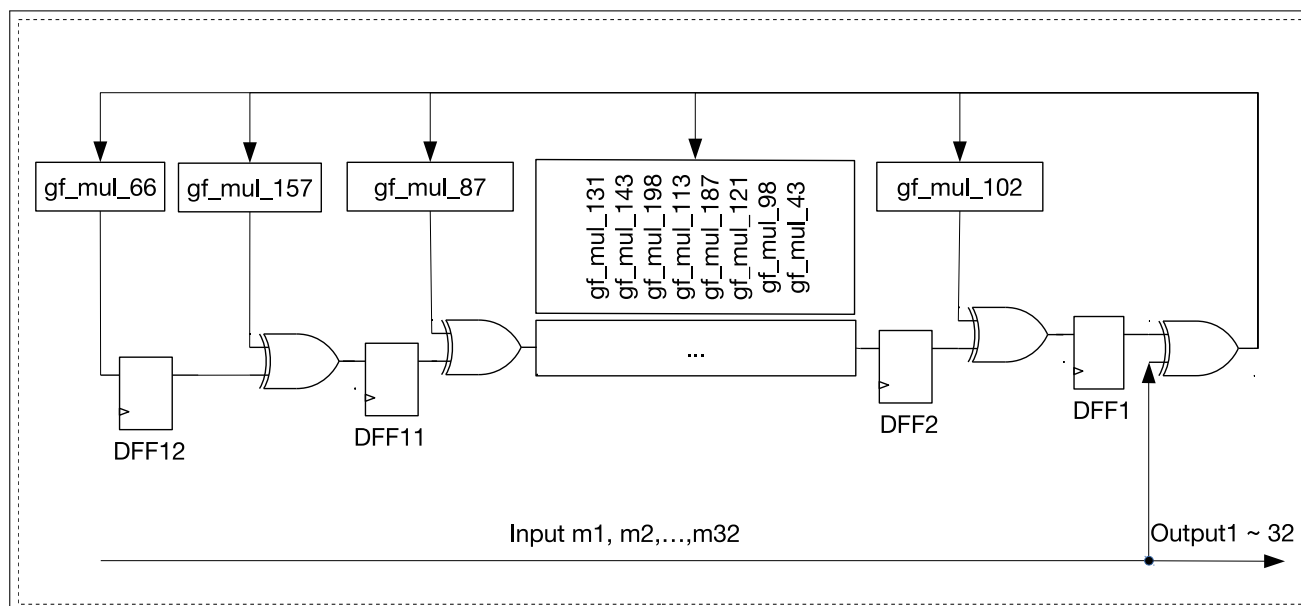


Figure 7.3-2. Shift Register Circuit (first 32 output)

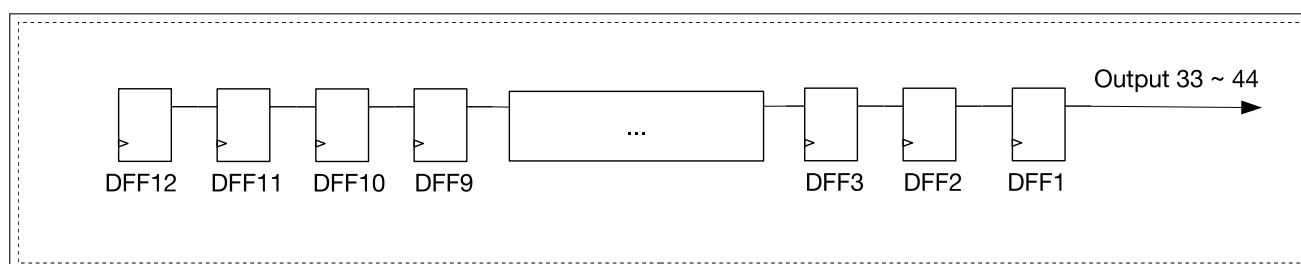


Figure 7.3-3. Shift Register Circuit (last 12 output)

The shift register circuit shown in Figure 7.3-2 and 7.3-3 processes 32 data bytes using RS (44, 32). This coding scheme encodes 32 bytes of data into 44 bytes:

- Bytes [0:31] are the data bytes itself
- Bytes [32:43] are the encoded parity bytes stored in 8-bit flip-flops DFF1, DFF2, ..., DFF12 ( $gf\_mul\_n$  is the result of multiplying a byte of data in  $GF(2^8)$  by  $\alpha^n$ , where  $n$  is an integer).

After that, the hardware programs into eFuse the 44-byte codeword consisting of the data bytes and the parity bytes. When the eFuse block is read, the eFuse controller automatically decodes the codeword and applies error correction if needed.

Because the RS check codes are generated on the entire 32-byte eFuse block, each block can only be written once.

Since the size of BLOCK1 is less than 32 bytes, the unused bits will be treated as 0 by hardware during the RS (44, 32) encoding. Thus, the final coding result will not be affected.

Among blocks using the RS (44, 32) coding scheme, the parameters in BLOCK1 is 24 bytes, and the RS check code is 12 bytes, so BLOCK1 occupies  $24 + 12 = 36$  bytes in eFuse memory.

The parameter in other blocks (Block2 ~ 10) is 32 bytes respectively, and the RS check code is 12 bytes, so they occupy  $(32 + 12) * 9 = 396$  bytes in eFuse memory.

### 7.3.2 Programming of Parameters

The eFuse controller can only program eFuse parameters in one block at a time. BLOCK0 ~ BLOCK10 share the same address range to store the parameters to be programmed. Configure parameter [EFUSE\\_BLK\\_NUM](#) to indicate which block should be programmed.

Since there is a one-to-one correspondence between the reading data registers and the programming data registers (see table [7.3-4](#) for details), users can find out where the data to be programmed is located in programming registers by checking the parameter description and the parameter location in the corresponding read registers.

For example, if the user wants to program the parameter [EFUSE\\_USB\\_DEVICE\\_EXCHG\\_PINS](#) in BLOCK0 to 1, they can first search the reading data registers [EFUSE\\_RD\\_REPEAT\\_DATA0 ~ 4\\_REG](#) in BLOCK0 for where the parameter is located, namely, the 8th bit in [EFUSE\\_RD\\_REPEAT\\_DATA0\\_REG](#). So, the user can set the 8th bit of [EFUSE\\_PGM\\_DATA1\\_REG](#) to 1 and follow the programming steps below. After the steps are completed, the corresponding bit in the eFuse memory will be programmed to 1.

#### Programming preparation

- Programming BLOCK0
  1. Set [EFUSE\\_BLK\\_NUM](#) to 0.
  2. Write into [EFUSE\\_PGM\\_DATA0\\_REG ~ EFUSE\\_PGM\\_DATA5\\_REG](#) the data to be programmed to BLOCK0.  
The data in [EFUSE\\_PGM\\_DATA6\\_REG ~ EFUSE\\_PGM\\_DATA7\\_REG](#) and [EFUSE\\_PGM\\_CHECK\\_VALUE0\\_REG ~ EFUSE\\_PGM\\_CHECK\\_VALUE2\\_REG](#) does not affect the programming of BLOCK0.
- BLOCK1 cannot be programmed by users as it has been programmed at manufacturing.
- Programming BLOCK2 ~ 10
  1. Set [EFUSE\\_BLK\\_NUM](#) to the block number.
  2. Write into [EFUSE\\_PGM\\_DATA0\\_REG ~ EFUSE\\_PGM\\_DATA7\\_REG](#) the data to be programmed. Write into [EFUSE\\_PGM\\_CHECK\\_VALUE0\\_REG ~ EFUSE\\_PGM\\_CHECK\\_VALUE2\\_REG](#) the corresponding RS code.

#### Programming process

The process of programming parameters is as follows:

1. Configure the value of parameter [EFUSE\\_BLK\\_NUM](#) to determine the block to be programmed.
2. Write parameters to be programmed to registers [EFUSE\\_PGM\\_DATA0\\_REG ~ EFUSE\\_PGM\\_DATA7\\_REG](#) and [EFUSE\\_PGM\\_CHECK\\_VALUE0\\_REG ~ EFUSE\\_PGM\\_CHECK\\_VALUE2\\_REG](#).
3. Make sure the eFuse programming voltage VDDQ is configured correctly as described in Section [7.3.4](#).
4. Configure the field [EFUSE\\_OP\\_CODE](#) of register [EFUSE\\_CONF\\_REG](#) to 0x5A5A.

5. Configure the field [EFUSE\\_PGM\\_CMD](#) of register [EFUSE\\_CMD\\_REG](#) to 1.
6. Poll register [EFUSE\\_CMD\\_REG](#) until it is 0x0, or wait for a PGM\_DONE interrupt. For more information on how to identify a PGM\_DONE or READ\_DONE interrupt, please see the end of Section 7.3.3.
7. Clear the parameters in [EFUSE\\_PGM\\_DATA0\\_REG](#) ~ [EFUSE\\_PGM\\_DATA7\\_REG](#) and [EFUSE\\_PGM\\_CHECK\\_VALUE0\\_REG](#) ~ [EFUSE\\_PGM\\_CHECK\\_VALUE2\\_REG](#).
8. Trigger an eFuse read operation (see Section 7.3.3) to update eFuse registers with the new values.
9. Check error record registers. If the values read in error record registers are not 0, the programming process should be performed again following above steps 1 ~ 7. Please check the following error record registers for different eFuse blocks:
  - BLOCK0: [EFUSE\\_RD\\_REPEAT\\_ERR0\\_REG](#) ~ [EFUSE\\_RD\\_REPEAT\\_ERR4\\_REG](#)
  - BLOCK1: [EFUSE\\_MAC\\_SYS\\_ERR\\_NUM](#), [EFUSE\\_MAC\\_SYS\\_FAIL](#)
  - BLOCK2: [EFUSE\\_SYS\\_PART1\\_ERR\\_NUM](#), [EFUSE\\_SYS\\_PART1\\_FAIL](#)
  - BLOCK3: [EFUSE\\_USR\\_DATA\\_ERR\\_NUM](#), [EFUSE\\_USR\\_DATA\\_FAIL](#)
  - BLOCK4: [EFUSE\\_KEY0\\_ERR\\_NUM](#), [EFUSE\\_KEY0\\_FAIL](#)
  - BLOCK5: [EFUSE\\_KEY1\\_ERR\\_NUM](#), [EFUSE\\_KEY1\\_FAIL](#)
  - BLOCK6: [EFUSE\\_KEY2\\_ERR\\_NUM](#), [EFUSE\\_KEY2\\_FAIL](#)
  - BLOCK7: [EFUSE\\_KEY3\\_ERR\\_NUM](#), [EFUSE\\_KEY3\\_FAIL](#)
  - BLOCK8: [EFUSE\\_KEY4\\_ERR\\_NUM](#), [EFUSE\\_KEY4\\_FAIL](#)
  - BLOCK9: [EFUSE\\_KEY5\\_ERR\\_NUM](#), [EFUSE\\_KEY5\\_FAIL](#)
  - BLOCK10: [EFUSE\\_SYS\\_PART2\\_ERR\\_NUM](#), [EFUSE\\_SYS\\_PART2\\_FAIL](#)

### Limitations

In BLOCK0, each bit can be programmed separately. However, we recommend to minimize programming cycles and program all the bits of a parameter in one programming action. In addition, after all parameters controlled by a certain bit of [EFUSE\\_WR\\_DIS](#) are programmed, that bit should be immediately programmed. The programming of parameters controlled by a certain bit of [EFUSE\\_WR\\_DIS](#), and the programming of the bit itself can even be completed at the same time in one programming action.

BLOCK1 cannot be programmed by users as it has been programmed at manufacturing.

BLOCK2 ~ 10 can only be programmed once. Repeated programming is not allowed.

## 7.3.3 Reading of Parameters by Users

Users cannot read eFuse bits directly. The eFuse controller hardware reads all eFuse bits and stores the results to their corresponding registers in its memory space. Then, users can read eFuse bits by reading the registers that start with [EFUSE\\_RD\\_](#). Details are provided in Table 7.3-4.

Table 7.3-4. Registers Information

| BLOCK | Read Registers   | Registers When Programming This Block   |
|-------|--|---|
| 0     | <a href="#">EFUSE_RD_WR_DIS_REG</a>  | <a href="#">EFUSE_PGM_DATA0_REG</a>     |
| 0     | <a href="#">EFUSE_RD_REPEAT_DATA0 ~ 4_REG</a>                              | <a href="#">EFUSE_PGM_DATA1 ~ 5_REG</a> |
| 1     | <a href="#">EFUSE_RD_MAC_SYS_0 ~ 5_REG</a>                                 | <a href="#">EFUSE_PGM_DATA0 ~ 5_REG</a> |
| 2     | <a href="#">EFUSE_RD_SYS_PART1_DATA0 ~ 7_REG</a>                           | <a href="#">EFUSE_PGM_DATA0 ~ 7_REG</a> |
| 3     | <a href="#">EFUSE_RD_USR_DATA0 ~ 7_REG</a>                                 | <a href="#">EFUSE_PGM_DATA0 ~ 7_REG</a> |
| 4-9   | <a href="#">EFUSE_RD_KEY<sub>n</sub>_DATA0 ~ 7_REG</a> ( <i>n</i> : 0 ~ 5) | <a href="#">EFUSE_PGM_DATA0 ~ 7_REG</a> |
| 10    | <a href="#">EFUSE_RD_SYS_PART2_DATA0 ~ 7_REG</a>                           | <a href="#">EFUSE_PGM_DATA0 ~ 7_REG</a> |

### Updating reading data registers

The eFuse controller reads eFuse memory to update corresponding registers. This read operation happens at system reset and can also be triggered manually by users as needed (e.g., if new eFuse values have been programmed). The process of triggering a read operation by users is as follows:

1. Configure the field [EFUSE\\_OP\\_CODE](#) in register [EFUSE\\_CONF\\_REG](#) to 0x5AA5.
2. Configure the field [EFUSE\\_READ\\_CMD](#) in register [EFUSE\\_CMD\\_REG](#) to 1.
3. Poll register [EFUSE\\_CMD\\_REG](#) until it is 0x0, or wait for a READ\_DONE interrupt. Information on how to identify a PGM\_DONE or READ\_DONE interrupt is provided below in this section.
4. Read the values of each parameter from eFuse memory.

The eFuse read registers will hold all values until the next read operation.

### Error detection

The programming error record registers allows users to check the integrity of parameters stored in the eFuse memory. For instance, they can help detect whether the four-backup parameters are consistent and whether parameters protected by RS encoding are decoded successfully.

Registers [EFUSE\\_RD\\_REPEAT\\_ERRO ~ 3\\_REG](#) indicate if there are any errors in programming parameters (except [EFUSE\\_WR\\_DIS](#)) to BLOCK0. The value 1 indicates an error is detected in programming the corresponding bit. The value 0 indicates no error.

Registers [EFUSE\\_RD\\_RS\\_ERRO ~ 1\\_REG](#) store the number of corrected bytes as well as the result of RS decoding when eFuse controller reads BLOCK1 ~ BLOCK10.

The values of the above registers will be updated every time the reading data registers of eFuse controller have been updated.

### Identifying completion of program or read operations

The methods to identify the completion of a program/read operation are described below. Please note that bit 1 corresponds to a program operation, and bit 0 corresponds to a read operation.

- Method one: Poll bit 1/0 in register [EFUSE\\_INT\\_RAW\\_REG](#) until it becomes 1, which represents the completion of a program/read operation.
- Method two:
  1. Set bit 1/0 in register [EFUSE\\_INT\\_ENA\\_REG](#) to 1 to enable the eFuse controller to post a PGM\_DONE or READ\_DONE interrupt.

2. Configure the Interrupt Matrix to enable the CPU to respond to eFuse interrupt signals. See Chapter 11 [Interrupt Matrix](#).
3. Wait for the PGM\_DONE or READ\_DONE interrupt.
4. Set bit 1/0 in register [EFUSE\\_INT\\_CLR\\_REG](#) to 1 to clear the PGM\_DONE or READ\_DONE interrupt.

#### Note

When eFuse controller is updating its registers, it will use [EFUSE\\_PGM\\_DATA<sub>n</sub>\\_REG](#) (n=0, 1, ... ,7) again to store data. So please do not write important data into these registers before this updating process is initiated.

During the chip boot process, eFuse controller will automatically update data from eFuse memory into the registers that can be accessed by users. Users can get programmed eFuse data by reading corresponding registers. Thus, there is no need to update the reading data registers in such case.

### 7.3.4 eFuse VDDQ Timing

The eFuse controller operates at the clock frequency of 20 MHz, and its programming voltage VDDQ should be configured as follows:

- [EFUSE\\_DAC\\_NUM](#) (the rising period of VDDQ): The default value of VDDQ is 2.5 V and the voltage increases by 0.01 V in each clock cycle. The default value of this parameter is 255.
- [EFUSE\\_DAC\\_CLK\\_DIV](#) (the clock divisor of VDDQ): The clock period to program VDDQ should be larger than 1  $\mu$ s.
- [EFUSE\\_PWR\\_ON\\_NUM](#) (the power-up time for VDDQ): The programming voltage should be stabilized after this time, which means the value of this parameter should be configured to exceed the result of [EFUSE\\_DAC\\_CLK\\_DIV](#) times [EFUSE\\_DAC\\_NUM](#).
- [EFUSE\\_PWR\\_OFF\\_NUM](#) (the power-out time for VDDQ): The value of this parameter should be larger than 10  $\mu$ s.

Table 7.3-5. Configuration of Default VDDQ Timing Parameters

| <a href="#">EFUSE_DAC_NUM</a> | <a href="#">EFUSE_DAC_CLK_DIV</a> | <a href="#">EFUSE_PWR_ON_NUM</a> | <a href="#">EFUSE_PWR_OFF_NUM</a> |
|-------------------------------|-----------------------------------|----------------------------------|-----------------------------------|
| 0xFF                          | 0x28                              | 0x3000                           | 0x190                             |

### 7.3.5 Parameters Used by Hardware Modules

Some hardware modules are directly connected to the eFuse peripheral in order to use the parameters that are marked with “Y” in columns “Accessible by Hardware” of Table 7.3-1 and Table 7.3-3. Users cannot intervene in this process.

## 7.4 Interrupts

ESP32-P4's eFuse controller can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- EFUSE\_INT



There are several internal interrupt sources from eFuse controller that can generate the above interrupt signal. The interrupt sources from eFuse controller are listed with their trigger conditions and the resulted interrupt signal in Table 7.4-1.

**Table 7.4-1. eFuse's Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition              | Interrupt Signal |
|---------------------------|--------------------------------|------------------|
| EFUSE_PGM_DONE_INT        | Programming of eFuse completes | EFUSE_INT        |
| EFUSE_READ_DONE_INT       | Reading of eFuse completes     |                  |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section 7.5 [Register Summary](#).

## 7.5 Register Summary

The addresses in this section are relative to eFuse controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <b>Programming Data Registers</b>            |   |         |        |
| <a href="#">EFUSE_PGM_DATA0_REG</a>          | Register 0 that stores data to be programmed  | 0x0000  | R/W    |
| <a href="#">EFUSE_PGM_DATA1_REG</a>          | Register 1 that stores data to be programmed  | 0x0004  | R/W    |
| <a href="#">EFUSE_PGM_DATA2_REG</a>          | Register 2 that stores data to be programmed  | 0x0008  | R/W    |
| <a href="#">EFUSE_PGM_DATA3_REG</a>          | Register 3 that stores data to be programmed  | 0x000C  | R/W    |
| <a href="#">EFUSE_PGM_DATA4_REG</a>          | Register 4 that stores data to be programmed  | 0x0010  | R/W    |
| <a href="#">EFUSE_PGM_DATA5_REG</a>          | Register 5 that stores data to be programmed  | 0x0014  | R/W    |
| <a href="#">EFUSE_PGM_DATA6_REG</a>          | Register 6 that stores data to be programmed  | 0x0018  | R/W    |
| <a href="#">EFUSE_PGM_DATA7_REG</a>          | Register 7 that stores data to be programmed  | 0x001C  | R/W    |
| <a href="#">EFUSE_PGM_CHECK_VALUE0_REG</a>   | Register 0 that stores the RS code to be programmed   | 0x0020  | R/W    |
| <a href="#">EFUSE_PGM_CHECK_VALUE1_REG</a>   | Register 1 that stores the RS code to be programmed   | 0x0024  | R/W    |
| <a href="#">EFUSE_PGM_CHECK_VALUE2_REG</a>   | Register 2 that stores the RS code to be programmed   | 0x0028  | R/W    |
| <b>Reading Data Registers for BLOCK0</b>     |   |         |        |
| <a href="#">EFUSE_RD_WR_DIS_REG</a>          | BLOCK0 data register 0 that represents whether programming of individual eFuse memory bit is disabled | 0x002C  | RO     |
| <a href="#">EFUSE_RD_REPEAT_DATA0_REG</a>    | BLOCK0 data register 1  | 0x0030  | RO     |
| <a href="#">EFUSE_RD_REPEAT_DATA1_REG</a>    | BLOCK0 data register 2  | 0x0034  | RO     |
| <a href="#">EFUSE_RD_REPEAT_DATA2_REG</a>    | BLOCK0 data register 3  | 0x0038  | RO     |
| <a href="#">EFUSE_RD_REPEAT_DATA3_REG</a>    | BLOCK0 data register 4  | 0x003C  | RO     |
| <a href="#">EFUSE_RD_REPEAT_DATA4_REG</a>    | BLOCK0 data register 5  | 0x0040  | RO     |
| <b>Reading Data Registers for BLOCK1</b>     |   |         |        |
| <a href="#">EFUSE_RD_MAC_SYS_0_REG</a>       | BLOCK1 data register 0  | 0x0044  | RO     |
| <a href="#">EFUSE_RD_MAC_SYS_1_REG</a>       | BLOCK1 data register 1  | 0x0048  | RO     |
| <a href="#">EFUSE_RD_MAC_SYS_2_REG</a>       | BLOCK1 data register 2  | 0x004C  | RO     |
| <a href="#">EFUSE_RD_MAC_SYS_3_REG</a>       | BLOCK1 data register 3  | 0x0050  | RO     |
| <a href="#">EFUSE_RD_MAC_SYS_4_REG</a>       | BLOCK1 data register 4  | 0x0054  | RO     |
| <a href="#">EFUSE_RD_MAC_SYS_5_REG</a>       | BLOCK1 data register 5  | 0x0058  | RO     |
| <b>Reading Data Registers for BLOCK2</b>     |   |         |        |
| <a href="#">EFUSE_RD_SYS_PART1_DATA0_REG</a> | Register 0 for BLOCK2 (system)  | 0x005C  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA1_REG</a> | Register 1 for BLOCK2 (system)  | 0x0060  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA2_REG</a> | Register 2 for BLOCK2 (system)  | 0x0064  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA3_REG</a> | Register 3 for BLOCK2 (system)  | 0x0068  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA4_REG</a> | Register 4 for BLOCK2 (system)  | 0x006C  | RO     |

| Name   | Description                    | Address | Access |
|--|--------------------------------|---------|--------|
| <a href="#">EFUSE_RD_SYS_PART1_DATA5_REG</a> | Register 5 for BLOCK2 (system) | 0x0070  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA6_REG</a> | Register 6 for BLOCK2 (system) | 0x0074  | RO     |
| <a href="#">EFUSE_RD_SYS_PART1_DATA7_REG</a> | Register 7 for BLOCK2 (system) | 0x0078  | RO     |
| <b>Reading Data Registers for BLOCK3</b>     |                                |         |        |
| <a href="#">EFUSE_RD_USR_DATA0_REG</a>       | Register 0 for BLOCK3 (user)   | 0x007C  | RO     |
| <a href="#">EFUSE_RD_USR_DATA1_REG</a>       | Register 1 for BLOCK3 (user)   | 0x0080  | RO     |
| <a href="#">EFUSE_RD_USR_DATA2_REG</a>       | Register 2 for BLOCK3 (user)   | 0x0084  | RO     |
| <a href="#">EFUSE_RD_USR_DATA3_REG</a>       | Register 3 for BLOCK3 (user)   | 0x0088  | RO     |
| <a href="#">EFUSE_RD_USR_DATA4_REG</a>       | Register 4 for BLOCK3 (user)   | 0x008C  | RO     |
| <a href="#">EFUSE_RD_USR_DATA5_REG</a>       | Register 5 for BLOCK3 (user)   | 0x0090  | RO     |
| <a href="#">EFUSE_RD_USR_DATA6_REG</a>       | Register 6 for BLOCK3 (user)   | 0x0094  | RO     |
| <a href="#">EFUSE_RD_USR_DATA7_REG</a>       | Register 7 for BLOCK3 (user)   | 0x0098  | RO     |
| <b>Reading Data Registers for BLOCK4</b>     |                                |         |        |
| <a href="#">EFUSE_RD_KEY0_DATA0_REG</a>      | Register 0 for BLOCK4 (KEY0)   | 0x009C  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA1_REG</a>      | Register 1 for BLOCK4 (KEY0)   | 0x00A0  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA2_REG</a>      | Register 2 for BLOCK4 (KEY0)   | 0x00A4  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA3_REG</a>      | Register 3 for BLOCK4 (KEY0)   | 0x00A8  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA4_REG</a>      | Register 4 for BLOCK4 (KEY0)   | 0x00AC  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA5_REG</a>      | Register 5 for BLOCK4 (KEY0)   | 0x00B0  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA6_REG</a>      | Register 6 for BLOCK4 (KEY0)   | 0x00B4  | RO     |
| <a href="#">EFUSE_RD_KEY0_DATA7_REG</a>      | Register 7 for BLOCK4 (KEY0)   | 0x00B8  | RO     |
| <b>Reading Data Registers for BLOCK5</b>     |                                |         |        |
| <a href="#">EFUSE_RD_KEY1_DATA0_REG</a>      | Register 0 for BLOCK5 (KEY1)   | 0x00BC  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA1_REG</a>      | Register 1 for BLOCK5 (KEY1)   | 0x00C0  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA2_REG</a>      | Register 2 for BLOCK5 (KEY1)   | 0x00C4  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA3_REG</a>      | Register 3 for BLOCK5 (KEY1)   | 0x00C8  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA4_REG</a>      | Register 4 for BLOCK5 (KEY1)   | 0x00CC  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA5_REG</a>      | Register 5 for BLOCK5 (KEY1)   | 0x00D0  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA6_REG</a>      | Register 6 for BLOCK5 (KEY1)   | 0x00D4  | RO     |
| <a href="#">EFUSE_RD_KEY1_DATA7_REG</a>      | Register 7 for BLOCK5 (KEY1)   | 0x00D8  | RO     |
| <b>Reading Data Registers for BLOCK6</b>     |                                |         |        |
| <a href="#">EFUSE_RD_KEY2_DATA0_REG</a>      | Register 0 for BLOCK6 (KEY2)   | 0x00DC  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA1_REG</a>      | Register 1 for BLOCK6 (KEY2)   | 0x00E0  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA2_REG</a>      | Register 2 for BLOCK6 (KEY2)   | 0x00E4  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA3_REG</a>      | Register 3 for BLOCK6 (KEY2)   | 0x00E8  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA4_REG</a>      | Register 4 for BLOCK6 (KEY2)   | 0x00EC  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA5_REG</a>      | Register 5 for BLOCK6 (KEY2)   | 0x00F0  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA6_REG</a>      | Register 6 for BLOCK6 (KEY2)   | 0x00F4  | RO     |
| <a href="#">EFUSE_RD_KEY2_DATA7_REG</a>      | Register 7 for BLOCK6 (KEY2)   | 0x00F8  | RO     |
| <b>Reading Data Registers for BLOCK7</b>     |                                |         |        |
| <a href="#">EFUSE_RD_KEY3_DATA0_REG</a>      | Register 0 for BLOCK7 (KEY3)   | 0x00FC  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA1_REG</a>      | Register 1 for BLOCK7 (KEY3)   | 0x0100  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA2_REG</a>      | Register 2 for BLOCK7 (KEY3)   | 0x0104  | RO     |

| Name   | Description                                       | Address | Access |
|--|---|---------|--------|
| <a href="#">EFUSE_RD_KEY3_DATA3_REG</a>      | Register 3 for BLOCK7 (KEY3)                      | 0x0108  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA4_REG</a>      | Register 4 for BLOCK7 (KEY3)                      | 0x010C  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA5_REG</a>      | Register 5 for BLOCK7 (KEY3)                      | 0x0110  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA6_REG</a>      | Register 6 for BLOCK7 (KEY3)                      | 0x0114  | RO     |
| <a href="#">EFUSE_RD_KEY3_DATA7_REG</a>      | Register 7 for BLOCK7 (KEY3)                      | 0x0118  | RO     |
| <b>Reading Data Registers for BLOCK8</b>     |   |         |        |
| <a href="#">EFUSE_RD_KEY4_DATA0_REG</a>      | Register 0 for BLOCK8 (KEY4)                      | 0x011C  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA1_REG</a>      | Register 1 for BLOCK8 (KEY4)                      | 0x0120  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA2_REG</a>      | Register 2 for BLOCK8 (KEY4)                      | 0x0124  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA3_REG</a>      | Register 3 for BLOCK8 (KEY4)                      | 0x0128  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA4_REG</a>      | Register 4 for BLOCK8 (KEY4)                      | 0x012C  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA5_REG</a>      | Register 5 for BLOCK8 (KEY4)                      | 0x0130  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA6_REG</a>      | Register 6 for BLOCK8 (KEY4)                      | 0x0134  | RO     |
| <a href="#">EFUSE_RD_KEY4_DATA7_REG</a>      | Register 7 for BLOCK8 (KEY4)                      | 0x0138  | RO     |
| <b>Reading Data Registers for BLOCK9</b>     |   |         |        |
| <a href="#">EFUSE_RD_KEY5_DATA0_REG</a>      | Register 0 for BLOCK9 (KEY5)                      | 0x013C  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA1_REG</a>      | Register 1 for BLOCK9 (KEY5)                      | 0x0140  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA2_REG</a>      | Register 2 for BLOCK9 (KEY5)                      | 0x0144  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA3_REG</a>      | Register 3 for BLOCK9 (KEY5)                      | 0x0148  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA4_REG</a>      | Register 4 for BLOCK9 (KEY5)                      | 0x014C  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA5_REG</a>      | Register 5 for BLOCK9 (KEY5)                      | 0x0150  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA6_REG</a>      | Register 6 for BLOCK9 (KEY5)                      | 0x0154  | RO     |
| <a href="#">EFUSE_RD_KEY5_DATA7_REG</a>      | Register 7 for BLOCK9 (KEY5)                      | 0x0158  | RO     |
| <b>Reading Data Registers for BLOCK10</b>    |   |         |        |
| <a href="#">EFUSE_RD_SYS_PART2_DATA0_REG</a> | Register 0 for BLOCK10 (system)                   | 0x015C  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA1_REG</a> | Register 1 for BLOCK10 (system)                   | 0x0160  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA2_REG</a> | Register 2 for BLOCK10 (system)                   | 0x0164  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA3_REG</a> | Register 3 for BLOCK10 (system)                   | 0x0168  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA4_REG</a> | Register 4 for BLOCK10 (system)                   | 0x016C  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA5_REG</a> | Register 5 for BLOCK10 (system)                   | 0x0170  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA6_REG</a> | Register 6 for BLOCK10 (system)                   | 0x0174  | RO     |
| <a href="#">EFUSE_RD_SYS_PART2_DATA7_REG</a> | Register 7 for BLOCK10 (system)                   | 0x0178  | RO     |
| <b>Error Report Registers for BLOCK0</b>     |   |         |        |
| <a href="#">EFUSE_RD_REPEAT_ERR0_REG</a>     | Programming error record register 0 for BLOCK0    | 0x017C  | RO     |
| <a href="#">EFUSE_RD_REPEAT_ERR1_REG</a>     | Programming error record register 1 for BLOCK0    | 0x0180  | RO     |
| <a href="#">EFUSE_RD_REPEAT_ERR2_REG</a>     | Programming error record register 2 for BLOCK0    | 0x0184  | RO     |
| <a href="#">EFUSE_RD_REPEAT_ERR3_REG</a>     | Programming error record register 3 for BLOCK0    | 0x0188  | RO     |
| <a href="#">EFUSE_RD_REPEAT_ERR4_REG</a>     | Programming error record register 4 for BLOCK0    | 0x018C  | RO     |
| <b>Error Report Registers for RS Block</b>   |   |         |        |
| <a href="#">EFUSE_RD_RS_ERR0_REG</a>         | Programming error record register 0 for BLOCK1-10 | 0x01C0  | RO     |

| Name   | Description  | Address | Access   |
|--|--|---------|----------|
| <a href="#">EFUSE_RD_RS_ERR1_REG</a>             | Programming error record register 1 for BLOCK1-10                    | 0x01C4  | RO       |
| <b>eFuse Clock Register</b>                      |  |         |          |
| <a href="#">EFUSE_CLK_REG</a>                    | eFuse clock configuration register                                   | 0x01C8  | R/W      |
| <b>eFuse Configuration Registers</b>             |  |         |          |
| <a href="#">EFUSE_CONF_REG</a>                   | Configures eFuse operation mode                                      | 0x01CC  | R/W      |
| <a href="#">EFUSE_DAC_CONF_REG</a>               | Configures the eFuse programming voltage                             | 0x01E8  | R/W      |
| <a href="#">EFUSE_RD_TIM_CONF_REG</a>            | Configures read timing parameters                                    | 0x01EC  | R/W      |
| <a href="#">EFUSE_WR_TIM_CONF1_REG</a>           | Configures eFuse programming timing parameters                       | 0x01F0  | R/W      |
| <a href="#">EFUSE_WR_TIM_CONF2_REG</a>           | Configures eFuse programming timing parameters                       | 0x01F4  | R/W      |
| <a href="#">EFUSE_WR_TIM_CONFO_RS_BYPASS_REG</a> | Configures eFuse programming time parameters and RS bypass operation | 0x01F8  | varies   |
| <b>eFuse Status Register</b>                     |  |         |          |
| <a href="#">EFUSE_STATUS_REG</a>                 | eFuse status register  | 0x01D0  | RO       |
| <b>eFuse Command Registers</b>                   |  |         |          |
| <a href="#">EFUSE_CMD_REG</a>                    | eFuse command register   | 0x01D4  | varies   |
| <b>eFuse Interrupt Registers</b>                 |  |         |          |
| <a href="#">EFUSE_INT_RAW_REG</a>                | eFuse raw interrupt register   | 0x01D8  | R/SS/WTC |
| <a href="#">EFUSE_INT_ST_REG</a>                 | eFuse interrupt status register                                      | 0x01DC  | RO       |
| <a href="#">EFUSE_INT_ENA_REG</a>                | eFuse interrupt enable register                                      | 0x01E0  | R/W      |
| <a href="#">EFUSE_INT_CLR_REG</a>                | eFuse interrupt clear register                                       | 0x01E4  | WT       |
| <b>eFuse Version Register</b>                    |  |         |          |
| <a href="#">EFUSE_DATE_REG</a>                   | eFuse version control register                                       | 0x01FC  | R/W      |

## 7.6 Registers

The addresses in this section are relative to eFuse controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 7.1. EFUSE\_PGM\_DATA $n$ \_REG ( $n$ : 0-7) (0x0000+0x4\* $n$ )**

|                     |   |
|---------------------|---|
| EFUSE_PGM_DATA_ $n$ |   |
| 31                  | 0 |
| 0x000000            |   |
| Reset               |   |

**EFUSE\_PGM\_DATA\_ $n$**  Configures the  $n$ th 32-bit data to be programmed. (R/W)

**Register 7.2. EFUSE\_PGM\_CHECK\_VALUE $m$ \_REG ( $m$ : 0-2) (0x0020+0x4\* $m$ )**

|                        |   |
|------------------------|---|
| EFUSE_PGM_RS_DATA_ $m$ |   |
| 31                     | 0 |
| 0x000000               |   |
| Reset                  |   |

**EFUSE\_PGM\_RS\_DATA\_ $m$**  Configures the  $m$ th 32-bit RS code to be programmed. (R/W)

**Register 7.3. EFUSE\_RD\_WR\_DIS\_REG (0x002C)**

|              |   |
|--------------|---|
| EFUSE_WR_DIS |   |
| 31           | 0 |
| 0x000000     |   |
| Reset        |   |

**EFUSE\_WR\_DIS** Represents whether programming of individual eFuse memory bit is disabled.

1: Disabled

0: Enabled

(RO)

#### Register 7.4. EFUSE\_RD\_REPEAT\_DATA0\_REG (0x0030)

[illegible]

**EFUSE\_RD\_DIS** Represents whether reading of individual eFuse block (BLOCK4 ~ BLOCK10) is disabled.

1: Disabled

0: Enabled

(RO)

**EFUSE\_USB\_DEVICE\_EXCHG\_PINS** Represents whether the USB Serial/JTAG pins D+ and D- are exchanged.

0: Not exchanged

1: Exchanged

(RO)

**EFUSE\_USB\_OTG11\_EXCHG\_PINS** Represents whether the USB FS pins D+ and D- are exchanged.

0: Not exchanged

1: Exchanged

(RO)

**EFUSE\_DIS\_USB\_JTAG** Represents whether the USB-to-JTAG function in USB Serial/JTAG is disabled.

1: Disabled

0: Enabled

(RO)

**EFUSE\_POWERGLITCH\_EN** Represents whether power glitch detection is enabled.

0: Disabled

1: Enabled

(RO)

**EFUSE\_DIS\_FORCE\_DOWNLOAD** Represents whether the function that forces chip into Download mode is disabled.

1: Disabled

0: Enabled

(RO)

**EFUSE\_SPI\_DOWNLOAD\_MSPI\_DIS** Represents accessing MSPI flash/MSPI RAM by SYS AXI matrix is disabled during boot\_mode\_download.

1: Disabled

0: Enabled

**EFUSE\_DIS\_TWAI** Represents whether TWAI function is disabled.

1: Disabled

### Register 7.5. EFUSE\_RD\_REPEAT\_DATA1\_REG (0x0034)

|                     |  |    |  |     |  |    |  |    |  |    |  |    |  |                     |  |    |  |     |  |    |  |    |  |    |  |    |  |                               |  |  |  |       |  |  |  |  |  |  |  |   |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------|--|----|--|-----|--|----|--|----|--|----|--|----|--|---------------------|--|----|--|-----|--|----|--|----|--|----|--|----|--|-------------------------------|--|--|--|-------|--|--|--|--|--|--|--|---|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| EFUSE_KEY_PURPOSE_1 |  |    |  |     |  |    |  |    |  |    |  |    |  | EFUSE_KEY_PURPOSE_0 |  |    |  |     |  |    |  |    |  |    |  |    |  | EFUSE_SECURE_BOOT_KEY_REVOKE2 |  |  |  |       |  |  |  |  |  |  |  |   |  | EFUSE_SECURE_BOOT_KEY_REVOKE1 |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_BOOT_KEY_REVOKE0 |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SPI_BOOT_CRYPT_CNT |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_WDT_DELAY_SEL |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_XTS_KEY_LENGTH_256 |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                  |  | 28 |  | 27  |  | 24 |  | 23 |  | 22 |  | 21 |  | 20                  |  | 18 |  | 17  |  | 16 |  | 15 |  | 14 |  | 13 |  | 0                             |  |  |  |       |  |  |  |  |  |  |  |   |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x0                 |  |    |  | 0x0 |  |    |  | 0  |  | 0  |  | 0  |  | 0x0                 |  |    |  | 0x0 |  |    |  | 0  |  | 0  |  | 0  |  | x                             |  |  |  |       |  |  |  |  |  |  |  | 0 |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                     |  |    |  |     |  |    |  |    |  |    |  |    |  |                     |  |    |  |     |  |    |  |    |  |    |  |    |  |                               |  |  |  | Reset |  |  |  |  |  |  |  |   |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |

**EFUSE\_XTS\_KEY\_LENGTH\_256** Represents which key is used for flash encryption.

0: XTS-256 key. Key length: 512 bits.

1: XTS-128 key. Key length: 256 bits.

(RO)

**EFUSE\_WDT\_DELAY\_SEL** Represents RTC watchdog timeout threshold.

0: The originally configured STGO threshold  $\times 2$

1: The originally configured STGO threshold  $\times 4$

2: The originally configured STGO threshold  $\times 8$

3: The originally configured STGO threshold  $\times 16$

(RO)

**EFUSE\_SPI\_BOOT\_CRYPT\_CNT** Represents whether SPI boot encryption/decryption is enabled.

Odd count of bits with a value of 1: Enabled

Even count of bits with a value of 1: Disabled

(RO)

**EFUSE\_SECURE\_BOOT\_KEY\_REVOKEO** Represents whether revoking Secure Boot key 0 is enabled.

1: Enabled

0: Disabled

(RO)

Continued on the next page...



**Register 7.5. EFUSE\_RD\_REPEAT\_DATA1\_REG (0x0034)**

Continued from the previous page...

**EFUSE\_SECURE\_BOOT\_KEY\_REVOKE1** Represents whether revoking Secure Boot key 1 is enabled.

1: Enabled  
0: Disabled  
(RO)

**EFUSE\_SECURE\_BOOT\_KEY\_REVOKE2** Represents whether revoking Secure Boot key 2 is enabled.

1: Enabled  
0: Disabled  
(RO)

**EFUSE\_KEY\_PURPOSE\_0** Represents the purpose of Key0. See Table 7.3-2. (RO)

**EFUSE\_KEY\_PURPOSE\_1** Represents the purpose of Key1. See Table 7.3-2. (RO)

**Register 7.6. EFUSE\_RD\_REPEAT\_DATA2\_REG (0x0038)**

|                  |  |    |  |    |    |    |    |    |    |    |    |    |    |    |     |     |  |     |  |     |   |                                 |   |     |  |     |   |     |  |       |  |                    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |
|------------------|--|----|--|----|----|----|----|----|----|----|----|----|----|----|-----|-----|--|-----|--|-----|---|---------------------------------|---|-----|--|-----|---|-----|--|-------|--|--------------------|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|
| EFUSE_FLASH_TPUW |  |    |  |    |    |    |    |    |    |    |    |    |    |    |     |     |  |     |  |     |   | EFUSE_DIS_USB_OTG_DOWNLOAD_MODE |   |     |  |     |   |     |  |       |  | EFUSE_FLASH_ECC_EN |  |  |  |  |  |  |  |  |  | EFUSE_FLASH_PAGE_SIZE |  |  |  |  |  |  |  |  |  | EFUSE_FLASH_TYPE (reserved) |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_BOOT_SIZE (reserved) |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_BOOT_EN |  |  |  |  |  |  |  |  |  | EFUSE_CRYPT_DPA_ENABLE |  |  |  |  |  |  |  |  |  | EFUSE_SEC_DPA_LEVEL |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_5 |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_4 |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_3 |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_2 |  |  |  |  |  |  |  |  |  |
| 31               |  | 28 |  | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16  | 15  |  | 12  |  | 11  | 8 |                                 | 7 | 4   |  | 3   | 0 |     |  |       |  |                    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |
| 0x0              |  |    |  | 0  | 0  | 0  |    | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 0x0 | 0x0 |  | 0x0 |  | 0x0 |   | 0x0                             |   | 0x0 |  | 0x0 |   | 0x0 |  | Reset |  |                    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |

**EFUSE\_KEY\_PURPOSE\_2** Represents the purpose of Key2. See Table 7.3-2. (RO)

**EFUSE\_KEY\_PURPOSE\_3** Represents the purpose of Key3. See Table 7.3-2. (RO)

**EFUSE\_KEY\_PURPOSE\_4** Represents the purpose of Key4. See Table 7.3-2. (RO)

**EFUSE\_KEY\_PURPOSE\_5** Represents the purpose of Key5. See Table 7.3-2. (RO)

**EFUSE\_SEC\_DPA\_LEVEL** Represents the security level of anti-DPA attack. The level is adjusted by configuring the clock random frequency division mode.

0: Security level is SEC\_DPA\_OFF

1: Security level is SEC\_DPA\_LOW

2: Security level is SEC\_DPA\_MIDDLE

3: Security level is SEC\_DPA\_HIGH

For more information, please refer to Chapter 3 *System Registers [to be added later]* > Section 3.1 *Anti-DPA Attack Security Control [to be added later]*.

(RO)

**EFUSE\_CRYPT\_DPA\_ENABLE** Represents whether defense against DPA attack is enabled.

1: Enabled

0: Disabled

(RO)

**EFUSE\_SECURE\_BOOT\_EN** Represents whether Secure Boot is enabled.

1: Enabled

0: Disabled

(RO)

**EFUSE\_SECURE\_BOOT\_AGGRESSIVE\_REVOKE** Represents whether aggressive revocation of Secure Boot is enabled.

1: Enabled

0: Disabled

(RO)

Continued on the next page...

**Register 7.6. EFUSE\_RD\_REPEAT\_DATA2\_REG (0x0038)**

Continued from the previous page...

**EFUSE\_FLASH\_TYPE** Represents the type of the interfaced flash.

0: Four data lines

1: eight data lines

(RO)

**EFUSE\_FLASH\_PAGE\_SIZE** Represents flash page size.

0: 256 bytes

1: 512 bytes

2: 1024 bytes

3: 2048 bytes

(RO)

**EFUSE\_FLASH\_ECC\_EN** Represents whether ECC is enabled during flash boot.

0: Disabled

1: Enabled

(RO)

**EFUSE\_DIS\_USB\_OTG\_DOWNLOAD\_MODE** Represents whether download via USB-OTG is disabled.

0: Enabled

1: Disabled

(RO)

**EFUSE\_FLASH\_TPUW** Represents the flash waiting time after power-up. Measurement unit: ms.

When the value is less than 15, the waiting time is the programmed value. Otherwise, the waiting time is a fixed value, i.e., 30 ms. (RO)

Register 7.7. EFUSE\_RD\_REPEAT\_DATA3\_REG (0x003C)

|                 |  |    |  |   |   |      |    |    |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |   |     |   |   |   |   |   |   |   |                                     |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-----------------|--|----|--|---|---|------|----|----|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|---|-----|---|---|---|---|---|---|---|-------------------------------------|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| EFUSE_DCDC_VSET |  |    |  |   |   |      |    |    |  |  |  |  |  |  |  | EFUSE_HYS_EN_PAD |  |  |  |  |  |  |   |     |   |   |   |   |   |   |   | EFUSE_SECURE_BOOT_DISABLE_FAST_WAKE |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_VERSION |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_FORCE_SEND_RESUME |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_UART_PRINT_CONTROL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_ENABLE_SECURITY_DOWNLOAD |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_DIS_USB_SERIAL_JTAG_DOWNLOAD_MODE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_DIS_DIRECT_BOOT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_DIS_DOWNLOAD_MODE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31              |  | 27 |  |   |   | 26   | 25 | 24 |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |   |     | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2                                   | 1 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x0             |  |    |  | 0 | 0 | 0x00 |    |    |  |  |  |  |  |  |  |                  |  |  |  |  |  |  | 0 | 0x0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |                                     |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**EFUSE\_DIS\_DOWNLOAD\_MODE** Represents whether all Download modes are disabled.

1: Disabled  
0: Enabled  
(RO)

**EFUSE\_DIS\_DIRECT\_BOOT** Represents whether direct boot mode is disabled.

1: Disabled  
0: Enabled  
(RO)

**EFUSE\_DIS\_USB\_SERIAL\_JTAG\_ROM\_PRINT** Represents whether print from USB-Serial-JTAG during ROM boot is disabled.

1: Disabled  
0: Enabled  
(RO)

**EFUSE\_DIS\_USB\_SERIAL\_JTAG\_DOWNLOAD\_MODE** Represents whether the USB-Serial-JTAG download function is disabled.

1: Disabled  
0: Enabled  
(RO)

**EFUSE\_ENABLE\_SECURITY\_DOWNLOAD** Represents whether security download is enabled. Only UART is supported for download. Reading/writing RAM or registers is not supported (i.e., stub download is not supported).

1: Enabled  
0: Disabled  
(RO)

Continued on the next page...

**Register 7.7. EFUSE\_RD\_REPEAT\_DATA3\_REG (0x003C)**

Continued from the previous page...

**EFUSE\_UART\_PRINT\_CONTROL** Represents the type of UART printing.

- 0: Force enable printing.
  - 1: Enable printing when GPIO36 is reset at low level.
  - 2: Enable printing when GPIO36 is reset at high level.
  - 3: Force disable printing.
- (RO)

**EFUSE\_FORCE\_SEND\_RESUME** Represents whether ROM code is forced to send a resume command during SPI boot.

- 1: Forced.
  - 0: Not forced.
- (RO)

**EFUSE\_SECURE\_VERSION** Represents the security version used by ESP-IDF anti-rollback feature.

(RO)

**EFUSE\_SECURE\_BOOT\_DISABLE\_FAST\_WAKE** Represents whether FAST VERIFY ON WAKE is disabled when Secure Boot is enabled.

- 1: Disabled
  - 0: Enabled
- (RO)

**EFUSE\_HYS\_EN\_PAD** Represents whether the hysteresis function of PADO – PAD27 is enabled.

- 1: Enabled
  - 0: Disabled
- (RO)

**EFUSE\_DCDC\_VSET** Represents the default DCDC voltage. (RO)

### Register 7.8. EFUSE\_RD\_REPEAT\_DATA4\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |    |   |    |    |    |    |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |    | EFUSE_DIS_SWDT<br>EFUSE_DIS_WDT<br>EFUSE_DCDC_VSET_EN<br>EFUSE_HP_PWR_SRC_SEL |    |    |    |    |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   | EFUSE_OPXA_TIEH_SEL_3<br>EFUSE_OPXA_TIEH_SEL_2<br>EFUSE_OPXA_TIEH_SEL_1<br>EFUSE_OPXA_TIEH_SEL_0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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| 31         |   |   |   |   |   |   |   |   | 22 | 21  | 20 | 19 | 18 | 17 |   |   |   |   |   |            |   |   | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1  | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0   | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EFUSE\_OPXA\_TIEH\_SEL\_0 Represents what controls the power supply for LDO V00.

- 0: The power supply is always high
  - 1: Controlled by the SDMMC1 peripheral
  - 2: Controlled by the PMU\_LDO\_VO\_TIEH\_O register field
  - 3: Controlled by the SDMMCO peripheral
- (RO)

EFUSE\_OPXA\_TIEH\_SEL\_1 Represents what controls the power supply for LDO VO1.

- 0: Controlled by the PMU\_LDO\_VO\_TIEH\_1 register field  
1: Controlled by the SDMMCO peripheral  
2: The power supply is always high  
3: Controlled by the SDMMC1 peripheral  
(RO)

**EFUSE\_OPXA\_TIEH\_SEL\_2** Represents what controls the power supply for LDO VO2.

- 0: Controlled by the PMU\_LDO\_VO\_TIEH\_2 register field  
1: Controlled by the SDMMCO peripheral  
2: The power supply is always high  
3: Controlled by the SDMMC1 peripheral  
(RO)

**EFUSE\_OPXA\_TIEH\_SEL\_3** Represents what controls the power supply for LDO VO3.

- 0: Controlled by the PMU\_LDO\_VO\_TIEH\_3 register field  
1: Controlled by the SDMMC0 peripheral  
2: The power supply is always high  
3: Controlled by the SDMMC1 peripheral  
(RO)

Continued on the next page...

**Register 7.8. EFUSE\_RD\_REPEAT\_DATA4\_REG (0x0040)**

Continued from the previous page...

**EFUSE\_HP\_PWR\_SRC\_SEL** Represents the HP system power source.

0: LDO

1: DCDC

(RO)

**EFUSE\_DCDC\_VSET\_EN** Represents whether to use the default voltage configured by [EFUSE\\_DCDC\\_VSET](#).

0: Not use

1: Use

(RO)

**EFUSE\_DIS\_WDT** Represents whether to disable the watchdog.

0: Enable

1: Disable

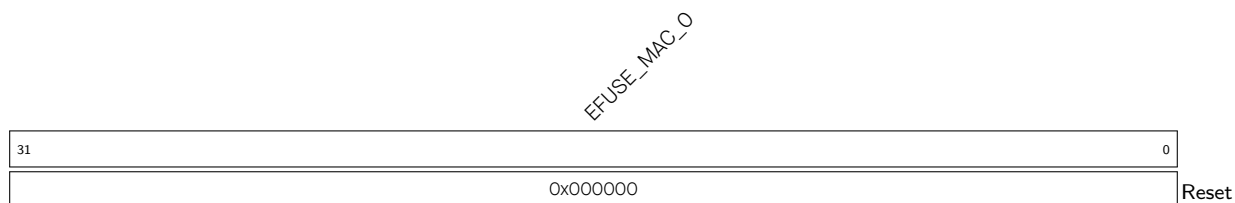
(RO)

**EFUSE\_DIS\_SWD** Represents whether to disable the super watchdog.

0: Enable

1: Disable

(RO)

**Register 7.9. EFUSE\_RD\_MAC\_SYS\_O\_REG (0x0044)****EFUSE\_MAC\_O** Represents the low 32 bits of MAC address. (RO)

**Register 7.10. EFUSE\_RD\_MAC\_SYS\_1\_REG (0x0048)**

|               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| EFUSE_MAC_EXT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | EFUSE_MAC_1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31            |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16 | 15          |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | 0x00        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**EFUSE\_MAC\_1** Represents the high 16 bits of MAC address. (RO)

**EFUSE\_MAC\_EXT** Represents the extended bits of MAC address. (RO)

**Register 7.11. EFUSE\_RD\_MAC\_SYS\_2\_REG (0x004C)**

|                      |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| EFUSE_MAC_RESERVED_0 |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_MAC_RESERVED_1 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31                   |  |  |  |  |  |  |  |  |  |  |  |  |  | 14                   | 13 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0x000                |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00                 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**EFUSE\_MAC\_RESERVED\_1** Reserved. (RO)

**EFUSE\_MAC\_RESERVED\_0** Reserved. (RO)

**Register 7.12. EFUSE\_RD\_MAC\_SYS\_3\_REG (0x0050)**

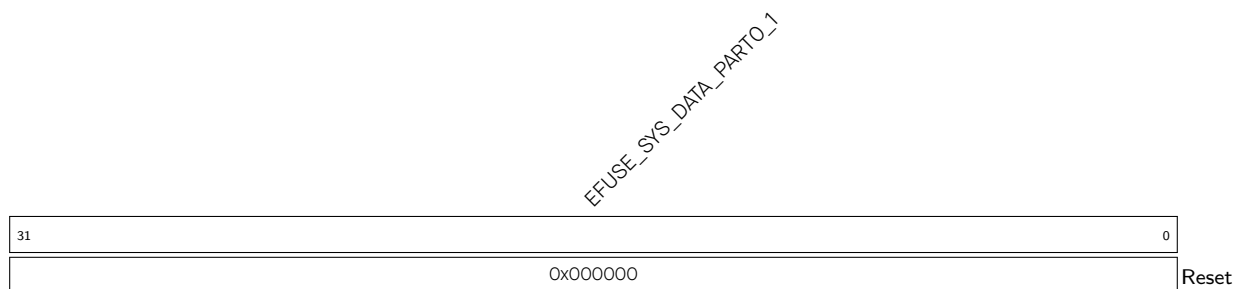
|                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |    |  |  |  |  |  |  |  |  |  |  |       |
|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|----|--|--|--|--|--|--|--|--|--|--|-------|
| EFUSE_SYS_DATA_PART0_0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_MAC_RESERVED_2 |    |  |  |  |  |  |  |  |  |  |  |       |
| 31                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 18                   | 17 |  |  |  |  |  |  |  |  |  |  | 0     |
| 0x00                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x000                |    |  |  |  |  |  |  |  |  |  |  | Reset |

**EFUSE\_MAC\_RESERVED\_2** Reserved. (RO)

**EFUSE\_SYS\_DATA\_PART0\_0** Represents the first 14 bits of the zeroth part of system data. (RO)

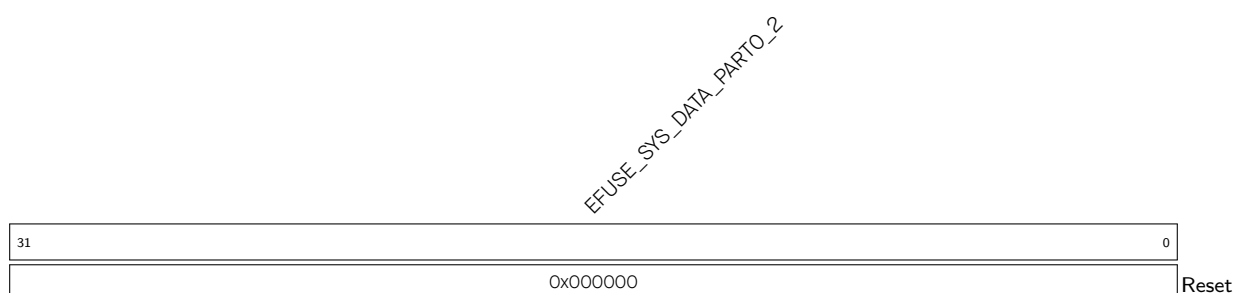


Register 7.13. EFUSE\_RD\_MAC\_SYS\_4\_REG (0x0054)

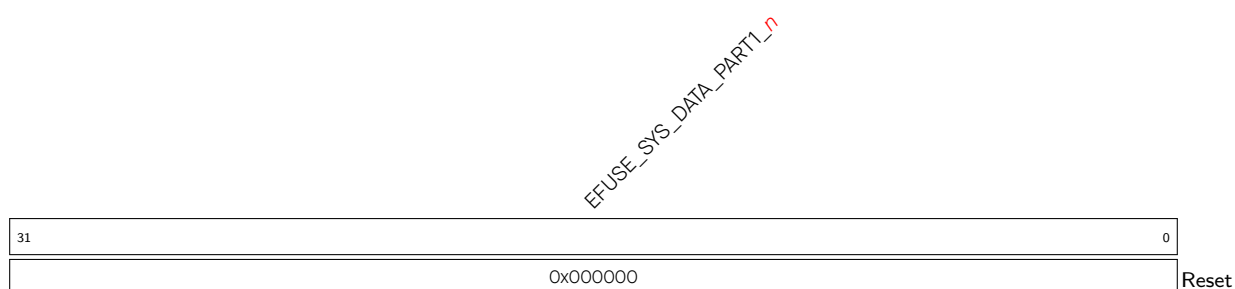


**EFUSE\_SYS\_DATA\_PART0\_1** Represents the first 32 bits of the zeroth part of system data. (RO)

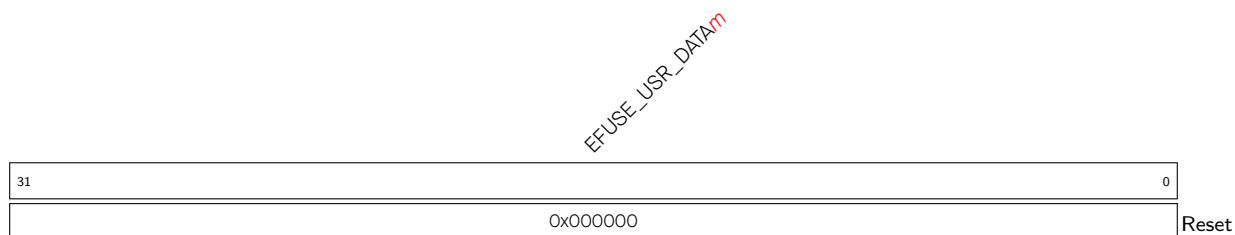
Register 7.14. EFUSE\_RD\_MAC\_SYS\_5\_REG (0x0058)



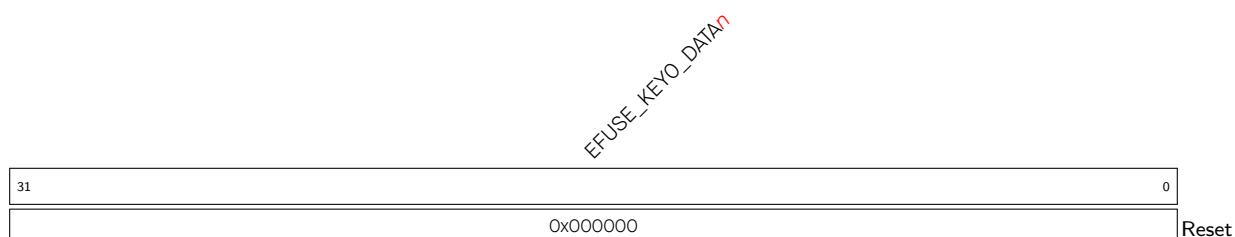
**EFUSE\_SYS\_DATA\_PART0\_2** Represents the second 32 bits of the zeroth part of system data. (RO)

Register 7.15. EFUSE\_RD\_SYS\_PART1\_DATA<sub>*n*</sub>\_REG (*n*: 0-7) (0x005C+0x4\**n*)

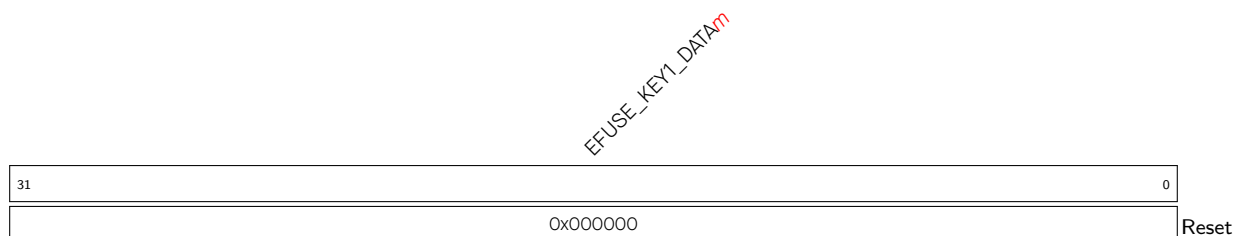
**EFUSE\_SYS\_DATA\_PART1\_*n*** Represents the *n*th 32 bits of the first part of system data. (RO)

Register 7.16. EFUSE\_RD\_USR\_DATA $m$ \_REG ( $m$ : 0-7) (0x007C+0x4\* $m$ )

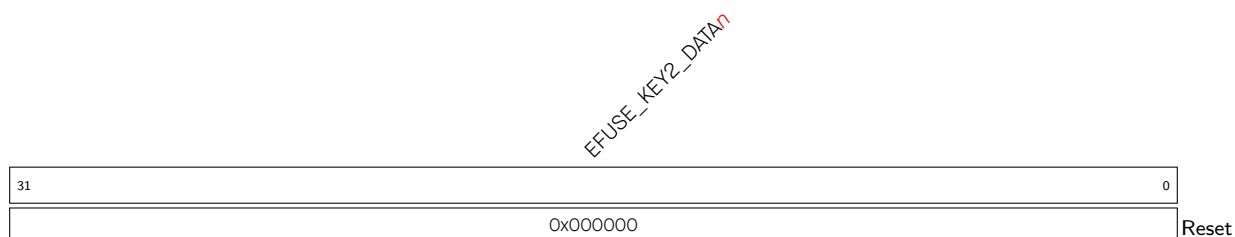
EFUSE\_USR\_DATA $m$  Represents the  $m$ th 32 bits of BLOCK3 (user). (RO)

Register 7.17. EFUSE\_RD\_KEY0\_DATA $n$ \_REG ( $n$ : 0-7) (0x009C+0x4\* $n$ )

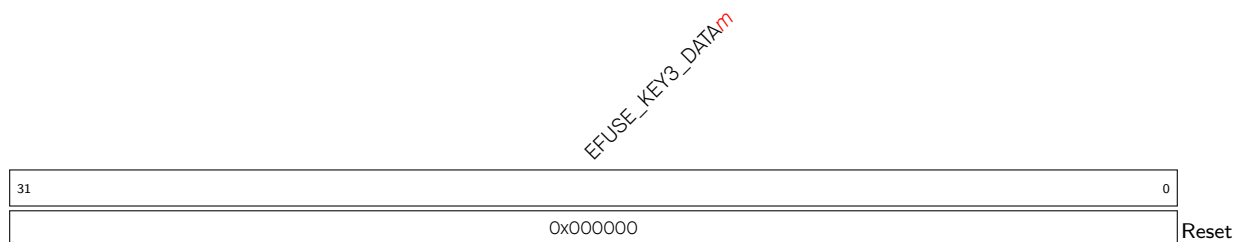
EFUSE\_KEY0\_DATA $n$  Represents the  $n$ th 32 bits of KEY0. (RO)

Register 7.18. EFUSE\_RD\_KEY1\_DATA $m$ \_REG ( $m$ : 0-7) (0x00BC+0x4\* $m$ )

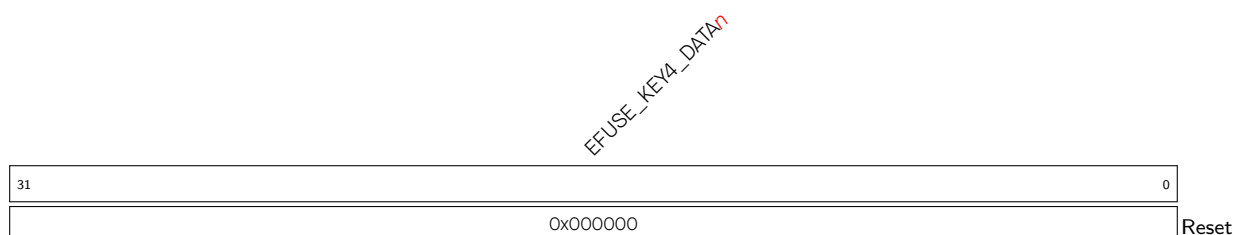
EFUSE\_KEY1\_DATA $m$  Represents the  $m$ th 32 bits of KEY1. (RO)

Register 7.19. EFUSE\_RD\_KEY2\_DATA $n$ \_REG ( $n$ : 0-7) (0x00DC+0x4\* $n$ )

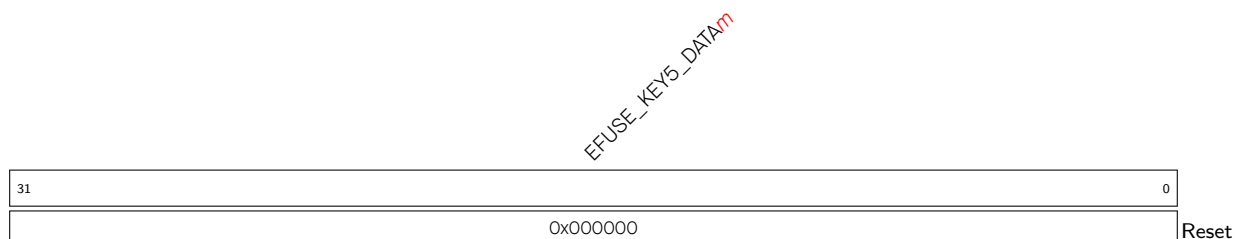
EFUSE\_KEY2\_DATA $n$  Represents the  $n$ th 32 bits of KEY2. (RO)

Register 7.20. EFUSE\_RD\_KEY3\_DATA $m$ \_REG ( $m$ : 0-7) (0x00FC+0x4\* $m$ )

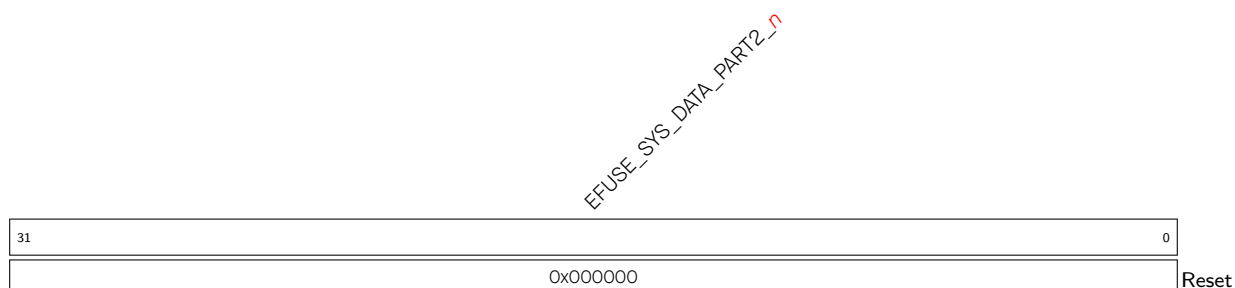
EFUSE\_KEY3\_DATA $m$  Represents the  $m$ th 32 bits of KEY3. (RO)

Register 7.21. EFUSE\_RD\_KEY4\_DATA $n$ \_REG ( $n$ : 0-7) (0x011C+0x4\* $n$ )

EFUSE\_KEY4\_DATA $n$  Represents the  $n$ th 32 bits of KEY4. (RO)

Register 7.22. EFUSE\_RD\_KEY5\_DATA $m$ \_REG ( $m$ : 0-7) (0x013C+0x4\* $m$ )

EFUSE\_KEY5\_DATA $m$  Represents the  $m$ th 32 bits of KEY5. (RO)

Register 7.23. EFUSE\_RD\_SYS\_PART2\_DATA $n$ \_REG ( $n$ : 0-7) (0x015C+0x4\* $n$ )

EFUSE\_SYS\_DATA\_PART2\_ $n$  Represents the  $n$ th 32 bits of the 2nd part of system data. (RO)

Register 7.24. EFUSE\_RD\_REPEAT\_ERR0\_REG (0x017C)

|            |  |  |  |                       |    |    |    |            |   |   |   |                                       |    |    |    |                        |   |   |   |                         |    |    |    |                           |    |    |   |                    |     |   |  |                                 |  |       |   |            |  |  |  |                          |  |  |  |                        |  |  |  |                                    |  |  |  |                                     |  |  |  |                  |  |  |  |
|------------|--|--|--|-----------------------|----|----|----|------------|---|---|---|---------------------------------------|----|----|----|------------------------|---|---|---|-------------------------|----|----|----|---------------------------|----|----|---|--------------------|-----|---|--|---------------------------------|--|-------|---|------------|--|--|--|--------------------------|--|--|--|------------------------|--|--|--|------------------------------------|--|--|--|-------------------------------------|--|--|--|------------------|--|--|--|
| (reserved) |  |  |  | EFUSE_USB_PHY_SEL_ERR |    |    |    | (reserved) |   |   |   | EFUSE_DIS_DOWNLOAD_MANUAL_ENCRYPT_ERR |    |    |    | EFUSE_DIS_PAD_JTAG_ERR |   |   |   | EFUSE_SOFT_DIS_JTAG_ERR |    |    |    | EFUSE_JTAG_SEL_ENABLE_ERR |    |    |   | EFUSE_DIS_TWAI_ERR |     |   |  | EFUSE_SPI_DOWNLOAD_MSPI_DIS_ERR |  |       |   | (reserved) |  |  |  | EFUSE_POWERGLITCH_EN_ERR |  |  |  | EFUSE_DIS_USB_JTAG_ERR |  |  |  | EFUSE_DIS_USB_OTG11_EXCHG_PINS_ERR |  |  |  | EFUSE_DIS_USB_DEVICE_EXCHG_PINS_ERR |  |  |  | EFUSE_RD_DIS_ERR |  |  |  |
| 31         |  |  |  |                       | 26 | 25 | 24 |            |   |   |   | 21                                    | 20 | 19 | 18 |                        |   |   |   | 16                      | 15 | 14 | 13 | 12                        | 11 | 10 | 9 | 8                  | 7   | 6 |  |                                 |  |       | 0 |            |  |  |  |                          |  |  |  |                        |  |  |  |                                    |  |  |  |                                     |  |  |  |                  |  |  |  |
| 0x0        |  |  |  |                       | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0x0                                   |    |    |    | 0                      | 0 | 0 | 0 | 0                       | 0  | 0  | 0  | 0                         | 0  | 0  | 0 | 0                  | 0x0 |   |  |                                 |  | Reset |   |            |  |  |  |                          |  |  |  |                        |  |  |  |                                    |  |  |  |                                     |  |  |  |                  |  |  |  |

**EFUSE\_RD\_DIS\_ERR** Any bit of this field being 1 represents a programming error of RD\_DIS. (RO)

**EFUSE\_DIS\_USB\_DEVICE\_EXCHG\_PINS\_ERR** This bit being 1 represents a programming error of DIS\_USB\_DEVICE\_EXCHG\_PINS. (RO)

**EFUSE\_DIS\_USB\_OTG11\_EXCHG\_PINS\_ERR** This bit being 1 represents a programming error of DIS\_USB\_OTG11\_EXCHG\_PINS. (RO)

**EFUSE\_DIS\_USB\_JTAG\_ERR** This bit being 1 represents a programming error of DIS\_USB\_JTAG. (RO)

**EFUSE\_POWERGLITCH\_EN\_ERR** This bit being 1 represents a programming error of POWER-GLITCH\_EN. (RO)

**EFUSE\_DIS\_FORCE\_DOWNLOAD\_ERR** This bit being 1 represents a programming error of DIS\_FORCE\_DOWNLOAD. (RO)

**EFUSE\_SPI\_DOWNLOAD\_MSPI\_DIS\_ERR** This bit being 1 represents a programming error of SPI\_DOWNLOAD\_MSPI\_DIS. (RO)

**EFUSE\_DIS\_TWAI\_ERR** This bit being 1 represents a programming error of DIS\_TWAI. (RO)

**EFUSE\_JTAG\_SEL\_ENABLE\_ERR** This bit being 1 represents a programming error of JTAG\_SEL\_ENABLE. (RO)

**EFUSE\_SOFT\_DIS\_JTAG\_ERR** Any bit of this field being 1 represents a programming error of SOFT\_DIS\_JTAG. (RO)

**EFUSE\_DIS\_PAD\_JTAG\_ERR** This bit being 1 represents a programming error of DIS\_PAD\_JTAG. (RO)

**EFUSE\_DIS\_DOWNLOAD\_MANUAL\_ENCRYPT\_ERR** This bit being 1 represents a programming error of DIS\_DOWNLOAD\_MANUAL\_ENCRYPT. (RO)

**EFUSE\_USB\_PHY\_SEL\_ERR** This bit being 1 represents a programming error of USB\_PHY\_SEL. (RO)

### Register 7.25. EFUSE\_RD\_REPEAT\_ERR1\_REG (0x0180)

|     |    |     |    |    |    |    |     |     |    |    |     |    |    |   |
|-----|----|-----|----|----|----|----|-----|-----|----|----|-----|----|----|---|
| 31  | 28 | 27  | 24 | 23 | 22 | 21 | 20  | 18  | 17 | 16 | 15  | 14 | 13 | 0 |
| 0x0 |    | 0x0 |    | 0  | 0  | 0  | 0x0 | 0x0 | 0  | 0  | 0x0 |    |    |   |

EFUSE\_KEY\_PURPOSE\_1\_ERR

EFUSE\_KEY\_PURPOSE\_0\_ERR

EFUSE\_SECURE\_BOOT\_KEY\_REVOKE2\_ERR

EFUSE\_SECURE\_BOOT\_KEY\_REVOKE1\_ERR

EFUSE\_SECURE\_BOOT\_KEY\_REVOKE0\_ERR

EFUSE\_SPI\_BOOT\_CRYPT\_CNT\_ERR

EFUSE\_WDT\_DELAY\_SEL\_ERR

(reserved)

EFUSE\_XTS\_KEY\_LENGTH\_256\_ERR

(reserved)

Reset

**EFUSE\_XTS\_KEY\_LENGTH\_256\_ERR** This bit being 1 represents a programming error of XTS\_KEY\_LENGTH\_256. (RO)

**EFUSE\_WDT\_DELAY\_SEL\_ERR** Any bit of this field being 1 represents a programming error of WDT\_DELAY\_SEL. (RO)

**EFUSE\_SPI\_BOOT\_CRYPT\_CNT\_ERR** Any bit of this field being 1 represents a programming error of SPI\_BOOT\_CRYPT\_CNT. (RO)

**EFUSE\_SECURE\_BOOT\_KEY\_REVOKEO\_ERR** This bit being 1 represents a programming error of SECURE\_BOOT\_KEY\_REVOKEO. (RO)

|  |  |
|--|--|
| <b>EFUSE_SECURE_BOOT_KEY_REVOKE1_ERR</b> | This bit being 1 represents a programming error of SECURE_BOOT_KEY_REVOKE1. (RO) |
|--|--|

**EFUSE\_SECURE\_BOOT\_KEY\_REVOKE2\_ERR** This bit being 1 represents a programming error of SECURE\_BOOT\_KEY\_REVOKE2. (RO)

**EFUSE\_KEY\_PURPOSE\_0\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_0. (RO)

**EFUSE\_KEY\_PURPOSE\_1\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_1. (RO)

**Register 7.26. EFUSE\_RD\_REPEAT\_ERR2\_REG (0x0184)**

|                      |  |  |  |    |  |   |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |                                     |  |    |  |     |  |     |  |    |  |     |  |  |  |     |  |  |  |     |  |   |  |                        |  |   |  |       |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------------------|--|--|--|----|--|---|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|-------------------------------------|--|----|--|-----|--|-----|--|----|--|-----|--|--|--|-----|--|--|--|-----|--|---|--|------------------------|--|---|--|-------|--|--|--|---|--|---|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| EFUSE_FLASH_TPUW_ERR |  |  |  |    |  |   |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  | EFUSE_DIS_USB_OTG_DOWNLOAD_MODE_ERR |  |    |  |     |  |     |  |    |  |     |  |  |  |     |  |  |  |     |  |   |  | EFUSE_FLASH_ECC_EN_ERR |  |   |  |       |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  | EFUSE_FLASH_PAGE_SIZE_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_FLASH_TYPE_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_BOOT_SIZE_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SECURE_BOOT_EN_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_CRYPT_DPA_ENABLE_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SEC_DPA_LEVEL_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_5_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_4_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_3_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_KEY_PURPOSE_2_ERR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                   |  |  |  | 28 |  |   |  | 27 |  | 26 |  | 25 |  | 24 |  | 23 |  | 22 |  | 21 |  | 20                                  |  | 19 |  | 18  |  | 17  |  | 16 |  | 15  |  |  |  | 12  |  |  |  | 11  |  | 8 |  |                        |  | 7 |  | 4     |  |  |  | 3 |  | 0 |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x0                  |  |  |  | 0  |  | 0 |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0                                   |  | 0  |  | 0x0 |  | 0x0 |  |    |  | 0x0 |  |  |  | 0x0 |  |  |  | 0x0 |  |   |  | 0x0                    |  |   |  | Reset |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**EFUSE\_KEY\_PURPOSE\_2\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_2. (RO)

**EFUSE\_KEY\_PURPOSE\_3\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_3. (RO)

**EFUSE\_KEY\_PURPOSE\_4\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_4. (RO)

**EFUSE\_KEY\_PURPOSE\_5\_ERR** Any bit of this field being 1 represents a programming error of KEY\_PURPOSE\_5. (RO)

**EFUSE\_SEC\_DPA\_LEVEL\_ERR** Any bit of this field being 1 represents a programming error of SEC\_DPA\_LEVEL. (RO)

**EFUSE\_CRYPT\_DPA\_ENABLE\_ERR** This bit being 1 represents a programming error of CRYPT\_DPA\_ENABLE. (RO)

**EFUSE\_SECURE\_BOOT\_EN\_ERR** This bit being 1 represents a programming error of SECURE\_BOOT\_EN. (RO)

**EFUSE\_SECURE\_BOOT\_AGGRESSIVE\_REVOKE\_ERR** This bit being 1 represents a programming error of SECURE\_BOOT\_AGGRESSIVE\_REVOKE. (RO)

**EFUSE\_FLASH\_TYPE\_ERR** This bit being 1 represents a programming error of FLASH\_TYPE. (RO)

**EFUSE\_FLASH\_PAGE\_SIZE\_ERR** This bit being 1 represents a programming error of FLASH\_PAGE\_SIZE. (RO)

**EFUSE\_FLASH\_ECC\_EN\_ERR** This bit being 1 represents a programming error of FLASH\_ECC\_EN. (RO)

**EFUSE\_DIS\_USB\_OTG\_DOWNLOAD\_MODE\_ERR** This bit being 1 represents a programming error of DIS\_USB\_OTG\_DOWNLOAD\_MODE. (RO)

**EFUSE\_FLASH\_TPUW\_ERR** This bit being 1 represents a programming error of FLASH\_TPUW. (RO)

### Register 7.27. EFUSE\_RD\_REPEAT\_ERR3\_REG (0x0188)

|     |    |    |    |      |   |   |     |   |   |   |   |   |   |   |
|-----|----|----|----|------|---|---|-----|---|---|---|---|---|---|---|
| 31  | 27 | 26 | 25 | 24   | 9 | 8 | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0x0 |    | 0  | 0  | 0x00 |   | 0 | 0x0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

EFUSE\_DDC\_VSET\_ERR

EFUSE\_HVS\_EN\_PAD\_ERR

EFUSE\_SECURE\_BOOT\_DISABLE\_FAST\_WAKE\_ERR

EFUSE\_SECURE\_VERSION\_ERR

EFUSE\_FORCE\_SEND\_RESUME\_ERR

EFUSE\_UART\_PRINT\_CONTROL\_ERR

EFUSE\_ENABLE\_SECURITY\_DOWNLOAD\_ERR

EFUSE\_DIS\_USB\_SERIAL\_JTAG\_DOWNLOAD\_MODE\_ERR

EFUSE\_DIS\_DIRECT\_BOOT\_ERR

EFUSE\_DIS\_DOWNLOAD\_MODE\_ERR

Reset

**EFUSE\_DIS\_DOWNLOAD\_MODE\_ERR** This bit being 1 represents a programming error of DIS\_DOWNLOAD\_MODE. (RO)

**EFUSE\_DIS\_DIRECT\_BOOT\_ERR** This bit being 1 represents a programming error of DIS\_DIRECT\_BOOT. (RO)

**EFUSE\_DIS\_USB\_SERIAL\_JTAG\_ROM\_PRINT\_ERR** This bit being 1 represents a programming error of DIS\_USB\_SERIAL\_JTAG\_ROM\_PRINT\_ERR. (RO)

**EFUSE\_DIS\_USB\_SERIAL\_JTAG\_DOWNLOAD\_MODE\_ERR** This bit being 1 represents a programming error of DIS\_USB\_SERIAL\_JTAG\_DOWNLOAD\_MODE. (RO)

**EFUSE\_ENABLE\_SECURITY\_DOWNLOAD\_ERR** This bit being 1 represents a programming error of ENABLE\_SECURITY\_DOWNLOAD. (RO)

|                                     |  |
|-------------------------------------|--|
| <b>EFUSE_UART_PRINT_CONTROL_ERR</b> | Any bit of this field being 1 represents a programming error of UART_PRINT_CONTROL. (RO) |
|-------------------------------------|--|

**EFUSE\_FORCE\_SEND\_RESUME\_ERR** This bit being 1 represents a programming error of FORCE\_SEND\_RESUME. (RO)

**EFUSE\_SECURE\_VERSION\_ERR** Any bit of this field being 1 represents a programming error of SECURE VERSION. (RO)

|  |  |
|--|--|
| <b>EFUSE_SECURE_BOOT_DISABLE_FAST_WAKE_ERR</b> | This bit being 1 represents a programming error of SECURE_BOOT_DISABLE_FAST_WAKE. (RO) |
|--|--|

**EFUSE\_HYS\_EN\_PAD\_ERR** This bit being 1 represents a programming error of HYS\_EN\_PAD. (RO)

**EFUSE\_DCDC\_VSET\_ERR** Any bit of this field being 1 represents a programming error of DCDC\_VSET.  
(RO)

**Register 7.28. EFUSE\_RD\_REPEAT\_ERR4\_REG (0x018C)**

|            |   |   |   |   |   |   |   |   |   |                   |    |    |    |                   |    |    |    |                        |    |    |    |                          |   |   |   |            |   |   |   |                           |   |   |   |                            |   |   |   |            |   |   |   |                           |   |   |   |                           |   |   |   |                           |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   | EFUSE_DIS_SWD_ERR |    |    |    | EFUSE_DIS_WDT_ERR |    |    |    | EFUSE_DCDC_VSET_EN_ERR |    |    |    | EFUSE_HP_PWR_SRC_SEL_ERR |   |   |   | (reserved) |   |   |   | EFUSE_USB_OTG11_DREFL_ERR |   |   |   | EFUSE_USB_DEVICE_DREFL_ERR |   |   |   | (reserved) |   |   |   | EFUSE_OPXA_TIEH_SEL_3_ERR |   |   |   | EFUSE_OPXA_TIEH_SEL_2_ERR |   |   |   | EFUSE_OPXA_TIEH_SEL_1_ERR |   |   |   | EFUSE_OPXA_TIEH_SEL_0_ERR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |                   | 22 | 21 | 20 | 19                | 18 | 17 | 16 | 15                     | 14 | 13 | 12 | 11                       |   |   |   |            | 8 | 7 | 6 | 5                         | 4 | 3 | 2 | 1                          | 0 |   |   |            |   |   |   |                           |   |   |   |                           |   |   |   |                           |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                 | 0  | 0  | 0  | 0                 | 0  | 0  | 0  | 0                      | 0  | 0  | 0  | 0                        | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**EFUSE\_OPXA\_TIEH\_SEL\_0\_ERR** Any bit of this field being 1 represents a programming error of OPXA\_TIEH\_SEL\_0. (RO)

**EFUSE\_OPXA\_TIEH\_SEL\_1\_ERR** Any bit of this field being 1 represents a programming error of OPXA\_TIEH\_SEL\_1. (RO)

**EFUSE\_OPXA\_TIEH\_SEL\_2\_ERR** Any bit of this field being 1 represents a programming error of OPXA\_TIEH\_SEL\_2. (RO)

**EFUSE\_OPXA\_TIEH\_SEL\_3\_ERR** Any bit of this field being 1 represents a programming error of OPXA\_TIEH\_SEL\_3. (RO)

**EFUSE\_USB\_DEVICE\_DREFL\_ERR** Any bit of this field being 1 represents a programming error of USB\_DEVICE\_DREFL. (RO)

**EFUSE\_USB\_OTG11\_DREFL\_ERR** Any bit of this field being 1 represents a programming error of USB\_OTG11\_DREFL. (RO)

**EFUSE\_HP\_PWR\_SRC\_SEL\_ERR** This bit being 1 represents a programming error of HP\_PWR\_SRC\_SEL. (RO)

**EFUSE\_DCDC\_VSET\_EN\_ERR** This bit being 1 represents a programming error of DCDC\_VSET\_EN. (RO)

**EFUSE\_DIS\_WDT\_ERR** This bit being 1 represents a programming error of DIS\_WDT. (RO)

**EFUSE\_DIS\_SWD\_ERR** This bit being 1 represents a programming error of DIS\_SWD. (RO)



**Register 7.29. EFUSE\_RD\_RS\_ERR0\_REG (0x01C0)**

|                 |     |                    |     |                 |     |                    |     |                 |     |                    |     |                 |     |                    |     |                 |     |                    |     |                     |     |                        |     |                      |  |                         |  |                    |  |                       |  |
|-----------------|-----|--------------------|-----|-----------------|-----|--------------------|-----|-----------------|-----|--------------------|-----|-----------------|-----|--------------------|-----|-----------------|-----|--------------------|-----|---------------------|-----|------------------------|-----|----------------------|--|-------------------------|--|--------------------|--|-----------------------|--|
| EFUSE_KEY4_FAIL |     | EFUSE_KEY4_ERR_NUM |     | EFUSE_KEY3_FAIL |     | EFUSE_KEY3_ERR_NUM |     | EFUSE_KEY2_FAIL |     | EFUSE_KEY2_ERR_NUM |     | EFUSE_KEY1_FAIL |     | EFUSE_KEY1_ERR_NUM |     | EFUSE_KEY0_FAIL |     | EFUSE_KEY0_ERR_NUM |     | EFUSE_USR_DATA_FAIL |     | EFUSE_USR_DATA_ERR_NUM |     | EFUSE_SYS_PART1_FAIL |  | EFUSE_SYS_PART1_ERR_NUM |  | EFUSE_MAC_SYS_FAIL |  | EFUSE_MAC_SYS_ERR_NUM |  |
| 31              | 30  | 28                 | 27  | 26              | 24  | 23                 | 22  | 20              | 19  | 18                 | 16  | 15              | 14  | 12                 | 11  | 10              | 8   | 7                  | 6   | 4                   | 3   | 2                      | 0   | Reset                |  |                         |  |                    |  |                       |  |
| 0               | 0x0 | 0                  | 0x0 | 0               | 0x0 | 0                  | 0x0 | 0               | 0x0 | 0                  | 0x0 | 0               | 0x0 | 0                  | 0x0 | 0               | 0x0 | 0                  | 0x0 | 0                   | 0x0 | 0                      | 0x0 |                      |  |                         |  |                    |  |                       |  |

**EFUSE\_MAC\_SYS\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_MAC\_SYS\_FAIL** Represents whether programming MAC\_SYS failed.

0: No failure and the data of MAC\_SYS is reliable.

1: Programming user data failed and the number of error bytes is over 6.

(RO)

**EFUSE\_SYS\_PART1\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_SYS\_PART1\_FAIL** Represents whether programming system part1 data failed.

0: No failure and the data of system part1 is reliable.

1: Programming user data failed and the number of error bytes is over 6.

(RO)

**EFUSE\_USR\_DATA\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_USR\_DATA\_FAIL** Represents whether programming user data failed.

0: No failure and the user data is reliable.

1: Programming user data failed and the number of error bytes is over 6.

(RO)

**EFUSE\_KEY0\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_KEY0\_FAIL** Represents whether programming key0 data failed.

0: No failure and the data of key0 is reliable.

1: Programming key0 failed and the number of error bytes is over 6.

(RO)

**EFUSE\_KEY1\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_KEY1\_FAIL** Represents whether programming key1 data failed.

0: No failure and the data of key1 is reliable.

1: Programming key1 failed and the number of error bytes is over 6.

(RO)

**EFUSE\_KEY2\_ERR\_NUM** Represents the number of error bytes. (RO)

**EFUSE\_KEY2\_FAIL** Represents whether programming key2 data failed.

0: No failure and the data of key2 is reliable.

1: Programming key2 failed and the number of error bytes is over 6.

(RO)

Continued on the next page...

**Register 7.29. EFUSE\_RD\_RS\_ERR0\_REG (0x01C0)**

Continued from the previous page...

**EFUSE\_KEY3\_ERR\_NUM** Represents the number of error bytes. (RO)**EFUSE\_KEY3\_FAIL** Represents whether programming key3 data failed.

0: No failure and the data of key3 is reliable.

1: Programming key3 failed and the number of error bytes is over 6.

(RO)

**EFUSE\_KEY4\_ERR\_NUM** Represents the number of error bytes. (RO)**EFUSE\_KEY4\_FAIL** Represents whether programming key4 data failed.

0: No failure and the data of key4 is reliable.

1: Programming key4 failed and the number of error bytes is over 6.

(RO)

**Register 7.30. EFUSE\_RD\_RS\_ERR1\_REG (0x01C4)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |     |   |   |                         |   |     |   |                 |   |       |  |                    |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|-----|---|---|-------------------------|---|-----|---|-----------------|---|-------|--|--------------------|--|--|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_SYS_PART2_FAIL |     |   |   | EFUSE_SYS_PART2_ERR_NUM |   |     |   | EFUSE_KEY5_FAIL |   |       |  | EFUSE_KEY5_ERR_NUM |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                    | 7   | 6 | 4 |                         |   |     | 3 | 2               | 0 |       |  |                    |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    | 0x0 |   |   |                         | 0 | 0x0 |   |                 |   | Reset |  |                    |  |  |  |

Reset

**EFUSE\_KEY5\_ERR\_NUM** Represents the number of error bytes. (RO)**EFUSE\_KEY5\_FAIL** Represents whether programming key5 data failed.

0: No failure and the data of key5 is reliable.

1: Programming key5 failed and the number of error bytes is over 6.

(RO)

**EFUSE\_SYS\_PART2\_ERR\_NUM** Represents the number of error bytes. (RO)**EFUSE\_SYS\_PART2\_FAIL** Represents whether programming system part2 data failed.

0: No failure and the data of system part2 is reliable.

1: Programming user data failed and the number of error bytes is over 6.

(RO)

### Register 7.31. EFUSE\_CLK\_REG (0x01C8)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |                                 |  |  |                    |  |  |  |                    |  |  |  |  |  |  |  |  |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|---------------------------------|--|--|--------------------|--|--|--|--------------------|--|--|--|--|--|--|--|--|---|---|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_CLK_EN                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_MEM_FORCE_PU |                                 |  |  | EFUSE_MEM_FORCE_ON |  |  |  | EFUSE_MEM_FORCE_PD |  |  |  |  |  |  |  |  |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16         | 15                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    | 3                               |  |  |                    |  |  |  |                    |  |  |  |  |  |  |  |  | 2 | 1 | 0 |   |       |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |                    |  |  |  |                    |  |  |  |  |  |  |  |  | 0 | 0 | 0 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |

**EFUSE\_MEM\_FORCE\_PD** Configures whether to force power down eFuse SRAM.

1: Force

0: No effect

(R/W)

**EFUSE\_MEM\_CLK\_FORCE\_ON** Configures whether to force activate clock signal of eFuse SRAM.

1: Force activate

0: No effect

(R/W)

**EFUSE\_MEM\_FORCE\_PU** Configures whether to force power up eFuse SRAM.

1: Force

0: No effect

(R/W)

**EFUSE\_CLK\_EN** Configures whether to force enable eFuse register configuration clock signal.

1: Force

0: The clock is enabled only during the reading and writing of registers

(R/W)

### Register 7.32. EFUSE\_CONF\_REG (0x01CC)

|                         |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |                    |  |  |  |               |  |  |  |    |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
|-------------------------|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--------------------|--|--|--|---------------|--|--|--|----|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|
| (reserved)              |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  | EFUSE_CFG_EDSA_BLK |  |  |  | EFUSE_OP_CODE |  |  |  |    |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
| 31                      |  |  |  |  |  |  |  |  |  |  |  | 20  |  |  |  | 19                 |  |  |  | 16            |  |  |  | 15 |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |
| 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  | 0x0 |  |  |  | 0x00               |  |  |  |               |  |  |  |    |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |

**EFUSE\_OP\_CODE** Configures operation command type.

0x5A5A: Program operation command

0x5AA5: Read operation command

Other values: No effect

(R/W)

**EFUSE\_CFG\_ECDSA\_BLK** Configures which block to use for ECDSA key output. (R/W)

**Register 7.33. EFUSE\_DAC\_CONF\_REG (0x01E8)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              |    |    |    |     |  |  |  |               |  |  |  |   |   |   |    |                       |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------|----|----|----|-----|--|--|--|---------------|--|--|--|---|---|---|----|-----------------------|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_OE_CLR |    |    |    |     |  |  |  | EFUSE_DAC_NUM |  |  |  |   |   |   |    | EFUSE_DAC_CLK_PAD_SEL |  |  |  |  |  |  |  | EFUSE_DAC_CLK_DIV |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              | 18 | 17 | 16 |     |  |  |  |               |  |  |  | 9 | 8 | 7 |    |                       |  |  |  |  |  |  |  |                   |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 0  | 0  | 0  | 255 |  |  |  |               |  |  |  | 0 | 0 | 7 | 23 |                       |  |  |  |  |  |  |  |                   |  |  |  |  |  |  | Reset |

**EFUSE\_DAC\_CLK\_DIV** Configures the division factor of the rising clock of the programming voltage.  
(R/W)

**EFUSE\_DAC\_CLK\_PAD\_SEL** Don't care. (R/W)

**EFUSE\_DAC\_NUM** Configures clock cycles for programming voltage to rise. Measurement unit: a clock cycle divided by [EFUSE\\_DAC\\_CLK\\_DIV](#). (R/W)

**EFUSE\_OE\_CLR** Configures whether to reduce the power supply of the programming voltage.  
0: Not reduce.  
1: Reduce.  
(R/W)

**Register 7.34. EFUSE\_RD\_TIM\_CONF\_REG (0x01EC)**

|                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |    |    |  |  |  |  |  |           |  |  |  |  |  |  |  |             |  |  |    |    |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |   |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |   |
|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|----|----|--|--|--|--|--|-----------|--|--|--|--|--|--|--|-------------|--|--|----|----|--|--|--|--|--|--|--|--|--|--|--|-----|--|--|--|--|---|---|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|---|
| EFUSE_READ_INIT_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | EFUSE_TSR_A |    |    |  |  |  |  |  | EFUSE_TRD |  |  |  |  |  |  |  | EFUSE_THR_A |  |  |    |    |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  |   |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |   |
| 31                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             | 24 | 23 |  |  |  |  |  |           |  |  |  |  |  |  |  |             |  |  | 16 | 15 |  |  |  |  |  |  |  |  |  |  |  |     |  |  |  |  | 8 | 7 |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  | 0 |
| 0xf                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x1         |    |    |  |  |  |  |  |           |  |  |  |  |  |  |  | 0x2         |  |  |    |    |  |  |  |  |  |  |  |  |  |  |  | 0x1 |  |  |  |  |   |   |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |   |

**EFUSE\_THR\_A** Configures the read hold time. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_TRD** Configures the read time. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_TSR\_A** Configures the read setup time. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_READ\_INIT\_NUM** Configures the waiting time of reading eFuse memory. Measurement unit: One cycle of the eFuse core clock. (R/W)

**Register 7.35. EFUSE\_WR\_TIM\_CONF1\_REG (0x01F0)**

|             |  |  |  |  |  |  |  |        |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |              |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|-------------|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| EFUSE_THP_A |  |  |  |  |  |  |  |        |  |  |  |  |  |  |  | EFUSE_PWR_ON_NUM |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | EFUSE_TSUP_A |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31          |  |  |  |  |  |  |  | 24     |  |  |  |  |  |  |  | 23               |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7            |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |
| 0x1         |  |  |  |  |  |  |  | 0x2667 |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | 0x1          |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**EFUSE\_TSUP\_A** Configures the programming setup time. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_PWR\_ON\_NUM** Configures the power up time for VDDQ. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_THP\_A** Configures the programming hold time. Measurement unit: One cycle of the eFuse core clock. (R/W)

**Register 7.36. EFUSE\_WR\_TIM\_CONF2\_REG (0x01F4)**

|                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                           |  |  |  |  |  |  |  |    |
|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|---------------------------|--|--|--|--|--|--|--|----|
| <i>EFUSE__TPGM</i> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | <i>EFUSE__PWR_OFF_NUM</i> |  |  |  |  |  |  |  |    |
| 31                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16 |                           |  |  |  |  |  |  |  | 15 |
| 0xa0               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | 0x140                     |  |  |  |  |  |  |  |    |
| Reset              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                           |  |  |  |  |  |  |  |    |

**EFUSE\_PWR\_OFF\_NUM** Configures the power outage time for VDDQ. Measurement unit: One cycle of the eFuse core clock. (R/W)

**EFUSE\_TPGM** Configures the active programming time. Measurement unit: One cycle of the eFuse core clock. (R/W)

### Register 7.37. EFUSE\_WR\_TIM\_CONFO\_RS\_BYPASS\_REG (0x01F8)

|                         |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |              |  |  |  |                         |  |  |  |  |  |  |  |    |  |  |  |                            |  |  |  |       |  |  |  |    |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |
|-------------------------|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|--------------|--|--|--|-------------------------|--|--|--|--|--|--|--|----|--|--|--|----------------------------|--|--|--|-------|--|--|--|----|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|
| (reserved)              |  |  |  |  |  |  |  |  |  |  |  | EFUSE_TPGM_INACTIVE |  |  |  |  |  |  |  |  |  |  |  | EFUSE_UPDATE |  |  |  | EFUSE_BYPASS_RS_BLK_NUM |  |  |  |  |  |  |  |    |  |  |  | EFUSE_BYPASS_RS_CORRECTION |  |  |  |       |  |  |  |    |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |
| 31                      |  |  |  |  |  |  |  |  |  |  |  | 21                  |  |  |  |  |  |  |  |  |  |  |  | 20           |  |  |  |                         |  |  |  |  |  |  |  | 13 |  |  |  |                            |  |  |  |       |  |  |  | 12 |  |  |  | 11 |  |  |  |  |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  | 0x1                 |  |  |  |  |  |  |  |  |  |  |  | 0            |  |  |  | 0x0                     |  |  |  |  |  |  |  |    |  |  |  | 0                          |  |  |  | Reset |  |  |  |    |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |

|                                   |   |
|-----------------------------------|---|
| <b>EFUSE_BYPASS_RS_CORRECTION</b> | Configures whether to bypass the Reed-Solomon (RS) correction step. |
|-----------------------------------|---|

0: Not bypass

1: Bypass

(R/W)

|                                |  |
|--------------------------------|--|
| <b>EFUSE_BYPASS_RS_BLK_NUM</b> | Configures which block number to bypass the Reed-Solomon (RS) correction step. (R/W) |
|--------------------------------|--|

**EFUSE\_UPDATE** Configures whether to update multi-bit register signals.

1: Update

0: No effect

(WT)

**EFUSE\_TPGM\_INACTIVE** Configures the inactive programming time. Measurement unit: One cycle of the eFuse core clock. (R/W)

### Register 7.38. EFUSE\_STATUS\_REG (0x01D0)

|                 |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |     |  |  |                          |    |  |  |  |    |  |  |                 |    |  |            |  |   |  |  |     |   |  |             |       |   |  |  |  |   |  |  |  |
|-----------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|-----|--|--|--------------------------|----|--|--|--|----|--|--|-----------------|----|--|------------|--|---|--|--|-----|---|--|-------------|-------|---|--|--|--|---|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | EFUSE_CUR_ECDSA_BLK |  |  |  |  |  |  |  |     |  |  | EFUSE_BLK0_VALID_BIT_CNT |    |  |  |  |    |  |  |                 |    |  | (reserved) |  |   |  |  |     |   |  | EFUSE_STATE |       |   |  |  |  |   |  |  |  |
| 31              |  |  |  |  |  |  |  | 24                  |  |  |  |  |  |  |  | 23  |  |  |                          | 20 |  |  |  | 19 |  |  |                 | 10 |  |            |  | 9 |  |  |     | 4 |  |             |       | 3 |  |  |  | 0 |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0                 |  |  |  |  |  |  |  | 0x0 |  |  |                          |    |  |  |  |    |  |  | 0 0 0 0 0 0 0 0 |    |  |            |  |   |  |  | 0x0 |   |  |             | Reset |   |  |  |  |   |  |  |  |

**EFUSE\_STATE** Represents the state of the eFuse state machine.

0: Reset state, the initial state after power-up

1: Idle state

Other values: Non-idle state

(RO)

**EFUSE\_BLK0\_VALID\_BIT\_CNT** Represents the number of block valid bit. (RO)

**EFUSE\_CUR\_ECDSA\_BLK** Represents which block is used for ECDSA key output. (RO)

Register 7.39. EFUSE\_CMD\_REG (0x01D4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |     |               |   |                |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|-----|---------------|---|----------------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_BLK_NUM |     | EFUSE_PGM_CMD |   | EFUSE_READ_CMD |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5             | 2   | 1             | 0 |                |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0x0 | 0             | 0 | Reset          |  |

**EFUSE\_READ\_CMD** Configures whether to send read commands.

- 1: Send
  - 0: No effect
- (R/W/SC)

**EFUSE\_PGM\_CMD** Configures whether to send programming commands.

- 1: Send
  - 0: No effect
- (R/W/SC)

**EFUSE\_BLK\_NUM** Represents the serial number of the block to be programmed. Value 0-10 corresponds to block number 0-10, respectively. (R/W)

Register 7.40. EFUSE\_INT\_RAW\_REG (0x01D8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |                         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_PGM_DONE_INT_RAW |   | EFUSE_READ_DONE_INT_RAW |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2                      | 1 | 0                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EFUSE\_READ\_DONE\_INT\_RAW** The raw interrupt status of EFUSE\_READ\_DONE\_INT. (R/SS/WTC)

**EFUSE\_PGM\_DONE\_INT\_RAW** The raw interrupt status of EFUSE\_PGM\_DONE\_INT. (R/SS/WTC)

Register 7.41. EFUSE\_INT\_ST\_REG (0x01DC)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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-|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_PGM_DONE_INT_ST<br>EFUSE_READ_DONE_INT_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2   | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**EFUSE\_READ\_DONE\_INT\_ST** The masked interrupt status of EFUSE\_READ\_DONE\_INT. (RO)

**EFUSE\_PGM\_DONE\_INT\_ST** The masked interrupt status of EFUSE\_PGM\_DONE\_INT. (RO)

Register 7.42. EFUSE\_INT\_ENA\_REG (0x01E0)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_PGM_DONE_INT_ENA<br>EFUSE_READ_DONE_INT_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2   | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EFUSE\_READ\_DONE\_INT\_ENA** Write 1 to enable EFUSE\_READ\_DONE\_INT. (R/W)

**EFUSE\_PGM\_DONE\_INT\_ENA** Write 1 to enable EFUSE\_PGM\_DONE\_INT. (R/W)

Register 7.43. EFUSE\_INT\_CLR\_REG (0x01E4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | EFUSE_PGM_DONE_INT_CLR<br>EFUSE_READ_DONE_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2   | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**EFUSE\_READ\_DONE\_INT\_CLR** Write 1 to clear EFUSE\_READ\_DONE\_INT. (WT)

**EFUSE\_PGM\_DONE\_INT\_CLR** Write 1 to clear EFUSE\_PGM\_DONE\_INT. (WT)



Register 7.44. EFUSE\_DATE\_REG (0x01FC)

|            |   |    |    |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|---|----|----|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |   |    |    | EFUSE_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |   | 28 | 27 |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0  | 0  | 0x2305050  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

**EFUSE\_DATE** Version control register. (R/W)

## Part IV

# System Component

Encompassing a range of system-level functionalities, this part describes components related to system boot, clocks, GPIO, timers, watchdogs, debug assistance, event and interrupt handling, low-power management, and various system registers.

## Chapter 8

# GPIO Matrix and IO MUX

## 8.1 Overview

GPIO matrix is a hardware structure that allows dynamic remapping between the GPIO pins and peripheral input/output signals to provide greater flexibility. IO MUX (Input/output multiplexing) is a technology that allows the same pin to perform different functions at different times, allowing dynamic switching of pin functions through configuration. ESP32-P4 provides two groups of IO MUX and GPIO matrix:

- HP GPIO matrix and HP IO MUX
- LP GPIO matrix and LP IO MUX

The ESP32-P4 chip features 55 GPIO pins, including 16 low-power (LP) GPIO pins and 39 high-performance (HP) GPIO pins. Each pin can be used as a general-purpose I/O, or be connected to an internal peripheral signal.

- Through HP GPIO matrix and HP IO MUX, HP peripheral input signals can be from any GPIO pins, and HP peripheral output signals can be routed to any GPIO pins.
- Through LP GPIO matrix and LP IO MUX, LP peripheral input signals can be from any LP GPIO pins, and LP peripheral output signals can be routed to any LP GPIO pins.

Together these modules provide highly configurable I/O. The 55 GPIO pins are numbered from GPIO0 to GPIO54.

- LP GPIO pins (GPIO0 ~ GPIO15) can be used by either HP or LP peripherals.
- HP GPIO pins (GPIO16 ~ GPIO54) can be used only by HP peripherals.

The ESP32-P4 chip has dedicated pins for external flash and in-package PSRAM. Such pins can not be used for other purpose. See [ESP32-P4 Datasheet](#) > Section *Pin Mapping Between Chip and Flash/PSRAM*.

Unless otherwise specified, GPIO matrix refers to both LP GPIO matrix and HP GPIO matrix, so as to IO MUX.

## 8.2 Features

### 8.2.1 HP GPIO Matrix and HP IO MUX

HP GPIO matrix has the following features:

- A full-switching matrix between HP peripheral input/output signals and the GPIO pins
- 222 HP peripheral input signals sourced from the input of any GPIO pins
- 232 HP peripheral output signals routed to the output of any GPIO pins

- Signal synchronization for HP peripheral inputs based on **HP IO MUX operating clock**
- GPIO Filter hardware for input signal filtering
- Glitch Filter hardware for second-time filtering on input signal
- Sigma delta modulated (SDM) output
- GPIO simple input and output
- HP GPIO Wakeup

**HP IO MUX has the following features:**

- Control of 55 GPIOs (GPIO0 ~ GPIO54) for HP peripherals.
- A configuration register [IO\\_MUX\\_GPIO \$n\$ \\_REG](#) provided for each GPIO pin, to control the pin's input/output, pull-up/pull-down, drive strength, and function selection.
- Better high-frequency digital performance achieved by routing some digital signals (SPI, EMAC) directly from HP IO MUX to peripherals.

## 8.2.2 LP GPIO Matrix and LP IO MUX

**LP GPIO matrix has the following features:**

- A full-switching matrix between the LP peripheral input/output signals and the LP GPIO pins
- 14 LP peripheral input signals sourced from the input of any LP GPIO pins
- 14 LP peripheral output signals routed to the output of any LP GPIO pins
- GPIO Filter hardware for input signal filtering
- GPIO simple input and output
- LP GPIO Wakeup

**LP IO MUX has the following feature:**

- Control of 16 LP GPIO pins (GPIO0 ~ GPIO15) for LP peripherals.
- A configuration register [LP\\_IOMUX\\_PAD \$n\$ \\_REG](#) provided for each LP GPIO pin, to control the pin's input/output, pull-up/pull-down, drive strength, function selection, and IO MUX selection.

## 8.3 Architectural Overview

Figure [8.3-1](#) shows in details how HP GPIO matrix, HP IO MUX, LP GPIO matrix, and LP IO MUX route signals from pins to peripherals, and from peripherals to pins.

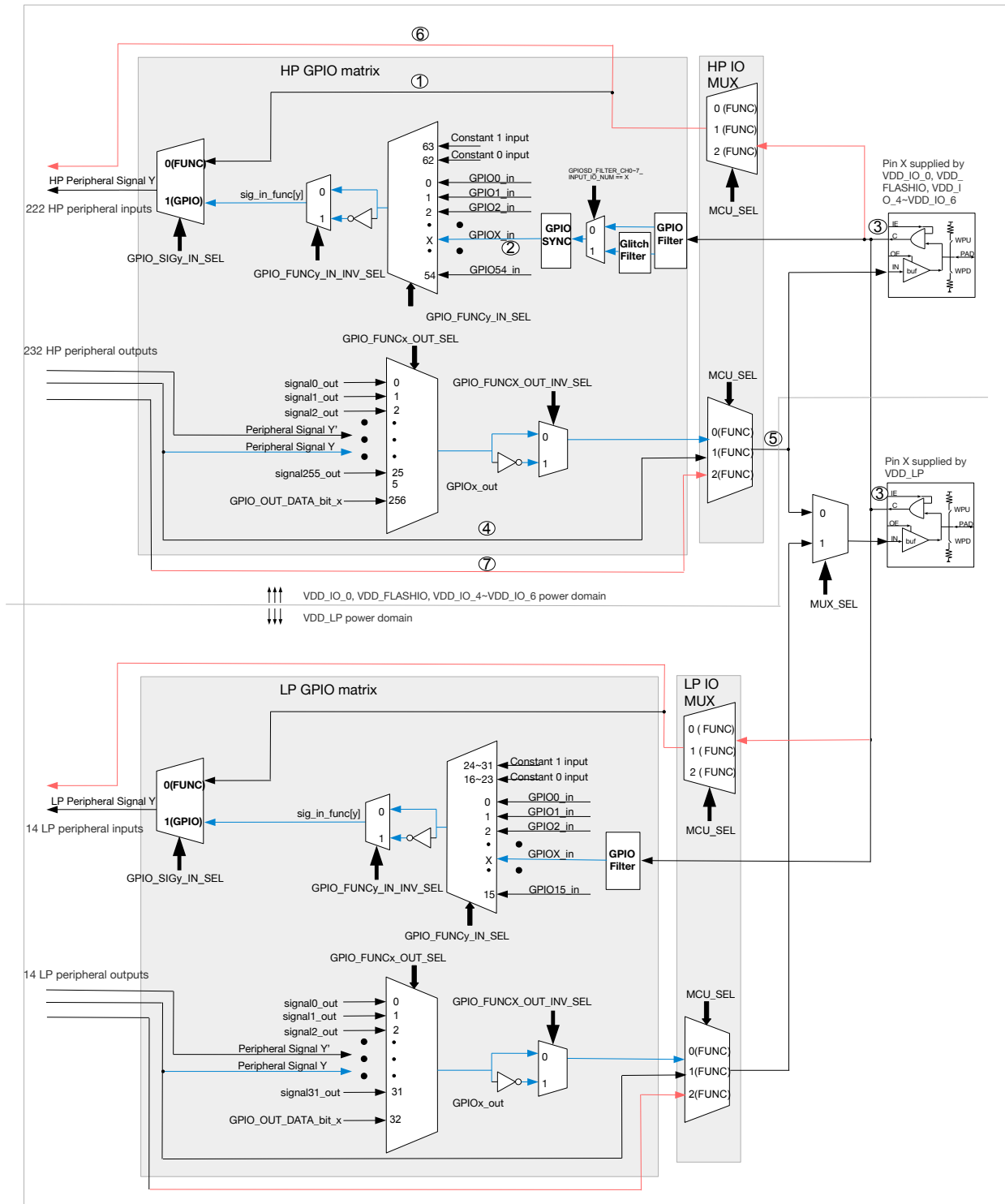


Figure 8.3-1. Architecture of HP GPIO Matrix, HP IO MUX, LP GPIO Matrix, and LP IO MUX

The following points explain the areas marked numerically in the figure above, taking the HP system as an example:

- ① Part of peripheral input signals (marked “yes” in column “Direct input through HP IO MUX” in Table

8.12-1) can be routed to the peripherals via HP IO MUX, or via HP GPIO matrix, while the other input signals can only be routed to the peripherals via HP GPIO matrix.

- ② There are only 55 inputs from GPIO SYNC to HP GPIO matrix, since ESP32-P4 provides 55 GPIO pins in total.
- ③ The pins supplied by VDD\_IO\_0, VDD\_FLASHIO, VDD\_IO\_4 ~ VDD\_IO\_6, and VDD\_LP are controlled by the signals: IE, OE, HYS, WPU, and WPD.
- ④ Part of peripheral outputs (marked “yes” in column “Direct output through HP IO MUX” in Table 8.12-1) can be routed to pins via HP IO MUX or via HP GPIO matrix, while the other output signals can only be routed to pins via HP GPIO matrix.
- ⑤ There are 55 outputs (corresponding to GPIO pin X: 0 ~ 54) from HP GPIO matrix to HP IO MUX.
- ⑥ There are peripheral inputs only through HP IO MUX.
- ⑦ There are peripheral outputs only through HP IO MUX.

Figure 8.3-2 shows the internal structure of a pad, which is an electrical interface between the chip logic and the GPIO pin. The structure is applicable to all 55 GPIO pins and can be controlled using IE, OE, WPU, and WPD signals. For the configuration of these signals, see [IO\\_MUX\\_GPIOX\\_REG](#) or [LP\\_IOMUX\\_PADX\\_REG](#).

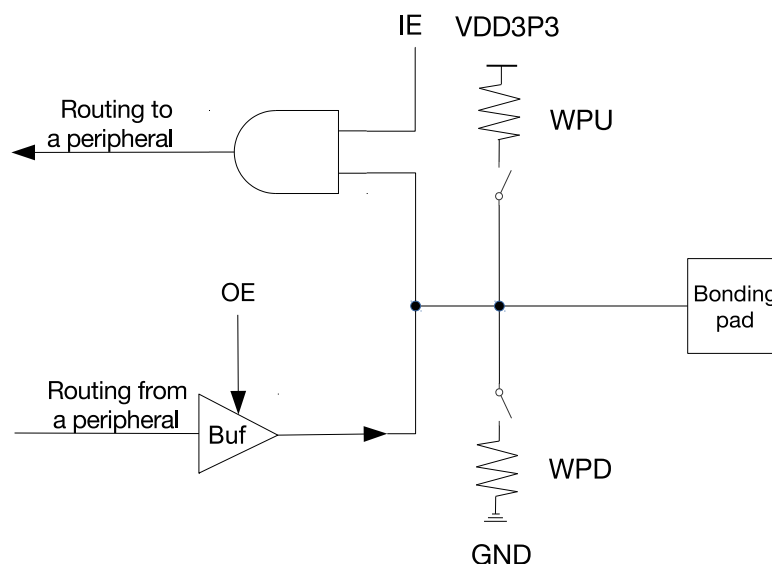


Figure 8.3-2. Internal Structure of a Pad

- IE: input enable
- OE: output enable
- WPU: internal weak pull-up resistor
- WPD: internal weak pull-down resistor
- Bonding pad: a terminal point of the chip logic used to make a physical connection from the chip die to GPIO pin in the chip package

## 8.4 Peripheral Input via GPIO Matrix

### 8.4.1 Overview

To receive a peripheral input signal via HP GPIO matrix,

- configure the matrix to source the peripheral input signal from one of the 55 GPIOs (0 ~ 54), see Table [8.12-1](#).
- configure the peripheral signal to receive input signal via HP GPIO matrix.
- configure the GPIO pin to be controlled by HP IO MUX.

For detailed configuration, see Figure [8.3-1](#) and Section [8.4.7](#).

To receive a peripheral input signal via LP GPIO matrix,

- configure the matrix to source the peripheral input signal from one of the 16 GPIOs (0 ~ 15), see Table [8.13-1](#).
- configure the peripheral signal to receive input signal via LP GPIO matrix.
- configure the LP GPIO pin to be controlled by LP IO MUX.

For detailed configuration, see Figure [8.3-1](#) and Section [8.4.7](#).

As shown in Figure [8.3-1](#), when GPIO matrix is used to input a signal from the pin, all external input signals are sourced from the GPIO pins and then filtered by the GPIO Filter, as shown in Step [2](#) in Section [8.4.7](#).

The Glitch Filter is only available in HP GPIO matrix. The Glitch Filter hardware can filter eight of the output signals from the GPIO Filter, and the other unselected signals go directly to the GPIO SYNC hardware, as shown in Step [3](#) in Section [8.4.7](#).

All signals filtered by the GPIO Filter hardware or the Glitch Filter hardware are synchronized by the GPIO SYNC hardware to IO MUX operating clock and then enter the GPIO matrix, see Section [8.4.2](#). Such signal filtering and synchronization features apply to all GPIO matrix signals but do not apply when using the IO MUX.

### 8.4.2 Signal Synchronization

Only HP GPIO matrix supports this signal synchronization function. Figure [8.4-1](#) shows the functionality of GPIO SYNC. In the figure, negative sync and positive sync mean GPIO input is synchronized on falling edge and on rising edge of HP IO MUX operating clock respectively.

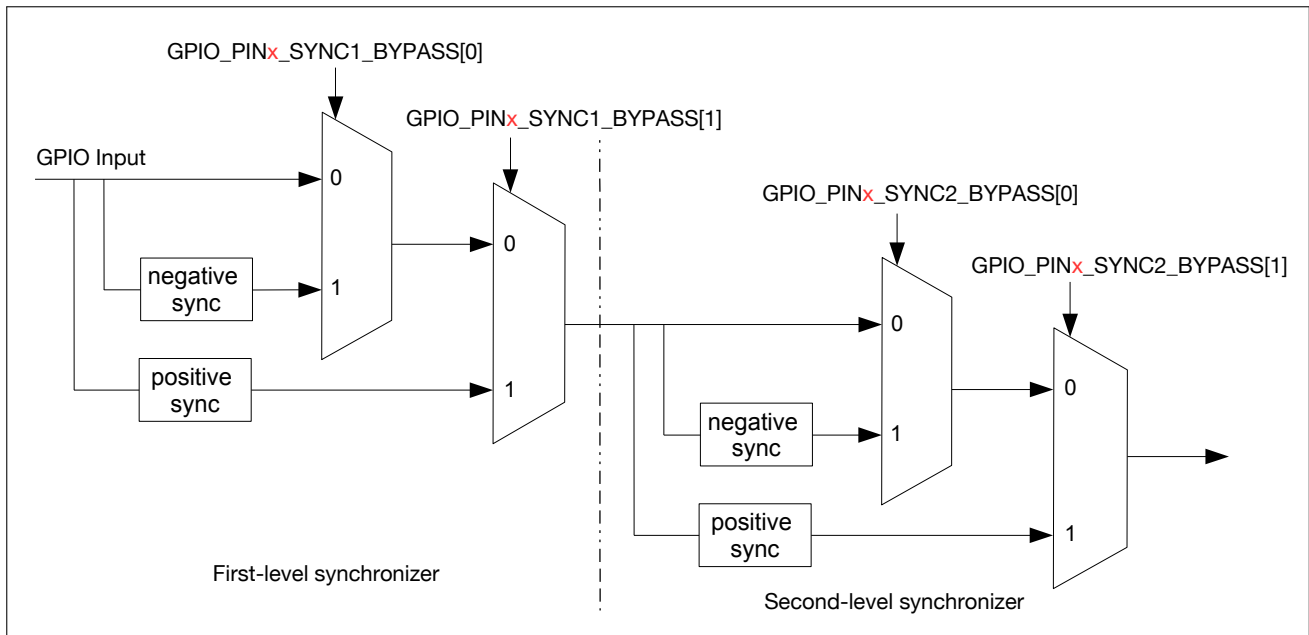


Figure 8.4-1. GPIO Input Synchronized on Rising Edge or on Falling Edge of HP IO MUX Operating Clock

The synchronization function is disabled by default by the synchronizer. But when an asynchronous peripheral signal is connected to the pin, the signal should be synchronized by the two-level synchronizer (i.e., the first-level synchronizer and the second-level synchronizer as shown in Figure 8.4-1) to lower the probability of causing metastability.

### 8.4.3 GPIO Filter

Both the HP GPIO matrix and LP GPIO matrix support GPIO Filter function. When this function is enabled, only signals with a valid width of more than two clock cycles can be sampled, as illustrated in Figure 8.4-2.

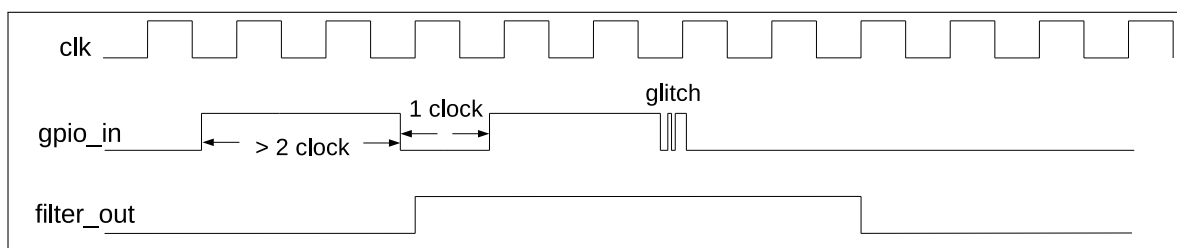


Figure 8.4-2. GPIO Filter Timing of GPIO Input Signals

### 8.4.4 Glitch Filter

The Glitch Filter function is exclusive to the HP GPIO matrix. The Glitch Filter hardware supports eight channels, each of which selects one signal from the 55 (0 ~ 54) output signals generated by the GPIO Filter hardware. It then conducts a second round of filtering on the selected signal. This Glitch Filter hardware can be used to filter slow-speed signals. For more information, see Step 3 in Section 8.4.71.



### 8.4.5 Simple GPIO Input

Both the HP GPIO matrix and LP GPIO matrix support the Simple GPIO Input function. Enabling this function allows the direct reading of the input value of a GPIO pin at any time, without the need to route the GPIO input to any peripherals.

For HP GPIO matrix, to implement simple GPIO input, follow the steps below:

- Set `IO_MUX_GPIOx_MCU_IE` in `IO_MUX_GPIOx_REG`, to enable pin input.
- Read the GPIO input from `GPIO_IN_REG[x]`.

For LP GPIO matrix, to implement simple GPIO input, follow the steps below:

- Set `LP_IOMUX_PADx_FUN_IE` in `LP_IO_MUX_PADx_REG`, to enable pin input.
- Read the GPIO input from `LP_GPIO_IN_REG[x]`.

### 8.4.6 GPIO Wakeup

#### 8.4.6.1 HP GPIO Wakeup

The HP GPIO wakeup feature is designed to awaken the system from Light-sleep when the HP system is in clock gating mode. HP GPIO wakeup is not available when the HP system is powered down.

GPIO0 ~ GPIO54 can be used to generate HP GPIO wakeup by enabling `GPIO_PINx_WAKEUP_ENABLE` ( $x$ : 0 ~ 54).

HP GPIO wakeup supports both high-voltage sensitive and low-voltage sensitive wakeups, with specific conditions based on the GPIO configuration.

**Table 8.4-1. HP GPIO Wakeup Signal Trigger and Clear Conditions**

| <code>GPIO_PINx_INT_TYPE</code> <sup>1,2</sup> | Wakeup is generated when      | Wakeup is cleared when        |
|--|-------------------------------|-------------------------------|
| 5  | the input GPIO is high-level. | the input GPIO is low-level.  |
| 4  | the input GPIO is low-level.  | the input GPIO is high-level. |

<sup>1</sup>  $x$  ranges from 0 to 54.

<sup>2</sup> If the register is configured to any other value, HP GPIO wakeup feature is disabled.

#### 8.4.6.2 LP GPIO Wakeup

The LP GPIO wakeup feature is designed to awaken the system from Deep-sleep when the LP peripherals are not in power gating mode. LP GPIO wakeup is not available when the LP peripherals are powered down.

GPIO0 ~ GPIO15 can be used to generate LP GPIO wakeup by enabling `LP_GPIO_PINn_WAKEUP_ENABLE` ( $n$ : 0 ~ 15).

LP GPIO wakeup supports posedge sensitive, negedge sensitive, both posedge and negedge sensitive, high-voltage sensitive and low-voltage sensitive wakeups, with specific conditions based on the GPIO configuration.

Table 8.4-2. LP GPIO Wakeup Signal Trigger and Clear Conditions

| LP_GPIO_PIN $x$ _INT_TYPE <sup>1,2</sup> | Wakeup is generated when  | Wakeup is cleared when                   |
|--|---|--|
| 1  | the input GPIO toggles from low-level to high-level.                | LP_GPIO_PIN $x$ _EDGE_WAKEUP_CLR is set. |
| 2  | the input GPIO toggles from high-level to low-level.                | LP_GPIO_PIN $x$ _EDGE_WAKEUP_CLR is set. |
| 3  | the input GPIO toggles from high-level to low-level, or vice versa. | LP_GPIO_PIN $x$ _EDGE_WAKEUP_CLR is set. |
| 4  | the input GPIO is low-level.  | the input GPIO is high-level.            |
| 5  | the input GPIO is high-level.                                       | the input GPIO is low-level.             |

<sup>1</sup>  $x$  ranges from 0 to 15.

<sup>2</sup> If the register is configured to any other value, LP GPIO wakeup feature is disabled.

## 8.4.7 Programming Procedure

### 8.4.7.1 HP GPIO Matrix

To read GPIO pin  $X$ <sup>1</sup> into HP peripheral signal  $Y$ , follow the steps below:

1. Configure GPIO\_FUNC $y$ \_IN\_SEL\_CFG\_REG corresponding to HP peripheral signal  $Y$  in HP GPIO matrix:

- Set GPIO\_SIG $y$ \_IN\_SEL to enable peripheral signal input via HP GPIO matrix.
- Set GPIO\_FUNC $y$ \_IN\_SEL to the desired GPIO pin, i.e.,  $X$  here.

**Note that** some peripheral signals have no valid GPIO\_SIG $y$ \_IN\_SEL bit, namely, these peripherals can only receive input signals via HP GPIO matrix.

2. Optionally enable the GPIO Filter for pin input signals by setting IO\_MUX\_GPIO $n$ \_FILTER\_EN.

3. Enable Glitch Filter feature as follows:

- Configure GPIO\_EXT\_FILTER\_CH $n$ \_INPUT\_IO\_NUM to  $m$ .  $n$  (0 ~ 7) represents the channel number.  $m$  (0 ~ 54) represents the GPIO pin number.
- Configure GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_WIDTH to **VALUE1** and GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_THRES to **VALUE2**. During **VALUE1** + 1 cycles, if there are **VALUE2** + 1 input signals that do not match the current output signal value, the Glitch Filter hardware inverts the output signal. GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_WIDTH and GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_THRES can be configured to the same value **VALUE3**, then only signals with a width greater than **VALUE3** + 1 clock cycles will be sampled.
- Set GPIO\_EXT\_FILTER\_CH $n$ \_EN to enable channel  $n$ .

An example is shown in Figure 8.4-3, where GPIO\_EXT\_FILTER\_CH $x$ \_WINDOW\_WIDTH is configured to 3 and GPIO\_EXT\_FILTER\_CH $x$ \_WINDOW\_THRES to 2. The output signal value (signal\_out) keeps as “0” in the four clock cycles before T1. The input signal value (signal\_in) has been “1” for three clock cycles in the same period, then the output signal is inverted to “1” after T1.

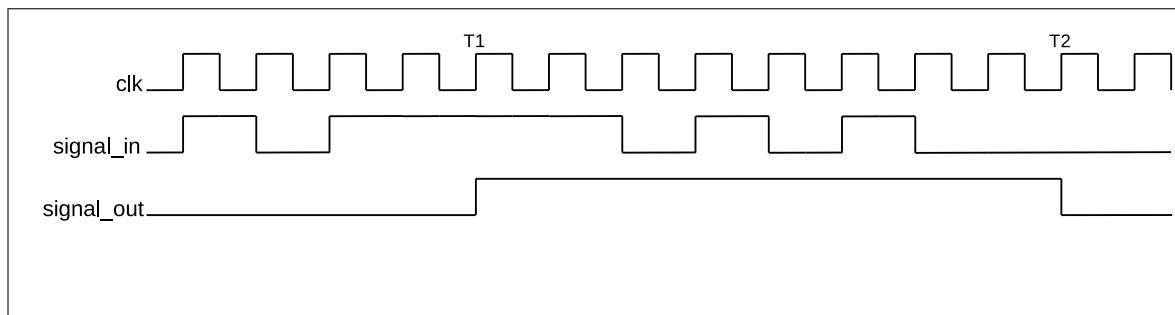


Figure 8.4-3. Glitch Filter Timing Example

4. Synchronize GPIO input signals. To do so, please set `GPIO_PINx_REG` corresponding to GPIO pin  $X$  as follows:
  - Set `GPIO_PINx_SYNC1_BYPASS` to enable input signal synchronized on rising edge or on falling edge in the first-level synchronization, see Figure 8.4-1.
  - Set `GPIO_PINx_SYNC2_BYPASS` to enable input signal synchronized on rising edge or on falling edge in the second-level synchronization, see Figure 8.4-1.
5. Configure HP IO MUX register to enable pin input. For this end, please set `IO_MUX_GPIOx_REG` corresponding to GPIO pin  $X$  as follows:
  - Set `IO_MUX_GPIOx_FUN_IE` to enable input<sup>2</sup>.
  - Set or clear `IO_MUX_GPIOx_FUN_WPU` and `IO_MUX_GPIOx_FUN_WPD` as desired to enable or disable pull-up and pull-down resistors.

For example, to connect UART0 TXD input signal<sup>3</sup> (`uart0_rxd_pad_in`, signal index 10) to GPIO7, please follow the steps below.

1. Set `GPIO_SIG10_IN_SEL` in `GPIO_FUNC10_IN_SEL_CFG_REG` to enable peripheral signal input via HP GPIO matrix.
2. Set `GPIO_FUNC10_IN_SEL` in `GPIO_FUNC10_IN_SEL_CFG_REG` to 7, i.e., select GPIO7.
3. Set `IO_MUX_GPIO7_FUN_IE` in `IO_MUX_GPIO7_REG` to enable pin input.

**Note:**

1. One input pin can be connected to multiple peripheral input signals.
2. The input signal can be inverted by configuring `GPIO_FUNCy_IN_INV_SEL`.
3. It is possible to have a HP peripheral read a constantly low or constantly high input value without connecting this input to a pin. This can be done by selecting a special `GPIO_FUNCy_IN_SEL` input, instead of a GPIO number:
  - When `GPIO_FUNCy_IN_SEL` is set to 62, input signal is always 0.
  - When `GPIO_FUNCy_IN_SEL` is set to 63, input signal is always 1.

### 8.4.7.2 LP GPIO Matrix

The programming procedure for peripheral input via the LP GPIO matrix resembles that of Section 8.4.7.1. However, it's worth noting that:

- the LP GPIO matrix lacks a Glitch Filter function.
- The control and status registers must use LP GPIO related registers. See Section [8.19.4](#) and Section [8.19.5](#).

**Note:**

It is possible to have a LP peripheral read a constantly low or constantly high input value without connecting this input to a pin. This can be done by selecting a special `LP_GPIO_SIGy_IN_SEL` input, instead of a GPIO number:

- When `LP_GPIO_SIGy_IN_SEL` is set to 16, input signal is always 0.
- When `LP_GPIO_SIGy_IN_SEL` is set to 24, input signal is always 1.

## 8.5 Peripheral Output via GPIO Matrix

### 8.5.1 Overview

To output a signal from a peripheral via GPIO matrix,

- configure the HP GPIO matrix to route HP peripheral output signals (only signals with a name assigned in the column “Output signal” in Table [8.12-1](#)) to one of the 55 GPIOs (0 ~ 54).
- Or configure the LP GPIO matrix to route LP peripherals (only signals with a name assigned in the column “Output signal” in Table [8.13-1](#)) to one of the 16 LP GPIOs (0 ~ 15).
- The output signal is routed from the peripheral into GPIO matrix and then into IO MUX. IO MUX must be configured to set the chosen pin to GPIO function. This enables the GPIO output signal to be connected to the pin.

**Note:**

There is a range of peripheral output signals (250 ~ 255 in Table [8.12-1](#)) which are not connected to any peripheral, but to the input signals (250 ~ 255) directly.

### 8.5.2 Simple GPIO Output

GPIO matrix can also be used for simple GPIO output. For this case, one GPIO pin can be configured to directly output the desired value, without routing any peripheral output to this pin.

Follow the steps below to configure HP GPIO matrix for simple GPIO output:

- Set `GPIO_FUNCx_OUT_SEL` with a special peripheral index 256 (0x100).
- Configure the corresponding bit in `GPIO_OUT_REG`/`GPIO_OUT1_REG` to the desired GPIO output value.

**Note:**

- `GPIO_OUT_REG[0] ~ GPIO_OUT_REG[31]` correspond to GPIO0 ~ GPIO31, and `GPIO_OUT1_REG[0] ~ GPIO_OUT1_REG[22]` to GPIO32 ~ GPIO54.
- Recommended operation: use `GPIO_OUT/OUT1_W1TS` and `GPIO_OUT/OUT1_W1TC` to set or clear `GPIO_OUT/OUT1_REG`.

Follow the steps below to configure LP GPIO matrix for simple GPIO output:

- Set `LP_GPIO_FUNCx_OUT_SEL` with a special peripheral index 32 (0x20).
- Configure the corresponding bit in `LP_GPIO_OUT_REG` to the desired GPIO output value.

**Note:**

Recommended operation: use `LP_GPIO_OUT_DATA_WITS` and `LP_GPIO_OUT_DATA_WITC` to set or clear `LP_GPIO_OUT_REG`.

## 8.5.3 Sigma Delta Modulated Output (SDM)

### 8.5.3.1 Functional Description

Eight HP peripheral output signals (index: 72 ~ 79 in Table 8.12-1) support 1-bit second-order sigma delta modulation. By default the output is enabled for these eight channels. This Sigma Delta modulator can also output PDM (pulse density modulation) signal with configurable duty cycle. The function is:

$$H(z) = X(z)z^{-1} + E(z)(1-z^{-1})^2$$

$E(z)$  is quantization error and  $X(z)$  is the input.

This modulator supports scaling down of IO MUX operating clock by divider 1 ~ 256:

- Set `GPIO_EXT_SD_FUNCTION_CLK_EN` to enable the modulator clock.
- Configure `GPIO_EXT_SDn_PRESCALE` ( $n = 0 \sim 7$  for the eight channels).

After scaling, the clock cycle is equal to one pulse output cycle from the modulator.

`GPIO_EXT_SDn_IN` is a signed number with a range of [-128, 127] and is used to control the duty cycle<sup>1</sup> of PDM output signal.

- `GPIO_EXT_SDn_IN` = -128, the duty cycle of the output signal is 0%.
- `GPIO_EXT_SDn_IN` = 0, the duty cycle of the output signal is near 50%.
- `GPIO_EXT_SDn_IN` = 127, the duty cycle of the output signal is near 100%.

The formula for calculating PDM signal duty cycle is shown as below:

$$Duty\_Cycle = \frac{GPIO\_EXT\_SDn\_IN + 128}{256}$$

**Note:**

For PDM signals, duty cycle refers to the percentage of high level cycles to the whole statistical period (several pulse cycles, for example, 256 pulse cycles).

### 8.5.3.2 SDM Configuration

The configuration of SDM is shown below:

- Route one of SDM outputs to a pin via HP GPIO matrix, see Section 8.5.4.1.

- Enable the modulator clock by setting [GPIO\\_EXT\\_SD\\_FUNCTION\\_CLK\\_EN](#).
- Configure the divider value by setting [GPIO\\_EXT\\_SD \$n\$ \\_PRESCALE](#).
- Configure the duty cycle of SDM output signal by setting [GPIO\\_EXT\\_SD \$n\$ \\_IN](#).

## 8.5.4 Programming Procedure

### 8.5.4.1 HP GPIO Matrix

The output signals with a name assigned in the column “Output signal” in Table 8.12-1 can be set to go through the HP GPIO matrix into HP IO MUX and then to a pin. Figure 8.3-1 illustrates the configuration.

To output peripheral signal  $Y$  to a particular GPIO pin  $X$ , follow the steps below:

1. Configure [GPIO\\_FUNC \$x\$ \\_OUT\\_SEL\\_CFG\\_REG](#) and [GPIO\\_ENABLE\\_REG\[ \$x\$ \]](#) corresponding to GPIO pin  $X$  in HP GPIO matrix. Recommended operation: use corresponding [WITS](#) (write 1 to set) and [WITC](#) (write 1 to clear) registers to set or clear [GPIO\\_ENABLE\\_REG](#).
  - Set the [GPIO\\_FUNC \$x\$ \\_OUT\\_SEL](#) field in register [GPIO\\_FUNC \$x\$ \\_OUT\\_SEL\\_CFG\\_REG](#) to the index of the desired peripheral output signal  $Y$ .
  - If the signal should always be enabled as an output, set the [GPIO\\_FUNC \$x\$ \\_OE\\_SEL](#) bit in register [GPIO\\_FUNC \$x\$ \\_OUT\\_SEL\\_CFG\\_REG](#) and the bit in register [GPIO\\_ENABLE\\_WITS\\_REG](#), corresponding to GPIO pin  $X$ . To have the output enable signal decided by internal logic (for example, the `spi2_dqs_pad_oe` in column “Output enable signal when [GPIO\\_FUNC \$n\$ \\_OE\\_SEL](#) = 0” in Table 8.12-1), clear the [GPIO\\_FUNC \$x\$ \\_OE\\_SEL](#) bit instead.
  - Set the corresponding bit in register [GPIO\\_ENABLE\\_WITC\\_REG](#) to disable the output from the GPIO pin.
2. For an open drain output, set the [GPIO\\_PIN \$x\$ \\_PAD\\_DRIVER](#) bit in register [GPIO\\_PIN \$x\$ \\_REG](#) corresponding to GPIO pin  $X$ .
3. Configure HP IO MUX register to enable output via HP GPIO matrix. Set [IO\\_MUX\\_GPIO \$x\$ \\_REG](#) corresponding to GPIO pin  $X$  as follows:
  - Set the field [IO\\_MUX\\_GPIO \$x\$ \\_MCU\\_SEL](#) to desired HP IO MUX function corresponding to GPIO pin  $X$ . This is Function 1 (GPIO function), numeric value 1, for all pins.
  - Set the [IO\\_MUX\\_GPIO \$x\$ \\_FUN\\_DRV](#) field to the desired value for output strength (0 ~ 3). The higher the drive strength, the more current can be sourced/sunk from the pin.
  - If using open drain mode, set/clear the [IO\\_MUX\\_GPIO \$x\$ \\_FUN\\_WPU](#) and [IO\\_MUX\\_GPIO \$x\$ \\_FUN\\_WPD](#) bits to enable/disable the internal pull-up/pull-down resistors.
4. Enable hysteresis function:
  - GPIO00 ~ GPIO15: set [LP\\_IOMUX\\_LP\\_GPIO\\_HYS\[ \$x\$ \]](#) ( $x$ : 0 ~ 15, corresponding to GPIO00 ~ GPIO15).
  - GPIO16 ~ GPIO47: set [HP\\_SYSTEM\\_GPIO\\_O\\_HYS\\_LOW\[ \$x\$ \]](#) ( $x$ : 0 ~ 31, corresponding to GPIO16 ~ GPIO47).
  - GPIO48 ~ GPIO54: set [HP\\_SYSTEM\\_GPIO\\_O\\_HYS\\_HIGH\[ \$x\$ \]](#) ( $x$ : 0 ~ 6, corresponding to GPIO48 ~ GPIO54).

**Note:**

- The output signal from a single peripheral can be sent to multiple pins simultaneously.
- The output signal can be inverted by setting `GPIO_FUNCx_OUT_INV_SEL`.

### 8.5.4.2 LP GPIO Matrix

The programming procedure for peripheral input via the LP GPIO matrix resembles that of 8.5.4.1. However, it's worth noting that the control and status registers must use LP GPIO matrix registers. See Section 8.19.4 and Section 8.19.5.

## 8.6 Direct Input and Output via IO MUX

### 8.6.1 Overview

Some digital signals (SDMMC, EMAC, etc.) can bypass GPIO matrix for better high-frequency digital performance. In this case, IO MUX is used to connect these pins directly to peripherals. This option is less flexible than routing signals via GPIO matrix, as the IO MUX register for each GPIO pin can only select from a limited number of functions, but high-frequency digital performance can be improved.

ESP32-P4 provides 16 GPIO pins with low power (LP) capabilities. These pins can be controlled by either HP IO MUX or LP IO MUX. If controlled by LP IO MUX, these pins will bypass HP IO MUX and HP GPIO matrix for the use by peripherals in LP system.

When configured as LP GPIOs, the pins can still be controlled by the peripherals in LP system during chip Deep-sleep, and wake up the chip from Deep-sleep.

### 8.6.2 Functional Description

The pins with LP functions (GPIO0 ~ GPIO15) are controlled by `LP_IOMUX_PADn_MUX_SEL` ( $n$ : 0 ~ 15) in register `LP_IOMUX_PADn_REG`. By default, all bits in these registers are set to 0, routing all input/output signals via HP IO MUX.

If `LP_IOMUX_PADn_MUX_SEL` is set, then input/output signals are controlled by LP IO MUX. In this mode, `LP_IOMUX_PADn_REG` is used to control the LP GPIO pins. See 8.15-1 for the LP functions of each LP GPIO pin. Note that `LP_IOMUX_PADn_REG` applies the LP GPIO pin numbering, not the HP GPIO pin numbering.

#### 8.6.2.1 HP IO MUX

Two fields must be configured in order to bypass HP GPIO matrix for HP peripheral input signals:

1. `IO_MUX_GPIOn_MCU_SEL` for the GPIO pin must be set to the required pin function. For the list of pin functions, please refer to Table 8.14-1.
2. Clear `GPIO_SIGn_IN_SEL` to route the input directly to the peripheral.

To bypass HP GPIO matrix for HP peripheral output signals, `IO_MUX_GPIOn_MCU_SEL` for the GPIO pin must be set to the required pin function.

### 8.6.2.2 LP IO MUX

Two fields must be configured in order to bypass LP GPIO matrix for LP peripheral input signals:

1. [LP\\_IOMUX\\_PAD \$n\$ \\_MUX\\_SEL](#) for the GPIO pin must be set to the required pin function. For the list of pin functions, please refer to Table 8.15-1.
2. Clear [LP\\_GPIO\\_GPIO\\_SIG \$n\$ \\_IN\\_SEL](#) to route the input directly to the peripheral.

To bypass LP GPIO matrix for LP peripheral output signals, [LP\\_IOMUX\\_PAD \$n\$ \\_MUX\\_SEL](#) for the GPIO pin must be set to the required pin function.

**Note:**

Not all signals can be directly connected to peripheral via IO MUX. Some input/output signals can only be connected to peripheral via GPIO matrix.

## 8.7 Analog Functions

### 8.7.1 Overview

ESP32-P4 provides 34 GPIO pins with analog functions, including 16 LP GPIO pins and 18 HP GPIO pins. See Table 8.16-1.

### 8.7.2 Analog Functions

When the pin is used for analog purpose, make sure this pin is left floating by configuring registers. By such way, the external analog signal is directly connected to internal analog signal via GPIO pin. The configuration is as follows:

- Clear [IO\\_MUX\\_GPIO \$n\$ \\_FUN\\_IE](#), [IO\\_MUX\\_GPIO \$n\$ \\_FUN\\_WPU](#), and [IO\\_MUX\\_GPIO \$n\$ \\_FUN\\_WPD](#), to set the pin floating.
- Write 1 to the corresponding bit in [GPIO\\_ENABLE\\_W1TC](#) and [GPIO\\_ENABLE1\\_W1TC](#), to clear output enable.

To use these functions listed in Table 8.16-1, please refer to the following related chapters:

- For XTAL\_32K related functions, see Chapter 13 *Low-Power Management*.
- For TOUCH related functions, see Chapter 55 *Touch Sensor (TOUCH)*.
- For ADC related functions, see Chapter 57 *ADC Controller (ADC)*.
- For COMP related functions, see Chapter 58 *Analog Voltage Comparator*.

**Note:**

GPIO51 ~ GPIO54 each has two different analog functions, which can be used simultaneously.



## 8.8 Pin Functions in Light-sleep

Pins may provide different functions when ESP32-P4 is in Light-sleep mode. If `IO_MUX_GPIO $n$ _SLP_SEL` in register `IO_MUX_GPIO $n$ _REG` for a GPIO pin is set to 1, a different set of bits will be used to control the pin when the chip is in Light-sleep mode.

**Table 8.8-1. Bit Used to Control IO MUX Functions in Light-sleep Mode**

| IO MUX Function       | Normal Execution<br>OR <code>IO_MUX_GPIO<math>n</math>_SLP_SEL</code> = 0 | Light-sleep Mode<br>AND <code>IO_MUX_GPIO<math>n</math>_SLP_SEL</code> = 1 |
|-----------------------|---|--|
| Output Drive Strength | <code>IO_MUX_GPIO<math>n</math>_FUN_DRV</code>                            | <code>IO_MUX_GPIO<math>n</math>_MCU_DRV</code>                             |
| Pull-up Resistor      | <code>IO_MUX_GPIO<math>n</math>_FUN_WPU</code>                            | <code>IO_MUX_GPIO<math>n</math>_MCU_WPU</code>                             |
| Pull-down Resistor    | <code>IO_MUX_GPIO<math>n</math>_FUN_WPD</code>                            | <code>IO_MUX_GPIO<math>n</math>_MCU_WPD</code>                             |
| Input Enable          | <code>IO_MUX_GPIO<math>n</math>_FUN_IE</code>                             | <code>IO_MUX_GPIO<math>n</math>_MCU_IE</code>                              |
| Output Enable         | <code>OE_SEL</code> from GPIO matrix*                                     | <code>IO_MUX_GPIO<math>n</math>_MCU_OE</code>                              |

**Note:**

If `IO_MUX_GPIO $n$ _SLP_SEL` is set to 0, pin functions remain the same in both normal execution and in Light-sleep mode. Please refer to Section 8.5.4.1 for how to enable output in normal execution.

## 8.9 Pin Hold Feature

Each GPIO pin has an individual hold function controlled by Power Management Unit (PMU) or registers. When the pin is set to hold, the state is latched at that moment and will not change no matter how the internal signals change or how the IO MUX/GPIO configuration is modified. Users can use the hold function for the pins to retain the pin state through a core reset triggered by watchdog time-out or Deep-sleep events.

### Digital Pins (GPIO16 ~ GPIO54):

The Hold state of each digital pin is controlled by the result of OR operation of the pin's Hold enable signal and the global Hold enable signal.

- `HP_SYSREG_GPIO_O_HOLD_LOW_REG[ $n$ ]` ( $n = 0 \sim 31$ ), controls the Hold signal of each pin of GPIO16 ~ GPIO47. `HP_SYSREG_GPIO_O_HOLD_HIGH_REG[ $n$ ]` ( $n = 0 \sim 7$ ), controls the Hold signal of each pin of GPIO48 ~ GPIO54.
- `PMU_TIE_HIGH_HP_PAD_HOLD_ALL`, controls the global Hold signal of all digital pins.

To use this feature, follow the steps below:

- To maintain the pin's input/output status in Deep-sleep, set `HP_SYSREG_GPIO_O_HOLD_LOW_REG[ $n$ ]` (where  $n = 0 \sim 31$  corresponds to GPIO16 ~ GPIO47) or `HP_SYSREG_GPIO_O_HOLD_HIGH_REG[ $n$ ]` (where  $n = 0 \sim 7$  corresponds to GPIO48 ~ GPIO54) before powering down. To disable the hold function after waking up, clear both registers.
- Alternatively, set `PMU_TIE_HIGH_HP_PAD_HOLD_ALL` to maintain the input/output status of all digital pins and set `PMU_TIE_LOW_HP_PAD_HOLD_ALL` to disable the hold function for all digital pins.

- Alternatively, configure the PMU task to hold the HP pins before Deep-sleep. In Deep-sleep, the HP pins would be hold automatically by the PMU.

#### LP Pins (GPIO0 ~ GPIO15):

The Hold state of each LP pin is controlled by the result of OR operation of the pin's Hold enable signal and the global Hold enable signal.

- [LP\\_IOMUX\\_LP\\_PAD\\_HOLD\\_REG\[n\]](#), controls the Hold signal of each pin of GPIO0 ~ GPIO15.
- [PMU\\_TIE\\_HIGH\\_LP\\_PAD\\_HOLD\\_ALL](#), controls the global Hold signal of all LP pins.

To use this feature, follow the steps below:

- To maintain the pin's input/output status in Deep-sleep, set [LP\\_IOMUX\\_LP\\_PAD\\_HOLD\\_REG\[n\]](#) to hold the value of GPIO $n$ , or clear [LP\\_IOMUX\\_LP\\_PAD\\_HOLD\\_REG\[n\]](#) to disable the hold function of GPIO $n$ .
- Alternatively, set [PMU\\_TIE\\_HIGH\\_LP\\_PAD\\_HOLD\\_ALL](#) to hold the values of all LP pins, and set [PMU\\_TIE\\_LOW\\_LP\\_PAD\\_HOLD\\_ALL](#) to disable the hold function of all LP pins.
- Alternatively, configure the PMU task to hold LP pins before Deep-sleep. In Deep-sleep, LP pins will be hold automatically by the PMU.

## 8.10 Hysteresis Characteristics of GPIO Pins

Each GPIO pin has hysteresis functionality. When hysteresis is not enabled, as shown in Figure 8.10-1, the level flip of the signal (C) input to the chip from the PAD has only one threshold ( $V_t$ , about 1.7 V). When the voltage on the PAD is higher than  $V_t$ , the level on the C is high. Otherwise, it is low. However, noise on the PAD may affect the signal on C.

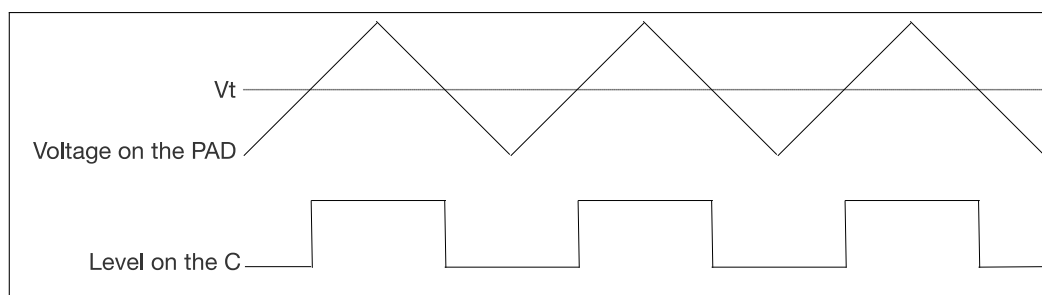


Figure 8.10-1. Example of Level Flip on the Chip Pad — Hysteresis Function Not Enabled

When hysteresis is enabled, as shown in Figure 8.10-2, the level flip of C has two thresholds, high-level threshold ( $V_{th}$ , about 1.7 V) and low-level threshold ( $V_{tl}$ , about 1.4 V). When the voltage of pad goes from low to high, if the voltage is higher than  $V_{th}$ , the level of C is high. When the voltage of PAD goes from high to low, if the voltage is lower than  $V_{tl}$ , the level of C is low. When the voltage of PAD is between  $V_{th}$  and  $V_{tl}$ , the level of C does not change. The hysteresis function plays an anti-interference role by mitigating the impact of noise, consequently reducing the level flip time of C.

To enable the hysteresis function, follow the steps below:

- Set [LP\\_IOMUX\\_LP\\_GPIO\\_HYS\[n\]](#) ( $n$  ranges from 0 ~ 15, corresponding to GPIO0 ~ GPIO15), [HP\\_SYS\\_GPIO0\\_HYS\\_LOW\[n\]](#) ( $n$  ranges from 0 ~ 31, corresponding to GPIO16 ~ GPIO47) or

HP\_SYS\_GPIO0\_HYS\_HIGH[*n*] (*n* ranges from 0 ~ 6, corresponding to GPIO48 ~ GPIO54) to 1 to enable the hysteresis function for GPIO*n*.

- Set LP\_IOMUX\_LP\_GPIO\_HYS[*n*] (*n* ranges from 0 ~ 15, corresponding to GPIO0 ~ GPIO15), HP\_SYS\_GPIO0\_HYS\_LOW[*n*] (*n* ranges from 0 ~ 31, corresponding to GPIO16 ~ GPIO47) or HP\_SYS\_GPIO0\_HYS\_HIGH[*n*] (*n* ranges from 0 ~ 6, corresponding to GPIO48 ~ GPIO54) to 0 to disable the hysteresis function for GPIO*n*.

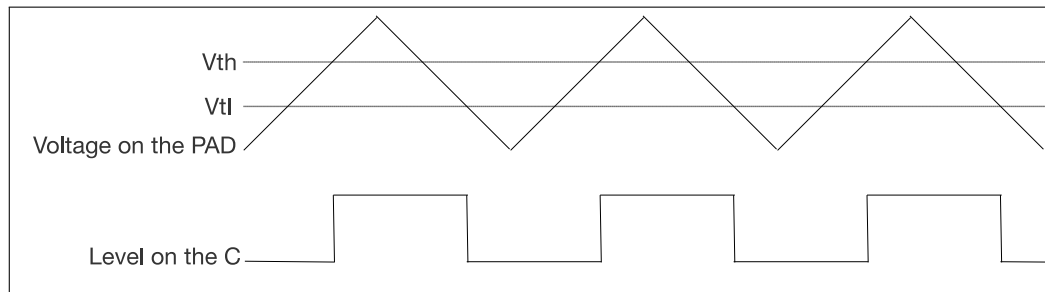


Figure 8.10-2. Example of Level Flip on the Chip Pad — Hysteresis Function Enabled

## 8.11 Power Supplies and Management of GPIO Pins

### 8.11.1 Power Supplies of GPIO Pins

For more information on the power supply for GPIO pins, please refer to Pin Definition in [ESP32-P4 Datasheet](#). All the pins can be used to wake up the chip from Light-sleep, but only the pins (GPIO0 ~ GPIO15) in VDD\_LP domain can be used to wake up the chip from Deep-sleep.

### 8.11.2 Power Supply Management

Each ESP32-P4 pin is connected to one of the following power domains.

- VDD\_LP: the input power supply for LP GPIO pins
- VDD\_IO\_0, VDD\_FLASHIO, VDD\_IO\_4 ~ VDD\_IO\_6: the input power supply for HP GPIO pins

## 8.12 HP Peripheral Signal List

Table 8.12-1 shows the peripheral input/output signals via HP GPIO matrix.

Please pay attention to the configuration of the bit `GPIO_FUNCn_OE_SEL`:

- `GPIO_FUNCn_OE_SEL` = 1: the output enable is controlled by the corresponding bit *n* of `GPIO_ENABLE/ENABLE1_REG`:
  - `GPIO_ENABLE/ENABLE1_REG` = 0: output is disabled.
  - `GPIO_ENABLE/ENABLE1_REG` = 1: output is enabled.
- `GPIO_FUNCn_OE_SEL` = 0: use the output enable signal from peripheral, for example `spi2_dqs_pad_oe` in the column “Output enable signal when `GPIO_FUNCn_OE_SEL` = 0” of Table 8.12-1. Note that the signals such as `spi2_dqs_pad_oe` can be 1 (1'd1) or 0 (1'd0), depending on the configuration of

corresponding peripherals. If it's 1'd1 in column "Output enable signal when `GPIO_FUNCn_OE_SEL` = 0", it indicates that once `GPIO_FUNCn_OE_SEL` is cleared, the output signal is always enabled by default.

**Note:**

Signals are numbered consecutively, but not all signals are valid.

- Only the signals with a name assigned in the column "Input signal" in Table 8.12-1 are valid input signals.
- Only the signals with a name assigned in the column "Output signal" in Table 8.12-1 are valid output signals.

Table 8.12-1. Peripheral Signals via HP GPIO Matrix

| Signal No. | Input Signal            | Default Value | Direct Input via HP IO MUX | Output Signal            | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|-------------------------|---------------|----------------------------|--------------------------|---|-----------------------------|
| 0          | -                       | -             | -                          | sd_card_cclk_2_pad_out   | 1'd1  | no                          |
| 1          | sd_card_ccmd_2_pad_in   | 1             | no                         | sd_card_ccmd_2_pad_out   | sd_card_ccmd_2_pad_oe                           | no                          |
| 2          | sd_card_cdata0_2_pad_in | 1             | no                         | sd_card_cdata0_2_pad_out | sd_card_cdata0_2_pad_oe                         | no                          |
| 3          | sd_card_cdata1_2_pad_in | 1             | no                         | sd_card_cdata1_2_pad_out | sd_card_cdata1_2_pad_oe                         | no                          |
| 4          | sd_card_cdata2_2_pad_in | 1             | no                         | sd_card_cdata2_2_pad_out | sd_card_cdata2_2_pad_oe                         | no                          |
| 5          | sd_card_cdata3_2_pad_in | 1             | no                         | sd_card_cdata3_2_pad_out | sd_card_cdata3_2_pad_oe                         | no                          |
| 6          | sd_card_cdata4_2_pad_in | 1             | no                         | sd_card_cdata4_2_pad_out | sd_card_cdata4_2_pad_oe                         | no                          |
| 7          | sd_card_cdata5_2_pad_in | 1             | no                         | sd_card_cdata5_2_pad_out | sd_card_cdata5_2_pad_oe                         | no                          |
| 8          | sd_card_cdata6_2_pad_in | 1             | no                         | sd_card_cdata6_2_pad_out | sd_card_cdata6_2_pad_oe                         | no                          |
| 9          | sd_card_cdata7_2_pad_in | 1             | no                         | sd_card_cdata7_2_pad_out | sd_card_cdata7_2_pad_oe                         | no                          |
| 10         | uart0_rxd_pad_in        | 0             | yes                        | uart0_txd_pad_out        | 1'd1  | yes                         |
| 11         | uart0_cts_pad_in        | 0             | yes                        | uart0_rts_pad_out        | 1'd1  | yes                         |
| 12         | uart0_dsr_pad_in        | 0             | no                         | uart0_dtr_pad_out        | 1'd1  | no                          |
| 13         | uart1_rxd_pad_in        | 0             | yes                        | uart1_txd_pad_out        | 1'd1  | yes                         |
| 14         | uart1_cts_pad_in        | 0             | yes                        | uart1_rts_pad_out        | 1'd1  | yes                         |
| 15         | uart1_dsr_pad_in        | 0             | no                         | uart1_dtr_pad_out        | 1'd1  | no                          |
| 16         | uart2_rxd_pad_in        | 0             | no                         | uart2_txd_pad_out        | 1'd1  | no                          |
| 17         | uart2_cts_pad_in        | 0             | no                         | uart2_rts_pad_out        | 1'd1  | no                          |
| 18         | uart2_dsr_pad_in        | 0             | no                         | uart2_dtr_pad_out        | 1'd1  | no                          |
| 19         | uart3_rxd_pad_in        | 0             | no                         | uart3_txd_pad_out        | 1'd1  | no                          |
| 20         | uart3_cts_pad_in        | 0             | no                         | uart3_rts_pad_out        | 1'd1  | no                          |
| 21         | uart3_dsr_pad_in        | 0             | no                         | uart3_dtr_pad_out        | 1'd1  | no                          |
| 22         | uart4_rxd_pad_in        | 0             | no                         | uart4_txd_pad_out        | 1'd1  | no                          |
| 23         | uart4_cts_pad_in        | 0             | no                         | uart4_rts_pad_out        | 1'd1  | no                          |
| 24         | uart4_dsr_pad_in        | 0             | no                         | uart4_dtr_pad_out        | 1'd1  | no                          |
| 25         | i2s0_o_bck_pad_in       | 0             | no                         | i2s0_o_bck_pad_out       | 1'd1  | no                          |
| 26         | i2s0_mclk_pad_in        | 0             | no                         | i2s0_mclk_pad_out        | 1'd1  | no                          |

| Signal No. | Input Signal      | Default Value | Direct Input via HP IO MUX | Output Signal      | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|-------------------|---------------|----------------------------|--------------------|---|-----------------------------|
| 27         | i2s0_o_ws_pad_in  | 0             | no                         | i2s0_o_ws_pad_out  | 1'd1  | no                          |
| 28         | i2s0_i_sd_pad_in  | 0             | no                         | i2s0_o_sd_pad_out  | 1'd1  | no                          |
| 29         | i2s0_i_bck_pad_in | 0             | no                         | i2s0_i_bck_pad_out | 1'd1  | no                          |
| 30         | i2s0_i_ws_pad_in  | 0             | no                         | i2s0_i_ws_pad_out  | 1'd1  | no                          |
| 31         | i2s1_o_bck_pad_in | 0             | no                         | i2s1_o_bck_pad_out | 1'd1  | no                          |
| 32         | i2s1_mclk_pad_in  | 0             | no                         | i2s1_mclk_pad_out  | 1'd1  | no                          |
| 33         | i2s1_o_ws_pad_in  | 0             | no                         | i2s1_o_ws_pad_out  | 1'd1  | no                          |
| 34         | i2s1_i_sd_pad_in  | 0             | no                         | i2s1_o_sd_pad_out  | 1'd1  | no                          |
| 35         | i2s1_i_bck_pad_in | 0             | no                         | i2s1_i_bck_pad_out | 1'd1  | no                          |
| 36         | i2s1_i_ws_pad_in  | 0             | no                         | i2s1_i_ws_pad_out  | 1'd1  | no                          |
| 37         | i2s2_o_bck_pad_in | 0             | no                         | i2s2_o_bck_pad_out | 1'd1  | no                          |
| 38         | i2s2_mclk_pad_in  | 0             | no                         | i2s2_mclk_pad_out  | 1'd1  | no                          |
| 39         | i2s2_o_ws_pad_in  | 0             | no                         | i2s2_o_ws_pad_out  | 1'd1  | no                          |
| 40         | i2s2_i_sd_pad_in  | 0             | no                         | i2s2_o_sd_pad_out  | 1'd1  | no                          |
| 41         | i2s2_i_bck_pad_in | 0             | no                         | i2s2_i_bck_pad_out | 1'd1  | no                          |
| 42         | i2s2_i_ws_pad_in  | 0             | no                         | i2s2_i_ws_pad_out  | 1'd1  | no                          |
| 43         | i2s0_i_sd1_pad_in | 0             | no                         | i2s0_o_sd1_pad_out | 1'd1  | no                          |
| 44         | i2s0_i_sd2_pad_in | 0             | no                         | spi2_dqs_pad_out   | spi2_dqs_pad_oe                                 | yes                         |
| 45         | i2s0_i_sd3_pad_in | 0             | no                         | spi3_cs2_pad_out   | spi3_cs2_pad_oe                                 | no                          |
| 46         | -                 | -             | -                          | spi3_cs1_pad_out   | spi3_cs1_pad_oe                                 | no                          |
| 47         | spi3_ck_pad_in    | 0             | no                         | spi3_ck_pad_out    | spi3_ck_pad_oe                                  | no                          |
| 48         | spi3_q_pad_in     | 0             | no                         | spi3_qo_pad_out    | spi3_q_pad_oe                                   | no                          |
| 49         | spi3_d_pad_in     | 0             | no                         | spi3_d_pad_out     | spi3_d_pad_oe                                   | no                          |
| 50         | spi3_hold_pad_in  | 0             | no                         | spi3_hold_pad_out  | spi3_hold_pad_oe                                | no                          |
| 51         | spi3_wp_pad_in    | 0             | no                         | spi3_wp_pad_out    | spi3_wp_pad_oe                                  | no                          |
| 52         | spi3_cs_pad_in    | 0             | no                         | spi3_cs_pad_out    | spi3_cs_pad_oe                                  | no                          |
| 53         | spi2_ck_pad_in    | 0             | yes                        | spi2_ck_pad_out    | spi2_ck_pad_oe                                  | yes                         |
| 54         | spi2_q_pad_in     | 0             | yes                        | spi2_q_pad_out     | spi2_q_pad_oe                                   | yes                         |

| Signal No. | Input Signal         | Default Value | Direct Input via HP IO MUX | Output Signal            | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|----------------------|---------------|----------------------------|--------------------------|---|-----------------------------|
| 55         | spi2_d_pad_in        | 0             | yes                        | spi2_d_pad_out           | spi2_d_pad_oe                                   | yes                         |
| 56         | spi2_hold_pad_in     | 0             | yes                        | spi2_hold_pad_out        | spi2_hold_pad_oe                                | yes                         |
| 57         | spi2_wp_pad_in       | 0             | yes                        | spi2_wp_pad_out          | spi2_wp_pad_oe                                  | yes                         |
| 58         | spi2_io4_pad_in      | 0             | yes                        | spi2_io4_pad_out         | spi2_io4_pad_oe                                 | yes                         |
| 59         | spi2_io5_pad_in      | 0             | yes                        | spi2_io5_pad_out         | spi2_io5_pad_oe                                 | yes                         |
| 60         | spi2_io6_pad_in      | 0             | yes                        | spi2_io6_pad_out         | spi2_io6_pad_oe                                 | yes                         |
| 61         | spi2_io7_pad_in      | 0             | yes                        | spi2_io7_pad_out         | spi2_io7_pad_oe                                 | yes                         |
| 62         | spi2_cs_pad_in       | 0             | yes                        | spi2_cs_pad_out          | spi2_cs_pad_oe                                  | yes                         |
| 63         | pcnt_rst_pad_in0     | 0             | no                         | spi2_cs1_pad_out         | spi2_cs1_pad_oe                                 | no                          |
| 64         | pcnt_rst_pad_in1     | 0             | no                         | spi2_cs2_pad_out         | spi2_cs2_pad_oe                                 | no                          |
| 65         | pcnt_rst_pad_in2     | 0             | no                         | spi2_cs3_pad_out         | spi2_cs3_pad_oe                                 | no                          |
| 66         | pcnt_rst_pad_in3     | 0             | no                         | spi2_cs4_pad_out         | spi2_cs4_pad_oe                                 | no                          |
| 67         | -                    | -             | -                          | spi2_cs5_pad_out         | spi2_cs5_pad_oe                                 | no                          |
| 68         | i2c0_scl_pad_in      | 1             | no                         | i2c0_scl_pad_out         | i2c0_scl_oe_pad_out                             | no                          |
| 69         | i2c0_sda_pad_in      | 1             | no                         | i2c0_sda_pad_out         | i2c0_sda_oe_pad_out                             | no                          |
| 70         | i2c1_scl_pad_in      | 1             | no                         | i2c1_scl_pad_out         | i2c1_scl_oe_pad_out                             | no                          |
| 71         | i2c1_sda_pad_in      | 1             | no                         | i2c1_sda_pad_out         | i2c1_sda_oe_pad_out                             | no                          |
| 72         | -                    | -             | -                          | gpio_sd0_out             | 1'd1  | no                          |
| 73         | -                    | -             | -                          | gpio_sd1_out             | 1'd1  | no                          |
| 74         | uart0_slp_clk_pad_in | 0             | no                         | gpio_sd2_out             | 1'd1  | no                          |
| 75         | uart1_slp_clk_pad_in | 0             | no                         | gpio_sd3_out             | 1'd1  | no                          |
| 76         | uart2_slp_clk_pad_in | 0             | no                         | gpio_sd4_out             | 1'd1  | no                          |
| 77         | uart3_slp_clk_pad_in | 0             | no                         | gpio_sd5_out             | 1'd1  | no                          |
| 78         | uart4_slp_clk_pad_in | 0             | no                         | gpio_sd6_out             | 1'd1  | no                          |
| 79         | -                    | -             | -                          | gpio_sd7_out             | 1'd1  | no                          |
| 80         | twai0_rx_pad_in      | 1             | no                         | twai0_tx_pad_out         | 1'd1  | no                          |
| 81         | -                    | -             | -                          | twai0_bus_off_on_pad_out | 1'd1  | no                          |
| 82         | -                    | -             | -                          | twai0_clkout_pad_out     | 1'd1  | no                          |

| Signal No. | Input Signal           | Default Value | Direct Input via HP IO MUX | Output Signal               | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|------------------------|---------------|----------------------------|-----------------------------|---|-----------------------------|
| 83         | twai1_rx_pad_in        | 1             | no                         | twai1_tx_pad_out            | 1'd1  | no                          |
| 84         | -                      | -             | -                          | twai1_bus_off_on_pad_out    | 1'd1  | no                          |
| 85         | -                      | -             | -                          | twai1_clkout_pad_out        | 1'd1  | no                          |
| 86         | twai2_rx_pad_in        | 1             | no                         | twai2_tx_pad_out            | 1'd1  | no                          |
| 87         | -                      | -             | -                          | twai2_bus_off_on_pad_out    | 1'd1  | no                          |
| 88         | -                      | -             | -                          | twai2_clkout_pad_out        | 1'd1  | no                          |
| 89         | pwm0_sync0_pad_in      | 0             | no                         | pwm0_ch0_a_pad_out          | 1'd1  | no                          |
| 90         | pwm0_sync1_pad_in      | 0             | no                         | pwm0_ch0_b_pad_out          | 1'd1  | no                          |
| 91         | pwm0_sync2_pad_in      | 0             | no                         | pwm0_ch1_a_pad_out          | 1'd1  | no                          |
| 92         | pwm0_f0_pad_in         | 0             | no                         | pwm0_ch1_b_pad_out          | 1'd1  | no                          |
| 93         | pwm0_f1_pad_in         | 0             | no                         | pwm0_ch2_a_pad_out          | 1'd1  | no                          |
| 94         | pwm0_f2_pad_in         | 0             | no                         | pwm0_ch2_b_pad_out          | 1'd1  | no                          |
| 95         | pwm0_cap0_pad_in       | 0             | no                         | pwm1_ch0_a_pad_out          | 1'd1  | no                          |
| 96         | pwm0_cap1_pad_in       | 0             | no                         | pwm1_ch0_b_pad_out          | 1'd1  | no                          |
| 97         | pwm0_cap2_pad_in       | 0             | no                         | pwm1_ch1_a_pad_out          | 1'd1  | no                          |
| 98         | pwm1_sync0_pad_in      | 0             | no                         | pwm1_ch1_b_pad_out          | 1'd1  | no                          |
| 99         | pwm1_sync1_pad_in      | 0             | no                         | pwm1_ch2_a_pad_out          | 1'd1  | no                          |
| 100        | pwm1_sync2_pad_in      | 0             | no                         | pwm1_ch2_b_pad_out          | 1'd1  | no                          |
| 101        | pwm1_f0_pad_in         | 0             | no                         | -                           | -   | -                           |
| 102        | pwm1_f1_pad_in         | 0             | no                         | -                           | -   | -                           |
| 103        | pwm1_f2_pad_in         | 0             | no                         | -                           | -   | -                           |
| 104        | pwm1_cap0_pad_in       | 0             | no                         | -                           | -   | -                           |
| 105        | pwm1_cap1_pad_in       | 0             | no                         | twai0_standby_pad_out       | 1'd1  | no                          |
| 106        | pwm1_cap2_pad_in       | 0             | no                         | twai1_standby_pad_out       | 1'd1  | no                          |
| 107        | gmii_mdi_pad_in        | 0             | no                         | twai2_standby_pad_out       | 1'd1  | no                          |
| 108        | gmac_phy_col_pad_in    | 0             | no                         | gmii_mdc_pad_out            | 1'd1  | no                          |
| 109        | gmac_phy_crs_pad_in    | 0             | no                         | gmii_mdo_pad_out            | gmii_mdo_oe_pad_out                             | no                          |
| 110        | usb_otg11_iddig_pad_in | 0             | no                         | usb_srp_dischrgvbus_pad_out | 1'd1  | no                          |



| Signal No. | Input Signal               | Default Value | Direct Input via HP IO MUX | Output Signal                | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|----------------------------|---------------|----------------------------|------------------------------|---|-----------------------------|
| 111        | usb_otg11_avalid_pad_in    | 0             | no                         | usb_otg11_idpullup_pad_out   | 1'd1  | no                          |
| 112        | usb_srp_bvalid_pad_in      | 0             | no                         | usb_otg11_dppulldown_pad_out | 1'd1  | no                          |
| 113        | usb_otg11_vbusvalid_pad_in | 0             | no                         | usb_otg11_dmpulldown_pad_out | 1'd1  | no                          |
| 114        | usb_srp_sessend_pad_in     | 0             | no                         | usb_otg11_drvvbus_pad_out    | 1'd1  | no                          |
| 115        | -                          | -             | -                          | usb_srp_chrgvbus_pad_out     | 1'd1  | no                          |
| 116        | -                          | -             | -                          | -                            | -   | -                           |
| 117        | ulpi_clk_pad_in            | 0             | no                         | -                            | -   | -                           |
| 118        | usb_hsphy_refclk_in        | 0             | no                         | -                            | -   | -                           |
| 119        | -                          | -             | -                          | -                            | -   | -                           |
| 120        | -                          | -             | -                          | -                            | -   | -                           |
| 121        | -                          | -             | -                          | -                            | -   | -                           |
| 122        | -                          | -             | -                          | -                            | -   | -                           |
| 123        | -                          | -             | -                          | -                            | -   | -                           |
| 124        | -                          | -             | -                          | -                            | -   | -                           |
| 125        | -                          | -             | -                          | -                            | -   | -                           |
| 126        | sd_card_detect_n_1_pad_in  | 0             | no                         | ledc_ls_sig_out_pad_out0     | 1'd1  | no                          |
| 127        | sd_card_detect_n_2_pad_in  | 0             | no                         | ledc_ls_sig_out_pad_out1     | 1'd1  | no                          |
| 128        | sd_card_int_n_1_pad_in     | 1             | no                         | ledc_ls_sig_out_pad_out2     | 1'd1  | no                          |
| 129        | sd_card_int_n_2_pad_in     | 1             | no                         | ledc_ls_sig_out_pad_out3     | 1'd1  | no                          |
| 130        | sd_card_write_prt_1_pad_in | 0             | no                         | ledc_ls_sig_out_pad_out4     | 1'd1  | no                          |
| 131        | sd_card_write_prt_2_pad_in | 0             | no                         | ledc_ls_sig_out_pad_out5     | 1'd1  | no                          |
| 132        | sd_data_strobe_1_pad_in    | 0             | no                         | ledc_ls_sig_out_pad_out6     | 1'd1  | no                          |
| 133        | sd_data_strobe_2_pad_in    | 0             | no                         | ledc_ls_sig_out_pad_out7     | 1'd1  | no                          |
| 134        | i3c_mst_scl_pad_in         | 1             | no                         | i3c_mst_scl_pad_out          | i3c_mst_scl_oe_pad_out                          | no                          |
| 135        | i3c_mst_sda_pad_in         | 1             | no                         | i3c_mst_sda_pad_out          | i3c_mst_sda_oe_pad_out                          | no                          |
| 136        | i3c_slv_scl_pad_in         | 1             | no                         | i3c_slv_scl_pad_out          | i3c_slv_scl_oe_pad_out                          | no                          |
| 137        | i3c_slv_sda_pad_in         | 1             | no                         | i3c_slv_sda_pad_out          | i3c_slv_sda_oe_pad_out                          | no                          |

| Signal No. | Input Signal               | Default Value | Direct Input via HP IO MUX | Output Signal                  | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|----------------------------|---------------|----------------------------|--------------------------------|---|-----------------------------|
| 138        | -                          | -             | -                          | i3c_mst_scl_pullup_en_pad_out  | 1'd1  | no                          |
| 139        | -                          | -             | -                          | i3c_mst_sda_pullup_en_pad_out  | 1'd1  | no                          |
| 140        | usb_jtag_tdo_bridge_pad_in | 0             | no                         | usb_jtag_tdi_bridge_pad_out    | 1'd1  | no                          |
| 141        | pcnt_sig_ch0_pad_in0       | 0             | no                         | usb_jtag_tms_bridge_pad_out    | 1'd1  | no                          |
| 142        | pcnt_sig_ch0_pad_in1       | 0             | no                         | usb_jtag_tck_bridge_pad_out    | 1'd1  | no                          |
| 143        | pcnt_sig_ch0_pad_in2       | 0             | no                         | usb_jtag_trst_bridge_pad_out   | 1'd1  | no                          |
| 144        | pcnt_sig_ch0_pad_in3       | 0             | no                         | lcd_cs_pad_out                 | 1'd1  | no                          |
| 145        | pcnt_sig_ch1_pad_in0       | 0             | no                         | lcd_dc_pad_out                 | 1'd1  | no                          |
| 146        | pcnt_sig_ch1_pad_in1       | 0             | no                         | sd_rst_n_1_pad_out             | 1'd1  | no                          |
| 147        | pcnt_sig_ch1_pad_in2       | 0             | no                         | sd_rst_n_2_pad_out             | 1'd1  | no                          |
| 148        | pcnt_sig_ch1_pad_in3       | 0             | no                         | sd_ccmd_od_pullup_en_n_pad_out | 1'd1  | no                          |
| 149        | pcnt_ctrl_ch0_pad_in0      | 0             | no                         | lcd_pclk_pad_out               | 1'd1  | no                          |
| 150        | pcnt_ctrl_ch0_pad_in1      | 0             | no                         | cam_clk_pad_out                | 1'd1  | no                          |
| 151        | pcnt_ctrl_ch0_pad_in2      | 0             | no                         | lcd_h_enable_pad_out           | 1'd1  | no                          |
| 152        | pcnt_ctrl_ch0_pad_in3      | 0             | no                         | lcd_h_sync_pad_out             | 1'd1  | no                          |
| 153        | pcnt_ctrl_ch1_pad_in0      | 0             | no                         | lcd_v_sync_pad_out             | 1'd1  | no                          |
| 154        | pcnt_ctrl_ch1_pad_in1      | 0             | no                         | lcd_data_out_pad_out0          | 1'd1  | no                          |
| 155        | pcnt_ctrl_ch1_pad_in2      | 0             | no                         | lcd_data_out_pad_out1          | 1'd1  | no                          |
| 156        | pcnt_ctrl_ch1_pad_in3      | 0             | no                         | lcd_data_out_pad_out2          | 1'd1  | no                          |
| 157        | -                          | -             | -                          | lcd_data_out_pad_out3          | 1'd1  | no                          |
| 158        | cam_pclk_pad_in            | 0             | no                         | lcd_data_out_pad_out4          | 1'd1  | no                          |
| 159        | cam_h_enable_pad_in        | 0             | no                         | lcd_data_out_pad_out5          | 1'd1  | no                          |
| 160        | cam_h_sync_pad_in          | 0             | no                         | lcd_data_out_pad_out6          | 1'd1  | no                          |
| 161        | cam_v_sync_pad_in          | 0             | no                         | lcd_data_out_pad_out7          | 1'd1  | no                          |
| 162        | cam_data_in_pad_in0        | 0             | no                         | lcd_data_out_pad_out8          | 1'd1  | no                          |
| 163        | cam_data_in_pad_in1        | 0             | no                         | lcd_data_out_pad_out9          | 1'd1  | no                          |

| Signal No. | Input Signal           | Default Value | Direct Input via HP IO MUX | Output Signal           | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|------------------------|---------------|----------------------------|-------------------------|---|-----------------------------|
| 164        | cam_data_in_pad_in2    | 0             | no                         | lcd_data_out_pad_out10  | 1'd1  | no                          |
| 165        | cam_data_in_pad_in3    | 0             | no                         | lcd_data_out_pad_out11  | 1'd1  | no                          |
| 166        | cam_data_in_pad_in4    | 0             | no                         | lcd_data_out_pad_out12  | 1'd1  | no                          |
| 167        | cam_data_in_pad_in5    | 0             | no                         | lcd_data_out_pad_out13  | 1'd1  | no                          |
| 168        | cam_data_in_pad_in6    | 0             | no                         | lcd_data_out_pad_out14  | 1'd1  | no                          |
| 169        | cam_data_in_pad_in7    | 0             | no                         | lcd_data_out_pad_out15  | 1'd1  | no                          |
| 170        | cam_data_in_pad_in8    | 0             | no                         | lcd_data_out_pad_out16  | 1'd1  | no                          |
| 171        | cam_data_in_pad_in9    | 0             | no                         | lcd_data_out_pad_out17  | 1'd1  | no                          |
| 172        | cam_data_in_pad_in10   | 0             | no                         | lcd_data_out_pad_out18  | 1'd1  | no                          |
| 173        | cam_data_in_pad_in11   | 0             | no                         | lcd_data_out_pad_out19  | 1'd1  | no                          |
| 174        | cam_data_in_pad_in12   | 0             | no                         | lcd_data_out_pad_out20  | 1'd1  | no                          |
| 175        | cam_data_in_pad_in13   | 0             | no                         | lcd_data_out_pad_out21  | 1'd1  | no                          |
| 176        | cam_data_in_pad_in14   | 0             | no                         | lcd_data_out_pad_out22  | 1'd1  | no                          |
| 177        | cam_data_in_pad_in15   | 0             | no                         | lcd_data_out_pad_out23  | 1'd1  | no                          |
| 178        | gmac_phy_rxdv_pad_in   | 0             | yes                        | gmac_phy_txen_pad_out   | 1'd1  | yes                         |
| 179        | gmac_phy_rxd0_pad_in   | 0             | yes                        | gmac_phy_txd0_pad_out   | 1'd1  | yes                         |
| 180        | gmac_phy_rxd1_pad_in   | 0             | yes                        | gmac_phy_txd1_pad_out   | 1'd1  | yes                         |
| 181        | gmac_phy_rxd2_pad_in   | 0             | no                         | gmac_phy_txd2_pad_out   | 1'd1  | no                          |
| 182        | gmac_phy_rxd3_pad_in   | 0             | no                         | gmac_phy_txd3_pad_out   | 1'd1  | no                          |
| 183        | gmac_phy_rxer_pad_in   | 0             | yes                        | gmac_phy_txer_pad_out   | 1'd1  | yes                         |
| 184        | gmac_rx_clk_pad_in     | 0             | no                         | -                       | -   | -                           |
| 185        | gmac_tx_clk_pad_in     | 0             | no                         | -                       | -   | -                           |
| 186        | parlio_rx_clk_pad_in   | 0             | no                         | parlio_rx_clk_pad_out   | 1'd1  | no                          |
| 187        | parlio_tx_clk_pad_in   | 0             | no                         | parlio_tx_clk_pad_out   | 1'd1  | no                          |
| 188        | parlio_rx_data0_pad_in | 0             | no                         | parlio_tx_data0_pad_out | 1'd1  | no                          |
| 189        | parlio_rx_data1_pad_in | 0             | no                         | parlio_tx_data1_pad_out | 1'd1  | no                          |
| 190        | parlio_rx_data2_pad_in | 0             | no                         | parlio_tx_data2_pad_out | 1'd1  | no                          |
| 191        | parlio_rx_data3_pad_in | 0             | no                         | parlio_tx_data3_pad_out | 1'd1  | no                          |

| Signal No. | Input Signal            | Default Value | Direct Input via HP IO MUX | Output Signal            | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|-------------------------|---------------|----------------------------|--------------------------|---|-----------------------------|
| 192        | parlio_rx_data4_pad_in  | 0             | no                         | parlio_tx_data4_pad_out  | 1'd1  | no                          |
| 193        | parlio_rx_data5_pad_in  | 0             | no                         | parlio_tx_data5_pad_out  | 1'd1  | no                          |
| 194        | parlio_rx_data6_pad_in  | 0             | no                         | parlio_tx_data6_pad_out  | 1'd1  | no                          |
| 195        | parlio_rx_data7_pad_in  | 0             | no                         | parlio_tx_data7_pad_out  | 1'd1  | no                          |
| 196        | parlio_rx_data8_pad_in  | 0             | no                         | parlio_tx_data8_pad_out  | 1'd1  | no                          |
| 197        | parlio_rx_data9_pad_in  | 0             | no                         | parlio_tx_data9_pad_out  | 1'd1  | no                          |
| 198        | parlio_rx_data10_pad_in | 0             | no                         | parlio_tx_data10_pad_out | 1'd1  | no                          |
| 199        | parlio_rx_data11_pad_in | 0             | no                         | parlio_tx_data11_pad_out | 1'd1  | no                          |
| 200        | parlio_rx_data12_pad_in | 0             | no                         | parlio_tx_data12_pad_out | 1'd1  | no                          |
| 201        | parlio_rx_data13_pad_in | 0             | no                         | parlio_tx_data13_pad_out | 1'd1  | no                          |
| 202        | parlio_rx_data14_pad_in | 0             | no                         | parlio_tx_data14_pad_out | 1'd1  | no                          |
| 203        | parlio_rx_data15_pad_in | 0             | no                         | parlio_tx_data15_pad_out | 1'd1  | no                          |
| 204        | -                       | -             | -                          | -                        | -   | -                           |
| 205        | -                       | -             | -                          | -                        | -   | -                           |
| 206        | -                       | -             | -                          | -                        | -   | -                           |
| 207        | -                       | -             | -                          | -                        | -   | -                           |
| 208        | -                       | -             | -                          | -                        | -   | -                           |
| 209        | -                       | -             | -                          | -                        | -   | -                           |
| 210        | -                       | -             | -                          | -                        | -   | -                           |
| 211        | -                       | -             | -                          | -                        | -   | -                           |
| 212        | -                       | -             | -                          | constant0_pad_out        | 1'd1  | no                          |
| 213        | -                       | -             | -                          | constant1_pad_out        | 1'd1  | no                          |
| 214        | core_gpio_in_pad_in0    | 0             | no                         | core_gpio_out_pad_out0   | core_gpio_oe_pad_out0                           | no                          |
| 215        | core_gpio_in_pad_in1    | 0             | no                         | core_gpio_out_pad_out1   | core_gpio_oe_pad_out1                           | no                          |
| 216        | core_gpio_in_pad_in2    | 0             | no                         | core_gpio_out_pad_out2   | core_gpio_oe_pad_out2                           | no                          |
| 217        | core_gpio_in_pad_in3    | 0             | no                         | core_gpio_out_pad_out3   | core_gpio_oe_pad_out3                           | no                          |
| 218        | core_gpio_in_pad_in4    | 0             | no                         | core_gpio_out_pad_out4   | core_gpio_oe_pad_out4                           | no                          |
| 219        | core_gpio_in_pad_in5    | 0             | no                         | core_gpio_out_pad_out5   | core_gpio_oe_pad_out5                           | no                          |

| Signal No. | Input Signal          | Default Value | Direct Input via HP IO MUX | Output Signal           | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|-----------------------|---------------|----------------------------|-------------------------|---|-----------------------------|
| 220        | core_gpio_in_pad_in6  | 0             | no                         | core_gpio_out_pad_out6  | core_gpio_oe_pad_out6                           | no                          |
| 221        | core_gpio_in_pad_in7  | 0             | no                         | core_gpio_out_pad_out7  | core_gpio_oe_pad_out7                           | no                          |
| 222        | core_gpio_in_pad_in8  | 0             | no                         | core_gpio_out_pad_out8  | core_gpio_oe_pad_out8                           | no                          |
| 223        | core_gpio_in_pad_in9  | 0             | no                         | core_gpio_out_pad_out9  | core_gpio_oe_pad_out9                           | no                          |
| 224        | core_gpio_in_pad_in10 | 0             | no                         | core_gpio_out_pad_out10 | core_gpio_oe_pad_out10                          | no                          |
| 225        | core_gpio_in_pad_in11 | 0             | no                         | core_gpio_out_pad_out11 | core_gpio_oe_pad_out11                          | no                          |
| 226        | core_gpio_in_pad_in12 | 0             | no                         | core_gpio_out_pad_out12 | core_gpio_oe_pad_out12                          | no                          |
| 227        | core_gpio_in_pad_in13 | 0             | no                         | core_gpio_out_pad_out13 | core_gpio_oe_pad_out13                          | no                          |
| 228        | core_gpio_in_pad_in14 | 0             | no                         | core_gpio_out_pad_out14 | core_gpio_oe_pad_out14                          | no                          |
| 229        | core_gpio_in_pad_in15 | 0             | no                         | core_gpio_out_pad_out15 | core_gpio_oe_pad_out15                          | no                          |
| 230        | core_gpio_in_pad_in16 | 0             | no                         | core_gpio_out_pad_out16 | core_gpio_oe_pad_out16                          | no                          |
| 231        | core_gpio_in_pad_in17 | 0             | no                         | core_gpio_out_pad_out17 | core_gpio_oe_pad_out17                          | no                          |
| 232        | core_gpio_in_pad_in18 | 0             | no                         | core_gpio_out_pad_out18 | core_gpio_oe_pad_out18                          | no                          |
| 233        | core_gpio_in_pad_in19 | 0             | no                         | core_gpio_out_pad_out19 | core_gpio_oe_pad_out19                          | no                          |
| 234        | core_gpio_in_pad_in20 | 0             | no                         | core_gpio_out_pad_out20 | core_gpio_oe_pad_out20                          | no                          |
| 235        | core_gpio_in_pad_in21 | 0             | no                         | core_gpio_out_pad_out21 | core_gpio_oe_pad_out21                          | no                          |
| 236        | core_gpio_in_pad_in22 | 0             | no                         | core_gpio_out_pad_out22 | core_gpio_oe_pad_out22                          | no                          |
| 237        | core_gpio_in_pad_in23 | 0             | no                         | core_gpio_out_pad_out23 | core_gpio_oe_pad_out23                          | no                          |
| 238        | core_gpio_in_pad_in24 | 0             | no                         | core_gpio_out_pad_out24 | core_gpio_oe_pad_out24                          | no                          |
| 239        | core_gpio_in_pad_in25 | 0             | no                         | core_gpio_out_pad_out25 | core_gpio_oe_pad_out25                          | no                          |
| 240        | core_gpio_in_pad_in26 | 0             | no                         | core_gpio_out_pad_out26 | core_gpio_oe_pad_out26                          | no                          |
| 241        | core_gpio_in_pad_in27 | 0             | no                         | core_gpio_out_pad_out27 | core_gpio_oe_pad_out27                          | no                          |
| 242        | core_gpio_in_pad_in28 | 0             | no                         | core_gpio_out_pad_out28 | core_gpio_oe_pad_out28                          | no                          |
| 243        | core_gpio_in_pad_in29 | 0             | no                         | core_gpio_out_pad_out29 | core_gpio_oe_pad_out29                          | no                          |
| 244        | core_gpio_in_pad_in30 | 0             | no                         | ana_comp0_out           | 1'd1  | no                          |
| 245        | core_gpio_in_pad_in31 | 0             | no                         | ana_comp1_out           | 1'd1  | no                          |
| 246        | rmt_sig_pad_in0       | 0             | no                         | rmt_sig_pad_out0        | 1'd1  | no                          |
| 247        | rmt_sig_pad_in1       | 0             | no                         | rmt_sig_pad_out1        | 1'd1  | no                          |

| Signal No. | Input Signal    | Default Value | Direct Input via HP IO MUX | Output Signal    | Output Enable Signal when GPIO_FUNCn_OE_SEL = 0 | Direct Output via HP IO MUX |
|------------|-----------------|---------------|----------------------------|------------------|---|-----------------------------|
| 248        | rmt_sig_pad_in2 | 0             | no                         | rmt_sig_pad_out2 | 1'd1  | no                          |
| 249        | rmt_sig_pad_in3 | 0             | no                         | rmt_sig_pad_out3 | 1'd1  | no                          |
| 250        | sig_in_func250  | 0             | no                         | sig_in_func250   | 1'd1  | no                          |
| 251        | sig_in_func251  | 0             | no                         | sig_in_func251   | 1'd1  | no                          |
| 252        | sig_in_func252  | 0             | no                         | sig_in_func252   | 1'd1  | no                          |
| 253        | sig_in_func253  | 0             | no                         | sig_in_func253   | 1'd1  | no                          |
| 254        | sig_in_func254  | 0             | no                         | sig_in_func254   | 1'd1  | no                          |
| 255        | sig_in_func255  | 0             | no                         | sig_in_func255   | 1'd1  | no                          |

## 8.13 LP Peripheral Signal List

Table 8.13-1 shows the peripheral input/output signals via LP GPIO matrix.

Please pay attention to the configuration of the bit `LP_GPIO_FUNC $n$ _OE_SEL`:

- `LP_GPIO_FUNC $n$ _OE_SEL` = 1: the output enable is controlled by the corresponding bit $n$  of `LP_GPIO_ENABLE_REG`:
  - `LP_GPIO_ENABLE_REG` = 0: output is disabled.
  - `LP_GPIO_ENABLE_REG` = 1: output is enabled.
- `LP_GPIO_FUNC $n$ _OE_SEL` = 0: use the output enable signal from peripheral, for example `lp_spi_clk_pad_oe` in the column “Output enable signal when `LP_GPIO_FUNC $n$ _OE_SEL` = 0” of Table 8.13-1. Note that the signals such as `lp_spi_clk_pad_oe` can be 1 (1'd1) or 0 (1'd0), depending on the configuration of corresponding peripherals. If it's 1'd1 in column “Output enable signal when `LP_GPIO_FUNC $n$ _OE_SEL` = 0”, it indicates that once `LP_GPIO_FUNC $n$ _OE_SEL` is cleared, the output signal is always enabled by default.

**Note:**

Signals are numbered consecutively, but not all signals are valid.

- Only the signals with a name assigned in the column “Input signal” in Table 8.13-1 are valid input signals.
- Only the signals with a name assigned in the column “Output signal” in Table 8.13-1 are valid output signals.

Table 8.13-1. Peripheral Signals via LP GPIO Matrix

| Signal No. | Input Signal        | Default value | Direct Input via LP IO MUX | Output Signal        | Output enable signal when LP_GPIO_FUNCn_OE_SEL = 0 | Direct Output via LP IO MUX |
|------------|---------------------|---------------|----------------------------|----------------------|--|-----------------------------|
| 0          | lp_i2c_scl_pad_in   | 1             | no                         | lp_i2c_scl_pad_out   | lp_i2c_scl_pad_oe                                  | no                          |
| 1          | lp_i2c_sda_pad_in   | 1             | no                         | lp_i2c_sda_pad_out   | lp_i2c_sda_pad_oe                                  | no                          |
| 2          | lp_uart_rxd_pad_in  | 0             | yes                        | lp_uart_txd_pad_out  | 1'd1   | yes                         |
| 3          | lp_uart_ctsn_pad_in | 1             | no                         | lp_uart_rtsn_pad_out | 1'd1   | no                          |
| 4          | lp_uart_dsrn_pad_in | 1             | no                         | lp_uart_dtrn_pad_out | 1'd1   | no                          |
| 5          | lp_spi_ck_pad_in    | 0             | no                         | lp_spi_ck_pad_out    | lp_spi_ck_pad_oe                                   | no                          |
| 6          | lp_spi_cs_pad_in    | 0             | no                         | lp_spi_cs_pad_out    | lp_spi_cs_pad_oe                                   | no                          |
| 7          | lp_spi_d_pad_in     | 0             | no                         | lp_spi_d_pad_out     | lp_spi_d_pad_oe                                    | no                          |
| 8          | lp_spi_q_pad_in     | 0             | no                         | lp_spi_q_pad_out     | lp_spi_q_pad_oe                                    | no                          |
| 9          | lp_i2s_i_bck_pad_in | 0             | no                         | lp_i2s_i_bck_pad_out | 1'd1   | no                          |
| 10         | lp_i2s_i_sd_pad_in  | 0             | no                         | lp_i2s_o_sd_pad_out  | 1'd1   | no                          |
| 11         | lp_i2s_i_ws_pad_in  | 0             | no                         | lp_i2s_i_ws_pad_out  | 1'd1   | no                          |
| 12         | lp_i2s_o_bck_pad_in | 0             | no                         | lp_i2s_o_bck_pad_out | 1'd1   | no                          |
| 13         | lp_i2s_o_ws_pad_in  | 0             | no                         | lp_i2s_o_ws_pad_out  | 1'd1   | no                          |
| 14         | -                   | -             | -                          | -                    | -  | -                           |
| 15         | -                   | -             | -                          | -                    | -  | -                           |
| 16         | -                   | -             | -                          | -                    | -  | -                           |
| 17         | -                   | -             | -                          | -                    | -  | -                           |
| 18         | -                   | -             | -                          | -                    | -  | -                           |
| 19         | -                   | -             | -                          | -                    | -  | -                           |
| 20         | -                   | -             | -                          | -                    | -  | -                           |
| 21         | -                   | -             | -                          | -                    | -  | -                           |
| 22         | -                   | -             | -                          | -                    | -  | -                           |
| 23         | -                   | -             | -                          | -                    | -  | -                           |



| Signal No. | Input Signal | Default value | Direct Input via LP IO MUX | Output Signal | Output enable signal when LP_GPIO_FUNCn_OE_SEL = 0 | Direct Output via LP IO MUX |
|------------|--------------|---------------|----------------------------|---------------|--|-----------------------------|
| 24         | -            | -             | -                          | -             | -  | -                           |
| 25         | -            | -             | -                          | -             | -  | -                           |
| 26         | -            | -             | -                          | -             | -  | -                           |
| 27         | -            | -             | -                          | -             | -  | -                           |
| 28         | -            | -             | -                          | -             | -  | -                           |
| 29         | -            | -             | -                          | -             | -  | -                           |
| 30         | -            | -             | -                          | -             | -  | -                           |
| 31         | -            | -             | -                          | -             | -  | -                           |

## 8.14 HP IO MUX Functions List

Table 8.14-1 shows the HP IO MUX functions and default states of each HP GPIO pin.

Table 8.14-1. HP IO MUX Pin Functions

| Name  | Function 0 | Function 1 | Function 2    | Function 3    | DRV | Reset | Notes |
|-------|------------|------------|---------------|---------------|-----|-------|-------|
| GPIO0 | GPIO0      | GPIO0      | -             | -             | 2   | 0     | R     |
| GPIO1 | GPIO1      | GPIO1      | -             | -             | 2   | 0     | R     |
| GPIO2 | MTCK       | GPIO2      | -             | -             | 2   | 1*    | R     |
| GPIO3 | MTDI       | GPIO3      | -             | -             | 2   | 1     | R     |
| GPIO4 | MTMS       | GPIO4      | -             | -             | 2   | 1     | R     |
| GPIO5 | MTDO       | GPIO5      | -             | -             | 2   | 0     | R     |
| GPIO6 | GPIO6      | GPIO6      | -             | SPI2_HOLD_PAD | 2   | 0     | R     |
| GPIO7 | GPIO7      | GPIO7      | -             | SPI2_CS_PAD   | 2   | 0     | R     |
| GPIO8 | GPIO8      | GPIO8      | UART0_RTS_PAD | SPI2_D_PAD    | 2   | 0     | R     |

Cont'd on next page

Table 8.14-1 – cont'd from previous page

| Name   | Function 0 | Function 1 | Function 2    | Function 3        | DRV | Reset | Notes  |
|--------|------------|------------|---------------|-------------------|-----|-------|--------|
| GPIO9  | GPIO9      | GPIO9      | UART0_CTS_PAD | SPI2_CK_PAD       | 2   | 0     | R      |
| GPIO10 | GPIO10     | GPIO10     | UART1_TXD_PAD | SPI2_Q_PAD        | 2   | 0     | R      |
| GPIO11 | GPIO11     | GPIO11     | UART1_RXD_PAD | SPI2_WP_PAD       | 2   | 0     | R      |
| GPIO12 | GPIO12     | GPIO12     | UART1_RTS_PAD | -                 | 2   | 0     | R      |
| GPIO13 | GPIO13     | GPIO13     | UART1_CTS_PAD | -                 | 2   | 0     | R      |
| GPIO14 | GPIO14     | GPIO14     | —             | -                 | 2   | 0     | R      |
| GPIO15 | GPIO15     | GPIO15     | —             | -                 | 2   | 0     | R      |
| GPIO16 | GPIO16     | GPIO16     | —             | -                 | 2   | 0     | R      |
| GPIO17 | GPIO17     | GPIO17     | —             | -                 | 2   | 0     | R      |
| GPIO18 | GPIO18     | GPIO18     | —             | -                 | 2   | 0     | R      |
| GPIO19 | GPIO19     | GPIO19     | —             | -                 | 2   | 0     | R      |
| GPIO20 | GPIO20     | GPIO20     | —             | -                 | 2   | 0     | R      |
| GPIO21 | GPIO21     | GPIO21     | —             | -                 | 2   | 0     | R      |
| GPIO22 | GPIO22     | GPIO22     | —             | -                 | 2   | 0     | R      |
| GPIO23 | GPIO23     | GPIO23     | —             | REF_50M_CLK_PAD   | 2   | 0     | R      |
| GPIO24 | GPIO24     | GPIO24     | —             | -                 | 3   | 0     | R, USB |
| GPIO25 | GPIO25     | GPIO25     | —             | -                 | 3   | 3*    | R, USB |
| GPIO26 | GPIO26     | GPIO26     | —             | -                 | 2   | 0     | R, USB |
| GPIO27 | GPIO27     | GPIO27     | —             | -                 | 2   | 0     | R, USB |
| GPIO28 | GPIO28     | GPIO28     | SPI2_CS_PAD   | GMAC_PHY_RXDV_PAD | 2   | 0     | —      |
| GPIO29 | GPIO29     | GPIO29     | SPI2_D_PAD    | GMAC_PHY_RXDO_PAD | 2   | 0     | —      |
| GPIO30 | GPIO30     | GPIO30     | SPI2_CK_PAD   | GMAC_PHY_RXD1_PAD | 2   | 0     | —      |
| GPIO31 | GPIO31     | GPIO31     | SPI2_Q_PAD    | GMAC_PHY_RXER_PAD | 2   | 0     | —      |
| GPIO32 | GPIO32     | GPIO32     | SPI2_HOLD_PAD | GMAC_RMII_CLK_PAD | 2   | 0     | —      |
| GPIO33 | GPIO33     | GPIO33     | SPI2_WP_PAD   | GMAC_PHY_TXEN_PAD | 2   | 0     | —      |
| GPIO34 | GPIO34     | GPIO34     | SPI2_IO4_PAD  | GMAC_PHY_TXDO_PAD | 2   | 0     | —      |
| GPIO35 | GPIO35     | GPIO35     | SPI2_IO5_PAD  | GMAC_PHY_TXD1_PAD | 2   | 0     | —      |

Cont'd on next page

Table 8.14-1 – cont'd from previous page

| Name   | Function 0      | Function 1 | Function 2   | Function 3        | DRV | Reset | Notes |
|--------|-----------------|------------|--------------|-------------------|-----|-------|-------|
| GPIO36 | GPIO36          | GPIO36     | SPI2_IO6_PAD | GMAC_PHY_TXER_PAD | 2   | 0     | —     |
| GPIO37 | UART0_TXD_PAD   | GPIO37     | SPI2_IO7_PAD | -                 | 2   | 5     | —     |
| GPIO38 | UART0_RXD_PAD   | GPIO38     | SPI2_DQS_PAD | -                 | 2   | 0     | —     |
| GPIO39 | SD1_CDATAB0_PAD | GPIO39     | —            | REF_50M_CLK_PAD   | 2   | 0     | —     |
| GPIO40 | SD1_CDATAB1_PAD | GPIO40     | —            | GMAC_PHY_TXEN_PAD | 2   | 0     | —     |
| GPIO41 | SD1_CDATAB2_PAD | GPIO41     | —            | GMAC_PHY_TXD0_PAD | 2   | 0     | —     |
| GPIO42 | SD1_CDATAB3_PAD | GPIO42     | —            | GMAC_PHY_TXD1_PAD | 2   | 0     | —     |
| GPIO43 | SD1_CCLK_PAD    | GPIO43     | —            | GMAC_PHY_TXER_PAD | 2   | 0     | —     |
| GPIO44 | SD1_CCMD_PAD    | GPIO44     | —            | GMAC_RMII_CLK_PAD | 2   | 0     | —     |
| GPIO45 | SD1_CDATAB4_PAD | GPIO45     | —            | GMAC_PHY_RXDV_PAD | 2   | 0     | —     |
| GPIO46 | SD1_CDATAB5_PAD | GPIO46     | —            | GMAC_PHY_RXD0_PAD | 2   | 0     | —     |
| GPIO47 | SD1_CDATAB6_PAD | GPIO47     | —            | GMAC_PHY_RXD1_PAD | 2   | 0     | —     |
| GPIO48 | SD1_CDATAB7_PAD | GPIO48     | —            | GMAC_PHY_RXER_PAD | 2   | 0     | —     |
| GPIO49 | GPIO49          | GPIO49     | —            | GMAC_PHY_TXEN_PAD | 2   | 0     | R     |
| GPIO50 | GPIO50          | GPIO50     | —            | GMAC_RMII_CLK_PAD | 2   | 0     | R     |
| GPIO51 | GPIO51          | GPIO51     | —            | GMAC_PHY_RXDV_PAD | 2   | 0     | R     |
| GPIO52 | GPIO52          | GPIO52     | —            | GMAC_PHY_RXD0_PAD | 2   | 0     | R     |
| GPIO53 | GPIO53          | GPIO53     | —            | GMAC_PHY_RXD1_PAD | 2   | 0     | R     |
| GPIO54 | GPIO54          | GPIO54     | —            | GMAC_PHY_RXER_PAD | 2   | 0     | R     |

## Drive Strength

“DRV” column shows the drive strength of each pin after reset:

- **0** - Drive current = ~5 mA
- **1** - Drive current = ~10 mA
- **2** - Drive current = ~20 mA
- **3** - Drive current = ~40 mA

## Reset

The default configuration of each pin after reset:

- **0** - input disabled, in high impedance state (IE = 0)
- **1** - input enabled, in high impedance state (IE = 1)
- **1\*** - When the value of eFuse bit EFUSE\_DIS\_PAD\_JTAG is  
0 (default), input enabled, pull-up resistor enabled (IE = 1, WPU = 1)  
1, input disabled, in high impedance state (IE = 1)
- **3\*** - input disabled, pull-up resistor enabled (IE = 0, USB\_PU = 1). See details in Notes.
- **5** - input disabled (IE = 0). Output is controlled by the peripheral of Function 0, and the default output is 1.

We recommend pulling high or low GPIO pins in high impedance state to avoid unnecessary power consumption. You may add pull-up and pull-down resistors in your PCB design, or enable internal pull-up and pull-down resistors during software initialization.

## Notes

- **R** - These pins have analog functions.
- **USB** - The pull-up value of a USB pin is controlled by the pin's pull-up value together with the USB pull-up value. If any of the two pull-up values is 1, the pin's pull-up resistor will be enabled.

### Notice:

In HP IO MUX, unused pins must be configured to GPIO function.

## 8.15 LP IO MUX Functions List

Table 8.15-1 shows the LP IO MUX functions of each GPIO pin. GPIO pins are default controlled by HP IO MUX, so Table 8.15-1 only show functions of LP IO MUX.

Table 8.15-1. LP IO MUX Pin Functions

| Name  | Function 0 | Function 1 |
|-------|------------|------------|
| GPIO0 | LP_GPIO0   | LP_GPIO0   |
| GPIO1 | LP_GPIO1   | LP_GPIO1   |
| GPIO2 | LP_GPIO2   | LP_GPIO2   |

| Name   | Function 0      | Function 1 |
|--------|-----------------|------------|
| GPIO3  | LP_GPIO3        | LP_GPIO3   |
| GPIO4  | LP_GPIO4        | LP_GPIO4   |
| GPIO5  | LP_GPIO5        | LP_GPIO5   |
| GPIO6  | LP_GPIO6        | LP_GPIO6   |
| GPIO7  | LP_GPIO7        | LP_GPIO7   |
| GPIO8  | LP_GPIO8        | LP_GPIO8   |
| GPIO9  | LP_GPIO9        | LP_GPIO9   |
| GPIO10 | LP_GPIO10       | LP_GPIO10  |
| GPIO11 | LP_GPIO11       | LP_GPIO11  |
| GPIO12 | LP_GPIO12       | LP_GPIO12  |
| GPIO13 | LP_GPIO13       | LP_GPIO13  |
| GPIO14 | LP_UART_TXD_PAD | LP_GPIO14  |
| GPIO15 | LP_UART_RXD_PAD | LP_GPIO15  |

**Notice:**

In LP IO MUX, unused pins must be configured to LP\_GPIO function.

## 8.16 GPIO Pin Analog Functions List

Table 8.16-1 shows the GPIO pins and their correspond analog functions.

**Table 8.16-1. GPIO Pin Analog Functions**

| Name   | Analog Function 0 | Analog Function 1 |
|--------|-------------------|-------------------|
| GPIO0  | XTAL_32K_N        | —                 |
| GPIO1  | XTAL_32K_P        | —                 |
| GPIO2  | TOUCH_CHANNEL0    | —                 |
| GPIO3  | TOUCH_CHANNEL1    | —                 |
| GPIO4  | TOUCH_CHANNEL2    | —                 |
| GPIO5  | TOUCH_CHANNEL3    | —                 |
| GPIO6  | TOUCH_CHANNEL4    | —                 |
| GPIO7  | TOUCH_CHANNEL5    | —                 |
| GPIO8  | TOUCH_CHANNEL6    | —                 |
| GPIO9  | TOUCH_CHANNEL7    | —                 |
| GPIO10 | TOUCH_CHANNEL8    | —                 |
| GPIO11 | TOUCH_CHANNEL9    | —                 |
| GPIO12 | TOUCH_CHANNEL10   | —                 |
| GPIO13 | TOUCH_CHANNEL11   | —                 |
| GPIO14 | TOUCH_CHANNEL12   | —                 |
| GPIO15 | TOUCH_CHANNEL13   | —                 |
| GPIO16 | ADC1_CHANNEL0     | —                 |
| GPIO17 | ADC1_CHANNEL1     | —                 |

| Name   | Analog Function 0 | Analog Function 1 |
|--------|-------------------|-------------------|
| GPIO18 | ADC1_CHANNEL2     | —                 |
| GPIO19 | ADC1_CHANNEL3     | —                 |
| GPIO20 | ADC1_CHANNEL4     | —                 |
| GPIO21 | ADC1_CHANNEL5     | —                 |
| GPIO22 | ADC1_CHANNEL6     | —                 |
| GPIO23 | ADC1_CHANNEL7     | —                 |
| GPIO24 | USB1P1_N0         | —                 |
| GPIO25 | USB1P1_PO         | —                 |
| GPIO26 | USB1P1_N1         | —                 |
| GPIO27 | USB1P1_P1         | —                 |
| GPIO49 | ADC2_CHANNEL2     | —                 |
| GPIO50 | ADC2_CHANNEL3     | —                 |
| GPIO51 | ADC2_CHANNEL4     | ANA_COMP0         |
| GPIO52 | ADC2_CHANNEL5     | ANA_COMP0         |
| GPIO53 | ADC2_CHANNEL6     | ANA_COMP1         |
| GPIO54 | ADC2_CHANNEL7     | ANA_COMP1         |

## 8.17 Event Task Matrix Function

In ESP32-P4, GPIO supports ETM function, that is, the ETM task of GPIO can be triggered by the ETM event of any peripheral, or the ETM task of any peripheral can be triggered by the ETM event of GPIO. For more details about ETM, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#). Only ETM tasks and ETM events related to GPIO are introduced here.

The GPIO ETM provides eight task channels  $x$  (0 ~ 7). The ETM tasks that each task channel can receive are:

- GPIO\_TASK\_CH $x$ \_SET: GPIO goes high when triggered.
- GPIO\_TASK\_CH $x$ \_CLEAR: GPIO goes low when triggered.
- GPIO\_TASK\_CH $x$ \_TOGGLE: GPIO toggles level when triggered.

Below is an example to configure task channel  $x$  to control GPIO $y$ :

- Configure [IO\\_MUX\\_GPIO \$y\$ \\_MCU\\_SEL](#) to 1, to select Function 1 listed in Table 8.14-1.
- Configure [GPIO\\_ENABLE\\_REG \$\[y\]\$](#)  to 1.
- Configure [GPIO\\_EXT\\_ETM\\_TASK\\_GPIO \$y\$ \\_SEL](#) to  $x$ .
- Set [GPIO\\_EXT\\_ETM\\_TASK\\_GPIO \$y\$ \\_EN](#), to enable ETM task channel  $x$  to control GPIO $y$ .

### Note:

- One task channel can be selected by one or more GPIOs.
- When two or three of the signals GPIO\_TASK\_CH $x$ \_SET, GPIO\_TASK\_CH $x$ \_CLEAR, and GPIO\_TASK\_CH $x$ \_TOGGLE of the task channel  $x$  selected by GPIO $y$  are valid at the same time, then GPIO\_TASK\_CH $x$ \_SET has the highest priority, GPIO\_TASK\_CH $x$ \_CLEAR takes the second higher priority, and GPIO\_TASK\_CH $x$ \_TOGGLE has the

lowest priority.

- When GPIO $y$  is controlled by ETM task channel, the values of `GPIO_OUT_REG`, `GPIO_FUNC $n$ _OUT_INV_SEL`, and `GPIO_FUNC $n$ _OUT_SEL` may be modified by the hardware. For such reason, it's recommended to reconfigure these registers when the GPIO is free from the control of ETM task channel.

GPIO has eight event channels, and the ETM events that each event channel can generate are:

- `GPIO_EVT_CH $x$ _RISE_EDGE`: Indicates that the output signal of the corresponding GPIO Filter (see Figure 8.3-1) has a rising edge.
- `GPIO_EVT_CH $x$ _FALL_EDGE`: Indicates that the output signal of the corresponding GPIO Filter (see Figure 8.3-1) has a falling edge.
- `GPIO_EVT_CH $x$ _ANY_EDGE`: Indicates that the output signal of the corresponding GPIO Filter (see Figure 8.3-1) is reversed.

The specific configuration of the event channel is as follows:

- Set `GPIO_EXT_ETM_CH $x$ _EVENT_EN` to enable event channel  $x$  (0 ~ 7).
- Configure `GPIO_EXT_ETM_CH $x$ _EVENT_SEL` to  $y$  (0 ~ 54), i.e., select one from the 55 GPIOs.

**Note:**

One GPIO can be selected by one or more event channels.

In specific applications, GPIO ETM events can be used to trigger GPIO ETM tasks. For example, event channel 0 selects GPIO0, GPIO1 selects task channel 0, and the `GPIO_EVT_CH0_RISE_EDGE` event is used to trigger the `GPIO_TASK_CH0_TOGGLE` task. When a square wave signal is input to the chip through GPIO0, the chip outputs a square wave signal with a frequency divided by 2 through GPIO1.

## 8.18 Interrupts

ESP32-P4's HP IO MUX and HP GPIO matrix can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- `GPIO_INTRO`
- `GPIO_INTR1`
- `GPIO_INTR2`
- `GPIO_INTR3`
- `GPIO_PAD_COMP_INTR`

There are several internal interrupt sources from HP IO MUX and HP GPIO matrix that can generate the above interrupt signals. The interrupt sources from HP IO MUX and HP GPIO matrix are listed with their trigger conditions and the resulted interrupt signals in Table 8.18-1. For more detailed information about `GPIO_PAD_COMP_INTR`, please refer to Chapter 58 [Analog Voltage Comparator](#).

**Table 8.18-1. HP IO MUX and HP GPIO Matrix's Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition | Interrupt Signal |
|---------------------------|-------------------|------------------|
|---------------------------|-------------------|------------------|

|            |   |            |
|------------|---|------------|
| GPIO_INTRO | GPIO_STATUS_INTERRUPT[n] & GPIO_PINn_INT_ENA[0] (n: 0 ~ 31)     | GPIO_INTRO |
| GPIO_INTRO | GPIO_STATUS1_INTERRUPT[n] & GPIO_PINn+32_INT_ENA[0] (n: 0 ~ 22) | GPIO_INTRO |
| GPIO_INTR1 | GPIO_STATUS_INTERRUPT[n] & GPIO_PINn_INT_ENA[1] (n: 0 ~ 31)     | GPIO_INTR1 |
| GPIO_INTR1 | GPIO_STATUS1_INTERRUPT[n] & GPIO_PINn+32_INT_ENA[1] (n: 0 ~ 22) | GPIO_INTR1 |
| GPIO_INTR2 | GPIO_STATUS_INTERRUPT[n] & GPIO_PINn_INT_ENA[3] (n: 0 ~ 31)     | GPIO_INTR2 |
| GPIO_INTR2 | GPIO_STATUS1_INTERRUPT[n] & GPIO_PINn+32_INT_ENA[3] (n: 0 ~ 22) | GPIO_INTR2 |
| GPIO_INTR3 | GPIO_STATUS_INTERRUPT[n] & GPIO_PINn_INT_ENA[4] (n: 0 ~ 31)     | GPIO_INTR3 |
| GPIO_INTR3 | GPIO_STATUS1_INTERRUPT[n] & GPIO_PINn+32_INT_ENA[4] (n: 0 ~ 22) | GPIO_INTR3 |

ESP32-P4's LP IO MUX and GPIO matrix can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- LP\_GPIO\_INTRO

The interrupt source from LP IO MUX and LP GPIO matrix are listed with their trigger conditions and the resulted interrupt signals in Table 8.18-2.

Table 8.18-2. LP IO MUX and LP GPIO Matrix's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition                  | Interrupt Signal |
|---------------------------|------------------------------------|------------------|
| LP_GPIO_INTR              | LP_GPIO_STATUS_DATA[n] (n: 0 ~ 15) | LP_GPIO_INTR     |

## 8.19 Register Summary

### 8.19.1 HP GPIO Matrix Register Summary

The addresses in this section are relative to HP GPIO matrix base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name                               | Description                          | Address | Access     |
|------------------------------------|--------------------------------------|---------|------------|
| <b>Configuration Registers</b>     |                                      |         |            |
| <a href="#">GPIO_OUT_REG</a>       | GPIO0 ~ GPIO31 output register       | 0x0004  | R/W/SC/WTC |
| <a href="#">GPIO_OUT_W1TS_REG</a>  | GPIO0 ~ GPIO31 output set register   | 0x0008  | WT         |
| <a href="#">GPIO_OUT_W1TC_REG</a>  | GPIO0 ~ GPIO31 output clear register | 0x000C  | WT         |
| <a href="#">GPIO_OUT1_REG</a>      | GPIO32 ~ GPIO56 output register      | 0x0010  | R/W/SC/WTC |
| <a href="#">GPIO_OUT1_W1TS_REG</a> | GPIO32 ~ GPIO56 output set register  | 0x0014  | WT         |



| Name  | Description                                     | Address | Access  |
|---|---|---------|---------|
| <a href="#">GPIO_OUT1_W1TC_REG</a>          | GPIO32 ~ GPIO56 output clear register           | 0x0018  | WT      |
| <a href="#">GPIO_ENABLE_REG</a>             | GPIO0 ~ GPIO31 output enable register           | 0x0020  | R/W/WTC |
| <a href="#">GPIO_ENABLE_W1TS_REG</a>        | GPIO0 ~ GPIO31 output enable set register       | 0x0024  | WT      |
| <a href="#">GPIO_ENABLE_W1TC_REG</a>        | GPIO0 ~ GPIO31 output enable clear register     | 0x0028  | WT      |
| <a href="#">GPIO_ENABLE1_REG</a>            | GPIO32 ~ GPIO56 output enable register          | 0x002C  | R/W/WTC |
| <a href="#">GPIO_ENABLE1_W1TS_REG</a>       | GPIO32 ~ GPIO56 output enable set register      | 0x0030  | WT      |
| <a href="#">GPIO_ENABLE1_W1TC_REG</a>       | GPIO32 ~ GPIO56 output enable clear register    | 0x0034  | WT      |
| <a href="#">GPIO_STRAP_REG</a>              | Strapping pin register                          | 0x0038  | RO      |
| <a href="#">GPIO_IN_REG</a>                 | GPIO0 ~ GPIO31 input register                   | 0x003C  | RO      |
| <a href="#">GPIO_IN1_REG</a>                | GPIO32 ~ GPIO56 input register                  | 0x0040  | RO      |
| <a href="#">GPIO_STATUS_REG</a>             | GPIO0 ~ GPIO31 interrupt status register        | 0x0044  | R/W/WTC |
| <a href="#">GPIO_STATUS_W1TS_REG</a>        | GPIO0 ~ GPIO31 interrupt status set register    | 0x0048  | WT      |
| <a href="#">GPIO_STATUS_W1TC_REG</a>        | GPIO0 ~ GPIO31 interrupt status clear register  | 0x004C  | WT      |
| <a href="#">GPIO_STATUS1_REG</a>            | GPIO32 ~ GPIO56 interrupt status register       | 0x0050  | R/W/WTC |
| <a href="#">GPIO_STATUS1_W1TS_REG</a>       | GPIO32 ~ GPIO56 interrupt status set register   | 0x0054  | WT      |
| <a href="#">GPIO_STATUS1_W1TC_REG</a>       | GPIO32 ~ GPIO56 interrupt status clear register | 0x0058  | WT      |
| <a href="#">GPIO_INTR_0_REG</a>             | GPIO0 ~ GPIO31 interrupt 0 status register      | 0x005C  | RO      |
| <a href="#">GPIO_INTR1_0_REG</a>            | GPIO32 ~ GPIO56 interrupt 0 status register     | 0x0060  | RO      |
| <a href="#">GPIO_INTR_1_REG</a>             | GPIO0 ~ GPIO31 interrupt 1 status register      | 0x0064  | RO      |
| <a href="#">GPIO_INTR1_1_REG</a>            | GPIO32 ~ GPIO56 interrupt 1 status register     | 0x0068  | RO      |
| <a href="#">GPIO_STATUS_NEXT_REG</a>        | GPIO0 ~ GPIO31 interrupt source register        | 0x006C  | RO      |
| <a href="#">GPIO_STATUS_NEXT1_REG</a>       | GPIO32 ~ GPIO56 interrupt source register       | 0x0070  | RO      |
| <a href="#">GPIO_PIN0_REG</a>               | GPIO pin0 configuration register                | 0x0074  | R/W     |
| <a href="#">GPIO_PIN1_REG</a>               | GPIO pin1 configuration register                | 0x0078  | R/W     |
| <a href="#">GPIO_PIN2_REG</a>               | GPIO pin2 configuration register                | 0x007C  | R/W     |
| <a href="#">GPIO_PIN3_REG</a>               | GPIO pin3 configuration register                | 0x0080  | R/W     |
| <a href="#">GPIO_PIN4_REG</a>               | GPIO pin4 configuration register                | 0x0084  | R/W     |
| ...   | ...   | ...     | ...     |
| <a href="#">GPIO_PIN54_REG</a>              | GPIO pin54 configuration register               | 0x014C  | R/W     |
| <a href="#">GPIO_PIN55_REG</a>              | GPIO pin55 configuration register               | 0x0150  | R/W     |
| <a href="#">GPIO_PIN56_REG</a>              | GPIO pin56 configuration register               | 0x0154  | R/W     |
| <a href="#">GPIO_FUNC1_IN_SEL_CFG_REG</a>   | Input signal 1 configuration register           | 0x015C  | R/W     |
| <a href="#">GPIO_FUNC2_IN_SEL_CFG_REG</a>   | Input signal 2 configuration register           | 0x0160  | R/W     |
| <a href="#">GPIO_FUNC3_IN_SEL_CFG_REG</a>   | Input signal 3 configuration register           | 0x0164  | R/W     |
| ...   | ...   | ...     | ...     |
| <a href="#">GPIO_FUNC253_IN_SEL_CFG_REG</a> | Input signal 253 configuration register         | 0x054C  | R/W     |
| <a href="#">GPIO_FUNC254_IN_SEL_CFG_REG</a> | Input signal 254 configuration register         | 0x0550  | R/W     |
| <a href="#">GPIO_FUNC255_IN_SEL_CFG_REG</a> | Input signal 255 configuration register         | 0x0554  | R/W     |
| <a href="#">GPIO_FUNC0_OUT_SEL_CFG_REG</a>  | GPIO0 output configuration register             | 0x0558  | varies  |
| <a href="#">GPIO_FUNC1_OUT_SEL_CFG_REG</a>  | GPIO1 output configuration register             | 0x055C  | varies  |
| <a href="#">GPIO_FUNC2_OUT_SEL_CFG_REG</a>  | GPIO2 output configuration register             | 0x0560  | varies  |
| <a href="#">GPIO_FUNC3_OUT_SEL_CFG_REG</a>  | GPIO3 output configuration register             | 0x0564  | varies  |
| ...   | ...   | ...     | ...     |

| Name  | Description                                     | Address | Access   |
|---|---|---------|----------|
| <a href="#">GPIO_FUNC53_OUT_SEL_CFG_REG</a>   | GPIO53 output configuration register            | 0x062C  | varies   |
| <a href="#">GPIO_FUNC54_OUT_SEL_CFG_REG</a>   | GPIO54 output configuration register            | 0x0630  | varies   |
| <a href="#">GPIO_FUNC55_OUT_SEL_CFG_REG</a>   | GPIO55 output configuration register            | 0x0634  | varies   |
| <a href="#">GPIO_FUNC56_OUT_SEL_CFG_REG</a>   | GPIO56 output configuration register            | 0x0638  | varies   |
| <a href="#">GPIO_INTR_2_REG</a>               | GPIO00 ~ GPIO31 interrupt 2 status register     | 0x063C  | RO       |
| <a href="#">GPIO_INTR1_2_REG</a>              | GPIO32 ~ GPIO56 interrupt 2 status register     | 0x0640  | RO       |
| <a href="#">GPIO_INTR_3_REG</a>               | GPIO00 ~ GPIO31 interrupt 3 status register     | 0x0644  | RO       |
| <a href="#">GPIO_INTR1_3_REG</a>              | GPIO32 ~ GPIO56 interrupt 3 status register     | 0x0648  | RO       |
| <a href="#">GPIO_CLOCK_GATE_REG</a>           | GPIO clock gate register                        | 0x064C  | R/W      |
| <a href="#">GPIO_ZERO_DET0_FILTER_CNT_REG</a> | GPIO analog comparator zero detect filter count | 0x0710  | R/W      |
| <a href="#">GPIO_ZERO_DET1_FILTER_CNT_REG</a> | GPIO analog comparator zero detect filter count | 0x0714  | R/W      |
| <b>GPIO Interrupt Registers</b>               |   |         |          |
| <a href="#">GPIO_INT_RAW_REG</a>              | Analog comparator interrupt raw register        | 0x0700  | R/WTC/SS |
| <a href="#">GPIO_INT_ST_REG</a>               | Analog comparator interrupt status register     | 0x0704  | RO       |
| <a href="#">GPIO_INT_ENA_REG</a>              | Analog comparator interrupt enable register     | 0x0708  | R/W      |
| <a href="#">GPIO_INT_CLR_REG</a>              | Analog comparator interrupt clear register      | 0x070C  | WT       |
| <b>Version Register</b>                       |   |         |          |
| <a href="#">GPIO_DATE_REG</a>                 | Version control register                        | 0x07FC  | R/W      |

## 8.19.2 HP IO MUX Register Summary

The addresses in this section are relative to the HP IO MUX base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                  | Description                              | Address | Access |
|---------------------------------------|--|---------|--------|
| <b>IO MUX Configuration Registers</b> |  |         |        |
| <a href="#">IO_MUX_GPIO0_REG</a>      | IO MUX configuration register for GPIO0  | 0x0004  | R/W    |
| <a href="#">IO_MUX_GPIO1_REG</a>      | IO MUX configuration register for GPIO1  | 0x0008  | R/W    |
| <a href="#">IO_MUX_GPIO2_REG</a>      | IO MUX configuration register for GPIO2  | 0x000C  | R/W    |
| <a href="#">IO_MUX_GPIO3_REG</a>      | IO MUX configuration register for GPIO3  | 0x0010  | R/W    |
| <a href="#">IO_MUX_GPIO4_REG</a>      | IO MUX configuration register for GPIO4  | 0x0014  | R/W    |
| <a href="#">IO_MUX_GPIO5_REG</a>      | IO MUX configuration register for GPIO5  | 0x0018  | R/W    |
| <a href="#">IO_MUX_GPIO6_REG</a>      | IO MUX configuration register for GPIO6  | 0x001C  | R/W    |
| <a href="#">IO_MUX_GPIO7_REG</a>      | IO MUX configuration register for GPIO7  | 0x0020  | R/W    |
| <a href="#">IO_MUX_GPIO8_REG</a>      | IO MUX configuration register for GPIO8  | 0x0024  | R/W    |
| <a href="#">IO_MUX_GPIO9_REG</a>      | IO MUX configuration register for GPIO9  | 0x0028  | R/W    |
| <a href="#">IO_MUX_GPIO10_REG</a>     | IO MUX configuration register for GPIO10 | 0x002C  | R/W    |
| <a href="#">IO_MUX_GPIO11_REG</a>     | IO MUX configuration register for GPIO11 | 0x0030  | R/W    |
| <a href="#">IO_MUX_GPIO12_REG</a>     | IO MUX configuration register for GPIO12 | 0x0034  | R/W    |
| <a href="#">IO_MUX_GPIO13_REG</a>     | IO MUX configuration register for GPIO13 | 0x0038  | R/W    |
| <a href="#">IO_MUX_GPIO14_REG</a>     | IO MUX configuration register for GPIO14 | 0x003C  | R/W    |
| <a href="#">IO_MUX_GPIO15_REG</a>     | IO MUX configuration register for GPIO15 | 0x0040  | R/W    |

| Name                              | Description                              | Address | Access |
|-----------------------------------|--|---------|--------|
| <a href="#">IO_MUX_GPIO16_REG</a> | IO MUX configuration register for GPIO16 | 0x0044  | R/W    |
| <a href="#">IO_MUX_GPIO17_REG</a> | IO MUX configuration register for GPIO17 | 0x0048  | R/W    |
| <a href="#">IO_MUX_GPIO18_REG</a> | IO MUX configuration register for GPIO18 | 0x004C  | R/W    |
| <a href="#">IO_MUX_GPIO19_REG</a> | IO MUX configuration register for GPIO19 | 0x0050  | R/W    |
| <a href="#">IO_MUX_GPIO20_REG</a> | IO MUX configuration register for GPIO20 | 0x0054  | R/W    |
| <a href="#">IO_MUX_GPIO21_REG</a> | IO MUX configuration register for GPIO21 | 0x0058  | R/W    |
| <a href="#">IO_MUX_GPIO22_REG</a> | IO MUX configuration register for GPIO22 | 0x005C  | R/W    |
| <a href="#">IO_MUX_GPIO23_REG</a> | IO MUX configuration register for GPIO23 | 0x0060  | R/W    |
| <a href="#">IO_MUX_GPIO24_REG</a> | IO MUX configuration register for GPIO24 | 0x0064  | R/W    |
| <a href="#">IO_MUX_GPIO25_REG</a> | IO MUX configuration register for GPIO25 | 0x0068  | R/W    |
| <a href="#">IO_MUX_GPIO26_REG</a> | IO MUX configuration register for GPIO26 | 0x006C  | R/W    |
| <a href="#">IO_MUX_GPIO27_REG</a> | IO MUX configuration register for GPIO27 | 0x0070  | R/W    |
| <a href="#">IO_MUX_GPIO28_REG</a> | IO MUX configuration register for GPIO28 | 0x0074  | R/W    |
| <a href="#">IO_MUX_GPIO29_REG</a> | IO MUX configuration register for GPIO29 | 0x0078  | R/W    |
| <a href="#">IO_MUX_GPIO30_REG</a> | IO MUX configuration register for GPIO30 | 0x007C  | R/W    |
| <a href="#">IO_MUX_GPIO31_REG</a> | IO MUX configuration register for GPIO31 | 0x0080  | R/W    |
| <a href="#">IO_MUX_GPIO32_REG</a> | IO MUX configuration register for GPIO32 | 0x0084  | R/W    |
| <a href="#">IO_MUX_GPIO33_REG</a> | IO MUX configuration register for GPIO33 | 0x0088  | R/W    |
| <a href="#">IO_MUX_GPIO34_REG</a> | IO MUX configuration register for GPIO34 | 0x008C  | R/W    |
| <a href="#">IO_MUX_GPIO35_REG</a> | IO MUX configuration register for GPIO35 | 0x0090  | R/W    |
| <a href="#">IO_MUX_GPIO36_REG</a> | IO MUX configuration register for GPIO36 | 0x0094  | R/W    |
| <a href="#">IO_MUX_GPIO37_REG</a> | IO MUX configuration register for GPIO37 | 0x0098  | R/W    |
| <a href="#">IO_MUX_GPIO38_REG</a> | IO MUX configuration register for GPIO38 | 0x009C  | R/W    |
| <a href="#">IO_MUX_GPIO39_REG</a> | IO MUX configuration register for GPIO39 | 0x00A0  | R/W    |
| <a href="#">IO_MUX_GPIO40_REG</a> | IO MUX configuration register for GPIO40 | 0x00A4  | R/W    |
| <a href="#">IO_MUX_GPIO41_REG</a> | IO MUX configuration register for GPIO41 | 0x00A8  | R/W    |
| <a href="#">IO_MUX_GPIO42_REG</a> | IO MUX configuration register for GPIO42 | 0x00AC  | R/W    |
| <a href="#">IO_MUX_GPIO43_REG</a> | IO MUX configuration register for GPIO43 | 0x00B0  | R/W    |
| <a href="#">IO_MUX_GPIO44_REG</a> | IO MUX configuration register for GPIO44 | 0x00B4  | R/W    |
| <a href="#">IO_MUX_GPIO45_REG</a> | IO MUX configuration register for GPIO45 | 0x00B8  | R/W    |
| <a href="#">IO_MUX_GPIO46_REG</a> | IO MUX configuration register for GPIO46 | 0x00BC  | R/W    |
| <a href="#">IO_MUX_GPIO47_REG</a> | IO MUX configuration register for GPIO47 | 0x00C0  | R/W    |
| <a href="#">IO_MUX_GPIO48_REG</a> | IO MUX configuration register for GPIO48 | 0x00C4  | R/W    |
| <a href="#">IO_MUX_GPIO49_REG</a> | IO MUX configuration register for GPIO49 | 0x00C8  | R/W    |
| <a href="#">IO_MUX_GPIO50_REG</a> | IO MUX configuration register for GPIO50 | 0x00CC  | R/W    |
| <a href="#">IO_MUX_GPIO51_REG</a> | IO MUX configuration register for GPIO51 | 0x00D0  | R/W    |
| <a href="#">IO_MUX_GPIO52_REG</a> | IO MUX configuration register for GPIO52 | 0x00D4  | R/W    |
| <a href="#">IO_MUX_GPIO53_REG</a> | IO MUX configuration register for GPIO53 | 0x00D8  | R/W    |
| <a href="#">IO_MUX_GPIO54_REG</a> | IO MUX configuration register for GPIO54 | 0x00DC  | R/W    |
| <b>Version Register</b>           |  |         |        |
| <a href="#">IO_MUX_DATE_REG</a>   | Version control register                 | 0x0104  | R/W    |

### 8.19.3 GPIO EXT Register Summary

GPIO EXT registers consist of SDM registers, Glitch Filter registers, and ETM registers.

The addresses in this section are relative to (HP GPIO matrix base address + 0x0F00). GPIO base address is provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>SDM Configuration Registers</b>             |  |         |        |
| <a href="#">GPIO_EXT_SIGMADELTA0_REG</a>       | SDM channel 0 duty cycle configuration register    | 0x0000  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA1_REG</a>       | SDM channel 1 duty cycle configuration register    | 0x0004  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA2_REG</a>       | SDM channel 2 duty cycle configuration register    | 0x0008  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA3_REG</a>       | SDM channel 3 duty cycle configuration register    | 0x000C  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA4_REG</a>       | SDM channel 4 duty cycle configuration register    | 0x0010  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA5_REG</a>       | SDM channel 5 duty cycle configuration register    | 0x0014  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA6_REG</a>       | SDM channel 6 duty cycle configuration register    | 0x0018  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA7_REG</a>       | SDM channel 7 duty cycle configuration register    | 0x001C  | R/W    |
| <a href="#">GPIO_EXT_SIGMADELTA_MISC_REG</a>   | MISC register                                      | 0x0024  | R/W    |
| <b>Glitch Filter Configuration Registers</b>   |  |         |        |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH0_REG</a> | Glitch Filter configuration register for channel 0 | 0x0030  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH1_REG</a> | Glitch Filter configuration register for channel 1 | 0x0034  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH2_REG</a> | Glitch Filter configuration register for channel 2 | 0x0038  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH3_REG</a> | Glitch Filter configuration register for channel 3 | 0x003C  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH4_REG</a> | Glitch Filter configuration register for channel 4 | 0x0040  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH5_REG</a> | Glitch Filter configuration register for channel 5 | 0x0044  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH6_REG</a> | Glitch Filter configuration register for channel 6 | 0x0048  | R/W    |
| <a href="#">GPIO_EXT_GLITCH_FILTER_CH7_REG</a> | Glitch Filter configuration register for channel 7 | 0x004C  | R/W    |
| <b>ETM Configuration Registers</b>             |  |         |        |
| <a href="#">GPIO_EXT_ETM_EVENT_CH0_CFG_REG</a> | ETM configuration register for channel 0           | 0x0060  | R/W    |

| Name   | Description                              | Address | Access |
|--|--|---------|--------|
| <a href="#">GPIO_EXT_ETM_EVENT_CH1_CFG_REG</a> | ETM configuration register for channel 1 | 0x0064  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH2_CFG_REG</a> | ETM configuration register for channel 2 | 0x0068  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH3_CFG_REG</a> | ETM configuration register for channel 3 | 0x006C  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH4_CFG_REG</a> | ETM configuration register for channel 4 | 0x0070  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH5_CFG_REG</a> | ETM configuration register for channel 5 | 0x0074  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH6_CFG_REG</a> | ETM configuration register for channel 6 | 0x0078  | R/W    |
| <a href="#">GPIO_EXT_ETM_EVENT_CH7_CFG_REG</a> | ETM configuration register for channel 7 | 0x007C  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P0_CFG_REG</a>   | GPIO selection register 0 for ETM        | 0x00A0  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P1_CFG_REG</a>   | GPIO selection register 1 for ETM        | 0x00A4  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P2_CFG_REG</a>   | GPIO selection register 2 for ETM        | 0x00A8  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P3_CFG_REG</a>   | GPIO selection register 3 for ETM        | 0x00AC  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P4_CFG_REG</a>   | GPIO selection register 4 for ETM        | 0x00B0  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P5_CFG_REG</a>   | GPIO selection register 5 for ETM        | 0x00B4  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P6_CFG_REG</a>   | GPIO selection register 6 for ETM        | 0x00B8  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P7_CFG_REG</a>   | GPIO selection register 7 for ETM        | 0x00BC  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P8_CFG_REG</a>   | GPIO selection register 8 for ETM        | 0x00C0  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P9_CFG_REG</a>   | GPIO selection register 9 for ETM        | 0x00C4  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P10_CFG_REG</a>  | GPIO selection register 10 for ETM       | 0x00C8  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P11_CFG_REG</a>  | GPIO selection register 11 for ETM       | 0x00CC  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P12_CFG_REG</a>  | GPIO selection register 12 for ETM       | 0x00D0  | R/W    |
| <a href="#">GPIO_EXT_ETM_TASK_P13_CFG_REG</a>  | GPIO selection register 13 for ETM       | 0x00D4  | R/W    |
| <b>Version Register</b>                        |  |         |        |
| <a href="#">GPIO_EXT_VERSION_REG</a>           | Version control register                 | 0x00FC  | R/W    |

### 8.19.4 LP GPIO Matrix Register Summary

The addresses in this section are relative to LP GPIO matrix base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                    | Description                             | Address | Access  |
|---|---|---------|---------|
| <b>Clock Enable Register</b>            |   |         |         |
| <a href="#">LP_GPIO_CLK_EN_REG</a>      | LP GPIO clock gate register             | 0x0000  | R/W     |
| <b>Configuration Registers</b>          |   |         |         |
| <a href="#">LP_GPIO_OUT_REG</a>         | LP GPIO output register                 | 0x0008  | R/W/WTC |
| <a href="#">LP_GPIO_OUT_WITS_REG</a>    | LP GPIO output set register             | 0x000C  | WT      |
| <a href="#">LP_GPIO_OUT_W1TC_REG</a>    | LP GPIO output clear register           | 0x0010  | WT      |
| <a href="#">LP_GPIO_ENABLE_REG</a>      | LP GPIO output enable register          | 0x0014  | R/W/WTC |
| <a href="#">LP_GPIO_ENABLE_WITS_REG</a> | LP GPIO output enable set register      | 0x0018  | WT      |
| <a href="#">LP_GPIO_ENABLE_W1TC_REG</a> | LP GPIO output enable clear register    | 0x001C  | WT      |
| <a href="#">LP_GPIO_STATUS_REG</a>      | LP GPIO interrupt status register       | 0x0020  | R/W/WTC |
| <a href="#">LP_GPIO_STATUS_WITS_REG</a> | LP GPIO interrupt status set register   | 0x0024  | WT      |
| <a href="#">LP_GPIO_STATUS_W1TC_REG</a> | LP GPIO interrupt status clear register | 0x0028  | WT      |



| Name   | Description                                 | Address | Access |
|--|---|---------|--------|
| <a href="#">LP_GPIO_STATUS_NEXT_REG</a>        | LP GPIO interrupt source register           | 0x002C  | RO     |
| <a href="#">LP_GPIO_IN_REG</a>                 | LP GPIO input register                      | 0x0030  | RO     |
| <a href="#">LP_GPIO_PIN0_REG</a>               | LP GPIO0 configuration register             | 0x0034  | varies |
| <a href="#">LP_GPIO_PIN1_REG</a>               | LP GPIO1 configuration register             | 0x0038  | varies |
| <a href="#">LP_GPIO_PIN2_REG</a>               | LP GPIO2 configuration register             | 0x003C  | varies |
| <a href="#">LP_GPIO_PIN3_REG</a>               | LP GPIO3 configuration register             | 0x0040  | varies |
| <a href="#">LP_GPIO_PIN4_REG</a>               | LP GPIO4 configuration register             | 0x0044  | varies |
| <a href="#">LP_GPIO_PIN5_REG</a>               | LP GPIO5 configuration register             | 0x0048  | varies |
| <a href="#">LP_GPIO_PIN6_REG</a>               | LP GPIO6 configuration register             | 0x004C  | varies |
| <a href="#">LP_GPIO_PIN7_REG</a>               | LP GPIO7 configuration register             | 0x0050  | varies |
| <a href="#">LP_GPIO_PIN8_REG</a>               | LP GPIO8 configuration register             | 0x0054  | varies |
| <a href="#">LP_GPIO_PIN9_REG</a>               | LP GPIO9 configuration register             | 0x0058  | varies |
| <a href="#">LP_GPIO_PIN10_REG</a>              | LP GPIO10 configuration register            | 0x005C  | varies |
| <a href="#">LP_GPIO_PIN11_REG</a>              | LP GPIO11 configuration register            | 0x0060  | varies |
| <a href="#">LP_GPIO_PIN12_REG</a>              | LP GPIO12 configuration register            | 0x0064  | varies |
| <a href="#">LP_GPIO_PIN13_REG</a>              | LP GPIO13 configuration register            | 0x0068  | varies |
| <a href="#">LP_GPIO_PIN14_REG</a>              | LP GPIO14 configuration register            | 0x006C  | varies |
| <a href="#">LP_GPIO_PIN15_REG</a>              | LP GPIO15 configuration register            | 0x0070  | varies |
| <a href="#">LP_GPIO_FUNC0_IN_SEL_CFG_REG</a>   | Configuration register for input signal 0   | 0x0074  | R/W    |
| <a href="#">LP_GPIO_FUNC1_IN_SEL_CFG_REG</a>   | Configuration register for input signal 1   | 0x0078  | R/W    |
| <a href="#">LP_GPIO_FUNC2_IN_SEL_CFG_REG</a>   | Configuration register for input signal 2   | 0x007C  | R/W    |
| <a href="#">LP_GPIO_FUNC3_IN_SEL_CFG_REG</a>   | Configuration register for input signal 3   | 0x0080  | R/W    |
| <a href="#">LP_GPIO_FUNC4_IN_SEL_CFG_REG</a>   | Configuration register for input signal 4   | 0x0084  | R/W    |
| <a href="#">LP_GPIO_FUNC5_IN_SEL_CFG_REG</a>   | Configuration register for input signal 5   | 0x0088  | R/W    |
| <a href="#">LP_GPIO_FUNC6_IN_SEL_CFG_REG</a>   | Configuration register for input signal 6   | 0x008C  | R/W    |
| <a href="#">LP_GPIO_FUNC7_IN_SEL_CFG_REG</a>   | Configuration register for input signal 7   | 0x0090  | R/W    |
| <a href="#">LP_GPIO_FUNC8_IN_SEL_CFG_REG</a>   | Configuration register for input signal 8   | 0x0094  | R/W    |
| <a href="#">LP_GPIO_FUNC9_IN_SEL_CFG_REG</a>   | Configuration register for input signal 9   | 0x0098  | R/W    |
| <a href="#">LP_GPIO_FUNC10_IN_SEL_CFG_REG</a>  | Configuration register for input signal 10  | 0x009C  | R/W    |
| <a href="#">LP_GPIO_FUNC11_IN_SEL_CFG_REG</a>  | Configuration register for input signal 11  | 0x00A0  | R/W    |
| <a href="#">LP_GPIO_FUNC12_IN_SEL_CFG_REG</a>  | Configuration register for input signal 12  | 0x00A4  | R/W    |
| <a href="#">LP_GPIO_FUNC13_IN_SEL_CFG_REG</a>  | Configuration register for input signal 13  | 0x00A8  | R/W    |
| <a href="#">LP_GPIO_FUNC0_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO0 output  | 0x00F4  | R/W    |
| <a href="#">LP_GPIO_FUNC1_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO1 output  | 0x00F8  | R/W    |
| <a href="#">LP_GPIO_FUNC2_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO2 output  | 0x00FC  | R/W    |
| <a href="#">LP_GPIO_FUNC3_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO3 output  | 0x0100  | R/W    |
| <a href="#">LP_GPIO_FUNC4_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO4 output  | 0x0104  | R/W    |
| <a href="#">LP_GPIO_FUNC5_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO5 output  | 0x0108  | R/W    |
| <a href="#">LP_GPIO_FUNC6_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO6 output  | 0x010C  | R/W    |
| <a href="#">LP_GPIO_FUNC7_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO7 output  | 0x0110  | R/W    |
| <a href="#">LP_GPIO_FUNC8_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO8 output  | 0x0114  | R/W    |
| <a href="#">LP_GPIO_FUNC9_OUT_SEL_CFG_REG</a>  | Configuration register for LP GPIO9 output  | 0x0118  | R/W    |
| <a href="#">LP_GPIO_FUNC10_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO10 output | 0x011C  | R/W    |

| Name   | Description                                 | Address | Access |
|--|---|---------|--------|
| <a href="#">LP_GPIO_FUNC11_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO11 output | 0x0120  | R/W    |
| <a href="#">LP_GPIO_FUNC12_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO12 output | 0x0124  | R/W    |
| <a href="#">LP_GPIO_FUNC13_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO13 output | 0x0128  | R/W    |
| <a href="#">LP_GPIO_FUNC14_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO14 output | 0x012C  | R/W    |
| <a href="#">LP_GPIO_FUNC15_OUT_SEL_CFG_REG</a> | Configuration register for LP GPIO15 output | 0x0130  | R/W    |
| <b>Version Register</b>                        |   |         |        |
| <a href="#">LP_GPIO_VER_DATE_REG</a>           | Version control register                    | 0x0004  | R/W    |

### 8.19.5 LP IO MUX Register Summary

The addresses in this section are relative to LP IO MUX base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                     | Description                                 | Address | Access |
|--|---|---------|--------|
| <b>Clock Enable Register</b>             |   |         |        |
| <a href="#">LP_IOMUX_CLK_EN_REG</a>      | LP IO MUX clock gate register               | 0x0000  | R/W    |
| <b>Configuration Registers</b>           |   |         |        |
| <a href="#">LP_IOMUX_PADO_REG</a>        | LP IO MUX configuration register for GPIO0  | 0x0008  | R/W    |
| <a href="#">LP_IOMUX_PAD1_REG</a>        | LP IO MUX configuration register for GPIO1  | 0x000C  | R/W    |
| <a href="#">LP_IOMUX_PAD2_REG</a>        | LP IO MUX configuration register for GPIO2  | 0x0010  | R/W    |
| <a href="#">LP_IOMUX_PAD3_REG</a>        | LP IO MUX configuration register for GPIO3  | 0x0014  | R/W    |
| <a href="#">LP_IOMUX_PAD4_REG</a>        | LP IO MUX configuration register for GPIO4  | 0x0018  | R/W    |
| <a href="#">LP_IOMUX_PAD5_REG</a>        | LP IO MUX configuration register for GPIO5  | 0x001C  | R/W    |
| <a href="#">LP_IOMUX_PAD6_REG</a>        | LP IO MUX configuration register for GPIO6  | 0x0020  | R/W    |
| <a href="#">LP_IOMUX_PAD7_REG</a>        | LP IO MUX configuration register for GPIO7  | 0x0024  | R/W    |
| <a href="#">LP_IOMUX_PAD8_REG</a>        | LP IO MUX configuration register for GPIO8  | 0x0028  | R/W    |
| <a href="#">LP_IOMUX_PAD9_REG</a>        | LP IO MUX configuration register for GPIO9  | 0x002C  | R/W    |
| <a href="#">LP_IOMUX_PAD10_REG</a>       | LP IO MUX configuration register for GPIO10 | 0x0030  | R/W    |
| <a href="#">LP_IOMUX_PAD11_REG</a>       | LP IO MUX configuration register for GPIO11 | 0x0034  | R/W    |
| <a href="#">LP_IOMUX_PAD12_REG</a>       | LP IO MUX configuration register for GPIO12 | 0x0038  | R/W    |
| <a href="#">LP_IOMUX_PAD13_REG</a>       | LP IO MUX configuration register for GPIO13 | 0x003C  | R/W    |
| <a href="#">LP_IOMUX_PAD14_REG</a>       | LP IO MUX configuration register for GPIO14 | 0x0040  | R/W    |
| <a href="#">LP_IOMUX_PAD15_REG</a>       | LP IO MUX configuration register for GPIO15 | 0x0044  | R/W    |
| <a href="#">LP_IOMUX_LP_PAD_HOLD_REG</a> | LP GPIO PAD hold control register           | 0x004C  | R/W    |
| <a href="#">LP_IOMUX_LP_PAD_HYS_REG</a>  | LP GPIO PAD hysteresis control register     | 0x0050  | R/W    |
| <b>Version Register</b>                  |   |         |        |
| <a href="#">LP_IOMUX_VER_DATE_REG</a>    | Version control register                    | 0x0004  | R/W    |

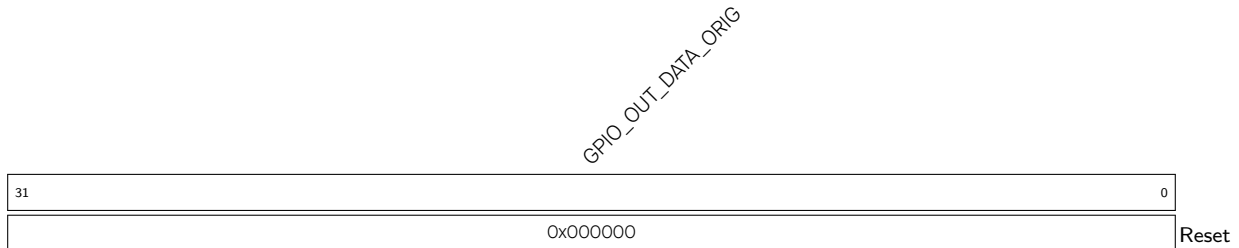
## 8.20 Registers

## 8.20.1 HP GPIO Matrix Registers

The addresses in this section are relative to HP GPIO matrix base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section IX.

**Register 8.1. GPIO\_OUT\_REG (0x0004)**



**GPIO\_OUT\_DATA\_ORIG** Configures the output value of GPIO0 ~ GPIO31 output in simple GPIO output mode.

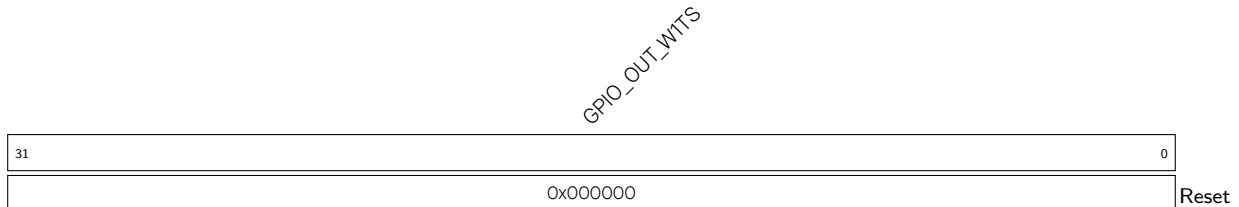
0: Low level

1: High level

The value of bit0 ~ bit31 correspond to the output value of GPIO0 ~ GPIO31 respectively.

(R/W/SC/WTC)

**Register 8.2. GPIO\_OUT\_W1TS\_REG (0x0008)**



**GPIO\_OUT\_W1TS** Configures whether or not to set the output register [GPIO\\_OUT\\_REG](#) of GPIO0 ~ GPIO31.

0: Not set

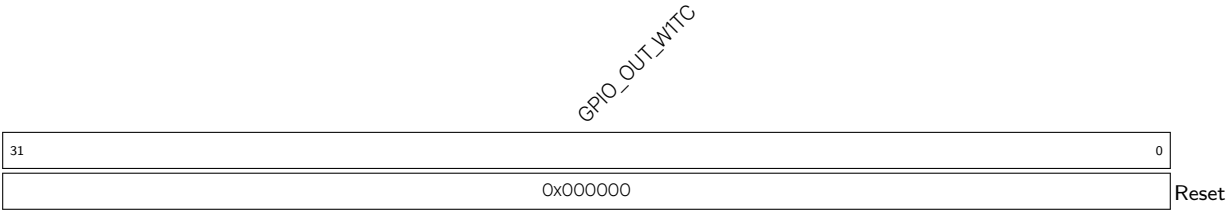
1: The corresponding bit in [GPIO\\_OUT\\_REG](#) will be set to 1

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. Recommended operation: use this register to set [GPIO\\_OUT\\_REG](#).

(WT)



Register 8.3. GPIO\_OUT\_W1TC\_REG (0x000C)



**GPIO\_OUT\_W1TC** Configures whether or not to clear the output register **GPIO\_OUT\_REG** of GPIO0 ~ GPIO31 output.

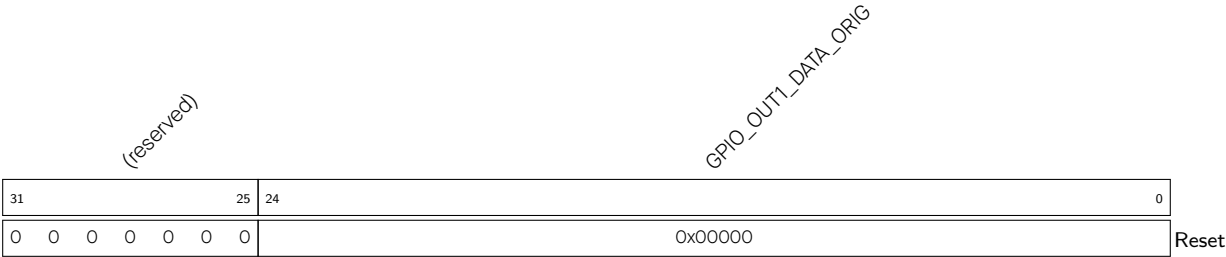
0: Not clear

1: The corresponding bit in **GPIO\_OUT\_REG** will be cleared.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. Recommended operation: use this register to clear **GPIO\_OUT\_REG**.

(WT)

Register 8.4. GPIO\_OUT1\_REG (0x0010)



**GPIO\_OUT1\_DATA\_ORIG** Configures the output value of GPIO32 ~ GPIO54 output in simple GPIO output mode.

0: Low level

1: High level

The value of bit0 ~ bit22 correspond to the output value of GPIO32 ~ GPIO54 respectively.

(R/W/SC/WTC)

(reserved)

GPIO\_OUT1\_WTS

0: Not set

1: The corresponding bit in `GPIO_OUT1_REG` will be set to 1

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. Recommended operation: use this register to set `GPIO_OUT1_REG`.

(WT)

(reserved)

GPIO\_OUT1\_WTTC

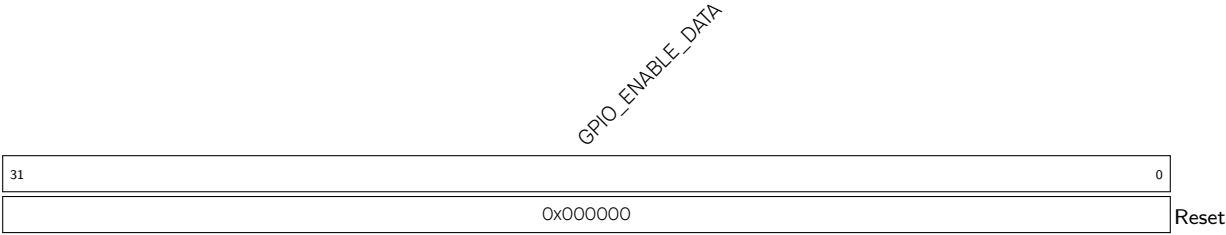
0: Not clear

1: The corresponding bit in `GPIO_OUT1_REG` will be cleared.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. Recommended operation: use this register to clear `GPIO_OUT_REG`.

(WT)

Register 8.7. GPIO\_ENABLE\_REG (0x0020)

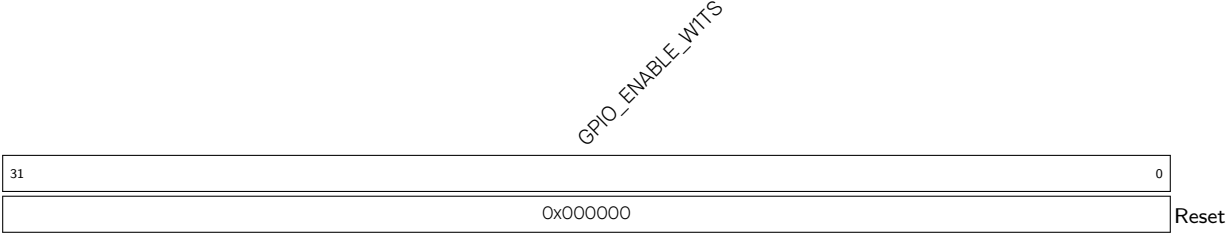


**GPIO\_ENABLE\_DATA** Configures whether or not to enable the output of GPIO0 ~ GPIO31.

- 0: Not enable
- 1: Enable

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31  
(R/W/WTC)

Register 8.8. GPIO\_ENABLE\_WITS\_REG (0x0024)

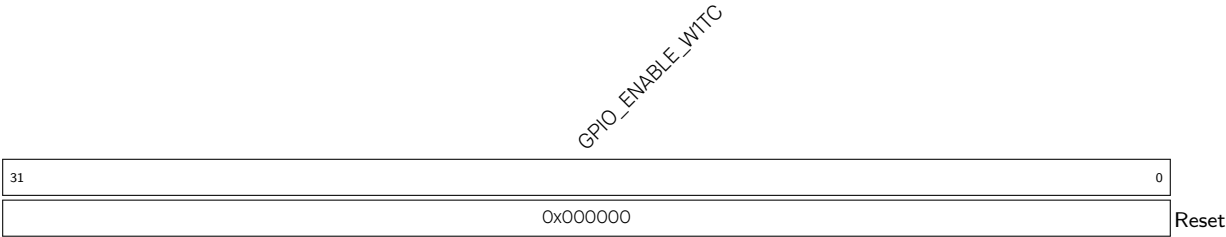


**GPIO\_ENABLE\_WITS** Configures whether or not to set the output enable register [GPIO\\_ENABLE\\_REG](#) of GPIO0 ~ GPIO31.

- 0: Not set
- 1: The corresponding bit in [GPIO\\_ENABLE\\_REG](#) will be set to 1

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. Recommended operation: use this register to set [GPIO\\_ENABLE\\_REG](#).  
(WT)

Register 8.9. GPIO\_ENABLE\_W1TC\_REG (0x0028)



**GPIO\_ENABLE\_W1TC** Configures whether or not to clear the output enable register [GPIO\\_ENABLE\\_REG](#) of GPIO0 ~ GPIO31.

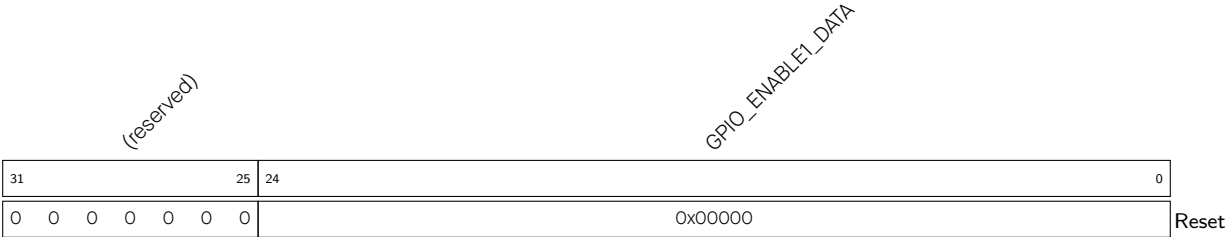
0: Not clear

1: The corresponding bit in [GPIO\\_ENABLE\\_REG](#) will be cleared

Bit0 ~ bit31 are corresponding to GPIO0 ~ 31. Recommended operation: use this register to clear [GPIO\\_ENABLE\\_REG](#).

(WT)

Register 8.10. GPIO\_ENABLE1\_REG (0x002C)



**GPIO\_ENABLE1\_DATA** Configures whether or not to enable the output of GPIO32 ~ GPIO54.

0: Not enable

1: Enable

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54.

(R/W/WTC)

(reserved)

GPIO\_ENABLE1\_WTS

0: Not set

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. Recommended operation: use this register to set `GPIO_ENABLE1_REG`.

(WT)

(reserved)

GPIO\_ENABLE1\_WITC

0: Not clear

Bit0 ~ bit22 are corresponding to GPIO32 ~ 54. Recommended operation: use this register to clear `GPIO_ENABLE1_REG`.

(WT)

### Register 8.13. GPIO\_STRAP\_REG (0x0038)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | GPIO_STRAPPING |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**GPIO\_STRAPPING** Represents the values of GPIO strapping pins.

bit0: GPIO38

bit1: GPIO37

bit2: GPIO36

bit3: GPIO35

bit4: GPIO34

bit5 ~ bit15: invalid

For more information about the functions controlled by strapping pins, see [ESP32-P4 Datasheet](#)

> Section *Strapping Pins*. (RO)

### Register 8.14. GPIO\_IN\_REG (0x003C)

Diagram of the `GPIO_IN_DATA_NEXT` register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value `0x0000000` is shown in the center, and the word "Reset" is at the bottom right.

**GPIO\_IN\_DATA\_NEXT** Represents the input value of GPIO0 ~ GPIO31. Each bit represents a pin

input value:

0: Low level

1: High level

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31.

(RO)

(reserved)

GPIO\_IN1\_DATA\_NEXT

input value:

0: Low level

1: High level

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54.

(RO)

GPIO\_STATUS\_INTERRUPT

GPIO\_STATUS\_INTERRUPT

ware.

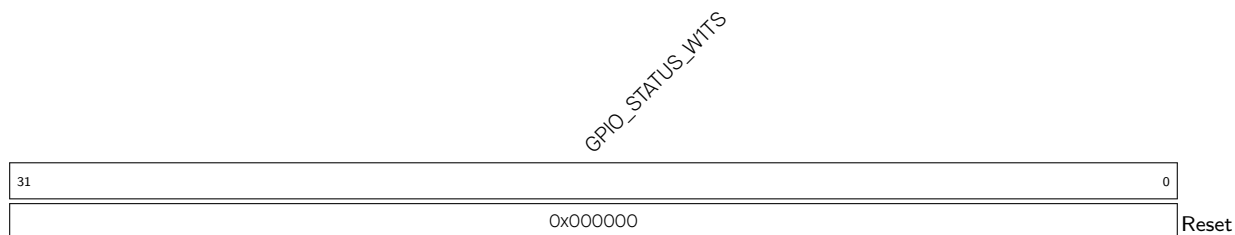
Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31.

Each bit represents the status of its corresponding GPIO:

0: Represents the GPIO does not generate the interrupt configured by `GPIO_PIN $n$ _INT_TYPE`, or this bit is configured to 0 by the software.

1: Represents the GPIO generates the interrupt configured by `GPIO_PINn_INT_TYPE`, or this bit is configured to 1 by the software.

(R/W/WTC)

**Register 8.17. GPIO\_STATUS\_W1TS\_REG (0x0048)**

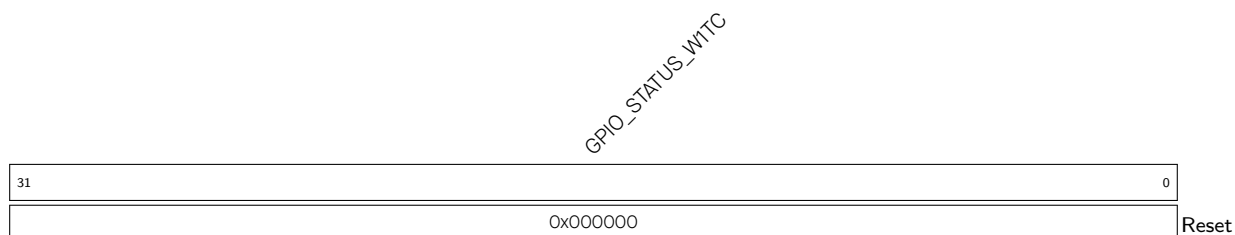
**GPIO\_STATUS\_W1TS** Configures whether or not to set the interrupt status register [GPIO\\_STATUS\\_INTERRUPT](#) of GPIO0 ~ GPIO31.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31.

If the value 1 is written to a bit here, the corresponding bit in [GPIO\\_STATUS\\_INTERRUPT](#) will be set to 1.

Recommended operation: use this register to set [GPIO\\_STATUS\\_INTERRUPT](#).

(WT)

**Register 8.18. GPIO\_STATUS\_W1TC\_REG (0x004C)**

**GPIO\_STATUS\_W1TC** Configures whether or not to clear the interrupt status register [GPIO\\_STATUS\\_INTERRUPT](#) of GPIO0 ~ GPIO31.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31.

If the value 1 is written to a bit here, the corresponding bit in [GPIO\\_STATUS\\_INTERRUPT](#) will be cleared.

Recommended operation: use this register to clear [GPIO\\_STATUS\\_INTERRUPT](#).

(WT)



### Register 8.19. GPIO\_STATUS1\_REG (0x0050)

Diagram illustrating the structure of the `GPIO_STATUS1` register. The register is 32 bits wide, divided into a 7-bit reserved field (bits 31-25) and a 25-bit field for `GPIO_STATUS1_INTERRUPT` (bits 24-0). The initial value is 0x00000.

**GPIO\_STATUS1\_INTERRUPT** The interrupt status of GPIO32 ~ GPIO54, can be configured by the software.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54.

Each bit represents the status of its corresponding GPIO:

0: Represents the GPIO does not generate the interrupt configured by `GPIO_PINn_INT_TYPE`, or this bit is configured to 0 by the software.

1: Represents the GPIO generates the interrupt configured by `GPIO_PINn_INT_TYPE`, or this bit is configured to 1 by the software.

(R/W/WTC)

### Register 8.20. GPIO\_STATUS1\_W1TS\_REG (0x0054)

|                 |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | GPIO_STATUS1_WTTS |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 25                |  |  |  |  |  |  |  | 24 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x00000           |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**GPIO\_STATUS1\_WITS** Configures whether or not to set the interrupt status register **GPIO\_STATUS1\_INTERRUPT** of GPIO32 ~ GPIO54.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54.

If the value 1 is written to a bit here, the corresponding bit in `GPIO_STATUS1_INTERRUPT` will be set to 1.

Recommended operation: use this register to set `GPIO_STATUS1_INTERRUPT`.

(WT)

### Register 8.21. GPIO\_STATUS1\_W1TC\_REG (0x0058)

|                 |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | GPIO_STATUS1_WTC |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|                 |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 25               |  |  |  |  |  |  |  | 24 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x00000          |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**GPIO\_STATUS1\_W1TC** Configures whether or not to clear the interrupt status register **GPIO\_STATUS1\_INTERRUPT** of GPIO32 ~ GPIO54.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54.

If the value 1 is written to a bit here, the corresponding bit in `GPIO_STATUS1_INTERRUPT` will be cleared.

Recommended operation: use this register to clear `GPIO_STATUS1_INTERRUPT`.

(WT)

### Register 8.22. GPIO\_INTR\_0\_REG (0x005C)

Diagram of the GPIO\_INT\_0 register. The register is 32 bits wide, with bit positions 31 to 0 labeled. The value 0x00000000 is shown, indicating all bits are 0. A 'Reset' label is at the bottom right.

**GPIO\_INT\_0** Represents the CPU interrupt 0 status of GPIO0 ~ GPIO31. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by `GPIO_PIN $n$ _INT_TYPE`.

1: Represents the GPIO generates an interrupt configured by `GPIO_PINn_INT_TYPE` after the CPU interrupt is enabled.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. This interrupt status is corresponding to the bit in `GPIO_STATUS_REG` when assert (high) enable signal (bit13 of `GPIO_PIN $n$ _REG`).

(RO)

### Register 8.23. GPIO\_INTR1\_O\_REG (0x0060)

|            |   |   |   |   |   |   |    |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|---|---|---|---|---|---|----|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |   |    | GPIO_INT1_0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         |   |   |   |   |   |   | 25 | 24          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0x00000     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

**GPIO\_INT1\_0** Represents the CPU interrupt 0 status of GPIO32 ~ GPIO54. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by `GPIO_PINn_INT_TYPE`.

1: Represents the GPIO generates an interrupt configured by `GPIO_PINn_INT_TYPE` after the CPU interrupt is enabled.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. This interrupt status is corresponding to the bit in `GPIO_STATUS1_REG` when assert (high) enable signal (bit13 of `GPIO_PINn_REG`).

(RO)

### Register 8.24. GPIO\_INTR\_1\_REG (0x0064)

Diagram of the GPIO\_INT\_1 register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value 0x0000000 is shown in the register box, and the label "Reset" is next to it.

**GPIO\_INT\_1** Represents the CPU interrupt 1 status of GPIO0 ~ GPIO31. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by `GPIO_PINn INT_TYPE`.

1: Represents the GPIO generates an interrupt configured by `GPIO_PINn_INT_TYPE` after the CPU interrupt is enabled.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. This interrupt status is corresponding to the bit in `GPIO_STATUS_REG` when assert (high) enable signal (bit14 of `GPIO_PINn_REG`).

(RO)

**Register 8.25. GPIO\_INTR1\_1\_REG (0x0068)**

|            |   |   |   |   |   |   |    |              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|----|--------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |    | GPIO_INTR1_1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   | 25 | 24           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  |              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
|            |   |   |   |   |   |   |    | 0x00000      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**GPIO\_INTR1\_1** Represents the CPU interrupt 1 status of GPIO32 ~ GPIO54. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by [GPIO\\_PIN \$n\$ \\_INT\\_TYPE](#).

1: Represents the GPIO generates an interrupt configured by [GPIO\\_PIN \$n\$ \\_INT\\_TYPE](#) after the CPU interrupt is enabled.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. This interrupt status is corresponding to the bit in [GPIO\\_STATUS1\\_REG](#) when assert (high) enable signal (bit14 of [GPIO\\_PIN \$n\$ \\_REG](#)).

(RO)

**Register 8.26. GPIO\_STATUS\_NEXT\_REG (0x006C)**

|                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| GPIO_STATUS_INTERRUPT_NEXT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0x000000                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**GPIO\_STATUS\_INTERRUPT\_NEXT** Represents the interrupt source signal of GPIO0 ~ GPIO31.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. Each bit represents:

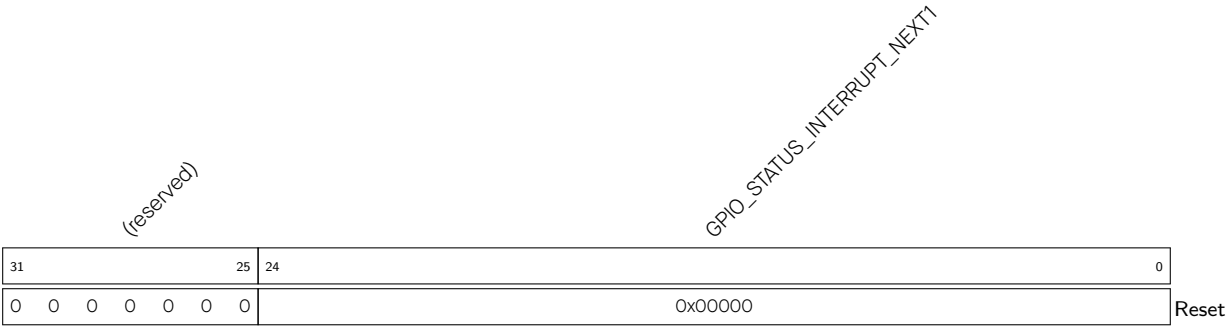
0: The GPIO does not generate the interrupt configured by [GPIO\\_PIN \$n\$ \\_INT\\_TYPE](#).

1: The GPIO generates an interrupt configured by [GPIO\\_PIN \$n\$ \\_INT\\_TYPE](#).

The interrupt could be rising edge interrupt, falling edge interrupt, level sensitive interrupt and any edge interrupt.

(RO)

Register 8.27. GPIO\_STATUS\_NEXT1\_REG (0x0070)



**GPIO\_STATUS\_INTERRUPT\_NEXT1** Represents the interrupt source signal of GPIO32 ~ GPIO54. Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. Each bit represents:

- 0: The GPIO does not generate the interrupt configured by `GPIO_PINn_INT_TYPE`.
- 1: The GPIO generates an interrupt configured by `GPIO_PINn_INT_TYPE`.

The interrupt could be rising edge interrupt, falling edge interrupt, level sensitive interrupt and any edge interrupt.

(RO)

**Register 8.28. GPIO\_PIN $n$ \_REG ( $n$ : 0 - 54) (0x0074+0x4\* $n$ )**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |            |  |   |  |                                      |  |   |  |            |  |     |  |                                     |  |     |  |                                   |  |     |  |                                     |  |   |  |   |  |   |  |   |  |   |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|------------|--|---|--|--------------------------------------|--|---|--|------------|--|-----|--|-------------------------------------|--|-----|--|-----------------------------------|--|-----|--|-------------------------------------|--|---|--|---|--|---|--|---|--|---|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | GPIO_PIN <sub>n</sub> _INT_ENA |  |  |  | (reserved) |  |   |  | GPIO_PIN <sub>n</sub> _WAKEUP_ENABLE |  |   |  | (reserved) |  |     |  | GPIO_PIN <sub>n</sub> _SYNC1_BYPASS |  |     |  | GPIO_PIN <sub>n</sub> _PAD_DRIVER |  |     |  | GPIO_PIN <sub>n</sub> _SYNC2_BYPASS |  |   |  |   |  |   |  |   |  |   |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 18                             |  |  |  | 17         |  |   |  | 13                                   |  |   |  | 12         |  | 11  |  | 10                                  |  | 9   |  | 7                                 |  | 6   |  | 5                                   |  | 4 |  | 3 |  | 2 |  | 1 |  | 0 |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0                            |  |  |  | 0x0        |  | 0 |  | 0x0                                  |  | 0 |  | 0          |  | 0x0 |  | 0                                   |  | 0x0 |  | 0                                 |  | 0x0 |  | Reset                               |  |   |  |   |  |   |  |   |  |   |  |

**GPIO\_PIN $n$ \_SYNC2\_BYPASS** Configures whether or not to synchronize GPIO input data on either edge of HP IO MUX operating clock for the second-level synchronization.

0: Not synchronize

1: Synchronize on falling edge

2: Synchronize on rising edge

3: Synchronize on rising edge

(R/W)

**GPIO\_PIN $n$ \_PAD\_DRIVER** Configures to select pin drive mode.

0: Normal output

1: Open drain output

(R/W)

**GPIO\_PIN $n$ \_SYNC1\_BYPASS** Configures whether or not to synchronize GPIO input data on either edge of HP IO MUX operating clock for the first-level synchronization.

0: Not synchronize

1: Synchronize on falling edge

2: Synchronize on rising edge

3: Synchronize on rising edge

(R/W)

**GPIO\_PIN $n$ \_INT\_TYPE** Configures GPIO interrupt type.

0: GPIO interrupt disabled

1: Rising edge trigger

2: Falling edge trigger

3: Any edge trigger

4: Low level trigger

5: High level trigger

(R/W)

**GPIO\_PIN $n$ \_WAKEUP\_ENABLE** Configures whether or not to enable GPIO wake-up function.

0: Disable

1: Enable

This function only wakes up the CPU from Light-sleep.

(R/W)

Continued on the next page...

**Register 8.28. GPIO\_PIN $n$ \_REG ( $n$ : 0 - 54) (0x0074+0x4\* $n$ )**

Continued from the previous page...

**GPIO\_PIN $n$ \_INT\_ENA** Configures whether or not to enable CPU interrupt or CPU non-maskable interrupt.

bit13: Configures whether or not to enable CPU interrupt 0:

0: Disable

1: Enable

bit14: Configures whether or not to enable CPU interrupt 1:

0: Disable

1: Enable

bit15: invalid

bit16: Configures whether or not to enable CPU interrupt 2:

0: Disable

1: Enable

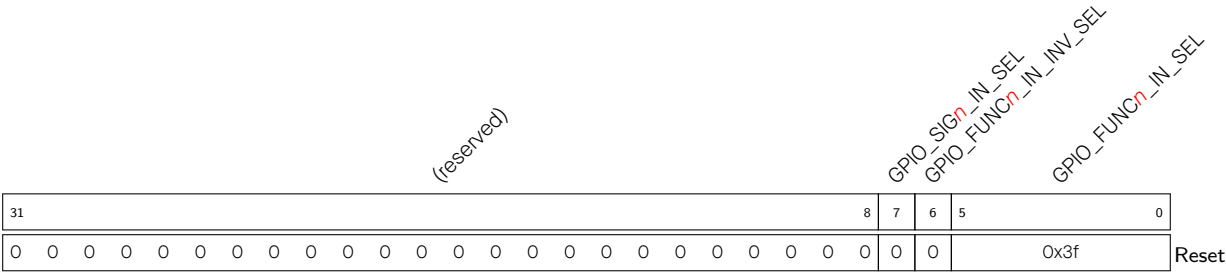
bit17: Configures whether or not to enable CPU interrupt 3:

0: Disable

1: Enable

(R/W)

Register 8.29. GPIO\_FUNCn\_IN\_SEL\_CFG\_REG (n: 0 - 255) (0x015C+4\*n)



GPIO\_FUNCn\_IN\_SEL Configures to select a pin from the 55 GPIO pins to connect the input signal n.

- 0: Select GPIO0
- 1: Select GPIO1
- .....
- 53: Select GPIO53
- 54: Select GPIO54
- 55 ~ 61: invalid
- Or
- 62: A constantly low input
- 63: A constantly high input
- (R/W)

GPIO\_FUNCn\_IN\_INV\_SEL Configures whether or not to invert the input value.

- 0: Not invert
- 1: Invert
- (R/W)

GPIO\_SIGn\_IN\_SEL Configures whether or not to route signals via HP GPIO matrix.

- 0: Bypass HP GPIO matrix, i.e., connect signals directly to peripheral configured in HP IO MUX.
- 1: Route signals via HP GPIO matrix.
- (R/W)



**Register 8.30. GPIO\_FUNC $n$ \_OUT\_SEL\_CFG\_REG ( $n$ : 0 - 54) (0x0558+0x4\* $n$ )**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |   |   |       |                                |    |   |   |                                     |  |  |  |                                 |  |  |  |  |  |  |       |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|---|---|-------|--------------------------------|----|---|---|-------------------------------------|--|--|--|---------------------------------|--|--|--|--|--|--|-------|--|--|--|--|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | GPIO_FUNC <sub>n</sub> _OE_INV_SEL |   |   |       | GPIO_FUNC <sub>n</sub> _OE_SEL |    |   |   | GPIO_FUNC <sub>n</sub> _OUT_INV_SEL |  |  |  | GPIO_FUNC <sub>n</sub> _OUT_SEL |  |  |  |  |  |  |       |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12                                 |   |   |       | 11                             | 10 | 9 | 8 | 0                                   |  |  |  |                                 |  |  |  |  |  |  |       |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                  | 0 | 0 | 0x100 |                                |    |   |   |                                     |  |  |  |                                 |  |  |  |  |  |  | Reset |  |  |  |  |

**GPIO\_FUNC $n$ \_OUT\_SEL** Configures to select a signal  $Y$  ( $0 \leq Y < 256$ ) from 256 peripheral signals to be output to GPIO $n$ .

0: Select signal 0

1: Select signal 1

.....

254: Select signal 254

255: Select signal 255

Or

256: Bit $n$  of [GPIO\\_OUT\\_REG](#) and [GPIO\\_OUT1\\_REG](#) are selected as the output value, [GPIO\\_ENABLE\\_REG](#) and [GPIO\\_ENABLE1\\_REG](#) are selected as the output enable.

257 ~ 511: invalid

For the detailed signal list, see Table 8.12-1.

(R/W/SC)

**GPIO\_FUNC $n$ \_OUT\_INV\_SEL** Configures whether or not to invert the output value.

0: Not invert

1: Invert

(R/W/SC)

**GPIO\_FUNC $n$ \_OE\_SEL** Configures to select the source of output enable signal.

0: Use output enable signal from peripheral.

1: Force the output enable signal to be sourced from bit $n$  ( $n$ : 0 ~ 31) of [GPIO\\_ENABLE\\_REG](#) and bit $n-32$  ( $n$ : 32 ~ 54) of [GPIO\\_ENABLE1\\_REG](#).

(R/W)

**GPIO\_FUNC $n$ \_OE\_INV\_SEL** Configures whether or not to invert the output enable signal.

0: Not invert

1: Invert

(R/W)

**Register 8.31. GPIO\_INTR\_2\_REG (0x063C)**

|             |   |
|-------------|---|
| GPIO_INTR_2 |   |
| 31          | 0 |
| 0x000000    |   |
| Reset       |   |

**GPIO\_INT\_2** Represents the CPU interrupt 2 status of GPIO0 ~ GPIO31. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by [GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#).

1: Represents the GPIO generates an interrupt configured by [GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#) after the CPU interrupt is enabled.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. This interrupt status is corresponding to the bit in [GPIO\\_STATUS\\_REG](#) when assert (high) enable signal (bit16 of [GPIO\\_PIN<sub>n</sub>\\_REG](#)).

(RO)

**Register 8.32. GPIO\_INTR1\_2\_REG (0x0640)**

|               |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---------------|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)    |  |  |  |  |  |  |  | GPIO_INT1_2 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31            |  |  |  |  |  |  |  | 25          |  |  |  |  |  |  |  | 24 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x00000     |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**GPIO\_INT1\_2** Represents the CPU interrupt 2 status of GPIO32 ~ GPIO54. Each bit represents:

0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by [GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#).

1: Represents the GPIO generates an interrupt configured by [GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#) after the CPU interrupt is enabled.

Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. This interrupt status is corresponding to the bit in [GPIO\\_STATUS1\\_REG](#) when assert (high) enable signal (bit16 of [GPIO\\_PIN<sub>n</sub>\\_REG](#)).

(RO)

GPIO\_INT\_3

**GPIO\_INT\_3** Represents the CPU interrupt 3 status of GPIO0 ~ GPIO31. Each bit represents:

- 0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by **GPIO\_PIN $n$ \_INT\_TYPE**.
- 1: Represents the GPIO generates an interrupt configured by **GPIO\_PIN $n$ \_INT\_TYPE** after the CPU interrupt is enabled.

Bit0 ~ bit31 are corresponding to GPIO0 ~ GPIO31. This interrupt status is corresponding to the bit in **GPIO\_STATUS\_REG** when assert (high) enable signal (bit17 of **GPIO\_PIN $n$ \_REG**).

(RO)

(reserved)

GPIO\_INT1\_3

**GPIO\_INT1\_3** Represents the CPU interrupt 3 status of GPIO32 ~ GPIO54. Each bit represents:

- 0: Represents CPU interrupt is not enabled, or the GPIO does not generate the interrupt configured by **GPIO\_PIN $n$ \_INT\_TYPE**.
- 1: Represents the GPIO generates an interrupt configured by **GPIO\_PIN $n$ \_INT\_TYPE** after the CPU interrupt is enabled.

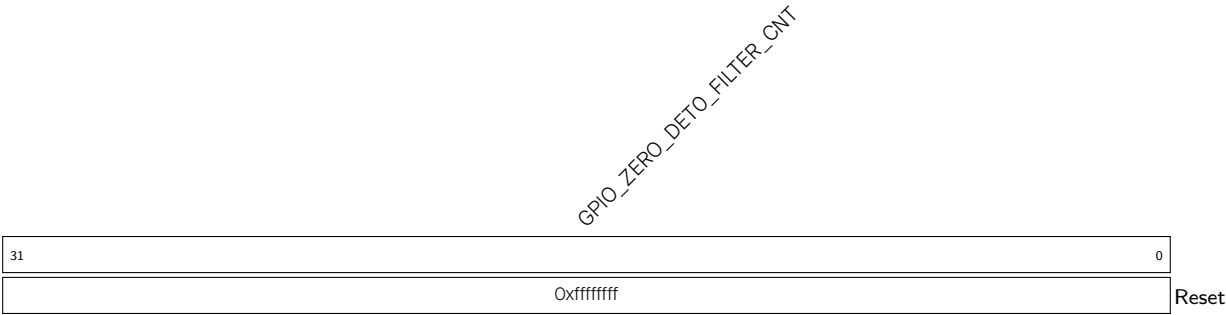
Bit0 ~ bit22 are corresponding to GPIO32 ~ GPIO54. This interrupt status is corresponding to the bit in **GPIO\_STATUS1\_REG** when assert (high) enable signal (bit17 of **GPIO\_PIN $n$ \_REG**).

(reserved)

GPIO\_CLK\_EN

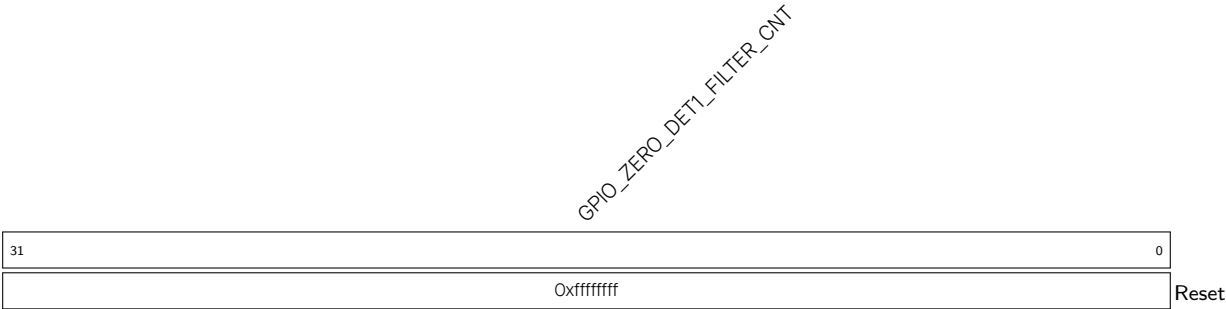
**GPIO\_CLK\_EN** Configures whether or not to enable clock gate.  
0: Not enable  
1: Enable, the clock is free running.  
(R/W)

Register 8.36. GPIO\_ZERO\_DET0\_FILTER\_CNT\_REG (0x0710)



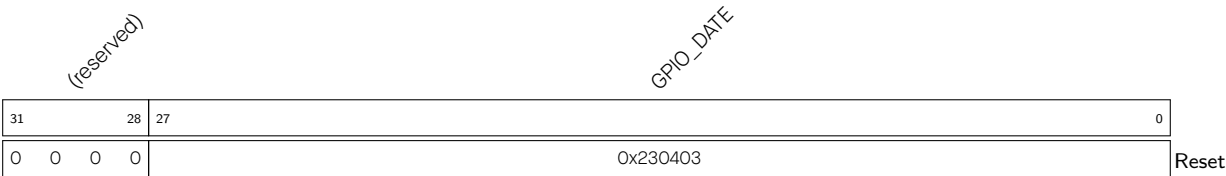
**GPIO\_ZERO\_DET0\_FILTER\_CNT** Configures to change GPIO analog comparator0 zero detect filter’s threshold.  
Interrupts in [GPIO\\_ZERO\\_DET0\\_FILTER\\_CNT](#) iomux\_core\_clk cycles after one interrupt will be filtered, and not be seen by CPU. (R/W)

Register 8.37. GPIO\_ZERO\_DET1\_FILTER\_CNT\_REG (0x0714)



**GPIO\_ZERO\_DET1\_FILTER\_CNT** Configures to change GPIO analog comparator1 zero detect filter’s threshold.  
Interrupts in [GPIO\\_ZERO\\_DET0\\_FILTER\\_CNT](#) iomux\_core\_clk cycles after one interrupt will be filtered, and not be seen by CPU. (R/W)

Register 8.38. GPIO\_DATE\_REG (0x07FC)



**GPIO\_DATE** Version control register.  
(R/W)

### Register 8.39. GPIO\_INT\_RAW\_REG (0x0700)

[illegible]

**GPIO\_COMPO\_NEG\_INT\_RAW** The raw interrupt status of [GPIO\\_COMPO\\_NEG\\_INT](#). (R/WTC/SS)

**GPIO** **COMPO** **POS** **INT** **RAW** The raw interrupt status of **GPIO** **COMPO** **POS** **INT**. (R/WTC/SS)

**GPIO\_COMPO\_ALL\_INT\_RAW** The raw interrupt status of [GPIO\\_COMPO\\_ALL\\_INT](#). (R/WTC/SS)

**GPIO\_COMP1\_NEG\_INT\_RAW** The raw interrupt status of **GPIO\_COMP1\_NEG\_INT**. (R/WTC/SS)

**GPIO\_COMP1\_POS\_INT\_RAW** The raw interrupt status of **GPIO\_COMP1\_POS\_INT**. (R/WTC/SS)

**GPIO\_COMP1\_ALL\_INT\_RAW** The raw interrupt status of [GPIO\\_COMP1\\_ALL\\_INT](#). (R/WTC/SS)

### Register 8.40. GPIO\_INT\_ST\_REG (0x0704)

[illegible]

**GPIO\_COMPO\_NEG\_INT\_ST** The masked interrupt status of [GPIO\\_COMPO\\_NEG\\_INT](#). (RO)

**GPIO\_COMP0\_POS\_INT\_ST** The masked interrupt status of [GPIO\\_COMP0\\_POS\\_INT](#). (RO)

**GPIO\_COMPO\_ALL\_INT\_ST** The masked interrupt status of [GPIO\\_COMPO\\_ALL\\_INT](#). (RO)

**GPIO\_COMP1\_NEG\_INT\_ST** The masked interrupt status of [GPIO\\_COMP1\\_NEG\\_INT](#). (RO)

**GPIO\_COMP1\_POS\_INT\_ST** The masked interrupt status of [GPIO\\_COMP1\\_POS\\_INT](#). (RO)

**GPIO\_COMP1\_ALL\_INT\_ST** The masked interrupt status of **GPIO\_COMP1\_ALL\_INT**. (RO)

Register 8.41. GPIO\_INT\_ENA\_REG (0x0708)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | GPIO_COMP1_ALL_INT_ENA<br>GPIO_COMP1_POS_INT_ENA<br>GPIO_COMP1_NEG_INT_ENA<br>GPIO_COMPO_ALL_INT_ENA<br>GPIO_COMPO_POS_INT_ENA<br>GPIO_COMPO_NEG_INT_ENA |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6  | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

GPIO\_COMPO\_NEG\_INT\_ENA Write 1 to enable [GPIO\\_COMPO\\_NEG\\_INT](#). (R/W)

GPIO\_COMPO\_POS\_INT\_ENA Write 1 to enable [GPIO\\_COMPO\\_POS\\_INT](#). (R/W)

GPIO\_COMPO\_ALL\_INT\_ENA Write 1 to enable [GPIO\\_COMPO\\_ALL\\_INT](#). (R/W)

GPIO\_COMP1\_NEG\_INT\_ENA Write 1 to enable [GPIO\\_COMP1\\_NEG\\_INT](#). (R/W)

GPIO\_COMP1\_POS\_INT\_ENA Write 1 to enable [GPIO\\_COMP1\\_POS\\_INT](#). (R/W)

GPIO\_COMP1\_ALL\_INT\_ENA Write 1 to enable [GPIO\\_COMP1\\_ALL\\_INT](#). (R/W)

Register 8.42. GPIO\_INT\_CLR\_REG (0x070C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | GPIO_COMP1_ALL_INT_CLR<br>GPIO_COMP1_POS_INT_CLR<br>GPIO_COMP1_NEG_INT_CLR<br>GPIO_COMPO_ALL_INT_CLR<br>GPIO_COMPO_POS_INT_CLR<br>GPIO_COMPO_NEG_INT_CLR |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6  | 5 | 4 | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | Reset |

GPIO\_COMPO\_NEG\_INT\_CLR Write 1 to clear [GPIO\\_COMPO\\_NEG\\_INT](#). (WT)

GPIO\_COMPO\_POS\_INT\_CLR Write 1 to clear [GPIO\\_COMPO\\_POS\\_INT](#). (WT)

GPIO\_COMPO\_ALL\_INT\_CLR Write 1 to clear [GPIO\\_COMPO\\_ALL\\_INT](#). (WT)

GPIO\_COMP1\_NEG\_INT\_CLR Write 1 to clear [GPIO\\_COMP1\\_NEG\\_INT](#). (WT)

GPIO\_COMP1\_POS\_INT\_CLR Write 1 to clear [GPIO\\_COMP1\\_POS\\_INT](#). (WT)

GPIO\_COMP1\_ALL\_INT\_CLR Write 1 to clear [GPIO\\_COMP1\\_ALL\\_INT](#). (WT)

## 8.20.2 HP IO MUX Registers

The addresses in this section are relative to the HP IO MUX base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section IX.

Register 8.43. IO\_MUX\_GPIO $n$ \_REG ( $n$ : 0 - 54) (0x0004+4\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |    |    |   |     |    |   |   |   |   |       |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|----|----|---|-----|----|---|---|---|---|-------|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | IO_MUX_GPIO <sub>n</sub> _FILTER_EN<br>IO_MUX_GPIO <sub>n</sub> _MCU_SEL<br>IO_MUX_GPIO <sub>n</sub> _FUN_DRV<br>IO_MUX_GPIO <sub>n</sub> _FUN_IE<br>IO_MUX_GPIO <sub>n</sub> _FUN_WPU<br>IO_MUX_GPIO <sub>n</sub> _FUN_WPD<br>IO_MUX_GPIO <sub>n</sub> _MCU_DRV<br>IO_MUX_GPIO <sub>n</sub> _MCU_IE<br>IO_MUX_GPIO <sub>n</sub> _MCU_WPU<br>IO_MUX_GPIO <sub>n</sub> _MCU_WPD<br>IO_MUX_GPIO <sub>n</sub> _SLP_SEL<br>IO_MUX_GPIO <sub>n</sub> _MCU_OE |     |    |    |   |     |    |   |   |   |   |       |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16  | 15  | 14 | 12 |   | 11  | 10 | 9 | 8 | 7 | 6 | 5     | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0x0 | 0  | 0  | 0 | 0x0 | 0  | 0 | 0 | 0 | 0 | Reset |   |   |   |   |   |

**IO\_MUX\_GPIO $n$ \_MCU\_OE** Configures whether or not to enable the output of GPIO $n$  in sleep mode.

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_SLP\_SEL** Configures whether or not to enter sleep mode for GPIO $n$ .

0: Not enter

1: Enter

(R/W)

**IO\_MUX\_GPIO $n$ \_MCU\_WPD** Configure whether or not to enable pull-down resistor of GPIO $n$  during sleep mode.

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_MCU\_WPU** Configures whether or not to enable pull-up resistor of GPIO $n$  during sleep mode.

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_MCU\_IE** Configures whether or not to enable the input of GPIO $n$  during sleep mode.

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_MCU\_DRV** Configures the drive strength of GPIO $n$  during sleep mode.

0: ~5 mA

1: ~10 mA

2: ~20 mA

3: ~40 mA

(R/W)

Continued on the next page...

**Register 8.43. IO\_MUX\_GPIO $n$ \_REG ( $n$ : 0 - 54) (0x0004+4\* $n$ )**

Continued from the previous page...

**IO\_MUX\_GPIO $n$ \_FUN\_WPD** Configures whether or not to enable pull-down resistor of GPIO $n$ .

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_FUN\_WPU** Configures whether or not enable pull-up resistor of GPIO $n$ .

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_FUN\_IE** Configures whether or not to enable input of GPIO $n$ .

0: Disable

1: Enable

(R/W)

**IO\_MUX\_GPIO $n$ \_FUN\_DRV** Configures the drive strength of GPIO $n$ .

0: ~5 mA

1: ~10 mA

2: ~20 mA

3: ~40 mA

(R/W)

**IO\_MUX\_GPIO $n$ \_MCU\_SEL** Configures to select IO MUX function for this pin.

0: Select Function 0

1: Select Function 1

.....

(R/W)

**IO\_MUX\_GPIO $n$ \_FILTER\_EN** Configures whether or not to enable filter for pin input signals.

0: Disable

1: Enable

(R/W)

**Register 8.44. IO\_MUX\_DATE\_REG (0x0104)**

|            |    |    |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | IO_MUX_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0  | 0  | 0 | 0x201222    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**IO\_MUX\_DATE** Version control register.

(R/W)





**Register 8.47. GPIO\_EXT\_GLITCH\_FILTER\_CH $n$ \_REG ( $n$ : 0 - 7) (0x0030+0x4\* $n$ )**

**GPIO\_EXT\_FILTER\_CH $n$ \_EN** Configures whether or not to enable channel  $n$  of Glitch Filter.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_FILTER\_CH $n$ \_INPUT\_IO\_NUM** Configures to select the input GPIO for Glitch Filter.

0: Select GPIO0

1: Select GPIO1

.....

53: Select GPIO53

54: Select GPIO54

(R/W)

**GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_THRES** Configures the window threshold for Glitch Filter. The window threshold should be less than or equal to [GPIO\\_EXT\\_FILTER\\_CH \$n\$ \\_WINDOW\\_WIDTH](#).

Measurement unit: HP IO MUX operating clock cycle

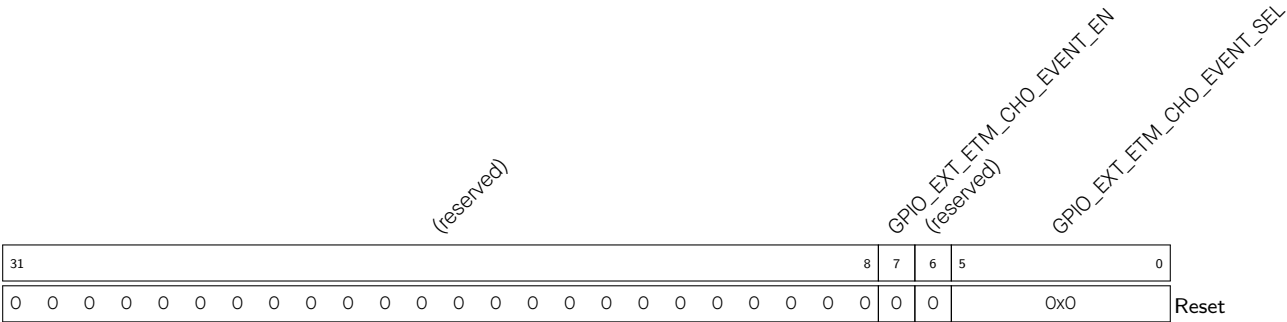
(R/W)

**GPIO\_EXT\_FILTER\_CH $n$ \_WINDOW\_WIDTH** Configures the window width for Glitch Filter. The effective value of window width is 0 ~ 62. 63 is a reserved value and can not be used.

Measurement unit: HP IO MUX operating clock cycle

(R/W)

Register 8.48. GPIO\_EXT\_ETM\_EVENT\_CHn\_CFG\_REG (n: 0 - 7) (0x0060+0x4\*n)



GPIO\_EXT\_ETM\_CHn\_EVENT\_SEL Configures to select GPIO for ETM event channel.

- 0: Select GPIO0
  - 1: Select GPIO1
  - .....
  - 53: Select GPIO53
  - 54: Select GPIO54
- (R/W)

GPIO\_EXT\_ETM\_CHn\_EVENT\_EN Configures whether or not to enable ETM event send.

- 0: Not enable
  - 1: Enable
- (R/W)

### Register 8.49. GPIO\_EXT\_ETM\_TASK\_PO\_CFG\_REG (0x00A0)

|            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|----|--|--|--|---|--|--|--|---|--|--|--|-----|--|--|--|---|--|--|--|-------|--|--|--|---|--|--|--|---|--|--|--|
| (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO3_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO3_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO2_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO2_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO1_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO1_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO0_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO0_EN |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
| 31         |  |  |  | 28                          |  |  |  | 27                         |  |  |  | 25         |  |  |  | 24                          |  |  |  | 23                         |  |  |  | 20         |  |  |  | 19                          |  |  |  | 17                         |  |  |  | 16         |  |  |  | 15                          |  |  |  | 12                         |  |  |  | 11 |  |  |  | 9 |  |  |  | 8 |  |  |  | 7   |  |  |  | 4 |  |  |  | 3     |  |  |  | 1 |  |  |  | 0 |  |  |  |
| 0          |  |  |  | 0                           |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0x0                         |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0                           |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0x0                         |  |  |  | 0                          |  |  |  | 0  |  |  |  | 0 |  |  |  | 0 |  |  |  | 0x0 |  |  |  | 0 |  |  |  | Reset |  |  |  |   |  |  |  |   |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 0 - 3)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 0 - 3) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.50. GPIO\_EXT\_ETM\_TASK\_P1\_CFG\_REG (0x00A4)

|            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |            |  |  |  |                             |  |  |  |                            |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|----|--|--|--|---|--|--|--|---|--|--|--|-----|--|--|--|---|--|--|--|-------|--|--|--|---|--|--|--|---|--|--|--|
| (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO7_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO7_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO6_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO6_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO5_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO5_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO4_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO4_EN |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
| 31         |  |  |  | 28                          |  |  |  | 27                         |  |  |  | 25         |  |  |  | 24                          |  |  |  | 23                         |  |  |  | 20         |  |  |  | 19                          |  |  |  | 17                         |  |  |  | 16         |  |  |  | 15                          |  |  |  | 12                         |  |  |  | 11 |  |  |  | 9 |  |  |  | 8 |  |  |  | 7   |  |  |  | 4 |  |  |  | 3     |  |  |  | 1 |  |  |  | 0 |  |  |  |
| 0          |  |  |  | 0                           |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0x0                         |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0                           |  |  |  | 0                          |  |  |  | 0          |  |  |  | 0x0                         |  |  |  | 0                          |  |  |  | 0  |  |  |  | 0 |  |  |  | 0 |  |  |  | 0x0 |  |  |  | 0 |  |  |  | Reset |  |  |  |   |  |  |  |   |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 4 - 7)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 4 - 7) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.51. GPIO\_EXT\_ETM\_TASK\_P2\_CFG\_REG (0x00A8)

|            |  |  |  |                              |  |  |  |            |  |  |  |                              |  |  |  |            |  |  |  |                             |  |  |  |            |  |  |  |                             |  |  |  |    |  |  |  |    |  |  |  |     |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
|------------|--|--|--|------------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|-----------------------------|--|--|--|----|--|--|--|----|--|--|--|-----|--|--|--|----|--|--|--|----|--|--|--|---|--|--|--|---|--|--|--|-----|--|--|--|---|--|--|--|-------|--|--|--|---|--|--|--|---|--|--|--|
| (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO11_SEL |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO10_SEL |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO9_SEL |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO8_SEL |  |  |  |    |  |  |  |    |  |  |  |     |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |     |  |  |  |   |  |  |  |       |  |  |  |   |  |  |  |   |  |  |  |
| 31         |  |  |  | 28                           |  |  |  | 27         |  |  |  | 25                           |  |  |  | 24         |  |  |  | 23                          |  |  |  | 20         |  |  |  | 19                          |  |  |  | 17 |  |  |  | 16 |  |  |  | 15  |  |  |  | 12 |  |  |  | 11 |  |  |  | 9 |  |  |  | 8 |  |  |  | 7   |  |  |  | 4 |  |  |  | 3     |  |  |  | 1 |  |  |  | 0 |  |  |  |
| 0          |  |  |  | 0                            |  |  |  | 0          |  |  |  | 0                            |  |  |  | 0x0        |  |  |  | 0                           |  |  |  | 0          |  |  |  | 0                           |  |  |  | 0  |  |  |  | 0  |  |  |  | 0x0 |  |  |  | 0  |  |  |  | 0  |  |  |  | 0 |  |  |  | 0 |  |  |  | 0x0 |  |  |  | 0 |  |  |  | Reset |  |  |  |   |  |  |  |   |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 8 - 11)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 8 - 11) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.52. GPIO\_EXT\_ETM\_TASK\_P3\_CFG\_REG (0x00AC)

|            |    |    |    |                              |     |    |    |            |    |    |     |                              |   |   |   |            |     |   |   |                              |   |     |   |            |  |  |  |                              |  |  |  |            |  |  |  |
|------------|----|----|----|------------------------------|-----|----|----|------------|----|----|-----|------------------------------|---|---|---|------------|-----|---|---|------------------------------|---|-----|---|------------|--|--|--|------------------------------|--|--|--|------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO15_SEL |     |    |    | (reserved) |    |    |     | GPIO_EXT_ETM_TASK_GPIO14_SEL |   |   |   | (reserved) |     |   |   | GPIO_EXT_ETM_TASK_GPIO13_SEL |   |     |   | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO12_SEL |  |  |  | (reserved) |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23  | 20 | 19 | 17         | 16 | 15 | 12  | 11                           | 9 | 8 | 7 | 4          | 3   | 1 | 0 |                              |   |     |   |            |  |  |  |                              |  |  |  |            |  |  |  |
| 0          | 0  | 0  | 0  | 0                            | 0x0 | 0  | 0  | 0          | 0  | 0  | 0x0 | 0                            | 0 | 0 | 0 | 0          | 0x0 | 0 | 0 | 0                            | 0 | 0x0 | 0 | Reset      |  |  |  |                              |  |  |  |            |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 12 - 15)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 12 - 15)** Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.53. GPIO\_EXT\_ETM\_TASK\_P4\_CFG\_REG (0x00B0)

|            |    |    |    |                              |     |    |    |            |    |    |    |                              |     |   |   |            |   |   |   |                              |   |       |  |            |  |  |  |                              |  |  |  |            |  |  |  |
|------------|----|----|----|------------------------------|-----|----|----|------------|----|----|----|------------------------------|-----|---|---|------------|---|---|---|------------------------------|---|-------|--|------------|--|--|--|------------------------------|--|--|--|------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO19_SEL |     |    |    | (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO18_SEL |     |   |   | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO17_SEL |   |       |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO16_SEL |  |  |  | (reserved) |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23  | 20 | 19 | 17         | 16 | 15 | 12 | 11                           | 9   | 8 | 7 | 4          | 3 | 1 | 0 |                              |   |       |  |            |  |  |  |                              |  |  |  |            |  |  |  |
| 0          | 0  | 0  | 0  | 0                            | 0x0 | 0  | 0  | 0          | 0  | 0  | 0  | 0                            | 0x0 | 0 | 0 | 0          | 0 | 0 | 0 | 0x0                          | 0 | Reset |  |            |  |  |  |                              |  |  |  |            |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 16 - 19)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 16 - 19)** Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)



Register 8.54. GPIO\_EXT\_ETM\_TASK\_P5\_CFG\_REG (0x00B4)

|            |    |    |    |                              |    |    |    |                             |    |     |    |            |   |   |   |                              |   |   |   |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|-----------------------------|----|-----|----|------------|---|---|---|------------------------------|---|---|---|-----------------------------|---|---|---|------------|---|-------|--|------------------------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO23_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO23_EN |    |     |    | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO22_SEL |   |   |   | GPIO_EXT_ETM_TASK_GPIO22_EN |   |   |   | (reserved) |   |       |  | GPIO_EXT_ETM_TASK_GPIO21_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO21_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO20_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO20_EN |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17                          | 16 | 15  | 12 | 11         | 9 | 8 | 7 | 4                            | 3 | 1 | 0 |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0                           | 0  | 0x0 | 0  | 0          | 0 | 0 | 0 | 0x0                          | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0x0        | 0 | Reset |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 20 - 23)** Configures whether or not to enable GPIO $n$  to re-  
sponse ETM task.  
0: Not enable  
1: Enable  
(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 20 - 23)** Configures to select an ETM task channel for  
GPIO $n$ .  
0: Select channel 0  
1: Select channel 1  
.....  
7: Select channel 7  
(R/W)

Register 8.55. GPIO\_EXT\_ETM\_TASK\_P6\_CFG\_REG (0x00B8)

|            |    |    |    |                              |    |    |    |                             |    |     |    |            |   |   |   |                              |   |   |   |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|-----------------------------|----|-----|----|------------|---|---|---|------------------------------|---|---|---|-----------------------------|---|---|---|------------|---|-------|--|------------------------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO27_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO27_EN |    |     |    | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO26_SEL |   |   |   | GPIO_EXT_ETM_TASK_GPIO26_EN |   |   |   | (reserved) |   |       |  | GPIO_EXT_ETM_TASK_GPIO25_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO25_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO24_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO24_EN |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17                          | 16 | 15  | 12 | 11         | 9 | 8 | 7 | 4                            | 3 | 1 | 0 |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0                           | 0  | 0x0 | 0  | 0          | 0 | 0 | 0 | 0x0                          | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0x0        | 0 | Reset |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 24 - 27)** Configures whether or not to enable GPIO $n$  to re-  
sponse ETM task.  
0: Not enable  
1: Enable  
(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 24 - 27)** Configures to select an ETM task channel for  
GPIO $n$ .  
0: Select channel 0  
1: Select channel 1  
.....  
7: Select channel 7  
(R/W)

Register 8.56. GPIO\_EXT\_ETM\_TASK\_P7\_CFG\_REG (0x00BC)

|            |    |    |    |                              |    |    |    |                             |    |     |    |            |   |   |   |                              |   |   |   |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|-----------------------------|----|-----|----|------------|---|---|---|------------------------------|---|---|---|-----------------------------|---|---|---|------------|---|-------|--|------------------------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO31_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO31_EN |    |     |    | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO30_SEL |   |   |   | GPIO_EXT_ETM_TASK_GPIO30_EN |   |   |   | (reserved) |   |       |  | GPIO_EXT_ETM_TASK_GPIO29_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO29_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO28_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO28_EN |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17                          | 16 | 15  | 12 | 11         | 9 | 8 | 7 | 4                            | 3 | 1 | 0 |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0                           | 0  | 0x0 | 0  | 0          | 0 | 0 | 0 | 0x0                          | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0x0        | 0 | Reset |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 28 - 31)** Configures whether or not to enable GPIO $n$  to re-  
sponse ETM task.  
0: Not enable  
1: Enable  
(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 28 - 31)** Configures to select an ETM task channel for  
GPIO $n$ .  
0: Select channel 0  
1: Select channel 1  
.....  
7: Select channel 7  
(R/W)

### Register 8.57. GPIO\_EXT\_ETM\_TASK\_P8\_CFG\_REG (0x00C0)

|            |    |    |    |                              |    |    |    |            |    |    |    |                              |   |   |   |            |     |   |   |                              |  |  |  |            |  |  |  |                              |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|------------|----|----|----|------------------------------|---|---|---|------------|-----|---|---|------------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO35_SEL |    |    |    | (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO34_SEL |   |   |   | (reserved) |     |   |   | GPIO_EXT_ETM_TASK_GPIO33_SEL |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO32_SEL |  |  |  |
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO35_EN  |    |    |    | (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO34_EN  |   |   |   | (reserved) |     |   |   | GPIO_EXT_ETM_TASK_GPIO33_EN  |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO32_EN  |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17         | 16 | 15 | 12 | 11                           | 9 | 8 | 7 | 4          | 3   | 1 | 0 |                              |  |  |  |            |  |  |  |                              |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0x0                          | 0 | 0 | 0 | 0          | 0x0 | 0 | 0 | Reset                        |  |  |  |            |  |  |  |                              |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 32 - 35)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 32 - 35)** Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.58. GPIO\_EXT\_ETM\_TASK\_P9\_CFG\_REG (0x00C4)

|            |    |   |   |                              |    |  |  |                             |    |    |   |            |     |    |  |                              |    |    |    |                             |   |     |   |            |  |   |   |                              |   |   |     |                             |  |  |   |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|---|---|------------------------------|----|--|--|-----------------------------|----|----|---|------------|-----|----|--|------------------------------|----|----|----|-----------------------------|---|-----|---|------------|--|---|---|------------------------------|---|---|-----|-----------------------------|--|--|---|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |   |   | GPIO_EXT_ETM_TASK_GPIO39_SEL |    |  |  | GPIO_EXT_ETM_TASK_GPIO39_EN |    |    |   | (reserved) |     |    |  | GPIO_EXT_ETM_TASK_GPIO38_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO38_EN |   |     |   | (reserved) |  |   |   | GPIO_EXT_ETM_TASK_GPIO37_SEL |   |   |     | GPIO_EXT_ETM_TASK_GPIO37_EN |  |  |   | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO36_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO36_EN |  |  |  |
| 31         | 28 |   |   | 27                           | 25 |  |  | 24                          | 23 | 20 |   |            | 19  | 17 |  |                              | 16 | 15 | 12 |                             |   | 11  | 9 |            |  | 8 | 7 | 4                            |   |   | 3   | 1                           |  |  | 0 |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0 | 0 | 0x0                          |    |  |  | 0                           | 0  | 0  | 0 | 0          | 0x0 |    |  |                              | 0  | 0  | 0  | 0                           | 0 | 0x0 |   |            |  | 0 | 0 | 0                            | 0 | 0 | 0x0 |                             |  |  | 0 | Reset      |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 36 - 39)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 36 - 39) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

Register 8.59. GPIO\_EXT\_ETM\_TASK\_P10\_CFG\_REG (0x00C8)

|            |    |    |    |                              |    |    |    |                             |    |     |    |            |   |   |   |                              |   |   |   |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|-----------------------------|----|-----|----|------------|---|---|---|------------------------------|---|---|---|-----------------------------|---|---|---|------------|---|-------|--|------------------------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO43_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO43_EN |    |     |    | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO42_SEL |   |   |   | GPIO_EXT_ETM_TASK_GPIO42_EN |   |   |   | (reserved) |   |       |  | GPIO_EXT_ETM_TASK_GPIO41_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO41_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO40_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO40_EN |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17                          | 16 | 15  | 12 | 11         | 9 | 8 | 7 | 4                            | 3 | 1 | 0 |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0                           | 0  | 0x0 | 0  | 0          | 0 | 0 | 0 | 0x0                          | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0x0        | 0 | Reset |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 40 - 43)** Configures whether or not to enable GPIO $n$  to re-  
sponse ETM task.  
0: Not enable  
1: Enable  
(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 40 - 43)** Configures to select an ETM task channel for  
GPIO $n$ .  
0: Select channel 0  
1: Select channel 1  
.....  
7: Select channel 7  
(R/W)

### Register 8.60. GPIO\_EXT\_ETM\_TASK\_P11\_CFG\_REG (0x00CC)

|            |    |    |    |                              |    |    |    |            |    |     |    |                              |   |   |   |            |   |   |   |                              |     |   |       |            |  |  |  |                              |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|------------|----|-----|----|------------------------------|---|---|---|------------|---|---|---|------------------------------|-----|---|-------|------------|--|--|--|------------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO47_SEL |    |    |    | (reserved) |    |     |    | GPIO_EXT_ETM_TASK_GPIO46_SEL |   |   |   | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO45_SEL |     |   |       | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO44_SEL |  |  |  |
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO47_EN  |    |    |    | (reserved) |    |     |    | GPIO_EXT_ETM_TASK_GPIO46_EN  |   |   |   | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO45_EN  |     |   |       | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO44_EN  |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17         | 16 | 15  | 12 | 11                           | 9 | 8 | 7 | 4          | 3 | 1 | 0 |                              |     |   |       |            |  |  |  |                              |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0          | 0  | 0x0 | 0  | 0                            | 0 | 0 | 0 | 0x0        | 0 | 0 | 0 | 0                            | 0x0 | 0 | Reset |            |  |  |  |                              |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 44 - 47)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 44 - 47) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

Register 8.61. GPIO\_EXT\_ETM\_TASK\_P12\_CFG\_REG (0x00D0)

|            |    |    |    |                              |    |    |    |                             |    |     |    |            |   |   |   |                              |   |   |   |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
|------------|----|----|----|------------------------------|----|----|----|-----------------------------|----|-----|----|------------|---|---|---|------------------------------|---|---|---|-----------------------------|---|---|---|------------|---|-------|--|------------------------------|--|--|--|-----------------------------|--|--|--|------------|--|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | GPIO_EXT_ETM_TASK_GPIO51_SEL |    |    |    | GPIO_EXT_ETM_TASK_GPIO51_EN |    |     |    | (reserved) |   |   |   | GPIO_EXT_ETM_TASK_GPIO50_SEL |   |   |   | GPIO_EXT_ETM_TASK_GPIO50_EN |   |   |   | (reserved) |   |       |  | GPIO_EXT_ETM_TASK_GPIO49_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO49_EN |  |  |  | (reserved) |  |  |  | GPIO_EXT_ETM_TASK_GPIO48_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO48_EN |  |  |  |
| 31         | 28 | 27 | 25 | 24                           | 23 | 20 | 19 | 17                          | 16 | 15  | 12 | 11         | 9 | 8 | 7 | 4                            | 3 | 1 | 0 |                             |   |   |   |            |   |       |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |
| 0          | 0  | 0  | 0  | 0x0                          | 0  | 0  | 0  | 0                           | 0  | 0x0 | 0  | 0          | 0 | 0 | 0 | 0x0                          | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0x0        | 0 | Reset |  |                              |  |  |  |                             |  |  |  |            |  |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 48 - 51)** Configures whether or not to enable GPIO $n$  to re-  
sponse ETM task.  
0: Not enable  
1: Enable  
(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL ( $n$ : 48 - 51)** Configures to select an ETM task channel for GPIO $n$ .  
0: Select channel 0  
1: Select channel 1  
.....  
7: Select channel 7  
(R/W)



### Register 8.62. GPIO\_EXT\_ETM\_TASK\_P13\_CFG\_REG (0x00D4)

|                         |  |  |  |  |  |  |  |  |  |  |  |                              |  |    |           |                             |     |    |   |            |  |     |   |                              |   |       |  |                             |  |   |   |            |   |  |  |                              |  |  |  |                             |  |  |  |
|-------------------------|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|----|-----------|-----------------------------|-----|----|---|------------|--|-----|---|------------------------------|---|-------|--|-----------------------------|--|---|---|------------|---|--|--|------------------------------|--|--|--|-----------------------------|--|--|--|
| (reserved)              |  |  |  |  |  |  |  |  |  |  |  | GPIO_EXT_ETM_TASK_GPIO54_SEL |  |    |           | GPIO_EXT_ETM_TASK_GPIO54_EN |     |    |   | (reserved) |  |     |   | GPIO_EXT_ETM_TASK_GPIO53_SEL |   |       |  | GPIO_EXT_ETM_TASK_GPIO53_EN |  |   |   | (reserved) |   |  |  | GPIO_EXT_ETM_TASK_GPIO52_SEL |  |  |  | GPIO_EXT_ETM_TASK_GPIO52_EN |  |  |  |
| 31                      |  |  |  |  |  |  |  |  |  |  |  | 20                           |  | 19 | 17        |                             | 16  | 15 |   | 12         |  | 11  | 9 |                              | 8 | 7     |  | 4                           |  | 3 | 1 |            | 0 |  |  |                              |  |  |  |                             |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  | 0x0                          |  | 0  | 0 0 0 0 0 |                             | 0x0 |    | 0 | 0 0 0 0 0  |  | 0x0 |   | 0                            |   | Reset |  |                             |  |   |   |            |   |  |  |                              |  |  |  |                             |  |  |  |

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_EN ( $n$ : 52 - 54)** Configures whether or not to enable GPIO $n$  to response ETM task.

0: Not enable

1: Enable

(R/W)

**GPIO\_EXT\_ETM\_TASK\_GPIO $n$ \_SEL** ( $n$ : 52 - 54) Configures to select an ETM task channel for GPIO $n$ .

0: Select channel 0

1: Select channel 1

• • • • •

7: Select channel 7

(R/W)

### Register 8.63. GPIO\_EXT\_VERSION\_REG (0x00FC)

|            |    |    |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |
|------------|----|----|---|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|-------|
| (reserved) |    |    |   | GPIO_EXT_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |
| 31         | 28 | 27 |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |       |
| 0          | 0  | 0  | 0 | 0x2203050     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  | Reset |

**GPIO\_EXT\_DATE** Version control register.

(R/W)

#### 8.20.4 LP GPIO Matrix Registers

The addresses in this section are relative to LP GPIO matrix base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section IX.

(reserved)

LP\_GPIO\_CLK\_EN

(R/W)

(reserved)

LP\_GPIO\_VER\_DATE

(R/W)

(reserved)

LP\_GPIO\_OUT\_DATA

(R/W/WTC)

**Register 8.67. LP\_GPIO\_OUT\_W1TS\_REG (0x000C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | LP_GPIO_OUT_DATA_W1TS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |

**LP\_GPIO\_OUT\_DATA\_W1TS** Configures whether or not to set the output register [LP\\_GPIO\\_OUT\\_REG](#) of GPIO0 ~ GPIO15.

0: Not set

1: The corresponding bit in [LP\\_GPIO\\_OUT\\_REG](#) will be set to 1

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid. Recommended operation: use this register to set [LP\\_GPIO\\_OUT\\_REG](#).

(WT)

**Register 8.68. LP\_GPIO\_OUT\_W1TC\_REG (0x0010)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | LP_GPIO_OUT_DATA_W1TC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

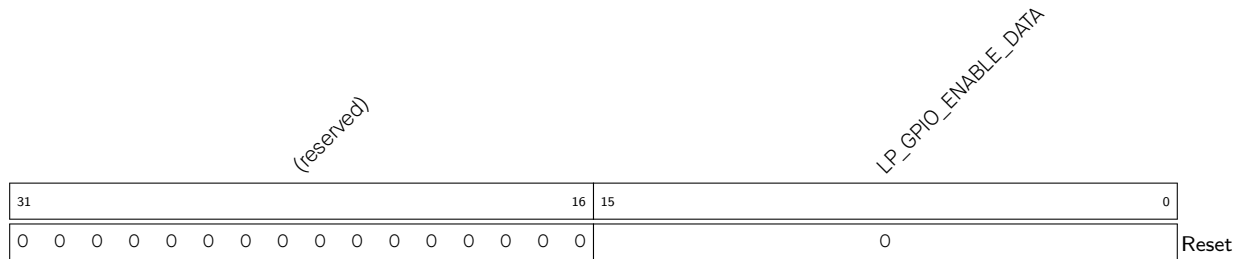
**LP\_GPIO\_OUT\_DATA\_W1TC** Configures whether or not to clear the output register [LP\\_GPIO\\_OUT\\_REG](#) of GPIO0 ~ GPIO15 output.

0: Not clear

1: The corresponding bit in [LP\\_GPIO\\_OUT\\_REG](#) will be cleared.

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid. Recommended operation: use this register to clear [LP\\_GPIO\\_OUT\\_REG](#).

(WT)

**Register 8.69. LP\_GPIO\_ENABLE\_REG (0x0014)**

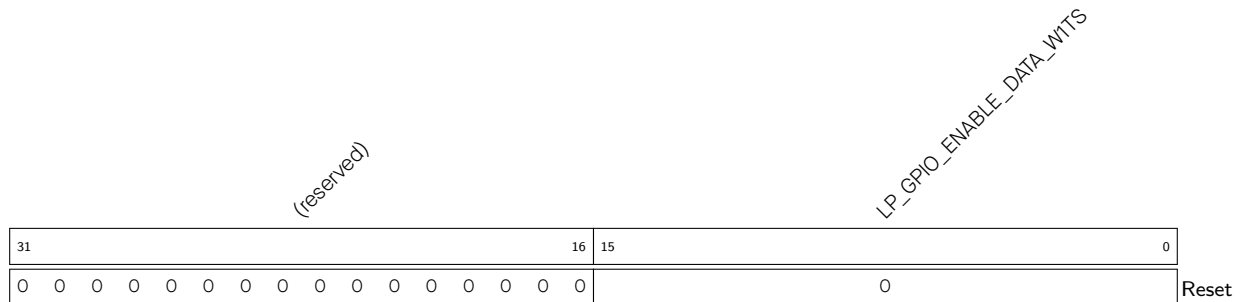
**LP\_GPIO\_ENABLE\_DATA** Configures whether or not to enable the output of GPIO0 ~ GPIO15.

0: Not enable

1: Enable

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid.

(R/W/WTC)

**Register 8.70. LP\_GPIO\_ENABLE\_W1TS\_REG (0x0018)**

**LP\_GPIO\_ENABLE\_DATA\_W1TS** Configures whether or not to set the output enable register [LP\\_GPIO\\_ENABLE\\_REG](#) of GPIO0 ~ GPIO15.

0: Not set

1: The corresponding bit in [LP\\_GPIO\\_ENABLE\\_REG](#) will be set to 1

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid. Recommended operation: use this register to set [LP\\_GPIO\\_ENABLE\\_REG](#).

(WT)

### Register 8.71. LP\_GPIO\_ENABLE\_W1TC\_REG (0x001C)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_GPIO_ENABLE_DATA_W1TC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_GPIO\_ENABLE\_DATA\_W1TC** Configures whether or not to clear the output enable register **LP\_GPIO\_ENABLE\_REG** of GPIO0 ~ GPIO15.

0: Not clear

1: The corresponding bit in `LP_GPIO_ENABLE_REG` will be cleared

Bit0 ~ bit15 are corresponding to GPIO0 ~ 15. Bit16 ~ bit31 are invalid. Recommended operation: use this register to clear [LP\\_GPIO\\_ENABLE\\_REG](#).

(WT)

### Register 8.72. LP\_GPIO\_STATUS\_REG (0x0020)

Diagram illustrating the structure of the LP\_GPIO\_STATUS register:

- Bits 31 to 16: (reserved)
- Bits 15 to 0: LP\_GPIO\_STATUS\_DATA
- Bit 0: Reset

**LP\_GPIO\_STATUS\_DATA** The interrupt status of GPIO0 ~ GPIO15, can be configured by the software.  
Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid.

Each bit represents the status of its corresponding GPIO:

0: Represents the GPIO does not generate the interrupt configured by `LP_GPIO_PIN $n$ _INT_TYPE`, or this bit is configured to 0 by the software.

1: Represents the GPIO generates the interrupt configured by `LP_GPIO_PIN $n$ _INT_TYPE`, or this bit is configured to 1 by the software.

(R/W/WTC)

**Register 8.73. LP\_GPIO\_STATUS\_WITS\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |    |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_GPIO_STATUS_DATA_WITS |    |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                       | 15 |  |  |  |  |  |  |  |  |  |  |  |  |       |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        |    |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |   |

**LP\_GPIO\_STATUS\_DATA\_WITS** Configures whether or not to set the interrupt status register [LP\\_GPIO\\_STATUS\\_DATA](#) of GPIO0 ~ GPIO15.

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid.

If the value 1 is written to a bit here, the corresponding bit in [LP\\_GPIO\\_STATUS\\_DATA](#) will be set to 1.

Recommended operation: use this register to set [LP\\_GPIO\\_STATUS\\_DATA](#).

(WT)

**Register 8.74. LP\_GPIO\_STATUS\_W1TC\_REG (0x0028)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_GPIO_STATUS_DATA_W1TC |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                       | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        |    |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

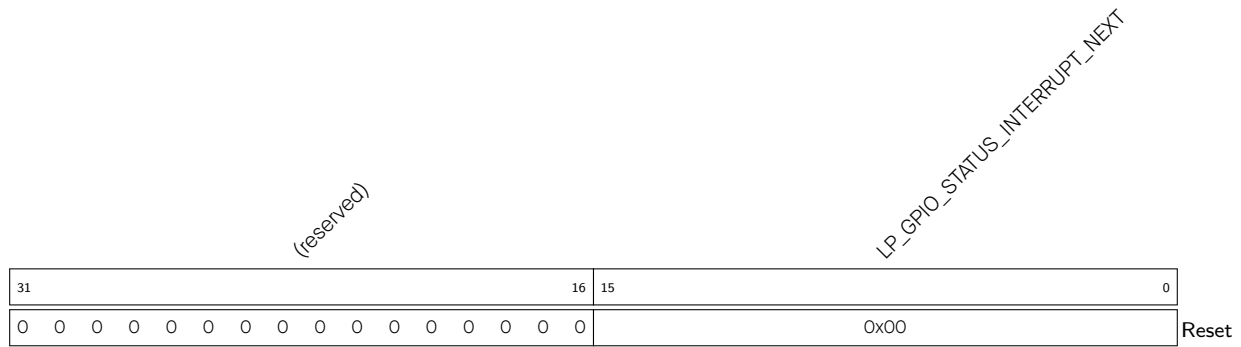
**LP\_GPIO\_STATUS\_DATA\_W1TC** Configures whether or not to clear the interrupt status register [LP\\_GPIO\\_STATUS\\_DATA](#) of GPIO0 ~ GPIO15.

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid.

If the value 1 is written to a bit here, the corresponding bit in [LP\\_GPIO\\_STATUS\\_DATA](#) will be cleared.

Recommended operation: use this register to clear [LP\\_GPIO\\_STATUS\\_DATA](#).

(WT)

**Register 8.75. LP\_GPIO\_STATUS\_NEXT\_REG (0x002C)**

**LP\_GPIO\_STATUS\_INTERRUPT\_NEXT** Represents the interrupt source signal of GPIO0 ~ GPIO15.

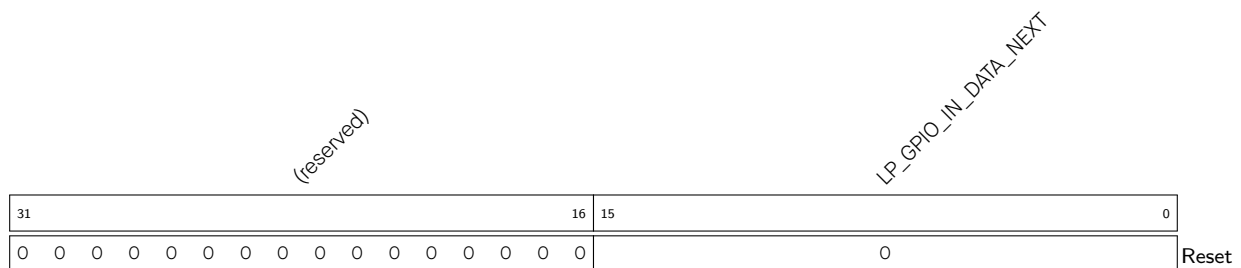
Bit0 ~ bit15 are corresponding to GPIO0 ~ 15. Bit16 ~ bit31 are invalid. Each bit represents:

0: The GPIO does not generate the interrupt configured by [LP\\_GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#).

1: The GPIO generates an interrupt configured by [LP\\_GPIO\\_PIN<sub>n</sub>\\_INT\\_TYPE](#).

The interrupt could be rising edge interrupt, falling edge interrupt, level sensitive interrupt and any edge interrupt.

(RO)

**Register 8.76. LP\_GPIO\_IN\_REG (0x0030)**

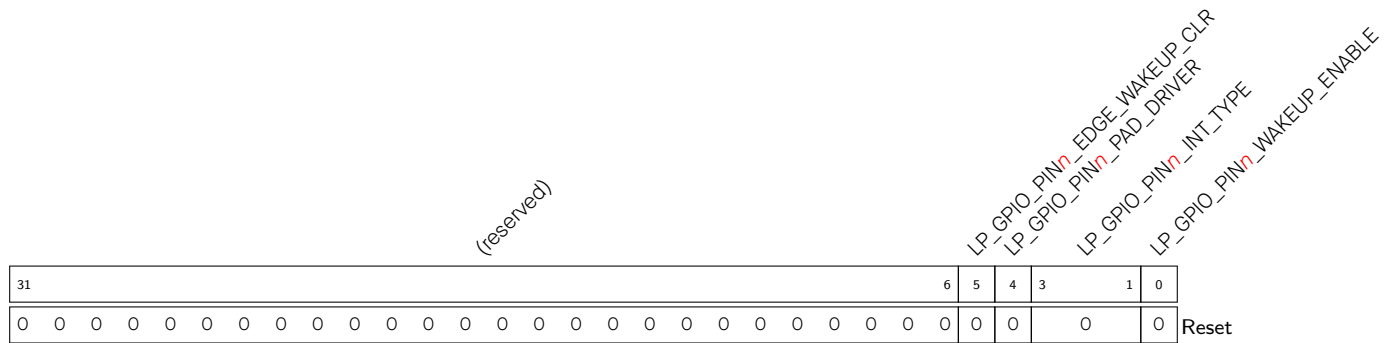
**LP\_GPIO\_IN\_DATA\_NEXT** Represents the input value of GPIO0 ~ GPIO15. Each bit represents a pin input value:

0: Low level

1: High level

Bit0 ~ bit15 are corresponding to GPIO0 ~ GPIO15. Bit16 ~ bit31 are invalid.

(RO)

Register 8.77. LP\_GPIO\_PIN $n$ \_REG ( $n$ : 0 - 15) (0x0034+4\* $n$ )

**LP\_GPIO\_PIN $n$ \_WAKEUP\_ENABLE** Configures whether or not to enable GPIO wake-up function.

0: Disable

1: Enable

This function only wakes up system from Deep-sleep.

(R/W)

**LP\_GPIO\_PIN $n$ \_INT\_TYPE** Configures GPIO interrupt type.

0: GPIO interrupt disabled

1: Rising edge trigger

2: Falling edge trigger

3: Any edge trigger

4: Low level trigger

5: High level trigger

(R/W)

**LP\_GPIO\_PIN $n$ \_PAD\_DRIVER** Configures to select pin drive mode.

0: Normal output

1: Open drain output

(R/W)

**LP\_GPIO\_PIN $n$ \_EDGE\_WAKEUP\_CLR** Configures to clear edge-triggered GPIO wake-up source in PMU.

1: The corresponding bit in LP\_PMU\_xxx will be cleared.

0: No effect.

(WT)



Register 8.78. LP\_GPIO\_FUNC $n$ \_IN\_SEL\_CFG\_REG ( $n$ : 0 - 15) (0x0074+4\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |   |        |  |                           |   |        |  |                           |  |            |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|---|--------|--|---------------------------|---|--------|--|---------------------------|--|------------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_GPIO_FUNC <sub>n</sub> |   | IN_SEL |  | LP_GPIO_FUNC <sub>n</sub> |   | IN_SEL |  | LP_GPIO_FUNC <sub>n</sub> |  | IN_INV_SEL |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                         | 7 | 2      |  | 1                         | 0 |        |  |                           |  |            |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x30                      |   |        |  | 0                         | 0 | Reset  |  |                           |  |            |  |

**LP\_GPIO\_FUNC $n$ \_IN\_INV\_SEL** Configures whether or not to invert the input value.

0: Not invert

1: Invert

(R/W)

**LP\_GPIO\_SIG<sub>n</sub>\_IN\_SEL** Configures whether or not to route signals via LP GPIO matrix.

0: Bypass LP GPIO matrix, i.e., connect signals directly to peripheral configured in LP IO MUX.

1: Route signals via LP GPIO matrix.

(R/W)

**LP\_GPIO\_FUNC*n*\_IN\_SEL** Configures to select a pin from the 16 LP GPIO pins to connect the input signal *n*.

0: Select GPIO0

1: Select GPIO1

• • • • •

14: Select GPIO14

15: Select GPIO15

16 ~ 31: Invalid

32 ~ 47: A constantly low input

48 ~ 63: A constantly high input

(R/W)

Register 8.79. LP\_GPIO\_FUNC $n$ \_OUT\_SEL\_CFG\_REG ( $n$ : 0 - 15) (0x00F4+4\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |   |  |  |  |   |   |       |                                   |  |  |  |                                       |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|---|--|--|--|---|---|-------|-----------------------------------|--|--|--|---------------------------------------|--|--|--|--|--|--|--|--|--|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_GPIO_FUNC <sub>n</sub> _OUT_SEL |   |  |  | LP_GPIO_FUNC <sub>n</sub> _OUT_INV_SEL |   |   |       | LP_GPIO_FUNC <sub>n</sub> _OE_SEL |  |  |  | LP_GPIO_FUNC <sub>n</sub> _OE_INV_SEL |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                                  | 8 |  |  |  | 3 | 2 | 1     | 0                                 |  |  |  |                                       |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x20                               |   |  |  | 0                                      | 0 | 0 | Reset |                                   |  |  |  |                                       |  |  |  |  |  |  |  |  |  |  |

**LP\_GPIO\_FUNC $n$ \_OE\_INV\_SEL** Configures whether or not to invert the output enable signal.

0: Not invert

1: Invert

(R/W)

**LP\_GPIO\_FUNC $n$ \_OE\_SEL** Configures to select the source of output enable signal.

0: Use output enable signal from peripheral.

1: Force the output enable signal to be sourced from bit $n$  of [LP\\_GPIO\\_ENABLE\\_REG](#).

(R/W)

**LP\_GPIO\_FUNC $n$ \_OUT\_INV\_SEL** Configures whether or not to invert the output value.

0: Not invert

1: Invert

(R/W)

**LP\_GPIO\_FUNC $n$ \_OUT\_SEL** Configures to select a signal  $Y$  ( $0 \leq Y < 32$ ) from 31 peripheral signals to be output to GPIO $n$ .

0: Select signal 0

1: Select signal 1

.....

30: Select signal 30

31: Select signal 31

Or

32: Bit $n$  of [LP\\_GPIO\\_OUT\\_REG](#) and [LP\\_GPIO\\_ENABLE\\_REG](#) are selected as the output value and output enable.

For the detailed signal list, see Table 8.13-1.

(R/W)

## 8.20.5 LP IO MUX Registers

The addresses in this section are relative to LP IO MUX base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section IX.

Register 8.80. LP\_IOMUX\_CLK\_EN\_REG (0x0000)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_IOMUX_CLK_EN |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1               | 0 |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 0 | 1 | Reset |

**LP\_IOMUX\_CLK\_EN** Configures whether or not to enable clock gate.

0: Not enable

1: Enable, the clock is free running.

(R/W)

Register 8.81. LP\_IOMUX\_VER\_DATE\_REG (0x0004)

|            |   |   |    |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
|------------|---|---|----|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|
| (reserved) |   |   |    | LP_IOMUX_VER_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
| 31         |   |   | 28 | 27                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |
| 0          | 0 | 0 | 0  | 0x230313          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |

**LP\_IOMUX\_VER\_DATE** Version control register.

(R/W)

Register 8.82. LP\_IOMUX\_PAD $n$ \_REG ( $n = 0 - 15$ ) (0x0008+4\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |   |   |   |   |   |   |   |   |   |       |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|---|---|---|---|---|---|---|---|---|-------|--|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_IOMUX_PAD <sub>n</sub> _FILTER_EN<br>LP_IOMUX_PAD <sub>n</sub> _FUN_IE<br>LP_IOMUX_PAD <sub>n</sub> _SLP_OE<br>LP_IOMUX_PAD <sub>n</sub> _SLP_IE<br>LP_IOMUX_PAD <sub>n</sub> _FUN_SEL<br>LP_IOMUX_PAD <sub>n</sub> _MUX_SEL<br>LP_IOMUX_PAD <sub>n</sub> _RUE<br>LP_IOMUX_PAD <sub>n</sub> _RDE<br>LP_IOMUX_PAD <sub>n</sub> _DRV |    |    |   |   |   |   |   |   |   |   |   |       |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12  | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0 | 0 | 0 |   | 0 | 0 | 0 | 0 | 2 | Reset |  |  |

**LP\_IOMUX\_PAD $n$ \_DRV** Configures the drive strength of GPIO $n$ .

- 0: ~5 mA
- 1: ~10 mA
- 2: ~20 mA
- 3: ~40 mA
- (R/W)

**LP\_IOMUX\_PAD $n$ \_RDE** Configures whether or not enable pull-down resistor of GPIO $n$ .

- 0: Disable
- 1: Enable
- (R/W)

**LP\_IOMUX\_PAD $n$ \_RUE** Configures whether or not to enable pull-up resistor of GPIO $n$ .

- 0: Disable
- 1: Enable
- (R/W)

**LP\_IOMUX\_PAD $n$ \_MUX\_SEL** Configures to decide GPIO $n$  is used by HP IO MUX or LP IO MUX.

- 0: GPIO $n$  is used by HP IO MUX
- 1: GPIO $n$  is used by LP IO MUX
- (R/W)

**LP\_IOMUX\_PAD $n$ \_FUN\_SEL** Configures to select LP IO MUX function for this signal.

- 0: Select Function 0
- 1: Select Function 1
- .....
- (R/W)

**LP\_IOMUX\_PAD $n$ \_SLP\_SEL** Configures whether or not to enter sleep mode for GPIO $n$ .

- 0: Not enter
- 1: Enter
- (R/W)

**LP\_IOMUX\_PAD $n$ \_SLP\_IE** Configures whether or not to enable the input of GPIO $n$  during sleep mode.

- 0: Disable
- 1: Enable
- (R/W)

Continued on the next page...

Register 8.83. LP\_IOMUX\_PADn\_REG (n = 0 - 15) (0x0008+4\*n)

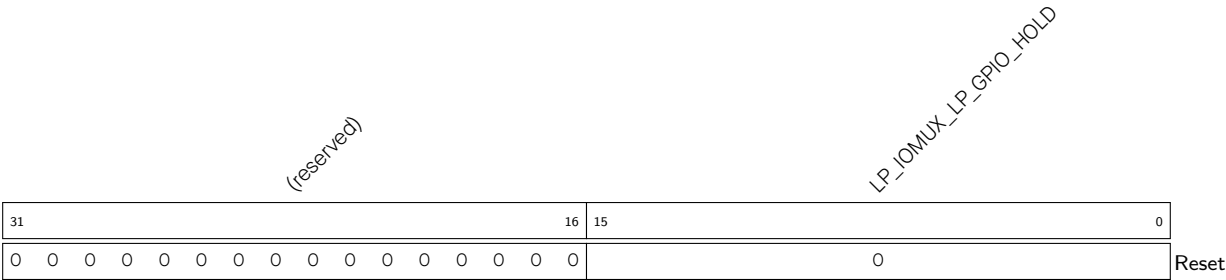
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**LP\_IOMUX\_PADn\_SLP\_OE** Configures whether or not to enable the output of GPIO $n$  in sleep mode.  
0: Disable  
1: Enable  
(R/W)

**LP\_IOMUX\_PADn\_FUN\_IE** Configures whether or not to enable input of GPIO $n$ .  
0: Disable  
1: Enable  
(R/W)

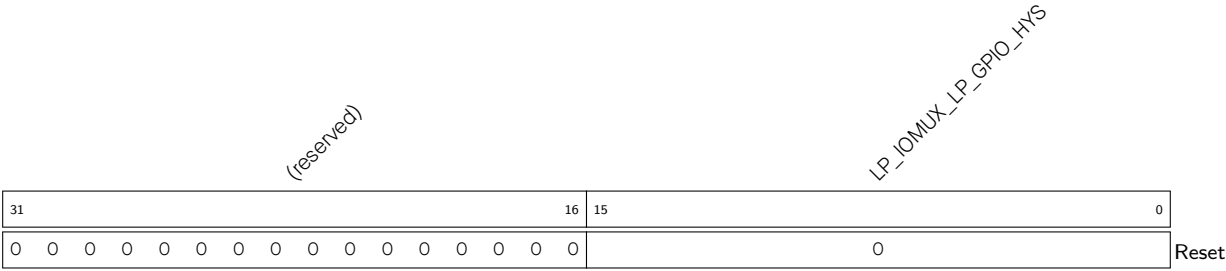
**LP\_IOMUX\_PADn\_FILTER\_EN** Configures whether or not to enable filter for pin input signals.  
0: Disable  
1: Enable  
(R/W)

Register 8.84. LP\_IOMUX\_LP\_PAD\_HOLD\_REG (0x004C)



**LP\_IOMUX\_LP\_GPIO\_HOLD** Configures whether or not to enable hold function of GPIO $n$ .  
0: Disable  
1: Enable  
(R/W)

Register 8.85. LP\_IOMUX\_LP\_PAD\_HYS\_REG (0x0050)



**LP\_IOMUX\_LP\_GPIO\_HYS** Configures whether or not to enable hysteresis function of GPIO<sub>n</sub>.  
0: Disable  
1: Enable  
Bit0 bit15 are corresponding to GPIO0 GPIO15.  
(R/W)

## Chapter 9

## Reset and Clock

### 9.1 Reset

#### 9.1.1 Overview

ESP32-P4 provides four types of reset that occur at different levels, namely CPU Reset, Core Reset, System Reset, and Chip Reset. All reset types mentioned above (except Chip Reset) preserve the data stored in internal memory. Figure 9.1-1 shows the scopes of affected subsystems by each type of reset.

#### 9.1.2 Architectural Overview

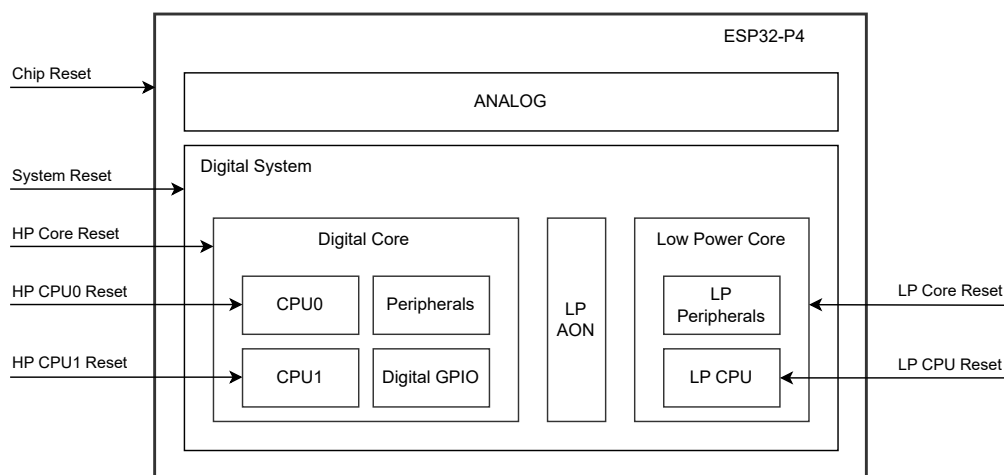


Figure 9.1-1. Reset Types

ESP32-P4's Digital System consists of [High Performance System \(HP system\)](#) that includes Digital Core and HP memory, and [Low Power System \(LP system\)](#) that includes the Low Power Always On (LP AON) system, LP Core, and LP memory. See Figure 9.1-1 for details (note that HP memory and LP memory would not be reset, so they are not shown in the figure).

#### 9.1.3 Features

- Four reset types:
  - CPU Reset: resets CPU core. HP CPU0, HP CPU1, and LP CPU can be reset independently:
    - \* HP CPU0 will be automatically released from reset after chip power-up, and start execution from CPU Reset Vector (0x30100000).

- \* HP CPU1 is at reset by default after chip power-up, and needs to be manually released from reset by writing 0 to [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_CORE1\\_GLOBAL](#). Once released from reset, HP CPU1 will start execution from CPU Reset Vector (0x30100000).
- \* LP CPU is at reset after chip power-up, and needs to be manually released from reset by configuring the power management unit (PMU). Once released from reset, LP CPU will start execution from LP\_SYSTEM\_LP\_CPU\_BOOT\_ADDR (0x50100000 by default). For details, see Chapter 13 [Low-Power Management](#).
- Core Reset: resets the whole digital system except for LP AON. HP core and LP core can be reset independently: HP Core Reset resets HP CPU0, HP CPU1, HP peripherals, HP GPIO, etc., and LP Core Reset resets LP CPU and LP peripherals.
- System Reset: resets the whole digital system, including the LP system.
- Chip Reset: resets the whole chip.
- Software reset and hardware reset:
  - Software Reset: triggered via software by configuring the corresponding registers of CPU, see Chapter 13 [Low-Power Management](#).
  - Hardware Reset: triggered directly by the hardware.

## 9.1.4 Functional Description

CPU will be reset immediately when any type of reset above occurs. After the reset is released, users can retrieve reset source codes by reading the following fields:

- HP CPU0: [LP\\_CLKRST\\_HPCORE0\\_RESET\\_CAUSE](#)
- HP CPU1: [LP\\_CLKRST\\_HPCORE1\\_RESET\\_CAUSE](#)
- LP CPU: [LP\\_CLKRST\\_LPCORE\\_RESET\\_CAUSE](#)

Table 9.1-1 and Table 9.1-2 list possible reset sources and the types of reset they trigger.

**Table 9.1-1. HP CPU Reset Source**

| Code | Source                       | Reset Type      | Note  |
|------|------------------------------|-----------------|---|
| 0x01 | Chip reset <sup>1</sup>      | Chip Reset      | —   |
| 0x03 | Software system reset        | HP Core Reset   | Triggered by configuring <a href="#">LP_SYSTEM_SYS_SW_RST</a>   |
| 0x05 | PMU core reset               | HP Core Reset   | See Chapter 13 <a href="#">Low-Power Management</a>   |
| 0x07 | MWDT core reset <sup>2</sup> | HP Core Reset   | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>  |
| 0x09 | RWDT core reset              | HP Core Reset   | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>  |
| 0x0B | MWDT CPU reset               | HP CPU0/1 Reset | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>  |
| 0x0C | Software CPU reset           | HP CPU0/1 Reset | Triggered by configuring <a href="#">LP_CLKRST_HPCORE0_SW_RESET</a> or <a href="#">LP_CLKRST_HPCORE1_SW_RESET</a> |
| 0x0D | RWDT CPU reset               | HP CPU0/1 Reset | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>  |

Cont'd on next page



Table 9.1-1 – cont'd from previous page

| Code | Source                 | Reset Type                 | Note   |
|------|------------------------|----------------------------|--|
| 0x0F | Brown-out system reset | Chip Reset or System Reset | Triggered by the brown-out detector. Once brown-out status is detected, the detector will trigger System Reset or Chip Reset, depending on the register configuration. See Chapter 13 <a href="#">Low-Power Management</a> |
| 0x10 | RWDT system reset      | System Reset               | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>   |
| 0x12 | Super Watchdog reset   | System Reset               | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>   |
| 0x13 | Power glitch reset     | System Reset               | See Chapter 21 <a href="#">Brown-out Detector</a>  |
| 0x14 | eFuse reset            | HP Core Reset              | Triggered by eFuse CRC error   |
| 0x16 | USB (JTAG) reset       | HP Core Reset              | Triggered when external USB host sends a specific command to the JTAG interface of USB Serial/JTAG Controller. See Chapter 46 <a href="#">USB Serial/JTAG Controller (USB_SERIAL_JTAG)</a>                                 |
| 0x17 | USB (UART) reset       | HP Core Reset              | Triggered when external USB host sends a specific command to the serial interface of USB Serial/JTAG Controller. See Chapter 46 <a href="#">USB Serial/JTAG Controller (USB_SERIAL_JTAG)</a>                               |
| 0x18 | JTAG CPU reset         | HP CPU0/1 Reset            | Triggered when a “GDB Resetting CPU” instruction is received   |
| 0x1A | Lockup reset           | HP CPU0/1 Reset            | Triggered when the CPU enters lockup. HP CPU0 and HP CPU1 can be reset in lockup state by configuring <a href="#">LP_CLKRST_HPCORE<sub>x</sub>_LOCKUP_RESET_EN</a>   |

<sup>1</sup> Chip Reset can be triggered by the following sources:

- Chip power-up
- Brown-out detector

<sup>2</sup> The HP system contains two watchdog timers called Main System Watchdog Timers (MWDT), and the MWDT that can trigger reset can be configured via [HP\\_SYS\\_CLKRST\\_HPCORE0\\_WDT\\_RESET\\_SOURCE\\_SEL](#) and [HP\\_SYS\\_CLKRST\\_HPCORE0\\_WDT\\_RESET\\_SOURCE\\_SEL](#) for HP CPU0 and HP CPU1 respectively.

Table 9.1-2. LP CPU Reset Source

| Code | Source                        | Reset Type                 | Note   |
|------|-------------------------------|----------------------------|--|
| 0x01 | Chip reset                    | Chip Reset                 | —  |
| 0x09 | PMU LP Peripheral reset       | LP Core Reset              | See Chapter 13 <a href="#">Low-Power Management</a>            |
| 0x0A | PMU LP CPU reset <sup>1</sup> | LP CPU Reset               | See Chapter 13 <a href="#">Low-Power Management</a>            |
| 0x0F | Brown-out system reset        | Chip Reset or System Reset | Triggered by the brown-out detector                            |
| 0x10 | RWDT system reset             | System Reset               | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>           |
| 0x12 | Super Watchdog reset          | System Reset               | See Chapter 16 <a href="#">Watchdog Timers (WDT)</a>           |
| 0x13 | Power glitch reset            | System Reset               | See Chapter 21 <a href="#">Brown-out Detector</a>              |
| 0x14 | Software LP CPU reset         | LP CPU Reset               | Triggered by configuring <a href="#">LPPERI_RST_EN_LP_CORE</a> |

Cont'd on next page

Table 9.1-2 – cont'd from previous page

| Code | Source | Reset Type | Note |
|------|--------|------------|------|
|------|--------|------------|------|

<sup>1</sup> LP CPU is reset by PMU after chip power-up. To retrieve the correct reset source code (0x01) when the LP CPU runs for the first time, the source code for PMU LP CPU reset (0x0A) will be masked. After the CPU's first run, clear [LP\\_CLKRST\\_LPCORE\\_RESET\\_CAUSE\\_PMU\\_LP\\_CPU\\_MASK](#) to unmask the 0x0A source code.

## 9.1.5 Peripheral Reset

Peripherals can be reset individually by configuring corresponding registers, or globally by Core Reset, System Reset, or Chip Reset.

ESP32-P4 has three groups of peripheral reset registers, prefixed with HP\_SYS\_CLKRST, LP\_CLKRST, and LPPERI. See Section [9.4 Register Summary](#) for detailed information.

## 9.2 Clock

### 9.2.1 Overview

ESP32-P4 clocks are mainly sourced from oscillator (OSC, including Resistor-Capacitor circuit), crystal (XTAL), and PLL circuit, and then processed by the dividers or selectors, which allows most functional modules to select their working clock according to their power consumption and performance requirements. Figure [9.2-1](#) shows the HP and LP system clock structure, including the main clock path and typical peripheral clock generator circuit. ESP32-P4 has a large number of peripherals, and limited by space, not all peripheral clocks are shown in the figure.

## 9.2.2 Architectural Overview

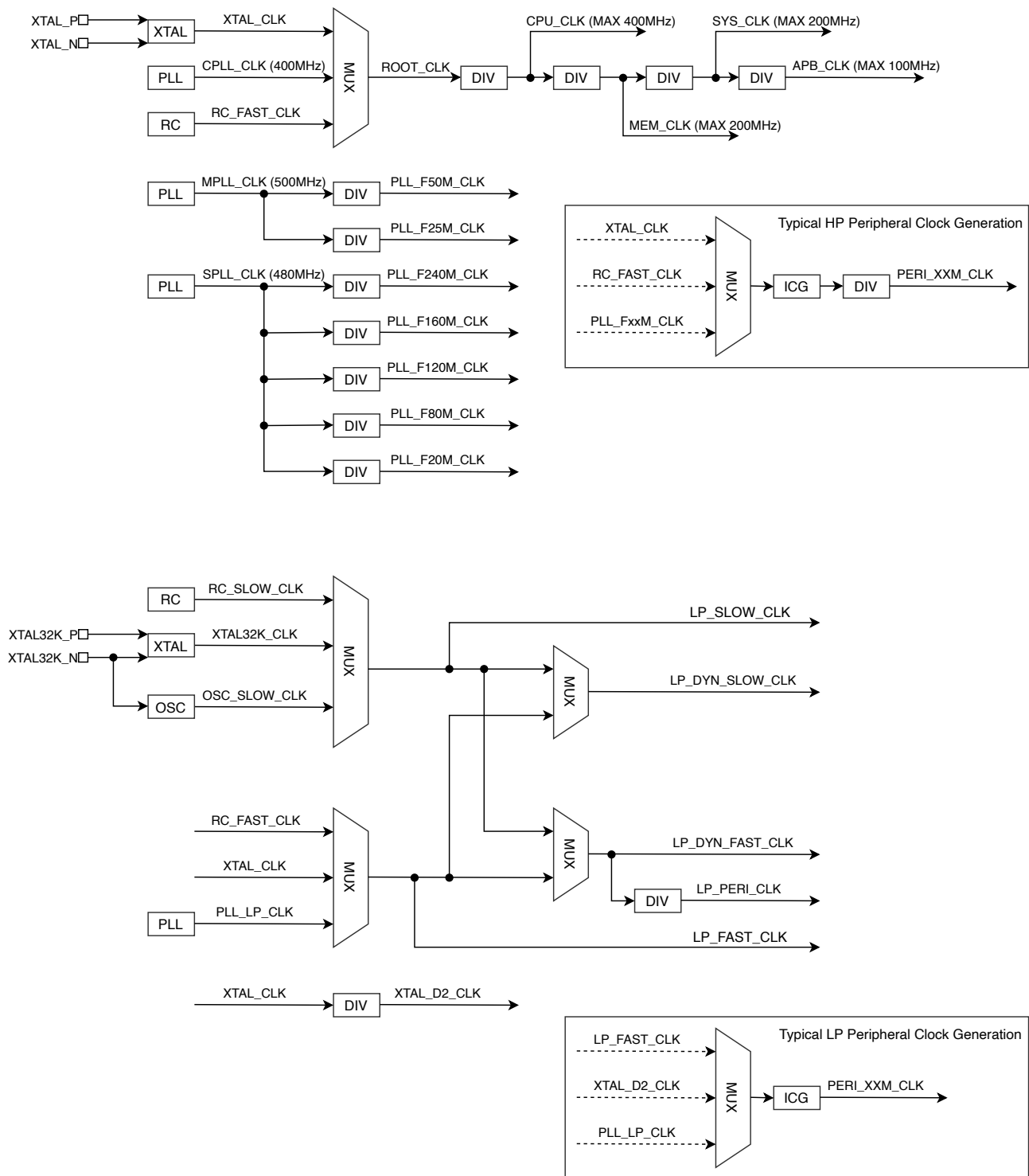


Figure 9.2-1. HP and LP System Clock

## 9.2.3 Features

ESP32-P4 clocks can be classified into two types depending on their frequencies:

- High speed clocks for devices working at a higher frequency, such as HP CPU0/1 and digital peripherals

- CPLL\_CLK: internal 360 MHz PLL clock. Its reference clock is XTAL\_CLK
- MPLL\_CLK: internal 500 MHz PLL clock. Its reference clock is XTAL\_CLK
- SPLL\_CLK: internal 480 MHz PLL clock. Its reference clock is XTAL\_CLK
- Slow speed clocks for LP system and some peripherals working in low-power mode
  - XTAL32K\_CLK: external 32 kHz crystal clock
  - RC\_SLOW\_CLK: internal 150 kHz slow RC oscillator
  - OSC\_SLOW\_CLK: external slow clock input through [XTAL\\_32K\\_N](#), with a frequency of 32 kHz by default. After configuring this GPIO, also configure the Hold function (see Chapter 8 [GPIO Matrix and IO MUX](#) > 8.9 [Pin Hold Feature](#))
  - XTAL\_CLK: 40 MHz external crystal clock
  - RC\_FAST\_CLK: internal fast RC oscillator with adjustable frequency (20 MHz by default)
  - PLL\_LP\_CLK: internal PLL clock with a frequency of 8 MHz by default. Its reference clock can be XTAL32K\_CLK

## 9.2.4 Functional Description

### 9.2.4.1 HP System Clock

As Figure 9.2-1 shows, XTAL\_CLK, CPLL\_CLK, and RC\_FAST\_CLK are the multiplexer inputs to generate ROOT\_CLK. For selecting which input, see Table 9.2-1.

Table 9.2-1. ROOT\_CLK Clock Source

| LP_CLKRST_HP_ROOT_CLK_SRC_SEL | Clock Source |
|-------------------------------|--------------|
| 0                             | XTAL_CLK     |
| 1                             | CPLL_CLK     |
| 2                             | RC_FAST_CLK  |

ROOT\_CLK is then divided by a series of dividers, and sequentially derives:

- CPU\_CLK, which drives HP CPUs and their logic
- MEM\_CLK, which drives the internal memories (L2 Cache, L2MEM, ROM) and their logic
- SYS\_CLK, which is the HP high-speed bus clock that drives the AXI and AHB bus logic
- APB\_CLK, which is the HP low-speed bus clock that drives the APB bus logic

The above four derived clocks are synchronous SoC clocks, asynchronous to peripheral clocks described in Section 9.2.4.3 [Peripheral Clocks](#). Peripheral clocks are asynchronous with each other unless otherwise stated.

The maximum frequencies allowed for these SoC clocks are as follows. Software should ensure that the frequencies of these clocks do not exceed the maximum frequency.

- CPU\_CLK: 360 MHz
- MEM\_CLK: 200 MHz

- SYS\_CLK: 200 MHz
- APB\_CLK: 100 MHz

Each module has an individual clock gate for the SoC clock it uses. For example, users can enable the clock for HP CPU0 and disable the clock for HP CPU1 by setting the [HP\\_SYS\\_CLKRST\\_CORE0\\_CPU\\_CLK\\_EN](#) bit and clearing the [HP\\_SYS\\_CLKRST\\_CORE1\\_CPU\\_CLK\\_EN](#) bit. “CPU\_CLK” in bit names indicates that the corresponding clock belongs to the CPU\_CLK group shown in Figure 9.2-1.

The internal PLL clocks of ESP32-P4, namely MPLL\_CLK and SPLL\_CLK, generate reference clocks for peripherals through a set of parallel clock dividers.

Besides these two PLL clocks, there are two additional PLL clocks dedicated to specific modules:

- SDIO\_PLL, which generates three clocks:
  - SDIO\_PLLO\_CLK, used for SDIO’s high-speed SDIO\_SLF\_CLK (internal signal clock) and the source of SDIO’s low-speed clock
  - SDIO\_PLL1\_CLK, users for SDIO’s high-speed SDIO\_DRV\_CLK (output signal driving clock)
  - SDIO\_PLL2\_CLK, used for SDIO’s high-speed SDIO\_SAM\_CLK (input signal sampling clock)
- APLL\_CLK, which is dedicated to I2S

A typical peripheral clock generation circuit consists of a clock selector, a clock gating unit, and a divider. In high-performance mode, the peripheral can select a high-speed clock source without division for higher processing speed. In low-power mode, the peripheral can select a low-speed clock source or divide it by a large divisor to lower power consumption. When the peripheral is disabled, its clock can be directly disabled.

**Note:**

Updates to [HP\\_SYS\\_CLKRST\\_ROOT\\_CLK\\_CTRL0/1/2/3\\_REG](#) will take effect only after [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) is set.

### 9.2.4.2 LP System Clock

The LP system can operate when most other clocks are disabled. LP system clocks include LP\_SLOW\_CLK, LP\_FAST\_CLK, LP\_DYN\_SLOW\_CLK, LP\_DYN\_FAST\_CLK, and XTAL\_D2\_CLK.

The clock sources for LP\_SLOW\_CLK and LP\_FAST\_CLK are low-frequency clocks:

- LP\_SLOW\_CLK has four clock sources, see Table 9.2-2:

**Table 9.2-2. LP\_SLOW\_CLK Clock Source Selection**

| <a href="#">LP_CLKRST_SLOW_CLK_SEL</a> | Clock Source |
|--|--------------|
| 0                                      | RC_SLOW_CLK  |
| 1                                      | XTAL32K_CLK  |
| 2                                      | Invalid      |
| 3                                      | OSC_SLOW_CLK |

- LP\_FAST\_CLK has three clock sources, see Table 9.2-3:

**Table 9.2-3. LP\_FAST\_CLK Clock Source Selection**

| <a href="#">LP_CLKRST_FAST_CLK_SEL</a> | Clock Source |
|--|--------------|
| 0                                      | XTAL_CLK     |
| 1                                      | RC_FAST_CLK  |
| 2                                      | PLL_LP_CLK   |

LP\_DYN\_SLOW\_CLK and LP\_DYN\_FAST\_CLK can be derived from LP\_SLOW\_CLK or LP\_FAST\_CLK depending on the chip's power mode (see Chapter [13 Low-Power Management](#)), and should be able to operate in all power modes to drive LP AON modules. These two clocks are always synchronous with each other.

- In Active mode, select LP\_FAST\_CLK as the clock source. In this case, LP\_DYN\_SLOW\_CLK has the same frequency with LP\_SLOW\_CLK, and the same phase with LP\_FAST\_CLK;
- In Deep-sleep mode, select the clock source according to PMU configurations. If the LP CPU is off, LP\_SLOW\_CLK is the clock source, and has the same frequency and phase as LP\_DYN\_FAST\_CLK in this case; if the LP CPU is on, LP\_FAST\_CLK is the clock source.

LP\_PERI\_CLK is derived from LP\_DYN\_FAST\_CLK and drives all the buses for LP peripherals.

XTAL\_D2\_CLK is derived from XTAL\_CLK divided by 2.

### 9.2.4.3 Peripheral Clocks

Table [9.2-4](#), Table [9.2-5](#), Table [9.2-6](#), and Table [9.2-7](#) list the derived HP/LP clock sources and HP clocks/LP clocks for each peripheral.

Table 9.2-4. Derived HP Clock sources

| Derived Clock | Source Clock |          |          |          |          |          |               | Derived Clock |         |         |         |              |               |               |
|---------------|--------------|----------|----------|----------|----------|----------|---------------|---------------|---------|---------|---------|--------------|---------------|---------------|
|               | RC_FAST_CLK  | XTAL_CLK | CPLL_CLK | MPLL_CLK | SPLL_CLK | APLL_CLK | SDIO_PLL0_CLK | ROOT_CLK      | CPU_CLK | MEM_CLK | SYS_CLK | PLL_F80M_CLK | PLL_F160M_CLK | PLL_F240M_CLK |
| ROOT_CLK      | Y            | Y        | Y        |          |          |          |               |               | Y       |         |         |              |               |               |
| CPU_CLK       |              |          |          |          |          |          |               |               |         | Y       |         |              |               |               |
| MEM_CLK       |              |          |          |          |          |          |               |               |         | Y       |         |              |               |               |
| SYS_CLK       |              |          |          |          |          |          |               |               |         |         | Y       |              |               |               |
| APB_CLK       |              |          |          |          |          |          |               |               |         |         | Y       |              |               |               |
| PLL_F50M_CLK  |              |          |          | Y        |          |          |               |               |         |         |         |              |               |               |
| PLL_F25M_CLK  |              |          |          | Y        |          |          |               |               |         |         |         |              |               |               |
| PLL_F240M_CLK |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F160M_CLK |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F120M_CLK |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F80M_CLK  |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F20M_CLK  |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F12M_CLK  |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| PLL_F48M_CLK  |              |          |          |          | Y        |          |               |               |         |         |         |              |               |               |
| FLASH_CLK     |              | Y        | Y        |          | Y        |          |               |               |         |         |         |              |               |               |
| PSRAM_CLK     |              | Y        | Y        | Y        | Y        |          |               |               |         |         |         |              |               |               |
| GPSPi_CLK     | Y            | Y        |          |          | Y        | Y        | Y             |               |         |         |         |              |               |               |
| ADC_CLK       | Y            | Y        |          |          |          |          |               |               |         |         |         | Y            |               |               |
| UART_CLK      | Y            | Y        |          |          |          |          |               |               |         |         |         | Y            |               |               |
| CRYPTO_CLK    | Y            | Y        |          |          |          |          |               |               |         |         |         |              | Y             | Y             |

Table 9.2-5. HP Peripheral Clocks

| Peripheral                           | Clock            | Clock Source |          |          |               |              |              |              |              |              |              |               |               |               | Derived Clock |           |           |         |          |            | Clock from IO |
|--------------------------------------|------------------|--------------|----------|----------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|-----------|-----------|---------|----------|------------|---------------|
|                                      |                  | RC_FAST_CLK  | XTAL_CLK | APLL_CLK | SDIO_PLL0_CLK | PLL_F12M_CLK | PLL_F20M_CLK | PLL_F25M_CLK | PLL_F48M_CLK | PLL_F50M_CLK | PLL_F80M_CLK | PLL_F120M_CLK | PLL_F160M_CLK | PLL_F240M_CLK | FLASH_CLK     | PSRAM_CLK | GPSPi_CLK | ADC_CLK | UART_CLK | CRYPTO_CLK |               |
| SPI0/1 (flash)                       | FLASH_PLL_CLK    |              |          |          |               |              |              |              |              |              |              |               |               |               | Y             |           |           |         |          |            |               |
|                                      | FLASH_CORE_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               | Y             |           |           |         |          |            |               |
| SPI0/1 (PSRAM)                       | PSRAM_PLL_CLK    |              |          |          |               |              |              |              |              |              |              |               |               |               |               | Y         |           |         |          |            |               |
|                                      | PSRAM_CORE_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               | Y         |           |         |          |            |               |
| I2S Controller (I2S)                 | I2S_RX_CLK       |              | Y        | Y        |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_I2S_MCLK  |
|                                      | I2S_TX_CLK       |              | Y        | Y        |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_I2S_MCLK  |
| I2C Controller (I2C)                 | I2C_CLK          | Y            | Y        |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            |               |
| Motor Control PWM (MCPWM)            | MCPWM_CLK        | Y            | Y        |          |               |              |              |              | Y            |              |              |               | Y             |               |               |           |           |         |          |            |               |
| Timer Group (TIMG)                   | TIMERGRP_TO_CLK  | Y            | Y        |          |               |              |              |              |              |              | Y            |               |               |               |               |           |           |         |          |            |               |
|                                      | TIMERGRP_T1_CLK  | Y            | Y        |          |               |              |              |              |              |              | Y            |               |               |               |               |           |           |         |          |            |               |
| Main System Watchdog Timer (MWDT)    | TIMERGRP_WDT_CLK | Y            | Y        |          |               |              |              |              | Y            |              | Y            |               |               |               |               |           |           |         |          |            |               |
| Two-Wire Automotive Interface (TWAI) | TAWI_CLK         | Y            | Y        |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            |               |
| GP-SPI2/GP-SPI3                      | GPSPi_HS_CLK     |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           | Y         |         |          |            |               |
|                                      | GPSPi_MST_CLK    |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           | Y         |         |          |            |               |

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Table 9.2-5 – cont'd from previous page

| Peripheral   | Clock   | Clock Source |          |          |               |              |              |              |              |              |              |               |               |               | Derived Clock |           |           |         |          |            | Clock from IO   |
|--|---|--------------|----------|----------|---------------|--------------|--------------|--------------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|-----------|-----------|---------|----------|------------|---|
|  |   | RC_FAST_CLK  | XTAL_CLK | APLL_CLK | SDIO_PLLO_CLK | PLL_F12M_CLK | PLL_F20M_CLK | PLL_F25M_CLK | PLL_F48M_CLK | PLL_F50M_CLK | PLL_F80M_CLK | PLL_F120M_CLK | PLL_F160M_CLK | PLL_F240M_CLK | FLASH_CLK     | PSRAM_CLK | GPSPI_CLK | ADC_CLK | UART_CLK | CRYPTO_CLK |   |
| Ethernet Media Access Controller (EMAC)  | EMAC_RMII_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_EMAC_TXRX_CLK<br>PAD_EMAC_RX_CLK<br>PAD_EMAC_TX_CLK |
|  | EMAC_RX_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_EMAC_TXRX_CLK<br>PAD_EMAC_RX_CLK                    |
|  | EMAC_TX_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_EMAC_TXRX_CLK<br>PAD_EMAC_TX_CLK                    |
|  | EMAC_PTP_REF_CLK  |              | Y        |          |               |              |              |              |              | Y            |              |               |               |               |               |           |           |         |          |            |   |
| CAM (CAM OUT)  | CAM_CLK   |              | Y        | Y        |               |              |              |              |              |              |              |               | Y             |               |               |           |           |         |          |            |   |
| IO MUX   | IOMUX_CLK   |              | Y        |          |               |              |              |              |              |              | Y            |               |               |               |               |           |           |         |          |            |   |
| LCD  | LCD_CLK   |              | Y        | Y        |               |              |              |              |              |              |              |               | Y             |               |               |           |           |         |          |            |   |
| LED PWM Controller (LEDC)  | LEDC_CLK  | Y            | Y        |          |               |              |              |              |              | Y            |              |               |               |               |               |           |           |         |          |            |   |
| ADC Controller (ADC)   | HPADC_CLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           | Y       |          |            |   |
|  | HPADC1_SARCLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           | Y       |          |            |   |
|  | HPADC2_SARCLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           | Y       |          |            |   |
| AES Accelerator (AES)<br>SHA Accelerator (SHA)<br>RSA Accelerator (RSA)<br>ECC Accelerator (ECC)<br>Digital Signature Algorithm (DSA)<br>HMAC Accelerator (HMAC)<br>Elliptic Curve Digital Signature Algorithm (ECDSA) | AES_CLK<br>SHA_CLK<br>RSA_CLK<br>ECC_CLK<br>DSA_CLK<br>HMAC_CLK<br>ECDSA_CLK<br>SEC_CLK |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          | Y          |   |
| RMT  | RMT_CLK   | Y            | Y        |          |               |              |              |              |              | Y            |              |               |               |               |               |           |           |         |          |            |   |
| System Timer   | SYSTEMER_CLK  | Y            | Y        |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            |   |
| UART Controller (UART)   | UART_FCLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         | Y        |            |   |
|  | UART_SCLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         | Y        |            |   |
|  | UART_SLP_CLK  |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            | PAD_UART_SLP_CLK  |
| Parallel IO Controller (PARLIO)  | PARLIO_RX_CLK   | Y            | Y        |          |               |              |              |              |              |              |              |               | Y             |               |               |           |           |         |          |            | PAD_PARLIO_RX_CLK                                       |
|  | PARLIO_TX_CLK   | Y            | Y        |          |               |              |              |              |              |              |              |               | Y             |               |               |           |           |         |          |            | PAD_PARLIO_TX_CLK                                       |
| I3C Controller [to be added later]   | I3C_MST_CLK   |              | Y        |          |               |              |              |              |              |              |              | Y             | Y             |               |               |           |           |         |          |            |   |
| Image Signal Processor (ISP)   | ISP_CLK   |              | Y        |          |               |              |              |              |              |              |              |               | Y             | Y             |               |           |           |         |          |            |   |
| MIPI DSI [to be added later]   | DSI_DPHY_CFG_CLK  | Y            |          |          |               |              | Y            | Y            |              |              |              |               |               |               |               |           |           |         |          |            |   |
|  | DSI_DPHY_PLL_REFCLK   |              |          |          |               |              |              |              |              |              |              |               |               |               |               |           |           |         |          |            |   |
|  | DSI_DPICLK  |              | Y        |          |               |              |              |              |              |              |              |               | Y             | Y             |               |           |           |         |          |            |   |
| MIPI CSI   | CSI_DPHY_CFG_CLK  | Y            |          |          |               |              | Y            | Y            |              |              |              |               |               |               |               |           |           |         |          |            |   |
| H264 Encoder [to be added later]   | H264_CLK  |              | Y        |          |               |              |              |              |              |              |              |               |               | Y             |               |           |           |         |          |            |   |
| USB Serial/JTAG Controller (USB_SERIAL_JTAG)   | USB_SERIAL_JTAG_CLK   |              |          |          |               |              |              |              | Y            |              |              |               |               |               |               |           |           |         |          |            |   |
| USB 2.0 Full-Speed OTG   | USB_OTG11_CLK   |              |          |          |               |              |              |              | Y            |              |              |               |               |               |               |           |           |         |          |            |   |
| USB 2.0 High-Speed OTG   | USB_HS_PHY_REFCLK   |              |          |          |               | Y            |              | Y            |              |              |              |               |               |               |               |           |           |         |          |            | PAD_USB_HSPHY_REFCLK                                    |
| SD/MMC Host Controller (SDHOST)  | SDIO_DRV_CLK (low-speed)<br>SDIO_SLF_CLK (low-speed)<br>SDIO_SAM_CLK (low-speed)        |              |          |          | Y             |              |              |              |              |              |              |               | Y             |               |               |           |           |         |          |            |   |

Table 9.2-6. Derived LP Clock Sources

| Derived clock | Source clock           |                       |                        |                       |                    |                     |  | Derived clock |             |                 |                 |             | Clock from IO |
|---------------|------------------------|-----------------------|------------------------|-----------------------|--------------------|---------------------|--|---------------|-------------|-----------------|-----------------|-------------|---------------|
|               | RC_SLOW_CLK<br>150 kHz | XTAL32K_CLK<br>32 kHz | OSC_SLOW_CLK<br>32 kHz | RC_FAST_CLK<br>20 MHz | XTAL_CLK<br>40 MHz | PLL_LP_CLK<br>8 MHz |  | LP_SLOW_CLK   | LP_FAST_CLK | LP_DYN_SLOW_CLK | LP_DYN_FAST_CLK | XTAL_D2_CLK |               |
| LP_FAST_CLK   |                        |                       |                        | Y                     | Y                  | Y                   |  |               |             |                 |                 |             |               |

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Table 9.2-6 -- Continued from the previous page...

| Derived clock   | Source clock           |                       |                        |                       |                    |                     | Derived clock |             |                 |                 |             | Clock from IO |
|-----------------|------------------------|-----------------------|------------------------|-----------------------|--------------------|---------------------|---------------|-------------|-----------------|-----------------|-------------|---------------|
|                 | RC_SLOW_CLK<br>150 kHz | XTAL32K_CLK<br>32 kHz | OSC_SLOW_CLK<br>32 kHz | RC_FAST_CLK<br>20 MHz | XTAL_CLK<br>40 MHz | PLL_LP_CLK<br>8 MHz | LP_SLOW_CLK   | LP_FAST_CLK | LP_DYN_SLOW_CLK | LP_DYN_FAST_CLK | XTAL_D2_CLK |               |
| LP_SLOW_CLK     | Y                      | Y                     | Y                      |                       |                    |                     |               |             |                 |                 |             |               |
| LP_DYN_FAST_CLK |                        |                       |                        |                       |                    |                     | Y             | Y           |                 |                 |             |               |
| LP_DYN_SLOW_CLK |                        |                       |                        |                       |                    |                     | Y             | Y           |                 |                 |             |               |
| LP_PERI_CLK     |                        |                       |                        |                       |                    |                     |               |             |                 | Y               |             |               |
| XTAL_D2_CLK     |                        |                       |                        |                       | Y                  |                     |               |             |                 |                 |             |               |

Table 9.2-7. LP Peripheral Clocks

| Derived clock               | Source clock           |                       |                        |                       |                    |                     | Derived clock |             |                 |                 |             |             | Clock from IO      |
|-----------------------------|------------------------|-----------------------|------------------------|-----------------------|--------------------|---------------------|---------------|-------------|-----------------|-----------------|-------------|-------------|--------------------|
|                             | RC_SLOW_CLK<br>150 kHz | XTAL32K_CLK<br>32 kHz | OSC_SLOW_CLK<br>32 kHz | RC_FAST_CLK<br>20 MHz | XTAL_CLK<br>40 MHz | PLL_LP_CLK<br>8 MHz | LP_SLOW_CLK   | LP_FAST_CLK | LP_DYN_SLOW_CLK | LP_DYN_FAST_CLK | LP_PERI_CLK | XTAL_D2_CLK |                    |
| eFuse Controller            |                        |                       |                        |                       |                    |                     |               |             |                 |                 |             | Y           |                    |
| RTC Watchdog Timer (RWDT)   | Y                      |                       |                        |                       |                    |                     |               |             | Y               | Y               |             |             |                    |
| RTC Timer                   |                        |                       |                        |                       |                    |                     |               |             | Y               | Y               |             |             |                    |
| Brown-out Detector          |                        |                       |                        |                       |                    |                     |               |             |                 | Y               |             |             |                    |
| Power Management Unit (PMU) | Y                      |                       |                        |                       |                    |                     |               | Y           | Y               | Y               |             |             |                    |
| LP UART                     |                        |                       |                        |                       |                    | Y                   |               |             |                 | Y               |             | Y           | PAD_LP_UART_SLP_CK |
| LP SPI                      |                        |                       |                        |                       |                    |                     |               |             |                 |                 |             |             | PAD_LP_SPI_CK      |
| LP I2C                      |                        |                       |                        |                       |                    | Y                   |               |             |                 | Y               |             | Y           |                    |
| Analog I2C Controller       |                        |                       |                        |                       |                    |                     |               | Y           |                 |                 |             |             |                    |
| LP I2S Controller           |                        |                       |                        |                       |                    | Y                   |               |             |                 | Y               |             | Y           |                    |
| LP ADC Controller           |                        |                       |                        |                       |                    |                     |               |             |                 |                 | Y           |             |                    |

**Note:**

To protect the encryption and decryption peripherals from DPA (Differential Power Analysis) attacks, a random divider strategy is implemented for its function clock. Four security levels are available, depending on the range of the random divider. Users can select the security level by configuring [HP\\_SYS\\_CLKRST\\_SEC\\_DPA\\_CFG\\_SEL](#).

If [HP\\_SYS\\_CLKRST\\_SEC\\_DPA\\_CFG\\_SEL](#) is set to 1, the security level is determined by the configuration of [HP\\_SYS\\_CLKRST\\_SEC\\_DPA\\_LEVEL](#). Otherwise, the security level is determined by the value of [EFUSE\\_SEC\\_DPA\\_LEVEL](#).

## 9.3 Programming Procedures

### 9.3.1 HP System Clock Configuration

- Configure the clock divisor for CPU\_CLK: [HP\\_SYS\\_CLKRST\\_CPU\\_CLK\\_DIV\\_NUM](#) for the integral part, [HP\\_SYS\\_CLKRST\\_CPU\\_CLK\\_DIV\\_NUMERATOR](#) for the numerator of the fractional part, and [HP\\_SYS\\_CLKRST\\_CPU\\_CLK\\_DIV\\_DENOMINATOR](#) for the denominator of the fractional part. Write 1 to [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) to apply the frequency divisor configurations for CPU\_CLK.
- Configure the clock divisor for MEM\_CLK: [HP\\_SYS\\_CLKRST\\_MEM\\_CLK\\_DIV\\_NUM](#) for the integral part, [HP\\_SYS\\_CLKRST\\_MEM\\_CLK\\_DIV\\_NUMERATOR](#) for the numerator of the fractional part, and [HP\\_SYS\\_CLKRST\\_MEM\\_CLK\\_DIV\\_DENOMINATOR](#) for the denominator of the fractional part. Write 1 to [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) to apply the frequency divisor configurations for MEM\_CLK.
- Configure the clock divisor for SYS\_CLK: [HP\\_SYS\\_CLKRST\\_SYS\\_CLK\\_DIV\\_NUM](#) for the integral part, [HP\\_SYS\\_CLKRST\\_SYS\\_CLK\\_DIV\\_NUMERATOR](#) for the numerator of the fractional part, and [HP\\_SYS\\_CLKRST\\_SYS\\_CLK\\_DIV\\_DENOMINATOR](#) for the denominator of the fractional part. Write 1 to [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) to apply the frequency divisor configurations for SYS\_CLK.
- Configure the clock divisor for APB\_CLK: [HP\\_SYS\\_CLKRST\\_APB\\_CLK\\_DIV\\_NUM](#) for the integral part, [HP\\_SYS\\_CLKRST\\_APB\\_CLK\\_DIV\\_NUMERATOR](#) for the numerator of the fractional part, and [HP\\_SYS\\_CLKRST\\_APB\\_CLK\\_DIV\\_DENOMINATOR](#) for the denominator of the fractional part. Write 1 to [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) to apply the frequency divisor configurations for APB\_CLK.
- Configure the clock source for ROOT\_CLK via [LP\\_CLKRST\\_HP\\_ROOT\\_CLK\\_SRC\\_SEL](#).

**Notice:**

1. It is recommended to first configure the frequency divisors for the SoC clocks and apply the configurations, and then configure the clock source for ROOT\_CLK.
2. Before changing the clock source for ROOT\_CLK, software needs to ensure that the configured clock divisors do not result in clock frequencies exceeding the allowed maximum frequencies.
3. Writing 1 to [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_DIV\\_UPDATE](#) will apply the frequency divisor configurations for CPU\_CLK, MEM\_CLK, SYS\_CLK, and APB\_CLK at one go, but it is not recommended to do so. It would be better to apply the configuration for each clock individually.
4. When switching from a high divisor to a low divisor, the recommended configuration order is APB\_CLK

→ SYS\_CLK → MEM\_CLK → CPU\_CLK. When switching from a low divisor to a high divisor, the recommended configuration order is CPU\_CLK → MEM\_CLK → SYS\_CLK → APB\_CLK. This helps to prevent high-frequency clock glitches.

### 9.3.2 LP System Clock Configuration

- Configure the clock source of LP\_SLOW\_CLK via [LP\\_CLKRST\\_SLOW\\_CLK\\_SEL](#)
- Configure the clock source of LP\_FAST\_CLK via [LP\\_CLKRST\\_FAST\\_CLK\\_SEL](#)
- Configure the clock divisor of LP\_PERI\_CLK via [LP\\_CLKRST\\_LP\\_PERI\\_DIV\\_NUM](#)

### 9.3.3 Peripheral Clock Reset and Configuration

**Notice:**

ESP32-P4 features low power consumption. This is why some peripheral clocks are gated (disabled) by default. Before using any of these peripherals, it is mandatory to enable the clock for the given peripheral by setting the corresponding CLK\_EN bit to 1, and release the peripheral from the reset state to make it operational by setting the RST\_EN bit to 0.

The clocks of most peripherals can be classified into two types:

- Bus clock: used to configure peripheral registers.
- Function clock: such as UART's reference clock, used by peripherals to operate.

The function clock of most peripherals can be selected from multiple clock sources. In the description of the gating registers, it will be stated whether a register is a bus clock (SYS\_CLK, APB\_CLK) gating register or a function clock gating register.

Bus clock enable/disable registers, function clock enable/disable registers, clock source selection registers, and clock frequency division registers are grouped into the HP\_SYS\_CLKRST, LP\_CLKRST, and LPPERI modules. Except for EMA, SDMMAC, USB Serial/JTAG, Full-Speed USB 2.0 OTG, and High-Speed USB 2.0 OTG, whose reset configuration registers are in the LP\_CLKRST module, all the other HP clock and reset registers are in the HP\_SYS\_CLKRST module. For more information, see Section [9.4 Register Summary](#).

When changing the clock configuration, it is recommended to turn off the corresponding clock gate first, update the clock divider configurations, clock sources, and other configurations, and then turn it on again.

When a peripheral is not working, users can turn off its function clock by configuring related registers. Turning off the peripheral's function clock does not affect the rest of the system.

Take I2C clock configuration as an example.

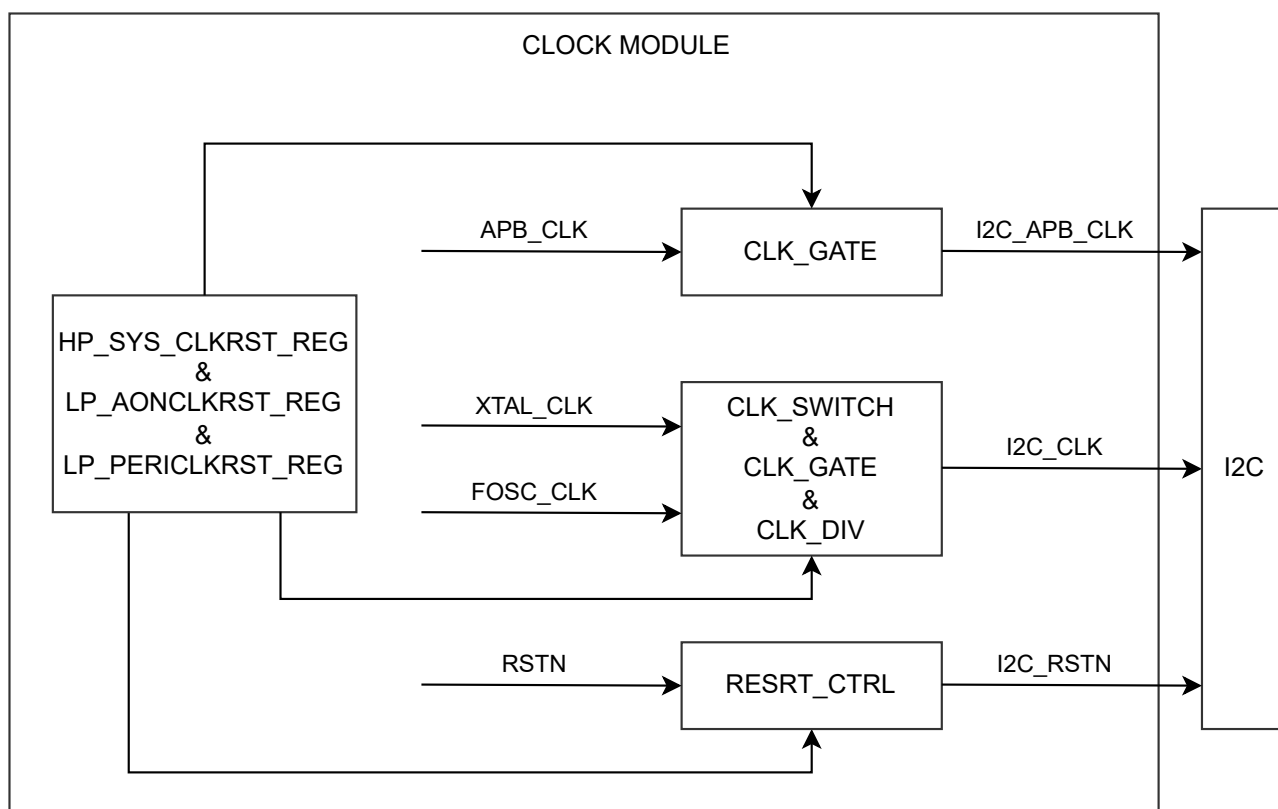


Figure 9.3-1. Clock Configuration Example

Figure 9.3-1 shows the clock structure of I2C. The clock structure of other peripherals is similar to this one. CLK\_SWITCH is used to select a clock output and CLK\_GATE to turn on/off the clock.

In scenarios that require low power consumption, when the peripheral is not in use, in addition to turning off the function clock, the bus clock of the peripheral can also be turned off to further lower power consumption.

Note that if you turn off the bus clock first, the functional clock may continue working. Therefore, when turning off clocks, it is recommended to turn off the functional clock first and then the bus clock; when turning on clocks, it is recommended to turn on the bus clock first and then the functional clock.

**Note:**

In this chapter, all divisor configuration registers are configured with the actual divisor minus 1.

## 9.4 Register Summary

### 9.4.1 Reset and Clock (HP\_SYS\_CLKRST) Register Summary

The addresses in this section are relative to HP\_SYS\_CLKRST base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <b>Clock gate enable register</b>                    |   |         |        |
| <a href="#">HP_SYS_CLKRST_CLK_ENO_REG</a>            | Register clock gate enable register                     | 0x0000  | R/W    |
| <a href="#">HP_SYS_CLKRST_CLK_FORCE_ON_CTRL0_REG</a> | System and peripheral clock gate configuration register | 0x00B4  | R/W    |
| <b>Root clock configuration register</b>             |   |         |        |
| <a href="#">HP_SYS_CLKRST_ROOT_CLK_CTRL0_REG</a>     | Root clock configuration register 0                     | 0x0004  | varies |
| <a href="#">HP_SYS_CLKRST_ROOT_CLK_CTRL1_REG</a>     | Root clock configuration register 1                     | 0x0008  | R/W    |
| <a href="#">HP_SYS_CLKRST_ROOT_CLK_CTRL2_REG</a>     | Root clock configuration register 2                     | 0x000C  | R/W    |
| <a href="#">HP_SYS_CLKRST_ROOT_CLK_CTRL3_REG</a>     | Root clock configuration register 3                     | 0x0010  | R/W    |
| <b>Bus clock configuration register</b>              |   |         |        |
| <a href="#">HP_SYS_CLKRST_SOC_CLK_CTRL0_REG</a>      | Bus clock configuration register 0                      | 0x0014  | R/W    |
| <a href="#">HP_SYS_CLKRST_SOC_CLK_CTRL1_REG</a>      | Bus clock configuration register 1                      | 0x0018  | R/W    |
| <a href="#">HP_SYS_CLKRST_SOC_CLK_CTRL2_REG</a>      | Bus clock configuration register 2                      | 0x001C  | R/W    |
| <a href="#">HP_SYS_CLKRST_SOC_CLK_CTRL3_REG</a>      | Bus clock configuration register 3                      | 0x0020  | R/W    |
| <b>Reference clock configuration register</b>        |   |         |        |
| <a href="#">HP_SYS_CLKRST_REF_CLK_CTRL0_REG</a>      | Reference clock configuration register 0                | 0x0024  | R/W    |
| <a href="#">HP_SYS_CLKRST_REF_CLK_CTRL1_REG</a>      | Reference clock configuration register 1                | 0x0028  | R/W    |
| <a href="#">HP_SYS_CLKRST_REF_CLK_CTRL2_REG</a>      | Reference clock configuration register 2                | 0x002C  | R/W    |
| <b>Peripheral clock configuration register</b>       |   |         |        |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL00_REG</a>    | Peripheral clock configuration register                 | 0x0030  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL01_REG</a>    | Peripheral clock configuration register                 | 0x0034  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL02_REG</a>    | Peripheral clock configuration register                 | 0x0038  | varies |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL03_REG</a>    | Peripheral clock configuration register                 | 0x003C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL10_REG</a>    | Peripheral clock configuration register                 | 0x0040  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL11_REG</a>    | Peripheral clock configuration register                 | 0x0044  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL12_REG</a>    | Peripheral clock configuration register                 | 0x0048  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL13_REG</a>    | Peripheral clock configuration register                 | 0x004C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL14_REG</a>    | Peripheral clock configuration register                 | 0x0050  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL15_REG</a>    | Peripheral clock configuration register                 | 0x0054  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL16_REG</a>    | Peripheral clock configuration register                 | 0x0058  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL17_REG</a>    | Peripheral clock configuration register                 | 0x005C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL18_REG</a>    | Peripheral clock configuration register                 | 0x0060  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL19_REG</a>    | Peripheral clock configuration register                 | 0x0064  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL110_REG</a>   | Peripheral clock configuration register                 | 0x0068  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL111_REG</a>   | Peripheral clock configuration register                 | 0x006C  | R/W    |

| Name   | Description                                    | Address | Access |
|--|--|---------|--------|
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL112_REG</a>         | Peripheral clock configuration register        | 0x0070  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL113_REG</a>         | Peripheral clock configuration register        | 0x0074  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL114_REG</a>         | Peripheral clock configuration register        | 0x0078  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL115_REG</a>         | Peripheral clock configuration register        | 0x007C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL116_REG</a>         | Peripheral clock configuration register        | 0x0080  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL117_REG</a>         | Peripheral clock configuration register        | 0x0084  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL118_REG</a>         | Peripheral clock configuration register        | 0x0088  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL119_REG</a>         | Peripheral clock configuration register        | 0x008C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL120_REG</a>         | Peripheral clock configuration register        | 0x0090  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL20_REG</a>          | Peripheral clock configuration register        | 0x0094  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL21_REG</a>          | Peripheral clock configuration register        | 0x0098  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL22_REG</a>          | Peripheral clock configuration register        | 0x009C  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL23_REG</a>          | Peripheral clock configuration register        | 0x00A0  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL24_REG</a>          | Peripheral clock configuration register        | 0x00A4  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL25_REG</a>          | Peripheral clock configuration register        | 0x00A8  | R/W    |
| <a href="#">HP_SYS_CLKRST_PERI_CLK_CTRL26_REG</a>          | Peripheral clock configuration register        | 0x00AC  | R/W    |
| <b>DPA clock configuration register</b>                    |  |         |        |
| <a href="#">HP_SYS_CLKRST_DPA_CTRL0_REG</a>                | DPA clock configuration register               | 0x00B8  | R/W    |
| <b>Analog PLL calibration configuration register</b>       |  |         |        |
| <a href="#">HP_SYS_CLKRST_ANA_PLL_CTRL0_REG</a>            | Analog PLL calibration configuration register  | 0x00BC  | varies |
| <b>Peripheral reset register</b>                           |  |         |        |
| <a href="#">HP_SYS_CLKRST_HP_RST_EN0_REG</a>               | Peripheral reset register 0                    | 0x00C0  | R/W    |
| <a href="#">HP_SYS_CLKRST_HP_RST_EN1_REG</a>               | Peripheral reset register 1                    | 0x00C4  | R/W    |
| <a href="#">HP_SYS_CLKRST_HP_RST_EN2_REG</a>               | Peripheral reset register 2                    | 0x00C8  | R/W    |
| <a href="#">HP_SYS_CLKRST_HP_FORCE_NORST0_REG</a>          | Peripheral reset disable register register 0   | 0x00CC  | R/W    |
| <a href="#">HP_SYS_CLKRST_HP_FORCE_NORST1_REG</a>          | Peripheral reset disable register register 1   | 0x00D0  | R/W    |
| <b>HP CPU WDT reset configuration register</b>             |  |         |        |
| <a href="#">HP_SYS_CLKRST_HPWDT_CORE0_RST_CTRL0_REG</a>    | HP CPU0 WDT reset configuration register       | 0x00D4  | R/W    |
| <a href="#">HP_SYS_CLKRST_HPWDT_CORE1_RST_CTRL0_REG</a>    | HP CPU1 WDT reset configuration register       | 0x00D8  | R/W    |
| <a href="#">HP_SYS_CLKRST_HPCORE_WDT_RESET_SOURCE0_REG</a> | HP CPU WDT reset source configuration register | 0x00EC  | R/W    |
| <b>CPU clock status register</b>                           |  |         |        |
| <a href="#">HP_SYS_CLKRST_CPU_SRC_FREQ0_REG</a>            | CPU source clock frequency register            | 0x00DC  | RO     |
| <a href="#">HP_SYS_CLKRST_CPU_CLK_STATUS0_REG</a>          | CPU clock status register                      | 0x00E0  | RO     |

### 9.4.2 LP Always on Clock and Reset (LP\_CLKRST) Register Summary

The addresses in this section are relative to LP\_CLKRST base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Configuration registers</b>                       |  |         |        |
| <a href="#">LP_CLKRST_LP_CLK_CONF_REG</a>            | LP root clock configuration register                 | 0x0000  | R/W    |
| <a href="#">LP_CLKRST_LP_CLK_EN_REG</a>              | LP always on peripheral clock configuration register | 0x0008  | R/W    |
| <a href="#">LP_CLKRST_LP_RST_EN_REG</a>              | LP always on peripheral reset configuration register | 0x000C  | R/W    |
| <a href="#">LP_CLKRST_RESET_CAUSE_REG</a>            | HP CPU and LP CPU reset cause register               | 0x0010  | varies |
| <a href="#">LP_CLKRST_HPCPU_RESET_CTRL0_REG</a>      | HP CPU reset configuration register 0                | 0x0014  | varies |
| <a href="#">LP_CLKRST_HPCPU_RESET_CTRL1_REG</a>      | HP CPU reset configuration register 1                | 0x0018  | R/W    |
| <a href="#">LP_CLKRST_FOSC_CNTL_REG</a>              | RC_FAST_CLK frequency configuration register         | 0x001C  | R/W    |
| <a href="#">LP_CLKRST_XTAL32K_REG</a>                | XTAL32K_CLK configuration register                   | 0x0030  | R/W    |
| <a href="#">LP_CLKRST_HP_CLK_CTRL_REG</a>            | HP clock control register                            | 0x0040  | R/W    |
| <a href="#">LP_CLKRST_HP_USB_CLKRST_CTRL0_REG</a>    | USB clock and reset control register 0               | 0x0044  | R/W    |
| <a href="#">LP_CLKRST_HP_USB_CLKRST_CTRL1_REG</a>    | USB clock and reset control register 1               | 0x0048  | R/W    |
| <a href="#">LP_CLKRST_HP_SDMMC_EMAC_RST_CTRL_REG</a> | SDMMC and EMAC reset control register                | 0x004C  | R/W    |
| <b>Version register</b>                              |  |         |        |
| <a href="#">LP_CLKRST_DATE_REG</a>                   | Version control register                             | 0x03FC  | R/W    |

### 9.4.3 LP Peripheral Clock and Reset (LPPERI) Register Summary

The addresses in this section are relative to LPPERI base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Configuration registers</b>                  |   |         |        |
| <a href="#">LPPERI_CLK_EN_REG</a>               | LP peripheral bus clock configuration register      | 0x0000  | R/W    |
| <a href="#">LPPERI_CORE_CLK_SEL_REG</a>         | LP peripheral function clock configuration register | 0x0004  | R/W    |
| <a href="#">LPPERI_RESET_EN_REG</a>             | LP peripheral reset configuration register          | 0x0008  | varies |
| <a href="#">LPPERI_CPU_REG</a>                  | LP CPU access configuration register                | 0x000C  | R/W    |
| <a href="#">LPPERI_MEM_CTRL_REG</a>             | LP UART miscellaneous control register              | 0x0028  | varies |
| <a href="#">LPPERI_ADC_CTRL_REG</a>             | LP ADC clock configuration register                 | 0x002C  | R/W    |
| <a href="#">LPPERI_LP_I2S_RXCLK_DIV_NUM_REG</a> | LP I2S RX clock configuration register              | 0x0030  | R/W    |
| <a href="#">LPPERI_LP_I2S_RXCLK_DIV_XYZ_REG</a> | LP I2S RX clock configuration register              | 0x0034  | R/W    |
| <b>Version register</b>                         |   |         |        |
| <a href="#">LPPERI_DATE_REG</a>                 | Version control register                            | 0x03FC  | R/W    |

## 9.5 Registers

### 9.5.1 Reset and Clock (HP\_SYS\_CLKRST) Registers

The addresses in this section are relative to HP\_SYS\_CLKRST base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 9.1. HP\_SYS\_CLKRST\_CLK\_ENO\_REG (0x0000)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Reset |

**HP\_SYS\_CLKRST\_CLK\_EN** Configures resister clock gating.  
0: Support clock only when application writes registers  
1: Force on clock gating for registers  
(R/W)



### Register 9.2. HP\_SYS\_CLKRST\_ROOT\_CLK\_CTRL0\_REG (0x0004)

|            |    |    |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |   |   |   |   |  |  |  |  |  |  |  |  |  |  |                                |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--------------------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    | HP_SYS_CLKRST_CPU_CLK_DIV_DENOMINATOR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_CPU_CLK_DIV_NUMERATOR |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_CPU_CLK_DIV_NUM |  |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SOC_CLK_DIV_UPDATE |  |  |  |   |   |   |   |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_CPUICM_DELAY_NUM |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 29 | 28 |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 21                                  | 20 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  | 13 | 12 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  | 5 | 4 | 3 | 0 |  |  |  |  |  |  |  |  |  |  |                                |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                   |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                             |  |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                |  |  |  |   |   |   |   |  |  |  |  |  |  |  |  |  |  | 0                              | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**HP\_SYS\_CLKRST\_CPUICM\_DELAY\_NUM** Configures the time required from entering WFI mode to the actual shutdown of the CPU clock.

Measurement unit: clock cycles. (R/W)

**HP\_SYS\_CLKRST\_SOC\_CLK\_DIV\_UPDATE** Configures whether to update the divisors for CPU\_CLK, MEM\_CLK, SYS\_CLK, APB\_CLK.

0: Not update

1: Update

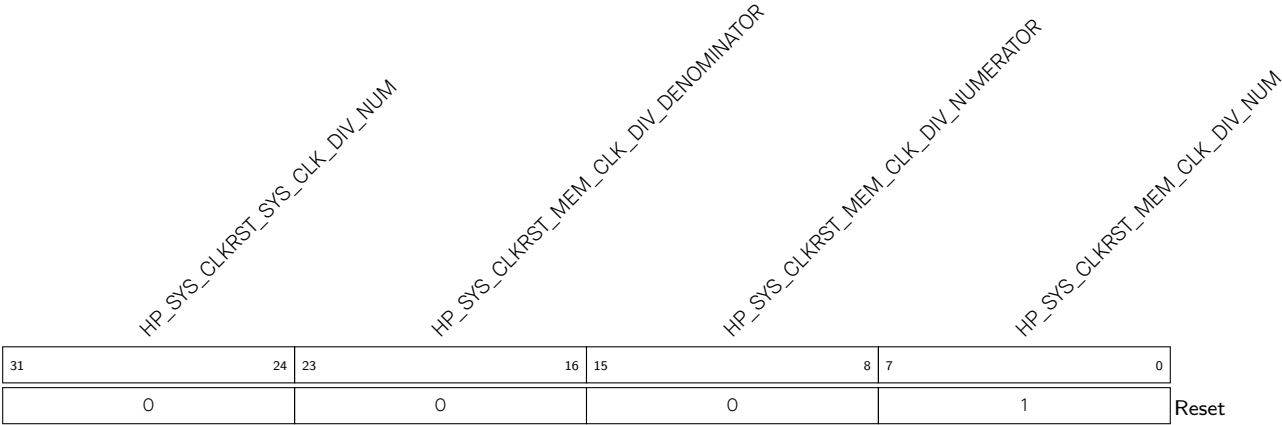
(WT)

**HP\_SYS\_CLKRST\_CPU\_CLK\_DIV\_NUM** Configures the integer part of the CPU\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_CPU\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for CPU\_CLK. (R/W)

**HP\_SYS\_CLKRST\_CPU\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for CPU\_CLK. (R/W)

Register 9.3. HP\_SYS\_CLKRST\_ROOT\_CLK\_CTRL1\_REG (0x0008)



- HP\_SYS\_CLKRST\_MEM\_CLK\_DIV\_NUM**    Configures the integer part of the MEM\_CLK clock divisor.  
(R/W)
- HP\_SYS\_CLKRST\_MEM\_CLK\_DIV\_NUMERATOR**    Configures the numerator of the divisor’s fractional part for MEM\_CLK. (R/W)
- HP\_SYS\_CLKRST\_MEM\_CLK\_DIV\_DENOMINATOR**    Configures the denominator of the divisor’s fractional part for MEM\_CLK . (R/W)
- HP\_SYS\_CLKRST\_SYS\_CLK\_DIV\_NUM**    Configures the integer part of the SYS\_CLK clock divisor.  
(R/W)

#### Register 9.4. HP\_SYS\_CLKRST\_ROOT\_CLK\_CTRL2\_REG (0x000C)

| 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 |       |
|----|----|----|----|----|---|---|---|-------|
|    |    |    |    |    |   |   |   | Reset |
|    |    |    |    |    |   |   |   |       |

**HP\_SYS\_CLKRST\_SYS\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for SYS\_CLK. (R/W)

**HP\_SYS\_CLKRST\_SYS\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for SYS\_CLK. (R/W)

**HP\_SYS\_CLKRST\_APB\_CLK\_DIV\_NUM** Configures the integer part of the APB\_CLK fclock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_APB\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for APB\_CLK. (R/W)

### Register 9.5. HP\_SYS\_CLKRST\_ROOT\_CLK\_CTRL3\_REG (0x0010)

|    |   |   |  |   |                                       |   |
|----|---|---|--|---|---------------------------------------|---|
| 31 |   | 8 |  | 7 |                                       | 0 |
|    | (reserved)                                      |   |  |   | HP_SYS_CLKRST_APB_CLK_DIV_DENOMINATOR |   |
|    | 0 |   |  |   | 0                                     |   |

**Reset**

**HP\_SYS\_CLKRST\_APB\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for APB\_CLK. (R/W)

Register 9.6. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL0\_REG (0x0014)

|                                |                                |                              |                                |                                   |                                |                                  |                                |                               |                              |                                   |                                |                                  |                                     |                                     |                                    |                                  |                               |                              |                                |                                  |                                     |                                     |                                    |                                 |                              |                                |                                |                               |                                 |                                 |                                 |
|--------------------------------|--------------------------------|------------------------------|--------------------------------|-----------------------------------|--------------------------------|----------------------------------|--------------------------------|-------------------------------|------------------------------|-----------------------------------|--------------------------------|----------------------------------|-------------------------------------|-------------------------------------|------------------------------------|----------------------------------|-------------------------------|------------------------------|--------------------------------|----------------------------------|-------------------------------------|-------------------------------------|------------------------------------|---------------------------------|------------------------------|--------------------------------|--------------------------------|-------------------------------|---------------------------------|---------------------------------|---------------------------------|
| HP_SYS_CLKRST_PSRAM_SYS_CLK_EN | HP_SYS_CLKRST_FLASH_SYS_CLK_EN | HP_SYS_CLKRST_ICM_SYS_CLK_EN | HP_SYS_CLKRST_SPMON_SYS_CLK_EN | HP_SYS_CLKRST_L2MEMMON_SYS_CLK_EN | HP_SYS_CLKRST_L2MEM_SYS_CLK_EN | HP_SYS_CLKRST_L2CACHE_SYS_CLK_EN | HP_SYS_CLKRST_TRACE_SYS_CLK_EN | HP_SYS_CLKRST_MISC_SYS_CLK_EN | HP_SYS_CLKRST_ICM_MEM_CLK_EN | HP_SYS_CLKRST_L2MEMMON_MEM_CLK_EN | HP_SYS_CLKRST_L2MEM_MEM_CLK_EN | HP_SYS_CLKRST_L2CACHE_MEM_CLK_EN | HP_SYS_CLKRST_L1CACHE_I1_MEM_CLK_EN | HP_SYS_CLKRST_L1CACHE_I0_MEM_CLK_EN | HP_SYS_CLKRST_L1CACHE_D_MEM_CLK_EN | HP_SYS_CLKRST_L1CACHE_MEM_CLK_EN | HP_SYS_CLKRST_GDMA_CPU_CLK_EN | HP_SYS_CLKRST_ICM_CPU_CLK_EN | HP_SYS_CLKRST_TRACE_CPU_CLK_EN | HP_SYS_CLKRST_L1CACHE_CPU_CLK_EN | HP_SYS_CLKRST_L1CACHE_I1_CPU_CLK_EN | HP_SYS_CLKRST_L1CACHE_I0_CPU_CLK_EN | HP_SYS_CLKRST_L1CACHE_D_CPU_CLK_EN | HP_SYS_CLKRST_BUSMON_CPU_CLK_EN | HP_SYS_CLKRST_SPM_CPU_CLK_EN | HP_SYS_CLKRST_CORE1_CPU_CLK_EN | HP_SYS_CLKRST_CORE0_CPU_CLK_EN | HP_SYS_CLKRST_MISC_CPU_CLK_EN | HP_SYS_CLKRST_CORE1_CLIC_CLK_EN | HP_SYS_CLKRST_CORE0_CLIC_CLK_EN | HP_SYS_CLKRST_CORE0_CLIC_CLK_EN |
| 31                             | 30                             | 29                           | 28                             | 27                                | 26                             | 25                               | 24                             | 23                            | 22                           | 21                                | 20                             | 19                               | 18                                  | 17                                  | 16                                 | 15                               | 14                            | 13                           | 12                             | 11                               | 10                                  | 9                                   | 8                                  | 7                               | 6                            | 5                              | 4                              | 3                             | 2                               | 1                               | 0                               |
| 1                              | 1                              | 1                            | 0                              | 0                                 | 1                              | 1                                | 0                              | 1                             | 1                            | 0                                 | 1                              | 1                                | 1                                   | 1                                   | 1                                  | 0                                | 0                             | 1                            | 0                              | 1                                | 1                                   | 1                                   | 1                                  | 0                               | 1                            | 0                              | 1                              | 1                             | 1                               | 1                               | 1                               |

Reset

**HP\_SYS\_CLKRST\_CORE0\_CLIC\_CLK\_EN** Configures whether to enable the bus clock of HP CPU0 CLIC.  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_CORE1\_CLIC\_CLK\_EN** Configures whether to enable the bus clock of HP CPU1 CLIC.  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_MISC\_CPU\_CLK\_EN** Configures whether to enable the bus clock of miscellaneous modules (CPU\_CLK clock domain).  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_CORE0\_CPU\_CLK\_EN** Configures whether to enable the bus clock of HP CPU0 (CPU\_CLK clock domain).  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_CORE1\_CPU\_CLK\_EN** Configures whether to enable the bus clock of HP CPU1 (CPU\_CLK clock domain).  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_SPM\_CPU\_CLK\_EN** Configures whether to enable the bus clock of SPM monitor (CPU\_CLK clock domain).  
 0: Disable  
 1: Enable  
 (R/W)

Continued on the next page...

**Register 9.6. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL0\_REG (0x0014)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_BUSMON\_CPU\_CLK\_EN** Configures whether to enable the bus clock of bus monitor (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_CPU\_CLK\_EN** Configures whether to enable the bus clock of L1 Cache (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_D\_CPU\_CLK\_EN** Configures whether to enable the bus clock of L1 D-Cache (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_IO\_CPU\_CLK\_EN** Configures whether to enable the bus clock of L1 I-Cache 0 (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_I1\_CPU\_CLK\_EN** Configures whether to enable the bus clock of L1 I-Cache 1 (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TRACE\_CPU\_CLK\_EN** Configures whether to enable the bus clock of RISC-V Trace Encoder (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ICM\_CPU\_CLK\_EN** Configures the bus clock of the bus module (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.6. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL0\_REG (0x0014)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_GDMA\_CPU\_CLK\_EN** Configures whether to enable the bus clock of VDMA (CPU\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L1 Cache (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_D\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L1 D-Cache (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_IO\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L1 I-Cache0 (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_I1\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L1 I-Cache1 (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L2CACHE\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L2 Cache (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.6. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL0\_REG (0x0014)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_L2MEM\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L2 memory (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L2MEMMON\_MEM\_CLK\_EN** Configures whether to enable the bus clock of L1 memory monitor (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ICM\_MEM\_CLK\_EN** Configures the bus clock of the bus module (MEM\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MISC\_SYS\_CLK\_EN** Configures whether to enable the bus clock of miscellaneous modules (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TRACE\_SYS\_CLK\_EN** Configures whether to enable the bus clock of RISC-V Trace Encoder (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L2CACHE\_SYS\_CLK\_EN** Configures whether to enable the bus clock of L2 Cache (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_L2MEM\_SYS\_CLK\_EN** Configures whether to enable the bus clock of L2 memory (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.6. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL0\_REG (0x0014)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_L2MEMMON\_SYS\_CLK\_EN** Configures whether to enable the bus clock of L2 memory monitor (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_SPMMON\_SYS\_CLK\_EN** Configures whether to enable the bus clock of L2 SPM monitor (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ICM\_SYS\_CLK\_EN** Configures the bus clock of the bus module (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_FLASH\_SYS\_CLK\_EN** Configures whether to enable the bus clock of flash (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PSRAM\_SYS\_CLK\_EN** Configures whether to enable the bus clock of PSRAM (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)



Register 9.7. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL1\_REG (0x0018)

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 |

Reset

**HP\_SYS\_CLKRST\_GPSPI2\_SYS\_CLK\_EN** Configures whether to enable the bus clock of GP-SPI2 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_GPSPI3\_SYS\_CLK\_EN** Configures whether to enable the bus clock of GP-SPI3 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_AHB\_PDMA\_SYS\_CLK\_EN** Configures whether to enable the bus clock of GDMA-AHB (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_AXI\_PDMA\_SYS\_CLK\_EN** Configures whether to enable the bus clock of GDMA-AXI (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_GDMA\_SYS\_CLK\_EN** Configures whether to enable the bus clock of VDMA (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.7. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL1\_REG (0x0018)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_DMA2D\_SYS\_CLK\_EN** Configures whether to enable the bus clock of 2DDMA (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_JPEG\_SYS\_CLK\_EN** Configures whether to enable the bus clock of JPEG (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PPA\_SYS\_CLK\_EN** Configures whether to enable the bus clock of PPA (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_CSI\_BRG\_SYS\_CLK\_EN** Configures whether to enable the bus clock of CSI Bridge and ISP (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_CSI\_HOST\_SYS\_CLK\_EN** Configures whether to enable the bus clock of CSI Host (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_DSI\_SYS\_CLK\_EN** Configures whether to enable the bus clock of DSI (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.7. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL1\_REG (0x0018)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_EMAC\_SYS\_CLK\_EN** Configures whether to enable the bus clock of EMAC (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_SDMMC\_SYS\_CLK\_EN** Configures whether to enable the bus clock of SDMMC (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_USB\_OTG11\_SYS\_CLK\_EN** Configures whether to enable the bus clock of Full-Speed USB 2.0 OTG (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_USB\_OTG20\_SYS\_CLK\_EN** Configures whether to enable the bus clock of High-Speed USB 2.0 OTG (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UHCI\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UHCI (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART0\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UART0 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART1\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UART1 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.7. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL1\_REG (0x0018)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_UART2\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UART2 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART3\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UART3 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART4\_SYS\_CLK\_EN** Configures whether to enable the bus clock of UART4 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PARLIO\_SYS\_CLK\_EN** Configures whether to enable the bus clock of PARLIO (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ETM\_SYS\_CLK\_EN** Configures whether to enable the bus clock of ETM (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W) 0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_CRYPTOSYS\_CLK\_EN** Configures whether to enable the bus clock of the crypto modules (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.7. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL1\_REG (0x0018)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_BITSRAMBLER\_SYS\_CLK\_EN** Configures whether to enable the bus clock of the Bit Scrambler (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_BITSRAMBLER\_RX\_SYS\_CLK\_EN** Configures whether to enable the bus clock of the Bit Scrambler RX (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_BITSRAMBLER\_TX\_SYS\_CLK\_EN** Configures whether to enable the bus clock of the Bit Scrambler TX (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_H264\_SYS\_CLK\_EN** Configures whether to enable the bus clock of H264 (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Register 9.8. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL2\_REG (0x001C)

|                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| HP_SYS_CLKRST_PARLO_APB_CLK_EN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_PONT_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_USB_DEVICE_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_MCPWM1_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_MCPWMO_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWA12_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWA11_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWAIO_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SYSTIMER_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TIMERGRP1_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TIMERGRP0_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_GSP13_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_GSP12_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I3C_SLV_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I3C_MST_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S2_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2SO_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2C1_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2CO_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART4_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART3_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART2_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART1_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UH01_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_ADC_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_INTRMTX_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_ICM_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SYSREG_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_HP_CLKRST_APB_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_RMT_SYS_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                              | 0  | 1  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | Reset                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**HP\_SYS\_CLKRST\_RMT\_SYS\_CLK\_EN** Configures whether to enable the bus clock of RMT (SYS\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_HP\_CLKRST\_APB\_CLK\_EN** Configures whether to enable the bus clock of the Reset and Clock module (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_SYSREG\_APB\_CLK\_EN** Configures whether to enable the bus clock of the HP System Registers (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ICM\_APB\_CLK\_EN** Configures the bus clock of the bus module (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_INTRMTX\_APB\_CLK\_EN** Configures whether to enable the bus clock of the Interrupt Matrix (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ADC\_APB\_CLK\_EN** Configures whether to enable the bus clock of the ADC (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

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**Register 9.8. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL2\_REG (0x001C)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_UHCI\_APB\_CLK\_EN** Configures whether to enable the bus clock of the UHCI (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART0\_APB\_CLK\_EN** Configures whether to enable the bus clock of UART0 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART1\_APB\_CLK\_EN** Configures whether to enable the bus clock of UART1 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART2\_APB\_CLK\_EN** Configures whether to enable the bus clock of UART2 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART3\_APB\_CLK\_EN** Configures whether to enable the bus clock of UART3 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_UART4\_APB\_CLK\_EN** Configures whether to enable the bus clock of UART4 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2CO\_APB\_CLK\_EN** Configures whether to enable the bus clock of I2CO (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

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**Register 9.8. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL2\_REG (0x001C)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_I2C1\_APB\_CLK\_EN** Configures whether to enable the bus clock of I2C1 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2S0\_APB\_CLK\_EN** Configures whether to enable the bus clock of I2S0 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2S1\_APB\_CLK\_EN** Configures whether to enable the bus clock of I2S1 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2S2\_APB\_CLK\_EN** Configures whether to enable the bus clock of I2S2 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I3C\_MST\_APB\_CLK\_EN** Configures whether to enable the bus clock of the I3C Master (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I3C\_SLV\_APB\_CLK\_EN** Configures whether to enable the bus clock of the I3C Slave (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_GPSPI2\_APB\_CLK\_EN** Configures whether to enable the bus clock of GP-SPI2 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

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**Register 9.8. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL2\_REG (0x001C)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_GPSPI3\_APB\_CLK\_EN** Configures whether to enable the bus clock of GP-SPI3 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_APB\_CLK\_EN** Configures whether to enable the bus clock of Timer Group 0 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_APB\_CLK\_EN** Configures whether to enable the bus clock of Timer Group 1 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_SYSTIMER\_APB\_CLK\_EN** Configures whether to enable the bus clock of the System Timer (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TWAIO\_APB\_CLK\_EN** Configures whether to enable the bus clock of TWAIO (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TWA11\_APB\_CLK\_EN** Configures whether to enable the bus clock of TWA11 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TWA12\_APB\_CLK\_EN** Configures whether to enable the bus clock of TWA12 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.8. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL2\_REG (0x001C)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_MCPWM0\_APB\_CLK\_EN** Configures whether to enable the bus clock of MCPWM0 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MCPWM1\_APB\_CLK\_EN** Configures whether to enable the bus clock of MCPWM1 (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_USB\_DEVICE\_APB\_CLK\_EN** Configures whether to enable the bus clock of the USB Serial/JTAG (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PCNT\_APB\_CLK\_EN** Configures whether to enable the bus clock of the PCNT (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PARLIO\_APB\_CLK\_EN** Configures whether to enable the bus clock of the PARLIO (APB\_CLK clock domain).

0: Disable

1: Enable

(R/W)

Register 9.9. HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL3\_REG (0x0020)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |       |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|-------|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_IOMUX_APB_CLK_EN  |   |   |       |  |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_ETM_APB_CLK_EN    |   |   |       |  |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_LCDCAM_APB_CLK_EN |   |   |       |  |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_LEDC_APB_CLK_EN   |   |   |       |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4 | 3 | 2 | 1                               | 0 |   |       |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0                               | 0 | 0 | Reset |  |  |

**HP\_SYS\_CLKRST\_LEDC\_APB\_CLK\_EN** Configures whether to enable the bus clock of LEDC (APB\_CLK clock domain).  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_LCDCAM\_APB\_CLK\_EN** Configures whether to enable the bus clock of the LCD\_CAM (APB\_CLK clock domain).  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_ETM\_APB\_CLK\_EN** Configures whether to enable the bus clock of ETM (APB\_CLK clock domain).  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_IOMUX\_APB\_CLK\_EN** Configures whether to enable the bus clock of IO MUX (APB\_CLK clock domain).  
0: Disable  
1: Enable  
(R/W)

Register 9.10. HP\_SYS\_CLKRST\_REF\_CLK\_CTRL0\_REG (0x0024)

|                                    |    |    |    |    |   |   |   |
|------------------------------------|----|----|----|----|---|---|---|
| HP_SYS_CLKRST_REF_160M_CLK_DIV_NUM |    |    |    |    |   |   |   |
| HP_SYS_CLKRST_REF_240M_CLK_DIV_NUM |    |    |    |    |   |   |   |
| HP_SYS_CLKRST_REF_25M_CLK_DIV_NUM  |    |    |    |    |   |   |   |
| HP_SYS_CLKRST_REF_50M_CLK_DIV_NUM  |    |    |    |    |   |   |   |
| 31                                 | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 2                                  |    | 1  |    | 19 |   | 9 |   |
| Reset                              |    |    |    |    |   |   |   |

- HP\_SYS\_CLKRST\_REF\_50M\_CLK\_DIV\_NUM    Configures the divisor of PLL\_F50M\_CLK. It is not recommended for users to change. (R/W)
- HP\_SYS\_CLKRST\_REF\_25M\_CLK\_DIV\_NUM    Configures the divisor of PLL\_F25M\_CLK. It is not recommended for users to change. (R/W)
- HP\_SYS\_CLKRST\_REF\_240M\_CLK\_DIV\_NUM    Configures the divisor of PLL\_F240M\_CLK. It is not recommended for users to change. (R/W)
- HP\_SYS\_CLKRST\_REF\_160M\_CLK\_DIV\_NUM    Configures the divisor of PLL\_F160M\_CLK. It is not recommended for users to change. (R/W)

Register 9.11. HP\_SYS\_CLKRST\_REF\_CLK\_CTRL1\_REG (0x0028)

|            |    |    |    |    |    |   |   |  |    |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |  |  |  |                               |  |  |  |  |  |  |  |  |  |   |  |   |   |  |  |            |  |  |  |  |  |  |  |  |       |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|----|----|----|----|---|---|--|----|----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|---|--|---|---|--|--|------------|--|--|--|--|--|--|--|--|-------|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |    |   |   |  |    |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |  |  |  | HP_SYS_CLKRST_REF_240M_CLK_EN |  |  |  |  |  |  |  |  |  |   |  |   |   |  |  | (reserved) |  |  |  |  |  |  |  |  |       |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_REF_25M_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_REF_50M_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_REF_20M_CLK_DIV_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_REF_80M_CLK_DIV_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_REF_120M_CLK_DIV_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30 | 29 | 28 | 27 | 26 |   |   |  | 24 | 23 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16 | 15 |  |  |  |                               |  |  |  |  |  |  |  |  |  |   |  | 8 | 7 |  |  |            |  |  |  |  |  |  |  |  |       |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 1  | 0  | 1  | 1  | 0  | 0 | 0 |  |    |    | 23 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5  |    |  |  |  |                               |  |  |  |  |  |  |  |  |  | 3 |  |   |   |  |  |            |  |  |  |  |  |  |  |  | Reset |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**HP\_SYS\_CLKRST\_REF\_120M\_CLK\_DIV\_NUM** Configures the divisor of PLL\_F120M\_CLK. (R/W)**HP\_SYS\_CLKRST\_REF\_80M\_CLK\_DIV\_NUM** Configures the divisor of PLL\_F80M\_CLK. (R/W)**HP\_SYS\_CLKRST\_REF\_20M\_CLK\_DIV\_NUM** Configures the divisor of PLL\_F20M\_CLK. (R/W)**HP\_SYS\_CLKRST\_REF\_50M\_CLK\_EN** Configures whether to enable PLL\_F50M\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_REF\_25M\_CLK\_EN** Configures whether to enable PLL\_F25M\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_REF\_240M\_CLK\_EN** Configures whether to enable PLL\_F240M\_CLK.

0: Disable

1: Enable

(R/W)

Register 9.12. HP\_SYS\_CLKRST\_REF\_CLK\_CTRL2\_REG (0x002C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |            |   |   |   |                              |   |   |   |            |   |   |   |                               |  |  |  |            |  |  |  |                               |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|------------|---|---|---|------------------------------|---|---|---|------------|---|---|---|-------------------------------|--|--|--|------------|--|--|--|-------------------------------|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_REF_20M_CLK_EN |   |   |   | (reserved) |   |   |   | HP_SYS_CLKRST_REF_80M_CLK_EN |   |   |   | (reserved) |   |   |   | HP_SYS_CLKRST_REF_120M_CLK_EN |  |  |  | (reserved) |  |  |  | HP_SYS_CLKRST_REF_160M_CLK_EN |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9                            | 8 | 7 | 5 | 4          | 3 | 2 | 1 | 0                            |   |   |   |            |   |   |   |                               |  |  |  |            |  |  |  |                               |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0          | 0 | 0 | 1 | 0                            | 0 | 0 | 1 | 0          | 1 | 0 | 1 | Reset                         |  |  |  |            |  |  |  |                               |  |  |  |  |

**HP\_SYS\_CLKRST\_REF\_160M\_CLK\_EN**   Configures whether to enable PLL\_F160M\_CLK.  
0: Disable  
1: Enable  
User modification is not recommended. (R/W)

**HP\_SYS\_CLKRST\_REF\_120M\_CLK\_EN**   Configures whether to enable PLL\_F120M\_CLK.  
0: Disable  
1: Enable  
User modification is not recommended. (R/W)

**HP\_SYS\_CLKRST\_REF\_80M\_CLK\_EN**   Configures whether to enable PLL\_F80M\_CLK.  
0: Disable  
1: Enable  
User modification is not recommended. (R/W)

**HP\_SYS\_CLKRST\_REF\_20M\_CLK\_EN**   Configures whether to enable PLL\_F20M\_CLK.  
0: Disable  
1: Enable  
User modification is not recommended. (R/W)

**Register 9.13. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL00\_REG (0x0030)**

|  |    |    |    |    |    |    |    |    |  |  |  |   |    |    |    |    |    |    |   |   |   |  |   |   |       |   |   |
|--|----|----|----|----|----|----|----|----|--|--|--|---|----|----|----|----|----|----|---|---|---|--|---|---|-------|---|---|
| <div>(reserved)</div> <div>HP_SYS_CLKRST_EMAC_RX_CLK_EN</div> <div>HP_SYS_CLKRST_EMAC_RX_CLK_SRC_SEL</div> <div>HP_SYS_CLKRST_EMAC_RMII_CLK_EN</div> <div>HP_SYS_CLKRST_EMAC_RMII_CLK_SRC_SEL</div> <div>HP_SYS_CLKRST_PAD_EMAC_REF_CLK_EN</div> <div>HP_SYS_CLKRST_PSRAM_CORE_CLK_DIV_NUM</div> <div>HP_SYS_CLKRST_PSRAM_CORE_CLK_EN</div> <div>HP_SYS_CLKRST_PSRAM_PLL_CLK_EN</div> <div>HP_SYS_CLKRST_PSRAM_CLK_SRC_SEL</div> <div>HP_SYS_CLKRST_FLASH_CORE_CLK_DIV_NUM</div> <div>HP_SYS_CLKRST_FLASH_CORE_CLK_EN</div> <div>HP_SYS_CLKRST_FLASH_PLL_CLK_EN</div> <div>HP_SYS_CLKRST_FLASH_CLK_SRC_SEL</div> |    |    |    |    |    |    |    |    |  |  |  |   |    |    |    |    |    |    |   |   |   |  |   |   |       |   |   |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 |  |  |  |   | 16 | 15 | 14 | 13 | 12 | 11 |   |   |   |  | 4 | 3 | 2     | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |  |  |  | 1 | 1  | 0  | 3  |    |    |    | 1 | 1 | 0 |  |   |   | Reset |   |   |

**HP\_SYS\_CLKRST\_FLASH\_CLK\_SRC\_SEL** Configures the clock source for FLASH\_CLK.

- 0: XTAL\_CLK
  - 1: SPLL\_CLK (480 MHz)
  - 2: CPLL\_CLK (360 MHz)
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_FLASH\_PLL\_CLK\_EN** Configures whether to enable FLASH\_PLL\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_FLASH\_CORE\_CLK\_EN** Configures whether to enable FLASH\_CORE\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_FLASH\_CORE\_CLK\_DIV\_NUM** Configures the clock divisor of FLASH\_CORE\_CLK. (R/W)

**HP\_SYS\_CLKRST\_PSRAM\_CLK\_SRC\_SEL** Configures the clock source for PSRAM\_CLK.

- 0: XTAL\_CLK
  - 1: MPLL\_CLK
  - 2: SPLL\_CLK (480 MHz)
  - 3: CPLL\_CLK (360 MHz)
- (R/W)

**HP\_SYS\_CLKRST\_PSRAM\_PLL\_CLK\_EN** Configures whether to enable PSRAM\_PLL\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_PSRAM\_CORE\_CLK\_EN** Configures whether to enable PSRAM\_CORE\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

Continued on the next page...

**Register 9.13. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL00\_REG (0x0030)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_PSRAM\_CORE\_CLK\_DIV\_NUM** Configures the clock divisor of PSRAM\_CORE\_CLK. (R/W)

**HP\_SYS\_CLKRST\_PAD\_EMAC\_REF\_CLK\_EN** Configures whether to enable PAD\_EMAC\_REF\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_RMII\_CLK\_SRC\_SEL** Configures the clock source for EMAC\_RMII\_CLK.  
0: PAD\_EMAC\_TXRX\_CLK  
1: PAD\_EMAC\_RX\_CLK  
2: PAD\_EMAC\_TX\_CLK  
3: Invalid  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_RMII\_CLK\_EN** Configures whether to enable EMAC\_RMII\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_RX\_CLK\_SRC\_SEL** Configures the clock source for EMAC\_RX\_CLK.  
0: PAD\_EMAC\_TXRX\_CLK  
1: PAD\_EMAC\_RX\_CLK  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_RX\_CLK\_EN** Configures whether to enable EMAC\_RX\_CLK.  
0: Disable  
1: Enable  
(R/W)



**Register 9.14. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL01\_REG (0x0034)**

|            |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |                                   |    |    |    |    |    |    |    |            |  |  |  |  |  |  |    |                            |  |  |  |  |  |  |   |                                   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|-----------------------------------|----|----|----|----|----|----|----|------------|--|--|--|--|--|--|----|----------------------------|--|--|--|--|--|--|---|-----------------------------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_EN |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_SRC_SEL |    |    |    |    |    |    |    | (reserved) |  |  |  |  |  |  |    | HP_SYS_CLKRST_SDIO_HS_MODE |  |  |  |  |  |  |   | HP_SYS_CLKRST_EMAC_PTP_REF_CLK_EN |   |   |  |  |  |  |  | HP_SYS_CLKRST_EMAC_PTP_REF_CLK_SRC_SEL |  |  |  |  |  |  |  | HP_SYS_CLKRST_EMAC_TX_CLK_DIV_NUM |  |  |  |  |  |  |  | HP_SYS_CLKRST_EMAC_TX_CLK_EN |  |  |  |  |  |  |  | HP_SYS_CLKRST_EMAC_TX_CLK_SRC_SEL |  |  |  |  |  |  |  | HP_SYS_CLKRST_EMAC_RX_CLK_DIV_NUM |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  | 25                           |  |  |  |  |  |  |  | 24                                | 23 | 22 | 21 | 20 | 19 | 18 | 17 |            |  |  |  |  |  |  | 10 |                            |  |  |  |  |  |  | 9 | 8                                 | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  | 0                            |  |  |  |  |  |  |  | 0                                 | 0  | 0  | 0  | 0  | 0  | 0  | 1  |            |  |  |  |  |  |  | 0  |                            |  |  |  |  |  |  | 0 | 1                                 |   |   |  |  |  |  |  | Reset                                  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_EMAC\_RX\_CLK\_DIV\_NUM** Configures the clock divisor for EMAC\_RX\_CLK.  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_TX\_CLK\_SRC\_SEL** Configures the clock source for EMAC\_TX\_CLK.  
0: PAD\_EMAC\_TXRX\_CLK  
1: PAD\_EMAC\_TX\_CLK  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_TX\_CLK\_EN** Configures whether to enable EMAC\_TX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_TX\_CLK\_DIV\_NUM** Configures the clock divisor for EMAC\_TX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_EMAC\_PTP\_REF\_CLK\_SRC\_SEL** Configures the clock source for EMAC\_PTP\_REF\_CLK.  
0: XTAL\_CLK  
1: PLL\_F80M\_CLK  
(R/W)

**HP\_SYS\_CLKRST\_EMAC\_PTP\_REF\_CLK\_EN** Configures whether to enable EMAC\_PTP\_REF\_CLK.  
0: Disable  
1: Enable  
(R/W)

Continued on the next page...

**Register 9.14. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL01\_REG (0x0034)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_SDIO\_HS\_MODE** Configures the mode of SDIO clock.

0: Low-speed mode

1: High-speed mode

(R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_SRC\_SEL** Configures the low-speed clock source for SDIO.

0: PLL\_F160M\_CLK

1: APLL\_CLK

(R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_EN** Configures whether to enable SDIO low-speed clock.

0: Disable

1: Enable

(R/W)

**Register 9.15. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL02\_REG (0x0038)**

|   |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |    |    |  |  |                                  |    |   |  |   |  |   |   |   |  |  |  |   |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|----|----|----|----|----|----|----|----|----|----|----|----|--|--|--|----|----|--|--|----------------------------------|----|---|--|---|--|---|---|---|--|--|--|---|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| HP_SYS_CLKRST_MIP1_DSI_DPHY_CLK_SRC_SEL |    |    |    |    |    |    |    |    |    |    |    |    |  |  |  |    |    |  |  | HP_SYS_CLKRST_SDIO_LS_SAM_CLK_EN |    |   |  |   |  |   |   |   |  |  |  |   |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_DRV_CLK_EN |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_SLF_CLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_SAM_CLK_EDGE_SEL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_DRV_CLK_EDGE_SEL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_SLF_CLK_EDGE_SEL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_EDGE_N |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_EDGE_H |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_EDGE_L |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_EDGE_CFG_UPDATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_SDIO_LS_CLK_DIV_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 17 |  |  |  | 16 | 13 |  |  |                                  | 12 | 9 |  |   |  | 8 | 7 | 0 |  |  |  |   |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                                       |    |    |    | 0  |    |    |    | 0  |    |    |    | 0  |  |  |  | 0  |    |  |  | 0                                |    |   |  | 0 |  |   |   | 0 |  |  |  | 0 |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_DIV\_NUM** Configures the divisor of the SDIO low-speed clock.  
(R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_EDGE\_CFG\_UPDATE** Configures whether to update the SDIO low-speed clock phase configuration.  
0: Not update  
1: Update (WT)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_EDGE\_L** Configures the threshold for the SDIO low-speed clock signal to switch to the low level. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_EDGE\_H** Configures the threshold for the SDIO low-speed clock signal to switch to the high level. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_CLK\_EDGE\_N** Configures the threshold for clearing the count value of the SDIO low-speed clock. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_SLF\_CLK\_EDGE\_SEL** Configures SDIO\_SLF\_CLK to select the SDIO low-speed clock phase. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_DRV\_CLK\_EDGE\_SEL** Configures SDIO\_DRV\_CLK to select the SDIO low-speed clock phase. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_SAM\_CLK\_EDGE\_SEL** Configures SDIO\_SAM\_CLK to select the SDIO low-speed clock phase. (R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_SLF\_CLK\_EN** Configures whether to enable SDIO\_SLF\_CLK.  
0: Disable  
1: Enable  
(R/W)

Continued on the next page...

**Register 9.15. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL02\_REG (0x0038)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_SDIO\_LS\_DRV\_CLK\_EN** Configures whether to enable SDIO\_DRV\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_SDIO\_LS\_SAM\_CLK\_EN** Configures whether to enable SDIO\_SAM\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPHY\_CLK\_SRC\_SEL** Configures the clock source for DSI\_DPHY\_CFG\_CLK and DSI\_DPHY\_PLL\_REFCLK.

0: PLL\_F20M\_CLK

1: RC\_FAST\_CLK

2: PLL\_F25M\_CLK

3: Invalid

(R/W)

Register 9.16. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL03\_REG (0x003C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |    |   |   |   |   |   |   |                                  |   |   |   |                                       |   |   |   |  |   |   |       |   |  |  |  |   |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|----|---|---|---|---|---|---|----------------------------------|---|---|---|---------------------------------------|---|---|---|--|---|---|-------|---|--|--|--|---|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_MIPI_DSI_DPICLK_DIV_NUM |    |   |   |   |   |   |   | HP_SYS_CLKRST_MIPI_DSI_DPICLK_EN |   |   |   | HP_SYS_CLKRST_MIPI_DSI_DPICLK_SRC_SEL |   |   |   | HP_SYS_CLKRST_MIPI_CSI_DPHY_CFG_CLK_EN |   |   |       | HP_SYS_CLKRST_MIPI_DSI_DPHY_CLK_SRC_SEL |  |  |  | HP_SYS_CLKRST_MIPI_DSI_DPHY_PLL_REFCLK_EN |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                                    | 15 |   |   |   |   |   |   |                                  |   | 8 | 7 | 6                                     | 5 | 4 | 3 | 2                                      | 1 | 0 |       |   |  |  |  |   |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0                                      | 0 | 0 | Reset |   |  |  |  |   |  |  |  |

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPHY\_CFG\_CLK\_EN**    Configures            whether            to            enable  
DSI\_DPHY\_CFG\_CLK clock.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPHY\_PLL\_REFCLK\_EN**    Configures            whether            to            enable  
DSI\_DPHY\_PLL\_REFCLK clock.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_MIPI\_CSI\_DPHY\_CLK\_SRC\_SEL**    Configures            the            clock            source            for  
CSI\_DPHY\_CFG\_CLK.  
0: PLL\_F20M\_CLK  
1: RC\_FAST\_CLK  
2: PLL\_F25M\_CLK  
3: Invalid  
(R/W)

**HP\_SYS\_CLKRST\_MIPI\_CSI\_DPHY\_CFG\_CLK\_EN**    Configures            whether            to            enable  
CSI\_DPHY\_CFG\_CLK clock.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPICLK\_SRC\_SEL**    Configures the clock source for DSI\_DPI\_CLK.  
0: XTAL\_CLK  
1: PLL\_F240M\_CLK  
2: PLL\_F160M\_CLK  
3: Invalid  
(R/W)

**Register 9.16. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL03\_REG (0x003C)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPICKL\_EN** Configures whether to enable DSI\_DPI\_CLK clock.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MIPI\_DSI\_DPICKL\_DIV\_NUM** Configures the clock divisor of DSI\_DPI\_CLK.

(R/W)

Register 9.17. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL10\_REG (0x0040)

|            |    |    |    |   |    |    |    |  |   |   |   |                                      |  |  |  |                                |  |  |  |   |  |  |  |
|------------|----|----|----|---|----|----|----|--|---|---|---|--------------------------------------|--|--|--|--------------------------------|--|--|--|---|--|--|--|
| (reserved) |    |    |    | HP_SYS_CLKRST_I2C1_CLK_EN<br>HP_SYS_CLKRST_I2C1_CLK_SRC_SEL |    |    |    | HP_SYS_CLKRST_I2CO_CLK_DIV_DENOMINATOR |   |   |   | HP_SYS_CLKRST_I2CO_CLK_DIV_NUMERATOR |  |  |  | HP_SYS_CLKRST_I2CO_CLK_DIV_NUM |  |  |  | HP_SYS_CLKRST_I2CO_CLK_EN<br>HP_SYS_CLKRST_I2CO_CLK_SRC_SEL |  |  |  |
| 31         | 28 | 27 | 26 | 25  | 18 | 17 | 10 | 9                                      | 2 | 1 | 0 | Reset                                |  |  |  |                                |  |  |  |   |  |  |  |
| 0          | 0  | 0  | 0  | 0   | 0  | 0  | 0  | 0                                      | 0 | 0 |   |                                      |  |  |  |                                |  |  |  |   |  |  |  |

**HP\_SYS\_CLKRST\_I2CO\_CLK\_SRC\_SEL** Configures the clock source for I2CO\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

(R/W)

**HP\_SYS\_CLKRST\_I2CO\_CLK\_EN** Configures whether to enable I2CO\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2CO\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor of I2CO\_CLK. (R/W)

**HP\_SYS\_CLKRST\_I2CO\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for clock divisor of I2CO\_CLK. (R/W)

**HP\_SYS\_CLKRST\_I2CO\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for clock divisor of I2CO\_CLK. (R/W)

**HP\_SYS\_CLKRST\_I2C1\_CLK\_SRC\_SEL** Configures the clock source for I2C1\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

(R/W)

**HP\_SYS\_CLKRST\_I2C1\_CLK\_EN** Configures whether to enable I2C1\_CLK.

0: Disable

1: Enable

(R/W)

Register 9.18. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL11\_REG (0x0044)

|            |   |    |   |   |   |                                   |    |    |    |    |  |                              |   |    |   |  |   |  |   |   |       |  |  |                                      |  |  |  |  |  |                                |  |  |  |  |  |
|------------|---|----|---|---|---|-----------------------------------|----|----|----|----|--|------------------------------|---|----|---|--|---|--|---|---|-------|--|--|--------------------------------------|--|--|--|--|--|--------------------------------|--|--|--|--|--|
| (reserved) |   |    |   |   |   | HP_SYS_CLKRST_I2SO_RX_CLK_SRC_SEL |    |    |    |    |  | HP_SYS_CLKRST_I2SO_RX_CLK_EN |   |    |   |  |   | HP_SYS_CLKRST_I2C1_CLK_DIV_DENOMINATOR |   |   |       |  |  | HP_SYS_CLKRST_I2C1_CLK_DIV_NUMERATOR |  |  |  |  |  | HP_SYS_CLKRST_I2C1_CLK_DIV_NUM |  |  |  |  |  |
| 31         |   | 27 |   |   |   | 26                                | 25 | 24 | 23 | 16 |  |                              |   | 15 | 8 |  |   |  | 7 | 0 |       |  |  |                                      |  |  |  |  |  |                                |  |  |  |  |  |
| 0          | 0 | 0  | 0 | 0 | 0 | 0                                 | 0  | 0  | 0  |    |  |                              | 0 |    |   |  | 0 |  |   |   | Reset |  |  |                                      |  |  |  |  |  |                                |  |  |  |  |  |

Reset

**HP\_SYS\_CLKRST\_I2C1\_CLK\_DIV\_NUM** Configures the integer part of the I2C1\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2C1\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for I2C1\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2C1\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for I2C1\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2SO\_RX\_CLK\_EN** Configures whether to enable I2SO\_RX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_I2SO\_RX\_CLK\_SRC\_SEL** Configures the clock source for I2SO\_RX\_CLK.  
0: XTAL\_CLK  
1: APLL\_CLK  
2: PAD\_I2SO\_MCLK  
3: Invalid  
(R/W)



Register 9.19. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL12\_REG (0x0048)

|            |   |   |   |   |   |    |                             |  |  |  |  |   |    |                             |  |  |   |  |  |   |                             |   |  |  |  |  |       |
|------------|---|---|---|---|---|----|-----------------------------|--|--|--|--|---|----|-----------------------------|--|--|---|--|--|---|-----------------------------|---|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |    | HP_SYS_CLKRST_I2SO_RX_DIV_Y |  |  |  |  |   |    | HP_SYS_CLKRST_I2SO_RX_DIV_X |  |  |   |  |  |   | HP_SYS_CLKRST_I2SO_RX_DIV_N |   |  |  |  |  |       |
| 31         |   |   |   |   |   | 26 | 25                          |  |  |  |  |   | 17 | 16                          |  |  |   |  |  | 8 | 7                           |   |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0  | 0                           |  |  |  |  | 0 |    |                             |  |  | 0 |  |  |   |                             | 0 |  |  |  |  | Reset |

**HP\_SYS\_CLKRST\_I2SO\_RX\_DIV\_N** Configures the integer part of the I2SO\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2SO\_RX\_DIV\_X** Configures the coefficient x of the I2SO\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2SO\_RX\_DIV\_Y** Configures the coefficient y of the I2SO\_RX\_CLK clock divisor.  
(R/W)

### Register 9.20. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL13\_REG (0x004C)

Diagram of the HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_X register. The register is 32 bits wide, divided into four 8-bit fields. Bit 31 is reserved. Bit 30 is 0. Bit 29 is 0. Bit 21 is 0. Bit 20 is 0. Bit 13 is 0. Bit 12 is 0. Bit 11 is 0. Bit 10 is 0. Bit 9 is 0. Bit 8 is 0. Bit 0 is 0. The register is labeled 'Reset'.

**HP\_SYS\_CLKRST\_I2SO\_RX\_DIV\_Z** Configures the coefficient z of I2SO\_RX\_CLK clock divisor.  
(R/W)

|                               |   |
|-------------------------------|---|
| HP_SYS_CLKRST_I2SO_RX_DIV_YN1 | Configures the coefficient yn1 of I2SO_RX_CLK clock divisor.<br>(R/W) |
|-------------------------------|---|

**HP\_SYS\_CLKRST\_I2SO\_TX\_CLK\_EN** Configures whether to enable I2SO\_TX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_I2SO\_TX\_CLK\_SRC\_SEL** Configures the clock source for I2SO\_TX\_CLK.

- 0: XTAL\_CLK
- 1: APLL\_CLK
- 2: PAD\_I2SO\_MCLK
- 3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_N** Configures the integer part of the clock divisor of I2S0\_TX\_CLK.  
(R/W)

**HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_X** Configures the coefficient x of I2S0\_TX\_CLK clock divisor. (R/W)

Register 9.21. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL14\_REG (0x0050)

|            |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |                                   |    |    |    |    |    |                              |    |   |  |  |  |                                |  |  |  |  |  |                               |  |  |  |   |  |                             |   |   |  |  |  |                             |  |  |  |  |  |  |  |  |       |  |  |  |
|------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|-----------------------------------|----|----|----|----|----|------------------------------|----|---|--|--|--|--------------------------------|--|--|--|--|--|-------------------------------|--|--|--|---|--|-----------------------------|---|---|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|-------|--|--|--|
| (reserved) |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_DIV_N |  |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_CLK_SRC_SEL |    |    |    |    |    | HP_SYS_CLKRST_I2S1_RX_CLK_EN |    |   |  |  |  | HP_SYS_CLKRST_I2S0_MST_CLK_SEL |  |  |  |  |  | HP_SYS_CLKRST_I2S0_TX_DIV_YN1 |  |  |  |   |  | HP_SYS_CLKRST_I2S0_TX_DIV_Z |   |   |  |  |  | HP_SYS_CLKRST_I2S0_TX_DIV_Y |  |  |  |  |  |  |  |  |       |  |  |  |
| 31         | 30 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |                                   | 23 | 22 | 21 | 20 | 19 | 18                           | 17 | 9 |  |  |  |                                |  |  |  |  |  |                               |  |  |  |   |  |                             | 8 | 0 |  |  |  |                             |  |  |  |  |  |  |  |  |       |  |  |  |
| 0          | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |                                   | 0  | 0  | 0  | 0  | 0  |                              |    |   |  |  |  |                                |  |  |  |  |  |                               |  |  |  | 0 |  |                             |   |   |  |  |  |                             |  |  |  |  |  |  |  |  | Reset |  |  |  |

**HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_Y** Configures the coefficient y for I2S0\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_Z** Configures the coefficient z for I2S0\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S0\_TX\_DIV\_YN1** Configures the coefficient yn1 for I2S0\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S0\_MST\_CLK\_SEL** Configures the clock source for the output clock PAD\_I2S0\_MST\_CLK.  
0: I2S0\_RX\_CLK  
1: I2S0\_TX\_CLK  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_CLK\_EN** Configures whether to enable I2S1\_RX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_CLK\_SRC\_SEL** Configures the clock source for I2S1\_RX\_CLK.  
0: XTAL\_CLK  
1: APLL\_CLK  
2: PAD\_I2S1\_MCLK  
3: Invalid  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_DIV\_N** Configures the integer part of the clock divisor for I2S1\_RX\_CLK.  
(R/W)

**Register 9.22. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL15\_REG (0x0054)**

|            |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |                                   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |                              |  |  |  |  |  |       |  |  |  |  |   |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|----|----|----|----|--|--|--|--|--|--|--|--|--|--|-----------------------------------|----|----|--|--|--|--|--|--|--|--|---|--|--|---|---|------------------------------|--|--|--|--|--|-------|--|--|--|--|---|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_TX_CLK_SRC_SEL |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   | HP_SYS_CLKRST_I2S1_TX_CLK_EN |  |  |  |  |  |       |  |  |  |  |   |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_DIV_YN1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_DIV_Z |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_DIV_Y |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_RX_DIV_X |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30 | 29 | 28 | 27 | 26 |  |  |  |  |  |  |  |  |  |  |                                   | 18 | 17 |  |  |  |  |  |  |  |  |   |  |  | 9 | 8 |                              |  |  |  |  |  |       |  |  |  |  | 0 |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0  |  |  |  |  |  |  |  |  |  |  | 0                                 |    |    |  |  |  |  |  |  |  |  | 0 |  |  |   |   |                              |  |  |  |  |  | Reset |  |  |  |  |   |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_I2S1\_RX\_DIV\_X** Configures the coefficient x for I2S1\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_DIV\_Y** Configures the coefficient y for I2S1\_RX\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_DIV\_Z** Configures the coefficient z for I2S1\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_RX\_DIV\_YN1** Configures the coefficient yn1 for I2S1\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_TX\_CLK\_EN** Configures whether to enable PI2S1\_TX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_TX\_CLK\_SRC\_SEL** Configures the clock source for I2S1\_TX\_CLK.  
0: XTAL\_CLK  
1: APLL\_CLK  
2: PAD\_I2S1\_MCLK  
3: Invalid  
(R/W)

Register 9.23. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL16\_REG (0x0058)

|            |   |   |   |   |   |                             |    |  |  |  |  |  |  |  |   |    |                             |  |  |  |  |  |   |  |   |   |  |  |  |                             |   |  |  |  |  |  |  |  |       |  |  |  |  |  |   |
|------------|---|---|---|---|---|-----------------------------|----|--|--|--|--|--|--|--|---|----|-----------------------------|--|--|--|--|--|---|--|---|---|--|--|--|-----------------------------|---|--|--|--|--|--|--|--|-------|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   | HP_SYS_CLKRST_I2S1_TX_DIV_Y |    |  |  |  |  |  |  |  |   |    | HP_SYS_CLKRST_I2S1_TX_DIV_X |  |  |  |  |  |   |  |   |   |  |  |  | HP_SYS_CLKRST_I2S1_TX_DIV_N |   |  |  |  |  |  |  |  |       |  |  |  |  |  |   |
| 31         |   |   |   |   |   | 26                          | 25 |  |  |  |  |  |  |  |   | 17 | 16                          |  |  |  |  |  |   |  | 8 | 7 |  |  |  |                             |   |  |  |  |  |  |  |  |       |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0                           | 0  |  |  |  |  |  |  |  | 0 |    |                             |  |  |  |  |  | 0 |  |   |   |  |  |  |                             | 0 |  |  |  |  |  |  |  | Reset |  |  |  |  |  |   |

HP\_SYS\_CLKRST\_I2S1\_TX\_DIV\_N    Configures the integer part of the clock divisor for I2S1\_TX\_CLK.  
(R/W)

HP\_SYS\_CLKRST\_I2S1\_TX\_DIV\_X    Configures the coefficient x for I2S1\_TX\_CLK clock divisor. (R/W)

HP\_SYS\_CLKRST\_I2S1\_TX\_DIV\_Y    Configures the coefficient y for I2S1\_TX\_CLK clock divisor. (R/W)

### Register 9.24. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL17\_REG (0x005C)

|            |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |                             |  |  |  |  |  |  |  |  |  |  |  |   |   |    |    |  |    |   |   |   |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|---|---|----|----|--|----|---|---|---|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S2_RX_DIV_X |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    | HP_SYS_CLKRST_I2S2_RX_DIV_N |  |  |  |  |  |  |  |  |  |  |  |   |   |    |    | HP_SYS_CLKRST_I2S2_RX_CLK_SRC_SEL<br>HP_SYS_CLKRST_I2S2_RX_CLK_EN<br>HP_SYS_CLKRST_I2S1_MST_CLK_SEL<br>HP_SYS_CLKRST_I2S1_TX_DIV_YN1 |    |   |   |   |  |  |  |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_I2S1_TX_DIV_Z |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  | 22 | 21 | 14                          |  |  |  |  |  |  |  |  |  |  |  |   |   | 13 | 12 | 11   | 10 | 9 | 8 | 0 |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  |    |                             |  |  |  |  |  |  |  |  |  |  |  | 0 | 0 | 0  | 0  | 0  |    |   |   |   |  |  |  |  |  |  |  |  |  |  |  | Reset                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_I2S1\_TX\_DIV\_Z** Configures the coefficient z for I2S1\_TX\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2S1\_TX\_DIV\_YN1** Configures the coefficient yn1 for I2S1\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S1\_MST\_CLK\_SEL** Configures the clock source for the output clock PAD\_I2S1\_MST\_CLK.

0: I2S1\_RX\_CLK

1: I2S1\_TX\_CLK

(R/W)

**HP\_SYS\_CLKRST\_I2S2\_RX\_CLK\_EN** Configures whether to enable I2S2\_RX\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I2S2\_RX\_CLK\_SRC\_SEL** Configures the clock source for I2S2\_RX\_CLK.

0: XTAL CLK

1: APLL\_CLK

2: PAD\_I2S2\_MCLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_I2S2\_RX\_DIV\_N** Configures the integer part of the clock divisor for I2S2\_RX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_I2S2\_RX\_DIV\_X** Configures the coefficient x for I2S2\_RX\_CLK clock divisor.  
(R/W)

### Register 9.25. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL18\_REG (0x0060)

|            |    |    |                             |  |  |   |                                   |    |    |    |                              |    |  |  |                              |   |   |   |                             |       |  |  |                             |  |  |  |
|------------|----|----|-----------------------------|--|--|---|-----------------------------------|----|----|----|------------------------------|----|--|--|------------------------------|---|---|---|-----------------------------|-------|--|--|-----------------------------|--|--|--|
| (reserved) |    |    | HP_SYS_CLKRST_I2S2_TX_DIV_N |  |  |   | HP_SYS_CLKRST_I2S2_TX_CLK_SRC_SEL |    |    |    | HP_SYS_CLKRST_I2S2_TX_CLK_EN |    |  |  | HP_SYS_CLKRST_I2S2_RX_DIV_N1 |   |   |   | HP_SYS_CLKRST_I2S2_RX_DIV_Z |       |  |  | HP_SYS_CLKRST_I2S2_RX_DIV_Y |  |  |  |
| 31         | 30 | 29 |                             |  |  |   | 22                                | 21 | 20 | 19 | 18                           | 17 |  |  |                              |   | 9 | 8 |                             |       |  |  | 0                           |  |  |  |
| 0          | 0  | 0  |                             |  |  | 0 |                                   |    |    | 0  | 0                            | 0  |  |  |                              | 0 |   |   |                             | Reset |  |  |                             |  |  |  |

**HP\_SYS\_CLKRST\_I2S2\_RX\_DIV\_Y** Configures the coefficient  $y$  for I2S2\_RX\_CLK clock divisor.  
(R/W)

HP\_SYS\_CLKRST\_I2S2\_RX\_DIV\_Z Configures the coefficient z for I2S2\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S2\_RX\_DIV\_YN1** Configures the coefficient yn1 for I2S2\_RX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_CLK\_EN** Configures whether to enable I2S2\_TX\_CLK.  
0: Disable  
1: Enable  
(R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_CLK\_SRC\_SEL** Configures the clock source for I2S2\_TX\_CLK.

- 0: XTAL\_CLK
- 1: APLL\_CLK
- 2: PAD\_I2S2\_MCLK
- 3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_DIV\_N** Configures the integer part for I2S2\_TX\_CLK clock divisor. (R/W)

**Register 9.26. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL19\_REG (0x0064)**

|                                |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
|--------------------------------|----|----|----|----|----|--|--|--|--|--|--|--|--|--|--|---|----|----|--|--|--|--|--|--|--|--|---|--|--|---|---|--|--|--|--|--|--|-------|--|--|--|--|---|
| HP_SYS_CLKRST_LCD_CLK_EN       |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_LCD_CLK_SRC_SEL  |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_I2S2_MST_CLK_SEL |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_I2S2_TX_DIV_YN1  |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_I2S2_TX_DIV_Z    |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_I2S2_TX_DIV_Y    |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| HP_SYS_CLKRST_I2S2_TX_DIV_X    |    |    |    |    |    |  |  |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |   |  |  |   |   |  |  |  |  |  |  |       |  |  |  |  |   |
| 31                             | 30 | 29 | 28 | 27 | 26 |  |  |  |  |  |  |  |  |  |  |   | 18 | 17 |  |  |  |  |  |  |  |  |   |  |  | 9 | 8 |  |  |  |  |  |  |       |  |  |  |  | 0 |
| 0                              | 0  | 0  | 0  | 0  | 0  |  |  |  |  |  |  |  |  |  |  | 0 |    |    |  |  |  |  |  |  |  |  | 0 |  |  |   |   |  |  |  |  |  |  | Reset |  |  |  |  |   |

**HP\_SYS\_CLKRST\_I2S2\_TX\_DIV\_X** Configures the coefficient x of I2S2\_TX\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_DIV\_Y** Configures the coefficient y of I2S2\_TX\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_DIV\_Z** Configures the coefficient z of I2S2\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S2\_TX\_DIV\_YN1** Configures the coefficient yn1 of I2S2\_TX\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_I2S2\_MST\_CLK\_SEL** Configures the clock source for output clock PAD\_I2S2\_MST\_CLK.  
0: I2S2\_RX\_CLK  
1: I2S2\_TX\_CLK  
(R/W)

**HP\_SYS\_CLKRST\_LCD\_CLK\_SRC\_SEL** Configures the clock source for LCD\_CLK.  
0: XTAL\_CLK  
1: PLL\_F160M\_CLK  
2: APLL\_CLK  
3: Invalid  
(R/W)

**HP\_SYS\_CLKRST\_LCD\_CLK\_EN** Configures whether to enable LCD\_CLK.  
0: Disable  
1: Enable  
(R/W)



**Register 9.27. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL110\_REG (0x0068)**

|            |   |   |   |   |                            |    |    |    |    |                                 |  |   |  |    |                                       |   |  |  |  |                                     |   |  |  |       |                               |   |  |  |  |
|------------|---|---|---|---|----------------------------|----|----|----|----|---------------------------------|--|---|--|----|---------------------------------------|---|--|--|--|-------------------------------------|---|--|--|-------|-------------------------------|---|--|--|--|
| (reserved) |   |   |   |   | HP_SYS_CLKRST_UART0_CLK_EN |    |    |    |    | HP_SYS_CLKRST_UART0_CLK_SRC_SEL |  |   |  |    | HP_SYS_CLKRST_LCD_CLK_DIV_DENOMINATOR |   |  |  |  | HP_SYS_CLKRST_LCD_CLK_DIV_NUMERATOR |   |  |  |       | HP_SYS_CLKRST_LCD_CLK_DIV_NUM |   |  |  |  |
| 31         |   |   |   |   | 27                         | 26 | 25 | 24 | 23 |                                 |  |   |  | 16 | 15                                    |   |  |  |  | 8                                   | 7 |  |  |       |                               | 0 |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0                          | 1  | 0  | 0  |    |                                 |  | 0 |  |    |                                       | 0 |  |  |  | 0                                   |   |  |  | Reset |                               |   |  |  |  |

Reset

**HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_NUM** Configures the integer part of the LCD\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for LCD\_CLK. (R/W)

**HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for LCD\_CLK. (R/W)

**HP\_SYS\_CLKRST\_UART0\_CLK\_SRC\_SEL** Configures the clock source for UART0\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_UART0\_CLK\_EN** Configures whether to enable UART0\_CLK.

0: Disable

1: Enable

(R/W)

**Register 9.28. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL111\_REG (0x006C)**

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| 31         |  | 27 | 26 | 25 | 24 | 23                         |  | 16 | 15 |  | 8 | 7                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_UART0\_SCLK\_DIV\_NUM** Configures the integer part of the UART0\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART0\_SCLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for UART0\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART0\_SCLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for UART0\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART1\_CLK\_SRC\_SEL** Configures the clock source for UART1\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_UART1\_CLK\_EN** Configures whether to enable UART1\_CLK.

0: Disable

1: Enable

(R/W)

**Register 9.29. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL112\_REG (0x0070)**

|            |   |   |   |   |                            |    |    |    |    |                                 |  |  |  |    |  |  |  |  |   |  |   |  |  |       |                                  |   |  |  |  |
|------------|---|---|---|---|----------------------------|----|----|----|----|---------------------------------|--|--|--|----|--|--|--|--|---|--|---|--|--|-------|----------------------------------|---|--|--|--|
| (reserved) |   |   |   |   | HP_SYS_CLKRST_UART2_CLK_EN |    |    |    |    | HP_SYS_CLKRST_UART2_CLK_SRC_SEL |  |  |  |    | HP_SYS_CLKRST_UART1_SCLK_DIV_DENOMINATOR |  |  |  |   | HP_SYS_CLKRST_UART1_SCLK_DIV_NUMERATOR |   |  |  |       | HP_SYS_CLKRST_UART1_SCLK_DIV_NUM |   |  |  |  |
| 31         |   |   |   |   | 27                         | 26 | 25 | 24 | 23 |                                 |  |  |  | 16 | 15                                       |  |  |  |   | 8                                      | 7 |  |  |       |                                  | 0 |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 1                          | 0  |    |    | 0  |                                 |  |  |  | 0  |  |  |  |  | 0 |  |   |  |  | Reset |                                  |   |  |  |  |

**HP\_SYS\_CLKRST\_UART1\_SCLK\_DIV\_NUM** Configures the integer part of the UART1\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART1\_SCLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for UART1\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART1\_SCLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for UART1\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART2\_CLK\_SRC\_SEL** Configures the clock source for UART2\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_UART2\_CLK\_EN** Configures whether to enable the UART2\_CLK clock.

0: Disable

1: Enable

(R/W)

Register 9.30. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL113\_REG (0x0074)

|            |   |   |   |   |   |                            |    |    |    |    |  |                                 |  |  |   |    |    |  |  |  |   |  |   |  |  |  |       |  |  |                                  |  |  |  |  |  |
|------------|---|---|---|---|---|----------------------------|----|----|----|----|--|---------------------------------|--|--|---|----|----|--|--|--|---|--|---|--|--|--|-------|--|--|----------------------------------|--|--|--|--|--|
| (reserved) |   |   |   |   |   | HP_SYS_CLKRST_UART3_CLK_EN |    |    |    |    |  | HP_SYS_CLKRST_UART3_CLK_SRC_SEL |  |  |   |    |    | HP_SYS_CLKRST_UART2_SCLK_DIV_DENOMINATOR |  |  |   |  |   | HP_SYS_CLKRST_UART2_SCLK_DIV_NUMERATOR |  |  |       |  |  | HP_SYS_CLKRST_UART2_SCLK_DIV_NUM |  |  |  |  |  |
| 31         |   |   |   |   |   | 27                         | 26 | 25 | 24 | 23 |  |                                 |  |  |   | 16 | 15 |  |  |  |   |  | 8 | 7                                      |  |  |       |  |  | 0                                |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 1                          | 0  |    | 0  |    |  |                                 |  |  | 0 |    |    |  |  |  | 0 |  |   |  |  |  | Reset |  |  |                                  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_UART2\_SCLK\_DIV\_NUM** Configures the integer part of the UART2\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART2\_SCLK\_DIV\_NUMERATOR** Configures the numerator of the fractional part of the UART2\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART2\_SCLK\_DIV\_DENOMINATOR** Configures the denominator of the fractional part of the UART2\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART3\_CLK\_SRC\_SEL** Configures the clock source for UART3\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_UART3\_CLK\_EN** Configures whether to enable the UART3\_CLK clock.

0: Disable

1: Enable

(R/W)

**Register 9.31. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL114\_REG (0x0078)**

|            |   |   |   |   |   |                            |    |    |    |    |  |                                 |  |  |   |    |    |  |  |  |   |  |   |  |  |  |       |  |  |                                  |  |  |  |  |  |
|------------|---|---|---|---|---|----------------------------|----|----|----|----|--|---------------------------------|--|--|---|----|----|--|--|--|---|--|---|--|--|--|-------|--|--|----------------------------------|--|--|--|--|--|
| (reserved) |   |   |   |   |   | HP_SYS_CLKRST_UART4_CLK_EN |    |    |    |    |  | HP_SYS_CLKRST_UART4_CLK_SRC_SEL |  |  |   |    |    | HP_SYS_CLKRST_UART3_SCLK_DIV_DENOMINATOR |  |  |   |  |   | HP_SYS_CLKRST_UART3_SCLK_DIV_NUMERATOR |  |  |       |  |  | HP_SYS_CLKRST_UART3_SCLK_DIV_NUM |  |  |  |  |  |
| 31         |   |   |   |   |   | 27                         | 26 | 25 | 24 | 23 |  |                                 |  |  |   | 16 | 15 |  |  |  |   |  | 8 | 7                                      |  |  |       |  |  | 0                                |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 1                          | 0  |    | 0  |    |  |                                 |  |  | 0 |    |    |  |  |  | 0 |  |   |  |  |  | Reset |  |  |                                  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_UART3\_SCLK\_DIV\_NUM** Configures the integer part of the UART3\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART3\_SCLK\_DIV\_NUMERATOR** Configures the numerator of the fractional part of the UART3\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART3\_SCLK\_DIV\_DENOMINATOR** Configures the denominator of the fractional part of the UART3\_SCLK. (R/W)

**HP\_SYS\_CLKRST\_UART4\_CLK\_SRC\_SEL** Configures the clock source for UART4\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_UART4\_CLK\_EN** Configures whether to enable the UART4\_CLK clock.

0: Disable

1: Enable

(R/W)

Register 9.32. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL115\_REG (0x007C)

|            |    |    |    |    |    |    |    |    |                            |  |  |  |  |  |  |  |  |                                 |    |  |  |  |  |  |  |  |                            |  |   |   |  |  |  |  |  |                                 |  |  |  |   |  |  |  |  |                            |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |
|------------|----|----|----|----|----|----|----|----|----------------------------|--|--|--|--|--|--|--|--|---------------------------------|----|--|--|--|--|--|--|--|----------------------------|--|---|---|--|--|--|--|--|---------------------------------|--|--|--|---|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |    |    |    |    | HP_SYS_CLKRST_TWA12_CLK_EN |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWA12_CLK_SRC_SEL |    |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWA11_CLK_EN |  |   |   |  |  |  |  |  | HP_SYS_CLKRST_TWA11_CLK_SRC_SEL |  |  |  |   |  |  |  |  | HP_SYS_CLKRST_TWA10_CLK_EN |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_TWA10_CLK_SRC_SEL |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART4_SCLK_DIV_DENOMINATOR |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART4_SCLK_DIV_NUMERATOR |  |  |  |  |  |  |  |  | HP_SYS_CLKRST_UART4_SCLK_DIV_NUM |  |  |  |  |  |  |  |  |
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 |                            |  |  |  |  |  |  |  |  | 16                              | 15 |  |  |  |  |  |  |  |                            |  | 8 | 7 |  |  |  |  |  |                                 |  |  |  | 0 |  |  |  |  |                            |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                          |  |  |  |  |  |  |  |  |                                 |    |  |  |  |  |  |  |  | 0                          |  |   |   |  |  |  |  |  | 0                               |  |  |  |   |  |  |  |  | 0                          |  |  |  |  |  |  |  |  | Reset                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_UART4\_SCLK\_DIV\_NUM** Configures the integer part of the UART4\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART4\_SCLK\_DIV\_NUMERATOR** Configures the numerator of the fractional part of the UART4\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_UART4\_SCLK\_DIV\_DENOMINATOR** Configures the denominator of the fractional part of the UART4\_SCLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_TWAI0\_CLK\_SRC\_SEL** Configures the clock source for TWAI0\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

(R/W)

**HP\_SYS\_CLKRST\_TWAIO\_CLK\_EN** Configures whether to enable TWAIO\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TWA1\_CLK\_SRC\_SEL** Configures the clock source for TWA1\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

(R/W)

**HP\_SYS\_CLKRST\_TWAI1\_CLK\_EN** Configures whether to enable TWAI1\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TWAI2\_CLK\_SRC\_SEL** Configures the clock source for TWAI2\_CLK.

0: XTAL CLK

1: RC FAST CLK

(R/W)

**HP\_SYS\_CLKRST\_TWAI2\_CLK\_EN** Configures whether to enable TWAI2\_CLK.

0: Disable

1: Enable

(R/W)

**Register 9.33. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL116\_REG (0x0080)**

|            |    |   |   |   |    |    |    |                                |    |    |   |                                  |  |    |   |                                 |  |  |   |                                      |   |  |  |                                     |       |  |  |                                |  |  |  |                                  |  |  |  |
|------------|----|---|---|---|----|----|----|--------------------------------|----|----|---|----------------------------------|--|----|---|---------------------------------|--|--|---|--------------------------------------|---|--|--|-------------------------------------|-------|--|--|--------------------------------|--|--|--|----------------------------------|--|--|--|
| (reserved) |    |   |   |   |    |    |    | HP_SYS_CLKRST_GPSPi3_HS_CLK_EN |    |    |   | HP_SYS_CLKRST_GPSPi3_CLK_SRC_SEL |  |    |   | HP_SYS_CLKRST_GPSPi2_MST_CLK_EN |  |  |   | HP_SYS_CLKRST_GPSPi2_MST_CLK_DIV_NUM |   |  |  | HP_SYS_CLKRST_GPSPi2_HS_CLK_DIV_NUM |       |  |  | HP_SYS_CLKRST_GPSPi2_HS_CLK_EN |  |  |  | HP_SYS_CLKRST_GPSPi2_CLK_SRC_SEL |  |  |  |
| 31         | 25 |   |   |   | 24 | 23 | 21 | 20                             | 19 | 12 |   |                                  |  | 11 | 4 |                                 |  |  | 3 | 2                                    | 0 |  |  |                                     |       |  |  |                                |  |  |  |                                  |  |  |  |
| 0          | 0  | 0 | 0 | 0 | 0  | 0  | 0  | 1                              | 0  | 1  | 0 |                                  |  |    | 0 |                                 |  |  | 1 | 0                                    |   |  |  |                                     | Reset |  |  |                                |  |  |  |                                  |  |  |  |

Reset

**HP\_SYS\_CLKRST\_GPSPI2\_CLK\_SRC\_SEL** Configures the clock source for GPSPI2\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: SDIO\_PLLO\_CLK
  - 3: APLL\_CLK
  - 4: SPLL\_CLK (480 MHz)
  - 5-7: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_GPSPI2\_HS\_CLK\_EN** Configures whether to enable GPSPI2\_HS\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_GPSPI2\_HS\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor of GPSPI2\_HS\_CLK. (R/W)**HP\_SYS\_CLKRST\_GPSPI2\_MST\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor of GPSPI2\_MST\_CLK. (R/W)**HP\_SYS\_CLKRST\_GPSPI2\_MST\_CLK\_EN** Configures whether to enable GPSPI2\_MST\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_GPSPI3\_CLK\_SRC\_SEL** Configures the clock source for GPSPI3\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: SDIO\_PLLO\_CLK
  - 3: APLL\_CLK
  - 4: SPLL\_CLK (480 MHz)
  - 5-7: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_GPSPI3\_HS\_CLK\_EN** Configures whether to enable GPSPI3\_HS\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

Register 9.34. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL117\_REG (0x0084)

|            |    |    |   |                                     |    |    |    |                                |    |   |   |                                     |   |   |   |                                 |   |   |   |                                      |   |   |   |                                     |   |   |   |
|------------|----|----|---|-------------------------------------|----|----|----|--------------------------------|----|---|---|-------------------------------------|---|---|---|---------------------------------|---|---|---|--------------------------------------|---|---|---|-------------------------------------|---|---|---|
| (reserved) |    |    |   | HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_NUM |    |    |    | HP_SYS_CLKRST_PARLIO_RX_CLK_EN |    |   |   | HP_SYS_CLKRST_PARLIO_RX_CLK_SRC_SEL |   |   |   | HP_SYS_CLKRST_GPSPI3_MST_CLK_EN |   |   |   | HP_SYS_CLKRST_GPSPI3_MST_CLK_DIV_NUM |   |   |   | HP_SYS_CLKRST_GPSPI3_HS_CLK_DIV_NUM |   |   |   |
| 31         | 28 | 27 |   | 20                                  | 19 | 18 | 17 | 16                             | 15 |   | 8 | 7                                   |   |   |   |                                 |   |   |   |                                      |   |   |   |                                     |   |   |   |
| 0          | 0  | 0  | 0 | 0                                   | 0  | 0  | 0  | 1                              | 0  | 0 | 0 | 0                                   | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0                                    | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 |

Reset

**HP\_SYS\_CLKRST\_GPSPI3\_HS\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor for GPSPI3\_HS\_CLK. (R/W)

**HP\_SYS\_CLKRST\_GPSPI3\_MST\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor for GPSPI3\_MST\_CLK. (R/W)

**HP\_SYS\_CLKRST\_GPSPI3\_MST\_CLK\_EN** Configures whether to enable GPSPI3\_MST\_CLK.  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_RX\_CLK\_SRC\_SEL** Configures the clock source for PARLIO\_RX\_CLK.  
 0: XTAL\_CLK  
 1: RC\_FAST\_CLK  
 2: PLL\_F160M\_CLK  
 3: PAD\_PARLIO\_RX\_CLK  
 (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_RX\_CLK\_EN** Configures whether to enable PARLIO\_RX\_CLK.  
 0: Disable  
 1: Enable  
 (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_RX\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor for PARLIO\_RX\_CLK. (R/W)



Register 9.35. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL118\_REG (0x0088)

|            |    |   |   |   |                                     |    |  |  |                                |    |    |    |                                     |   |   |  |   |   |       |  |   |  |  |  |
|------------|----|---|---|---|-------------------------------------|----|--|--|--------------------------------|----|----|----|-------------------------------------|---|---|--|---|---|-------|--|---|--|--|--|
| (reserved) |    |   |   |   | HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_NUM |    |  |  | HP_SYS_CLKRST_PARLIO_TX_CLK_EN |    |    |    | HP_SYS_CLKRST_PARLIO_TX_CLK_SRC_SEL |   |   |  | HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_DENOMINATOR |   |       |  | HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_NUMERATOR |  |  |  |
| 31         | 27 |   |   |   | 26                                  | 19 |  |  |                                | 18 | 17 | 16 | 15                                  | 8 |   |  |   | 7 | 0     |  |   |  |  |  |
| 0          | 0  | 0 | 0 | 0 | 0                                   |    |  |  | 0                              | 0  | 0  |    |                                     |   | 0 |  |   |   | Reset |  |   |  |  |  |

Reset

**HP\_SYS\_CLKRST\_PARLIO\_RX\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for clock divisor for PARLIO\_RX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_RX\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for clock divisor for PARLIO\_RX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_TX\_CLK\_SRC\_SEL** Configures the clock source for PARLIO\_TX\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F160M\_CLK

3: PAD\_PARLIO\_TX\_CLK

(R/W)

**HP\_SYS\_CLKRST\_PARLIO\_TX\_CLK\_EN** Configures whether to enable PARLIO\_TX\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_PARLIO\_TX\_CLK\_DIV\_NUM** Configures the integer part of the clock divisor for PARLIO\_TX\_CLK. (R/W)

**Register 9.36. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL119\_REG (0x008C)**

|            |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| (reserved) |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   | HP_SYS_CLKRST_CAM_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_CAM_CLK_SRC_SEL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_I3C_MST_CLK_DIV_NUM |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_I3C_MST_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_I3C_MST_CLK_SRC_SEL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_DENOMINATOR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_NUMERATOR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         | 30 | 29 | 28 | 27 | 26 | 19 | 18 | 17 | 16 | 15 | 8 | 7 | 0 |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

Reset

**HP\_SYS\_CLKRST\_PARLIO\_TX\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for PARLIO\_TX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_PARLIO\_TX\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for PARLIO\_TX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_I3C\_MST\_CLK\_SRC\_SEL** Configures the clock source for I3C\_MST\_CLK.

0: XTAL\_CLK

1: PLL\_F160M\_CLK

2: PLL\_F120M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_I3C\_MST\_CLK\_EN** Configures whether to enable I3C\_MST\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_I3C\_MST\_CLK\_DIV\_NUM** Configures the integer part of the I3C\_MST\_CLK clock divisor. (R/W)

**HP\_SYS\_CLKRST\_CAM\_CLK\_SRC\_SEL** Configures the clock source for the output clock CAM\_CLK.

0: XTAL\_CLK

1: PLL\_F160M\_CLK

2: APLL\_CLK

3: Invalid

(R/W)

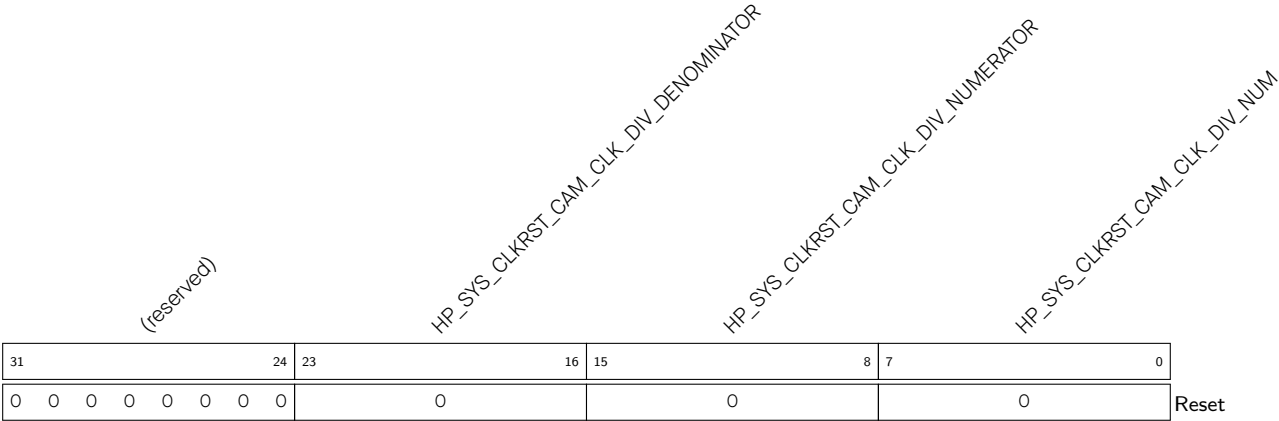
**HP\_SYS\_CLKRST\_CAM\_CLK\_EN** Configures whether to enable the output clock CAM\_CLK.

0: Disable

1: Enable

(R/W)

Register 9.37. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL120\_REG (0x0090)



**HP\_SYS\_CLKRST\_CAM\_CLK\_DIV\_NUM**    Configures the integer part of the CAM\_CLK clock divisor.  
(R/W)

**HP\_SYS\_CLKRST\_CAM\_CLK\_DIV\_NUMERATOR**    Configures the numerator of the divisor’s fractional part for CAM\_CLK. (R/W)

**HP\_SYS\_CLKRST\_CAM\_CLK\_DIV\_DENOMINATOR**    Configures the denominator of the divisor’s fractional part for CAM\_CLK. (R/W)

Register 9.38. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL20\_REG (0x0094)

|                                     |  |                                    |  |                                    |  |                                     |  |                                   |  |                                    |  |                                   |  |                                    |  |                                  |  |                             |  |                                  |  |                                  |  |                             |  |                                  |  |                                  |  |                             |  |                                  |  |                                  |  |                             |  |                                  |  |
|-------------------------------------|--|------------------------------------|--|------------------------------------|--|-------------------------------------|--|-----------------------------------|--|------------------------------------|--|-----------------------------------|--|------------------------------------|--|----------------------------------|--|-----------------------------|--|----------------------------------|--|----------------------------------|--|-----------------------------|--|----------------------------------|--|----------------------------------|--|-----------------------------|--|----------------------------------|--|----------------------------------|--|-----------------------------|--|----------------------------------|--|
| 31                                  |  | 30                                 |  | 29                                 |  | 28                                  |  | 27                                |  | 26                                 |  | 25                                |  | 24                                 |  | 23                               |  | 22                          |  | 21                               |  | 14                               |  | 13                          |  | 12                               |  | 11                               |  | 10                          |  | 3                                |  | 2                                |  | 1                           |  | 0                                |  |
| 1                                   |  | 1                                  |  | 0                                  |  | 1                                   |  | 0                                 |  | 1                                  |  | 0                                 |  | 0                                  |  | 0                                |  | 0                           |  | 0                                |  | 0                                |  | 0                           |  | 0                                |  | 0                                |  | 0                           |  | 0                                |  | 0                                |  | 0                           |  | Reset                            |  |
| HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_EN |  | HP_SYS_CLKRST_TIMERGRPO_WDT_CLK_EN |  | HP_SYS_CLKRST_TIMERGRPO_WDT_CLK_EN |  | HP_SYS_CLKRST_TIMERGRPO_WDT_SRC_SEL |  | HP_SYS_CLKRST_TIMERGRPO_T1_CLK_EN |  | HP_SYS_CLKRST_TIMERGRPO_T1_SRC_SEL |  | HP_SYS_CLKRST_TIMERGRPO_TO_CLK_EN |  | HP_SYS_CLKRST_TIMERGRPO_TO_SRC_SEL |  | HP_SYS_CLKRST_MCPWM1_CLK_DIV_NUM |  | HP_SYS_CLKRST_MCPWM1_CLK_EN |  | HP_SYS_CLKRST_MCPWM1_CLK_SRC_SEL |  | HP_SYS_CLKRST_MCPWM0_CLK_DIV_NUM |  | HP_SYS_CLKRST_MCPWM0_CLK_EN |  | HP_SYS_CLKRST_MCPWM0_CLK_SRC_SEL |  | HP_SYS_CLKRST_MCPWM0_CLK_DIV_NUM |  | HP_SYS_CLKRST_MCPWM0_CLK_EN |  | HP_SYS_CLKRST_MCPWM0_CLK_SRC_SEL |  | HP_SYS_CLKRST_MCPWM0_CLK_DIV_NUM |  | HP_SYS_CLKRST_MCPWM0_CLK_EN |  | HP_SYS_CLKRST_MCPWM0_CLK_SRC_SEL |  |

**HP\_SYS\_CLKRST\_MCPWMO\_CLK\_SRC\_SEL** Configures the clock source for MCPWMO\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F160\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_MCPWMO\_CLK\_EN** Configures whether to enable MCPWMO\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MCPWMO\_CLK\_DIV\_NUM** Configures the clock divisor of MCPWMO\_CLK. (R/W)

**HP\_SYS\_CLKRST\_MCPWM1\_CLK\_SRC\_SEL** Configures the clock source for MCPWM1\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F160\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_MCPWM1\_CLK\_EN** Configures whether to enable MCPWM1\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_MCPWM1\_CLK\_DIV\_NUM** Configures the clock divisor of MCPWM1\_CLK. (R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_TO\_SRC\_SEL** Configures the clock source for TIMER-GRPO TO CLK.

0: XTAL CLK

1: RC FAST CLK

2: PLL F80M CLK

3: Invalid

(R/W)

**Register 9.38. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL20\_REG (0x0094)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_TIMERGRPO\_TO\_CLK\_EN** Configures whether to enable TIMERGRPO\_TO\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_T1\_SRC\_SEL** Configures the clock source for TIMERGRPO\_T1\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_T1\_CLK\_EN** Configures whether to enable TIMERGRPO\_T1\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_WDT\_SRC\_SEL** Configures the clock source for TIMERGRPO\_WDT\_CLK.

0: XTAL\_CLK

1: RC\_FAST\_CLK

2: PLL\_F80M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_WDT\_CLK\_EN** Configures whether to enable TIMERGRPO\_WDT\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_TGRT\_CLK\_EN** Configures whether to enable TIMERGRPO\_TGRT\_CLK.

0: Disable

1: Enable

(R/W)

**Register 9.39. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL21\_REG (0x0098)**

|                   |    |    |    |    |    |    |    |    |    |   |    |    |   |  |  |  |  |  |  |   |   |  |  |  |  |  |  |  |  |
|-------------------|----|----|----|----|----|----|----|----|----|---|----|----|---|--|--|--|--|--|--|---|---|--|--|--|--|--|--|--|--|
| <i>(reserved)</i> |    |    |    |    |    |    |    |    |    | <i>HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_DIV_NUM</i> |    |    |   |  |  |  |  |  |  | <i>HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_SRC_SEL</i> |   |  |  |  |  |  |  |  |  |
| 31                | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21  | 20 | 19 |   |  |  |  |  |  |  | 4   | 3 |  |  |  |  |  |  |  |  |
| 0                 | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0   |    |    | 0 |  |  |  |  |  |  |   | 0 |  |  |  |  |  |  |  |  |

Reset

**HP\_SYS\_CLKRST\_TIMERGRPO\_TGRT\_CLK\_SRC\_SEL** Configures the clock source for TIMER-GRPO\_TGRT\_CLK.

- 0: MPLL\_CLK (500 MHz)
  - 1: SPLL\_CLK (480 MHz)
  - 2: CPLL\_CLK (360 MHz)
  - 3: APLL\_CLK
  - 4: SDIO\_PLLO\_CLK
  - 5: SDIO\_PLL1\_CLK
  - 6: SDIO\_PLL2\_CLK
  - 7: RC\_FAST\_CLK
  - 8: RC\_SLOW\_CLK
  - 9: Invalid
  - 10: XTAL32K\_CLK
  - 11: PLL\_LP\_CLK
  - 12-15: Clock tie 0
- (R/W)

**HP\_SYS\_CLKRST\_TIMERGRPO\_TGRT\_CLK\_DIV\_NUM** Configures the clock divisor of TIMER-GRPO\_TGRT\_CLK. (R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_TO\_SRC\_SEL** Configures the clock source for TIMERGRP1\_TO\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F80M\_CLK
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_TO\_CLK\_EN** Configures whether to enable TIMERGRP1\_TO\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

Continued on the next page...

**Register 9.39. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL21\_REG (0x0098)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_TIMERGRP1\_T1\_SRC\_SEL** Configures the clock source for TIMERGRP1\_T1\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F80M\_CLK
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_T1\_CLK\_EN** Configures whether to enable TIMERGRP1\_T1\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_WDT\_SRC\_SEL** Configures the clock source for TIMERGRP1\_WDT\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F80M\_CLK
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_TIMERGRP1\_WDT\_CLK\_EN** Configures whether to enable TIMERGRP1\_WDT\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_SYSTIMER\_CLK\_SRC\_SEL** Configures the clock source for SYSTIMER\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
- (R/W)

**HP\_SYS\_CLKRST\_SYSTIMER\_CLK\_EN** Configures whether to enable SYSTIMER\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

Register 9.40. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL22\_REG (0x009C)

|                               |    |    |    |                                       |    |    |    |                                     |    |    |    |                               |    |    |    |                          |    |    |    |                               |    |   |   |                           |   |   |   |                                |   |   |   |
|-------------------------------|----|----|----|---------------------------------------|----|----|----|-------------------------------------|----|----|----|-------------------------------|----|----|----|--------------------------|----|----|----|-------------------------------|----|---|---|---------------------------|---|---|---|--------------------------------|---|---|---|
| HP_SYS_CLKRST_ADC_CLK_SRC_SEL |    |    |    | HP_SYS_CLKRST_RMT_CLK_DIV_DENOMINATOR |    |    |    | HP_SYS_CLKRST_RMT_CLK_DIV_NUMERATOR |    |    |    | HP_SYS_CLKRST_RMT_CLK_DIV_NUM |    |    |    | HP_SYS_CLKRST_RMT_CLK_EN |    |    |    | HP_SYS_CLKRST_RMT_CLK_SRC_SEL |    |   |   | HP_SYS_CLKRST_LEDC_CLK_EN |   |   |   | HP_SYS_CLKRST_LEDC_CLK_SRC_SEL |   |   |   |
| 31                            | 30 | 29 | 28 | 27                                    | 26 | 25 | 24 | 23                                  | 22 | 21 | 20 | 19                            | 18 | 17 | 16 | 15                       | 14 | 13 | 12 | 11                            | 10 | 9 | 8 | 7                         | 6 | 5 | 4 | 3                              | 2 | 1 | 0 |
| 0                             | 0  | 0  | 0  | 0                                     | 0  | 0  | 0  | 0                                   | 0  | 0  | 0  | 0                             | 0  | 0  | 0  | 0                        | 0  | 0  | 0  | 0                             | 0  | 0 | 0 | 0                         | 0 | 0 | 0 | 0                              | 0 | 0 | 0 |

Reset

**HP\_SYS\_CLKRST\_LEDC\_CLK\_SRC\_SEL** Configures the clock source for LEDC\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F80M\_CLK
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_LEDC\_CLK\_EN** Configures whether to enable LEDC\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_RMT\_CLK\_SRC\_SEL** Configures the clock source for RMT\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F80M\_CLK
  - 3: Invalid
- (R/W)

**HP\_SYS\_CLKRST\_RMT\_CLK\_EN** Configures whether to enable RMT\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_RMT\_CLK\_DIV\_NUM** Configures the integer part of the RMT\_CLK clock divisor.  
(R/W)**HP\_SYS\_CLKRST\_RMT\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor's fractional part for RMT\_CLK. (R/W)**HP\_SYS\_CLKRST\_RMT\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor's fractional part for RMT\_CLK. (R/W)

Continued on the next page...



Register 9.40. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL22\_REG (0x009C)

Continued from the previous page...

**HP\_SYS\_CLKRST\_ADC\_CLK\_SRC\_SEL** Configures the clock source for HPADC\_CLK.

- 0: XTAL\_CLK
- 1: RC\_FAST\_CLK
- 2: PLL\_F80M\_CLK
- 3: Invalid

(R/W)

Register 9.41. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL23\_REG (0x00A0)

|            |  |  |  |  |  |  |  |                                       |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|---------------------------------------|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  | HP_SYS_CLKRST_ADC_CLK_DIV_DENOMINATOR |  |  |  |  |  |  |  | HP_SYS_CLKRST_ADC_CLK_DIV_NUMERATOR |  |  |  |  |  |  |  | HP_SYS_CLKRST_ADC_CLK_DIV_NUM |  |  |  |  |  |  |  | HP_SYS_CLKRST_ADC_CLK_EN |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  | 25                                    |  |  |  |  |  |  |  | 24                                  |  |  |  |  |  |  |  | 17                            |  |  |  |  |  |  |  | 16                       |  |  |  |  |  |  |  | 9 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  | 0                                     |  |  |  |  |  |  |  | 0                                   |  |  |  |  |  |  |  | 0                             |  |  |  |  |  |  |  | 0                        |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_ADC\_CLK\_EN** Configures whether to enable HPADC\_CLK.

- 0: Disable
- 1: Enable

(R/W)

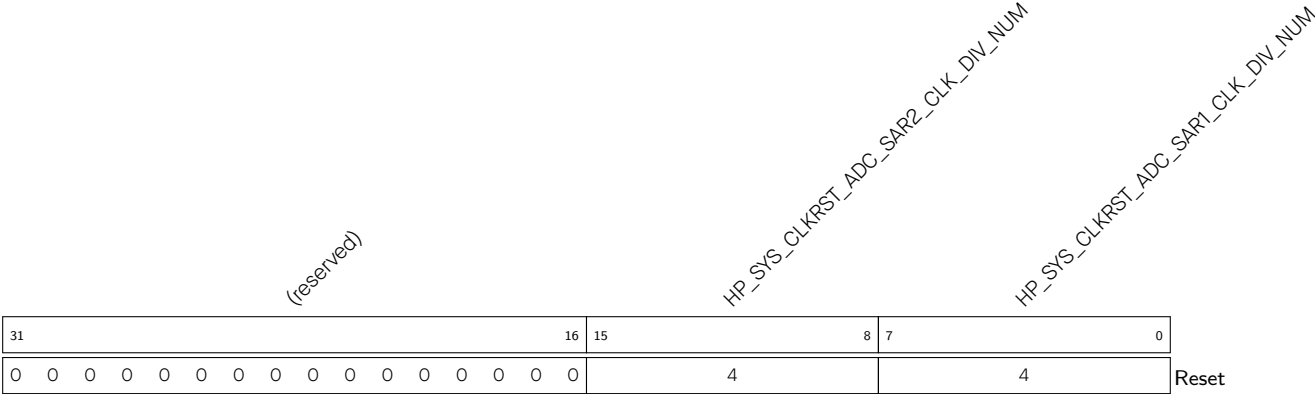
**HP\_SYS\_CLKRST\_ADC\_CLK\_DIV\_NUM** Configures the integer part of the HPADC\_CLK clock divisor.

(R/W)

**HP\_SYS\_CLKRST\_ADC\_CLK\_DIV\_NUMERATOR** Configures the numerator of the divisor’s fractional part for HPADC\_CLK. (R/W)

**HP\_SYS\_CLKRST\_ADC\_CLK\_DIV\_DENOMINATOR** Configures the denominator of the divisor’s fractional part for HPADC\_CLK. (R/W)

Register 9.42. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL24\_REG (0x00A4)



**HP\_SYS\_CLKRST\_ADC\_SAR1\_CLK\_DIV\_NUM**   Configures the integer part of the clock divisor for ADC\_SAR1\_CLK. (R/W)

**HP\_SYS\_CLKRST\_ADC\_SAR2\_CLK\_DIV\_NUM**   Configures the integer part of the clock divisor for ADC\_SAR2\_CLK. (R/W)

**Register 9.43. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL25\_REG (0x00A8)**

|            |    |   |   |   |   |                          |    |                               |    |            |    |                                   |    |                                 |    |                                 |    |                                 |    |                                  |   |                                 |   |                                 |   |                                 |   |            |   |       |
|------------|----|---|---|---|---|--------------------------|----|-------------------------------|----|------------|----|-----------------------------------|----|---------------------------------|----|---------------------------------|----|---------------------------------|----|----------------------------------|---|---------------------------------|---|---------------------------------|---|---------------------------------|---|------------|---|-------|
| (reserved) |    |   |   |   |   | HP_SYS_CLKRST_ISP_CLK_EN |    | HP_SYS_CLKRST_ISP_CLK_SRC_SEL |    | (reserved) |    | HP_SYS_CLKRST_CRYPTO_ECDSA_CLK_EN |    | HP_SYS_CLKRST_CRYPTO_SHA_CLK_EN |    | HP_SYS_CLKRST_CRYPTO_SEC_CLK_EN |    | HP_SYS_CLKRST_CRYPTO_RSA_CLK_EN |    | HP_SYS_CLKRST_CRYPTO_HMAC_CLK_EN |   | HP_SYS_CLKRST_CRYPTO_ECC_CLK_EN |   | HP_SYS_CLKRST_CRYPTO_DSA_CLK_EN |   | HP_SYS_CLKRST_CRYPTO_AES_CLK_EN |   | (reserved) |   |       |
| 31         | 26 |   |   |   |   | 25                       | 24 | 23                            | 22 | 21         | 20 | 19                                | 18 | 17                              | 16 | 15                              | 14 | 13                              | 12 | 11                               | 0 |                                 |   |                                 |   |                                 |   |            |   |       |
| 0          | 0  | 0 | 0 | 0 | 0 | 0                        | 0  | 1                             | 1  | 1          | 1  | 1                                 | 1  | 1                               | 1  | 1                               | 1  | 0                               | 0  | 0                                | 0 | 0                               | 0 | 0                               | 0 | 0                               | 0 | 0          | 0 | Reset |

**HP\_SYS\_CLKRST\_CRYPTO\_CLK\_SRC\_SEL** Configures the clock source for CRYPTO\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_F240M\_CLK
  - 3: PLL\_F160M\_CLK
- (R/W)

**HP\_SYS\_CLKRST\_CRYPTO\_AES\_CLK\_EN** Configures whether to enable AES\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_CRYPTO\_DSA\_CLK\_EN** Configures whether to enable DSA\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_CRYPTO\_ECC\_CLK\_EN** Configures whether to enable ECC\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_CRYPTO\_HMAC\_CLK\_EN** Configures whether to enable HMAC\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**HP\_SYS\_CLKRST\_CRYPTO\_RSA\_CLK\_EN** Configures whether to enable RSA\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

Continued on the next page...

**Register 9.43. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL25\_REG (0x00A8)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_CRYPT0\_SEC\_CLK\_EN** Configures whether to enable SEC\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_CRYPT0\_SHA\_CLK\_EN** Configures whether to enable SHA\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_CRYPT0\_ECDSA\_CLK\_EN** Configures whether to enable ECDSA\_CLK.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_ISP\_CLK\_SRC\_SEL** Configures the clock source for ISP\_CLK.

0: XTAL\_CLK

1: PLL\_F240M\_CLK

2: PLL\_F160M\_CLK

3: Invalid

(R/W)

**HP\_SYS\_CLKRST\_ISP\_CLK\_EN** Configures whether to enable ISP\_CLK.

0: Disable

1: Enable

(R/W)

Register 9.44. HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL26\_REG (0x00AC)

|            |    |    |   |                                |    |    |    |                           |    |   |   |                                |   |   |   |                                 |   |   |   |                            |   |   |   |                                 |   |   |   |                               |   |   |   |
|------------|----|----|---|--------------------------------|----|----|----|---------------------------|----|---|---|--------------------------------|---|---|---|---------------------------------|---|---|---|----------------------------|---|---|---|---------------------------------|---|---|---|-------------------------------|---|---|---|
| (reserved) |    |    |   | HP_SYS_CLKRST_H264_CLK_DIV_NUM |    |    |    | HP_SYS_CLKRST_H264_CLK_EN |    |   |   | HP_SYS_CLKRST_H264_CLK_SRC_SEL |   |   |   | HP_SYS_CLKRST_IOMUX_CLK_DIV_NUM |   |   |   | HP_SYS_CLKRST_IOMUX_CLK_EN |   |   |   | HP_SYS_CLKRST_IOMUX_CLK_SRC_SEL |   |   |   | HP_SYS_CLKRST_ISP_CLK_DIV_NUM |   |   |   |
| 31         | 28 | 27 |   | 20                             | 19 | 18 | 17 |                           | 10 | 9 | 8 | 7                              |   |   |   |                                 |   |   |   |                            |   |   |   |                                 |   |   |   |                               |   |   |   |
| 0          | 0  | 0  | 0 | 0                              | 0  | 0  | 0  | 0                         | 0  | 1 | 0 | 0                              | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0                             | 0 | 0 | 0 |

Reset

**HP\_SYS\_CLKRST\_ISP\_CLK\_DIV\_NUM** Configures the clock divisor of ISP\_CLK. (R/W)

**HP\_SYS\_CLKRST\_IOMUX\_CLK\_SRC\_SEL** Configures the clock source for IOMUX\_CLK.

0: XTAL\_CLK

1: PLL\_F80M\_CLK

(R/W)

**HP\_SYS\_CLKRST\_IOMUX\_CLK\_EN** Configures whether to enable the IOMUX\_CLK clock.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_IOMUX\_CLK\_DIV\_NUM** Configures the clock divisor of IOMUX\_CLK. (R/W)

**HP\_SYS\_CLKRST\_H264\_CLK\_SRC\_SEL** Configures the clock source for H264\_CLK.

0: XTAL\_CLK

1: PLL\_F240M\_CLK

(R/W)

**HP\_SYS\_CLKRST\_H264\_CLK\_EN** Configures whether to enable the H264\_CLK clock.

0: Disable

1: Enable

(R/W)

**HP\_SYS\_CLKRST\_H264\_CLK\_DIV\_NUM** Configures the clock divisor of H264\_CLK. (R/W)

Register 9.45. HP\_SYS\_CLKRST\_CLK\_FORCE\_ON\_CTRL0\_REG (0x00B4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|---|---|---|---|---|---|-------|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_GMAC_TX_CLK_FORCE_ON<br>HP_SYS_CLKRST_SAR2_CLK_FORCE_ON<br>HP_SYS_CLKRST_SAR1_CLK_FORCE_ON<br>HP_SYS_CLKRST_L2MEM_MEM_CLK_FORCE_ON<br>HP_SYS_CLKRST_L2CACHE_MEM_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_I1_MEM_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_I0_MEM_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_D_MEM_CLK_FORCE_ON<br>HP_SYS_CLKRST_TRACE_SYS_CLK_FORCE_ON<br>HP_SYS_CLKRST_TRACE_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_I1_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_I0_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_L1CACHE_D_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_BUSMON_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_SPM_CPU_CLK_FORCE_ON<br>HP_SYS_CLKRST_CPUICM_GATED_CLK_FORCE_ON |    |    |    |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 18   | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | Reset |   |   |   |  |

**HP\_SYS\_CLKRST\_CPUICM\_GATED\_CLK\_FORCE\_ON** Configures the CPUICM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_SPM\_CPU\_CLK\_FORCE\_ON** Configures the SPM\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_BUSMON\_CPU\_CLK\_FORCE\_ON** Configures the BUSMON\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_CPU\_CLK\_FORCE\_ON** Configures the L1CACHE\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_D\_CPU\_CLK\_FORCE\_ON** Configures the L1DCACHE\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

Continued on the next page...

**Register 9.45. HP\_SYS\_CLKRST\_CLK\_FORCE\_ON\_CTRL0\_REG (0x00B4)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_L1CACHE\_IO\_CPU\_CLK\_FORCE\_ON** Configures the L1I0CACHE\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_I1\_CPU\_CLK\_FORCE\_ON** Configures the L1I1CACHE\_CPU\_CLK clock gating path.

(R/W)

**HP\_SYS\_CLKRST\_TRACE\_CPU\_CLK\_FORCE\_ON** Configures the TRACE\_CPU\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_TRACE\_SYS\_CLK\_FORCE\_ON** Configures the TRACE\_SYS\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_MEM\_CLK\_FORCE\_ON** Configures the L1CACHE\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_D\_MEM\_CLK\_FORCE\_ON** Configures the L1DCACHE\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_IO\_MEM\_CLK\_FORCE\_ON** Configures the L1I0CACHE\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L1CACHE\_I1\_MEM\_CLK\_FORCE\_ON** Configures the L1I1CACHE\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

Continued on the next page...

**Register 9.45. HP\_SYS\_CLKRST\_CLK\_FORCE\_ON\_CTRL0\_REG (0x00B4)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_L2CACHE\_MEM\_CLK\_FORCE\_ON** Configures the L2CACHE\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_L2MEM\_MEM\_CLK\_FORCE\_ON** Configures the L2MEM\_MEM\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_SAR1\_CLK\_FORCE\_ON** Configures the SAR1\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_SAR2\_CLK\_FORCE\_ON** Configures the SAR2\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)

**HP\_SYS\_CLKRST\_GMAC\_TX\_CLK\_FORCE\_ON** Configures the GMAC\_TX\_CLK clock gating path.

0: Clock gating is enabled

1: Force on the clock, bypassing the clock gating

(R/W)



### Register 9.46. HP\_SYS\_CLKRST\_DPA\_CTRL0\_REG (0x00B8)

[illegible]

**HP\_SYS\_CLKRST\_SEC\_DPA\_LEVEL** Configures the security level of CRYPTO\_CLK against DPA attacks.

0: Low security level

1: High security level

(R/W)

**HP\_SYS\_CLKRST\_SEC\_DPA\_CFG\_SEL** Configures the source of the security level of CRYPTO\_CLK against DPA attacks.

0: The security level is determined by EFUSE\_SEC\_DPA\_LEVEL

1: The security level is determined by HP\_SYS\_CLKRST\_SEC\_DPA\_LEVEL

(R/W)

Register 9.47. HP\_SYS\_CLKRST\_ANA\_PLL\_CTRL0\_REG (0x00BC)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_MSPI_CAL_STOP<br>HP_SYS_CLKRST_MSPI_CAL_END<br>HP_SYS_CLKRST_SYS_PLL_CAL_STOP<br>HP_SYS_CLKRST_SYS_PLL_CAL_END<br>HP_SYS_CLKRST_SDIO_PLL_CAL_STOP<br>HP_SYS_CLKRST_SDIO_PLL_CAL_END<br>HP_SYS_CLKRST_CPU_PLL_CAL_STOP<br>HP_SYS_CLKRST_CPU_PLL_CAL_END<br>HP_SYS_CLKRST_PLLA_CAL_STOP<br>HP_SYS_CLKRST_PLLA_CAL_END |   |       |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10  | 9 | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | Reset |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |

**HP\_SYS\_CLKRST\_PLLA\_CAL\_END** Represents whether the APLL\_CLK calibration is finished.

0: Calibration in progress

1: Calibration done

(RO)

**HP\_SYS\_CLKRST\_PLLA\_CAL\_STOP** Configures whether to start or stop the APLL\_CLK calibration.

0: Start calibration

1: Stop calibration

(R/W)

**HP\_SYS\_CLKRST\_CPU\_PLL\_CAL\_END** Represents whether the CPLL\_CLK calibration is finished.

0: Calibration in progress

1: Calibration done

(RO)

**HP\_SYS\_CLKRST\_CPU\_PLL\_CAL\_STOP** Configures whether to start or stop the CPLL\_CLK calibration.

0: Start calibration

1: Stop calibration

(R/W)

**HP\_SYS\_CLKRST\_SDIO\_PLL\_CAL\_END** Represents whether the SDIO\_PLL calibration is finished.

0: Calibration in progress

1: Calibration done

(RO)

**HP\_SYS\_CLKRST\_SDIO\_PLL\_CAL\_STOP** Configures whether to start or stop the SDIO\_PLL calibration.

0: Start calibration

1: Stop calibration

(R/W)

Continued on the next page...

**Register 9.47. HP\_SYS\_CLKRST\_ANA\_PLL\_CTRL0\_REG (0x00BC)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_SYS\_PLL\_CAL\_END** Represents whether the SPLL\_CLK calibration is finished.

0: Calibration in progress

1: Calibration done

(RO)

**HP\_SYS\_CLKRST\_SYS\_PLL\_CAL\_STOP** Configures whether to start or stop the SPLL\_CLK calibration.

0: Start calibration

1: Stop calibration

(R/W)

**HP\_SYS\_CLKRST\_MSPI\_CAL\_END** Represents whether the MPLL\_CLK calibration is finished.

0: Calibration in progress

1: Calibration done

(RO)

**HP\_SYS\_CLKRST\_MSPI\_CAL\_STOP** Configures whether to start or stop the MPLL\_CLK calibration.

0: Start calibration

1: Stop calibration

(R/W)

**Register 9.48. HP\_SYS\_CLKRST\_HP\_RST\_EN0\_REG (0x00C0)**

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |  |  |   |   |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|--|--|---|---|
| HP_SYS_CLKRST_RST_EN_DMA2D<br>HP_SYS_CLKRST_RST_EN_JPEG<br>(reserved)<br>HP_SYS_CLKRST_RST_EN_CSI_BRG<br>HP_SYS_CLKRST_RST_EN_CSI_HOST<br>HP_SYS_CLKRST_RST_EN_DSI_BRG<br>HP_SYS_CLKRST_RST_EN_DUAL_MSPI_APB<br>HP_SYS_CLKRST_RST_EN_DUAL_MSPI_AXI<br>(reserved)<br>HP_SYS_CLKRST_RST_EN_GDMA<br>HP_SYS_CLKRST_RST_EN_SPMON<br>HP_SYS_CLKRST_RST_EN_L2MEMMON<br>HP_SYS_CLKRST_RST_EN_L2_MEM<br>HP_SYS_CLKRST_RST_EN_L1_D_CACHE<br>HP_SYS_CLKRST_RST_EN_L1_I1_CACHE<br>HP_SYS_CLKRST_RST_EN_L1_IO_CACHE<br>HP_SYS_CLKRST_RST_EN_HP_CACHE<br>HP_SYS_CLKRST_RST_EN_HP_SPM<br>(reserved)<br>HP_SYS_CLKRST_RST_EN_CORETRACE1<br>HP_SYS_CLKRST_RST_EN_CORE1_GLOBAL<br>HP_SYS_CLKRST_RST_EN_CORE0_GLOBAL<br>HP_SYS_CLKRST_RST_EN_CORECTRL |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |  |  |   |   |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 |   |   |   |   |   |   |   |       |  |  | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |  |   |   |

**HP\_SYS\_CLKRST\_RST\_EN\_CORECTRL** Configures whether to reset CORECTRL.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CORE0\_GLOBAL** Configures whether to reset HP CPU0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CORE1\_GLOBAL** Configures whether to reset HP CPU1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CORETRACE0** Configures whether to reset RISC-V Trace Encoder0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CORETRACE1** Configures whether to reset RISC-V Trace Encoder1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_HP\_SPM** Configures whether to reset SPM.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.48. HP\_SYS\_CLKRST\_HP\_RST\_ENO\_REG (0x00C0)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_HP\_CACHE** Configures whether to reset L1 I-Cache0, L1 I-Cache1, L1 D-Cache, L2 Cache.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L1\_IO\_CACHE** Configures whether to reset L1 I-Cache0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L1\_I1\_CACHE** Configures whether to reset L1 I-Cache1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L1\_D\_CACHE** Configures whether to reset L1 D-Cache.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L2\_CACHE** Configures whether to reset L2 Cache.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L2\_MEM** Configures whether to reset L2 MEM.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_L2MEMMON** Configures whether to reset L2 MEM monitor.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_SPMON** Configures whether to reset SPM monitor.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_GDMA** Configures whether to reset VDMA.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.48. HP\_SYS\_CLKRST\_HP\_RST\_ENO\_REG (0x00C0)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_MSPI\_AXI** Configures whether to reset FLASH MSPI AXI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_DUAL\_MSPI\_AXI** Configures whether to reset PSRAM MSPI AXI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_MSPI\_APB** Configures whether to reset FLASH MSPI APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_DUAL\_MSPI\_APB** Configures whether to reset PSRAM MSPI APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_DSI\_BRG** Configures whether to reset DSI Bridge.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CSI\_HOST** Configures whether to reset CSI Host.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CSI\_BRG** Configures whether to reset CSI Bridge and ISP.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_JPEG** Configures whether to reset JPEG.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_DMA2D** Configures whether to reset 2DDMA.

0: Release from reset

1: Reset

(R/W)

Register 9.49. HP\_SYS\_CLKRST\_HP\_RST\_EN1\_REG (0x00C4)

|                          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--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| HP_SYS_CLKRST_RST_EN_ETM |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_PONT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_LEDC |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_CAN2 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_CAN1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_CAN0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_PWM1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_PWM0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_RMT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_I2C0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_I2C1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_I3CSLV |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UHCI |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART4_APB |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART3_APB |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART2_APB |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART1_APB |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART0_APB |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART3_CORE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART2_CORE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART1_CORE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_UART0_CORE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_TIMERGRP1 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_TIMERGRP0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_IOMUX |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_AXI_PDMA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_AHB_PDMA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HP_SYS_CLKRST_RST_EN_PPA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31                       | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |   |   |   |   |   |   |   |   |   |   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  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                        | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**HP\_SYS\_CLKRST\_RST\_EN\_PPA** Configures whether to reset PPA.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_AHB\_PDMA** Configures whether to reset GDMA-AHB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_AXI\_PDMA** Configures whether to reset GDMA-AXI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_IOMUX** Configures whether to reset IO MUX.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_STIMER** Configures whether to reset the System Timer.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_TIMERGRP0** Configures whether to reset Timer Group 0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_TIMERGRP1** Configures whether to reset Timer Group 1.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.49. HP\_SYS\_CLKRST\_HP\_RST\_EN1\_REG (0x00C4)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_UART0\_CORE** Configures whether to reset UART0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART1\_CORE** Configures whether to reset UART1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART2\_CORE** Configures whether to reset UART2.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART3\_CORE** Configures whether to reset UART3.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART4\_CORE** Configures whether to reset UART4.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART0\_APB** Configures whether to reset UART0 APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART1\_APB** Configures whether to reset UART1 APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART2\_APB** Configures whether to reset UART2 APB.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...



**Register 9.49. HP\_SYS\_CLKRST\_HP\_RST\_EN1\_REG (0x00C4)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_UART3\_APB** Configures whether to reset UART3 APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UART4\_APB** Configures whether to reset UART4 APB.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_UHCI** Configures whether to reset UHCI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I3CMST** Configures whether to reset I3C Master.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I3CSLV** Configures whether to reset I3C Slave.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I2C1** Configures whether to reset I2C1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I2C0** Configures whether to reset I2C0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_RMT** Configures whether to reset RMT.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_PWM0** Configures whether to reset MCPMW0.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.49. HP\_SYS\_CLKRST\_HP\_RST\_EN1\_REG (0x00C4)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_PWM1** Configures whether to reset MCPWM1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CAN0** Configures whether to reset TWAIO.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CAN1** Configures whether to reset TWAI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CAN2** Configures whether to reset TWAI.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_LEDC** Configures whether to reset LEDC.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_PCNT** Configures whether to reset PCNT.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_ETM** Configures whether to reset ETM.

0: Release from reset

1: Reset

(R/W)

**Register 9.50. HP\_SYS\_CLKRST\_HP\_RST\_EN2\_REG (0x00C8)**

[illegible]

**HP\_SYS\_CLKRST\_RST\_EN\_INTRMTX** Configures whether to reset the Interrupt Matrix.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_PARLIO** Configures whether to reset PARLIO.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_PARLIO\_RX** Configures whether to reset PARLIO RX.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_PARLIO\_TX** Configures whether to reset PARLIO TX.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I2S0\_APB** Configures whether to reset I2S0.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I2S1\_APB** Configures whether to reset I2S1.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_I2S2\_APB** Configures whether to reset I2S2.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.50. HP\_SYS\_CLKRST\_HP\_RST\_EN2\_REG (0x00C8)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_SPI2** Configures whether to reset SPI2.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_SPI3** Configures whether to reset SPI3.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_LCDCAM** Configures whether to reset the LCD\_CAM.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_ADC** Configures whether to reset ADC.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_BITSRAMBLER** Configures whether to reset the Bit Scrambler.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_BITSRAMBLER\_RX** Configures whether to reset the Bit Scrambler RX.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_BITSRAMBLER\_TX** Configures whether to reset the Bit Scrambler TX.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_CRYPT** Configures whether to reset the crypto modules.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_SEC** Configures whether to reset SEC.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.50. HP\_SYS\_CLKRST\_HP\_RST\_EN2\_REG (0x00C8)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_RST\_EN\_AES** Configures whether to reset AES.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_DS** Configures whether to reset DS.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_SHA** Configures whether to reset SHA.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_HMAC** Configures whether to reset HMAC.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_ECDSA** Configures whether to reset ECDSA.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_RSA** Configures whether to reset RSA.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_ECC** Configures whether to reset ECC.

0: Release from reset

1: Reset

(R/W)

**HP\_SYS\_CLKRST\_RST\_EN\_H264** Configures whether to reset H264.

0: Release from reset

1: Reset

(R/W)

Register 9.51. HP\_SYS\_CLKRST\_HP\_FORCE\_NORSTO\_REG (0x00CC)

|                                  |                                |                                 |                                 |                                 |                                 |            |                                     |                                     |                                  |                                 |                                    |            |                               |                                 |                                |                                   |                                    |                                   |   |   |                                |                                 |                                    |                                      |                                 |       |   |   |   |   |   |
|----------------------------------|--------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|------------|-------------------------------------|-------------------------------------|----------------------------------|---------------------------------|------------------------------------|------------|-------------------------------|---------------------------------|--------------------------------|-----------------------------------|------------------------------------|-----------------------------------|---|---|--------------------------------|---------------------------------|------------------------------------|--------------------------------------|---------------------------------|-------|---|---|---|---|---|
| HP_SYS_CLKRST_FORCE_NORST_I3CMST | HP_SYS_CLKRST_FORCE_NORST_UHCI | HP_SYS_CLKRST_FORCE_NORST_UART4 | HP_SYS_CLKRST_FORCE_NORST_UART3 | HP_SYS_CLKRST_FORCE_NORST_UART2 | HP_SYS_CLKRST_FORCE_NORST_UART1 | (reserved) | HP_SYS_CLKRST_FORCE_NORST_TIMERGRP1 | HP_SYS_CLKRST_FORCE_NORST_TIMERGRP0 | HP_SYS_CLKRST_FORCE_NORST_STIMER | HP_SYS_CLKRST_FORCE_NORST_IOMUX | HP_SYS_CLKRST_FORCE_NORST_AXI_PDMA | (reserved) | HP_SYS_CLKRST_FORCE_NORST_PPA | HP_SYS_CLKRST_FORCE_NORST_DMA2D | HP_SYS_CLKRST_FORCE_NORST_JPEG | HP_SYS_CLKRST_FORCE_NORST_CSI_BRG | HP_SYS_CLKRST_FORCE_NORST_CSI_HOST | HP_SYS_CLKRST_FORCE_NORST_DSI_BRG | HP_SYS_CLKRST_FORCE_NORST_DUAL_MSPI_APB | HP_SYS_CLKRST_FORCE_NORST_DUAL_MSPI_AXI | HP_SYS_CLKRST_FORCE_NORST_GDMA | HP_SYS_CLKRST_FORCE_NORST_SPMON | HP_SYS_CLKRST_FORCE_NORST_L2MEMMON | HP_SYS_CLKRST_FORCE_NORST_CORETRACE1 | HP_SYS_CLKRST_FORCE_NORST_CORE0 | Reset |   |   |   |   |   |
| 31                               | 30                             | 29                              | 28                              | 27                              | 26                              | 25         | 24                                  | 23                                  | 22                               | 21                              | 20                                 | 19         | 18                            | 17                              | 16                             | 15                                | 14                                 | 13                                | 12                                      | 11                                      | 10                             | 9                               | 8                                  | 7                                    | 6                               | 5     | 4 | 3 | 2 | 1 | 0 |
| 0                                | 0                              | 0                               | 0                               | 0                               | 0                               | 0          | 0                                   | 0                                   | 0                                | 0                               | 0                                  | 0          | 0                             | 0                               | 0                              | 0                                 | 0                                  | 0                                 | 0                                       | 0                                       | 0                              | 0                               | 0                                  | 0                                    | 0                               | 0     | 0 | 0 | 0 | 0 | 0 |

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CORE0** Configures whether HP CPU0 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CORE1** Configures whether HP CPU1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CORETRACE0** Configures whether RISC-V Trace Encoder 0 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CORETRACE1** Configures whether RISC-V Trace Encoder 1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_L2MEMMON** Configures whether L2 MEM monitor can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_SPMMON** Configures whether SPM monitor can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Continued on the next page...

**Register 9.51. HP\_SYS\_CLKRST\_HP\_FORCE\_NORSTO\_REG (0x00CC)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_GDMA** Configures whether VDMA can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_MSPI\_AXI** Configures whether FLASH MSPI can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_DUAL\_MSPI\_AXI** Configures whether PSRAM MSPI can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_MSPI\_APB** Configures whether FLASH MSPI APB can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_DUAL\_MSPI\_APB** Configures whether PSRAM MSPI APB can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_DSI\_BRG** Configures whether DSI Bridge can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CSI\_HOST** Configures whether CSI Host can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CSI\_BRG** Configures whether CSI Bridge, ISP can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Continued on the next page...

**Register 9.51. HP\_SYS\_CLKRST\_HP\_FORCE\_NORSTO\_REG (0x00CC)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_JPEG** Configures whether JPEG can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_DMA2D** Configures whether 2DDMA can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_PPA** Configures whether PPA can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_AHB\_PDMA** Configures whether GDMA-AHB can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_AXI\_PDMA** Configures whether GDMA-AXI can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_IOMUX** Configures whether IO MUX can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_STIMER** Configures whether the System Timer can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_TIMERGRP0** Configures whether Timer Group 0 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_TIMERGRP1** Configures whether Timer Group 1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Continued on the next page...



**Register 9.51. HP\_SYS\_CLKRST\_HP\_FORCE\_NORSTO\_REG (0x00CC)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UART0** Configures whether UART0 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UART1** Configures whether UART1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UART2** Configures whether UART2 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UART3** Configures whether UART3 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UART4** Configures whether UART4 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_UHCI** Configures whether UHCI can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_I3CMST** Configures whether I3C Master can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

(reserved)

HP\_SYS\_CLKRST\_FORCE\_NORST\_H264  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_BITSRAMBLER\_TX  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_BITSRAMBLER\_RX  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_ADC  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_L0DCAM  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_SPI3  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_SPI2  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S2  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S1  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S0  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO\_TX  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO\_RX  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_INTRMTX  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_ETM  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_P0CNT  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_LED0  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_CAN2  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_CAN1  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_CAN0  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_PWM1  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_PWM0  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I2C0  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I2C1  
 HP\_SYS\_CLKRST\_FORCE\_NORST\_I3CSLV

**Register 9.52. HP\_SYS\_CLKRST\_HP\_FORCE\_NORST1\_REG (0x00D0)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CAN1** Configures whether TWAI1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_CAN2** Configures whether TWAI2 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_LEDC** Configures whether LEDC can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_PCNT** Configures whether PCNT can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_ETM** Configures whether ETM can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_INTRMTX** Configures whether the interrupt matrix can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO** Configures whether PARLIO can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO\_RX** Configures whether PARLIO RX can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_PARLIO\_TX** Configures whether PARLIO TX can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Continued on the next page...

**Register 9.52. HP\_SYS\_CLKRST\_HP\_FORCE\_NORST1\_REG (0x00D0)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S0** Configures whether I2S0 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S1** Configures whether I2S1 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_I2S2** Configures whether I2S2 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_SPI2** Configures whether SPI2 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_SPI3** Configures whether SPI3 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_LCDCAM** Configures whether the LCD\_CAM can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_ADC** Configures whether ADC can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Continued on the next page...

**Register 9.52. HP\_SYS\_CLKRST\_HP\_FORCE\_NORST1\_REG (0x00D0)**

Continued from the previous page...

**HP\_SYS\_CLKRST\_FORCE\_NORST\_BITSRAMBLER** Configures whether the Bit Scrambler can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_BITSRAMBLER\_RX** Configures whether the Bit Scrambler RX can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**HP\_SYS\_CLKRST\_FORCE\_NORST\_BITSRAMBLER\_TX** Configures whether the Bit Scrambler TX can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

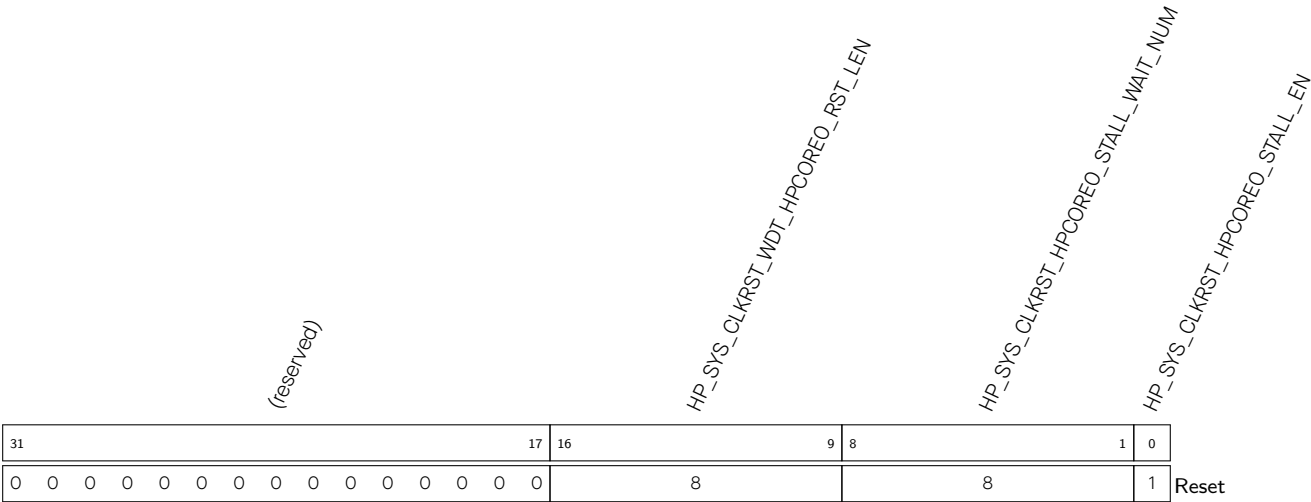
**HP\_SYS\_CLKRST\_FORCE\_NORST\_H264** Configures whether H264 can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

Register 9.53. HP\_SYS\_CLKRST\_HPWDT\_CORE0\_RST\_CTRL0\_REG (0x00D4)



**HP\_SYS\_CLKRST\_HPCORE0\_STALL\_EN**    Configures the behavior when MWDT triggers HP CPU0 reset.

0: Immediately reset HP CPU0

1: Stall HP CPU0 first

(R/W)

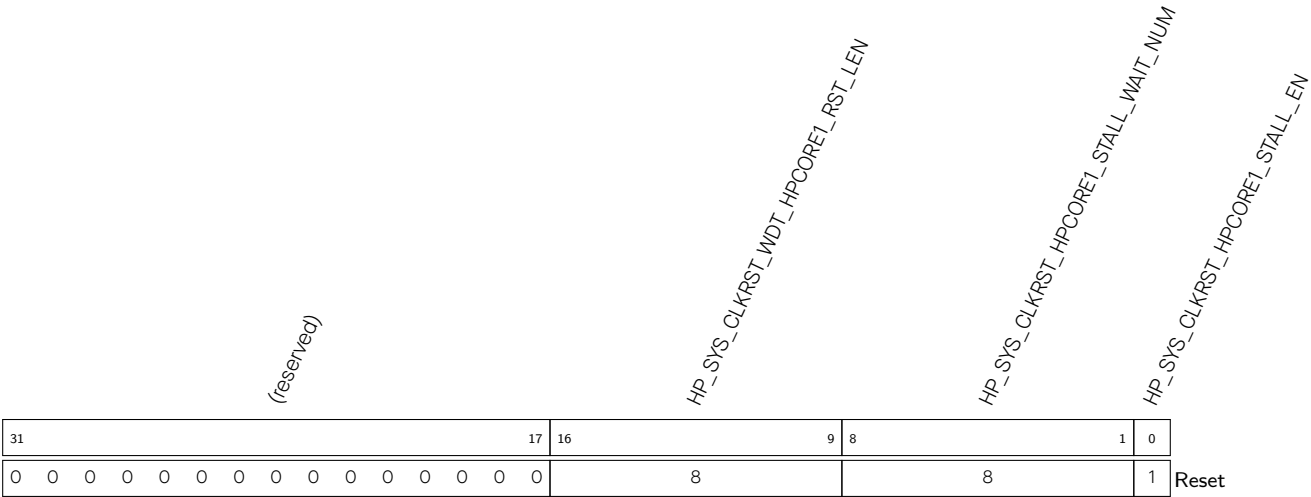
**HP\_SYS\_CLKRST\_HPCORE0\_STALL\_WAIT\_NUM**    Configures the duration of HP CPU0 stall when MWDT triggers HP CPU0 reset and HP\_SYS\_CLKRST\_HPCORE0\_STALL\_EN is set to 1.

Measurement unit: Clock cycles. (R/W)

**HP\_SYS\_CLKRST\_WDT\_HPCORE0\_RST\_LEN**    Configures the duration of the reset when MWDT triggers HP CPU0 reset.

Measurement unit: Clock cycles. (R/W)

Register 9.54. HP\_SYS\_CLKRST\_HPWDT\_CORE1\_RST\_CTRL0\_REG (0x00D8)



**HP\_SYS\_CLKRST\_HPCORE1\_STALL\_EN** Configures the behavior when MWDT triggers HP CPU1 reset.

- 0: Immediately reset HP CPU1
- 1: Stall HP CPU1 first

(R/W)

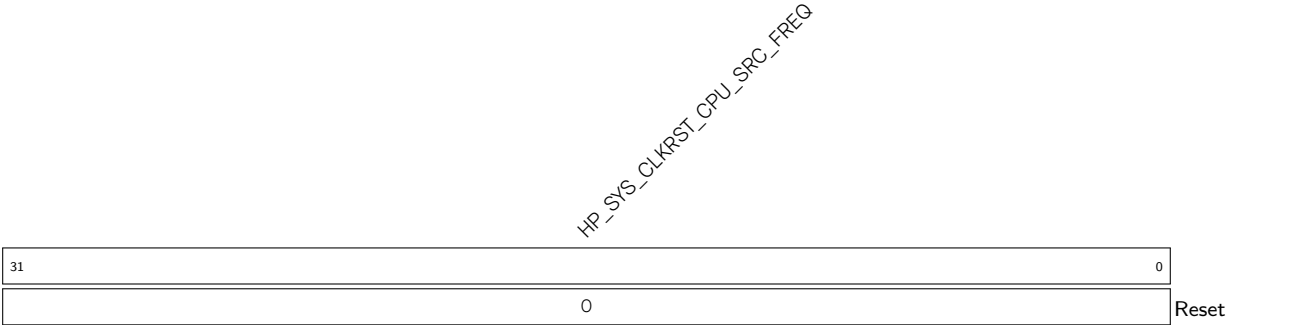
**HP\_SYS\_CLKRST\_HPCORE1\_STALL\_WAIT\_NUM** Configures the duration of HP CPU1 stall when MWDT triggers HP CPU1 reset and HP\_SYS\_CLKRST\_HPCORE1\_STALL\_EN is set to 1.

Measurement unit: Clock cycles. (R/W)

**HP\_SYS\_CLKRST\_WDT\_HPCORE1\_RST\_LEN** Configures the duration of the reset when MWDT triggers HP CPU1 reset.

Measurement unit: Clock cycles. (R/W)

Register 9.55. HP\_SYS\_CLKRST\_CPU\_SRC\_FREQ0\_REG (0x00DC)

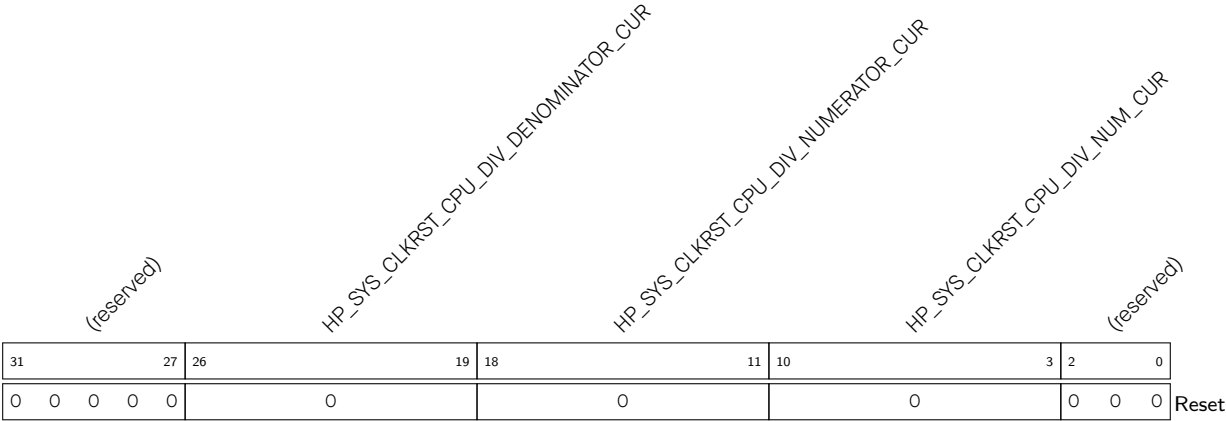


**HP\_SYS\_CLKRST\_CPU\_SRC\_FREQ** Represents the CPU source clock frequency.

- 80: RC\_FAST\_CLK
- 160: XTAL\_CLK
- 1600: CPLL\_CLK

(RO)

Register 9.56. HP\_SYS\_CLKRST\_CPU\_CLK\_STATUS0\_REG (0x00E0)



- HP\_SYS\_CLKRST\_CPU\_DIV\_NUM\_CUR

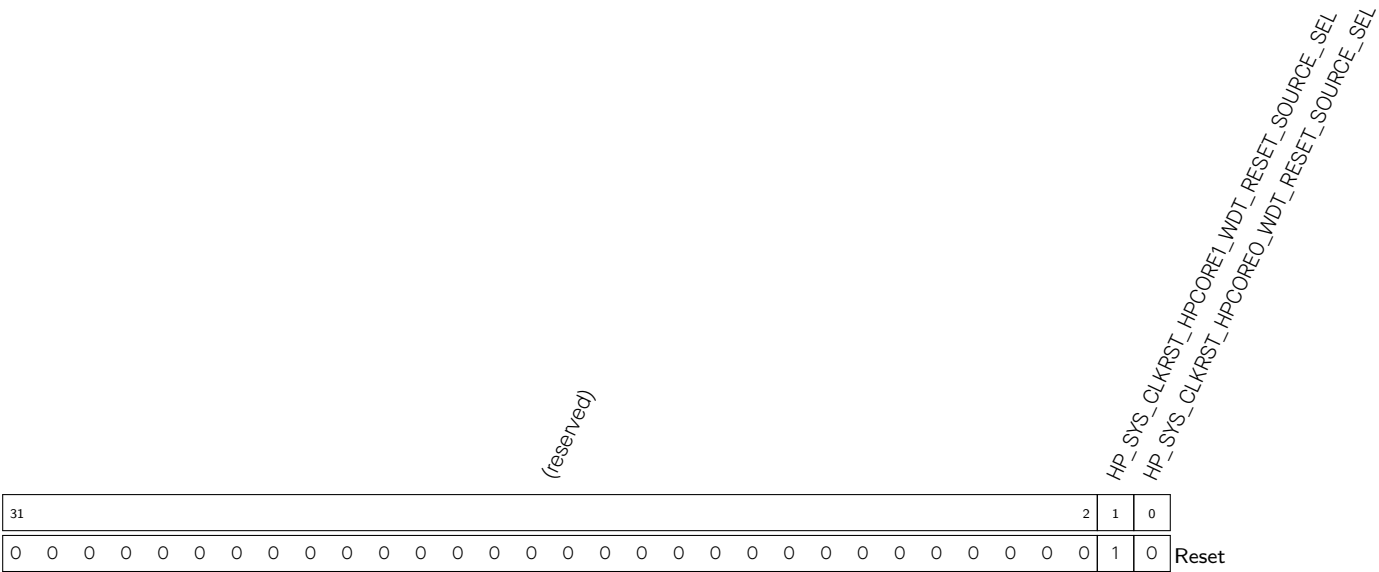
Represents the integer part of the current CPU\_CLK clock divisor. (RO)
- HP\_SYS\_CLKRST\_CPU\_DIV\_NUMERATOR\_CUR

Represents the current numerator of the divisor's fractional part for the CPU\_CLK. (RO)
- HP\_SYS\_CLKRST\_CPU\_DIV\_DENOMINATOR\_CUR

Represents the current denominator of the divisor's fractional part for the CPU\_CLK. (RO)



Register 9.57. HP\_SYS\_CLKRST\_HPCORE0\_WDT\_RESET\_SOURCE0\_REG (0x00EC)



**HP\_SYS\_CLKRST\_HPCORE0\_WDT\_RESET\_SOURCE\_SEL** Configures the MWDT used to trigger the HP CPU0 reset.  
0: MWDTO  
1: MWDT1  
(R/W)

**HP\_SYS\_CLKRST\_HPCORE1\_WDT\_RESET\_SOURCE\_SEL** Configures the MWDT used to trigger the HP CPU1 reset.  
0: MWDTO  
1: MWDT1  
(R/W)

9.5.2 LP Always on Clock and Reset (LP\_CLKRST) Registers

The addresses in this section are relative to LP\_CLKRST base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

Register 9.58. LP\_CLKRST\_LP\_CLK\_CONF\_REG (0x0000)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |                           |   |  |  |  |  |  |  |  |  |  |  |                        |   |  |  |  |  |  |  |  |  |  |  |                        |   |  |  |  |  |  |  |  |  |  |  |       |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|---------------------------|---|--|--|--|--|--|--|--|--|--|--|------------------------|---|--|--|--|--|--|--|--|--|--|--|------------------------|---|--|--|--|--|--|--|--|--|--|--|-------|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_ANA_SEL_REF_PLL8M |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_LP_PERI_DIV_NUM |   |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_FAST_CLK_SEL |   |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_SLOW_CLK_SEL |   |  |  |  |  |  |  |  |  |  |  |       |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11                          |  |  |  |  |  |  |  |  |  |  |  | 10                        | 9 |  |  |  |  |  |  |  |  |  |  |                        | 4 |  |  |  |  |  |  |  |  |  |  |                        | 3 |  |  |  |  |  |  |  |  |  |  |       | 2 |  |  |  |  |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                           |  |  |  |  |  |  |  |  |  |  |  | 0x0                       |   |  |  |  |  |  |  |  |  |  |  | 0x1                    |   |  |  |  |  |  |  |  |  |  |  | 0x0                    |   |  |  |  |  |  |  |  |  |  |  | Reset |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |

**LP\_CLKRST\_SLOW\_CLK\_SEL** Configures the clock source of LP\_SLOW\_CLK.

- 0: RC\_SLOW\_CLK
  - 1: XTAL32K\_CLK
  - 2: Invalid
  - 3: OSC\_SLOW\_CLK
- (R/W)

**LP\_CLKRST\_FAST\_CLK\_SEL** Configures the clock source of LP\_FAST\_CLK.

- 0: XTAL\_CLK
  - 1: RC\_FAST\_CLK
  - 2: PLL\_LP\_CLK
  - 3: Invalid
- (R/W)

**LP\_CLKRST\_LP\_PERI\_DIV\_NUM** Configures the clock divisor for LP\_PERI\_CLK. (R/W)

**LP\_CLKRST\_ANA\_SEL\_REF\_PLL8M** Configures the reference clock of PLL\_LP\_CLK.

- 0: Invalid
  - 1: XTAL32K\_CLK
- (R/W)

**Register 9.59. LP\_CLKRST\_LP\_CLK\_EN\_REG (0x0008)**

|                                |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--------------------------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| LP_CLKRST_FOSC_CLK_FORCE_ON    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| LP_CLKRST_XTAL_CLK_FORCE_ON    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| LP_CLKRST_PLL8M_CLK_FORCE_ON   |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| LP_CLKRST_ETM_EVENT_TICK_EN    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| LP_CLKRST_OK_EN_LP_RAM         |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| LP_CLKRST_LP_RTC_XTAL_FORCE_ON |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| (reserved)                     |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |       |
| 0                              | 0  | 0  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_CLKRST\_LP\_RTC\_XTAL\_FORCE\_ON** Configures whether to force on the XTAL\_CLK control of LP CALI.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

**LP\_CLKRST\_CK\_EN\_LP\_RAM** Configure whether to enable the clock of LP RAM.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_ETM\_EVENT\_TICK\_EN** Configures whether to enable the ETM event timer.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_PLL8M\_CLK\_FORCE\_ON** Configures whether to force on PLL\_LP\_CLK as LP\_FAST\_CLK source.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

**LP\_CLKRST\_XTAL\_CLK\_FORCE\_ON** Configures whether to force on XTAL\_CLK as LP\_FAST\_CLK source.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

**LP\_CLKRST\_FOSC\_CLK\_FORCE\_ON** Configures whether to force on RC\_FAST\_CLK as LP\_FAST\_CLK source.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

Register 9.60. LP\_CLKRST\_LP\_RST\_EN\_REG (0x000C)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LP_CLKRST_RST_EN_LP_RAM<br>LP_CLKRST_RST_EN_LP_AONEFUSEREG<br>LP_CLKRST_RST_EN_LP_MAILBOX<br>LP_CLKRST_RST_EN_LP_RTC<br>LP_CLKRST_RST_EN_LP_TIMER<br>LP_CLKRST_RST_EN_LP_WDT<br>LP_CLKRST_RST_EN_LP_ANAPERI<br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><br><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|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|

**LP\_CLKRST\_RST\_EN\_LP\_ANAPERI** Configures whether to reset LP analog peripherals.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_WDT** Configures whether to reset RWDT.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_TIMER** Configures whether to reset LP timer.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_RTC** Configures whether to reset the LP clock calibration module.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_MAILBOX** Configures whether to reset LP Mailbox.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_AONEFUSEREG** Configures whether to reset LP eFuse.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_LP\_RAM** Configures whether to reset LP RAM.

0: Release from reset

1: Reset

(R/W)

**Register 9.61. LP\_CLKRST\_RESET\_CAUSE\_REG (0x0010)**

|                                  |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |                                   |  |    |  |    |  |    |  |     |  |    |  |     |  |    |  |                                  |  |   |  |     |  |       |  |  |  |   |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------------------------------|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|-----------------------------------|--|----|--|----|--|----|--|-----|--|----|--|-----|--|----|--|----------------------------------|--|---|--|-----|--|-------|--|--|--|---|--|--|--|--|--|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LP_CLKRST_HPCORE1_RESET_FLAG_CLR |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  | LP_CLKRST_HPCORE1_RESET_CAUSE_CLR |  |    |  |    |  |    |  |     |  |    |  |     |  |    |  | LP_CLKRST_HPCORE0_RESET_FLAG_CLR |  |   |  |     |  |       |  |  |  |   |  |  |  |  |  | LP_CLKRST_HPCORE0_RESET_CAUSE_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_LPCORE_RESET_FLAG_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_LPCORE_RESET_CAUSE_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_HPCORE1_RESET_FLAG |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_HPCORE1_RESET_CAUSE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_HPCORE0_RESET_FLAG |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_HPCORE0_RESET_CAUSE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_LPCORE_RESET_FLAG |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_CLKRST_LPCORE_RESET_CAUSE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                               |  | 30 |  | 29 |  | 28 |  | 27 |  | 26 |  | 25 |  | 24 |  |                                   |  | 21 |  | 20 |  | 19 |  |     |  | 14 |  | 13  |  | 12 |  |                                  |  | 7 |  | 6   |  | 5     |  |  |  | 0 |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                                |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 1  |  | 0  |  | 0                                 |  | 0  |  | 0  |  | 0  |  | 0x0 |  | 0  |  | 0x0 |  | 0  |  | 0x0                              |  | 0 |  | 0x0 |  | Reset |  |  |  |   |  |  |  |  |  |                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**LP\_CLKRST\_LPCORE\_RESET\_CAUSE** Represents the reset source of LP CPU.

- 0x01: Chip reset
- 0x09: PMU LP Peripheral reset
- 0x0A: PMU LP CPU reset
- 0x0F: Brown-out system reset
- 0x10: RWDT system reset
- 0x12: Super watchdog reset
- 0x13: Power glitch reset
- 0x14: Software LP CPU reset
- (RO)

**LP\_CLKRST\_LPCORE\_RESET\_FLAG** Represents the reset flag of LP CPU.

- 0: Not reset
- 1: Reset
- (RO)

Continued on the next page...

**Register 9.61. LP\_CLKRST\_RESET\_CAUSE\_REG (0x0010)**

Continued from the previous page...

**LP\_CLKRST\_HPCORE0\_RESET\_CAUSE** Represents the reset source of HP CPU0.

0x01: Chip reset  
0x03: Software system reset  
0x05: PMU core reset  
0x07: MWDT core reset  
0x09: RWDT core reset  
0x0B: MWDT CPU reset  
0x0C: Software CPU reset  
0x0D: RWDT CPU reset  
0x0F: Brown-out system reset  
0x10: RWDT system reset  
0x12: Super watchdog reset  
0x13: Power glitch reset  
0x14: eFuse reset  
0x16: USB (JTAG) reset  
0x17: USB (UART) reset  
0x18: JTAG CPU reset  
0x1A: Lockup reset  
(RO)

**LP\_CLKRST\_HPCORE0\_RESET\_FLAG** Represents the reset flag of HP CPU0.

0: Not reset  
1: Reset  
(RO)

Continued on the next page...

**Register 9.61. LP\_CLKRST\_RESET\_CAUSE\_REG (0x0010)**

Continued from the previous page...

**LP\_CLKRST\_HPCORE1\_RESET\_CAUSE** Represents the reset source of HP CPU1.

0x01: Chip reset  
0x03: Software system reset  
0x05: PMU core reset  
0x07: MWDT core reset  
0x09: RWDT core reset  
0x0B: MWDT CPU reset  
0x0C: Software CPU reset  
0x0D: RWDT CPU reset  
0x0F: Brown-out system reset  
0x10: RWDT system reset  
0x12: Super watchdog reset  
0x13: Power glitch reset  
0x14: eFuse reset  
0x16: USB (JTAG) reset  
0x17: USB (UART) reset  
0x18: JTAG CPU reset  
0x1A: Lockup reset  
(RO)

**LP\_CLKRST\_HPCORE1\_RESET\_FLAG** Represents the reset flag of HP CPU1.

0: Not reset  
1: Reset  
(RO)

**LP\_CLKRST\_LPCORE\_RESET\_CAUSE\_PMU\_LP\_CPU\_MASK** Configures whether to mask the reset source code 0x0A of PMU LP CPU reset.

0: Not mask  
1: Mask  
(R/W)

Continued on the next page...

**Register 9.61. LP\_CLKRST\_RESET\_CAUSE\_REG (0x0010)**

Continued from the previous page...

**LP\_CLKRST\_LPCORE\_RESET\_CAUSE\_CLR** Write 1 to clear LP\_CLKRST\_LPCORE\_RESET\_CAUSE.  
(WT)

**LP\_CLKRST\_LPCORE\_RESET\_FLAG\_CLR** Write 1 to clear LP\_CLKRST\_LPCORE\_RESET\_FLAG. (WT)

**LP\_CLKRST\_HPCORE0\_RESET\_CAUSE\_CLR** Write 1 to clear LP\_CLKRST\_HPCORE0\_RESET\_CAUSE.  
(WT)

**LP\_CLKRST\_HPCORE0\_RESET\_FLAG\_CLR** Write 1 to clear LP\_CLKRST\_HPCORE0\_RESET\_FLAG.  
(WT)

**LP\_CLKRST\_HPCORE1\_RESET\_CAUSE\_CLR** Write 1 to clear LP\_CLKRST\_HPCORE1\_RESET\_CAUSE.  
(WT)

**LP\_CLKRST\_HPCORE1\_RESET\_FLAG\_CLR** Write 1 to clear LP\_CLKRST\_HPCORE1\_RESET\_FLAG.  
(WT)



Register 9.62. LP\_CLKRST\_HPCPU\_RESET\_CTRL0\_REG (0x0014)

|                                   |    |    |    |    |                                     |    |    |    |    |                            |    |    |    |    |                              |    |    |    |    |                                   |    |   |   |   |                                       |   |   |   |   |                                   |   |       |  |  |                                     |  |  |  |  |                            |  |  |  |  |                              |  |  |  |  |                                   |  |  |  |  |                                       |  |  |  |  |                                   |  |  |  |  |
|-----------------------------------|----|----|----|----|-------------------------------------|----|----|----|----|----------------------------|----|----|----|----|------------------------------|----|----|----|----|-----------------------------------|----|---|---|---|---------------------------------------|---|---|---|---|-----------------------------------|---|-------|--|--|-------------------------------------|--|--|--|--|----------------------------|--|--|--|--|------------------------------|--|--|--|--|-----------------------------------|--|--|--|--|---------------------------------------|--|--|--|--|-----------------------------------|--|--|--|--|
| LP_CLKRST_HPCORE1_STAT_VECTOR_SEL |    |    |    |    | LP_CLKRST_HPCORE1_ODD_HALT_ON_RESET |    |    |    |    | LP_CLKRST_HPCORE1_SW_RESET |    |    |    |    | LP_CLKRST_HPCORE1_STALL_WAIT |    |    |    |    | LP_CLKRST_LP_WDT_HPCORE1_RESET_EN |    |   |   |   | LP_CLKRST_LP_WDT_HPCORE1_RESET_LENGTH |   |   |   |   | LP_CLKRST_HPCORE0_STAT_VECTOR_SEL |   |       |  |  | LP_CLKRST_HPCORE0_ODD_HALT_ON_RESET |  |  |  |  | LP_CLKRST_HPCORE0_SW_RESET |  |  |  |  | LP_CLKRST_HPCORE0_STALL_WAIT |  |  |  |  | LP_CLKRST_LP_WDT_HPCORE0_RESET_EN |  |  |  |  | LP_CLKRST_LP_WDT_HPCORE0_RESET_LENGTH |  |  |  |  | LP_CLKRST_HPCORE0_LOCKUP_RESET_EN |  |  |  |  |
| 31                                | 30 | 29 | 28 | 27 | 26                                  | 25 | 24 | 23 | 22 | 21                         | 20 | 19 | 18 | 17 | 16                           | 15 | 14 | 13 | 12 | 11                                | 10 | 9 | 8 | 7 | 6                                     | 5 | 4 | 3 | 2 | 1                                 | 0 |       |  |  |                                     |  |  |  |  |                            |  |  |  |  |                              |  |  |  |  |                                   |  |  |  |  |                                       |  |  |  |  |                                   |  |  |  |  |
| 1                                 | 0  | 0  | 0  | 0  | 0                                   | 0  | 0  | 0  | 0  | 0                          | 0  | 1  | 0  | 0  | 0                            | 1  | 0  | 0  | 0  | 0                                 | 0  | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 1 | 0                                 | 0 | Reset |  |  |                                     |  |  |  |  |                            |  |  |  |  |                              |  |  |  |  |                                   |  |  |  |  |                                       |  |  |  |  |                                   |  |  |  |  |

Reset

**LP\_CLKRST\_HPCORE0\_LOCKUP\_RESET\_EN** Configures whether to enable Lockup to trigger HP CPU0 reset.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_LP\_WDT\_HPCORE0\_RESET\_LENGTH** Configures the duration of the reset when RWDT and software trigger HP CPU0 reset.

Measurement unit: Clock cycles. (R/W)

**LP\_CLKRST\_LP\_WDT\_HPCORE0\_RESET\_EN** Configures whether to enable RWDT to trigger HP CPU0 reset.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HPCORE0\_STALL\_WAIT** Configures the time HP CPU0 stalls when RWDT and software trigger HP CPU0 reset.

Measurement unit: Clock cycles. (R/W)

**LP\_CLKRST\_HPCORE0\_STALL\_EN** Configures the behavior when RWDT and software trigger HP CPU0 reset.

0: Immediately reset HP CPU0

1: Stall HP CPU0 first

(R/W)

**LP\_CLKRST\_HPCORE0\_SW\_RESET** Write 1 to trigger HP CPU0 software reset. (WT)

**LP\_CLKRST\_HPCORE0\_OCD\_HALT\_ON\_RESET** Configures whether HP CPU0 halts at the first instruction after released from reset.

0: No halt

1: Halt

(R/W)

Continued on the next page...

**Register 9.62. LP\_CLKRST\_HPCPU\_RESET\_CTRL0\_REG (0x0014)**

Continued from the previous page...

**LP\_CLKRST\_HPCORE0\_STAT\_VECTOR\_SEL** Configures the address from which the HP CPU0 starts.

0: From LP SPM RAM (0x50108000)

1: From HP SPM ROM (0x4FC00000)

(R/W)

**LP\_CLKRST\_HPCORE1\_LOCKUP\_RESET\_EN** Configures whether to enable Lockup to trigger HP CPU1 reset.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_LP\_WDT\_HPCORE1\_RESET\_LENGTH** Configures the duration of the reset when RWDT and software trigger HP CPU1 reset.

Measurement unit: Clock cycles. (R/W)

**LP\_CLKRST\_LP\_WDT\_HPCORE1\_RESET\_EN** Configures whether to enable RWDT to trigger HP CPU1 reset.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HPCORE1\_STALL\_WAIT** Configures the time HP CPU1 stalls when RWDT and software trigger HP CPU1 reset.

Measurement unit: Clock cycles. (R/W)

**LP\_CLKRST\_HPCORE1\_STALL\_EN** Configures the behavior when RWDT and software trigger HP CPU1 reset.

0: Immediately reset HP CPU1

1: Stall HP CPU1 first

(R/W)

**LP\_CLKRST\_HPCORE1\_SW\_RESET** Write 1 to trigger HP CPU1 software reset. (WT)

**LP\_CLKRST\_HPCORE1\_OCD\_HALT\_ON\_RESET** Configures whether HP CPU1 halts at the first instruction after released from reset.

0: No halt

1: Halt

(R/W)

**LP\_CLKRST\_HPCORE1\_STAT\_VECTOR\_SEL** Configures the address from which the HP CPU1 starts.

0: From LP SPM RAM (0x50108000)

1: From HP SPM ROM (0x4FC00000)

(R/W)

**Register 9.63. LP\_CLKRST\_HPCPU\_RESET\_CTRL1\_REG (0x0018)**

[illegible]

**LP\_CLKRST\_HPCORE0\_SW\_STALL\_CODE** Configures the threshold for HP CPU0 stall triggered by software. (R/W)

**LP\_CLKRST\_HPCORE1\_SW\_STALL\_CODE** Configures the threshold for HP CPU1 stall triggered by software. (R/W)

**Register 9.64. LP\_CLKRST\_FOSC\_CNTL\_REG (0x001C)**

**LP\_CLKRST\_FOSC\_DFREQ** Configures the frequency of RC\_FAST\_CLK. (R/W)

Register 9.65. LP\_CLKRST\_XTAL32K\_REG (0x0030)

|                       |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |   |  |  |   |  |  |   |                        |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |                       |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |                        |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |            |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  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| LP_CLKRST_DAC_XTAL32K |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |   |  |  |   |  |  |   | LP_CLKRST_DBUF_XTAL32K |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  | LP_CLKRST_DGM_XTAL32K |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  | LP_CLKRST_DRES_XTAL32K |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   | (reserved) |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  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| 31                    |  |  | 29 |  |  | 28 |  |  | 27 |  |  | 25 |  |  | 24 |  |  | 22 |  |  | 21 |  |  | 0 |  |  |   |  |  |   |                        |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |                       |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |                        |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |            |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  |   |  |  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| 3                     |  |  | 0  |  |  | 3  |  |  | 3  |  |  | 0  |  |  | 0  |  |  | 0  |  |  | 0  |  |  | 0 |  |  | 0 |  |  | 0 |                        |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |                       | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0                      |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |            |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  |

**LP\_CLKRST\_DRES\_XTAL32K** Configures the bias resistor of XTAL32K\_CLK.  
0: Turn off internal resistor, use external resistor  
1-3: Internal bias resistor value  
(R/W)

**LP\_CLKRST\_DGM\_XTAL32K** Configures the gm of XTAL32K\_CLK. (R/W)

**LP\_CLKRST\_DBUF\_XTAL32K** Configures the buffer of XTAL32K\_CLK.  
0: Single-ended buffer  
1: Differential buffer  
(R/W)

**LP\_CLKRST\_DAC\_XTAL32K** Configures the bias current DAC of XTAL32K\_CLK. (R/W)

Register 9.66. LP\_CLKRST\_HP\_CLK\_CTRL\_REG (0x0040)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |  |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|--|
| <div>(reserved)</div> <div>LP_CLKRST_HP_MPLL_500M_CLK_EN</div> <div>LP_CLKRST_HP_SPLL_480M_CLK_EN</div> <div>LP_CLKRST_HP_CPLL_400M_CLK_EN</div> <div>LP_CLKRST_HP_XTAL_40M_CLK_EN</div> <div>LP_CLKRST_HP_FOSC_20M_CLK_EN</div> <div>LP_CLKRST_HP_SDIO_PLLO_CLK_EN</div> <div>LP_CLKRST_HP_SDIO_PLL1_CLK_EN</div> <div>LP_CLKRST_HP_AUDIO_PLL2_CLK_EN</div> <div>(reserved)</div> <div>LP_CLKRST_HP_PLL_8M_CLK_EN</div> <div>LP_CLKRST_HP_SOSC_150K_CLK_EN</div> <div>LP_CLKRST_HP_XTAL_32K_CLK_EN</div> <div>LP_CLKRST_HP_PAD_EMAC_TXRX_CLK_EN</div> <div>LP_CLKRST_HP_PAD_EMAC_RX_CLK_EN</div> <div>LP_CLKRST_HP_PAD_I2S0_MCLK_EN</div> <div>LP_CLKRST_HP_PAD_I2S1_MCLK_EN</div> <div>LP_CLKRST_HP_PAD_I2S2_MCLK_EN</div> <div>LP_CLKRST_HP_PAD_UART0_SLP_CLK_EN</div> <div>LP_CLKRST_HP_PAD_UART1_SLP_CLK_EN</div> <div>LP_CLKRST_HP_PAD_UART2_SLP_CLK_EN</div> <div>LP_CLKRST_HP_PAD_UART3_SLP_CLK_EN</div> <div>LP_CLKRST_HP_PAD_UART4_SLP_CLK_EN</div> <div>LP_CLKRST_HP_PAD_PARLIO_RX_CLK_EN</div> <div>LP_CLKRST_HP_PAD_PARLIO_TX_CLK_EN</div> <div>LP_CLKRST_HP_ROOT_CLK_SRC_SEL</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |  |
| 31   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |  |
| 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | Reset |  |

Reset

**LP\_CLKRST\_HP\_ROOT\_CLK\_SRC\_SEL** Configures the clock source of ROOT\_CLK.

- 0: XTAL\_CLK
  - 1: CPLL\_CLK (360 MHz)
  - 2: RC\_FAST\_CLK
  - 3: Invalid
- (R/W)

**LP\_CLKRST\_HP\_ROOT\_CLK\_EN** Configures whether to enable ROOT\_CLK.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_CLKRST\_HP\_PAD\_PARLIO\_TX\_CLK\_EN** Configures whether to enable PAD\_PARLIO\_TX\_CLK from IO pin.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_CLKRST\_HP\_PAD\_PARLIO\_RX\_CLK\_EN** Configures whether to enable PAD\_PARLIO\_RX\_CLK from IO pin.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_CLKRST\_HP\_PAD\_UART4\_SLP\_CLK\_EN** Configures whether to enable PAD\_UART4\_SLP\_CLK from IO pin.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_CLKRST\_HP\_PAD\_UART3\_SLP\_CLK\_EN** Configures whether to enable PAD\_UART3\_SLP\_CLK from IO pin.

- 0: Disable
  - 1: Enable
- (R/W)

Continued on the next page...

**Register 9.66. LP\_CLKRST\_HP\_CLK\_CTRL\_REG (0x0040)**

Continued from the previous page...

**LP\_CLKRST\_HP\_PAD\_UART2\_SLP\_CLK\_EN** Configures whether to enable PAD\_UART2\_SLP\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_UART1\_SLP\_CLK\_EN** Configures whether to enable PAD\_UART1\_SLP\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_UART0\_SLP\_CLK\_EN** Configures whether to enable PAD\_UART0\_SLP\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_I2S2\_MCLK\_EN** Configures whether to enable PAD\_I2S2\_MCLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_I2S1\_MCLK\_EN** Configures whether to enable PAD\_I2S1\_MCLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_I2S0\_MCLK\_EN** Configures whether to enable PAD\_I2S0\_MCLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_ETH\_TX\_CLK\_EN** Configures whether to enable PAD\_ETH\_TX\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.66. LP\_CLKRST\_HP\_CLK\_CTRL\_REG (0x0040)**

Continued from the previous page...

**LP\_CLKRST\_HP\_PAD\_EMAC\_RX\_CLK\_EN** Configures whether to enable PAD\_EMAC\_TX\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PAD\_EMAC\_TXRX\_CLK\_EN** Configures whether to enable PAD\_EMAC\_TXRX\_CLK from IO pin.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_XTAL\_32K\_CLK\_EN** Configures whether to enable XTAL32K\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_SOSC\_150K\_CLK\_EN** Configures whether to enable RC\_SLOW\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_PLL\_8M\_CLK\_EN** Configures whether to enable PLL\_LP\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_AUDIO\_PLL\_CLK\_EN** Configures whether to enable APLL\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_SDIO\_PLL2\_CLK\_EN** Configures whether to enable SDIO\_PLL2\_CLK.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.66. LP\_CLKRST\_HP\_CLK\_CTRL\_REG (0x0040)**

Continued from the previous page...

**LP\_CLKRST\_HP\_SDIO\_PLL1\_CLK\_EN** Configures whether to enable SDIO\_PLL1\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_SDIO\_PLLO\_CLK\_EN** Configures whether to enable SDIO\_PLLO\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_FOSC\_20M\_CLK\_EN** Configures whether to enable RC\_FAST\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_XTAL\_40M\_CLK\_EN** Configures whether to enable XTAL\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_CPLL\_400M\_CLK\_EN** Configures whether to enable CPLL\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_SPLL\_480M\_CLK\_EN** Configures whether to enable SPLL\_CLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_HP\_MPLL\_500M\_CLK\_EN** Configures whether to enable MPLL\_CLK.

0: Disable

1: Enable

(R/W)



### Register 9.67. LP\_CLKRST\_HP\_USB\_CLKRST\_CTRL0\_REG (0x0044)

|            |    |                           |    |                           |    |                           |  |                                 |   |                                |   |                                   |   |                                |   |                                   |  |                                |  |
|------------|----|---------------------------|----|---------------------------|----|---------------------------|--|---------------------------------|---|--------------------------------|---|-----------------------------------|---|--------------------------------|---|-----------------------------------|--|--------------------------------|--|
| (reserved) |    | LP_CLKRST_USB_I2M_DIV_NUM |    | LP_CLKRST_USB_25M_DIV_NUM |    | LP_CLKRST_USB_48M_DIV_NUM |  | LP_CLKRST_USB_DEVICE_48M_CLK_EN |   | LP_CLKRST_USB_OTG11_48M_CLK_EN |   | LP_CLKRST_USB_OTG11_BK_SYS_CLK_EN |   | LP_CLKRST_USB_OTG11_SLEEP_MODE |   | LP_CLKRST_USB_OTG20_BK_SYS_CLK_EN |  | LP_CLKRST_USB_OTG20_SLEEP_MODE |  |
| 31         | 30 | 29                        | 22 |                           | 21 | 14                        |  | 13                              | 6 |                                | 5 | 4                                 | 3 | 2                              | 1 | 0                                 |  |                                |  |
| 0          | 0  | 39                        |    | 19                        |    | 9                         |  |                                 |   | 1                              | 1 | 1                                 | 0 | 1                              | 0 | Reset                             |  |                                |  |

**LP\_CLKRST\_USB\_OTG20\_SLEEP\_MODE** Not used. (R/W)

LP CLKRST USB OTG20 BK SYS CLK EN Not used. (R/W)

**LP\_CLKRST\_USB\_OTG11\_SLEEP\_MODE** Not used. (R/W)

LP\_CLKRST\_USB\_OTG11\_BK\_SYS\_CLK\_EN Not used. (R/W)

**LP\_CLKRST\_USB\_OTG11\_48M\_CLK\_EN** Configures whether to enable the Full-Speed USB 2.0 OTG PHY clock.  
0: Disable  
1: Enable  
(R/W)

**LP\_CLKRST\_USB\_DEVICE\_48M\_CLK\_EN** Configures whether to enable the USB Serial/JTAG PHY clock.  
0: Disable  
1: Enable  
(R/W)

**LP\_CLKRST\_USB\_48M\_DIV\_NUM** Configures the division number from USB 480M to 25M. (R/W)

**LP\_CLKRST\_USB\_25M\_DIV\_NUM** Configures the division number from USB 500M to 25M. (R/W)

**LP\_CLKRST\_USB\_12M\_DIV\_NUM** Configures the division number from USB 480M to 12M. (R/W)

**Register 9.68. LP\_CLKRST\_HP\_USB\_CLKRST\_CTRL1\_REG (0x0048)**

|                                 |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
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| LP_CLKRST_USB_OTG20_ULPI_CLK_EN |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_USB_OTG20_PHYREF_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_USB_OTG20_PHYREF_CLK_SRC_SEL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_RST_EN_USB_DEVICE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_RST_EN_USB_OTG11 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_RST_EN_USB_OTG20 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_RST_EN_USB_OTG20_PHY |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_CLKRST_RST_EN_USB_OTG20_ADP |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31                              | 30 | 29 | 28 | 27 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 4 | 3 | 2 | 1 | 0 |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 1                               | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

**LP\_CLKRST\_RST\_EN\_USB\_OTG20\_ADP** Configures whether to reset High-Speed USB 2.0 OTG ADP.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_USB\_OTG20\_PHY** Configures whether to reset High-Speed USB 2.0 OTG PHY.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_USB\_OTG20** Configures whether to reset High-Speed USB 2.0 OTG.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_USB\_OTG11** Configures whether to reset Full-Speed USB 2.0 OTG.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_RST\_EN\_USB\_DEVICE** Configures whether to reset USB Serial/JTAG.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.68. LP\_CLKRST\_HP\_USB\_CLKRST\_CTRL1\_REG (0x0048)**

Continued from the previous page...

**LP\_CLKRST\_USB\_OTG20\_PHYREF\_CLK\_SRC\_SEL** Configures the clock source of High-Speed USB 2.0 OTG HS PHY.

0: PLL\_F12M\_CLK

1: PLL\_F25M\_CLK

2: PAD\_USB\_HSPHY\_REFCLK

3: Invalid

(R/W)

**LP\_CLKRST\_USB\_OTG20\_PHYREF\_CLK\_EN** Configures whether to enable High-Speed USB 2.0 OTG HS PHY REFCLK.

0: Disable

1: Enable

(R/W)

**LP\_CLKRST\_USB\_OTG20\_ULPI\_CLK\_EN** Configures whether to enable High-Speed USB 2.0 OTG ULPI clock.

0: Disable

1: Enable

(R/W)

**Register 9.69. LP\_CLKRST\_HP\_SDMMC\_EMAC\_RST\_CTRL\_REG (0x004C)**

LP\_CLKRST\_FORCE\_NORST\_EMAC

LP\_CLKRST\_RST\_EN\_EMAC

LP\_CLKRST\_FORCE\_NORST\_SDMMC

LP\_CLKRST\_RST\_EN\_SDMMC

(reserved)

|    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 | 29 | 28 | 27 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**LP\_CLKRST\_RST\_EN\_SDMMC** Configures whether to reset SDMMC.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_FORCE\_NORST\_SDMMC** Configures whether SDMMC can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**LP\_CLKRST\_RST\_EN\_EMAC** Configures whether to reset EMAC.

0: Release from reset

1: Reset

(R/W)

**LP\_CLKRST\_FORCE\_NORST\_EMAC** Configures whether EMAC can be reset.

0: Can be reset

1: Force not to be reset

(R/W)

**Register 9.70. LP\_CLKRST\_DATE\_REG (0x03FC)**

|                  |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LP_CLKRST_CLK_EN |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| (reserved)       |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31               | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**LP\_CLKRST\_CLK\_EN** Configures register clock gating.

0: Support clock only when application writes registers

1: Force on clock gating for registers

(R/W)

### 9.5.3 LP Peripheral Clock and Reset (LPPERI) Registers

The addresses in this section are relative to LPPERI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

### Register 9.71. LPPERI\_CLK\_EN\_REG (0x0000)

**LPPERI\_CK\_EN\_RNG** Configures whether to enable LP RNG clock.

0: Disable

1: Enable

(R/W)

**LPperi\_ck\_en\_lp\_tsens** Configures whether to enable LP temperature sensor clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_PMS** Configures whether to enable LP PMS clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_EFUSE** Configures whether to enable LP eFuse clock.

0: Disable

1: Enable

(R/W)

**LPperi\_ck\_en\_lp\_iomux** Configures whether to enable LP IO MUX clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_TOUCH** Configures whether to enable LP touch sensor clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_SPI** Configures whether to enable LP SPI clock.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 9.71. LPPERI\_CLK\_EN\_REG (0x0000)**

Continued from the previous page...

**LPPERI\_CK\_EN\_LP\_ADC** Configures whether to enable LP ADC clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_I2S\_RX** Configures whether to enable LP I2S RX clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_I2S** Configures whether to enable LP I2S clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_I2CMST** Configures whether to enable LP I2C master clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_I2C** Configures whether to enable LP I2C clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_UART** Configures whether to enable LP UART clock.

0: Disable

1: Enable

(R/W)

**LPPERI\_CK\_EN\_LP\_INTR** Configures whether to enable LP interrupt matrix clock.

0: Disable

1: Enable

(R/W)

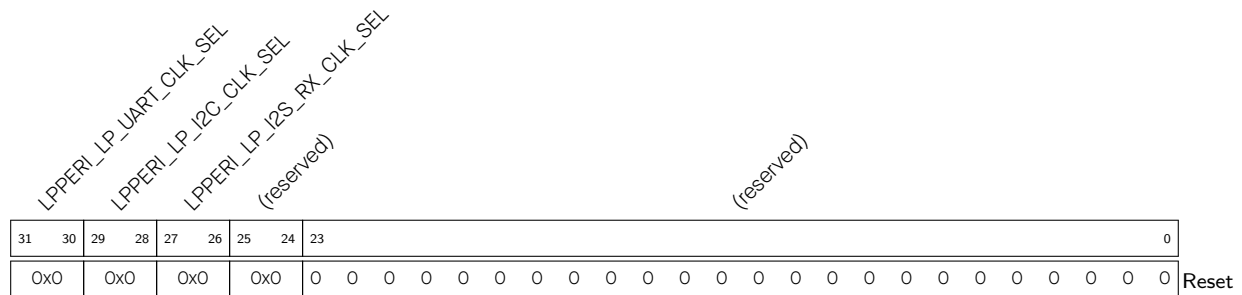
**LPPERI\_CK\_EN\_LP\_CORE** Configures whether to force on LP CPU clock.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

### Register 9.72. LPPERI\_CORE\_CLK\_SEL\_REG (0x0004)



**LPPERI\_LP\_I2S\_RX\_CLK\_SEL** Configures LP I2S RX clock source.

- 0: LP\_FAST\_CLK  
1: XTAL\_D2\_CLK  
2: PLL\_LP\_CLK  
3: Invalid  
(R/W)

**LPPERI\_LP\_I2C\_CLK\_SEL** Configures LP I2C clock source.

- 0: LP\_FAST\_CLK  
1: XTAL\_D2\_CLK  
2: PLL\_LP\_CLK  
3: Invalid  
(R/W)

**LPPERI\_LP\_UART\_CLK\_SEL** Configures LP UART clock source.

- 0: LP\_FAST\_CLK  
1: XTAL\_D2\_CLK  
2: PLL\_LP\_CLK  
3: Invalid  
(R/W)



Register 9.73. LPPERI\_RESET\_EN\_REG (0x0008)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div>LPPERI_RST_EN_LP_CORE<br/>LPPERI_RST_EN_LP_ROM<br/>LPPERI_RST_EN_LP_INTR<br/>LPPERI_RST_EN_LP_UART<br/>LPPERI_RST_EN_LP_I2C<br/>LPPERI_RST_EN_LP_I2CMST<br/>LPPERI_RST_EN_LP_I2S<br/>LPPERI_RST_EN_LP_ADC<br/>LPPERI_RST_EN_LP_SPI<br/>LPPERI_RST_EN_LP_TOUCH<br/>LPPERI_RST_EN_LP_IOMUX<br/>LPPERI_RST_EN_LP_EFUSE<br/>LPPERI_RST_EN_LP_PMS<br/>LPPERI_RST_EN_LP_TSENS</div> <div>(reserved)</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LPPERI\_RST\_EN\_LP\_TSENS** Configures whether to reset LP temperature sensor.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_PMS** Configures whether to reset LP PMS.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_EFUSE** Configures whether to reset LP eFuse.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_IOMUX** Configures whether to reset LP IO MUX.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_TOUCH** Configures whether to reset LP touch sensor.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_SPI** Configures whether to reset LP SPI.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_ADC** Configures whether to reset LP ADC.

0: Release from reset

1: Reset

(R/W)

Continued on the next page...

**Register 9.73. LPPERI\_RESET\_EN\_REG (0x0008)**

Continued from the previous page...

**LPPERI\_RST\_EN\_LP\_I2S** Configures whether to reset LP I2S.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_I2CMST** Configures whether to reset LP I2C master.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_I2C** Configures whether to reset LP I2C.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_UART** Configures whether to reset LP UART.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_INTR** Configures whether to reset LP interrupt matrix.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_ROM** Configures whether to reset LP ROM.

0: Release from reset

1: Reset

(R/W)

**LPPERI\_RST\_EN\_LP\_CORE** Writing 1 triggers LP CPU software reset. (WT)

### Register 9.74. LPPERI\_CPU\_REG (0x000C)

Diagram of the LPPER1\_LPCORE\_DBGM\_UNAVAILABLE register. The register is 32 bits wide, with bit 31 labeled 'LPPER1\_LPCORE\_DBGM\_UNAVAILABLE' and bit 0 labeled 'Reset'. The register is divided into two sections: a 30-bit section labeled '(reserved)' and a 2-bit section labeled 'LPPER1\_LPCORE\_DBGM\_UNAVAILABLE'.

**LPperi\_LPCore\_DBGm\_Unavailable** Configures whether the LP CPU can be accessed by the HP CPU.

0: Not accessible

1: Accessible

(R/W)

Register 9.75. LPPERI\_MEM\_CTRL\_REG (0x0028)

|                             |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
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| LPPERI_LP_UART_MEM_FORCE_PU |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPPERI_LP_UART_WAKEUP_FLAG_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| LPPERI_LP_UART_MEM_FORCE_PU |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPPERI_LP_UART_WAKEUP_FLAG_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| LPPERI_LP_UART_WAKEUP_EN    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31                          | 30 | 29 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2          | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 1                           | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

**LPPERI\_LP\_UART\_WAKEUP\_FLAG\_CLR** Write 1 to clear LPPERI\_LP\_UART\_WAKEUP\_FLAG. (WT)

**LPPERI\_LP\_UART\_WAKEUP\_FLAG** Represents whether an LP UART wakeup has occurred.

0: No LP UART wakeup occurred

1: LP UART wakeup occurred

(R/WTC/SS)

**LPPERI\_LP\_UART\_WAKEUP\_EN** Configures whether to enable the LP UART wakeup function.

0: Enable

1: Disable

(R/W)

**LPPERI\_LP\_UART\_MEM\_FORCE\_PD** Configures whether to force the LP UART memory to power down.

0: Do not force power down

1: Force power down

(R/W)

**LPPERI\_LP\_UART\_MEM\_FORCE\_PU** Configures whether to force the LP UART memory to power up.

0: Do not force power up

1: Force power up

(R/W)

Register 9.76. LPPERI\_ADC\_CTRL\_REG (0x002C)

|                           |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  |  |  |   |  |   |  |   |  |   |  |       |  |   |  |  |  |  |  |  |  |
|---------------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|---|--|---|--|---|--|---|--|--|--|---|--|---|--|---|--|---|--|-------|--|---|--|--|--|--|--|--|--|
| LPPERI_LPADC_SAR1_DIV_NUM |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  | LPPERI_LPADC_SAR2_DIV_NUM |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  | LPPERI_LPADC_FUNC_DIV_NUM |  |  |  |  |  |  |  |   |  |   |  |   |  |   |  | LPPERI_SAR1_CLK_FORCE_ON<br>LPPERI_SAR2_CLK_FORCE_ON<br>(reserved) |  |   |  |   |  |   |  |   |  |       |  |   |  |  |  |  |  |  |  |
| 31                        |  |  |  |  |  |  |  | 24 |  |  |  |  |  |  |  | 23                        |  |  |  |  |  |  |  | 16 |  |  |  |  |  |  |  | 15                        |  |  |  |  |  |  |  | 8 |  |   |  |   |  |   |  | 7  |  | 6 |  | 5 |  |   |  |   |  |       |  | 0 |  |  |  |  |  |  |  |
| 0x4                       |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  | 0x4                       |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  | 0x4                       |  |  |  |  |  |  |  | 0 |  | 0 |  | 0 |  | 0 |  | 0  |  | 0 |  | 0 |  | 0 |  | 0 |  | Reset |  |   |  |  |  |  |  |  |  |

**LPPERI\_SAR2\_CLK\_FORCE\_ON** Configures whether to force on the LP ADC SAR1 clock.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

**LPPERI\_SAR1\_CLK\_FORCE\_ON** Configures whether to force on the LP ADC SAR2 clock.

0: Controlled by hardware

1: Force on, bypassing hardware control

(R/W)

**LPPERI\_LPADC\_FUNC\_DIV\_NUM** Configures the LP ADC function clock divisor. (R/W)

**LPPERI\_LPADC\_SAR2\_DIV\_NUM** Configures the LP ADC SAR1 clock divisor.(R/W)

**LPPERI\_LPADC\_SAR1\_DIV\_NUM** Configures the LP ADC SAR2 clock divisor.(R/W)

Register 9.77. LPPERI\_LP\_I2S\_RXCLK\_DIV\_NUM\_REG (0x0030)

|                               |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|-------------------------------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| LPPERI_LP_I2S_RX_CLKM_DIV_NUM |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                            |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 24         |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x2                           |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**LPPERI\_LP\_I2S\_RX\_CLKM\_DIV\_NUM** Configures the integer part of the LP I2S RX clock divisor.

(R/W)

Register 9.78. LPPERI\_LP\_I2S\_RXCLK\_DIV\_XYZ\_REG (0x0034)

|   |    |     |    |     |   |   |   |   |   |
|---|----|-----|----|-----|---|---|---|---|---|
| LPPERI_LP_I2S_RX_CLKM_DIV_X                 |    |     |    |     |   |   |   |   |   |
| LPPERI_LP_I2S_RX_CLKM_DIV_Y                 |    |     |    |     |   |   |   |   |   |
| LPPERI_LP_I2S_RX_CLKM_DIV_Z                 |    |     |    |     |   |   |   |   |   |
| LPPERI_LP_I2S_RX_CLKM_DIV_YN1<br>(reserved) |    |     |    |     |   |   |   |   |   |
| 31  | 23 | 22  | 14 | 13  | 5 | 4 | 3 | 0 |   |
| 0x0   |    | 0x1 |    | 0x0 |   | 0 | 0 | 0 | 0 |

Reset

**LPPERI\_LP\_I2S\_RX\_CLKM\_DIV\_YN1** Configures the yn1 coefficient of the LP I2S RX clock divisor. (R/W)

**LPPERI\_LP\_I2S\_RX\_CLKM\_DIV\_Z** Configures the z coefficient of the LP I2S RX clock divisor. (R/W)

**LPPERI\_LP\_I2S\_RX\_CLKM\_DIV\_Y** Configures the y coefficient of the LP I2S RX clock divisor. (R/W)

**LPPERI\_LP\_I2S\_RX\_CLKM\_DIV\_X** Configures the x coefficient of the LP I2S RX clock divisor. (R/W)

Register 9.79. LPPERI\_DATE\_REG (0x03FC)

|               |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LPPERI_CLK_EN |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| (reserved)    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31            | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |
| 0             | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**LPPERI\_CLK\_EN** Configures resister clock gating.  
 0: Support clock only when application writes registers  
 1: Force on clock gating for registers  
 (R/W)

## Chapter 10

### Chip Boot Control

#### 10.1 Overview

Chip boot process and some chip functions are determined on power-on or hardware reset using strapping pins and eFuse bits. The following functionality can be determined:

- chip boot mode
- enable or disable of ROM messages printing
- source of JTAG signals

ESP32-P4 has five strapping pins:

- GPIO34
- GPIO35
- GPIO36
- GPIO37
- GPIO38

During Chip Reset (see Chapter 9 [Reset and Clock](#)), hardware samples and stores the voltage level of strapping pins as strapping bit of “0” or “1” in latches, and holds these bits until the chip is powered down. Software can read the latch status (strapping value) from [GPIO\\_STRAPPING](#).

#### 10.2 Functional Description

This section provides description of the chip functions and the patterns of the strapping pins and eFuse values to invoke each function.

**Notice:**

Only documented patterns should be used. If an undocumented pattern is used, it may trigger unexpected behaviors.

##### 10.2.1 Default Configuration

By default, GPIO35 is connected to the chip’s internal pull-up resistor. If GPIO35 is not connected or is connected to an external high-impedance circuit, the internal weak pull-up determines the default input level of this strapping pin (see Table [10.2-1](#)).

**Table 10.2-1. Default Configuration of Strapping Pins**

| Strapping Pin | Default Configuration |
|---------------|-----------------------|
| <b>GPIO34</b> | Floating              |
| <b>GPIO35</b> | Pull-up               |
| <b>GPIO36</b> | Floating              |
| <b>GPIO37</b> | Floating              |
| <b>GPIO38</b> | Floating              |

To change the strapping bit values, users can apply external pull-down/pull-up resistors, or use host MCU GPIOs to control the voltage level of these pins when powering on ESP32-P4. After the reset is released, the strapping pins work as normal-function pins.

## 10.2.2 Boot Mode Control

The values of GPIO35, GPIO36, GPIO37 and GPIO38 at reset determine the boot mode after the reset is released. Table 10.2-2 shows the strapping pin values of GPIO35, GPIO36, GPIO37 and GPIO38 and the associated boot modes.

**Table 10.2-2. Boot Mode Control**

| Boot Mode                             | GPIO35 | GPIO36         | GPIO37 | GPIO38 |
|---------------------------------------|--------|----------------|--------|--------|
| SPI Boot mode (default)               | 1      | x <sup>1</sup> | x      | x      |
| Joint Download Boot mode <sup>2</sup> | 0      | 1              | x      | x      |
| SPI Download Boot mode <sup>3</sup>   | 0      | 0              | 0      | 1      |
| Invalid Combination <sup>4</sup>      | 0      | 0              | 1      | x      |
|                                       | 0      | 0              | 0      | 0      |

<sup>1</sup> x: values that have no effect on the result and can therefore be ignored.

<sup>2</sup> Joint Download Boot mode: Joint Download Boot mode supports the following download methods:

- USB-Serial-JTAG Download Boot
- UART Download Boot
- SPI Slave Download Boot
- USB 2.0 OTG Download Boot

<sup>3</sup> SPI Download Boot mode: GPIO37 and GPIO38 need to be reserved only when using SPI Download Boot mode. GPIO37 and GPIO38 are floating by default and are in a high-impedance state at reset.

<sup>4</sup> Invalid Combination: This combination can trigger unexpected behavior and should be avoided.

In SPI Boot mode, the ROM bootloader loads and executes the program from SPI flash to boot the system. SPI Boot mode can be further classified as follows:

- Normal flash Boot: supports Secure Boot. The ROM bootloader loads the program from flash into L2MEM and executes it. In most practical scenarios, this program is the 2nd stage bootloader, which later boots the target application.

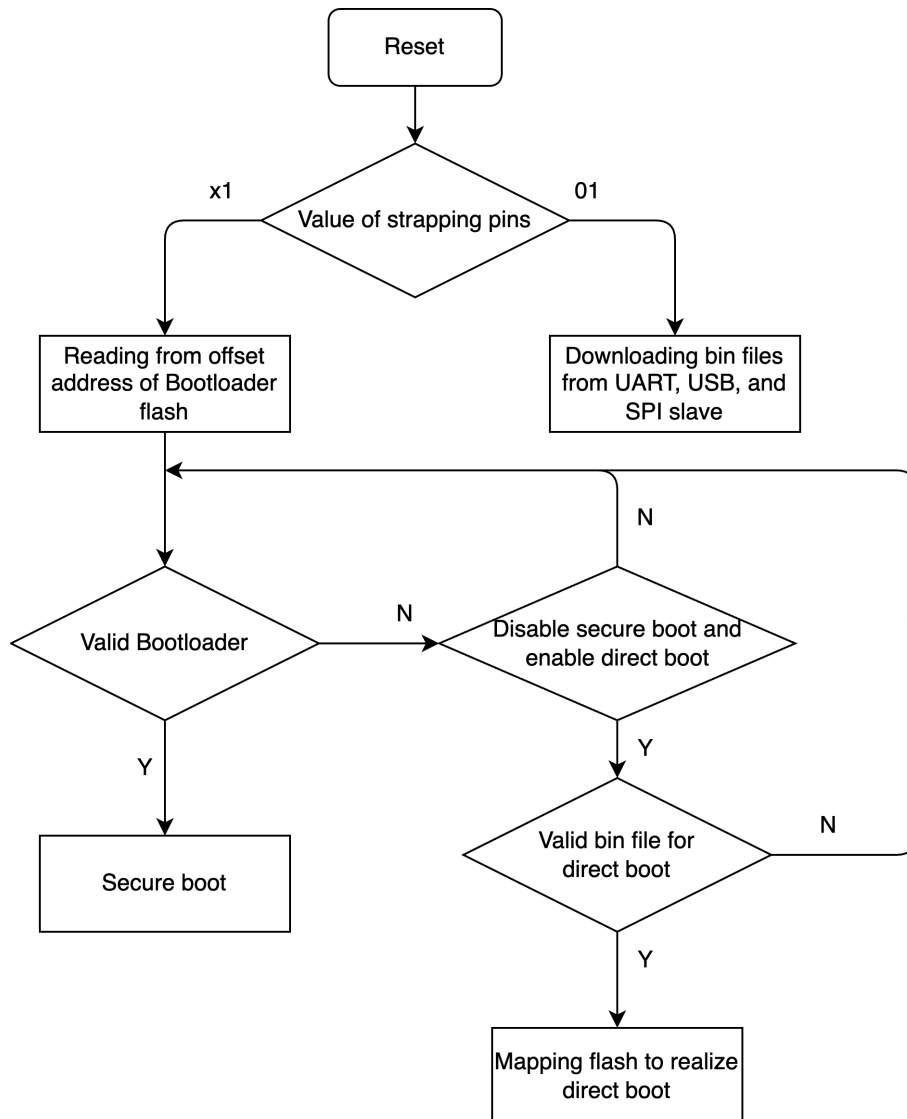


- **Direct Boot:** does not support Secure Boot and programs run directly from flash. To enable this mode, make sure that the first two words of the bin file downloaded to flash are 0xaedb041d. For more detailed process, see Figure 10.2-1.

In Joint Download Boot mode, users can download binary files into flash using UART0, SPI slave, USB 2.0 OTG or USB Serial/JTAG interface. It is also possible to download binary files into L2MEM and execute it from L2MEM.

In SPI Download Boot mode, users can download binary files into flash using SPI interface. It is also possible to download binary files into L2MEM and execute it from L2MEM.

Figure 10.2-1 shows the detailed boot flow of the chip.



**Note:** “x1” and “01” are combination values of strapping pins GPIO35 and GPIO36, see Table 10.2-2.

Figure 10.2-1. Chip Boot Flow

The following eFuse bits allows controlling boot mode behaviors:

- [EFUSE\\_DIS\\_FORCE\\_DOWNLOAD](#)

If this eFuse is 0 (default), software can force switch the chip from SPI Boot mode to Joint Download

Boot mode by setting register LPSYSREG\_FORCE\_DOWNLOAD\_BOOT and triggering a CPU reset. If this eFuse is 1, LPSYSREG\_FORCE\_DOWNLOAD\_BOOT is disabled.

- [EFUSE\\_DIS\\_DOWNLOAD\\_MODE](#)

If this eFuse is 1, Joint Download Boot mode is permanently disabled.

- [EFUSE\\_ENABLE\\_SECURITY\\_DOWNLOAD](#)

If this eFuse is 1, Joint Download Boot mode only allows reading, writing, and erasing plaintext flash and does not support any L2MEM or register operations. Ignore this eFuse if Download Boot mode is disabled.

- [EFUSE\\_DIS\\_DIRECT\\_BOOT](#)

If this eFuse is 1, Direct Boot would be disabled in SPI Boot Mode.

USB Serial/JTAG Controller can also force switch the chip to Joint Download Boot mode from SPI Boot mode, and vice versa. For detailed information, please refer to Chapter [46 USB Serial/JTAG Controller \(USB\\_SERIAL\\_JTAG\)](#).

You can set eFuse bit EFUSE\_DIS\_USB\_SERIAL\_JTAG\_DOWNLOAD\_MODE to disable USB Serial/JTAG Controller from force switching to Joint Download Boot mode.

### 10.2.3 ROM Messages Printing Control

During early SPI Boot process, the messages by the ROM code can be printed to:

- (Default) UART0 and USB Serial/JTAG controller
- UART0
- USB Serial/JTAG controller

[EFUSE\\_UART\\_PRINT\\_CONTROL](#) and GPIO36 control ROM messages printing to **UART0** as shown in Table 10.2-3 ROM Message Printing Control.

Table 10.2-3. ROM Message Printing Control

| eFuse <sup>1</sup> | GPIO36         | ROM Code Printing |
|--------------------|----------------|-------------------|
| 0                  | x <sup>2</sup> | Always enabled    |
| 1                  | 0              | Enabled           |
|                    | 1              | Disabled          |
| 2                  | 0              | Disabled          |
|                    | 1              | Enabled           |
| 3                  | x              | Always disabled   |

<sup>1</sup> eFuse: [EFUSE\\_UART\\_PRINT\\_CONTROL](#)

<sup>2</sup> x: values that have no effect on the result and can therefore be ignored.

[EFUSE\\_DIS\\_USB\\_SERIAL\\_JTAG\\_ROM\\_PRINT](#) controls the printing to **USB Serial/JTAG controller**. When this bit is 1, printing to USB Serial/JTAG controller is disabled. When this bit is 0, and USB Serial/JTAG controller is enabled via [EFUSE\\_DIS\\_USB\\_SERIAL\\_JTAG](#), ROM messages can be printed to USB Serial/JTAG controller.

Note that if [EFUSE\\_DIS\\_USB\\_SERIAL\\_JTAG\\_ROM\\_PRINT](#) is set to 0 to print to USB, but USB Serial/JTAG Controller has been disabled, then ROM messages will not be printed to USB Serial/JTAG Controller.

## 10.2.4 JTAG Signal Source Control

GPIO34 controls the source of JTAG signals during the early boot process. This GPIO is used together with [EFUSE\\_DIS\\_PAD\\_JTAG](#), [EFUSE\\_DIS\\_USB\\_JTAG](#), and [EFUSE\\_JTAG\\_SEL\\_ENABLE](#). See Table 10.2-4.

Table 10.2-4. JTAG Signal Source Control

| eFuse 1 <sup>a</sup> | eFuse 2 <sup>b</sup> | eFuse 3 <sup>c</sup> | GPIO34         | Signal Source   |
|----------------------|----------------------|----------------------|----------------|---|
| 0                    | 0                    | 0                    | x <sup>d</sup> | JTAG signals come from USB Serial/JTAG Controller.                    |
|                      |                      | 1                    | 0              | JTAG signals come from corresponding pins MTDI, MTCK, MTMS, and MTDO. |
|                      |                      |                      | 1              | JTAG signals come from USB Serial/JTAG Controller.                    |
| 0                    | 1                    | x                    | x              | JTAG signals come from corresponding pins MTDI, MTCK, MTMS, and MTDO. |
| 1                    | 0                    | x                    | x              | JTAG signals come from USB Serial/JTAG Controller.                    |
| 1                    | 1                    | x                    | x              | JTAG is disabled.   |

<sup>a</sup> eFuse 1: [EFUSE\\_DIS\\_PAD\\_JTAG](#)

<sup>b</sup> eFuse 2: [EFUSE\\_DIS\\_USB\\_JTAG](#)

<sup>c</sup> eFuse 3: [EFUSE\\_JTAG\\_SEL\\_ENABLE](#)

<sup>d</sup> x: values that have no effect on the result and can therefore be ignored.

# Chapter 11

## Interrupt Matrix

### 11.1 Overview

The interrupt matrix embedded in ESP32-P4 independently routes peripheral interrupt sources to the ESP-RISC-V CPU's peripheral interrupts to timely inform HP CPU0 or HP CPU1 to process the coming interrupts.

Peripheral interrupt sources must be routed to HP CPU0/HP CPU1 peripheral interrupts via this interrupt matrix due to the following considerations:

- ESP32-P4 has 126 peripheral interrupt sources. To map them to 32 HP CPU0 interrupts or 32 HP CPU1 interrupts, this matrix is needed.
- Through this matrix, one peripheral interrupt source can be mapped to multiple HP CPU0 interrupts or HP CPU1 interrupts according to application requirements.

**Note:**

This chapter focuses on how to map peripheral interrupt sources to HP CPU0/HP CPU1 interrupts. For more details about interrupt configuration, vector, and interrupt handling operations recommended by the ISA, please refer to Chapter 1 *High-Performance CPU [to be added later]*.

### 11.2 Interrupt Terminology in ESP32-P4

The following terms related to interrupts are defined in the context of the *ESP32-P4 Technical Reference Manual* to help readers better understand this document:

#### 11.2.1 Interrupt

An interrupt refers to the event or condition that occurs, causing the CPU to temporarily suspend its current execution and handle a higher-priority task. It is a mechanism that allows the CPU to respond to specific events promptly.

The *ESP32-P4 Technical Reference Manual* may use the term “interrupt” in a broader sense to refer to both interrupt signal and interrupt source.

#### 11.2.2 Interrupt Signal/interrupt Source

Interrupt signal and interrupt source are only defined from different perspectives and mean the same thing.

From the perspective of peripherals, interrupt signals are generated by the peripheral's internal interrupt sources and are sent to the interrupt matrix.

From the perspective of the interrupt matrix, it receives the interrupt signals sent from the peripheral and considers them interrupt sources. The interrupt matrix then outputs CPU peripheral interrupt signals to the CPU.

From the perspective of the CPU, the interrupt signals from the interrupt matrix become sources and are sent to the CPU core together with the core local interrupt sources.

### 11.2.3 Interrupt Flow in ESP32-P4

Figure 11.2-1 shows the interrupt flow in ESP32-P4.

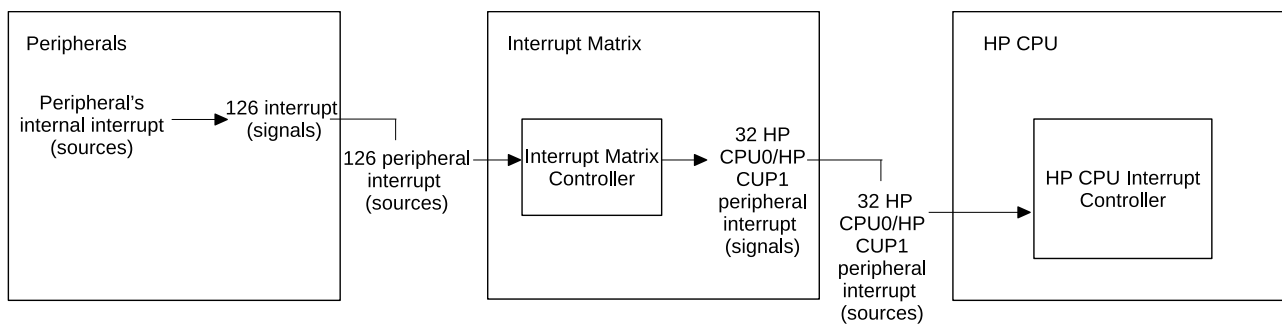


Figure 11.2-1. Interrupt Flow in ESP32-P4

## 11.3 Features

The interrupt matrix embedded in ESP32-P4 has the following features:

- 126 peripheral interrupt sources accepted as input
- 32 HP CPU0 peripheral interrupts and 32 HP CPU1 peripheral interrupts generated to HP CPU as output
- Current interrupt status query of peripheral interrupt sources
- Multiple interrupt sources mapping to a single HP CPU0 or HP CPU1 interrupt (i.e., shared interrupts)

Figure 11.3-1 shows the structure of the interrupt matrix.

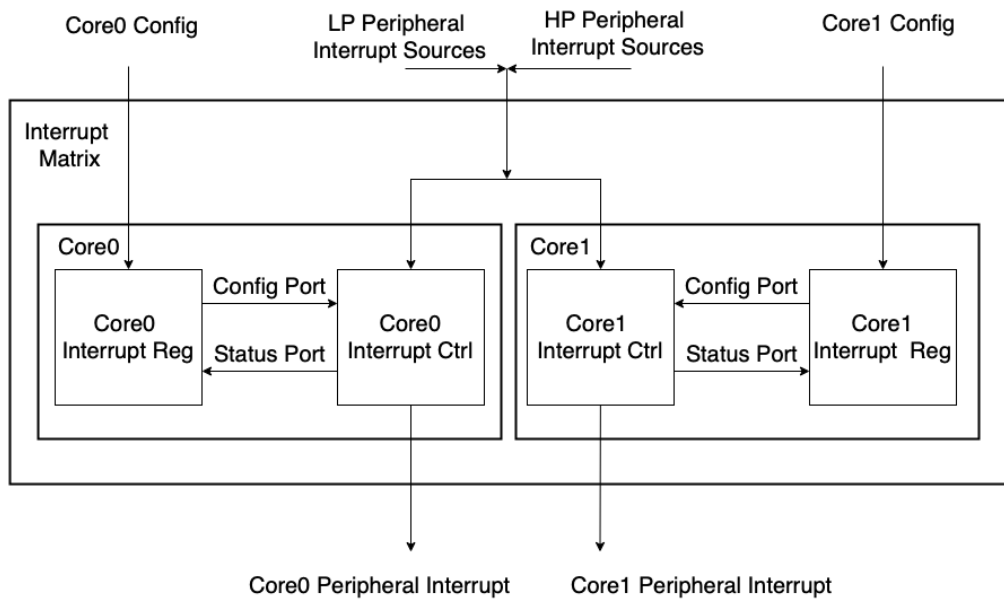


Figure 11.3-1. Interrupt Matrix Structure

All the interrupts generated by the peripheral interrupt sources can be handled by HP CPU0 or HP CPU1. Users can configure [HP CPU0 interrupt registers](#) (“Core0 Interrupt Reg” module in Figure 11.3-1) to assign peripheral interrupt sources to HP CPU0, or configure [HP CPU1 interrupt registers](#) (“Core1 Interrupt Reg” module in Figure 11.3-1) to assign peripheral interrupt sources to HP CPU1. Peripheral interrupt sources can be assigned both to HP CPU0 and HP CPU1 simultaneously, and if so, HP CPU0 and HP CPU1 will both accept the interrupts.

## 11.4 Functional Description

### 11.4.1 Peripheral Interrupt Sources

ESP32-P4 has 126 peripheral interrupt sources in total. Table 11.4-1 lists all these sources and their mapping/status registers.

- Column “No.”: Peripheral interrupt source number, can be 0 ~ 98, 100 ~ 111, 113 ~ 127 (99 and 112 are reserved).
- Column “Chapter”: in which chapter the interrupt source is described in detail.
- Column “Interrupt Source”: Name of the peripheral interrupt source.
- Column “Interrupt Source Mapping Register”: Registers used for routing the peripheral interrupt sources to HP CPU peripheral interrupts.
- Column “Interrupt Status Register”: Registers used for indicating the interrupt status of peripheral interrupt sources.
  - Column “Interrupt Status Register - Bit”: Bit position in status register, indicating the interrupt status.
  - Column “Interrupt Status Register - Name”: Name of status registers.

The register in column “Interrupt Source Mapping Register” and in column “Interrupt Status Register” correspond to the peripheral interrupt source in column “Interrupt Source”. For example, the interrupt source

mapping register for interrupt source RMT\_INTR is `COREx_RMT_INT_MAP_REG`, and its status register is `COREx_INTR_STATUS_REG_1_REG`.

Note that CORE<sub>x</sub> in the table can be CORE0 (HP CPU0) or CORE1 (HP CPU1).

Table 11.4-1. CPU Peripheral Interrupt Source Mapping/Status Registers and Peripheral Interrupt Sources

| No. | Chapter  | Interrupt Source    | Interrupt Source Mapping Register                | Interrupt Status Register |   |
|-----|--|---------------------|--|---------------------------|---|
|     |  |                     |  | Bit                       | Name  |
| 0   | <a href="#">RTC Timer</a>                                    | LP_RTC_INTR         | <a href="#">COREx_LP_RTC_INT_MAP_REG</a>         | 0                         | <a href="#">COREx_INTR_STATUS_REG_O_REG</a> |
| 1   | <a href="#">Watchdog Timers (WDT)</a>                        | LP_WDT_INTR         | <a href="#">COREx_LP_WDT_INT_MAP_REG</a>         | 1                         |   |
| 2   | <a href="#">RTC Timer</a>                                    | LP_TIMER_REG_O_INTR | <a href="#">COREx_LP_TIMER_REG_O_INT_MAP_REG</a> | 2                         |   |
| 3   | <a href="#">RTC Timer</a>                                    | LP_TIMER_REG_1_INTR | <a href="#">COREx_LP_TIMER_REG_1_INT_MAP_REG</a> | 3                         |   |
| 4   | <a href="#">LP Mailbox</a>                                   | MB_LP_INTR          | <a href="#">COREx_MB_LP_INT_MAP_REG</a>          | 4                         |   |
| 5   | <a href="#">LP Mailbox</a>                                   | MB_HP_INTR          | <a href="#">COREx_MB_LP_INT_MAP_REG</a>          | 5                         |   |
| 6   | <a href="#">Low-Power Management</a>                         | PMU_REG_O_INTR      | <a href="#">COREx_PMU_REG_O_INT_MAP_REG</a>      | 6                         |   |
| 7   | <a href="#">Low-Power Management</a>                         | PMU_REG_1_INTR      | <a href="#">COREx_PMU_REG_1_INT_MAP_REG</a>      | 7                         |   |
| 8   | <a href="#">Brown-out Detector</a>                           | LP_ANAPERI_INTR     | <a href="#">COREx_PMU_REG_O_INT_MAP_REG</a>      | 8                         |   |
| 9   | <a href="#">ADC Controller (ADC)</a>                         | LP_ADC_INTR         | <a href="#">COREx_PMU_REG_O_INT_MAP_REG</a>      | 9                         |   |
| 10  | <a href="#">GPIO Matrix and IO MUX</a>                       | LP_GPIO_INTR        | <a href="#">COREx_LP_GPIO_INT_MAP_REG</a>        | 10                        |   |
| 11  | <a href="#">I2C Controller (I2C)</a>                         | LP_I2C_INTR         | <a href="#">COREx_LP_I2C_INT_MAP_REG</a>         | 11                        |   |
| 12  | <a href="#">I2S Controller (I2S)</a>                         | LP_I2S_INTR         | <a href="#">COREx_LP_I2S_INT_MAP_REG</a>         | 12                        |   |
| 13  | <a href="#">SPI Controller (SPI)</a>                         | LP_SPI_INTR         | <a href="#">COREx_LP_SPI_INT_MAP_REG</a>         | 13                        |   |
| 14  | <a href="#">Touch Sensor (TOUCH)</a>                         | LP_TOUCH_INTR       | <a href="#">COREx_LP_TOUCH_INT_MAP_REG</a>       | 14                        |   |
| 15  | <a href="#">Temperature Sensor (TSENS)</a>                   | LP_TSENS_INTR       | <a href="#">COREx_LP_TSENS_INT_MAP_REG</a>       | 15                        |   |
| 16  | <a href="#">UART Controller (UART)</a>                       | LP_UART_INTR        | <a href="#">COREx_LP_UART_INT_MAP_REG</a>        | 16                        |   |
| 17  | <a href="#">eFuse Controller</a>                             | LP_EFUSE_INTR       | <a href="#">COREx_LP_EFUSE_INT_MAP_REG</a>       | 17                        |   |
| 18  | <a href="#">Low-Power CPU</a>                                | LP_SW_INTR          | <a href="#">COREx_LP_SW_INT_MAP_REG</a>          | 18                        |   |
| 19  | <a href="#">System Registers [to be added later]</a>         | LP_SYSREG_INTR      | <a href="#">COREx_LP_SYSREG_INT_MAP_REG</a>      | 19                        |   |
| 20  | n/a  | reserved            | reserved   | 20                        |   |
| 21  | <a href="#">System Registers [to be added later]</a>         | SYS_ICM_INTR        | <a href="#">COREx_SYS_ICM_INT_MAP_REG</a>        | 21                        |   |
| 22  | <a href="#">USB Serial/JTAG Controller (USB_SERIAL_JTAG)</a> | USB_DEVICE_INTR     | <a href="#">COREx_USB_DEVICE_INT_MAP_REG</a>     | 22                        |   |
| 23  | <a href="#">SD/MMC Host Controller (SDHOST)</a>              | SDIO_HOST_INTR      | <a href="#">COREx_SDIO_HOST_INT_MAP_REG</a>      | 23                        |   |
| 24  | <a href="#">VDMA Controller (VDMA)</a>                       | GDMA_INTR           | <a href="#">COREx_GDMA_INT_MAP_REG</a>           | 24                        |   |
| 25  | <a href="#">SPI Controller (SPI)</a>                         | SPI2_INTR           | <a href="#">COREx_SPI2_INT_MAP_REG</a>           | 25                        |   |
| 26  | <a href="#">SPI Controller (SPI)</a>                         | SPI3_INTR           | <a href="#">COREx_SPI3_INT_MAP_REG</a>           | 26                        |   |
| 27  | <a href="#">I2S Controller (I2S)</a>                         | I2S0_INTR           | <a href="#">COREx_I2S0_INT_MAP_REG</a>           | 27                        |   |
| 28  | <a href="#">I2S Controller (I2S)</a>                         | I2S1_INTR           | <a href="#">COREx_I2S1_INT_MAP_REG</a>           | 28                        |   |
| 29  | <a href="#">I2S Controller (I2S)</a>                         | I2S2_INTR_O         | <a href="#">COREx_I2S2_INT_MAP_REG</a>           | 29                        |   |
| 30  | <a href="#">UART Controller (UART)</a>                       | UHCIO_INTR          | <a href="#">COREx_UHCIO_INT_MAP_REG</a>          | 30                        |   |
| 31  | <a href="#">UART Controller (UART)</a>                       | UARTO_INTR          | <a href="#">COREx_UARTO_INT_MAP_REG</a>          | 31                        |   |



| No. | Chapter  | Interrupt Source      | Interrupt Source Mapping Register                  | Interrupt Status Register |   |
|-----|--|-----------------------|--|---------------------------|---|
|     |  |                       |  | Bit                       | Name  |
| 32  | <a href="#">UART Controller (UART)</a>               | UART1_INTR            | <a href="#">COREx_UART1_INT_MAP_REG</a>            | 0                         | <a href="#">COREx_INTR_STATUS_REG_1_REG</a> |
| 33  | <a href="#">UART Controller (UART)</a>               | UART2_INTR            | <a href="#">COREx_UART2_INT_MAP_REG</a>            | 1                         |   |
| 34  | <a href="#">UART Controller (UART)</a>               | UART3_INTR            | <a href="#">COREx_UART3_INT_MAP_REG</a>            | 2                         |   |
| 35  | <a href="#">UART Controller (UART)</a>               | UART4_INTR            | <a href="#">COREx_UART4_INT_MAP_REG</a>            | 3                         |   |
| 36  | <a href="#">LCD and Camera Controller (LCD_CAM)</a>  | LCD_CAM_INTR          | <a href="#">COREx_LCD_CAM_INT_MAP_REG</a>          | 4                         |   |
| 37  | <a href="#">ADC Controller (ADC)</a>                 | ADC_INTR              | <a href="#">COREx_ADC_INT_MAP_REG</a>              | 5                         |   |
| 38  | <a href="#">Motor Control PWM (MCPWM)</a>            | PWM0_INTR             | <a href="#">COREx_PWM0_INT_MAP_REG</a>             | 6                         |   |
| 39  | <a href="#">Motor Control PWM (MCPWM)</a>            | PWM1_INTR             | <a href="#">COREx_PWM1_INT_MAP_REG</a>             | 7                         |   |
| 40  | <a href="#">Two-Wire Automotive Interface (TWAI)</a> | TWAI0_INTR            | <a href="#">COREx_TWAI0_INT_MAP_REG</a>            | 8                         |   |
| 41  | <a href="#">Two-Wire Automotive Interface (TWAI)</a> | TWAI1_INTR            | <a href="#">COREx_TWAI1_INT_MAP_REG</a>            | 9                         |   |
| 42  | <a href="#">Two-Wire Automotive Interface (TWAI)</a> | TWAI2_INTR            | <a href="#">COREx_TWAI2_INT_MAP_REG</a>            | 10                        |   |
| 43  | <a href="#">Remote Control Peripheral (RMT)</a>      | RMT_INTR              | <a href="#">COREx_RMT_INT_MAP_REG</a>              | 11                        |   |
| 44  | <a href="#">I2C Controller (I2C)</a>                 | I2C0_INTR             | <a href="#">COREx_I2C0_INT_MAP_REG</a>             | 12                        |   |
| 45  | <a href="#">I2C Controller (I2C)</a>                 | I2C1_INTR             | <a href="#">COREx_I2C1_INT_MAP_REG</a>             | 13                        |   |
| 46  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRPO_TO_INTR     | <a href="#">COREx_TIMRTGRPO_TO_INT_MAP_REG</a>     | 14                        |   |
| 47  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRPO_T1_INTR     | <a href="#">COREx_TIMERGRPO_T1_INT_MAP_REG</a>     | 15                        |   |
| 48  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRPO_WDT_INTR    | <a href="#">COREx_TIMERGRPO_WDT_INT_MAP_REG</a>    | 16                        |   |
| 49  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRP1_TO_INTR     | <a href="#">COREx_TIMRTGRP1_TO_INT_MAP_REG</a>     | 17                        |   |
| 50  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRP1_T1_INTR     | <a href="#">COREx_TIMERGRP1_T1_INT_MAP_REG</a>     | 18                        |   |
| 51  | <a href="#">Timer Group (TIMG)</a>                   | TIMERGRP1_WDT_INTR    | <a href="#">COREx_TIMERGRP1_WDT_INT_MAP_REG</a>    | 19                        |   |
| 52  | <a href="#">LED PWM Controller (LEDC)</a>            | LEDC_INTR             | <a href="#">COREx_LEDC_INTR</a>                    | 20                        |   |
| 53  | <a href="#">System Timer</a>                         | SYSTIMER_TARGET0_INTR | <a href="#">COREx_SYSTIMER_TARGET0_INTR</a>        | 21                        |   |
| 54  | <a href="#">System Timer</a>                         | SYSTIMER_TARGET1_INTR | <a href="#">COREx_SYSTIMER_TARGET1_INTR</a>        | 22                        |   |
| 55  | <a href="#">System Timer</a>                         | SYSTIMER_TARGET2_INTR | <a href="#">COREx_SYSTIMER_TARGET2_INTR</a>        | 23                        |   |
| 56  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_IN_CHO_INTR  | <a href="#">COREx_AHB_PDMA_IN_CHO_INT_MAP_REG</a>  | 24                        |   |
| 57  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_IN_CH1_INTR  | <a href="#">COREx_AHB_PDMA_IN_CH1_INT_MAP_REG</a>  | 25                        |   |
| 58  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_IN_CH2_INTR  | <a href="#">COREx_AHB_PDMA_IN_CH2_INT_MAP_REG</a>  | 26                        |   |
| 59  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_OUT_CHO_INTR | <a href="#">COREx_AHB_PDMA_OUT_CHO_INT_MAP_REG</a> | 27                        |   |
| 60  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_OUT_CH1_INTR | <a href="#">COREx_AHB_PDMA_OUT_CH1_INT_MAP_REG</a> | 28                        |   |
| 61  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AHB_PDMA_OUT_CH2_INTR | <a href="#">COREx_AHB_PDMA_OUT_CH2_INT_MAP_REG</a> | 29                        |   |
| 62  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AXI_PDMA_IN_CHO_INTR  | <a href="#">COREx_AXI_PDMA_IN_CHO_INT_MAP_REG</a>  | 30                        |   |
| 63  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a> | AXI_PDMA_IN_CH1_INTR  | <a href="#">COREx_AXI_PDMA_IN_CH1_INT_MAP_REG</a>  | 31                        |   |

| No. | Chapter  | Interrupt Source             | Interrupt Source Mapping Register                         | Interrupt Status Register |   |
|-----|--|------------------------------|---|---------------------------|---|
|     |  |                              |   | Bit                       | Name  |
| 64  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a>               | AXI_PDMA_IN_CH2_INTR         | <a href="#">COREx_AXI_PDMA_IN_CH2_INT_MAP_REG</a>         | 0                         | <a href="#">COREx_INTR_STATUS_REG_2_REG</a> |
| 65  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a>               | AXI_PDMA_OUT_CHO_INTR        | <a href="#">COREx_AXI_PDMA_OUT_CHO_INT_MAP_REG</a>        | 1                         |   |
| 66  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a>               | AXI_PDMA_OUT_CH1_INTR        | <a href="#">COREx_AXI_PDMA_OUT_CH1_INT_MAP_REG</a>        | 2                         |   |
| 67  | <a href="#">GDMA Controller (GDMA-AHB, GDMA-AXI)</a>               | AXI_PDMA_OUT_CH2_INTR        | <a href="#">COREx_AXI_PDMA_OUT_CH2_INT_MAP_REG</a>        | 3                         |   |
| 68  | <a href="#">RSA Accelerator (RSA)</a>                              | RSA_INTR                     | <a href="#">COREx_RSA_INT_MAP_REG</a>                     | 4                         |   |
| 69  | <a href="#">AES Accelerator (AES)</a>                              | AES_INTR                     | <a href="#">COREx_AES_INT_MAP_REG</a>                     | 5                         |   |
| 70  | <a href="#">SHA Accelerator (SHA)</a>                              | SHA_INTR                     | <a href="#">COREx_SHA_INT_MAP_REG</a>                     | 6                         |   |
| 71  | <a href="#">SHA Accelerator (SHA)</a>                              | ECC_INTR                     | <a href="#">COREx_ECC_INT_MAP_REG</a>                     | 7                         |   |
| 72  | <a href="#">Elliptic Curve Digital Signature Algorithm (ECDSA)</a> | ECDSA_INTR                   | <a href="#">COREx_ECDSA_INT_MAP_REG</a>                   | 8                         |   |
| 73  | n/a  | reserved                     | reserved  | 9                         |   |
| 74  | <a href="#">GPIO Matrix and IO MUX</a>                             | GPIO_INTRO                   | <a href="#">COREx_GPIO_INTRO_MAP_REG</a>                  | 10                        |   |
| 75  | <a href="#">GPIO Matrix and IO MUX</a>                             | GPIO_INTR1                   | <a href="#">COREx_GPIO_INTR1_MAP_REG</a>                  | 11                        |   |
| 76  | <a href="#">GPIO Matrix and IO MUX</a>                             | GPIO_INTR2                   | <a href="#">COREx_GPIO_INTR2_MAP_REG</a>                  | 12                        |   |
| 77  | <a href="#">GPIO Matrix and IO MUX</a>                             | GPIO_INTR3                   | <a href="#">COREx_GPIO_INTR3_MAP_REG</a>                  | 13                        |   |
| 78  | <a href="#">GPIO Matrix and IO MUX</a>                             | GPIO_PAD_COMP_INTR           | <a href="#">COREx_GPIO_PAD_COMP_INT_MAP_REG</a>           | 14                        |   |
| 79  | <a href="#">System Registers [to be added later]</a>               | CPU_INTR_FROM_CPU_0          | <a href="#">COREx_CPU_INTR_FROM_CPU_0_MAP_REG</a>         | 15                        |   |
| 80  | <a href="#">System Registers [to be added later]</a>               | CPU_INTR_FROM_CPU_1          | <a href="#">COREx_CPU_INTR_FROM_CPU_1_MAP_REG</a>         | 16                        |   |
| 81  | <a href="#">System Registers [to be added later]</a>               | CPU_INTR_FROM_CPU_2          | <a href="#">COREx_CPU_INTR_FROM_CPU_2_MAP_REG</a>         | 17                        |   |
| 82  | <a href="#">System Registers [to be added later]</a>               | CPU_INTR_FROM_CPU_3          | <a href="#">COREx_CPU_INTR_FROM_CPU_3_MAP_REG</a>         | 18                        |   |
| 83  | n/a  | reserved                     | reserved  | 19                        |   |
| 84  | <a href="#">SPI Controller (SPI)</a>                               | FLASH_MSPI_INTR              | <a href="#">COREx_FLASH_MSPI_INT_MAP_REG</a>              | 20                        | <a href="#">COREx_INTR_STATUS_REG_3_REG</a> |
| 85  | <a href="#">MIPI CSI</a>   | CSI_BRIDGE_INTR              | <a href="#">COREx_CSI_BRIDGE_INT_MAP_REG</a>              | 21                        |   |
| 86  | <a href="#">MIPI DSI [to be added later]</a>                       | DSI_BRIDGE_INTR              | <a href="#">COREx_DSI_BRIDGE_INT_MAP_REG</a>              | 22                        |   |
| 87  | <a href="#">MIPI CSI</a>   | CSI_INTR                     | <a href="#">COREx_CSI_INT_MAP_REG</a>                     | 23                        |   |
| 88  | <a href="#">MIPI DSI [to be added later]</a>                       | DSI_INTR                     | <a href="#">COREx_DSI_INT_MAP_REG</a>                     | 24                        |   |
| 89  | <a href="#">Ethernet Media Access Controller (EMAC)</a>            | GMII_PHY_INTR                | <a href="#">COREx_GMII_PHY_INT_MAP_REG</a>                | 25                        |   |
| 90  | <a href="#">Ethernet Media Access Controller (EMAC)</a>            | LPI_INTR                     | <a href="#">COREx_LPI_INT_MAP_REG</a>                     | 26                        |   |
| 91  | <a href="#">Ethernet Media Access Controller (EMAC)</a>            | PMT_INTR                     | <a href="#">COREx_PMT_INT_MAP_REG</a>                     | 27                        |   |
| 92  | <a href="#">Ethernet Media Access Controller (EMAC)</a>            | ETH_MAC_INTR                 | <a href="#">COREx_ETH_MAC_INT_MAP_REG</a>                 | 28                        |   |
| 93  | <a href="#">USB 2.0 High-Speed OTG</a>                             | USB_OTG_INTR                 | <a href="#">COREx_USB_OTG_INT_MAP_REG</a>                 | 29                        |   |
| 94  | <a href="#">USB 2.0 High-Speed OTG</a>                             | USB_OTG_ENDP_MULTI_PROC_INTR | <a href="#">COREx_USB_OTG_ENDP_MULTI_PROC_INT_MAP_REG</a> | 30                        |   |
| 95  | <a href="#">JPEG Codec</a>   | JPEG_INTR                    | <a href="#">COREx_JPEG_INT_MAP_REG</a>                    | 31                        |   |
| 96  | <a href="#">Pixel-Processing Accelerator (PPA)</a>                 | PPA_INTR                     | <a href="#">COREx_PPA_INT_MAP_REG</a>                     | 0                         |   |
| 97  | <a href="#">RISC-V Trace Encoder (TRACE)</a>                       | CORE0_TRACE_INTR             | <a href="#">COREx_CORE0_TRACE_INT_MAP_REG</a>             | 1                         |   |

| No. | Chapter  | Interrupt Source        | Interrupt Source Mapping Register                    | Interrupt Status Register |      |
|-----|--|-------------------------|--|---------------------------|------|
|     |  |                         |  | Bit                       | Name |
| 98  | <a href="#">RISC-V Trace Encoder (TRACE)</a>         | CORE1_TRACE_INTR        | <a href="#">COREx_CORE1_TRACE_INT_MAP_REG</a>        | 2                         |      |
| 99  | n/a  | reserved                | reserved   | 3                         |      |
| 100 | <a href="#">Image Signal Processor (ISP)</a>         | ISP_INTR                | <a href="#">COREx_ISP_INT_MAP_REG</a>                | 4                         |      |
| 101 | <a href="#">I3C Controller [to be added later]</a>   | I3C_MST_INTR            | <a href="#">COREx_I3C_MST_INT_MAP_REG</a>            | 5                         |      |
| 102 | <a href="#">I3C Controller [to be added later]</a>   | I3C_SLV_INTR            | <a href="#">COREx_I3C_SLV_INT_MAP_REG</a>            | 6                         |      |
| 103 | <a href="#">USB 2.0 Full-Speed OTG</a>               | USB_OTG11_INTR          | <a href="#">COREx_USB_OTG11_INT_MAP_REG</a>          | 7                         |      |
| 104 | <a href="#">2D-DMA Controller (2D-DMA)</a>           | DMA2D_IN_CHO_INTR       | <a href="#">COREx_DMA2D_IN_CHO_INT_MAP_REG</a>       | 8                         |      |
| 105 | <a href="#">2D-DMA Controller (2D-DMA)</a>           | DMA2D_IN_CH1_INTR       | <a href="#">COREx_DMA2D_IN_CH1_INT_MAP_REG</a>       | 9                         |      |
| 106 | <a href="#">2D-DMA Controller (2D-DMA)</a>           | DMA2D_OUT_CHO_INTR      | <a href="#">COREx_DMA2D_OUT_CHO_INT_MAP_REG</a>      | 10                        |      |
| 107 | <a href="#">2D-DMA Controller (2D-DMA)</a>           | DMA2D_OUT_CH1_INTR      | <a href="#">COREx_DMA2D_OUT_CH1_INT_MAP_REG</a>      | 11                        |      |
| 108 | <a href="#">2D-DMA Controller (2D-DMA)</a>           | DMA2D_OUT_CH2_INTR      | <a href="#">COREx_DMA2D_OUT_CH2_INT_MAP_REG</a>      | 12                        |      |
| 109 | <a href="#">SPI Controller (SPI)</a>                 | PSRAM_MSPI_INTR         | <a href="#">COREx_PSRAM_MSPI_INT_MAP_REG</a>         | 13                        |      |
| 110 | <a href="#">System Registers [to be added later]</a> | HP_SYSREG_INTR          | <a href="#">COREx_HP_SYSREG_INT_MAP_REG</a>          | 14                        |      |
| 111 | <a href="#">Pulse Count Controller (PCNT)</a>        | PCNT_INTR               | <a href="#">COREx_PCNT_INT_MAP_REG</a>               | 15                        |      |
| 112 | n/a  | reserved                | reserved   | 16                        |      |
| 113 | <a href="#">Parallel IO Controller (PARLIO)</a>      | HP_PARLIO_RX_INTR       | <a href="#">COREx_HP_PARLIO_RX_INT_MAP_REG</a>       | 17                        |      |
| 114 | <a href="#">Parallel IO Controller (PARLIO)</a>      | HP_PARLIO_TX_INTR       | <a href="#">COREx_HP_PARLIO_TX_INT_MAP_REG</a>       | 18                        |      |
| 115 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_OUT_CHO_INTR | <a href="#">COREx_H264_DMA2D_OUT_CHO_INT_MAP_REG</a> | 19                        |      |
| 116 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_OUT_CH1_INTR | <a href="#">COREx_H264_DMA2D_OUT_CH1_INT_MAP_REG</a> | 20                        |      |
| 117 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_OUT_CH2_INTR | <a href="#">COREx_H264_DMA2D_OUT_CH2_INT_MAP_REG</a> | 21                        |      |
| 118 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_OUT_CH3_INTR | <a href="#">COREx_H264_DMA2D_OUT_CH3_INT_MAP_REG</a> | 22                        |      |
| 119 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_OUT_CH4_INTR | <a href="#">COREx_H264_DMA2D_OUT_CH4_INT_MAP_REG</a> | 23                        |      |
| 120 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CHO_INTR  | <a href="#">COREx_H264_DMA2D_IN_CHO_INT_MAP_REG</a>  | 24                        |      |
| 121 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CH1_INTR  | <a href="#">COREx_H264_DMA2D_IN_CH1_INT_MAP_REG</a>  | 25                        |      |
| 122 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CH2_INTR  | <a href="#">COREx_H264_DMA2D_IN_CH2_INT_MAP_REG</a>  | 26                        |      |
| 123 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CH3_INTR  | <a href="#">COREx_H264_DMA2D_IN_CH3_INT_MAP_REG</a>  | 27                        |      |
| 124 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CH4_INTR  | <a href="#">COREx_H264_DMA2D_IN_CH4_INT_MAP_REG</a>  | 28                        |      |
| 125 | <a href="#">H264 Encoder [to be added later]</a>     | H264_DMA2D_IN_CH5_INTR  | <a href="#">COREx_H264_DMA2D_IN_CH5_INT_MAP_REG</a>  | 29                        |      |
| 126 | <a href="#">H264 Encoder [to be added later]</a>     | H264_REG_INTR           | <a href="#">COREx_H264_REG_INT_MAP_REG</a>           | 30                        |      |
| 127 | <a href="#">Debug Assistant</a>                      | ASSIST_DEBUG_INTR       | <a href="#">COREx_ASSIST_DEBUG_INT_MAP_REG</a>       | 31                        |      |

## 11.4.2 Assign Peripheral Interrupt Source to HP CPU Interrupt

In this section, the following terms are used to describe the operation of the interrupt matrix.

- Source\_*Y*: stands for a peripheral interrupt source, wherein *Y* means the number of this interrupt source in Table 11.4-1.
- CORE<sub>x</sub>\_SOURCE\_*Y*\_MAP\_REG: stands for an interrupt source mapping register for the peripheral interrupt source (Source\_*Y*) of HP CPU<sub>x</sub>.
- Num\_P: the index of HP CPU interrupts which can be 16 ~ 47.
- Interrupt\_P: stands for the HP CPU interrupt numbered as Num\_P.

### 11.4.2.1 Assign One Peripheral Interrupt Source (Source\_*Y*) to HP CPU<sub>x</sub>

Setting the corresponding source mapping register CORE<sub>x</sub>\_SOURCE\_*Y*\_MAP\_REG of Source\_*Y* to Num\_P assigns this interrupt source to Interrupt\_P.

### 11.4.2.2 Assign Multiple Peripheral Interrupt Sources (Source\_*Y*) to HP CPU<sub>x</sub>

Setting the corresponding source mapping register CORE<sub>x</sub>\_SOURCE\_*Y*\_MAP\_REG of each interrupt source to the same Num\_P assigns multiple sources to the same Interrupt\_P of HP CPU<sub>x</sub>. Any of these sources can trigger CPU Interrupt\_P of HP CPU<sub>x</sub>. In other words, the CPU Interrupt\_p will be shared between these interrupt sources. When an interrupt signal is generated, HP CPU<sub>x</sub> should check the interrupt status registers to figure out which peripheral generated the interrupt. For more information, see Chapter 1 *High-Performance CPU [to be added later]*.

### 11.4.2.3 Disable HP CPU<sub>x</sub> Peripheral Interrupt Source (Source\_*x*)

Writing 0 to the CORE<sub>x</sub>\_SOURCE\_*Y*\_MAP\_REG register disables the corresponding interrupt source.

## 11.4.3 Query Current Interrupt Status of HP CPU<sub>x</sub> Peripheral Interrupt Source

After enabling peripheral interrupt sources, users can query current interrupt status of HP CPU<sub>x</sub> peripheral interrupt source by reading the bit value in CORE<sub>x</sub>\_INTR\_STATUS\_*n* (read only). For the mapping between CORE<sub>x</sub>\_INTR\_STATUS\_*n* and peripheral interrupt sources, please refer to Table 11.4-1.

## 11.5 Register Summary

The addresses in this section are relative to the interrupt matrix HP CPU0/HP CPU1 base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

### 11.5.1 HP CPU0 Interrupt Matrix Register Summary

| Name   | Description                          | Address | Access |
|--|--------------------------------------|---------|--------|
| <b>CORE0 LP RTC INT MAP REG</b>                  |                                      |         |        |
| <a href="#">CORE0_LP_RTC_INT_MAP_REG</a>         | LP_RTC_INTR mapping register         | 0x0000  | R/W    |
| <b>CORE0 LP WDT INT MAP REG</b>                  |                                      |         |        |
| <a href="#">CORE0_LP_WDT_INT_MAP_REG</a>         | LP_WDT_INTR mapping register         | 0x0004  | R/W    |
| <b>CORE0 LP TIMER REG 0 INT MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_LP_TIMER_REG_0_INT_MAP_REG</a> | LP_TIMER_REG_0_INTR mapping register | 0x0008  | R/W    |
| <b>CORE0 LP TIMER REG 1 INT MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_LP_TIMER_REG_1_INT_MAP_REG</a> | LP_TIMER_REG_1_INTR mapping register | 0x000C  | R/W    |
| <b>CORE0 MB HP INT MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_MB_HP_INT_MAP_REG</a>          | MB_HP_INTR mapping register          | 0x0010  | R/W    |
| <b>CORE0 MB LP INT MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_MB_LP_INT_MAP_REG</a>          | MB_LP_INTR mapping register          | 0x0014  | R/W    |
| <b>CORE0 PMU REG 0 INT MAP REG</b>               |                                      |         |        |
| <a href="#">CORE0_PMU_REG_0_INT_MAP_REG</a>      | PMU_REG_0_INTR mapping register      | 0x0018  | R/W    |
| <b>CORE0 PMU REG 1 INT MAP REG</b>               |                                      |         |        |
| <a href="#">CORE0_PMU_REG_1_INT_MAP_REG</a>      | PMU_REG_1_INTR mapping register      | 0x001C  | R/W    |
| <b>CORE0 LP ANAPERI INT MAP REG</b>              |                                      |         |        |
| <a href="#">CORE0_LP_ANAPERI_INT_MAP_REG</a>     | LP_ANAPERI_INTR mapping register     | 0x0020  | R/W    |
| <b>CORE0 LP ADC INT MAP REG</b>                  |                                      |         |        |
| <a href="#">CORE0_LP_ADC_INT_MAP_REG</a>         | LP_ADC_INTR mapping register         | 0x0024  | R/W    |
| <b>CORE0 LP GPIO INT MAP REG</b>                 |                                      |         |        |

| Name   | Description                      | Address | Access |
|--|----------------------------------|---------|--------|
| <a href="#">CORE0_LP_GPIO_INT_MAP_REG</a>    | LP_GPIO_INTR mapping register    | 0x0028  | R/W    |
| <b>CORE0 LP I2C INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE0_LP_I2C_INT_MAP_REG</a>     | LP_I2C_INTR mapping register     | 0x002C  | R/W    |
| <b>CORE0 LP I2S INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE0_LP_I2S_INT_MAP_REG</a>     | LP_I2S_INTR mapping register     | 0x0030  | R/W    |
| <b>CORE0 LP SPI INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE0_LP_SPI_INT_MAP_REG</a>     | LP_SPI_INTR mapping register     | 0x0034  | R/W    |
| <b>CORE0 LP TOUCH INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE0_LP_TOUCH_INT_MAP_REG</a>   | LP_TOUCH_INTR mapping register   | 0x0038  | R/W    |
| <b>CORE0 LP TSENS INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE0_LP_TSENS_INT_MAP_REG</a>   | LP_TSENS_INTR mapping register   | 0x003C  | R/W    |
| <b>CORE0 LP UART INT MAP REG</b>             |                                  |         |        |
| <a href="#">CORE0_LP_UART_INT_MAP_REG</a>    | LP_UART_INTR mapping register    | 0x0040  | R/W    |
| <b>CORE0 LP EFUSE INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE0_LP_EFUSE_INT_MAP_REG</a>   | LP_EFUSE_INTR mapping register   | 0x0044  | R/W    |
| <b>CORE0 LP SW INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE0_LP_SW_INT_MAP_REG</a>      | LP_SW_INTR mapping register      | 0x0048  | R/W    |
| <b>CORE0 LP SYSREG INT MAP REG</b>           |                                  |         |        |
| <a href="#">CORE0_LP_SYSREG_INT_MAP_REG</a>  | LP_SYSREG_INTR mapping register  | 0x004C  | R/W    |
| <b>CORE0 SYS ICM INT MAP REG</b>             |                                  |         |        |
| <a href="#">CORE0_SYS_ICM_INT_MAP_REG</a>    | SYS_ICM_INTR mapping register    | 0x0054  | R/W    |
| <b>CORE0 USB DEVICE INT MAP REG</b>          |                                  |         |        |
| <a href="#">CORE0_USB_DEVICE_INT_MAP_REG</a> | USB_DEVICE_INTR mapping register | 0x0058  | R/W    |
| <b>CORE0 SDIO HOST INT MAP REG</b>           |                                  |         |        |
| <a href="#">CORE0_SDIO_HOST_INT_MAP_REG</a>  | SDIO_HOST_INTR mapping register  | 0x005C  | R/W    |
| <b>CORE0 GDMA INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE0_GDMA_INT_MAP_REG</a>       | GDMA_INTR mapping register       | 0x0060  | R/W    |
| <b>CORE0 SPI2 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE0_SPI2_INT_MAP_REG</a>       | SPI2_INTR mapping register       | 0x0064  | R/W    |

| Name                                      | Description                   | Address | Access |
|---|-------------------------------|---------|--------|
| <b>CORE0 SPI3 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_SPI3_INT_MAP_REG</a>    | SPI3_INTR mapping register    | 0x0068  | R/W    |
| <b>CORE0 I2S0 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_I2S0_INT_MAP_REG</a>    | I2S0_INTR mapping register    | 0x006C  | R/W    |
| <b>CORE0 I2S1 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_I2S1_INT_MAP_REG</a>    | I2S1_INTR mapping register    | 0x0070  | R/W    |
| <b>CORE0 I2S2 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_I2S2_INT_MAP_REG</a>    | I2S2_INTR mapping register    | 0x0074  | R/W    |
| <b>CORE0 UHCIO INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UHCIO_INT_MAP_REG</a>   | UHCIO_INTR mapping register   | 0x0078  | R/W    |
| <b>CORE0 UART0 INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UART0_INT_MAP_REG</a>   | UART0_INTR mapping register   | 0x007C  | R/W    |
| <b>CORE0 UART1 INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UART1_INT_MAP_REG</a>   | UART1_INTR mapping register   | 0x0080  | R/W    |
| <b>CORE0 UART2 INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UART2_INT_MAP_REG</a>   | UART2_INTR mapping register   | 0x0084  | R/W    |
| <b>CORE0 UART3 INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UART3_INT_MAP_REG</a>   | UART3_INTR mapping register   | 0x0088  | R/W    |
| <b>CORE0 UART4 INT MAP REG</b>            |                               |         |        |
| <a href="#">CORE0_UART4_INT_MAP_REG</a>   | UART4_INTR mapping register   | 0x008C  | R/W    |
| <b>CORE0 LCD CAM INT MAP REG</b>          |                               |         |        |
| <a href="#">CORE0_LCD_CAM_INT_MAP_REG</a> | LCD_CAM_INTR mapping register | 0x0090  | R/W    |
| <b>CORE0 ADC INT MAP REG</b>              |                               |         |        |
| <a href="#">CORE0_ADC_INT_MAP_REG</a>     | ADC_INTR mapping register     | 0x0094  | R/W    |
| <b>CORE0 PWM0 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_PWM0_INT_MAP_REG</a>    | PWM0_INTR mapping register    | 0x0098  | R/W    |
| <b>CORE0 PWM1 INT MAP REG</b>             |                               |         |        |
| <a href="#">CORE0_PWM1_INT_MAP_REG</a>    | PWM1_INTR mapping register    | 0x009C  | R/W    |
| <b>CORE0 TWAIO INT MAP REG</b>            |                               |         |        |

| Name   | Description                            | Address | Access |
|--|--|---------|--------|
| <a href="#">CORE0_TWAI0_INT_MAP_REG</a>            | TWAI0_INTR mapping register            | 0x00A0  | R/W    |
| <b>CORE0 TWAI1 INT MAP REG</b>                     |  |         |        |
| <a href="#">CORE0_TWAI1_INT_MAP_REG</a>            | TWAI1_INTR mapping register            | 0x00A4  | R/W    |
| <b>CORE0 TWAI2 INT MAP REG</b>                     |  |         |        |
| <a href="#">CORE0_TWAI2_INT_MAP_REG</a>            | TWAI2_INTR mapping register            | 0x00A8  | R/W    |
| <b>CORE0 RMT INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE0_RMT_INT_MAP_REG</a>              | RMT_INTR mapping register              | 0x00AC  | R/W    |
| <b>CORE0 I2C0 INT MAP REG</b>                      |  |         |        |
| <a href="#">CORE0_I2C0_INT_MAP_REG</a>             | I2C0_INTR mapping register             | 0x00B0  | R/W    |
| <b>CORE0 I2C1 INT MAP REG</b>                      |  |         |        |
| <a href="#">CORE0_I2C1_INT_MAP_REG</a>             | I2C1_INTR mapping register             | 0x00B4  | R/W    |
| <b>CORE0 TIMERGRPO TO INT MAP REG</b>              |  |         |        |
| <a href="#">CORE0_TIMERGRPO_TO_INT_MAP_REG</a>     | TIMERGRPO_TO_INTR mapping register     | 0x00B8  | R/W    |
| <b>CORE0 TIMERGRPO T1 INT MAP REG</b>              |  |         |        |
| <a href="#">CORE0_TIMERGRPO_T1_INT_MAP_REG</a>     | TIMERGRPO_T1_INTR mapping register     | 0x00BC  | R/W    |
| <b>CORE0 TIMERGRPO WDT INT MAP REG</b>             |  |         |        |
| <a href="#">CORE0_TIMERGRPO_WDT_INT_MAP_REG</a>    | TIMERGRPO_WDT_INTR mapping register    | 0x00C0  | R/W    |
| <b>CORE0 TIMERGRP1 TO INT MAP REG</b>              |  |         |        |
| <a href="#">CORE0_TIMERGRP1_TO_INT_MAP_REG</a>     | TIMERGRP1_TO_INTR mapping register     | 0x00C4  | R/W    |
| <b>CORE0 TIMERGRP1 T1 INT MAP REG</b>              |  |         |        |
| <a href="#">CORE0_TIMERGRP1_T1_INT_MAP_REG</a>     | TIMERGRP1_T1_INTR mapping register     | 0x00C8  | R/W    |
| <b>CORE0 TIMERGRP1 WDT INT MAP REG</b>             |  |         |        |
| <a href="#">CORE0_TIMERGRP1_WDT_INT_MAP_REG</a>    | TIMERGRP1_WDT_INTR mapping register    | 0x00CC  | R/W    |
| <b>CORE0 LEDC INT MAP REG</b>                      |  |         |        |
| <a href="#">CORE0_LEDC_INT_MAP_REG</a>             | LEDC_INTR mapping register             | 0x00D0  | R/W    |
| <b>CORE0 SYSTIMER TARGET0 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_SYSTIMER_TARGET0_INT_MAP_REG</a> | SYSTIMER_TARGET0_INTR mapping register | 0x00D4  | R/W    |
| <b>CORE0 SYSTIMER TARGET1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_SYSTIMER_TARGET1_INT_MAP_REG</a> | SYSTIMER_TARGET1_INTR mapping register | 0x00D8  | R/W    |



| Name   | Description                            | Address | Access |
|--|--|---------|--------|
| <b>CORE0 SYSTIMER TARGET2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_SYSTIMER_TARGET2_INT_MAP_REG</a> | SYSTIMER_TARGET2_INTR mapping register | 0x00DC  | R/W    |
| <b>CORE0 AHB PDMA IN CHO INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AHB_PDMA_IN_CHO_INT_MAP_REG</a>  | AHB_PDMA_IN_CHO_INTR mapping register  | 0x00E0  | R/W    |
| <b>CORE0 AHB PDMA IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AHB_PDMA_IN_CH1_INT_MAP_REG</a>  | AHB_PDMA_IN_CH1_INTR mapping register  | 0x00E4  | R/W    |
| <b>CORE0 AHB PDMA IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AHB_PDMA_IN_CH2_INT_MAP_REG</a>  | AHB_PDMA_IN_CH2_INTR mapping register  | 0x00E8  | R/W    |
| <b>CORE0 AHB PDMA OUT CHO INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AHB_PDMA_OUT_CHO_INT_MAP_REG</a> | AHB_PDMA_OUT_CHO_INTR mapping register | 0x00EC  | R/W    |
| <b>CORE0 AHB PDMA OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AHB_PDMA_OUT_CH1_INT_MAP_REG</a> | AHB_PDMA_OUT_CH1_INTR mapping register | 0x00F0  | R/W    |
| <b>CORE0 AHB PDMA OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AHB_PDMA_OUT_CH2_INT_MAP_REG</a> | AHB_PDMA_OUT_CH2_INTR mapping register | 0x00F4  | R/W    |
| <b>CORE0 AXI PDMA IN CHO INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AXI_PDMA_IN_CHO_INT_MAP_REG</a>  | AXI_PDMA_IN_CHO_INTR mapping register  | 0x00F8  | R/W    |
| <b>CORE0 AXI PDMA IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AXI_PDMA_IN_CH1_INT_MAP_REG</a>  | AXI_PDMA_IN_CH1_INTR mapping register  | 0x00FC  | R/W    |
| <b>CORE0 AXI PDMA IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_AXI_PDMA_IN_CH2_INT_MAP_REG</a>  | AXI_PDMA_IN_CH2_INTR mapping register  | 0x0100  | R/W    |
| <b>CORE0 AXI PDMA OUT CHO INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AXI_PDMA_OUT_CHO_INT_MAP_REG</a> | AXI_PDMA_OUT_CHO_INTR mapping register | 0x0104  | R/W    |
| <b>CORE0 AXI PDMA OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AXI_PDMA_OUT_CH1_INT_MAP_REG</a> | AXI_PDMA_OUT_CH1_INTR mapping register | 0x0108  | R/W    |
| <b>CORE0 AXI PDMA OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_AXI_PDMA_OUT_CH2_INT_MAP_REG</a> | AXI_PDMA_OUT_CH2_INTR mapping register | 0x010C  | R/W    |
| <b>CORE0 RSA INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE0_RSA_INT_MAP_REG</a>              | RSA_INTR mapping register              | 0x0110  | R/W    |
| <b>CORE0 AES INT MAP REG</b>                       |  |         |        |

| Name   | Description                          | Address | Access |
|--|--------------------------------------|---------|--------|
| <a href="#">CORE0_AES_INT_MAP_REG</a>            | AES_INTR mapping register            | 0x0114  | R/W    |
| <b>CORE0 SHA INT MAP REG</b>                     |                                      |         |        |
| <a href="#">CORE0_SHA_INT_MAP_REG</a>            | SHA_INTR mapping register            | 0x0118  | R/W    |
| <b>CORE0 ECC INT MAP REG</b>                     |                                      |         |        |
| <a href="#">CORE0_ECC_INT_MAP_REG</a>            | ECC_INTR mapping register            | 0x011C  | R/W    |
| <b>CORE0 ECDSA INT MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_ECDSA_INT_MAP_REG</a>          | ECDSA_INTR mapping register          | 0x0120  | R/W    |
| <b>CORE0 GPIO INTO MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_GPIO_INT0_MAP_REG</a>          | GPIO_INT0 mapping register           | 0x0128  | R/W    |
| <b>CORE0 GPIO INT1 MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_GPIO_INT1_MAP_REG</a>          | GPIO_INTR1 mapping register          | 0x012C  | R/W    |
| <b>CORE0 GPIO INT2 MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_GPIO_INT2_MAP_REG</a>          | GPIO_INTR2 mapping register          | 0x0130  | R/W    |
| <b>CORE0 GPIO INT3 MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE0_GPIO_INT3_MAP_REG</a>          | GPIO_INTR3 mapping register          | 0x0134  | R/W    |
| <b>CORE0 GPIO PAD COMP INT MAP REG</b>           |                                      |         |        |
| <a href="#">CORE0_GPIO_PAD_COMP_INT_MAP_REG</a>  | GPIO_PAD_COMP_INTR mapping register  | 0x0138  | R/W    |
| <b>CORE0 CPU INT FROM CPU 0 MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_CPU_INT_FROM_CPU_0_MAP_REG</a> | CPU_INTR_FROM_CPU_0 mapping register | 0x013C  | R/W    |
| <b>CORE0 CPU INT FROM CPU 1 MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_CPU_INT_FROM_CPU_1_MAP_REG</a> | CPU_INTR_FROM_CPU_1 mapping register | 0x0140  | R/W    |
| <b>CORE0 CPU INT FROM CPU 2 MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_CPU_INT_FROM_CPU_2_MAP_REG</a> | CPU_INTR_FROM_CPU_2 mapping register | 0x0144  | R/W    |
| <b>CORE0 CPU INT FROM CPU 3 MAP REG</b>          |                                      |         |        |
| <a href="#">CORE0_CPU_INT_FROM_CPU_3_MAP_REG</a> | CPU_INTR_FROM_CPU_3 mapping register | 0x0148  | R/W    |
| <b>CORE0 FLASH MSPI INT MAP REG</b>              |                                      |         |        |
| <a href="#">CORE0_FLASH_MSPI_INT_MAP_REG</a>     | FLASH_MSPI_INTR mapping register     | 0x0150  | R/W    |
| <b>CORE0 CSI BRIDGE INT MAP REG</b>              |                                      |         |        |
| <a href="#">CORE0_CSI_BRIDGE_INT_MAP_REG</a>     | CSI_BRIDGE_INTR mapping register     | 0x0154  | R/W    |

| Name  | Description                                   | Address | Access |
|---|---|---------|--------|
| <b>CORE0 DSI BRIDGE INT MAP REG</b>                       |   |         |        |
| <a href="#">CORE0_DSI_BRIDGE_INT_MAP_REG</a>              | DSI_BRIDGE_INTR mapping register              | 0x0158  | R/W    |
| <b>CORE0 CSI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_CSI_INT_MAP_REG</a>                     | CSI_INTR mapping register                     | 0x015C  | R/W    |
| <b>CORE0 DSI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_DSI_INT_MAP_REG</a>                     | DSI_INTR mapping register                     | 0x0160  | R/W    |
| <b>CORE0 GMII PHY INT MAP REG</b>                         |   |         |        |
| <a href="#">CORE0_GMII_PHY_INT_MAP_REG</a>                | GMII_PHY_INTR mapping register                | 0x0164  | R/W    |
| <b>CORE0 LPI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_LPI_INT_MAP_REG</a>                     | LPI_INTR mapping register                     | 0x0168  | R/W    |
| <b>CORE0 PMT INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_PMT_INT_MAP_REG</a>                     | PMT_INTR mapping register                     | 0x016C  | R/W    |
| <b>CORE0 SBD INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_ETH_MAC_INT_MAP_REG</a>                 | ETH_MAC_INTR mapping register                 | 0x0170  | R/W    |
| <b>CORE0 USB OTG INT MAP REG</b>                          |   |         |        |
| <a href="#">CORE0_USB_OTG_INT_MAP_REG</a>                 | USB_OTG_INTR mapping register                 | 0x0174  | R/W    |
| <b>CORE0 USB OTG ENDP MULTI PROC INT MAP REG</b>          |   |         |        |
| <a href="#">CORE0_USB_OTG_ENDP_MULTI_PROC_INT_MAP_REG</a> | USB_OTG_ENDP_MULTI_PROC_INTR mapping register | 0x0178  | R/W    |
| <b>CORE0 JPEG INT MAP REG</b>                             |   |         |        |
| <a href="#">CORE0_JPEG_INT_MAP_REG</a>                    | JPEG_INTR mapping register                    | 0x017C  | R/W    |
| <b>CORE0 PPA INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_PPA_INT_MAP_REG</a>                     | PPA_INTR mapping register                     | 0x0180  | R/W    |
| <b>CORE0 CORE0 TRACE INT MAP REG</b>                      |   |         |        |
| <a href="#">CORE0_CORE0_TRACE_INT_MAP_REG</a>             | CORE0_TRACE_INTR mapping register             | 0x0184  | R/W    |
| <b>CORE0 CORE1 TRACE INT MAP REG</b>                      |   |         |        |
| <a href="#">CORE0_CORE1_TRACE_INT_MAP_REG</a>             | CORE1_TRACE_INTR mapping register             | 0x0188  | R/W    |
| <b>CORE0 ISP INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE0_ISP_INT_MAP_REG</a>                     | ISP_INTR mapping register                     | 0x0190  | R/W    |

| Name   | Description                              | Address | Access |
|--|--|---------|--------|
| <b>CORE0 I3C MST INT MAP REG</b>                     |  |         |        |
| <a href="#">CORE0_I3C_MST_INT_MAP_REG</a>            | I3C_MST_INTR mapping register            | 0x0194  | R/W    |
| <b>CORE0 I3C SLV INT MAP REG</b>                     |  |         |        |
| <a href="#">CORE0_I3C_SLV_INT_MAP_REG</a>            | I3C_SLV_INTR mapping register            | 0x0198  | R/W    |
| <b>CORE0 USB OTG11 INT MAP REG</b>                   |  |         |        |
| <a href="#">CORE0_USB_OTG11_INT_MAP_REG</a>          | USB_OTG11_INTR mapping register          | 0x019C  | R/W    |
| <b>CORE0 DMA2D IN CHO INT MAP REG</b>                |  |         |        |
| <a href="#">CORE0_DMA2D_IN_CHO_INT_MAP_REG</a>       | DMA2D_IN_CHO_INTR mapping register       | 0x01A0  | R/W    |
| <b>CORE0 DMA2D IN CH1 INT MAP REG</b>                |  |         |        |
| <a href="#">CORE0_DMA2D_IN_CH1_INT_MAP_REG</a>       | DMA2D_IN_CH1_INTR mapping register       | 0x01A4  | R/W    |
| <b>CORE0 DMA2D OUT CHO INT MAP REG</b>               |  |         |        |
| <a href="#">CORE0_DMA2D_OUT_CHO_INT_MAP_REG</a>      | DMA2D_OUT_CHO_INTR mapping register      | 0x01A8  | R/W    |
| <b>CORE0 DMA2D OUT CH1 INT MAP REG</b>               |  |         |        |
| <a href="#">CORE0_DMA2D_OUT_CH1_INT_MAP_REG</a>      | DMA2D_OUT_CH1_INTR mapping register      | 0x01AC  | R/W    |
| <b>CORE0 DMA2D OUT CH2 INT MAP REG</b>               |  |         |        |
| <a href="#">CORE0_DMA2D_OUT_CH2_INT_MAP_REG</a>      | DMA2D_OUT_CH2_INTR mapping register      | 0x01B0  | R/W    |
| <b>CORE0 PSRAM MSPI INT MAP REG</b>                  |  |         |        |
| <a href="#">CORE0_PSRAM_MSPI_INT_MAP_REG</a>         | PSRAM_MSPI_INTR mapping register         | 0x01B4  | R/W    |
| <b>CORE0 HP SYSREG INT MAP REG</b>                   |  |         |        |
| <a href="#">CORE0_HP_SYSREG_INT_MAP_REG</a>          | HP_SYSREG_INTR mapping register          | 0x01B8  | R/W    |
| <b>CORE0 PCNT INT MAP REG</b>                        |  |         |        |
| <a href="#">CORE0_PCNT_INT_MAP_REG</a>               | PCNT_INTR mapping register               | 0x01BC  | R/W    |
| <b>CORE0 HP PARLIO RX INT MAP REG</b>                |  |         |        |
| <a href="#">CORE0_HP_PARLIO_RX_INT_MAP_REG</a>       | HP_PARLIO_RX_INTR mapping register       | 0x01C4  | R/W    |
| <b>CORE0 HP PARLIO TX INT MAP REG</b>                |  |         |        |
| <a href="#">CORE0_HP_PARLIO_TX_INT_MAP_REG</a>       | HP_PARLIO_TX_INTR mapping register       | 0x01C8  | R/W    |
| <b>CORE0 H264 DMA2D OUT CHO INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_H264_DMA2D_OUT_CHO_INT_MAP_REG</a> | H264_DMA2D_OUT_CHO_INTR mapping register | 0x01CC  | R/W    |

| Name   | Description                              | Address | Access |
|--|--|---------|--------|
| <b>CORE0 H264 DMA2D OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_H264_DMA2D_OUT_CH1_INT_MAP_REG</a> | H264_DMA2D_OUT_CH1_INTR mapping register | 0x01D0  | R/W    |
| <b>CORE0 H264 DMA2D OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_H264_DMA2D_OUT_CH2_INT_MAP_REG</a> | H264_DMA2D_OUT_CH2_INTR mapping register | 0x01D4  | R/W    |
| <b>CORE0 H264 DMA2D OUT CH3 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_H264_DMA2D_OUT_CH3_INT_MAP_REG</a> | H264_DMA2D_OUT_CH3_INTR mapping register | 0x01D8  | R/W    |
| <b>CORE0 H264 DMA2D OUT CH4 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE0_H264_DMA2D_OUT_CH4_INT_MAP_REG</a> | H264_DMA2D_OUT_CH4_INTR mapping register | 0x01DC  | R/W    |
| <b>CORE0 H264 DMA2D IN CH0 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH0_INT_MAP_REG</a>  | H264_DMA2D_IN_CH0_INTR mapping register  | 0x01E0  | R/W    |
| <b>CORE0 H264 DMA2D IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH1_INT_MAP_REG</a>  | H264_DMA2D_IN_CH1_INTR mapping register  | 0x01E4  | R/W    |
| <b>CORE0 H264 DMA2D IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH2_INT_MAP_REG</a>  | H264_DMA2D_IN_CH2_INTR mapping register  | 0x01E8  | R/W    |
| <b>CORE0 H264 DMA2D IN CH3 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH3_INT_MAP_REG</a>  | H264_DMA2D_IN_CH3_INTR mapping register  | 0x01EC  | R/W    |
| <b>CORE0 H264 DMA2D IN CH4 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH4_INT_MAP_REG</a>  | H264_DMA2D_IN_CH4_INTR mapping register  | 0x01F0  | R/W    |
| <b>CORE0 H264 DMA2D IN CH5 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE0_H264_DMA2D_IN_CH5_INT_MAP_REG</a>  | H264_DMA2D_IN_CH5_INTR mapping register  | 0x01F4  | R/W    |
| <b>CORE0 H264 REG INT MAP REG</b>                    |  |         |        |
| <a href="#">CORE0_H264_REG_INT_MAP_REG</a>           | H264_REG_INTR mapping register           | 0x01F8  | R/W    |
| <b>CORE0 ASSIST DEBUG INT MAP REG</b>                |  |         |        |
| <a href="#">CORE0_ASSIST_DEBUG_INT_MAP_REG</a>       | ASSIST_DEBUG_INTR mapping register       | 0x01FC  | R/W    |
| <b>CORE0 INTR STATUS REG 0 REG</b>                   |  |         |        |

| Name   | Description                                    | Address | Access |
|--|--|---------|--------|
| <a href="#">CORE0_INTR_STATUS_REG_0_REG</a>  | Status register for interrupt sources 0 ~ 31   | 0x0200  | RO     |
| <b>CORE0 INTR STATUS REG 1 REG</b>           |  |         |        |
| <a href="#">CORE0_INTR_STATUS_REG_1_REG</a>  | Status register for interrupt sources 32 ~ 63  | 0x0204  | RO     |
| <b>CORE0 INTR STATUS REG 2 REG</b>           |  |         |        |
| <a href="#">CORE0_INTR_STATUS_REG_2_REG</a>  | Status register for interrupt sources 64 ~ 95  | 0x0208  | RO     |
| <b>CORE0 INTR STATUS REG 3 REG</b>           |  |         |        |
| <a href="#">CORE0_INTR_STATUS_REG_3_REG</a>  | Status register for interrupt sources 96 ~ 127 | 0x020C  | RO     |
| <b>CORE0 CLOCK GATE REG</b>                  |  |         |        |
| <a href="#">CORE0_CLOCK_GATE_REG</a>         | Clock gating register                          | 0x0210  | R/W    |
| <b>CORE0 INTERRUPT REG DATE REG</b>          |  |         |        |
| <a href="#">CORE0_INTERRUPT_REG_DATE_REG</a> | Version control register                       | 0x03FC  | R/W    |

### 11.5.2 HP CPU1 Interrupt Matrix Register Summary

| Name   | Description                          | Address | Access |
|--|--------------------------------------|---------|--------|
| <b>CORE1 LP RTC INT MAP REG</b>                  |                                      |         |        |
| <a href="#">CORE1_LP_RTC_INT_MAP_REG</a>         | LP_RTC_INTR mapping register         | 0x0000  | R/W    |
| <b>CORE1 LP WDT INT MAP REG</b>                  |                                      |         |        |
| <a href="#">CORE1_LP_WDT_INT_MAP_REG</a>         | LP_WDT_INTR mapping register         | 0x0004  | R/W    |
| <b>CORE1 LP TIMER REG 0 INT MAP REG</b>          |                                      |         |        |
| <a href="#">CORE1_LP_TIMER_REG_0_INT_MAP_REG</a> | LP_TIMER_REG_0_INTR mapping register | 0x0008  | R/W    |
| <b>CORE1 LP TIMER REG 1 INT MAP REG</b>          |                                      |         |        |
| <a href="#">CORE1_LP_TIMER_REG_1_INT_MAP_REG</a> | LP_TIMER_REG_1_INTR mapping register | 0x000C  | R/W    |
| <b>CORE1 MB HP INT MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE1_MB_HP_INT_MAP_REG</a>          | MB_HP_INTR mapping register          | 0x0010  | R/W    |
| <b>CORE1 MB LP INT MAP REG</b>                   |                                      |         |        |
| <a href="#">CORE1_MB_LP_INT_MAP_REG</a>          | MB_LP_INTR mapping register          | 0x0014  | R/W    |
| <b>CORE1 PMU REG 0 INT MAP REG</b>               |                                      |         |        |

| Name   | Description                      | Address | Access |
|--|----------------------------------|---------|--------|
| <a href="#">CORE1_PMU_REG_O_INT_MAP_REG</a>  | PMU_REG_O_INTR mapping register  | 0x0018  | R/W    |
| <b>CORE1 PMU REG 1 INT MAP REG</b>           |                                  |         |        |
| <a href="#">CORE1_PMU_REG_1_INT_MAP_REG</a>  | PMU_REG_1_INTR mapping register  | 0x001C  | R/W    |
| <b>CORE1 LP ANAPERI INT MAP REG</b>          |                                  |         |        |
| <a href="#">CORE1_LP_ANAPERI_INT_MAP_REG</a> | LP_ANAPERI_INTR mapping register | 0x0020  | R/W    |
| <b>CORE1 LP ADC INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE1_LP_ADC_INT_MAP_REG</a>     | LP_ADC_INTR mapping register     | 0x0024  | R/W    |
| <b>CORE1 LP GPIO INT MAP REG</b>             |                                  |         |        |
| <a href="#">CORE1_LP_GPIO_INT_MAP_REG</a>    | LP_GPIO_INTR mapping register    | 0x0028  | R/W    |
| <b>CORE1 LP I2C INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE1_LP_I2C_INT_MAP_REG</a>     | LP_I2C_INTR mapping register     | 0x002C  | R/W    |
| <b>CORE1 LP I2S INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE1_LP_I2S_INT_MAP_REG</a>     | LP_I2S_INTR mapping register     | 0x0030  | R/W    |
| <b>CORE1 LP SPI INT MAP REG</b>              |                                  |         |        |
| <a href="#">CORE1_LP_SPI_INT_MAP_REG</a>     | LP_SPI_INTR mapping register     | 0x0034  | R/W    |
| <b>CORE1 LP TOUCH INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE1_LP_TOUCH_INT_MAP_REG</a>   | LP_TOUCH_INTR mapping register   | 0x0038  | R/W    |
| <b>CORE1 LP TSENS INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE1_LP_TSENS_INT_MAP_REG</a>   | LP_TSENS_INTR mapping register   | 0x003C  | R/W    |
| <b>CORE1 LP UART INT MAP REG</b>             |                                  |         |        |
| <a href="#">CORE1_LP_UART_INT_MAP_REG</a>    | LP_UART_INTR mapping register    | 0x0040  | R/W    |
| <b>CORE1 LP EFUSE INT MAP REG</b>            |                                  |         |        |
| <a href="#">CORE1_LP_EFUSE_INT_MAP_REG</a>   | LP_EFUSE_INTR mapping register   | 0x0044  | R/W    |
| <b>CORE1 LP SW INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_LP_SW_INT_MAP_REG</a>      | LP_SW_INTR mapping register      | 0x0048  | R/W    |
| <b>CORE1 LP SYSREG INT MAP REG</b>           |                                  |         |        |
| <a href="#">CORE1_LP_SYSREG_INT_MAP_REG</a>  | LP_SYSREG_INTR mapping register  | 0x004C  | R/W    |
| <b>CORE1 SYS ICM INT MAP REG</b>             |                                  |         |        |
| <a href="#">CORE1_SYS_ICM_INT_MAP_REG</a>    | SYS_ICM_INTR mapping register    | 0x0054  | R/W    |

| Name   | Description                      | Address | Access |
|--|----------------------------------|---------|--------|
| <b>CORE1 USB DEVICE INT MAP REG</b>          |                                  |         |        |
| <a href="#">CORE1_USB_DEVICE_INT_MAP_REG</a> | USB_DEVICE_INTR mapping register | 0x0058  | R/W    |
| <b>CORE1 SDIO HOST INT MAP REG</b>           |                                  |         |        |
| <a href="#">CORE1_SDIO_HOST_INT_MAP_REG</a>  | SDIO_HOST_INTR mapping register  | 0x005C  | R/W    |
| <b>CORE1 GDMA INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_GDMA_INT_MAP_REG</a>       | GDMA_INTR mapping register       | 0x0060  | R/W    |
| <b>CORE1 SPI2 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_SPI2_INT_MAP_REG</a>       | SPI2_INTR mapping register       | 0x0064  | R/W    |
| <b>CORE1 SPI3 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_SPI3_INT_MAP_REG</a>       | SPI3_INTR mapping register       | 0x0068  | R/W    |
| <b>CORE1 I2S0 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_I2S0_INT_MAP_REG</a>       | I2S0_INTR mapping register       | 0x006C  | R/W    |
| <b>CORE1 I2S1 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_I2S1_INT_MAP_REG</a>       | I2S1_INTR mapping register       | 0x0070  | R/W    |
| <b>CORE1 I2S2 INT MAP REG</b>                |                                  |         |        |
| <a href="#">CORE1_I2S2_INT_MAP_REG</a>       | I2S2_INTR mapping register       | 0x0074  | R/W    |
| <b>CORE1 UHCIO INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UHCIO_INT_MAP_REG</a>      | UHCIO_INTR mapping register      | 0x0078  | R/W    |
| <b>CORE1 UART0 INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UART0_INT_MAP_REG</a>      | UART0_INTR mapping register      | 0x007C  | R/W    |
| <b>CORE1 UART1 INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UART1_INT_MAP_REG</a>      | UART1_INTR mapping register      | 0x0080  | R/W    |
| <b>CORE1 UART2 INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UART2_INT_MAP_REG</a>      | UART2_INTR mapping register      | 0x0084  | R/W    |
| <b>CORE1 UART3 INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UART3_INT_MAP_REG</a>      | UART3_INTR mapping register      | 0x0088  | R/W    |
| <b>CORE1 UART4 INT MAP REG</b>               |                                  |         |        |
| <a href="#">CORE1_UART4_INT_MAP_REG</a>      | UART4_INTR mapping register      | 0x008C  | R/W    |
| <b>CORE1 LCD CAM INT MAP REG</b>             |                                  |         |        |



| Name  | Description                         | Address | Access |
|---|-------------------------------------|---------|--------|
| <a href="#">CORE1_LCD_CAM_INT_MAP_REG</a>       | LCD_CAM_INTR mapping register       | 0x0090  | R/W    |
| <b>CORE1 ADC INT MAP REG</b>                    |                                     |         |        |
| <a href="#">CORE1_ADC_INT_MAP_REG</a>           | ADC_INTR mapping register           | 0x0094  | R/W    |
| <b>CORE1 PWM0 INT MAP REG</b>                   |                                     |         |        |
| <a href="#">CORE1_PWM0_INT_MAP_REG</a>          | PWM0_INTR mapping register          | 0x0098  | R/W    |
| <b>CORE1 PWM1 INT MAP REG</b>                   |                                     |         |        |
| <a href="#">CORE1_PWM1_INT_MAP_REG</a>          | PWM1_INTR mapping register          | 0x009C  | R/W    |
| <b>CORE1 TWAIO INT MAP REG</b>                  |                                     |         |        |
| <a href="#">CORE1_TWAIO_INT_MAP_REG</a>         | TWAIO_INTR mapping register         | 0x00A0  | R/W    |
| <b>CORE1 TWAI1 INT MAP REG</b>                  |                                     |         |        |
| <a href="#">CORE1_TWAI1_INT_MAP_REG</a>         | TWAI1_INTR mapping register         | 0x00A4  | R/W    |
| <b>CORE1 TWAI2 INT MAP REG</b>                  |                                     |         |        |
| <a href="#">CORE1_TWAI2_INT_MAP_REG</a>         | TWAI2_INTR mapping register         | 0x00A8  | R/W    |
| <b>CORE1 RMT INT MAP REG</b>                    |                                     |         |        |
| <a href="#">CORE1_RMT_INT_MAP_REG</a>           | RMT_INTR mapping register           | 0x00AC  | R/W    |
| <b>CORE1 I2C0 INT MAP REG</b>                   |                                     |         |        |
| <a href="#">CORE1_I2C0_INT_MAP_REG</a>          | I2C0_INTR mapping register          | 0x00B0  | R/W    |
| <b>CORE1 I2C1 INT MAP REG</b>                   |                                     |         |        |
| <a href="#">CORE1_I2C1_INT_MAP_REG</a>          | I2C1_INTR mapping register          | 0x00B4  | R/W    |
| <b>CORE1 TIMERGRPO TO INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_TIMERGRPO_TO_INT_MAP_REG</a>  | TIMERGRPO_TO_INTR mapping register  | 0x00B8  | R/W    |
| <b>CORE1 TIMERGRPO T1 INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_TIMERGRPO_T1_INT_MAP_REG</a>  | TIMERGRPO_T1_INTR mapping register  | 0x00BC  | R/W    |
| <b>CORE1 TIMERGRPO WDT INT MAP REG</b>          |                                     |         |        |
| <a href="#">CORE1_TIMERGRPO_WDT_INT_MAP_REG</a> | TIMERGRPO_WDT_INTR mapping register | 0x00C0  | R/W    |
| <b>CORE1 TIMERGRP1 TO INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_TIMERGRP1_TO_INT_MAP_REG</a>  | TIMERGRP1_TO_INTR mapping register  | 0x00C4  | R/W    |
| <b>CORE1 TIMERGRP1 T1 INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_TIMERGRP1_T1_INT_MAP_REG</a>  | TIMERGRP1_T1_INTR mapping register  | 0x00C8  | R/W    |

| Name   | Description                            | Address | Access |
|--|--|---------|--------|
| <b>CORE1 TIMERGRP1 WDT INT MAP REG</b>             |  |         |        |
| <a href="#">CORE1_TIMERGRP1_WDT_INT_MAP_REG</a>    | TIMERGRP1_WDT_INTR mapping register    | 0x00CC  | R/W    |
| <b>CORE1 LEDC INT MAP REG</b>                      |  |         |        |
| <a href="#">CORE1_LEDC_INT_MAP_REG</a>             | LEDC_INTR mapping register             | 0x00D0  | R/W    |
| <b>CORE1 SYSTIMER TARGET0 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_SYSTIMER_TARGET0_INT_MAP_REG</a> | SYSTIMER_TARGET0_INTR mapping register | 0x00D4  | R/W    |
| <b>CORE1 SYSTIMER TARGET1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_SYSTIMER_TARGET1_INT_MAP_REG</a> | SYSTIMER_TARGET1_INTR mapping register | 0x00D8  | R/W    |
| <b>CORE1 SYSTIMER TARGET2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_SYSTIMER_TARGET2_INT_MAP_REG</a> | SYSTIMER_TARGET2_INTR mapping register | 0x00DC  | R/W    |
| <b>CORE1 AHB PDMA IN CHO INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AHB_PDMA_IN_CHO_INT_MAP_REG</a>  | AHB_PDMA_IN_CHO_INTR mapping register  | 0x00E0  | R/W    |
| <b>CORE1 AHB PDMA IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AHB_PDMA_IN_CH1_INT_MAP_REG</a>  | AHB_PDMA_IN_CH1_INTR mapping register  | 0x00E4  | R/W    |
| <b>CORE1 AHB PDMA IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AHB_PDMA_IN_CH2_INT_MAP_REG</a>  | AHB_PDMA_IN_CH2_INTR mapping register  | 0x00E8  | R/W    |
| <b>CORE1 AHB PDMA OUT CHO INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_AHB_PDMA_OUT_CHO_INT_MAP_REG</a> | AHB_PDMA_OUT_CHO_INTR mapping register | 0x00EC  | R/W    |
| <b>CORE1 AHB PDMA OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_AHB_PDMA_OUT_CH1_INT_MAP_REG</a> | AHB_PDMA_OUT_CH1_INTR mapping register | 0x00F0  | R/W    |
| <b>CORE1 AHB PDMA OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_AHB_PDMA_OUT_CH2_INT_MAP_REG</a> | AHB_PDMA_OUT_CH2_INTR mapping register | 0x00F4  | R/W    |
| <b>CORE1 AXI PDMA IN CHO INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AXI_PDMA_IN_CHO_INT_MAP_REG</a>  | AXI_PDMA_IN_CHO_INTR mapping register  | 0x00F8  | R/W    |
| <b>CORE1 AXI PDMA IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AXI_PDMA_IN_CH1_INT_MAP_REG</a>  | AXI_PDMA_IN_CH1_INTR mapping register  | 0x00FC  | R/W    |
| <b>CORE1 AXI PDMA IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_AXI_PDMA_IN_CH2_INT_MAP_REG</a>  | AXI_PDMA_IN_CH2_INTR mapping register  | 0x0100  | R/W    |
| <b>CORE1 AXI PDMA OUT CHO INT MAP REG</b>          |  |         |        |

| Name   | Description                            | Address | Access |
|--|--|---------|--------|
| <a href="#">CORE1_AXI_PDMA_OUT_CH0_INT_MAP_REG</a> | AXI_PDMA_OUT_CH0_INTR mapping register | 0x0104  | R/W    |
| <b>CORE1 AXI PDMA OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_AXI_PDMA_OUT_CH1_INT_MAP_REG</a> | AXI_PDMA_OUT_CH1_INTR mapping register | 0x0108  | R/W    |
| <b>CORE1 AXI PDMA OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_AXI_PDMA_OUT_CH2_INT_MAP_REG</a> | AXI_PDMA_OUT_CH2_INTR mapping register | 0x010C  | R/W    |
| <b>CORE1 RSA INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE1_RSA_INT_MAP_REG</a>              | RSA_INTR mapping register              | 0x0110  | R/W    |
| <b>CORE1 AES INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE1_AES_INT_MAP_REG</a>              | AES_INTR mapping register              | 0x0114  | R/W    |
| <b>CORE1 SHA INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE1_SHA_INT_MAP_REG</a>              | SHA_INTR mapping register              | 0x0118  | R/W    |
| <b>CORE1 ECC INT MAP REG</b>                       |  |         |        |
| <a href="#">CORE1_ECC_INT_MAP_REG</a>              | ECC_INTR mapping register              | 0x011C  | R/W    |
| <b>CORE1 ECDSA INT MAP REG</b>                     |  |         |        |
| <a href="#">CORE1_ECDSA_INT_MAP_REG</a>            | ECDSA_INTR mapping register            | 0x0120  | R/W    |
| <b>CORE1 GPIO INTO MAP REG</b>                     |  |         |        |
| <a href="#">CORE1_GPIO_INT0_MAP_REG</a>            | GPIO_INT0 mapping register             | 0x0128  | R/W    |
| <b>CORE1 GPIO INT1 MAP REG</b>                     |  |         |        |
| <a href="#">CORE1_GPIO_INT1_MAP_REG</a>            | GPIO_INTR1 mapping register            | 0x012C  | R/W    |
| <b>CORE1 GPIO INT2 MAP REG</b>                     |  |         |        |
| <a href="#">CORE1_GPIO_INT2_MAP_REG</a>            | GPIO_INTR2 mapping register            | 0x0130  | R/W    |
| <b>CORE1 GPIO INT3 MAP REG</b>                     |  |         |        |
| <a href="#">CORE1_GPIO_INT3_MAP_REG</a>            | GPIO_INTR3 mapping register            | 0x0134  | R/W    |
| <b>CORE1 GPIO PAD COMP INT MAP REG</b>             |  |         |        |
| <a href="#">CORE1_GPIO_PAD_COMP_INT_MAP_REG</a>    | GPIO_PAD_COMP_INTR mapping register    | 0x0138  | R/W    |
| <b>CORE1 CPU INT FROM CPU 0 MAP REG</b>            |  |         |        |
| <a href="#">CORE1_CPU_INT_FROM_CPU_0_MAP_REG</a>   | CPU_INTR_FROM_CPU_0 mapping register   | 0x013C  | R/W    |
| <b>CORE1 CPU INT FROM CPU 1 MAP REG</b>            |  |         |        |
| <a href="#">CORE1_CPU_INT_FROM_CPU_1_MAP_REG</a>   | CPU_INTR_FROM_CPU_1 mapping register   | 0x0140  | R/W    |

| Name  | Description                                   | Address | Access |
|---|---|---------|--------|
| <b>CORE1 CPU INT FROM CPU 2 MAP REG</b>                   |   |         |        |
| <a href="#">CORE1_CPU_INT_FROM_CPU_2_MAP_REG</a>          | CPU_INTR_FROM_CPU_2 mapping register          | 0x0144  | R/W    |
| <b>CORE1 CPU INT FROM CPU 3 MAP REG</b>                   |   |         |        |
| <a href="#">CORE1_CPU_INT_FROM_CPU_3_MAP_REG</a>          | CPU_INTR_FROM_CPU_3 mapping register          | 0x0148  | R/W    |
| <b>CORE1 FLASH MSPI INT MAP REG</b>                       |   |         |        |
| <a href="#">CORE1_FLASH_MSPI_INT_MAP_REG</a>              | FLASH_MSPI_INTR mapping register              | 0x0150  | R/W    |
| <b>CORE1 CSI BRIDGE INT MAP REG</b>                       |   |         |        |
| <a href="#">CORE1_CSI_BRIDGE_INT_MAP_REG</a>              | CSI_BRIDGE_INTR mapping register              | 0x0154  | R/W    |
| <b>CORE1 DSI BRIDGE INT MAP REG</b>                       |   |         |        |
| <a href="#">CORE1_DSI_BRIDGE_INT_MAP_REG</a>              | DSI_BRIDGE_INTR mapping register              | 0x0158  | R/W    |
| <b>CORE1 CSI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE1_CSI_INT_MAP_REG</a>                     | CSI_INTR mapping register                     | 0x015C  | R/W    |
| <b>CORE1 DSI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE1_DSI_INT_MAP_REG</a>                     | DSI_INTR mapping register                     | 0x0160  | R/W    |
| <b>CORE1 GMII PHY INT MAP REG</b>                         |   |         |        |
| <a href="#">CORE1_GMII_PHY_INT_MAP_REG</a>                | GMII_PHY_INTR mapping register                | 0x0164  | R/W    |
| <b>CORE1 LPI INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE1_LPI_INT_MAP_REG</a>                     | LPI_INTR mapping register                     | 0x0168  | R/W    |
| <b>CORE1 PMT INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE1_PMT_INT_MAP_REG</a>                     | PMT_INTR mapping register                     | 0x016C  | R/W    |
| <b>CORE1 SBD INT MAP REG</b>                              |   |         |        |
| <a href="#">CORE1_ETH_MAC_INT_MAP_REG</a>                 | ETH_MAC_INTR mapping register                 | 0x0170  | R/W    |
| <b>CORE1 USB OTG INT MAP REG</b>                          |   |         |        |
| <a href="#">CORE1_USB_OTG_INT_MAP_REG</a>                 | USB_OTG_INTR mapping register                 | 0x0174  | R/W    |
| <b>CORE1 USB OTG ENDP MULTI PROC INT MAP REG</b>          |   |         |        |
| <a href="#">CORE1_USB_OTG_ENDP_MULTI_PROC_INT_MAP_REG</a> | USB_OTG_ENDP_MULTI_PROC_INTR mapping register | 0x0178  | R/W    |
| <b>CORE1 JPEG INT MAP REG</b>                             |   |         |        |
| <a href="#">CORE1_JPEG_INT_MAP_REG</a>                    | JPEG_INTR mapping register                    | 0x017C  | R/W    |

| Name  | Description                         | Address | Access |
|---|-------------------------------------|---------|--------|
| <b>CORE1 PPA INT MAP REG</b>                    |                                     |         |        |
| <a href="#">CORE1_PPA_INT_MAP_REG</a>           | PPA_INTR mapping register           | 0x0180  | R/W    |
| <b>CORE1 CORE0 TRACE INT MAP REG</b>            |                                     |         |        |
| <a href="#">CORE1_CORE0_TRACE_INT_MAP_REG</a>   | CORE0_TRACE_INTR mapping register   | 0x0184  | R/W    |
| <b>CORE1 CORE1 TRACE INT MAP REG</b>            |                                     |         |        |
| <a href="#">CORE1_CORE1_TRACE_INT_MAP_REG</a>   | CORE1_TRACE_INTR mapping register   | 0x0188  | R/W    |
| <b>CORE1 ISP INT MAP REG</b>                    |                                     |         |        |
| <a href="#">CORE1_ISP_INT_MAP_REG</a>           | ISP_INTR mapping register           | 0x0190  | R/W    |
| <b>CORE1 I3C MST INT MAP REG</b>                |                                     |         |        |
| <a href="#">CORE1_I3C_MST_INT_MAP_REG</a>       | I3C_MST_INTR mapping register       | 0x0194  | R/W    |
| <b>CORE1 I3C SLV INT MAP REG</b>                |                                     |         |        |
| <a href="#">CORE1_I3C_SLV_INT_MAP_REG</a>       | I3C_SLV_INTR mapping register       | 0x0198  | R/W    |
| <b>CORE1 USB OTG11 INT MAP REG</b>              |                                     |         |        |
| <a href="#">CORE1_USB_OTG11_INT_MAP_REG</a>     | USB_OTG11_INTR mapping register     | 0x019C  | R/W    |
| <b>CORE1 DMA2D IN CHO INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_DMA2D_IN_CHO_INT_MAP_REG</a>  | DMA2D_IN_CHO_INTR mapping register  | 0x01A0  | R/W    |
| <b>CORE1 DMA2D IN CH1 INT MAP REG</b>           |                                     |         |        |
| <a href="#">CORE1_DMA2D_IN_CH1_INT_MAP_REG</a>  | DMA2D_IN_CH1_INTR mapping register  | 0x01A4  | R/W    |
| <b>CORE1 DMA2D OUT CHO INT MAP REG</b>          |                                     |         |        |
| <a href="#">CORE1_DMA2D_OUT_CHO_INT_MAP_REG</a> | DMA2D_OUT_CHO_INTR mapping register | 0x01A8  | R/W    |
| <b>CORE1 DMA2D OUT CH1 INT MAP REG</b>          |                                     |         |        |
| <a href="#">CORE1_DMA2D_OUT_CH1_INT_MAP_REG</a> | DMA2D_OUT_CH1_INTR mapping register | 0x01AC  | R/W    |
| <b>CORE1 DMA2D OUT CH2 INT MAP REG</b>          |                                     |         |        |
| <a href="#">CORE1_DMA2D_OUT_CH2_INT_MAP_REG</a> | DMA2D_OUT_CH2_INTR mapping register | 0x01B0  | R/W    |
| <b>CORE1 PSRAM MSPI INT MAP REG</b>             |                                     |         |        |
| <a href="#">CORE1_PSRAM_MSPI_INT_MAP_REG</a>    | PSRAM_MSPI_INTR mapping register    | 0x01B4  | R/W    |
| <b>CORE1 HP SYSREG INT MAP REG</b>              |                                     |         |        |
| <a href="#">CORE1_HP_SYSREG_INT_MAP_REG</a>     | HP_SYSREG_INTR mapping register     | 0x01B8  | R/W    |
| <b>CORE1 PCNT INT MAP REG</b>                   |                                     |         |        |

| Name   | Description                              | Address | Access |
|--|--|---------|--------|
| <a href="#">CORE1_PCNT_INT_MAP_REG</a>               | PCNT_INTR mapping register               | 0x01BC  | R/W    |
| <b>CORE1 HP PARLIO RX INT MAP REG</b>                |  |         |        |
| <a href="#">CORE1_HP_PARLIO_RX_INT_MAP_REG</a>       | HP_PARLIO_RX_INTR mapping register       | 0x01C4  | R/W    |
| <b>CORE1 HP PARLIO TX INT MAP REG</b>                |  |         |        |
| <a href="#">CORE1_HP_PARLIO_TX_INT_MAP_REG</a>       | HP_PARLIO_TX_INTR mapping register       | 0x01C8  | R/W    |
| <b>CORE1 H264 DMA2D OUT CHO INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_OUT_CHO_INT_MAP_REG</a> | H264_DMA2D_OUT_CHO_INTR mapping register | 0x01CC  | R/W    |
| <b>CORE1 H264 DMA2D OUT CH1 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_OUT_CH1_INT_MAP_REG</a> | H264_DMA2D_OUT_CH1_INTR mapping register | 0x01D0  | R/W    |
| <b>CORE1 H264 DMA2D OUT CH2 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_OUT_CH2_INT_MAP_REG</a> | H264_DMA2D_OUT_CH2_INTR mapping register | 0x01D4  | R/W    |
| <b>CORE1 H264 DMA2D OUT CH3 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_OUT_CH3_INT_MAP_REG</a> | H264_DMA2D_OUT_CH3_INTR mapping register | 0x01D8  | R/W    |
| <b>CORE1 H264 DMA2D OUT CH4 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_OUT_CH4_INT_MAP_REG</a> | H264_DMA2D_OUT_CH4_INTR mapping register | 0x01DC  | R/W    |
| <b>CORE1 H264 DMA2D IN CHO INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_H264_DMA2D_IN_CHO_INT_MAP_REG</a>  | H264_DMA2D_IN_CHO_INTR mapping register  | 0x01E0  | R/W    |
| <b>CORE1 H264 DMA2D IN CH1 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_H264_DMA2D_IN_CH1_INT_MAP_REG</a>  | H264_DMA2D_IN_CH1_INTR mapping register  | 0x01E4  | R/W    |
| <b>CORE1 H264 DMA2D IN CH2 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_H264_DMA2D_IN_CH2_INT_MAP_REG</a>  | H264_DMA2D_IN_CH2_INTR mapping register  | 0x01E8  | R/W    |
| <b>CORE1 H264 DMA2D IN CH3 INT MAP REG</b>           |  |         |        |
| <a href="#">CORE1_H264_DMA2D_IN_CH3_INT_MAP_REG</a>  | H264_DMA2D_IN_CH3_INTR mapping register  | 0x01EC  | R/W    |
| <b>CORE1 H264 DMA2D IN CH4 INT MAP REG</b>           |  |         |        |

| Name  | Description                                    | Address | Access |
|---|--|---------|--------|
| <a href="#">CORE1_H264_DMA2D_IN_CH4_INT_MAP_REG</a> | H264_DMA2D_IN_CH4_INTR mapping register        | 0x01F0  | R/W    |
| <b>CORE1 H264 DMA2D IN CH5 INT MAP REG</b>          |  |         |        |
| <a href="#">CORE1_H264_DMA2D_IN_CH5_INT_MAP_REG</a> | H264_DMA2D_IN_CH5_INTR mapping register        | 0x01F4  | R/W    |
| <b>CORE1 H264 REG INT MAP REG</b>                   |  |         |        |
| <a href="#">CORE1_H264_REG_INT_MAP_REG</a>          | H264_REG_INTR mapping register                 | 0x01F8  | R/W    |
| <b>CORE1 ASSIST DEBUG INT MAP REG</b>               |  |         |        |
| <a href="#">CORE1_ASSIST_DEBUG_INT_MAP_REG</a>      | ASSIST_DEBUG_INTR mapping register             | 0x01FC  | R/W    |
| <b>CORE1 INTR STATUS REG 0 REG</b>                  |  |         |        |
| <a href="#">CORE1_INTR_STATUS_REG_0_REG</a>         | Status register for interrupt sources 0 ~ 31   | 0x0200  | RO     |
| <b>CORE1 INTR STATUS REG 1 REG</b>                  |  |         |        |
| <a href="#">CORE1_INTR_STATUS_REG_1_REG</a>         | Status register for interrupt sources 32 ~ 63  | 0x0204  | RO     |
| <b>CORE1 INTR STATUS REG 2 REG</b>                  |  |         |        |
| <a href="#">CORE1_INTR_STATUS_REG_2_REG</a>         | Status register for interrupt sources 64 ~ 95  | 0x0208  | RO     |
| <b>CORE1 INTR STATUS REG 3 REG</b>                  |  |         |        |
| <a href="#">CORE1_INTR_STATUS_REG_3_REG</a>         | Status register for interrupt sources 96 ~ 127 | 0x020C  | RO     |
| <b>CORE1 CLOCK GATE REG</b>                         |  |         |        |
| <a href="#">CORE1_CLOCK_GATE_REG</a>                | Clock gating register                          | 0x0210  | R/W    |
| <b>CORE1 INTERRUPT REG DATE REG</b>                 |  |         |        |
| <a href="#">CORE1_INTERRUPT_REG_DATE_REG</a>        | Version control register                       | 0x03FC  | R/W    |

## 11.6 Registers

The addresses in this section are relative to the interrupt matrix base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

### 11.6.1 HP CPUO Interrupt Matrix Registers

Register 11.1. COREO\_LP\_RTC\_INT\_MAP\_REG (0x0000)

Register 11.2. COREO\_LP\_WDT\_INT\_MAP\_REG (0x0004)

Register 11.3. COREO\_LP\_TIMER\_REG\_O\_INT\_MAP\_REG (0x0008)

Register 11.4. COREO\_LP\_TIMER\_REG\_1\_INT\_MAP\_REG (0x000C)

Register 11.5. COREO\_MB\_HP\_INT\_MAP\_REG (0x0010)

Register 11.6. COREO\_MB\_LP\_INT\_MAP\_REG (0x0014)

Register 11.7. COREO\_PMU\_REG\_O\_INT\_MAP\_REG (0x0018)

Register 11.8. COREO\_PMU\_REG\_1\_INT\_MAP\_REG (0x001C)

Register 11.9. COREO\_LP\_ANAPERI\_INT\_MAP\_REG (0x0020)

Register 11.10. COREO\_LP\_ADC\_INT\_MAP\_REG (0x0024)

Register 11.11. COREO\_LP\_GPIO\_INT\_MAP\_REG (0x0028)

Register 11.12. COREO\_LP\_I2C\_INT\_MAP\_REG (0x002C)

Register 11.13. COREO\_LP\_I2S\_INT\_MAP\_REG (0x0030)

Register 11.14. COREO\_LP\_SPI\_INT\_MAP\_REG (0x0034)

Register 11.15. COREO\_LP\_TOUCH\_INT\_MAP\_REG (0x0038)

Register 11.16. COREO\_LP\_TSENS\_INT\_MAP\_REG (0x003C)

Register 11.17. COREO\_LP\_UART\_INT\_MAP\_REG (0x0040)

Register 11.18. COREO\_LP\_EFUSE\_INT\_MAP\_REG (0x0044)

Register 11.19. COREO\_LP\_SW\_INT\_MAP\_REG (0x0048)

Register 11.20. COREO\_LP\_SYSREG\_INT\_MAP\_REG (0x004C)

Register 11.21. COREO\_SYS\_ICM\_INT\_MAP\_REG (0x0054)

Register 11.22. COREO\_USB\_DEVICE\_INT\_MAP\_REG (0x0058)

Register 11.23. COREO\_SDIO\_HOST\_INT\_MAP\_REG (0x005C)

Register 11.24. COREO\_GDMA\_INT\_MAP\_REG (0x0060)

Register 11.25. COREO\_SPI2\_INT\_MAP\_REG (0x0064)

Register 11.26. COREO\_SPI3\_INT\_MAP\_REG (0x0068)

Register 11.27. COREO\_I2SO\_INT\_MAP\_REG (0x006C)

Register 11.28. COREO\_I2S1\_INT\_MAP\_REG (0x0070)



Register 11.29. COREO\_*I2S2\_INT*\_MAP\_REG (0x0074)

Register 11.30. COREO\_*UHCIO\_INT*\_MAP\_REG (0x0078)

Register 11.31. COREO\_*UART0\_INT*\_MAP\_REG (0x007C)

Register 11.32. COREO\_*UART1\_INT*\_MAP\_REG (0x0080)

Register 11.33. COREO\_*UART2\_INT*\_MAP\_REG (0x0084)

Register 11.34. COREO\_*UART3\_INT*\_MAP\_REG (0x0088)

Register 11.35. COREO\_*UART4\_INT*\_MAP\_REG (0x008C)

Register 11.36. COREO\_*LCD\_CAM\_INT*\_MAP\_REG (0x0090)

Register 11.37. COREO\_*ADC\_INT*\_MAP\_REG (0x0094)

Register 11.38. COREO\_*PWMO\_INT*\_MAP\_REG (0x0098)

Register 11.39. COREO\_*PWM1\_INT*\_MAP\_REG (0x009C)

Register 11.40. COREO\_*TWAI0\_INT*\_MAP\_REG (0x00A0)

Register 11.41. COREO\_*TWAI1\_INT*\_MAP\_REG (0x00A4)

Register 11.42. COREO\_*TWAI2\_INT*\_MAP\_REG (0x00A8)

Register 11.43. COREO\_*RMT\_INT*\_MAP\_REG (0x00AC)

Register 11.44. COREO\_*I2CO\_INT*\_MAP\_REG (0x00B0)

Register 11.45. COREO\_*I2C1\_INT*\_MAP\_REG (0x00B4)

Register 11.46. COREO\_*TIMERGRPO\_TO\_INT*\_MAP\_REG (0x00B8)

Register 11.47. COREO\_*TIMERGRPO\_T1\_INT*\_MAP\_REG (0x00BC)

Register 11.48. COREO\_*TIMERGRPO\_WDT\_INT*\_MAP\_REG (0x00C0)

Register 11.49. COREO\_*TIMERGRP1\_TO\_INT*\_MAP\_REG (0x00C4)

Register 11.50. COREO\_*TIMERGRP1\_T1\_INT*\_MAP\_REG (0x00C8)

Register 11.51. COREO\_*TIMERGRP1\_WDT\_INT*\_MAP\_REG (0x00CC)

Register 11.52. COREO\_*LEDC\_INT*\_MAP\_REG (0x00D0)

Register 11.53. COREO\_*SYSTIMER\_TARGET0\_INT*\_MAP\_REG (0x00D4)

Register 11.54. COREO\_*SYSTIMER\_TARGET1\_INT*\_MAP\_REG (0x00D8)

Register 11.55. COREO\_*SYSTIMER\_TARGET2\_INT*\_MAP\_REG (0x00DC)

Register 11.56. COREO\_*AHB\_PDMA\_IN\_CHO\_INT*\_MAP\_REG (0x00E0)

Register 11.57. COREO\_*AHB\_PDMA\_IN\_CH1\_INT*\_MAP\_REG (0x00E4)

Register 11.58. COREO\_*AHB\_PDMA\_IN\_CH2\_INT*\_MAP\_REG (0x00E8)

Register 11.59. COREO\_*AHB\_PDMA\_OUT\_CHO\_INT*\_MAP\_REG (0x00EC)

Register 11.60. COREO\_*AHB\_PDMA\_OUT\_CH1\_INT*\_MAP\_REG (0x00F0)

Register 11.61. COREO\_*AHB\_PDMA\_OUT\_CH2\_INT*\_MAP\_REG (0x00F4)

Register 11.62. COREO\_*AXI\_PDMA\_IN\_CHO\_INT*\_MAP\_REG (0x00F8)

Register 11.63. COREO\_*AXI\_PDMA\_IN\_CH1\_INT*\_MAP\_REG (0x00FC)

- Register 11.64. COREO\_[AXI\\_PDMA\\_IN\\_CH2\\_INT](#)\_MAP\_REG (0x0100)
- Register 11.65. COREO\_[AXI\\_PDMA\\_OUT\\_CHO\\_INT](#)\_MAP\_REG (0x0104)
- Register 11.66. COREO\_[AXI\\_PDMA\\_OUT\\_CH1\\_INT](#)\_MAP\_REG (0x0108)
- Register 11.67. COREO\_[AXI\\_PDMA\\_OUT\\_CH2\\_INT](#)\_MAP\_REG (0x010C)
- Register 11.68. COREO\_[RSA\\_INT](#)\_MAP\_REG (0x0110)
- Register 11.69. COREO\_[AES\\_INT](#)\_MAP\_REG (0x0114)
- Register 11.70. COREO\_[SHA\\_INT](#)\_MAP\_REG (0x0118)
- Register 11.71. COREO\_[ECC\\_INT](#)\_MAP\_REG (0x011C)
- Register 11.72. COREO\_[ECDSA\\_INT](#)\_MAP\_REG (0x0120)
- Register 11.73. COREO\_[GPIO\\_INT0](#)\_MAP\_REG (0x0128)
- Register 11.74. COREO\_[GPIO\\_INT1](#)\_MAP\_REG (0x012C)
- Register 11.75. COREO\_[GPIO\\_INT2](#)\_MAP\_REG (0x0130)
- Register 11.76. COREO\_[GPIO\\_INT3](#)\_MAP\_REG (0x0134)
- Register 11.77. COREO\_[GPIO\\_PAD\\_COMP\\_INT](#)\_MAP\_REG (0x0138)
- Register 11.78. COREO\_[CPU\\_INT\\_FROM\\_CPU\\_0](#)\_MAP\_REG (0x013C)
- Register 11.79. COREO\_[CPU\\_INT\\_FROM\\_CPU\\_1](#)\_MAP\_REG (0x0140)
- Register 11.80. COREO\_[CPU\\_INT\\_FROM\\_CPU\\_2](#)\_MAP\_REG (0x0144)
- Register 11.81. COREO\_[CPU\\_INT\\_FROM\\_CPU\\_3](#)\_MAP\_REG (0x0148)
- Register 11.82. COREO\_[FLASH\\_MSPI\\_INT](#)\_MAP\_REG (0x0150)
- Register 11.83. COREO\_[CSI\\_BRIDGE\\_INT](#)\_MAP\_REG (0x0154)
- Register 11.84. COREO\_[DSI\\_BRIDGE\\_INT](#)\_MAP\_REG (0x0158)
- Register 11.85. COREO\_[CSI\\_INT](#)\_MAP\_REG (0x015C)
- Register 11.86. COREO\_[DSI\\_INT](#)\_MAP\_REG (0x0160)
- Register 11.87. COREO\_[GMII\\_PHY\\_INT](#)\_MAP\_REG (0x0164)
- Register 11.88. COREO\_[LPI\\_INT](#)\_MAP\_REG (0x0168)
- Register 11.89. COREO\_[PMT\\_INT](#)\_MAP\_REG (0x016C)
- Register 11.90. COREO\_[ETH\\_MAC\\_INT](#)\_MAP\_REG (0x0170)
- Register 11.91. COREO\_[USB\\_OTG\\_INT](#)\_MAP\_REG (0x0174)
- Register 11.92. COREO\_[USB\\_OTG\\_ENDP\\_MULTI\\_PROC\\_INT](#)\_MAP\_REG (0x0178)
- Register 11.93. COREO\_[JPEG\\_INT](#)\_MAP\_REG (0x017C)
- Register 11.94. COREO\_[PPA\\_INT](#)\_MAP\_REG (0x0180)
- Register 11.95. COREO\_[CORE0\\_TRACE\\_INT](#)\_MAP\_REG (0x0184)
- Register 11.96. COREO\_[CORE1\\_TRACE\\_INT](#)\_MAP\_REG (0x0188)
- Register 11.97. COREO\_[ISP\\_INT](#)\_MAP\_REG (0x0190)
- Register 11.98. COREO\_[I3C\\_MST\\_INT](#)\_MAP\_REG (0x0194)

Register 11.99. COREO\_*I3C\_SLV\_INT*\_MAP\_REG (0x0198)

Register 11.100. COREO\_*USB\_OTG11\_INT*\_MAP\_REG (0x019C)

Register 11.101. COREO\_*DMA2D\_IN\_CHO\_INT*\_MAP\_REG (0x01A0)

Register 11.102. COREO\_*DMA2D\_IN\_CH1\_INT*\_MAP\_REG (0x01A4)

Register 11.103. COREO\_*DMA2D\_OUT\_CHO\_INT*\_MAP\_REG (0x01A8)

Register 11.104. COREO\_*DMA2D\_OUT\_CH1\_INT*\_MAP\_REG (0x01AC)

Register 11.105. COREO\_*DMA2D\_OUT\_CH2\_INT*\_MAP\_REG (0x01B0)

Register 11.106. COREO\_*PSRAM\_MSPI\_INT*\_MAP\_REG (0x01B4)

Register 11.107. COREO\_*HP\_SYSREG\_INT*\_MAP\_REG (0x01B8)

Register 11.108. COREO\_*PCNT\_INT*\_MAP\_REG (0x01BC)

Register 11.109. COREO\_*HP\_PAU\_INT*\_MAP\_REG (0x01C0)

Register 11.110. COREO\_*HP\_PARLIO\_RX\_INT*\_MAP\_REG (0x01C4)

Register 11.111. COREO\_*HP\_PARLIO\_TX\_INT*\_MAP\_REG (0x01C8)

Register 11.112. COREO\_*H264\_DMA2D\_OUT\_CHO\_INT*\_MAP\_REG (0x01CC)

Register 11.113. COREO\_*H264\_DMA2D\_OUT\_CH1\_INT*\_MAP\_REG (0x01D0)

Register 11.114. COREO\_*H264\_DMA2D\_OUT\_CH2\_INT*\_MAP\_REG (0x01D4)

Register 11.115. COREO\_*H264\_DMA2D\_OUT\_CH3\_INT*\_MAP\_REG (0x01D8)

Register 11.116. COREO\_*H264\_DMA2D\_OUT\_CH4\_INT*\_MAP\_REG (0x01DC)

Register 11.117. COREO\_*H264\_DMA2D\_IN\_CHO\_INT*\_MAP\_REG (0x01E0)

Register 11.118. COREO\_*H264\_DMA2D\_IN\_CH1\_INT*\_MAP\_REG (0x01E4)

Register 11.119. COREO\_*H264\_DMA2D\_IN\_CH2\_INT*\_MAP\_REG (0x01E8)

Register 11.120. COREO\_*H264\_DMA2D\_IN\_CH3\_INT*\_MAP\_REG (0x01EC)

Register 11.121. COREO\_*H264\_DMA2D\_IN\_CH4\_INT*\_MAP\_REG (0x01F0)

Register 11.122. COREO\_*H264\_DMA2D\_IN\_CH5\_INT*\_MAP\_REG (0x01F4)

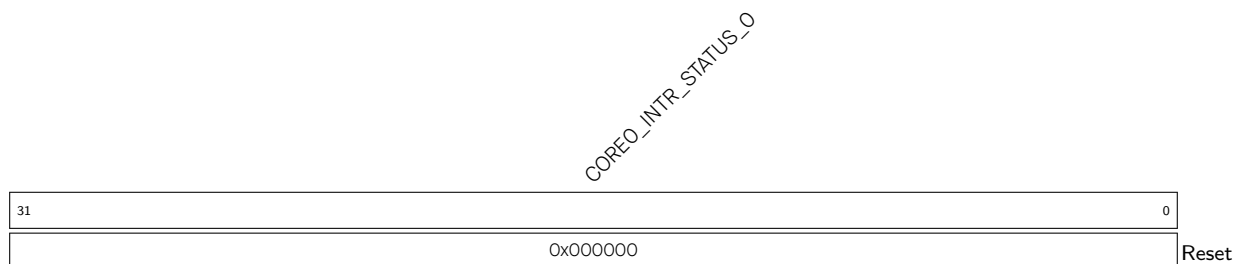
Register 11.123. COREO\_*H264\_REG\_INT*\_MAP\_REG (0x01F8)

Register 11.124. COREO\_*ASSIST\_DEBUG\_INT*\_MAP\_REG (0x01FC)

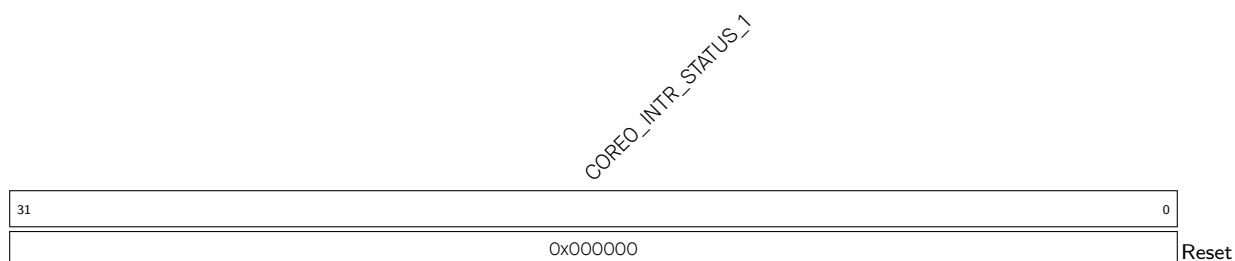
Register 11.125. COREO\_*SOURCE\_Y*\_MAP\_REG (0x0000 - 0x01FC)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |       |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|-------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | COREO_SOURCE_Y_MAP |  |  |  |  |  |       |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6                  |  |  |  |  |  | 5     | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                  |  |  |  |  |  | Reset |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

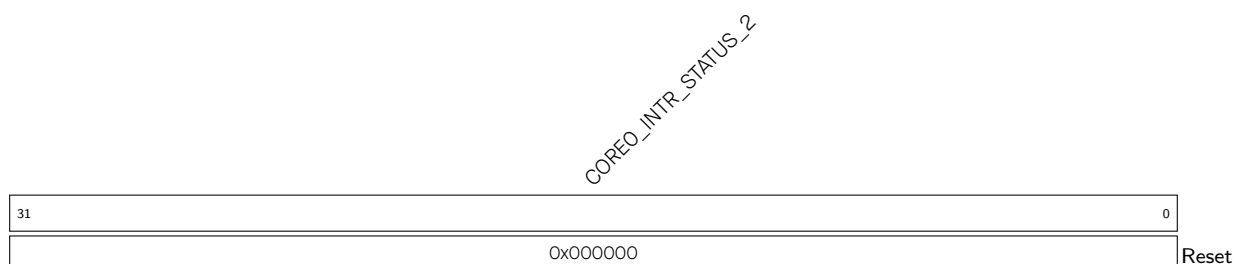
**COREO\_SOURCE\_Y\_MAP** Map interrupt signal of source (Source\_Y) to one of CPU0's external interrupts, can be configured as 16 ~ 47. Writing 0 ~ 15 will disable the interrupt source (0 is the recommended value). The remaining values are invalid. For Source\_Y, see Table 11.4-1. (R/W)

**Register 11.126. COREO\_INTR\_STATUS\_REG\_0\_REG (0x0200)**

**COREO\_INTR\_STATUS\_0** Represents the status of the interrupt sources from 0 ~ 31. Each bit corresponds to one interrupt source. (RO)

**Register 11.127. COREO\_INTR\_STATUS\_REG\_1\_REG (0x0204)**

**COREO\_INTR\_STATUS\_1** Represents the status of the interrupt sources from 32 ~ 63. Each bit corresponds to one interrupt source. (RO)

**Register 11.128. COREO\_INTR\_STATUS\_REG\_2\_REG (0x0208)**

**COREO\_INTR\_STATUS\_2** Represents the status of the interrupt sources from 64 ~ 95. Each bit corresponds to one interrupt source. (RO)



Register 11.134. CORE1\_LP\_TIMER\_REG\_O\_INT\_MAP\_REG (0x0008)

Register 11.135. CORE1\_LP\_TIMER\_REG\_1\_INT\_MAP\_REG (0x000C)

Register 11.136. CORE1\_MB\_HP\_INT\_MAP\_REG (0x0010)

Register 11.137. CORE1\_MB\_LP\_INT\_MAP\_REG (0x0014)

Register 11.138. CORE1\_PMU\_REG\_O\_INT\_MAP\_REG (0x0018)

Register 11.139. CORE1\_PMU\_REG\_1\_INT\_MAP\_REG (0x001C)

Register 11.140. CORE1\_LP\_ANAPERI\_INT\_MAP\_REG (0x0020)

Register 11.141. CORE1\_LP\_ADC\_INT\_MAP\_REG (0x0024)

Register 11.142. CORE1\_LP\_GPIO\_INT\_MAP\_REG (0x0028)

Register 11.143. CORE1\_LP\_I2C\_INT\_MAP\_REG (0x002C)

Register 11.144. CORE1\_LP\_I2S\_INT\_MAP\_REG (0x0030)

Register 11.145. CORE1\_LP\_SPI\_INT\_MAP\_REG (0x0034)

Register 11.146. CORE1\_LP\_TOUCH\_INT\_MAP\_REG (0x0038)

Register 11.147. CORE1\_LP\_TSENS\_INT\_MAP\_REG (0x003C)

Register 11.148. CORE1\_LP\_UART\_INT\_MAP\_REG (0x0040)

Register 11.149. CORE1\_LP\_EFUSE\_INT\_MAP\_REG (0x0044)

Register 11.150. CORE1\_LP\_SW\_INT\_MAP\_REG (0x0048)

Register 11.151. CORE1\_LP\_SYSREG\_INT\_MAP\_REG (0x004C)

Register 11.152. CORE1\_LP\_HUK\_INT\_MAP\_REG (0x0050)

Register 11.153. CORE1\_SYS\_ICM\_INT\_MAP\_REG (0x0054)

Register 11.154. CORE1\_USB\_DEVICE\_INT\_MAP\_REG (0x0058)

Register 11.155. CORE1\_SDIO\_HOST\_INT\_MAP\_REG (0x005C)

Register 11.156. CORE1\_GDMA\_INT\_MAP\_REG (0x0060)

Register 11.157. CORE1\_SPI2\_INT\_MAP\_REG (0x0064)

Register 11.158. CORE1\_SPI3\_INT\_MAP\_REG (0x0068)

Register 11.159. CORE1\_I2SO\_INT\_MAP\_REG (0x006C)

Register 11.160. CORE1\_I2S1\_INT\_MAP\_REG (0x0070)

Register 11.161. CORE1\_I2S2\_INT\_MAP\_REG (0x0074)

Register 11.162. CORE1\_UHCIO\_INT\_MAP\_REG (0x0078)

Register 11.163. CORE1\_UART0\_INT\_MAP\_REG (0x007C)

Register 11.164. CORE1\_UART1\_INT\_MAP\_REG (0x0080)

Register 11.165. CORE1\_UART2\_INT\_MAP\_REG (0x0084)

Register 11.166. CORE1\_UART3\_INT\_MAP\_REG (0x0088)

Register 11.167. CORE1\_UART4\_INT\_MAP\_REG (0x008C)

Register 11.168. CORE1\_LCD\_CAM\_INT\_MAP\_REG (0x0090)

Register 11.169. CORE1\_**ADC\_INT**\_MAP\_REG (0x0094)

Register 11.170. CORE1\_**PWMO\_INT**\_MAP\_REG (0x0098)

Register 11.171. CORE1\_**PWM1\_INT**\_MAP\_REG (0x009C)

Register 11.172. CORE1\_**TWAI0\_INT**\_MAP\_REG (0x00A0)

Register 11.173. CORE1\_**TWAI1\_INT**\_MAP\_REG (0x00A4)

Register 11.174. CORE1\_**TWAI2\_INT**\_MAP\_REG (0x00A8)

Register 11.175. CORE1\_**RMT\_INT**\_MAP\_REG (0x00AC)

Register 11.176. CORE1\_**I2CO\_INT**\_MAP\_REG (0x00B0)

Register 11.177. CORE1\_**I2C1\_INT**\_MAP\_REG (0x00B4)

Register 11.178. CORE1\_**TIMERGRPO\_TO\_INT**\_MAP\_REG (0x00B8)

Register 11.179. CORE1\_**TIMERGRPO\_T1\_INT**\_MAP\_REG (0x00BC)

Register 11.180. CORE1\_**TIMERGRPO\_WDT\_INT**\_MAP\_REG (0x00C0)

Register 11.181. CORE1\_**TIMERGRP1\_TO\_INT**\_MAP\_REG (0x00C4)

Register 11.182. CORE1\_**TIMERGRP1\_T1\_INT**\_MAP\_REG (0x00C8)

Register 11.183. CORE1\_**TIMERGRP1\_WDT\_INT**\_MAP\_REG (0x00CC)

Register 11.184. CORE1\_**LEDC\_INT**\_MAP\_REG (0x00D0)

Register 11.185. CORE1\_**SYSTIMER\_TARGET0\_INT**\_MAP\_REG (0x00D4)

Register 11.186. CORE1\_**SYSTIMER\_TARGET1\_INT**\_MAP\_REG (0x00D8)

Register 11.187. CORE1\_**SYSTIMER\_TARGET2\_INT**\_MAP\_REG (0x00DC)

Register 11.188. CORE1\_**AHB\_PDMA\_IN\_CHO\_INT**\_MAP\_REG (0x00E0)

Register 11.189. CORE1\_**AHB\_PDMA\_IN\_CH1\_INT**\_MAP\_REG (0x00E4)

Register 11.190. CORE1\_**AHB\_PDMA\_IN\_CH2\_INT**\_MAP\_REG (0x00E8)

Register 11.191. CORE1\_**AHB\_PDMA\_OUT\_CHO\_INT**\_MAP\_REG (0x00EC)

Register 11.192. CORE1\_**AHB\_PDMA\_OUT\_CH1\_INT**\_MAP\_REG (0x00F0)

Register 11.193. CORE1\_**AHB\_PDMA\_OUT\_CH2\_INT**\_MAP\_REG (0x00F4)

Register 11.194. CORE1\_**AXI\_PDMA\_IN\_CHO\_INT**\_MAP\_REG (0x00F8)

Register 11.195. CORE1\_**AXI\_PDMA\_IN\_CH1\_INT**\_MAP\_REG (0x00FC)

Register 11.196. CORE1\_**AXI\_PDMA\_IN\_CH2\_INT**\_MAP\_REG (0x0100)

Register 11.197. CORE1\_**AXI\_PDMA\_OUT\_CHO\_INT**\_MAP\_REG (0x0104)

Register 11.198. CORE1\_**AXI\_PDMA\_OUT\_CH1\_INT**\_MAP\_REG (0x0108)

Register 11.199. CORE1\_**AXI\_PDMA\_OUT\_CH2\_INT**\_MAP\_REG (0x010C)

Register 11.200. CORE1\_**RSA\_INT**\_MAP\_REG (0x0110)

Register 11.201. CORE1\_**AES\_INT**\_MAP\_REG (0x0114)

Register 11.202. CORE1\_**SHA\_INT**\_MAP\_REG (0x0118)

Register 11.203. CORE1\_**ECC\_INT**\_MAP\_REG (0x011C)

- Register 11.204. CORE1\_ [ECDSA\\_INT\\_MAP\\_REG](#) (0x0120)
- Register 11.205. CORE1\_ [KM\\_INT\\_MAP\\_REG](#) (0x0124)
- Register 11.206. CORE1\_ [GPIO\\_INT0\\_MAP\\_REG](#) (0x0128)
- Register 11.207. CORE1\_ [GPIO\\_INT1\\_MAP\\_REG](#) (0x012C)
- Register 11.208. CORE1\_ [GPIO\\_INT2\\_MAP\\_REG](#) (0x0130)
- Register 11.209. CORE1\_ [GPIO\\_INT3\\_MAP\\_REG](#) (0x0134)
- Register 11.210. CORE1\_ [GPIO\\_PAD\\_COMP\\_INT\\_MAP\\_REG](#) (0x0138)
- Register 11.211. CORE1\_ [CPU\\_INT\\_FROM\\_CPU\\_0\\_MAP\\_REG](#) (0x013C)
- Register 11.212. CORE1\_ [CPU\\_INT\\_FROM\\_CPU\\_1\\_MAP\\_REG](#) (0x0140)
- Register 11.213. CORE1\_ [CPU\\_INT\\_FROM\\_CPU\\_2\\_MAP\\_REG](#) (0x0144)
- Register 11.214. CORE1\_ [CPU\\_INT\\_FROM\\_CPU\\_3\\_MAP\\_REG](#) (0x0148)
- Register 11.215. CORE1\_ [FLASH\\_MSPI\\_INT\\_MAP\\_REG](#) (0x0150)
- Register 11.216. CORE1\_ [CSI\\_BRIDGE\\_INT\\_MAP\\_REG](#) (0x0154)
- Register 11.217. CORE1\_ [DSI\\_BRIDGE\\_INT\\_MAP\\_REG](#) (0x0158)
- Register 11.218. CORE1\_ [CSI\\_INT\\_MAP\\_REG](#) (0x015C)
- Register 11.219. CORE1\_ [DSI\\_INT\\_MAP\\_REG](#) (0x0160)
- Register 11.220. CORE1\_ [GMII\\_PHY\\_INT\\_MAP\\_REG](#) (0x0164)
- Register 11.221. CORE1\_ [LPI\\_INT\\_MAP\\_REG](#) (0x0168)
- Register 11.222. CORE1\_ [PMT\\_INT\\_MAP\\_REG](#) (0x016C)
- Register 11.223. CORE1\_ [ETH\\_MAC\\_INT\\_MAP\\_REG](#) (0x0170)
- Register 11.224. CORE1\_ [USB\\_OTG\\_INT\\_MAP\\_REG](#) (0x0174)
- Register 11.225. CORE1\_ [USB\\_OTG\\_ENDP\\_MULTI\\_PROC\\_INT\\_MAP\\_REG](#) (0x0178)
- Register 11.226. CORE1\_ [JPEG\\_INT\\_MAP\\_REG](#) (0x017C)
- Register 11.227. CORE1\_ [PPA\\_INT\\_MAP\\_REG](#) (0x0180)
- Register 11.228. CORE1\_ [CORE0\\_TRACE\\_INT\\_MAP\\_REG](#) (0x0184)
- Register 11.229. CORE1\_ [CORE1\\_TRACE\\_INT\\_MAP\\_REG](#) (0x0188)
- Register 11.230. CORE1\_ [ISP\\_INT\\_MAP\\_REG](#) (0x0190)
- Register 11.231. CORE1\_ [I3C\\_MST\\_INT\\_MAP\\_REG](#) (0x0194)
- Register 11.232. CORE1\_ [I3C\\_SLV\\_INT\\_MAP\\_REG](#) (0x0198)
- Register 11.233. CORE1\_ [USB\\_OTG11\\_INT\\_MAP\\_REG](#) (0x019C)
- Register 11.234. CORE1\_ [DMA2D\\_IN\\_CHO\\_INT\\_MAP\\_REG](#) (0x01A0)
- Register 11.235. CORE1\_ [DMA2D\\_IN\\_CH1\\_INT\\_MAP\\_REG](#) (0x01A4)
- Register 11.236. CORE1\_ [DMA2D\\_OUT\\_CHO\\_INT\\_MAP\\_REG](#) (0x01A8)
- Register 11.237. CORE1\_ [DMA2D\\_OUT\\_CH1\\_INT\\_MAP\\_REG](#) (0x01AC)
- Register 11.238. CORE1\_ [DMA2D\\_OUT\\_CH2\\_INT\\_MAP\\_REG](#) (0x01B0)



Register 11.239. CORE1\_PSRAM\_MSPI\_INT\_MAP\_REG (0x01B4)

Register 11.240. CORE1\_HP\_SYSREG\_INT\_MAP\_REG (0x01B8)

Register 11.241. CORE1\_PCNT\_INT\_MAP\_REG (0x01BC)

Register 11.242. CORE1\_HP\_PAU\_INT\_MAP\_REG (0x01C0)

Register 11.243. CORE1\_HP\_PARLIO\_RX\_INT\_MAP\_REG (0x01C4)

Register 11.244. CORE1\_HP\_PARLIO\_TX\_INT\_MAP\_REG (0x01C8)

Register 11.245. CORE1\_H264\_DMA2D\_OUT\_CHO\_INT\_MAP\_REG (0x01CC)

Register 11.246. CORE1\_H264\_DMA2D\_OUT\_CH1\_INT\_MAP\_REG (0x01D0)

Register 11.247. CORE1\_H264\_DMA2D\_OUT\_CH2\_INT\_MAP\_REG (0x01D4)

Register 11.248. CORE1\_H264\_DMA2D\_OUT\_CH3\_INT\_MAP\_REG (0x01D8)

Register 11.249. CORE1\_H264\_DMA2D\_OUT\_CH4\_INT\_MAP\_REG (0x01DC)

Register 11.250. CORE1\_H264\_DMA2D\_IN\_CHO\_INT\_MAP\_REG (0x01E0)

Register 11.251. CORE1\_H264\_DMA2D\_IN\_CH1\_INT\_MAP\_REG (0x01E4)

Register 11.252. CORE1\_H264\_DMA2D\_IN\_CH2\_INT\_MAP\_REG (0x01E8)

Register 11.253. CORE1\_H264\_DMA2D\_IN\_CH3\_INT\_MAP\_REG (0x01EC)

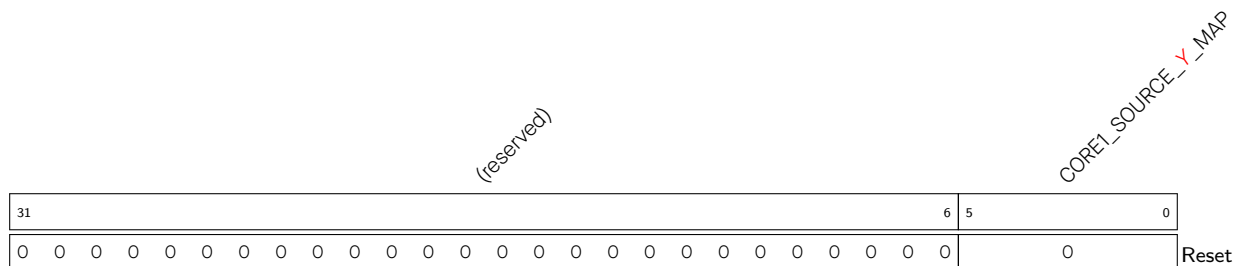
Register 11.254. CORE1\_H264\_DMA2D\_IN\_CH4\_INT\_MAP\_REG (0x01F0)

Register 11.255. CORE1\_H264\_DMA2D\_IN\_CH5\_INT\_MAP\_REG (0x01F4)

Register 11.256. CORE1\_H264\_REG\_INT\_MAP\_REG (0x01F8)

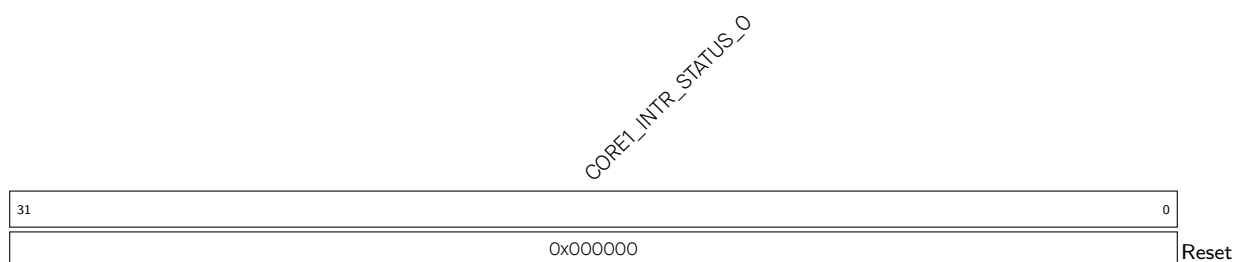
Register 11.257. CORE1\_ASSIST\_DEBUG\_INT\_MAP\_REG (0x01FC)

Register 11.258. CORE1\_SOURCE\_Y\_MAP\_REG (0x0000 - 0x01FC)

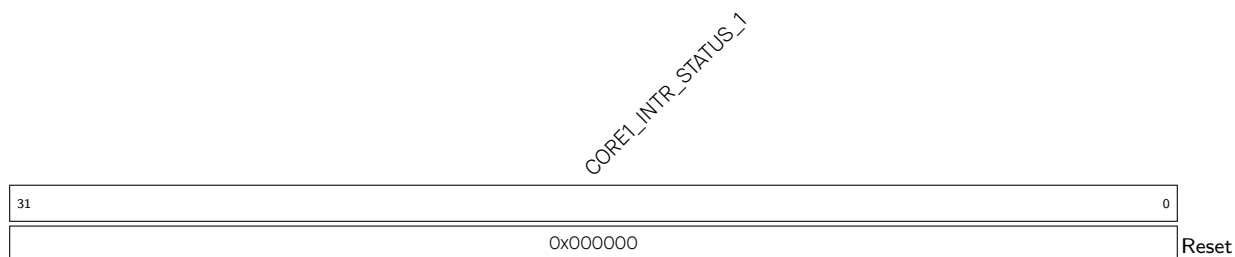


**CORE1\_SOURCE\_Y\_MAP** Map interrupt signal of source (Source\_Y) to one of CPU1 external interrupts, can be configured as 16 ~ 47. Writing 0 ~ 15 will disable the interrupt source (0 is the recommended value). The remaining values are invalid. For Source\_Y, see Table 11.4-1. (R/W)

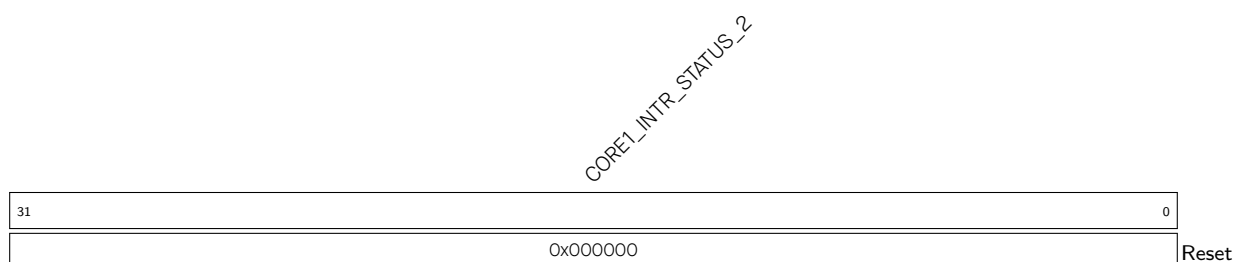
Register 11.259. CORE1\_INTR\_STATUS\_REG\_O\_REG (0x0200)



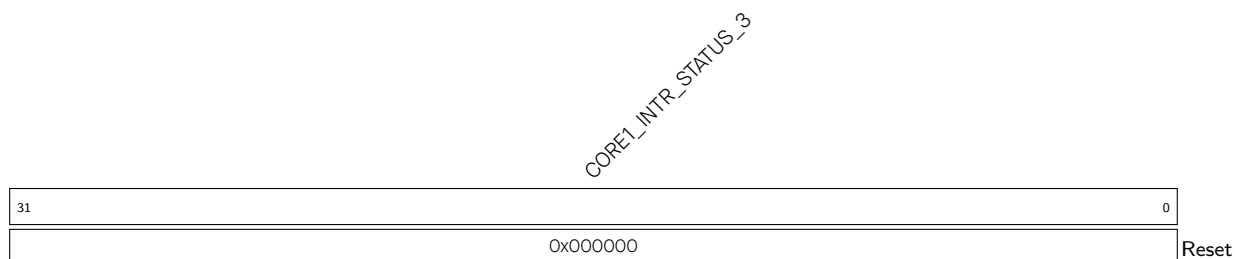
**CORE1\_INTR\_STATUS\_O** Represents the status of the interrupt sources from 0 ~ 31. Each bit corresponds to one interrupt source. (RO)

**Register 11.260. CORE1\_INTR\_STATUS\_REG\_1\_REG (0x0204)**

**CORE1\_INTR\_STATUS\_1** Represents the status of the interrupt sources from 32 ~ 63. Each bit corresponds to one interrupt source. (RO)

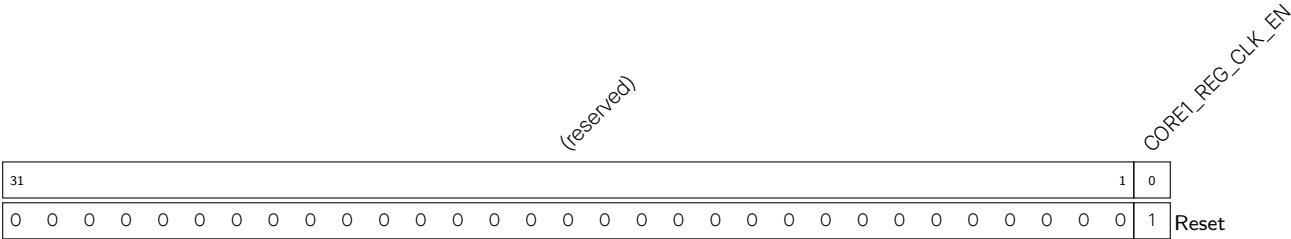
**Register 11.261. CORE1\_INTR\_STATUS\_REG\_2\_REG (0x0208)**

**CORE1\_INTR\_STATUS\_2** Represents the status of the interrupt sources from 64 ~ 95. Each bit corresponds to one interrupt source. (RO)

**Register 11.262. CORE1\_INTR\_STATUS\_REG\_3\_REG (0x020C)**

**CORE1\_INTR\_STATUS\_3** Represents the status of the interrupt sources numbered from 96 ~ 127. Bit 0 ~ 31 each corresponds to one interrupt source. (RO)

Register 11.263. CORE1\_CLOCK\_GATE\_REG (0x0210)

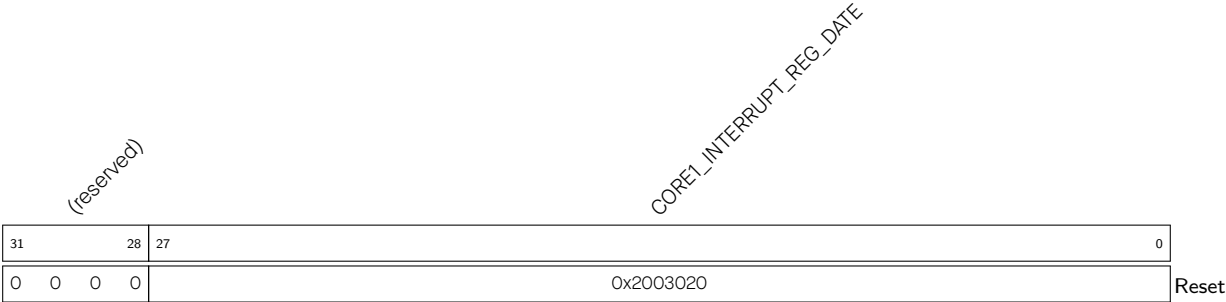


**CORE1\_REG\_CLK\_EN** Configures whether to force interrupt register clock-date on.

- 0: No effect
- 1: Force interrupt register clock-gate on

(R/W)

Register 11.264. CORE1\_INTERRUPT\_REG\_DATE\_REG (0x03FC)



**CORE1\_INTERRUPT\_REG\_DATE** Version control register. (R/W)

## Chapter 12

### Event Task Matrix (ETM)

#### 12.1 Overview

The Event Task Matrix (ETM) peripheral contains 50 configurable channels. Each channel can map an event of any specified peripheral to a task of any specified peripheral. In this way, peripherals can be triggered to execute specified tasks without CPU intervention.

#### 12.2 Features

The Event Task Matrix has the following features:

- Receive various events from multiple peripherals
- Generate various tasks for multiple peripherals
- 50 independently configurable ETM channels
- An ETM channel can be set up to receive any event, and map it to any task
- Each ETM channel can be enabled independently. If not enabled, the channel will not respond to the configured event and generate the task mapped to that event
- Support for checking event and task status
- Peripherals supporting ETM include GPIO, LED PWM, general-purpose timers, RTC Timer, system timer, MCPWM, temperature sensor, ADC, I2S, LP CPU, GDMA-AHB, GDMA-AXI, 2D DMA, and PMU

Note that the 50 ETM channels are identical regarding their features and operations. Thus, in the following sections, ETM channels are collectively referred to as channel *n* (where *n* ranges from 0 to 49).

#### 12.3 Functional Description

##### 12.3.1 Architecture

The Event Task Matrix has 50 independent channels. A channel can choose any event as input, and map the event to any task as output (see Section 12.3.2 and Section 12.3.3 respectively). Each channel has an individual enable bit (see Section 12.3.6).

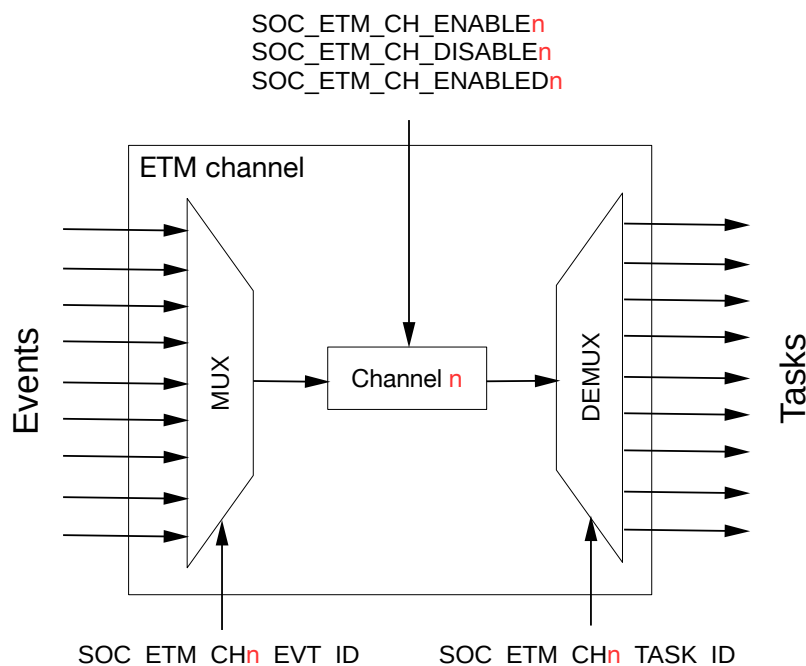
Figure 12.3-1. ETM Channel $n$  Architecture

Figure 12.3-1 illustrates the structure of an ETM channel. The `SOC_ETM_CH $n$ _EVT_ID` field configures the MUX (multiplexer) to select one of the events as the input of channel $n$ . The `SOC_ETM_CH $n$ _TASK_ID` field configures the DEMUX (demultiplexer) to map the event selected by channel $n$  to one of the tasks. `SOC_ETM_CH_ENABLE $n$`  and `SOC_ETM_CH_DISABLE $n$`  are used to enable or disable channel $n$ . `SOC_ETM_CH_ENABLED $n$`  is used to indicate the status of the channel $n$ .

## 12.3.2 Events

An ETM channel can be set up to choose which event to receive by configuring the `SOC_ETM_CH $n$ _EVT_ID` field. Table 12.3-1 shows the configuration values of `SOC_ETM_CH $n$ _EVT_ID` and their corresponding events.

Table 12.3-1. Selectable Events for ETM Channel $n$ 

| <code>SOC_ETM_CH<math>n</math>_EVT_ID</code> | Selected Event         | Peripheral Generating This Event |
|--|------------------------|----------------------------------|
| 1  | GPIO_EVT_CHO_RISE_EDGE | GPIO                             |
| 2  | GPIO_EVT_CH1_RISE_EDGE |                                  |
| 3  | GPIO_EVT_CH2_RISE_EDGE |                                  |
| 4  | GPIO_EVT_CH3_RISE_EDGE |                                  |
| 5  | GPIO_EVT_CH4_RISE_EDGE |                                  |
| 6  | GPIO_EVT_CH5_RISE_EDGE |                                  |
| 7  | GPIO_EVT_CH6_RISE_EDGE |                                  |
| 8  | GPIO_EVT_CH7_RISE_EDGE |                                  |
| 9  | GPIO_EVT_CHO_FALL_EDGE |                                  |
| 10   | GPIO_EVT_CH1_FALL_EDGE |                                  |

| SOC_ETM_CH $n$ _EVT_ID | Selected Event             | Peripheral Generating This Event |
|------------------------|----------------------------|----------------------------------|
| 11                     | GPIO_EVT_CH2_FALL_EDGE     |                                  |
| 12                     | GPIO_EVT_CH3_FALL_EDGE     |                                  |
| 13                     | GPIO_EVT_CH4_FALL_EDGE     |                                  |
| 14                     | GPIO_EVT_CH5_FALL_EDGE     |                                  |
| 15                     | GPIO_EVT_CH6_FALL_EDGE     |                                  |
| 16                     | GPIO_EVT_CH7_FALL_EDGE     |                                  |
| 17                     | GPIO_EVT_CH0_ANY_EDGE      |                                  |
| 18                     | GPIO_EVT_CH1_ANY_EDGE      |                                  |
| 19                     | GPIO_EVT_CH2_ANY_EDGE      |                                  |
| 20                     | GPIO_EVT_CH3_ANY_EDGE      |                                  |
| 21                     | GPIO_EVT_CH4_ANY_EDGE      |                                  |
| 22                     | GPIO_EVT_CH5_ANY_EDGE      |                                  |
| 23                     | GPIO_EVT_CH6_ANY_EDGE      |                                  |
| 24                     | GPIO_EVT_CH7_ANY_EDGE      |                                  |
| 25                     | GPIO_EVT_ZERO_DET_POS0     |                                  |
| 26                     | GPIO_EVT_ZERO_DET_NEG0     |                                  |
| 27                     | GPIO_EVT_ZERO_DET_POS1     |                                  |
| 28                     | GPIO_EVT_ZERO_DET_NEG1     |                                  |
| 29                     | LEDC_EVT_DUTY_CHNG_END_CH0 | LED PWM Controller (LEDC)        |
| 30                     | LEDC_EVT_DUTY_CHNG_END_CH1 |                                  |
| 31                     | LEDC_EVT_DUTY_CHNG_END_CH2 |                                  |
| 32                     | LEDC_EVT_DUTY_CHNG_END_CH3 |                                  |
| 33                     | LEDC_EVT_DUTY_CHNG_END_CH4 |                                  |
| 34                     | LEDC_EVT_DUTY_CHNG_END_CH5 |                                  |
| 35                     | LEDC_EVT_DUTY_CHNG_END_CH6 |                                  |
| 36                     | LEDC_EVT_DUTY_CHNG_END_CH7 |                                  |
| 37                     | LEDC_EVT_OVF_CNT_PLS_CH0   |                                  |
| 38                     | LEDC_EVT_OVF_CNT_PLS_CH1   |                                  |
| 39                     | LEDC_EVT_OVF_CNT_PLS_CH2   |                                  |
| 40                     | LEDC_EVT_OVF_CNT_PLS_CH3   |                                  |
| 41                     | LEDC_EVT_OVF_CNT_PLS_CH4   |                                  |
| 42                     | LEDC_EVT_OVF_CNT_PLS_CH5   |                                  |
| 43                     | LEDC_EVT_OVF_CNT_PLS_CH6   |                                  |
| 44                     | LEDC_EVT_OVF_CNT_PLS_CH7   |                                  |
| 45                     | LEDC_EVT_TIME_OVF_TIMER0   |                                  |
| 46                     | LEDC_EVT_TIME_OVF_TIMER1   |                                  |
| 47                     | LEDC_EVT_TIME_OVF_TIMER2   |                                  |
| 48                     | LEDC_EVT_TIME_OVF_TIMER3   |                                  |
| 49                     | LEDC_EVT_TIMER0_CMP        |                                  |
| 50                     | LEDC_EVT_TIMER1_CMP        |                                  |
| 51                     | LEDC_EVT_TIMER2_CMP        |                                  |
| 52                     | LEDC_EVT_TIMER3_CMP        |                                  |
| 53                     | TGO_EVT_CNT_CMP_TIMER0     | General-purpose timer group 0    |
| 55                     | TG1_EVT_CNT_CMP_TIMER0     | General-purpose timer group 1    |
| 57                     | SYSTIMER_EVT_CNT_CMPO      | System Timer                     |

| SOC_ETM_CH <sub>n</sub> _EVT_ID | Selected Event         | Peripheral Generating This Event |
|---------------------------------|------------------------|----------------------------------|
| 58                              | SYSTIMER_EVT_CNT_CMP1  |                                  |
| 59                              | SYSTIMER_EVT_CNT_CMP2  |                                  |
| 60                              | MCPWMO_EVT_TIMER0_STOP | MCPWMO                           |
| 61                              | MCPWMO_EVT_TIMER1_STOP |                                  |
| 62                              | MCPWMO_EVT_TIMER2_STOP |                                  |
| 63                              | MCPWMO_EVT_TIMER0_TEZ  |                                  |
| 64                              | MCPWMO_EVT_TIMER1_TEZ  |                                  |
| 65                              | MCPWMO_EVT_TIMER2_TEZ  |                                  |
| 66                              | MCPWMO_EVT_TIMER0_TEP  |                                  |
| 67                              | MCPWMO_EVT_TIMER1_TEP  |                                  |
| 68                              | MCPWMO_EVT_TIMER2_TEP  |                                  |
| 69                              | MCPWMO_EVT_OPO_TEA     |                                  |
| 70                              | MCPWMO_EVT_OP1_TEA     |                                  |
| 71                              | MCPWMO_EVT_OP2_TEA     |                                  |
| 72                              | MCPWMO_EVT_OPO_TEB     |                                  |
| 73                              | MCPWMO_EVT_OP1_TEB     |                                  |
| 74                              | MCPWMO_EVT_OP2_TEB     |                                  |
| 75                              | MCPWMO_EVT_F0          |                                  |
| 76                              | MCPWMO_EVT_F1          |                                  |
| 77                              | MCPWMO_EVT_F2          |                                  |
| 78                              | MCPWMO_EVT_F0_CLR      |                                  |
| 79                              | MCPWMO_EVT_F1_CLR      |                                  |
| 80                              | MCPWMO_EVT_F2_CLR      |                                  |
| 81                              | MCPWMO_EVT_TZ0_CBC     |                                  |
| 82                              | MCPWMO_EVT_TZ1_CBC     |                                  |
| 83                              | MCPWMO_EVT_TZ2_CBC     |                                  |
| 84                              | MCPWMO_EVT_TZ0_OST     |                                  |
| 85                              | MCPWMO_EVT_TZ1_OST     |                                  |
| 86                              | MCPWMO_EVT_TZ2_OST     |                                  |
| 87                              | MCPWMO_EVT_CAP0        |                                  |
| 88                              | MCPWMO_EVT_CAP1        |                                  |
| 89                              | MCPWMO_EVT_CAP2        |                                  |
| 90                              | MCPWMO_EVT_OPO_TEE1    |                                  |
| 91                              | MCPWMO_EVT_OP1_TEE1    |                                  |
| 92                              | MCPWMO_EVT_OP2_TEE1    |                                  |
| 93                              | MCPWMO_EVT_OPO_TEE2    |                                  |
| 94                              | MCPWMO_EVT_OP1_TEE2    |                                  |
| 95                              | MCPWMO_EVT_OP2_TEE2    |                                  |
| 96                              | MCPWM1_EVT_TIMER0_STOP | MCPWM1                           |
| 97                              | MCPWM1_EVT_TIMER1_STOP |                                  |
| 98                              | MCPWM1_EVT_TIMER2_STOP |                                  |
| 99                              | MCPWM1_EVT_TIMER0_TEZ  |                                  |
| 100                             | MCPWM1_EVT_TIMER1_TEZ  |                                  |
| 101                             | MCPWM1_EVT_TIMER2_TEZ  |                                  |
| 102                             | MCPWM1_EVT_TIMER0_TEP  |                                  |

| SOC_ETM_CH $n$ _EVT_ID | Selected Event            | Peripheral Generating This Event |
|------------------------|---------------------------|----------------------------------|
| 103                    | MCPWM1_EVT_TIMER1_TEP     |                                  |
| 104                    | MCPWM1_EVT_TIMER2_TEP     |                                  |
| 105                    | MCPWM1_EVT_OPO_TEA        |                                  |
| 106                    | MCPWM1_EVT_OP1_TEA        |                                  |
| 107                    | MCPWM1_EVT_OP2_TEA        |                                  |
| 108                    | MCPWM1_EVT_OPO_TEB        |                                  |
| 109                    | MCPWM1_EVT_OP1_TEB        |                                  |
| 110                    | MCPWM1_EVT_OP2_TEB        |                                  |
| 111                    | MCPWM1_EVT_F0             |                                  |
| 112                    | MCPWM1_EVT_F1             |                                  |
| 113                    | MCPWM1_EVT_F2             |                                  |
| 114                    | MCPWM1_EVT_F0_CLR         |                                  |
| 115                    | MCPWM1_EVT_F1_CLR         |                                  |
| 116                    | MCPWM1_EVT_F2_CLR         |                                  |
| 117                    | MCPWM1_EVT_TZ0_CBC        |                                  |
| 118                    | MCPWM1_EVT_TZ1_CBC        |                                  |
| 119                    | MCPWM1_EVT_TZ2_CBC        |                                  |
| 120                    | MCPWM1_EVT_TZ0_OST        |                                  |
| 121                    | MCPWM1_EVT_TZ1_OST        |                                  |
| 122                    | MCPWM1_EVT_TZ2_OST        |                                  |
| 123                    | MCPWM1_EVT_CAPO           |                                  |
| 124                    | MCPWM1_EVT_CAP1           |                                  |
| 125                    | MCPWM1_EVT_CAP2           |                                  |
| 126                    | MCPWM1_EVT_OPO_TEE1       |                                  |
| 127                    | MCPWM1_EVT_OP1_TEE1       |                                  |
| 128                    | MCPWM1_EVT_OP2_TEE1       |                                  |
| 129                    | MCPWM1_EVT_OPO_TEE2       |                                  |
| 130                    | MCPWM1_EVT_OP1_TEE2       |                                  |
| 131                    | MCPWM1_EVT_OP2_TEE2       |                                  |
| 132                    | ADC_EVT_CONV_CMPLT0       | ADC Controller (ADC)             |
| 133                    | ADC_EVT_EQ_ABOVE_THRESH0  |                                  |
| 134                    | ADC_EVT_EQ_ABOVE_THRESH1  |                                  |
| 135                    | ADC_EVT_EQ_BELOW_THRESH0  |                                  |
| 136                    | ADC_EVT_EQ_BELOW_THRESH1  |                                  |
| 138                    | ADC_EVT_STOPPED0          |                                  |
| 139                    | ADC_EVT_STARTED0          |                                  |
| 148                    | TMPSNSR_EVT_OVER_LIMIT    | Temperature Sensor (TSENS)       |
| 149                    | I2SO_EVT_RX_DONE          | I2SO                             |
| 150                    | I2SO_EVT_TX_DONE          |                                  |
| 151                    | I2SO_EVT_X_WORDS_RECEIVED |                                  |
| 152                    | I2SO_EVT_X_WORDS_SENT     |                                  |
| 153                    | I2S1_EVT_RX_DONE          | I2S1                             |
| 154                    | I2S1_EVT_TX_DONE          |                                  |
| 155                    | I2S1_EVT_X_WORDS_RECEIVED |                                  |



| SOC_ETM_CH $n$ _EVT_ID | Selected Event                  | Peripheral Generating This Event |
|------------------------|---------------------------------|----------------------------------|
| 156                    | I2S1_EVT_X_WORDS_SENT           |                                  |
| 157                    | I2S2_EVT_RX_DONE                | I2S2                             |
| 158                    | I2S2_EVT_TX_DONE                |                                  |
| 159                    | I2S2_EVT_X_WORDS_RECEIVED       |                                  |
| 160                    | I2S2_EVT_X_WORDS_SENT           |                                  |
| 161                    | ULP_EVT_ERR_INTR                | Low-Power CPU                    |
| 162                    | ULP_EVT_HALT                    |                                  |
| 163                    | ULP_EVT_START_INTR              |                                  |
| 164                    | RTC_EVT_TICK                    | RTC Timer                        |
| 165                    | RTC_EVT_OVF                     |                                  |
| 166                    | RTC_EVT_CMP                     |                                  |
| 167                    | GDMA_AHB_EVT_IN_DONE_CHO        | GDMA-AHB                         |
| 168                    | GDMA_AHB_EVT_IN_DONE_CH1        |                                  |
| 169                    | GDMA_AHB_EVT_IN_DONE_CH2        |                                  |
| 170                    | GDMA_AHB_EVT_IN_SUC_EOF_CHO     |                                  |
| 171                    | GDMA_AHB_EVT_IN_SUC_EOF_CH1     |                                  |
| 172                    | GDMA_AHB_EVT_IN_SUC_EOF_CH2     |                                  |
| 173                    | GDMA_AHB_EVT_IN_FIFO_EMPTY_CHO  |                                  |
| 174                    | GDMA_AHB_EVT_IN_FIFO_EMPTY_CH1  |                                  |
| 175                    | GDMA_AHB_EVT_IN_FIFO_EMPTY_CH2  |                                  |
| 176                    | GDMA_AHB_EVT_IN_FIFO_FULL_CHO   |                                  |
| 177                    | GDMA_AHB_EVT_IN_FIFO_FULL_CH1   |                                  |
| 178                    | GDMA_AHB_EVT_IN_FIFO_FULL_CH2   |                                  |
| 179                    | GDMA_AHB_EVT_OUT_DONE_CHO       |                                  |
| 180                    | GDMA_AHB_EVT_OUT_DONE_CH1       |                                  |
| 181                    | GDMA_AHB_EVT_OUT_DONE_CH2       |                                  |
| 182                    | GDMA_AHB_EVT_OUT_EOF_CHO        |                                  |
| 183                    | GDMA_AHB_EVT_OUT_EOF_CH1        |                                  |
| 184                    | GDMA_AHB_EVT_OUT_EOF_CH2        |                                  |
| 185                    | GDMA_AHB_EVT_OUT_TOTAL_EOF_CHO  |                                  |
| 186                    | GDMA_AHB_EVT_OUT_TOTAL_EOF_CH1  |                                  |
| 187                    | GDMA_AHB_EVT_OUT_TOTAL_EOF_CH2  |                                  |
| 188                    | GDMA_AHB_EVT_OUT_FIFO_EMPTY_CHO |                                  |
| 189                    | GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH1 |                                  |
| 190                    | GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH2 |                                  |
| 191                    | GDMA_AHB_EVT_OUT_FIFO_FULL_CHO  |                                  |
| 192                    | GDMA_AHB_EVT_OUT_FIFO_FULL_CH1  |                                  |
| 193                    | GDMA_AHB_EVT_OUT_FIFO_FULL_CH2  |                                  |
| 194                    | GDMA_AXI_EVT_IN_DONE_CHO        | GDMA-AXI                         |
| 195                    | GDMA_AXI_EVT_IN_DONE_CH1        |                                  |
| 196                    | GDMA_AXI_EVT_IN_DONE_CH2        |                                  |
| 197                    | GDMA_AXI_EVT_IN_SUC_EOF_CHO     |                                  |
| 198                    | GDMA_AXI_EVT_IN_SUC_EOF_CH1     |                                  |
| 199                    | GDMA_AXI_EVT_IN_SUC_EOF_CH2     |                                  |
| 200                    | GDMA_AXI_EVT_IN_FIFO_EMPTY_CHO  |                                  |

| SOC_ETM_CH $n$ _EVT_ID | Selected Event                  | Peripheral Generating This Event |
|------------------------|---------------------------------|----------------------------------|
| 201                    | GDMA_AXI_EVT_IN_FIFO_EMPTY_CH1  |                                  |
| 202                    | GDMA_AXI_EVT_IN_FIFO_EMPTY_CH2  |                                  |
| 203                    | GDMA_AXI_EVT_IN_FIFO_FULL_CHO   |                                  |
| 204                    | GDMA_AXI_EVT_IN_FIFO_FULL_CH1   |                                  |
| 205                    | GDMA_AXI_EVT_IN_FIFO_FULL_CH2   |                                  |
| 206                    | GDMA_AXI_EVT_OUT_DONE_CHO       |                                  |
| 207                    | GDMA_AXI_EVT_OUT_DONE_CH1       |                                  |
| 208                    | GDMA_AXI_EVT_OUT_DONE_CH2       |                                  |
| 209                    | GDMA_AXI_EVT_OUT_EOF_CHO        |                                  |
| 210                    | GDMA_AXI_EVT_OUT_EOF_CH1        |                                  |
| 211                    | GDMA_AXI_EVT_OUT_EOF_CH2        |                                  |
| 212                    | GDMA_AXI_EVT_OUT_TOTAL_EOF_CHO  |                                  |
| 213                    | GDMA_AXI_EVT_OUT_TOTAL_EOF_CH1  |                                  |
| 214                    | GDMA_AXI_EVT_OUT_TOTAL_EOF_CH2  |                                  |
| 215                    | GDMA_AXI_EVT_OUT_FIFO_EMPTY_CHO |                                  |
| 216                    | GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH1 |                                  |
| 217                    | GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2 |                                  |
| 218                    | GDMA_AXI_EVT_OUT_FIFO_FULL_CHO  |                                  |
| 219                    | GDMA_AXI_EVT_OUT_FIFO_FULL_CH1  |                                  |
| 220                    | GDMA_AXI_EVT_OUT_FIFO_FULL_CH2  |                                  |
| 221                    | PMU_EVT_SLEEP_WEEKUP            | PMU                              |
| 222                    | DMA2D_EVT_IN_DONE_CHO           | 2D-DMA Controller (2D-DMA)       |
| 223                    | DMA2D_EVT_IN_DONE_CH1           |                                  |
| 224                    | DMA2D_EVT_IN_SUC_EOF_CHO        |                                  |
| 225                    | DMA2D_EVT_IN_SUC_EOF_CH1        |                                  |
| 226                    | DMA2D_EVT_OUT_DONE_CHO          |                                  |
| 227                    | DMA2D_EVT_OUT_DONE_CH1          |                                  |
| 228                    | DMA2D_EVT_OUT_DONE_CH2          |                                  |
| 229                    | DMA2D_EVT_OUT_EOF_CHO           |                                  |
| 230                    | DMA2D_EVT_OUT_EOF_CH1           |                                  |
| 231                    | DMA2D_EVT_OUT_EOF_CH2           |                                  |
| 232                    | DMA2D_EVT_OUT_TOTAL_EOF_CHO     |                                  |
| 233                    | DMA2D_EVT_OUT_TOTAL_EOF_CH1     |                                  |
| 234                    | DMA2D_EVT_OUT_TOTAL_EOF_CH2     |                                  |

Whenever any of these events occurs, the corresponding peripheral generates a pulse signal. As soon as the pulse signal is high, the event is considered as being received.

For more detailed descriptions of an event, please refer to the chapter for the peripheral generating this event.

### 12.3.3 Tasks

An ETM channel can be set up to map its event to one of the tasks by configuring the `SOC_ETM_CH $n$ _TASK_ID` field. Table 12.3-2 shows the configuration values of `SOC_ETM_CH $n$ _TASK_ID` and

their corresponding tasks.

**Table 12.3-2. Mappable Tasks for ETM Channel  $n$**

| SOC_ETM_CH $n$ _TASK_ID | Mapped Task                     | Peripheral Receiving This Task |
|-------------------------|---------------------------------|--------------------------------|
| 1                       | GPIO_TASK_CH0_SET               | GPIO                           |
| 2                       | GPIO_TASK_CH1_SET               |                                |
| 3                       | GPIO_TASK_CH2_SET               |                                |
| 4                       | GPIO_TASK_CH3_SET               |                                |
| 5                       | GPIO_TASK_CH4_SET               |                                |
| 6                       | GPIO_TASK_CH5_SET               |                                |
| 7                       | GPIO_TASK_CH6_SET               |                                |
| 8                       | GPIO_TASK_CH7_SET               |                                |
| 9                       | GPIO_TASK_CH0_CLEAR             |                                |
| 10                      | GPIO_TASK_CH1_CLEAR             |                                |
| 11                      | GPIO_TASK_CH2_CLEAR             |                                |
| 12                      | GPIO_TASK_CH3_CLEAR             |                                |
| 13                      | GPIO_TASK_CH4_CLEAR             |                                |
| 14                      | GPIO_TASK_CH5_CLEAR             |                                |
| 15                      | GPIO_TASK_CH6_CLEAR             |                                |
| 16                      | GPIO_TASK_CH7_CLEAR             |                                |
| 17                      | GPIO_TASK_CH0_TOGGLE            |                                |
| 18                      | GPIO_TASK_CH1_TOGGLE            |                                |
| 19                      | GPIO_TASK_CH2_TOGGLE            |                                |
| 20                      | GPIO_TASK_CH3_TOGGLE            |                                |
| 21                      | GPIO_TASK_CH4_TOGGLE            |                                |
| 22                      | GPIO_TASK_CH5_TOGGLE            |                                |
| 23                      | GPIO_TASK_CH6_TOGGLE            |                                |
| 24                      | GPIO_TASK_CH7_TOGGLE            |                                |
| 25                      | LEDC_TASK_TIMER0_RES_UPDATE     | LED PWM Controller (LEDC)      |
| 26                      | LEDC_TASK_TIMER1_RES_UPDATE     |                                |
| 27                      | LEDC_TASK_TIMER2_RES_UPDATE     |                                |
| 28                      | LEDC_TASK_TIMER3_RES_UPDATE     |                                |
| 29                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH0 |                                |
| 30                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH1 |                                |
| 31                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH2 |                                |
| 32                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH3 |                                |
| 33                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH4 |                                |
| 34                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH5 |                                |
| 35                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH6 |                                |
| 36                      | LEDC_TASK_DUTY_SCALE_UPDATE_CH7 |                                |
| 37                      | LEDC_TASK_TIMER0_CAP            |                                |
| 38                      | LEDC_TASK_TIMER1_CAP            |                                |
| 39                      | LEDC_TASK_TIMER2_CAP            |                                |
| 40                      | LEDC_TASK_TIMER3_CAP            |                                |
| 41                      | LEDC_TASK_SIG_OUT_DIS_CH0       |                                |

| SOC_ETM_CHn_TASK_ID | Mapped Task                 | Peripheral Receiving This Task |
|---------------------|-----------------------------|--------------------------------|
| 42                  | LEDC_TASK_SIG_OUT_DIS_CH1   |                                |
| 43                  | LEDC_TASK_SIG_OUT_DIS_CH2   |                                |
| 44                  | LEDC_TASK_SIG_OUT_DIS_CH3   |                                |
| 45                  | LEDC_TASK_SIG_OUT_DIS_CH4   |                                |
| 46                  | LEDC_TASK_SIG_OUT_DIS_CH5   |                                |
| 47                  | LEDC_TASK_SIG_OUT_DIS_CH6   |                                |
| 48                  | LEDC_TASK_SIG_OUT_DIS_CH7   |                                |
| 49                  | LEDC_TASK_OVF_CNT_RST_CHO   |                                |
| 50                  | LEDC_TASK_OVF_CNT_RST_CH1   |                                |
| 51                  | LEDC_TASK_OVF_CNT_RST_CH2   |                                |
| 52                  | LEDC_TASK_OVF_CNT_RST_CH3   |                                |
| 53                  | LEDC_TASK_OVF_CNT_RST_CH4   |                                |
| 54                  | LEDC_TASK_OVF_CNT_RST_CH5   |                                |
| 55                  | LEDC_TASK_OVF_CNT_RST_CH6   |                                |
| 56                  | LEDC_TASK_OVF_CNT_RST_CH7   |                                |
| 57                  | LEDC_TASK_TIMER0_RST        |                                |
| 58                  | LEDC_TASK_TIMER1_RST        |                                |
| 59                  | LEDC_TASK_TIMER2_RST        |                                |
| 60                  | LEDC_TASK_TIMER3_RST        |                                |
| 61                  | LEDC_TASK_TIMER0_RESUME     |                                |
| 62                  | LEDC_TASK_TIMER1_RESUME     |                                |
| 63                  | LEDC_TASK_TIMER2_RESUME     |                                |
| 64                  | LEDC_TASK_TIMER3_RESUME     |                                |
| 65                  | LEDC_TASK_TIMER0_PAUSE      |                                |
| 66                  | LEDC_TASK_TIMER1_PAUSE      |                                |
| 67                  | LEDC_TASK_TIMER2_PAUSE      |                                |
| 68                  | LEDC_TASK_TIMER3_PAUSE      |                                |
| 69                  | LEDC_TASK_GAMMA_RESTART_CHO |                                |
| 70                  | LEDC_TASK_GAMMA_RESTART_CH1 |                                |
| 71                  | LEDC_TASK_GAMMA_RESTART_CH2 |                                |
| 72                  | LEDC_TASK_GAMMA_RESTART_CH3 |                                |
| 73                  | LEDC_TASK_GAMMA_RESTART_CH4 |                                |
| 74                  | LEDC_TASK_GAMMA_RESTART_CH5 |                                |
| 75                  | LEDC_TASK_GAMMA_RESTART_CH6 |                                |
| 76                  | LEDC_TASK_GAMMA_RESTART_CH7 |                                |
| 77                  | LEDC_TASK_GAMMA_PAUSE_CHO   |                                |
| 78                  | LEDC_TASK_GAMMA_PAUSE_CH1   |                                |
| 79                  | LEDC_TASK_GAMMA_PAUSE_CH2   |                                |
| 80                  | LEDC_TASK_GAMMA_PAUSE_CH3   |                                |
| 81                  | LEDC_TASK_GAMMA_PAUSE_CH4   |                                |
| 82                  | LEDC_TASK_GAMMA_PAUSE_CH5   |                                |
| 83                  | LEDC_TASK_GAMMA_PAUSE_CH6   |                                |
| 84                  | LEDC_TASK_GAMMA_PAUSE_CH7   |                                |
| 85                  | LEDC_TASK_GAMMA_RESUME_CHO  |                                |
| 86                  | LEDC_TASK_GAMMA_RESUME_CH1  |                                |

| SOC_ETM_CH <sub>n</sub> _TASK_ID | Mapped Task                  | Peripheral Receiving This Task |
|----------------------------------|------------------------------|--------------------------------|
| 87                               | LEDC_TASK_GAMMA_RESUME_CH2   |                                |
| 88                               | LEDC_TASK_GAMMA_RESUME_CH3   |                                |
| 89                               | LEDC_TASK_GAMMA_RESUME_CH4   |                                |
| 90                               | LEDC_TASK_GAMMA_RESUME_CH5   |                                |
| 91                               | LEDC_TASK_GAMMA_RESUME_CH6   |                                |
| 92                               | LEDC_TASK_GAMMA_RESUME_CH7   |                                |
| 93                               | TGO_TASK_CNT_START_TIMER0    | General-purpose timer group 0  |
| 94                               | TGO_TASK_ALARM_START_TIMER0  |                                |
| 95                               | TGO_TASK_CNT_STOP_TIMER0     |                                |
| 96                               | TGO_TASK_CNT_RELOAD_TIMER0   |                                |
| 97                               | TGO_TASK_CNT_CAP_TIMER0      |                                |
| 103                              | TG1_TASK_CNT_START_TIMER0    | General-purpose timer group 1  |
| 104                              | TG1_TASK_ALARM_START_TIMER0  |                                |
| 105                              | TG1_TASK_CNT_STOP_TIMER0     |                                |
| 106                              | TG1_TASK_CNT_RELOAD_TIMER0   |                                |
| 107                              | TG1_TASK_CNT_CAP_TIMER0      |                                |
| 113                              | MCPWMO_TASK_CMPRO_A_UP       | MCPWMO                         |
| 114                              | MCPWMO_TASK_CMPR1_A_UP       |                                |
| 115                              | MCPWMO_TASK_CMPR2_A_UP       |                                |
| 116                              | MCPWMO_TASK_CMPRO_B_UP       |                                |
| 117                              | MCPWMO_TASK_CMPR1_B_UP       |                                |
| 118                              | MCPWMO_TASK_CMPR2_B_UP       |                                |
| 119                              | MCPWMO_TASK_GEN_STOP         |                                |
| 120                              | MCPWMO_TASK_TIMER0_SYN       |                                |
| 121                              | MCPWMO_TASK_TIMER1_SYN       |                                |
| 122                              | MCPWMO_TASK_TIMER2_SYN       |                                |
| 123                              | MCPWMO_TASK_TIMER0_PERIOD_UP |                                |
| 124                              | MCPWMO_TASK_TIMER1_PERIOD_UP |                                |
| 125                              | MCPWMO_TASK_TIMER2_PERIOD_UP |                                |
| 126                              | MCPWMO_TASK_TZO_OST          |                                |
| 127                              | MCPWMO_TASK_TZ1_OST          |                                |
| 128                              | MCPWMO_TASK_TZ2_OST          |                                |
| 129                              | MCPWMO_TASK_CLR0_OST         |                                |
| 130                              | MCPWMO_TASK_CLR1_OST         |                                |
| 131                              | MCPWMO_TASK_CLR2_OST         |                                |
| 132                              | MCPWMO_TASK_CAPO             |                                |
| 133                              | MCPWMO_TASK_CAP1             |                                |
| 134                              | MCPWMO_TASK_CAP2             |                                |
| 135                              | MCPWM1_TASK_CMPRO_A_UP       | MCPWM1                         |
| 136                              | MCPWM1_TASK_CMPR1_A_UP       |                                |
| 137                              | MCPWM1_TASK_CMPR2_A_UP       |                                |
| 138                              | MCPWM1_TASK_CMPRO_B_UP       |                                |
| 139                              | MCPWM1_TASK_CMPR1_B_UP       |                                |
| 140                              | MCPWM1_TASK_CMPR2_B_UP       |                                |
| 141                              | MCPWM1_TASK_GEN_STOP         |                                |

| SOC_ETM_CHn_TASK_ID | Mapped Task                  | Peripheral Receiving This Task |
|---------------------|------------------------------|--------------------------------|
| 142                 | MCPWM1_TASK_TIMER0_SYN       |                                |
| 143                 | MCPWM1_TASK_TIMER1_SYN       |                                |
| 144                 | MCPWM1_TASK_TIMER2_SYN       |                                |
| 145                 | MCPWM1_TASK_TIMER0_PERIOD_UP |                                |
| 146                 | MCPWM1_TASK_TIMER1_PERIOD_UP |                                |
| 147                 | MCPWM1_TASK_TIMER2_PERIOD_UP |                                |
| 148                 | MCPWM1_TASK_TZ0_OST          |                                |
| 149                 | MCPWM1_TASK_TZ1_OST          |                                |
| 150                 | MCPWM1_TASK_TZ2_OST          |                                |
| 151                 | MCPWM1_TASK_CLR0_OST         |                                |
| 152                 | MCPWM1_TASK_CLR1_OST         |                                |
| 153                 | MCPWM1_TASK_CLR2_OST         |                                |
| 154                 | MCPWM1_TASK_CAP0             |                                |
| 155                 | MCPWM1_TASK_CAP1             |                                |
| 156                 | MCPWM1_TASK_CAP2             |                                |
| 157                 | ADC_TASK_SAMPLE0             | ADC Controller (ADC)           |
| 159                 | ADC_TASK_START0              |                                |
| 160                 | ADC_TASK_STOP0               |                                |
| 165                 | TMPSNSR_TASK_START_SAMPLE    | Temperature Sensor (TSENS)     |
| 166                 | TMPSNSR_TASK_STOP_SAMPLE     |                                |
| 167                 | I2S0_TASK_START_RX           | I2S0                           |
| 168                 | I2S0_TASK_START_TX           |                                |
| 169                 | I2S0_TASK_STOP_RX            |                                |
| 170                 | I2S0_TASK_STOP_TX            |                                |
| 171                 | I2S1_TASK_START_RX           | I2S1                           |
| 172                 | I2S1_TASK_START_TX           |                                |
| 173                 | I2S1_TASK_STOP_RX            |                                |
| 174                 | I2S1_TASK_STOP_TX            |                                |
| 175                 | I2S2_TASK_START_RX           | I2S2                           |
| 176                 | I2S2_TASK_START_TX           |                                |
| 177                 | I2S2_TASK_STOP_RX            |                                |
| 178                 | I2S2_TASK_STOP_TX            |                                |
| 179                 | ULP_TASK_WEAKUP_CPU          | Low-Power CPU                  |
| 180                 | ULP_TASK_INT_CPU             |                                |
| 185                 | GDMA_AHB_TASK_IN_START_CH0   | GDMA-AHB                       |
| 186                 | GDMA_AHB_TASK_IN_START_CH1   |                                |
| 187                 | GDMA_AHB_TASK_IN_START_CH2   |                                |
| 188                 | GDMA_AHB_TASK_OUT_START_CH0  |                                |
| 189                 | GDMA_AHB_TASK_OUT_START_CH1  |                                |
| 190                 | GDMA_AHB_TASK_OUT_START_CH2  |                                |
| 191                 | GDMA_AXI_TASK_IN_START_CH0   | GDMA-AXI                       |
| 192                 | GDMA_AXI_TASK_IN_START_CH1   |                                |
| 193                 | GDMA_AXI_TASK_IN_START_CH2   |                                |
| 194                 | GDMA_AXI_TASK_OUT_START_CH0  |                                |
| 195                 | GDMA_AXI_TASK_OUT_START_CH1  |                                |

| SOC_ETM_CH $n$ _TASK_ID | Mapped Task                   | Peripheral Receiving This Task |
|-------------------------|-------------------------------|--------------------------------|
| 196                     | GDMA_AXI_TASK_OUT_START_CH2   |                                |
| 197                     | PMU_TASK_SLEEP_REQ            | PMU                            |
| 198                     | DMA2D_TASK_IN_START_CH0       | 2D-DMA Controller (2D-DMA)     |
| 199                     | DMA2D_TASK_IN_START_CH1       |                                |
| 200                     | DMA2D_TASK_IN_DSCR_READY_CH0  |                                |
| 201                     | DMA2D_TASK_IN_DSCR_READY_CH1  |                                |
| 202                     | DMA2D_TASK_OUT_START_CH0      |                                |
| 203                     | DMA2D_TASK_OUT_START_CH1      |                                |
| 204                     | DMA2D_TASK_OUT_START_CH2      |                                |
| 205                     | DMA2D_TASK_OUT_DSCR_READY_CH0 |                                |
| 206                     | DMA2D_TASK_OUT_DSCR_READY_CH1 |                                |
| 207                     | DMA2D_TASK_OUT_DSCR_READY_CH2 |                                |

When a channel receives a valid event pulse signal, it generates the mapped task pulse signal.

For more detailed descriptions of a task, please refer to the chapter for the peripheral receiving this task.

Events from different channels can be optionally mapped to the same task. For example, field [SOC\\_ETM\\_CH \$n\$ \\_TASK\\_ID](#) of multiple channels can be configured with the same value, and field [SOC\\_ETM\\_CH \$n\$ \\_EVT\\_ID](#) can be configured with the same or different values. In this case, when the event received by any of the channels is valid, the task is generated. If events received by multiple channels are valid at the same time, the task will be generated only once.

### 12.3.4 Event and Task Status

The ETM module supports checking the status of events and tasks by reading registers as follows:

- Event status can be checked by reading the [SOC\\_ETM\\_EVT\\_ST \$n\$ \\_REG](#) register. If the field corresponding to an event is 1, it indicates that the event has been received by ETM. Otherwise, it indicates that the event has not been received by ETM. The fields in the [SOC\\_ETM\\_EVT\\_ST \$n\$ \\_REG](#) register can be cleared by writing 1 to the corresponding fields in the [SOC\\_ETM\\_EVT\\_ST \$n\$ \\_CLR\\_REG](#) register.
- Task status can be checked by reading the [SOC\\_ETM\\_TASK\\_ST \$n\$ \\_REG](#) register. If the field corresponding to a task is 1, it indicates that the task has been generated by ETM. Otherwise, it indicates that the task has not been generated by ETM. The fields in the [SOC\\_ETM\\_TASK\\_ST \$n\$ \\_REG](#) register can be cleared by writing 1 to the corresponding fields in the [SOC\\_ETM\\_TASK\\_ST \$n\$ \\_CLR\\_REG](#) register.

### 12.3.5 Timing Considerations

Figure [12.3-2](#) shows the structure of clocks that drive received events, sent tasks, and ETM channels.

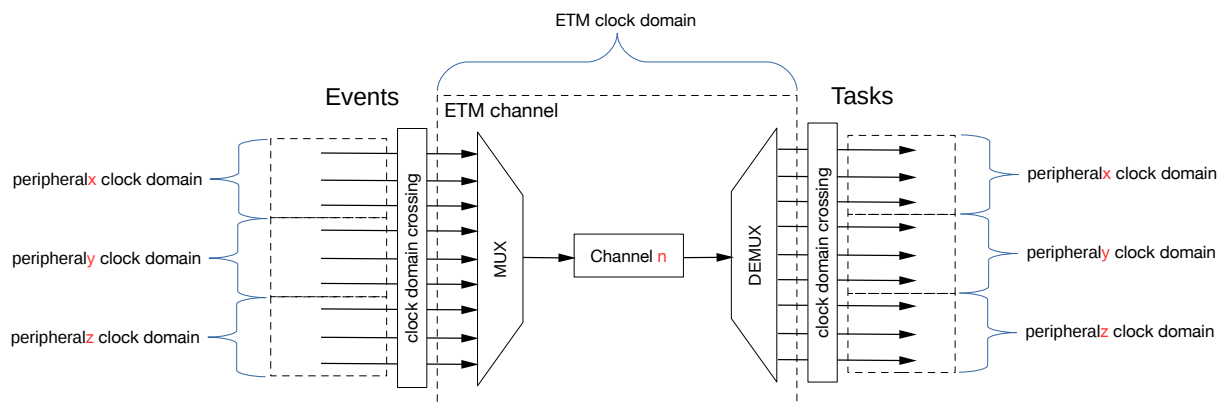


Figure 12.3-2. Event Task Matrix Clock Architecture

ETM is running at the SYS\_CLK domain (see Chapter 9 *Reset and Clock*). Each event corresponds to a pulse signal generated by the corresponding peripheral in its clock domain, while each task is mapped by the ETM to a pulse signal under its corresponding peripheral clock domain. The peripherals generating events, the Event Task Matrix, and peripherals receiving tasks are not necessarily running off the same clock and as such need to be synchronized. Therefore, to avoid event loss, there should be a delay between two consecutive event pulses which is dependent on the clock of the peripheral generating the event, on the ETM's clock, and on the clock of the peripheral executing the task.

To make sure the Event Task Matrix receives every event successfully, for peripherals generating event pulses, the interval between two consecutive pulses must be greater than one ETM clock cycle, namely  $\text{ceil}(\frac{\text{peripheral\_clock\_frequency}}{\text{ETM\_clock\_frequency}})$  in the unit of peripheral clock cycles.

For example, assuming that peripheral A is in the 80 MHz clock domain (REF\_80M\_CLK), and the ETM runs in the 40 MHz clock domain (SYS\_CLK). Peripheral A generates event 1, which should be received by ETM. To receive each event 1 successfully, the interval between two consecutive event 1 must be greater than two peripheral A clock cycles (i.e., one ETM clock cycle).

Likewise, to make sure the Event Task Matrix maps the received event (i.e., event synchronized to the ETM's clock domain) successfully to a task, the interval between two consecutive event pulses in the ETM clock domain must be greater than one peripheral clock cycle, namely  $\text{ceil}(\frac{\text{ETM\_clock\_frequency}}{\text{peripheral\_clock\_frequency}})$  in the unit of ETM clock cycles.

For example, assuming that peripheral B is in the 20 MHz clock domain (FOSC\_20M\_CLK), and the ETM runs in the 40 MHz clock domain (SYS\_CLK). ETM maps an event to task 1, which should be received by peripheral B. To map each received event successfully to task 1, the interval between two consecutive events must be greater than two ETM clock cycles (i.e., one peripheral B clock cycle).

As a result, to map two consecutive events generated by peripheral A to peripheral B, the interval between these two events must be  $\text{ceil}(\frac{\text{peripheral\_A\_clock\_frequency}}{\text{ETM\_clock\_frequency}}) * \text{ceil}(\frac{\text{ETM\_clock\_frequency}}{\text{peripheral\_B\_clock\_frequency}})$  in the unit of peripheral A clock cycles.

For example, assuming that peripheral A is in the 80 MHz clock domain (REF\_80M\_CLK), peripheral B is in the 20 MHz clock domain (FOSC\_20M\_CLK), and the ETM runs in the 40 MHz clock domain (SYS\_CLK). ETM maps event 1 generated by peripheral A to task 1 received by peripheral B. To successfully map each event 1 to task 1, the interval between two consecutive event 1 must be greater than  $2 * 2 = 4$  peripheral A clock



cycles.

### 12.3.6 Channel Control

Each ETM channel can be independently configured to be enabled or disabled. When channel *n* is enabled and receives the event configured via `SOC_ETM_CHn_EVT_ID`, it maps the event to the task configured via `SOC_ETM_CHn_TASK_ID`. When channel *n* is disabled, even if it receives the event configured via `SOC_ETM_CHn_EVT_ID`, no task will be generated.

To enable ETM channel *n*, write 1 to `SOC_ETM_CH_ENABLEn`. To disable ETM channel *n*, Write 1 to `SOC_ETM_CH_DISABLEn`.

The status of ETM channel *n* can be obtained by reading `SOC_ETM_CH_ENABLEDn`. 1 indicates that channel *n* has been enabled, and 0 indicates disabled.

If `SOC_ETM_CHn_EVT_ID` or `SOC_ETM_CHn_TASK_ID` is configured to 0, ETM channel *n* will also be disabled.

The complete procedure to configure ETM channel *n* is as follows:

1. Enable the ETM's clock by writing 1 to `HP_SYS_CLKRST_REG_ETM_SYS_CLK_EN`
2. Select the event to be received by channel *n* via `SOC_ETM_CHn_EVT_ID`
3. Select the task mapped to the received event via `SOC_ETM_CHn_TASK_ID`
4. Enable channel *n* by setting `SOC_ETM_CH_ENABLEn`
5. When channel *n* no longer needs to map the selected event to the selected task, disable channel *n* by setting `SOC_ETM_CH_DISABLEn`. To configure a new event and task mapping, repeat Steps 2 to 4. If no configurations, channel *n* will remain disabled
6. The whole ETM module (i.e., all ETM channels) can be reset by writing 1 and then 0 to the `HP_SYS_CLKRST_REG_RST_EN_ETM` field

## 12.4 Register Summary

The addresses in this section are relative to Event Task Matrix base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                       | Description                | Address | Access    |
|--|----------------------------|---------|-----------|
| <b>Status register</b>                     |                            |         |           |
| <a href="#">SOC_ETM_CH_ENA_ADO_REG</a>     | Channel status register    | 0x0000  | R/WTC/WTS |
| <a href="#">SOC_ETM_CH_ENA_AD1_REG</a>     | Channel status register    | 0x000C  | R/WTC/WTS |
| <a href="#">SOC_ETM_EVT_ST0_REG</a>        | Event status register      | 0x01A8  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST1_REG</a>        | Event status register      | 0x01B0  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST2_REG</a>        | Event status register      | 0x01B8  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST3_REG</a>        | Event status register      | 0x01C0  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST4_REG</a>        | Event status register      | 0x01C8  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST5_REG</a>        | Event status register      | 0x01D0  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST6_REG</a>        | Event status register      | 0x01D8  | R/WTC/SS  |
| <a href="#">SOC_ETM_EVT_ST7_REG</a>        | Event status register      | 0x01E0  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST0_REG</a>       | Task status register       | 0x01E8  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST1_REG</a>       | Task status register       | 0x01F0  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST2_REG</a>       | Task status register       | 0x01F8  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST3_REG</a>       | Task status register       | 0x0200  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST4_REG</a>       | Task status register       | 0x0208  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST5_REG</a>       | Task status register       | 0x0210  | R/WTC/SS  |
| <a href="#">SOC_ETM_TASK_ST6_REG</a>       | Task status register       | 0x0218  | R/WTC/SS  |
| <b>Configuration Register</b>              |                            |         |           |
| <a href="#">SOC_ETM_CH_ENA_ADO_SET_REG</a> | Channel enable register    | 0x0004  | WT        |
| <a href="#">SOC_ETM_CH_ENA_ADO_CLR_REG</a> | Channel disable register   | 0x0008  | WT        |
| <a href="#">SOC_ETM_CH_ENA_AD1_SET_REG</a> | Channel enable register    | 0x0010  | WT        |
| <a href="#">SOC_ETM_CH_ENA_AD1_CLR_REG</a> | Channel disable register   | 0x0014  | WT        |
| <a href="#">SOC_ETM_CH0_EVT_ID_REG</a>     | Channel0 event ID register | 0x0018  | R/W       |
| <a href="#">SOC_ETM_CH0_TASK_ID_REG</a>    | Channel0 task ID register  | 0x001C  | R/W       |
| <a href="#">SOC_ETM_CH1_EVT_ID_REG</a>     | Channel1 event ID register | 0x0020  | R/W       |
| <a href="#">SOC_ETM_CH1_TASK_ID_REG</a>    | Channel1 task ID register  | 0x0024  | R/W       |
| <a href="#">SOC_ETM_CH2_EVT_ID_REG</a>     | Channel2 event ID register | 0x0028  | R/W       |
| <a href="#">SOC_ETM_CH2_TASK_ID_REG</a>    | Channel2 task ID register  | 0x002C  | R/W       |
| <a href="#">SOC_ETM_CH3_EVT_ID_REG</a>     | Channel3 event ID register | 0x0030  | R/W       |
| <a href="#">SOC_ETM_CH3_TASK_ID_REG</a>    | Channel3 task ID register  | 0x0034  | R/W       |
| <a href="#">SOC_ETM_CH4_EVT_ID_REG</a>     | Channel4 event ID register | 0x0038  | R/W       |
| <a href="#">SOC_ETM_CH4_TASK_ID_REG</a>    | Channel4 task ID register  | 0x003C  | R/W       |
| <a href="#">SOC_ETM_CH5_EVT_ID_REG</a>     | Channel5 event ID register | 0x0040  | R/W       |
| <a href="#">SOC_ETM_CH5_TASK_ID_REG</a>    | Channel5 task ID register  | 0x0044  | R/W       |
| <a href="#">SOC_ETM_CH6_EVT_ID_REG</a>     | Channel6 event ID register | 0x0048  | R/W       |
| <a href="#">SOC_ETM_CH6_TASK_ID_REG</a>    | Channel6 task ID register  | 0x004C  | R/W       |

| Name                                     | Description                 | Address | Access |
|--|-----------------------------|---------|--------|
| <a href="#">SOC_ETM_CH7_EVT_ID_REG</a>   | Channel7 event ID register  | 0x0050  | R/W    |
| <a href="#">SOC_ETM_CH7_TASK_ID_REG</a>  | Channel7 task ID register   | 0x0054  | R/W    |
| <a href="#">SOC_ETM_CH8_EVT_ID_REG</a>   | Channel8 event ID register  | 0x0058  | R/W    |
| <a href="#">SOC_ETM_CH8_TASK_ID_REG</a>  | Channel8 task ID register   | 0x005C  | R/W    |
| <a href="#">SOC_ETM_CH9_EVT_ID_REG</a>   | Channel9 event ID register  | 0x0060  | R/W    |
| <a href="#">SOC_ETM_CH9_TASK_ID_REG</a>  | Channel9 task ID register   | 0x0064  | R/W    |
| <a href="#">SOC_ETM_CH10_EVT_ID_REG</a>  | Channel10 event ID register | 0x0068  | R/W    |
| <a href="#">SOC_ETM_CH10_TASK_ID_REG</a> | Channel10 task ID register  | 0x006C  | R/W    |
| <a href="#">SOC_ETM_CH11_EVT_ID_REG</a>  | Channel11 event ID register | 0x0070  | R/W    |
| <a href="#">SOC_ETM_CH11_TASK_ID_REG</a> | Channel11 task ID register  | 0x0074  | R/W    |
| <a href="#">SOC_ETM_CH12_EVT_ID_REG</a>  | Channel12 event ID register | 0x0078  | R/W    |
| <a href="#">SOC_ETM_CH12_TASK_ID_REG</a> | Channel12 task ID register  | 0x007C  | R/W    |
| <a href="#">SOC_ETM_CH13_EVT_ID_REG</a>  | Channel13 event ID register | 0x0080  | R/W    |
| <a href="#">SOC_ETM_CH13_TASK_ID_REG</a> | Channel13 task ID register  | 0x0084  | R/W    |
| <a href="#">SOC_ETM_CH14_EVT_ID_REG</a>  | Channel14 event ID register | 0x0088  | R/W    |
| <a href="#">SOC_ETM_CH14_TASK_ID_REG</a> | Channel14 task ID register  | 0x008C  | R/W    |
| <a href="#">SOC_ETM_CH15_EVT_ID_REG</a>  | Channel15 event ID register | 0x0090  | R/W    |
| <a href="#">SOC_ETM_CH15_TASK_ID_REG</a> | Channel15 task ID register  | 0x0094  | R/W    |
| <a href="#">SOC_ETM_CH16_EVT_ID_REG</a>  | Channel16 event ID register | 0x0098  | R/W    |
| <a href="#">SOC_ETM_CH16_TASK_ID_REG</a> | Channel16 task ID register  | 0x009C  | R/W    |
| <a href="#">SOC_ETM_CH17_EVT_ID_REG</a>  | Channel17 event ID register | 0x00A0  | R/W    |
| <a href="#">SOC_ETM_CH17_TASK_ID_REG</a> | Channel17 task ID register  | 0x00A4  | R/W    |
| <a href="#">SOC_ETM_CH18_EVT_ID_REG</a>  | Channel18 event ID register | 0x00A8  | R/W    |
| <a href="#">SOC_ETM_CH18_TASK_ID_REG</a> | Channel18 task ID register  | 0x00AC  | R/W    |
| <a href="#">SOC_ETM_CH19_EVT_ID_REG</a>  | Channel19 event ID register | 0x00B0  | R/W    |
| <a href="#">SOC_ETM_CH19_TASK_ID_REG</a> | Channel19 task ID register  | 0x00B4  | R/W    |
| <a href="#">SOC_ETM_CH20_EVT_ID_REG</a>  | Channel20 event ID register | 0x00B8  | R/W    |
| <a href="#">SOC_ETM_CH20_TASK_ID_REG</a> | Channel20 task ID register  | 0x00BC  | R/W    |
| <a href="#">SOC_ETM_CH21_EVT_ID_REG</a>  | Channel21 event ID register | 0x00C0  | R/W    |
| <a href="#">SOC_ETM_CH21_TASK_ID_REG</a> | Channel21 task ID register  | 0x00C4  | R/W    |
| <a href="#">SOC_ETM_CH22_EVT_ID_REG</a>  | Channel22 event ID register | 0x00C8  | R/W    |
| <a href="#">SOC_ETM_CH22_TASK_ID_REG</a> | Channel22 task ID register  | 0x00CC  | R/W    |
| <a href="#">SOC_ETM_CH23_EVT_ID_REG</a>  | Channel23 event ID register | 0x00D0  | R/W    |
| <a href="#">SOC_ETM_CH23_TASK_ID_REG</a> | Channel23 task ID register  | 0x00D4  | R/W    |
| <a href="#">SOC_ETM_CH24_EVT_ID_REG</a>  | Channel24 event ID register | 0x00D8  | R/W    |
| <a href="#">SOC_ETM_CH24_TASK_ID_REG</a> | Channel24 task ID register  | 0x00DC  | R/W    |
| <a href="#">SOC_ETM_CH25_EVT_ID_REG</a>  | Channel25 event ID register | 0x00E0  | R/W    |
| <a href="#">SOC_ETM_CH25_TASK_ID_REG</a> | Channel25 task ID register  | 0x00E4  | R/W    |
| <a href="#">SOC_ETM_CH26_EVT_ID_REG</a>  | Channel26 event ID register | 0x00E8  | R/W    |
| <a href="#">SOC_ETM_CH26_TASK_ID_REG</a> | Channel26 task ID register  | 0x00EC  | R/W    |
| <a href="#">SOC_ETM_CH27_EVT_ID_REG</a>  | Channel27 event ID register | 0x00F0  | R/W    |
| <a href="#">SOC_ETM_CH27_TASK_ID_REG</a> | Channel27 task ID register  | 0x00F4  | R/W    |
| <a href="#">SOC_ETM_CH28_EVT_ID_REG</a>  | Channel28 event ID register | 0x00F8  | R/W    |

| Name                                     | Description                 | Address | Access |
|--|-----------------------------|---------|--------|
| <a href="#">SOC_ETM_CH28_TASK_ID_REG</a> | Channel28 task ID register  | 0x00FC  | R/W    |
| <a href="#">SOC_ETM_CH29_EVT_ID_REG</a>  | Channel29 event ID register | 0x0100  | R/W    |
| <a href="#">SOC_ETM_CH29_TASK_ID_REG</a> | Channel29 task ID register  | 0x0104  | R/W    |
| <a href="#">SOC_ETM_CH30_EVT_ID_REG</a>  | Channel30 event ID register | 0x0108  | R/W    |
| <a href="#">SOC_ETM_CH30_TASK_ID_REG</a> | Channel30 task ID register  | 0x010C  | R/W    |
| <a href="#">SOC_ETM_CH31_EVT_ID_REG</a>  | Channel31 event ID register | 0x0110  | R/W    |
| <a href="#">SOC_ETM_CH31_TASK_ID_REG</a> | Channel31 task ID register  | 0x0114  | R/W    |
| <a href="#">SOC_ETM_CH32_EVT_ID_REG</a>  | Channel32 event ID register | 0x0118  | R/W    |
| <a href="#">SOC_ETM_CH32_TASK_ID_REG</a> | Channel32 task ID register  | 0x011C  | R/W    |
| <a href="#">SOC_ETM_CH33_EVT_ID_REG</a>  | Channel33 event ID register | 0x0120  | R/W    |
| <a href="#">SOC_ETM_CH33_TASK_ID_REG</a> | Channel33 task ID register  | 0x0124  | R/W    |
| <a href="#">SOC_ETM_CH34_EVT_ID_REG</a>  | Channel34 event ID register | 0x0128  | R/W    |
| <a href="#">SOC_ETM_CH34_TASK_ID_REG</a> | Channel34 task ID register  | 0x012C  | R/W    |
| <a href="#">SOC_ETM_CH35_EVT_ID_REG</a>  | Channel35 event ID register | 0x0130  | R/W    |
| <a href="#">SOC_ETM_CH35_TASK_ID_REG</a> | Channel35 task ID register  | 0x0134  | R/W    |
| <a href="#">SOC_ETM_CH36_EVT_ID_REG</a>  | Channel36 event ID register | 0x0138  | R/W    |
| <a href="#">SOC_ETM_CH36_TASK_ID_REG</a> | Channel36 task ID register  | 0x013C  | R/W    |
| <a href="#">SOC_ETM_CH37_EVT_ID_REG</a>  | Channel37 event ID register | 0x0140  | R/W    |
| <a href="#">SOC_ETM_CH37_TASK_ID_REG</a> | Channel37 task ID register  | 0x0144  | R/W    |
| <a href="#">SOC_ETM_CH38_EVT_ID_REG</a>  | Channel38 event ID register | 0x0148  | R/W    |
| <a href="#">SOC_ETM_CH38_TASK_ID_REG</a> | Channel38 task ID register  | 0x014C  | R/W    |
| <a href="#">SOC_ETM_CH39_EVT_ID_REG</a>  | Channel39 event ID register | 0x0150  | R/W    |
| <a href="#">SOC_ETM_CH39_TASK_ID_REG</a> | Channel39 task ID register  | 0x0154  | R/W    |
| <a href="#">SOC_ETM_CH40_EVT_ID_REG</a>  | Channel40 event ID register | 0x0158  | R/W    |
| <a href="#">SOC_ETM_CH40_TASK_ID_REG</a> | Channel40 task ID register  | 0x015C  | R/W    |
| <a href="#">SOC_ETM_CH41_EVT_ID_REG</a>  | Channel41 event ID register | 0x0160  | R/W    |
| <a href="#">SOC_ETM_CH41_TASK_ID_REG</a> | Channel41 task ID register  | 0x0164  | R/W    |
| <a href="#">SOC_ETM_CH42_EVT_ID_REG</a>  | Channel42 event ID register | 0x0168  | R/W    |
| <a href="#">SOC_ETM_CH42_TASK_ID_REG</a> | Channel42 task ID register  | 0x016C  | R/W    |
| <a href="#">SOC_ETM_CH43_EVT_ID_REG</a>  | Channel43 event ID register | 0x0170  | R/W    |
| <a href="#">SOC_ETM_CH43_TASK_ID_REG</a> | Channel43 task ID register  | 0x0174  | R/W    |
| <a href="#">SOC_ETM_CH44_EVT_ID_REG</a>  | Channel44 event ID register | 0x0178  | R/W    |
| <a href="#">SOC_ETM_CH44_TASK_ID_REG</a> | Channel44 task ID register  | 0x017C  | R/W    |
| <a href="#">SOC_ETM_CH45_EVT_ID_REG</a>  | Channel45 event ID register | 0x0180  | R/W    |
| <a href="#">SOC_ETM_CH45_TASK_ID_REG</a> | Channel45 task ID register  | 0x0184  | R/W    |
| <a href="#">SOC_ETM_CH46_EVT_ID_REG</a>  | Channel46 event ID register | 0x0188  | R/W    |
| <a href="#">SOC_ETM_CH46_TASK_ID_REG</a> | Channel46 task ID register  | 0x018C  | R/W    |
| <a href="#">SOC_ETM_CH47_EVT_ID_REG</a>  | Channel47 event ID register | 0x0190  | R/W    |
| <a href="#">SOC_ETM_CH47_TASK_ID_REG</a> | Channel47 task ID register  | 0x0194  | R/W    |
| <a href="#">SOC_ETM_CH48_EVT_ID_REG</a>  | Channel48 event ID register | 0x0198  | R/W    |
| <a href="#">SOC_ETM_CH48_TASK_ID_REG</a> | Channel48 task ID register  | 0x019C  | R/W    |
| <a href="#">SOC_ETM_CH49_EVT_ID_REG</a>  | Channel49 event ID register | 0x01A0  | R/W    |
| <a href="#">SOC_ETM_CH49_TASK_ID_REG</a> | Channel49 task ID register  | 0x01A4  | R/W    |

| Name                                     | Description                 | Address | Access |
|--|-----------------------------|---------|--------|
| <a href="#">SOC_ETM_EVT_ST0_CLR_REG</a>  | Event status clear register | 0x01AC  | WT     |
| <a href="#">SOC_ETM_EVT_ST1_CLR_REG</a>  | Event status clear register | 0x01B4  | WT     |
| <a href="#">SOC_ETM_EVT_ST2_CLR_REG</a>  | Event status clear register | 0x01BC  | WT     |
| <a href="#">SOC_ETM_EVT_ST3_CLR_REG</a>  | Event status clear register | 0x01C4  | WT     |
| <a href="#">SOC_ETM_EVT_ST4_CLR_REG</a>  | Event status clear register | 0x01CC  | WT     |
| <a href="#">SOC_ETM_EVT_ST5_CLR_REG</a>  | Event status clear register | 0x01D4  | WT     |
| <a href="#">SOC_ETM_EVT_ST6_CLR_REG</a>  | Event status clear register | 0x01DC  | WT     |
| <a href="#">SOC_ETM_EVT_ST7_CLR_REG</a>  | Event status clear register | 0x01E4  | WT     |
| <a href="#">SOC_ETM_TASK_ST0_CLR_REG</a> | Task status clear register  | 0x01EC  | WT     |
| <a href="#">SOC_ETM_TASK_ST1_CLR_REG</a> | Task status clear register  | 0x01F4  | WT     |
| <a href="#">SOC_ETM_TASK_ST2_CLR_REG</a> | Task status clear register  | 0x01FC  | WT     |
| <a href="#">SOC_ETM_TASK_ST3_CLR_REG</a> | Task status clear register  | 0x0204  | WT     |
| <a href="#">SOC_ETM_TASK_ST4_CLR_REG</a> | Task status clear register  | 0x020C  | WT     |
| <a href="#">SOC_ETM_TASK_ST5_CLR_REG</a> | Task status clear register  | 0x0214  | WT     |
| <a href="#">SOC_ETM_TASK_ST6_CLR_REG</a> | Task status clear register  | 0x021C  | WT     |
| <a href="#">SOC_ETM_CLK_EN_REG</a>       | ETM clock enable register   | 0x0220  | R/W    |
| <b>Version Register</b>                  |                             |         |        |
| <a href="#">SOC_ETM_DATE_REG</a>         | Version control register    | 0x0224  | R/W    |

## 12.5 Registers

The addresses in this section are relative to Event Task Matrix base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 12.1. SOC\_ETM\_CH\_ENA\_ADO\_REG (0x0000)**

|                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| SOC_ETM_CH_ENABLED31 | SOC_ETM_CH_ENABLED30 | SOC_ETM_CH_ENABLED29 | SOC_ETM_CH_ENABLED28 | SOC_ETM_CH_ENABLED27 | SOC_ETM_CH_ENABLED26 | SOC_ETM_CH_ENABLED25 | SOC_ETM_CH_ENABLED24 | SOC_ETM_CH_ENABLED23 | SOC_ETM_CH_ENABLED22 | SOC_ETM_CH_ENABLED21 | SOC_ETM_CH_ENABLED20 | SOC_ETM_CH_ENABLED19 | SOC_ETM_CH_ENABLED18 | SOC_ETM_CH_ENABLED17 | SOC_ETM_CH_ENABLED16 | SOC_ETM_CH_ENABLED15 | SOC_ETM_CH_ENABLED14 | SOC_ETM_CH_ENABLED13 | SOC_ETM_CH_ENABLED12 | SOC_ETM_CH_ENABLED11 | SOC_ETM_CH_ENABLED10 | SOC_ETM_CH_ENABLED9 | SOC_ETM_CH_ENABLED8 | SOC_ETM_CH_ENABLED7 | SOC_ETM_CH_ENABLED6 | SOC_ETM_CH_ENABLED5 | SOC_ETM_CH_ENABLED4 | SOC_ETM_CH_ENABLED3 | SOC_ETM_CH_ENABLED2 | SOC_ETM_CH_ENABLED1 | SOC_ETM_CH_ENABLED0 |
| 31                   | 30                   | 29                   | 28                   | 27                   | 26                   | 25                   | 24                   | 23                   | 22                   | 21                   | 20                   | 19                   | 18                   | 17                   | 16                   | 15                   | 14                   | 13                   | 12                   | 11                   | 10                   | 9                   | 8                   | 7                   | 6                   | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |
| 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   |

Reset

**SOC\_ETM\_CH\_ENABLED $n$  ( $n$ : 0-31)** Represents the status of channel $n$ .

0: Disabled

1: Enabled

(R/WTC/SS)

**Register 12.2. SOC\_ETM\_CH\_ENA\_AD1\_REG (0x000C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  | 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 |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  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 |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  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 |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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 |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**SOC\_ETM\_CH\_ENABLED $n$  ( $n$ : 32-49)** Represents the status of channel $n$ .

0: Disabled

1: Enabled

(R/WTC/SS)

**Register 12.3. SOC\_ETM\_EVT\_STO\_REG (0x01A8)**

| Soc ETM LEDC_EVT_DUTY_CHNG_END_CH3_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Soc ETM LEDC_EVT_DUTY_CHNG_END_CH2_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM LEDC_EVT_DUTY_CHNG_END_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_ZERO_DET_NEG1_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_ZERO_DET_POS1_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_ZERO_DET_NEG0_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH7_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH6_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH5_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH4_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH3_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH2_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH1_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH0_ANY_EDGE_ST      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH7_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH6_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH5_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH4_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH3_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH2_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH1_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH0_FALL_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH7_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH6_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH5_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH4_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH3_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH2_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH1_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM_GPIO_EVT_CH0_RISE_EDGE_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_GPIO\_EVT\_CHO\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CHO\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH1\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH1\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH2\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH2\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH3\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH3\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH4\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH4\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH5\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH5\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...

**Register 12.3. SOC\_ETM\_EVT\_STO\_REG (0x01A8)****Continued from the previous page...****SOC\_ETM\_GPIO\_EVT\_CH6\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH6\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH7\_RISE\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH7\_RISE\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CHO\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CHO\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH1\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH1\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH2\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH2\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH3\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH3\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH4\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH4\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH5\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH5\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**Continued on the next page...**



**Register 12.3. SOC\_ETM\_EVT\_STO\_REG (0x01A8)**

Continued from the previous page...

**SOC\_ETM\_GPIO\_EVT\_CH6\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH6\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH7\_FALL\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH7\_FALL\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CHO\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CHO\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH1\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH1\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH2\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH2\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH3\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH3\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH4\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH4\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...

**Register 12.3. SOC\_ETM\_EVT\_STO\_REG (0x01A8)**

Continued from the previous page...

**SOC\_ETM\_GPIO\_EVT\_CH5\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH5\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH6\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH6\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_CH7\_ANY\_EDGE\_ST** Represents the status of GPIO\_EVT\_CH7\_ANY\_EDGE.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_ZERO\_DET\_POS0\_ST** Represents the status of GPIO\_EVT\_ZERO\_DET\_POS0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_ZERO\_DET\_NEG0\_ST** Represents the status of GPIO\_EVT\_ZERO\_DET\_NEG0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_ZERO\_DET\_POS1\_ST** Represents the status of GPIO\_EVT\_ZERO\_DET\_POS1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GPIO\_EVT\_ZERO\_DET\_NEG1\_ST** Represents the status of GPIO\_EVT\_ZERO\_DET\_NEG1.

0: Not received

1: Received

(R/WTC/SS)

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**Register 12.3. SOC\_ETM\_EVT\_STO\_REG (0x01A8)**

Continued from the previous page...

|  |            |     |        |    |
|--|------------|-----|--------|----|
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH0_ST</b> | Represents | the | status | of |
| LEDC_EVT_DUTY_CHNG_END_CH0.                  |            |     |        |    |
| 0: Not received                              |            |     |        |    |
| 1: Received                                  |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH1_ST</b> | Represents | the | status | of |
| LEDC_EVT_DUTY_CHNG_END_CH1.                  |            |     |        |    |
| 0: Not received                              |            |     |        |    |
| 1: Received                                  |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH2_ST</b> | Represents | the | status | of |
| LEDC_EVT_DUTY_CHNG_END_CH2.                  |            |     |        |    |
| 0: Not received                              |            |     |        |    |
| 1: Received                                  |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH3_ST</b> | Represents | the | status | of |
| LEDC_EVT_DUTY_CHNG_END_CH3.                  |            |     |        |    |
| 0: Not received                              |            |     |        |    |
| 1: Received                                  |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |

## Register 12.4. SOC\_ETM\_EVT\_ST1\_REG (0x01B0)

|                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |                              |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   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|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|------------------------------|-------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|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| SOC_ETM_MCPWMO_EVT_TIMER1_TEZ_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWMO_EVT_TIMER2_ST |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWMO_EVT_TIMER1_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWMO_EVT_TIMER2_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_SYSTIMER_EVT_CNT_CMP2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_SYSTIMER_EVT_CNT_CMP1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_TG1_EVT_CNT_CMP_TIMER1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_TG0_EVT_CNT_CMP_TIMER0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_TG0_EVT_CNT_CMP_TIMER1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIMER3_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIMER2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIMER1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIMER0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIME_OVF_TIMER3_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIME_OVF_TIMER2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_TIME_OVF_TIMER1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH7_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH6_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH5_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH4_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH3_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_CH1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_CH0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH7_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH6_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH5_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH4_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0                            | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH4\_ST** Represents the status of LEDC\_EVT\_DUTY\_CHNG\_END\_CH4.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH5\_ST** Represents the status of LEDC\_EVT\_DUTY\_CHNG\_END\_CH5.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH6\_ST** Represents the status of LEDC\_EVT\_DUTY\_CHNG\_END\_CH6.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH7\_ST** Represents the status of LEDC\_EVT\_DUTY\_CHNG\_END\_CH7.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CHO\_ST** Represents the status of LEDC\_EVT\_OVF\_CNT\_PLS\_CHO.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH1\_ST** Represents the status of LEDC\_EVT\_OVF\_CNT\_PLS\_CH1.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

## Register 12.4. SOC\_ETM\_EVT\_ST1\_REG (0x01B0)

Continued from the previous page...

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH2\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH2.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH3\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH3.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH4\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH4.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH5\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH5.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH6\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH6.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CH7\_ST** Represents the status of  
LEDC\_EVT\_OVF\_CNT\_PLS\_CH7.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIME\_OVF\_TIMER0\_ST** Represents the status of  
LEDC\_EVT\_TIME\_OVF\_TIMER0.  
0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIME\_OVF\_TIMER1\_ST** Represents the status of  
LEDC\_EVT\_TIME\_OVF\_TIMER1.  
0: Not received  
1: Received  
(R/WTC/SS)

**Register 12.4. SOC\_ETM\_EVT\_ST1\_REG (0x01B0)****Continued from the previous page...**

**SOC\_ETM\_LEDC\_EVT\_TIME\_OVF\_TIMER2\_ST** Represents the status of  
LEDC\_EVT\_TIME\_OVF\_TIMER2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIME\_OVF\_TIMER3\_ST** Represents the status of  
LEDC\_EVT\_TIME\_OVF\_TIMER3.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIMER0\_CMP\_ST** Represents the status of LEDC\_EVT\_TIMER0\_CMP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIMER1\_CMP\_ST** Represents the status of LEDC\_EVT\_TIMER1\_CMP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIMER2\_CMP\_ST** Represents the status of LEDC\_EVT\_TIMER2\_CMP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_LEDC\_EVT\_TIMER3\_CMP\_ST** Represents the status of LEDC\_EVT\_TIMER3\_CMP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_TGO\_EVT\_CNT\_CMP\_TIMER0\_ST** Represents the status of  
TGO\_EVT\_CNT\_CMP\_TIMER0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_TGO\_EVT\_CNT\_CMP\_TIMER1\_ST** Represents the status of TGO\_EVT\_CNT\_CMP\_TIMER1.

0: Not received

1: Received

(R/WTC/SS)

**Continued on the next page...**

**Register 12.4. SOC\_ETM\_EVT\_ST1\_REG (0x01B0)**

Continued from the previous page...

**SOC\_ETM\_TG1\_EVT\_CNT\_CMP\_TIMER0\_ST** Represents the status of TG1\_EVT\_CNT\_CMP\_TIMER0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_TG1\_EVT\_CNT\_CMP\_TIMER1\_ST** Represents the status of TG1\_EVT\_CNT\_CMP\_TIMER1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_SYSTIMER\_EVT\_CNT\_CMPO\_ST** Represents the status of SYSTIMER\_EVT\_CNT\_CMPO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_SYSTIMER\_EVT\_CNT\_CMP1\_ST** Represents the status of SYSTIMER\_EVT\_CNT\_CMP1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_SYSTIMER\_EVT\_CNT\_CMP2\_ST** Represents the status of SYSTIMER\_EVT\_CNT\_CMP2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TIMER0\_STOP\_ST** Represents the status of MCPWMO\_EVT\_TIMER0\_STOP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TIMER1\_STOP\_ST** Represents the status of MCPWMO\_EVT\_TIMER1\_STOP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TIMER2\_STOP\_ST** Represents the status of MCPWMO\_EVT\_TIMER2\_STOP.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...

**Register 12.4. SOC\_ETM\_EVT\_ST1\_REG (0x01B0)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_TIMER0\_TEZ\_ST** Represents the status of  
MCPWMO\_EVT\_TIMER0\_TEZ.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TIMER1\_TEZ\_ST** Represents the status of MCPWMO\_EVT\_TIMER1\_TEZ.

0: Not received

1: Received

(R/WTC/SS)



**Register 12.5. SOC\_ETM\_EVT\_ST2\_REG (0x01B8)**

|                                   |                                   |                                |                                |                                |                                |                                |                                |                            |                            |                               |                               |                               |                               |                               |                               |                              |                              |                              |                          |                          |                          |                               |                               |                               |                               |                               |                               |                                  |                                  |                                  |                                  |
|-----------------------------------|-----------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|----------------------------|----------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|------------------------------|------------------------------|------------------------------|--------------------------|--------------------------|--------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| SOC_ETM_MCPWM1_EVT_TIMER0_STOP_ST | SOC_ETM_MCPWM0_EVT_TIMER0_STOP_ST | SOC_ETM_MCPWM0_EVT_OP2_TEE2_ST | SOC_ETM_MCPWM0_EVT_OP1_TEE2_ST | SOC_ETM_MCPWM0_EVT_OPO_TEE2_ST | SOC_ETM_MCPWM0_EVT_OP2_TEE2_ST | SOC_ETM_MCPWM0_EVT_OP1_TEE1_ST | SOC_ETM_MCPWM0_EVT_OPO_TEE1_ST | SOC_ETM_MCPWM0_EVT_CAP2_ST | SOC_ETM_MCPWM0_EVT_CAP1_ST | SOC_ETM_MCPWM0_EVT_TZ2_OST_ST | SOC_ETM_MCPWM0_EVT_TZ1_OST_ST | SOC_ETM_MCPWM0_EVT_TZ0_OST_ST | SOC_ETM_MCPWM0_EVT_TZ2_CBC_ST | SOC_ETM_MCPWM0_EVT_TZ1_CBC_ST | SOC_ETM_MCPWM0_EVT_TZ0_CBC_ST | SOC_ETM_MCPWM0_EVT_F2_CLR_ST | SOC_ETM_MCPWM0_EVT_F1_CLR_ST | SOC_ETM_MCPWM0_EVT_F0_CLR_ST | SOC_ETM_MCPWM0_EVT_F2_ST | SOC_ETM_MCPWM0_EVT_F1_ST | SOC_ETM_MCPWM0_EVT_F0_ST | SOC_ETM_MCPWM0_EVT_OP2_TEB_ST | SOC_ETM_MCPWM0_EVT_OP1_TEB_ST | SOC_ETM_MCPWM0_EVT_OPO_TEB_ST | SOC_ETM_MCPWM0_EVT_OP2_TEA_ST | SOC_ETM_MCPWM0_EVT_OP1_TEA_ST | SOC_ETM_MCPWM0_EVT_OPO_TEA_ST | SOC_ETM_MCPWM0_EVT_TIMER2_TEP_ST | SOC_ETM_MCPWM0_EVT_TIMER1_TEP_ST | SOC_ETM_MCPWM0_EVT_TIMER0_TEP_ST | SOC_ETM_MCPWM0_EVT_TIMER2_TEZ_ST |
| 31                                | 30                                | 29                             | 28                             | 27                             | 26                             | 25                             | 24                             | 23                         | 22                         | 21                            | 20                            | 19                            | 18                            | 17                            | 16                            | 15                           | 14                           | 13                           | 12                       | 11                       | 10                       | 9                             | 8                             | 7                             | 6                             | 5                             | 4                             | 3                                | 2                                | 1                                | 0                                |
| 0                                 | 0                                 | 0                              | 0                              | 0                              | 0                              | 0                              | 0                              | 0                          | 0                          | 0                             | 0                             | 0                             | 0                             | 0                             | 0                             | 0                            | 0                            | 0                            | 0                        | 0                        | 0                        | 0                             | 0                             | 0                             | 0                             | 0                             | 0                             | 0                                | 0                                | 0                                | 0                                |

Reset

**SOC\_ETM\_MCPWM0\_EVT\_TIMER2\_TEZ\_ST** Represents the status of MCPWM0\_EVT\_TIMER2\_TEZ.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER0\_TEP\_ST** Represents the status of MCPWM0\_EVT\_TIMER0\_TEP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER1\_TEP\_ST** Represents the status of MCPWM0\_EVT\_TIMER1\_TEP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER2\_TEP\_ST** Represents the status of MCPWM0\_EVT\_TIMER2\_TEP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_EVT\_OPO\_TEA\_ST** Represents the status of MCPWM0\_EVT\_OPO\_TEA.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_EVT\_OP1\_TEA\_ST** Represents the status of MCPWM0\_EVT\_OP1\_TEA.

0: Not received

1: Received

(R/WTC/SS)

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**Register 12.5. SOC\_ETM\_EVT\_ST2\_REG (0x01B8)**

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**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEA\_ST** Represents the status of MCPWMO\_EVT\_OP2\_TEA.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEB\_ST** Represents the status of MCPWMO\_EVT\_OPO\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEB\_ST** Represents the status of MCPWMO\_EVT\_OP1\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEB\_ST** Represents the status of MCPWMO\_EVT\_OP2\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_F0\_ST** Represents the status of MCPWMO\_EVT\_F0.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_F1\_ST** Represents the status of MCPWMO\_EVT\_F1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_F2\_ST** Represents the status of MCPWMO\_EVT\_F2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_F0\_CLR\_ST** Represents the status of MCPWMO\_EVT\_F0\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_F1\_CLR\_ST** Represents the status of MCPWMO\_EVT\_F1\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

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**Register 12.5. SOC\_ETM\_EVT\_ST2\_REG (0x01B8)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_F2\_CLR\_ST** Represents the status of MCPWMO\_EVT\_F2\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ0\_CBC\_ST** Represents the status of MCPWMO\_EVT\_TZ0\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ1\_CBC\_ST** Represents the status of MCPWMO\_EVT\_TZ1\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ2\_CBC\_ST** Represents the status of MCPWMO\_EVT\_TZ2\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ0\_OST\_ST** Represents the status of MCPWMO\_EVT\_TZ0\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ1\_OST\_ST** Represents the status of MCPWMO\_EVT\_TZ1\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_TZ2\_OST\_ST** Represents the status of MCPWMO\_EVT\_TZ2\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_CAPO\_ST** Represents the status of MCPWMO\_EVT\_CAPO.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_CAP1\_ST** Represents the status of MCPWMO\_EVT\_CAP1.

0: Not received  
1: Received  
(R/WTC/SS)

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**Register 12.5. SOC\_ETM\_EVT\_ST2\_REG (0x01B8)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_CAP2\_ST** Represents the status of MCPWMO\_EVT\_CAP2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEE1\_ST** Represents the status of MCPWMO\_EVT\_OPO\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEE1\_ST** Represents the status of MCPWMO\_EVT\_OP1\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEE1\_ST** Represents the status of MCPWMO\_EVT\_OP2\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEE2\_ST** Represents the status of MCPWMO\_EVT\_OPO\_TEE2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEE2\_ST** Represents the status of MCPWMO\_EVT\_OP1\_TEE2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEE2\_ST** Represents the status of MCPWMO\_EVT\_OP2\_TEE2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_STOP\_ST** Represents the status of MCPWM1\_EVT\_TIMER0\_STOP.

0: Not received  
1: Received  
(R/WTC/SS)

**Register 12.6. SOC\_ETM\_EVT\_ST3\_REG (0x01C0)**

|                                |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOC_ETM_MCPWM1_EVT_OP2_TEE1_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP1_TEE1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OPO_TEE1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_CAP2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_CAP1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_CAPO_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ2_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ1_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ0_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ2_CBC_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ1_CBC_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TZ0_CBC_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F2_CLR_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F1_CLR_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F0_CLR_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_F0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP2_TEB_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP1_TEB_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OPO_TEB_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP2_TEA_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP1_TEA_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OPO_TEA_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER2_TEP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER1_TEP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER0_TEP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER2_TEZ_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER1_TEZ_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER0_TEZ_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER2_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER1_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_TIMER0_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                             | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                              | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                        | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_STOP\_ST** Represents the status of  
MCPWM1\_EVT\_TIMER1\_STOP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_STOP\_ST** Represents the status of  
MCPWM1\_EVT\_TIMER2\_STOP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_TEZ\_ST** Represents the status of MCPWM1\_EVT\_TIMER0\_TEZ.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_TEZ\_ST** Represents the status of MCPWM1\_EVT\_TIMER1\_TEZ.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_TEZ\_ST** Represents the status of MCPWM1\_EVT\_TIMER2\_TEZ.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_TEP\_ST** Represents the status of MCPWM1\_EVT\_TIMER0\_TEP.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...

**Register 12.6. SOC\_ETM\_EVT\_ST3\_REG (0x01C0)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_TEP\_ST** Represents the status of MCPWM1\_EVT\_TIMER1\_TEP.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_TEP\_ST** Represents the status of MCPWM1\_EVT\_TIMER2\_TEP.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEA\_ST** Represents the status of MCPWM1\_EVT\_OPO\_TEA.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEA\_ST** Represents the status of MCPWM1\_EVT\_OP1\_TEA.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEA\_ST** Represents the status of MCPWM1\_EVT\_OP2\_TEA.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEB\_ST** Represents the status of MCPWM1\_EVT\_OPO\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEB\_ST** Represents the status of MCPWM1\_EVT\_OP1\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEB\_ST** Represents the status of MCPWM1\_EVT\_OP2\_TEB.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_FO\_ST** Represents the status of MCPWM1\_EVT\_FO.

0: Not received  
1: Received  
(R/WTC/SS)

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**Register 12.6. SOC\_ETM\_EVT\_ST3\_REG (0x01C0)**

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**SOC\_ETM\_MCPWM1\_EVT\_F1\_ST** Represents the status of MCPWM1\_EVT\_F1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_F2\_ST** Represents the status of MCPWM1\_EVT\_F2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_F0\_CLR\_ST** Represents the status of MCPWM1\_EVT\_F0\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_F1\_CLR\_ST** Represents the status of MCPWM1\_EVT\_F1\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_F2\_CLR\_ST** Represents the status of MCPWM1\_EVT\_F2\_CLR.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TZO\_CBC\_ST** Represents the status of MCPWM1\_EVT\_TZO\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TZ1\_CBC\_ST** Represents the status of MCPWM1\_EVT\_TZ1\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TZ2\_CBC\_ST** Represents the status of MCPWM1\_EVT\_TZ2\_CBC.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TZO\_OST\_ST** Represents the status of MCPWM1\_EVT\_TZO\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

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**Register 12.6. SOC\_ETM\_EVT\_ST3\_REG (0x01C0)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_EVT\_TZ1\_OST\_ST** Represents the status of MCPWM1\_EVT\_TZ1\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_TZ2\_OST\_ST** Represents the status of MCPWM1\_EVT\_TZ2\_OST.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_CAPO\_ST** Represents the status of MCPWM1\_EVT\_CAPO.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_CAP1\_ST** Represents the status of MCPWM1\_EVT\_CAP1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_CAP2\_ST** Represents the status of MCPWM1\_EVT\_CAP2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEE1\_ST** Represents the status of MCPWM1\_EVT\_OPO\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEE1\_ST** Represents the status of MCPWM1\_EVT\_OP1\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEE1\_ST** Represents the status of MCPWM1\_EVT\_OP2\_TEE1.

0: Not received  
1: Received  
(R/WTC/SS)



Register 12.7. SOC\_ETM\_EVT\_ST4\_REG (0x01C8)

|                                  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           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  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   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|----------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOC_ETM_I2S2_EVT_X_WORDS_SENT_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_X_WORDS_RECEIVED_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_TX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_RX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_X_WORDS_SENT_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_X_WORDS_RECEIVED_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_TX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_RX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_X_WORDS_SENT_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_TX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_RX_DONE_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_TSPNSR_EVT_OVER_LIMIT_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR3_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE3_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_STARTED0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_STOPPED0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_RESULT_DONE0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_BELOW_THRESH0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_BELOW_THRESH1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_ABOVE_THRESH0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_ABOVE_THRESH1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_CONV_CMPLT0_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP2_TEE2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP1_TEE2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OPO_TEE2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                               | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                                | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEE2\_ST** Represents the status of MCPWM1\_EVT\_OPO\_TEE2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEE2\_ST** Represents the status of MCPWM1\_EVT\_OP1\_TEE2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEE2\_ST** Represents the status of MCPWM1\_EVT\_OP2\_TEE2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_CONV\_CMPLT0\_ST** Represents the status of ADC\_EVT\_CONV\_CMPLT0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_EQ\_ABOVE\_THRESH0\_ST** Represents the status of ADC\_EVT\_EQ\_ABOVE\_THRESH0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_EQ\_ABOVE\_THRESH1\_ST** Represents the status of ADC\_EVT\_EQ\_ABOVE\_THRESH1.

0: Not received

1: Received

(R/WTC/SS)

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**Register 12.7. SOC\_ETM\_EVT\_ST4\_REG (0x01C8)**

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**SOC\_ETM\_ADC\_EVT\_EQ\_BELOW\_THRESH0\_ST** Represents the status of ADC\_EVT\_EQ\_BELOW\_THRESH0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_EQ\_BELOW\_THRESH1\_ST** Represents the status of ADC\_EVT\_EQ\_BELOW\_THRESH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_RESULT\_DONE0\_ST** Represents the status of ADC\_EVT\_RESULT\_DONE0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_STOPPED0\_ST** Represents the status of ADC\_EVT\_STOPPED0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_ADC\_EVT\_STARTED0\_ST** Represents the status of ADC\_EVT\_STARTED0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_DONE0\_ST** Represents the status of REGDMA\_EVT\_DONE0.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_DONE1\_ST** Represents the status of REGDMA\_EVT\_DONE1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_DONE2\_ST** Represents the status of REGDMA\_EVT\_DONE2.

0: Not received

1: Received

(R/WTC/SS)

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**Register 12.7. SOC\_ETM\_EVT\_ST4\_REG (0x01C8)**

Continued from the previous page...

**SOC\_ETM\_REGDMA\_EVT\_DONE3\_ST** Represents the status of REGDMA\_EVT\_DONE3.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_ERRO\_ST** Represents the status of REGDMA\_EVT\_ERRO.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_ERR1\_ST** Represents the status of REGDMA\_EVT\_ERR1.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_ERR2\_ST** Represents the status of REGDMA\_EVT\_ERR2.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_REGDMA\_EVT\_ERR3\_ST** Represents the status of REGDMA\_EVT\_ERR3.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_TMPSNSR\_EVT\_OVER\_LIMIT\_ST** Represents the status of TMP-SNSR\_EVT\_OVER\_LIMIT.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2SO\_EVT\_RX\_DONE\_ST** Represents the status of I2SO\_EVT\_RX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2SO\_EVT\_TX\_DONE\_ST** Represents the status of I2SO\_EVT\_TX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2SO\_EVT\_X\_WORDS\_RECEIVED\_ST** Represents the status of I2SO\_EVT\_X\_WORDS\_RECEIVED.

0: Not received  
1: Received  
(R/WTC/SS)

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**Register 12.7. SOC\_ETM\_EVT\_ST4\_REG (0x01C8)**

Continued from the previous page...

**SOC\_ETM\_I2SO\_EVT\_X\_WORDS\_SENT\_ST** Represents the status of I2SO\_EVT\_X\_WORDS\_SENT.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S1\_EVT\_RX\_DONE\_ST** Represents the status of I2S1\_EVT\_RX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S1\_EVT\_TX\_DONE\_ST** Represents the status of I2S1\_EVT\_TX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S1\_EVT\_X\_WORDS\_RECEIVED\_ST** Represents the status of I2S1\_EVT\_X\_WORDS\_RECEIVED.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S1\_EVT\_X\_WORDS\_SENT\_ST** Represents the status of I2S1\_EVT\_X\_WORDS\_SENT.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S2\_EVT\_RX\_DONE\_ST** Represents the status of I2S2\_EVT\_RX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S2\_EVT\_TX\_DONE\_ST** Represents the status of I2S2\_EVT\_TX\_DONE.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S2\_EVT\_X\_WORDS\_RECEIVED\_ST** Represents the status of I2S2\_EVT\_X\_WORDS\_RECEIVED.

0: Not received  
1: Received  
(R/WTC/SS)

**SOC\_ETM\_I2S2\_EVT\_X\_WORDS\_SENT\_ST** Represents the status of I2S2\_EVT\_X\_WORDS\_SENT.

0: Not received  
1: Received  
(R/WTC/SS)

**Register 12.8. SOC\_ETM\_EVT\_ST5\_REG (0x01D0)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH1_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH0_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH2_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH0_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_TOTAL_EOF_CH2_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_TOTAL_EOF_CH1_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH2_ST        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH1_ST        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH0_ST        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_DONE_CH2_ST       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_OUT_DONE_CH1_ST       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_FIFO_FULL_CH2_ST   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_FIFO_FULL_CH1_ST   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CH2_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CH1_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH2_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH1_ST     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_GDMA_AHB_EVT_IN_DONE_CH2_ST        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_RTC_EVT_CMP_ST                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ULP_EVT_OVF_ST                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ULP_EVT_TICK_ST                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ULP_EVT_START_INTR_ST              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ULP_EVT_HALT_ST                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ULP_EVT_ERR_INTR_ST                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 31    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

Reset

**SOC\_ETM\_ULP\_EVT\_ERR\_INTR\_ST** Represents the status of ULP\_EVT\_ERR\_INTR.

- 0: Not received
- 1: Received
- (R/WTC/SS)

**SOC\_ETM\_ULP\_EVT\_HALT\_ST** Represents the status of ULP\_EVT\_HALT.

- 0: Not received
- 1: Received
- (R/WTC/SS)

**SOC\_ETM\_ULP\_EVT\_START\_INTR\_ST** Represents the status of ULP\_EVT\_START\_INTR.

- 0: Not received
- 1: Received
- (R/WTC/SS)

**SOC\_ETM\_RTC\_EVT\_TICK\_ST** Represents the status of RTC\_EVT\_TICK.

- 0: Not received
- 1: Received
- (R/WTC/SS)

**SOC\_ETM\_RTC\_EVT\_OVF\_ST** Represents the status of RTC\_EVT\_OVF.

- 0: Not received
- 1: Received
- (R/WTC/SS)

**SOC\_ETM\_RTC\_EVT\_CMP\_ST** Represents the status of RTC\_EVT\_CMP.

- 0: Not received
- 1: Received
- (R/WTC/SS)

Continued on the next page...

**Register 12.8. SOC\_ETM\_EVT\_ST5\_REG (0x01D0)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_DONE\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_DONE\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_DONE\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_DONE\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_DONE\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_DONE\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_SUC\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**Register 12.8. SOC\_ETM\_EVT\_ST5\_REG (0x01D0)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_DONE\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_DONE\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_DONE\_CH2.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...

**Register 12.8. SOC\_ETM\_EVT\_ST5\_REG (0x01D0)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_EOF\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH1\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH2\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CHO\_ST** Represents the status of  
GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CHO.

0: Not received

1: Received

(R/WTC/SS)

Continued on the next page...



**Register 12.8. SOC\_ETM\_EVT\_ST5\_REG (0x01D0)**

Continued from the previous page...

|   |            |     |        |    |
|---|------------|-----|--------|----|
| <b>SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH1_ST</b> | Represents | the | status | of |
| GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH1.                  |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH2_ST</b> | Represents | the | status | of |
| GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH2.                  |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CHO_ST</b>  | Represents | the | status | of |
| GDMA_AHB_EVT_OUT_FIFO_FULL_CHO.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH1_ST</b>  | Represents | the | status | of |
| GDMA_AHB_EVT_OUT_FIFO_FULL_CH1.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |

|                                     |                                  |                                  |                                 |   |  |   |  |  |  |   |   |   |                                     |                                     |                                     |                                     |                                     |                                      |                                      |  |  |  |   |   |   |  |  |  |                                     |   |   |
|-------------------------------------|----------------------------------|----------------------------------|---------------------------------|---|--|---|--|--|--|---|---|---|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--------------------------------------|--------------------------------------|--|--|--|---|---|---|--|--|--|-------------------------------------|---|---|
| 31                                  | 30                               | 29                               | 28                              | 27  | 26   | 25  | 24   | 23   | 22   | 21  | 20  | 19  | 18                                  | 17                                  | 16                                  | 15                                  | 14                                  | 13                                   | 12                                   | 11                                       | 10                                       | 9  | 8   | 7   | 6   | 5                                      | 4                                      | 3                                      | 2                                   | 1   | 0 |
| 0                                   | 0                                | 0                                | 0                               | 0   | 0  | 0   | 0  | 0  | 0  | 0   | 0   | 0   | 0                                   | 0                                   | 0                                   | 0                                   | 0                                   | 0                                    | 0                                    | 0  | 0  | 0  | 0   | 0   | 0   | 0                                      | 0                                      | 0                                      | 0                                   | 0   | 0 |
| SOC_ETM_DMA2D_EVT_IN_SUC_EOF_CH0_ST | SOC_ETM_DMA2D_EVT_IN_DONE_CH1_ST | SOC_ETM_DMA2D_EVT_IN_DONE_CH0_ST | SOC_ETM_PMU_EVT_SLEEP_WEEKUP_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_FULL_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_FULL_CH1_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH1_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH0_ST | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH1_ST | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH0_ST | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH1_ST | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH0_ST | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH1_ST | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH0_ST | SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH2_ST | SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH1_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH0_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH2_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH1_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_EMPTY_CH0_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_EMPTY_CH2_ST | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_EMPTY_CH1_ST | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH0_ST | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH2_ST | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH1_ST | SOC_ETM_GDMA_AXI_EVT_IN_DONE_CH0_ST | SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH2_ST |   |

0: Not received  
1: Received  
(R/WTC/SS)

0: Not received  
1: Received  
(R/WTC/SS)

0: Not received  
1: Received  
(R/WTC/SS)

0: Not received  
1: Received  
(R/WTC/SS)

0: Not received  
1: Received  
(R/WTC/SS)

Espressif Systems

**Register 12.9. SOC\_ETM\_EVT\_ST6\_REG (0x01D8)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH1\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH2\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CHO\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH1\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH2\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CHO\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH1\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH2\_ST** Represents the status of  
GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**Register 12.9. SOC\_ETM\_EVT\_ST6\_REG (0x01D8)**

Continued from the previous page...

|  |            |     |        |    |
|--|------------|-----|--------|----|
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CHO_ST</b>      | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_DONE_CHO.                       |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH1_ST</b>      | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_DONE_CH1.                       |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH2_ST</b>      | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_DONE_CH2.                       |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CHO_ST</b>       | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_EOF_CHO.                        |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH1_ST</b>       | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_EOF_CH1.                        |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH2_ST</b>       | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_EOF_CH2.                        |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CHO_ST</b> | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_TOTAL_EOF_CHO.                  |            |     |        |    |
| 0: Not received                                  |            |     |        |    |
| 1: Received                                      |            |     |        |    |
| (R/WTC/SS)                                       |            |     |        |    |

Continued on the next page...

**Register 12.9. SOC\_ETM\_EVT\_ST6\_REG (0x01D8)**

Continued from the previous page...

|   |            |     |        |    |
|---|------------|-----|--------|----|
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH1_ST</b>  | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_TOTAL_EOF_CH1.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH2_ST</b>  | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_TOTAL_EOF_CH2.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH0_ST</b> | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH0.                  |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH1_ST</b> | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH1.                  |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2_ST</b> | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2.                  |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_FULL_CH0_ST</b>  | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_FIFO_FULL_CH0.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_FULL_CH1_ST</b>  | Represents | the | status | of |
| GDMA_AXI_EVT_OUT_FIFO_FULL_CH1.                   |            |     |        |    |
| 0: Not received                                   |            |     |        |    |
| 1: Received                                       |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |

Continued on the next page...

**Register 12.9. SOC\_ETM\_EVT\_ST6\_REG (0x01D8)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH2\_ST** Represents the status of GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_PMU\_EVT\_SLEEP\_WEEKUP\_ST** Represents the status of PMU\_EVT\_SLEEP\_WEEKUP.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_IN\_DONE\_CHO\_ST** Represents the status of DMA2D\_EVT\_IN\_DONE\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_IN\_DONE\_CH1\_ST** Represents the status of DMA2D\_EVT\_IN\_DONE\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_IN\_SUC\_EOF\_CHO\_ST** Represents the status of DMA2D\_EVT\_IN\_SUC\_EOF\_CHO.

0: Not received

1: Received

(R/WTC/SS)

Register 12.10. SOC\_ETM\_EVT\_ST7\_REG (0x01E0)

|            |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |       |   |   |   |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|---|---|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH2_ST<br>SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH1_ST<br>SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH0_ST<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH2_ST<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH1_ST<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH0_ST<br>SOC_ETM_DMA2D_EVT_OUT_DONE_CH2_ST<br>SOC_ETM_DMA2D_EVT_OUT_DONE_CH1_ST<br>SOC_ETM_DMA2D_EVT_IN_SUC_EOF_CH1_ST |   |       |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   | 10 |   |   |   |   |   |   |   |   |   | 9 | 8   | 7 | 6     | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | Reset |   |   |   |   |   |   |  |

**SOC\_ETM\_DMA2D\_EVT\_IN\_SUC\_EOF\_CH1\_ST** Represents the status of DMA2D\_EVT\_IN\_SUC\_EOF\_CH1.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH0\_ST** Represents the status of DMA2D\_EVT\_OUT\_DONE\_CH0.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH1\_ST** Represents the status of DMA2D\_EVT\_OUT\_DONE\_CH1.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH2\_ST** Represents the status of DMA2D\_EVT\_OUT\_DONE\_CH2.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH0\_ST** Represents the status of DMA2D\_EVT\_OUT\_EOF\_CH0.  
 0: Not received  
 1: Received  
 (R/WTC/SS)

Continued on the next page...

**Register 12.10. SOC\_ETM\_EVT\_ST7\_REG (0x01E0)**

Continued from the previous page...

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH1\_ST** Represents the status of DMA2D\_EVT\_OUT\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH2\_ST** Represents the status of DMA2D\_EVT\_OUT\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CHO\_ST** Represents the status of DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CHO.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH1\_ST** Represents the status of DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH1.

0: Not received

1: Received

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH2\_ST** Represents the status of DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH2.

0: Not received

1: Received

(R/WTC/SS)



|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |
| SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH3_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH2_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH1_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_LEDC_TASK_TIMER3_RES_UPDATE_CH0_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_LEDC_TASK_TIMER2_RES_UPDATE_ST     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_TIMER1_RES_UPDATE_ST     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH7_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH6_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH5_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH4_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH3_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH2_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH1_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH0_TOGGLE_ST            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH7_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH6_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH5_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH4_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH3_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH2_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH1_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH0_CLEAR_ST             |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH7_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH6_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH5_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH4_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH3_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH2_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| SOC_ETM_GPIO_TASK_CH0_SET_ST               |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |

(R/WTC/SS)

(R/WTC/SS)

(R/WTC/SS)

(R/WTC/SS)

(R/WTC/SS)

(R/WTC/SS)

(R/WTC/SS)

**Register 12.11. SOC\_ETM\_TASK\_STO\_REG (0x01E8)**

Continued from the previous page...

**SOC\_ETM\_GPIO\_TASK\_CH7\_SET\_ST** Represents the status of GPIO\_TASK\_CH7\_SET.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH0\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH0\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH1\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH1\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH2\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH2\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH3\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH3\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH4\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH4\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH5\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH5\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH6\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH6\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH7\_CLEAR\_ST** Represents the status of GPIO\_TASK\_CH7\_CLEAR.

0: Not generated  
1: Generated  
(R/WTC/SS)

Continued on the next page...

**Register 12.11. SOC\_ETM\_TASK\_STO\_REG (0x01E8)**

Continued from the previous page...

**SOC\_ETM\_GPIO\_TASK\_CH0\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH0\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH1\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH1\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH2\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH2\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH3\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH3\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH4\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH4\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH5\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH5\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH6\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH6\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GPIO\_TASK\_CH7\_TOGGLE\_ST** Represents the status of GPIO\_TASK\_CH7\_TOGGLE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_RES\_UPDATE\_ST** Represents the status of LEDC\_TASK\_TIMER0\_RES\_UPDATE.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

## Register 12.11. SOC\_ETM\_TASK\_STO\_REG (0x01E8)

Continued from the previous page...

|   |            |     |        |    |
|---|------------|-----|--------|----|
| <b>SOC_ETM_LEDC_TASK_TIMER1_RES_UPDATE_ST</b>     | Represents | the | status | of |
| LEDC_TASK_TIMER1_RES_UPDATE.                      |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_TIMER2_RES_UPDATE_ST</b>     | Represents | the | status | of |
| LEDC_TASK_TIMER2_RES_UPDATE.                      |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_TIMER3_RES_UPDATE_ST</b>     | Represents | the | status | of |
| LEDC_TASK_TIMER3_RES_UPDATE.                      |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CHO_ST</b> | Represents | the | status | of |
| LEDC_TASK_DUTY_SCALE_UPDATE_CHO.                  |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH1_ST</b> | Represents | the | status | of |
| LEDC_TASK_DUTY_SCALE_UPDATE_CH1.                  |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH2_ST</b> | Represents | the | status | of |
| LEDC_TASK_DUTY_SCALE_UPDATE_CH2.                  |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH3_ST</b> | Represents | the | status | of |
| LEDC_TASK_DUTY_SCALE_UPDATE_CH3.                  |            |     |        |    |
| 0: Not generated                                  |            |     |        |    |
| 1: Generated                                      |            |     |        |    |
| (R/WTC/SS)  |            |     |        |    |

Register 12.12. SOC\_ETM\_TASK\_ST1\_REG (0x01F0)

| Soc  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| Soc_ETM_LEDC_Task_Timer3_Resume_St         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer2_Resume_St         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer1_Resume_St         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer0_Resume_St         |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer3_Rst_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer2_Rst_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer1_Rst_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer0_Rst_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch7_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch6_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch5_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch4_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch3_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch2_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Ovf_Cnt_Rst_Ch1_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch0_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch7_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch6_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch5_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch4_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch3_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch2_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Sig_Out_Dis_Ch1_St       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer3_Cap_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer2_Cap_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer1_Cap_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Timer0_Cap_St            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Duty_Scale_Update_Ch7_St |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Duty_Scale_Update_Ch6_St |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Duty_Scale_Update_Ch5_St |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_Task_Duty_Scale_Update_Ch4_St |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH4\_ST** Represents the status of LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH4.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH5\_ST** Represents the status of LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH5.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH6\_ST** Represents the status of LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH6.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH7\_ST** Represents the status of LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH7.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_CAP\_ST** Represents the status of LEDC\_TASK\_TIMER0\_CAP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER1\_CAP\_ST** Represents the status of LEDC\_TASK\_TIMER1\_CAP.

0: Not generated

1: Generated

(R/WTC/SS)

**Register 12.12. SOC\_ETM\_TASK\_ST1\_REG (0x01F0)****Continued from the previous page...****SOC\_ETM\_LEDC\_TASK\_TIMER2\_CAP\_ST** Represents the status of LEDC\_TASK\_TIMER2\_CAP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER3\_CAP\_ST** Represents the status of LEDC\_TASK\_TIMER3\_CAP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CHO\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH1\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH2\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH3\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CH3.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH4\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CH4.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH5\_ST** Represents the status of LEDC\_TASK\_SIG\_OUT\_DIS\_CH5.

0: Not generated

1: Generated

(R/WTC/SS)

**Continued on the next page...**

## Register 12.12. SOC\_ETM\_TASK\_ST1\_REG (0x01F0)

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH6\_ST** Represents the status of  
LEDC\_TASK\_SIG\_OUT\_DIS\_CH6.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_SIG\_OUT\_DIS\_CH7\_ST** Represents the status of  
LEDC\_TASK\_SIG\_OUT\_DIS\_CH7.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH0\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH1\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH2\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH3\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH3.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH4\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH4.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH5\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH5.

0: Not generated

1: Generated

(R/WTC/SS)

**Register 12.12. SOC\_ETM\_TASK\_ST1\_REG (0x01F0)****Continued from the previous page...**

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH6\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH6.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_OVF\_CNT\_RST\_CH7\_ST** Represents the status of  
LEDC\_TASK\_OVF\_CNT\_RST\_CH7.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_RST\_ST** Represents the status of LEDC\_TASK\_TIMER0\_RST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER1\_RST\_ST** Represents the status of LEDC\_TASK\_TIMER1\_RST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER2\_RST\_ST** Represents the status of LEDC\_TASK\_TIMER2\_RST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER3\_RST\_ST** Represents the status of LEDC\_TASK\_TIMER3\_RST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_RESUME\_ST** Represents the status of  
LEDC\_TASK\_TIMER0\_RESUME.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER1\_RESUME\_ST** Represents the status of  
LEDC\_TASK\_TIMER1\_RESUME.

0: Not generated

1: Generated

(R/WTC/SS)

**Continued on the next page...**



## Register 12.12. SOC\_ETM\_TASK\_ST1\_REG (0x01F0)

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_TIMER2\_RESUME\_ST** Represents the status of  
LEDC\_TASK\_TIMER2\_RESUME.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER3\_RESUME\_ST** Represents the status of  
LEDC\_TASK\_TIMER3\_RESUME.

0: Not generated

1: Generated

(R/WTC/SS)

Register 12.13. SOC\_ETM\_TASK\_ST2\_REG (0x01F8)

| Soc                                   |                                     |  |                                       |                                       |                                       |                                       |                                       |                                       |                                       |                                      |                                      |                                      |                                      |                                      |                                      |                                      |                                      |  |  |  |  |  |  |                                   |                                   |                                   |                                   |   |   |   |   |       |
|---------------------------------------|-------------------------------------|--|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--|--|--|--|--|--|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|---|---|---|---|-------|
| 31                                    | 30                                  | 29                                     | 28                                    | 27                                    | 26                                    | 25                                    | 24                                    | 23                                    | 22                                    | 21                                   | 20                                   | 19                                   | 18                                   | 17                                   | 16                                   | 15                                   | 14                                   | 13                                     | 12                                     | 11                                     | 10                                     | 9                                      | 8                                      | 7                                 | 6                                 | 5                                 | 4                                 | 3 | 2 | 1 | 0 | Reset |
| SOC_ETM_TGO_TASK_CNT_RELOAD_TIMER0_ST | SOC_ETM_TGO_TASK_CNT_STOP_TIMER0_ST | SOC_ETM_TGO_TASK_ALARM_START_TIMER0_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH7_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH6_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH5_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH4_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH3_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH2_ST | SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH1_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH0_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH7_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH6_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH5_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH4_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH3_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH2_ST | SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH1_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH7_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH6_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH5_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH4_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH3_ST | SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH2_ST | SOC_ETM_LEDC_TASK_TIMER3_PAUSE_ST | SOC_ETM_LEDC_TASK_TIMER2_PAUSE_ST | SOC_ETM_LEDC_TASK_TIMER1_PAUSE_ST | SOC_ETM_LEDC_TASK_TIMER0_PAUSE_ST |   |   |   |   |       |
| 0                                     | 0                                   | 0                                      | 0                                     | 0                                     | 0                                     | 0                                     | 0                                     | 0                                     | 0                                     | 0                                    | 0                                    | 0                                    | 0                                    | 0                                    | 0                                    | 0                                    | 0                                    | 0                                      | 0                                      | 0                                      | 0                                      | 0                                      | 0                                      | 0                                 | 0                                 | 0                                 | 0                                 | 0 | 0 | 0 | 0 |       |

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_PAUSE\_ST** Represents the status of LEDC\_TASK\_TIMER0\_PAUSE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER1\_PAUSE\_ST** Represents the status of LEDC\_TASK\_TIMER1\_PAUSE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER2\_PAUSE\_ST** Represents the status of LEDC\_TASK\_TIMER2\_PAUSE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_TIMER3\_PAUSE\_ST** Represents the status of LEDC\_TASK\_TIMER3\_PAUSE.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CHO\_ST** Represents the status of LEDC\_TASK\_GAMMA\_RESTART\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

## Register 12.13. SOC\_ETM\_TASK\_ST2\_REG (0x01F8)

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH1\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH2\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH3\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH3.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH4\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH4.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH5\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH5.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH6\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH6.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CH7\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESTART\_CH7.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_PAUSE\_CHO\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_PAUSE\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**Register 12.13. SOC\_ETM\_TASK\_ST2\_REG (0x01F8)**

Continued from the previous page...

|   |            |     |        |    |
|---|------------|-----|--------|----|
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH1_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH1.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH2_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH2.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH3_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH3.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH4_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH4.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH5_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH5.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH6_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH6.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH7_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_PAUSE_CH7.                  |            |     |        |    |
| 0: Not generated                            |            |     |        |    |
| 1: Generated                                |            |     |        |    |
| (R/WTC/SS)                                  |            |     |        |    |

Continued on the next page...

**Register 12.13. SOC\_ETM\_TASK\_ST2\_REG (0x01F8)**

Continued from the previous page...

|  |            |     |        |    |
|--|------------|-----|--------|----|
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CHO_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CHO.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH1_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH1.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH2_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH2.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH3_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH3.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH4_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH4.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH5_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH5.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH6_ST</b> | Represents | the | status | of |
| LEDC_TASK_GAMMA_RESUME_CH6.                  |            |     |        |    |
| 0: Not generated                             |            |     |        |    |
| 1: Generated                                 |            |     |        |    |
| (R/WTC/SS)                                   |            |     |        |    |

Continued on the next page...

## Register 12.13. SOC\_ETM\_TASK\_ST2\_REG (0x01F8)

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH7\_ST** Represents the status of  
LEDC\_TASK\_GAMMA\_RESUME\_CH7.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_START\_TIMER0\_ST** Represents the status of  
TGO\_TASK\_CNT\_START\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_ALARM\_START\_TIMER0\_ST** Represents the status of  
TGO\_TASK\_ALARM\_START\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_STOP\_TIMER0\_ST** Represents the status of  
TGO\_TASK\_CNT\_STOP\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_RELOAD\_TIMER0\_ST** Represents the status of  
TGO\_TASK\_CNT\_RELOAD\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

### Register 12.14. SOC\_ETM\_TASK\_ST3\_REG (0x0200)

[illegible]

**SOC\_ETM\_TGO\_TASK\_CNT\_CAP\_TIMER0\_ST** Represents the status of TGO\_TASK\_CNT\_CAP\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_START\_TIMER1\_ST** Represents the status of TGO\_TASK\_CNT\_START\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_ALARM\_START\_TIMER1\_ST** Represents the status of TGO\_TASK\_ALARM\_START\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_STOP\_TIMER1\_ST** Represents the status of TGO TASK CNT\_STOP\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TGO\_TASK\_CNT\_RELOAD\_TIMER1\_ST** Represents the status of TGO TASK CNT RELOAD TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

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## Register 12.14. SOC\_ETM\_TASK\_ST3\_REG (0x0200)

Continued from the previous page...

**SOC\_ETM\_TGO\_TASK\_CNT\_CAP\_TIMER1\_ST** Represents the status of TGO\_TASK\_CNT\_CAP\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_START\_TIMER0\_ST** Represents the status of TG1\_TASK\_CNT\_START\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_ALARM\_START\_TIMER0\_ST** Represents the status of TG1\_TASK\_ALARM\_START\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_STOP\_TIMER0\_ST** Represents the status of TG1\_TASK\_CNT\_STOP\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_RELOAD\_TIMER0\_ST** Represents the status of TG1\_TASK\_CNT\_RELOAD\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_CAP\_TIMER0\_ST** Represents the status of TG1\_TASK\_CNT\_CAP\_TIMER0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_START\_TIMER1\_ST** Represents the status of TG1\_TASK\_CNT\_START\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_ALARM\_START\_TIMER1\_ST** Represents the status of TG1\_TASK\_ALARM\_START\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)



**Register 12.14. SOC\_ETM\_TASK\_ST3\_REG (0x0200)**

Continued from the previous page...

**SOC\_ETM\_TG1\_TASK\_CNT\_STOP\_TIMER1\_ST** Represents the status of  
TG1\_TASK\_CNT\_STOP\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_RELOAD\_TIMER1\_ST** Represents the status of  
TG1\_TASK\_CNT\_RELOAD\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_TG1\_TASK\_CNT\_CAP\_TIMER1\_ST** Represents the status of TG1\_TASK\_CNT\_CAP\_TIMER1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_CMPRO\_A\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPRO\_A\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_CMPR1\_A\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPR1\_A\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_CMPR2\_A\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPR2\_A\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_CMPRO\_B\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPRO\_B\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

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**Register 12.14. SOC\_ETM\_TASK\_ST3\_REG (0x0200)**

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**SOC\_ETM\_MCPWMO\_TASK\_CMPR1\_B\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPR1\_B\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_CMPR2\_B\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_CMPR2\_B\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_GEN\_STOP\_ST** Represents the status of MCPWMO\_TASK\_GEN\_STOP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER0\_SYN\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER0\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER1\_SYN\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER1\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER2\_SYN\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER2\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER0\_PERIOD\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER0\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

**Register 12.14. SOC\_ETM\_TASK\_ST3\_REG (0x0200)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_TASK\_TIMER1\_PERIOD\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER1\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER2\_PERIOD\_UP\_ST** Represents the status of  
MCPWMO\_TASK\_TIMER2\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TZO\_OST\_ST** Represents the status of MCPWMO\_TASK\_TZO\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TZ1\_OST\_ST** Represents the status of MCPWMO\_TASK\_TZ1\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWMO\_TASK\_TZ2\_OST\_ST** Represents the status of MCPWMO\_TASK\_TZ2\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

Register 12.15. SOC\_ETM\_TASK\_ST4\_REG (0x0208)

|                           |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOC_ETM_ADC_TASK_STOPO_ST |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_TASK_STARTO_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_TASK_SAMPLEO_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAP2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAP1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAPO_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLR2_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLR1_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLRO_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TZ2_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TZ1_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TZO_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER2_PERIOD_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER1_PERIOD_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER0_PERIOD_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER2_SYN_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER1_SYN_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_TIMER0_SYN_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_GEN_STOP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CMPR2_B_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CMPR1_B_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CMPR2_A_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CMPR1_A_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CMPR0_A_UP_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAP2_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAP1_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CAPO_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLR2_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLR1_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_TASK_CLRO_OST_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                        | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |                            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                         | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SOC\_ETM\_MCPWM0\_TASK\_CLRO\_OST\_ST** Represents the status of MCPWM0\_TASK\_CLRO\_OST.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_TASK\_CLR1\_OST\_ST** Represents the status of MCPWM0\_TASK\_CLR1\_OST.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_TASK\_CLR2\_OST\_ST** Represents the status of MCPWM0\_TASK\_CLR2\_OST.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_TASK\_CAPO\_ST** Represents the status of MCPWM0\_TASK\_CAPO.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_TASK\_CAP1\_ST** Represents the status of MCPWM0\_TASK\_CAP1.

0: Not generated  
1: Generated  
(R/WTC/SS)

**SOC\_ETM\_MCPWM0\_TASK\_CAP2\_ST** Represents the status of MCPWM0\_TASK\_CAP2.

0: Not generated  
1: Generated  
(R/WTC/SS)

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## Register 12.15. SOC\_ETM\_TASK\_ST4\_REG (0x0208)

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|  |  |     |        |    |
|--|--|-----|--------|----|
| <b>SOC_ETM_MCPWM1_TASK_CMPRO_A_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPRO_A_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_CMPR1_A_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPR1_A_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_CMPR2_A_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPR2_A_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_CMPRO_B_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPRO_B_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_CMPR1_B_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPR1_B_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_CMPR2_B_UP_ST</b> | Represents                                     | the | status | of |
| MCPWM1_TASK_CMPR2_B_UP.                  |  |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |
| <b>SOC_ETM_MCPWM1_TASK_GEN_STOP_ST</b>   | Represents the status of MCPWM1_TASK_GEN_STOP. |     |        |    |
| 0: Not generated                         |  |     |        |    |
| 1: Generated                             |  |     |        |    |
| (R/WTC/SS)                               |  |     |        |    |

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## Register 12.15. SOC\_ETM\_TASK\_ST4\_REG (0x0208)

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**SOC\_ETM\_MCPWM1\_TASK\_TIMER0\_SYN\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER0\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER1\_SYN\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER1\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER2\_SYN\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER2\_SYN.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER0\_PERIOD\_UP\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER0\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER1\_PERIOD\_UP\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER1\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER2\_PERIOD\_UP\_ST** Represents the status of  
MCPWM1\_TASK\_TIMER2\_PERIOD\_UP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TZO\_OST\_ST** Represents the status of MCPWM1\_TASK\_TZO\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

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**Register 12.15. SOC\_ETM\_TASK\_ST4\_REG (0x0208)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_TASK\_TZ1\_OST\_ST** Represents the status of MCPWM1\_TASK\_TZ1\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_TZ2\_OST\_ST** Represents the status of MCPWM1\_TASK\_TZ2\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_CLRO\_OST\_ST** Represents the status of MCPWM1\_TASK\_CLRO\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_CLR1\_OST\_ST** Represents the status of MCPWM1\_TASK\_CLR1\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_CLR2\_OST\_ST** Represents the status of MCPWM1\_TASK\_CLR2\_OST.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_CAPO\_ST** Represents the status of MCPWM1\_TASK\_CAPO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_MCPWM1\_TASK\_CAP1\_ST** Represents the status of MCPWM1\_TASK\_CAP1.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

**Register 12.15. SOC\_ETM\_TASK\_ST4\_REG (0x0208)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_TASK\_CAP2\_ST** Represents the status of MCPWM1\_TASK\_CAP2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_ADC\_TASK\_SAMPLE0\_ST** Represents the status of ADC\_TASK\_SAMPLE0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_ADC\_TASK\_START0\_ST** Represents the status of ADC\_TASK\_START0.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_ADC\_TASK\_STOP0\_ST** Represents the status of ADC\_TASK\_STOP0.

0: Not generated

1: Generated

(R/WTC/SS)



Register 12.16. SOC\_ETM\_TASK\_ST5\_REG (0x0210)

|                                       |                                       |  |  |                                       |                                       |                                |                         |                          |                           |                                 |                              |                              |                               |                              |                              |                               |                              |                              |                                  |                                 |                                     |                               |                               |                               |                               |   |   |   |   |   |       |
|---------------------------------------|---------------------------------------|--|--|---------------------------------------|---------------------------------------|--------------------------------|-------------------------|--------------------------|---------------------------|---------------------------------|------------------------------|------------------------------|-------------------------------|------------------------------|------------------------------|-------------------------------|------------------------------|------------------------------|----------------------------------|---------------------------------|-------------------------------------|-------------------------------|-------------------------------|-------------------------------|-------------------------------|---|---|---|---|---|-------|
| SOC_ETM_GDMA_AXI_TASK_IN_START_CH1_ST | SOC_ETM_GDMA_AXI_TASK_IN_START_CH0_ST | SOC_ETM_GDMA_AHB_TASK_OUT_START_CH2_ST | SOC_ETM_GDMA_AHB_TASK_OUT_START_CH1_ST | SOC_ETM_GDMA_AHB_TASK_IN_START_CH0_ST | SOC_ETM_GDMA_AHB_TASK_IN_START_CH1_ST | SOC_ETM_RTC_TASK_TRIGGERFLW_ST | SOC_ETM_RTC_TASK_CLR_ST | SOC_ETM_ULP_TASK_STOP_ST | SOC_ETM_ULP_TASK_START_ST | SOC_ETM_I2S2_TASK_WAKEUP_CPU_ST | SOC_ETM_I2S2_TASK_STOP_TX_ST | SOC_ETM_I2S2_TASK_STOP_RX_ST | SOC_ETM_I2S1_TASK_START_TX_ST | SOC_ETM_I2S1_TASK_STOP_TX_ST | SOC_ETM_I2S1_TASK_STOP_RX_ST | SOC_ETM_I2S0_TASK_START_TX_ST | SOC_ETM_I2S0_TASK_STOP_TX_ST | SOC_ETM_I2S0_TASK_STOP_RX_ST | SOC_ETM_TMPSNSR_TASK_START_TX_ST | SOC_ETM_TMPSNSR_TASK_STOP_RX_ST | SOC_ETM_REGDMA_TASK_START_SAMPLE_ST | SOC_ETM_REGDMA_TASK_START3_ST | SOC_ETM_REGDMA_TASK_START2_ST | SOC_ETM_REGDMA_TASK_START1_ST | SOC_ETM_REGDMA_TASK_START0_ST |   |   |   |   |   |       |
| 31                                    | 30                                    | 29                                     | 28                                     | 27                                    | 26                                    | 25                             | 24                      | 23                       | 22                        | 21                              | 20                           | 19                           | 18                            | 17                           | 16                           | 15                            | 14                           | 13                           | 12                               | 11                              | 10                                  | 9                             | 8                             | 7                             | 6                             | 5 | 4 | 3 | 2 | 1 | 0     |
| 0                                     | 0                                     | 0                                      | 0                                      | 0                                     | 0                                     | 0                              | 0                       | 0                        | 0                         | 0                               | 0                            | 0                            | 0                             | 0                            | 0                            | 0                             | 0                            | 0                            | 0                                | 0                               | 0                                   | 0                             | 0                             | 0                             | 0                             | 0 | 0 | 0 | 0 | 0 | Reset |

**SOC\_ETM\_REGDMA\_TASK\_START0\_ST** Represents the status of REGDMA\_TASK\_START0.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

**SOC\_ETM\_REGDMA\_TASK\_START1\_ST** Represents the status of REGDMA\_TASK\_START1.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

**SOC\_ETM\_REGDMA\_TASK\_START2\_ST** Represents the status of REGDMA\_TASK\_START2.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

**SOC\_ETM\_REGDMA\_TASK\_START3\_ST** Represents the status of REGDMA\_TASK\_START3.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

**SOC\_ETM\_TMPSNSR\_TASK\_START\_SAMPLE\_ST** Represents the status of TMP-SNSR\_TASK\_START\_SAMPLE.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

**SOC\_ETM\_TMPSNSR\_TASK\_STOP\_SAMPLE\_ST** Represents the status of TMP-SNSR\_TASK\_STOP\_SAMPLE.

- 0: Not generated
- 1: Generated
- (R/WTC/SS)

Continued on the next page...

**Register 12.16. SOC\_ETM\_TASK\_ST5\_REG (0x0210)**

Continued from the previous page...

**SOC\_ETM\_I2SO\_TASK\_START\_RX\_ST** Represents the status of I2SO\_TASK\_START\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2SO\_TASK\_START\_TX\_ST** Represents the status of I2SO\_TASK\_START\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2SO\_TASK\_STOP\_RX\_ST** Represents the status of I2SO\_TASK\_STOP\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2SO\_TASK\_STOP\_TX\_ST** Represents the status of I2SO\_TASK\_STOP\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S1\_TASK\_START\_RX\_ST** Represents the status of I2S1\_TASK\_START\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S1\_TASK\_START\_TX\_ST** Represents the status of I2S1\_TASK\_START\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S1\_TASK\_STOP\_RX\_ST** Represents the status of I2S1\_TASK\_STOP\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S1\_TASK\_STOP\_TX\_ST** Represents the status of I2S1\_TASK\_STOP\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S2\_TASK\_START\_RX\_ST** Represents the status of I2S2\_TASK\_START\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S2\_TASK\_START\_TX\_ST** Represents the status of I2S2\_TASK\_START\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

**Register 12.16. SOC\_ETM\_TASK\_ST5\_REG (0x0210)**

Continued from the previous page...

**SOC\_ETM\_I2S2\_TASK\_STOP\_RX\_ST** Represents the status of I2S2\_TASK\_STOP\_RX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_I2S2\_TASK\_STOP\_TX\_ST** Represents the status of I2S2\_TASK\_STOP\_TX.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_ULP\_TASK\_WAKEUP\_CPU\_ST** Represents the status of ULP\_TASK\_WAKEUP\_CPU.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_ULP\_TASK\_INT\_CPU\_ST** Represents the status of ULP\_TASK\_INT\_CPU.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_RTC\_TASK\_START\_ST** Represents the status of RTC\_TASK\_START.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_RTC\_TASK\_STOP\_ST** Represents the status of RTC\_TASK\_STOP.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_RTC\_TASK\_CLR\_ST** Represents the status of RTC\_TASK\_CLR.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_RTC\_TASK\_TRIGGERFLW\_ST** Represents the status of RTC\_TASK\_TRIGGERFLW.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

## Register 12.16. SOC\_ETM\_TASK\_ST5\_REG (0x0210)

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CHO\_ST** Represents the status of  
GDMA\_AHB\_TASK\_IN\_START\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CH1\_ST** Represents the status of  
GDMA\_AHB\_TASK\_IN\_START\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CH2\_ST** Represents the status of  
GDMA\_AHB\_TASK\_IN\_START\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_TASK\_OUT\_START\_CHO\_ST** Represents the status of  
GDMA\_AHB\_TASK\_OUT\_START\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_TASK\_OUT\_START\_CH1\_ST** Represents the status of  
GDMA\_AHB\_TASK\_OUT\_START\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AHB\_TASK\_OUT\_START\_CH2\_ST** Represents the status of  
GDMA\_AHB\_TASK\_OUT\_START\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_TASK\_IN\_START\_CHO\_ST** Represents the status of  
GDMA\_AXI\_TASK\_IN\_START\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_GDMA\_AXI\_TASK\_IN\_START\_CH1\_ST** Represents the status of  
GDMA\_AXI\_TASK\_IN\_START\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

### Register 12.17. SOC\_ETM\_TASK\_ST6\_REG (0x0218)

|    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
|    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 14                                       | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_OUT_DSCR_READY_CH2_ST |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_DMA2D_TASK_OUT_DSCR_READY_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_OUT_DSCR_READY_CH0_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_OUT_START_CH2_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_OUT_START_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_OUT_START_CH0_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_IN_DSCR_READY_CH2_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_IN_DSCR_READY_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_IN_START_CH2_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_IN_START_CH1_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_DMA2D_TASK_IN_START_CH0_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|  |  |
|--|--|
| <b>SOC_ETM_GDMA_AXI_TASK_IN_START_CH2_ST</b> | Represents the status of GDMA_AXI_TASK_IN_START_CH2. |
| 0:   | Not generated  |
| 1:   | Generated  |
| (R/WTC/SS)                                   |  |

|   |   |
|---|---|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CHO_ST</b> | Represents the status of GDMA_AXI_TASK_OUT_START_CHO. |
| 0:  | Not generated   |
| 1:  | Generated   |
| (R/WTC/SS)                                    |   |

|   |   |
|---|---|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CH1_ST</b> | Represents the status of GDMA_AXI_TASK_OUT_START_CH1. |
| 0:  | Not generated   |
| 1:  | Generated   |
| (R/WTC/SS)                                    |   |

|   |   |
|---|---|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CH2_ST</b> | Represents the status of GDMA_AXI_TASK_OUT_START_CH2. |
| 0:  | Not generated   |
| 1:  | Generated   |
| (R/WTC/SS)                                    |   |

**SOC\_ETM\_PMU\_TASK\_SLEEP\_REQ\_ST** Represents the status of PMU\_TASK\_SLEEP\_REQ.

- 0: Not generated
- 1: Generated

(R/WTC/SS)

|   |            |     |        |    |
|---|------------|-----|--------|----|
| <b>SOC_ETM_DMA2D_TASK_IN_START_CHO_ST</b> | Represents | the | status | of |
| DMA2D_TASK_IN_START_CHO.                  |            |     |        |    |
| 0: Not generated                          |            |     |        |    |
| 1: Generated                              |            |     |        |    |
| (P/WTC/SS)                                |            |     |        |    |

**Register 12.17. SOC\_ETM\_TASK\_ST6\_REG (0x0218)**

Continued from the previous page...

**SOC\_ETM\_DMA2D\_TASK\_IN\_START\_CH1\_ST** Represents the status of  
DMA2D\_TASK\_IN\_START\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_IN\_DSCR\_READY\_CHO\_ST** Represents the status of  
DMA2D\_TASK\_IN\_DSCR\_READY\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_IN\_DSCR\_READY\_CH1\_ST** Represents the status of  
DMA2D\_TASK\_IN\_DSCR\_READY\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CHO\_ST** Represents the status of  
DMA2D\_TASK\_OUT\_START\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CH1\_ST** Represents the status of  
DMA2D\_TASK\_OUT\_START\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CH2\_ST** Represents the status of  
DMA2D\_TASK\_OUT\_START\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CHO\_ST** Represents the status of  
DMA2D\_TASK\_OUT\_DSCR\_READY\_CHO.

0: Not generated

1: Generated

(R/WTC/SS)

Continued on the next page...

**Register 12.17. SOC\_ETM\_TASK\_ST6\_REG (0x0218)**

Continued from the previous page...

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CH1\_ST** Represents the status of DMA2D\_TASK\_OUT\_DSCR\_READY\_CH1.

0: Not generated

1: Generated

(R/WTC/SS)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CH2\_ST** Represents the status of DMA2D\_TASK\_OUT\_DSCR\_READY\_CH2.

0: Not generated

1: Generated

(R/WTC/SS)

**Register 12.18. SOC\_ETM\_CH\_ENA\_ADO\_SET\_REG (0x0004)**

|                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |                    |                    |                    |                    |                    |                    |                    |                    |                    |                    |
|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| SOC_ETM_CH_ENABLE31 | SOC_ETM_CH_ENABLE30 | SOC_ETM_CH_ENABLE29 | SOC_ETM_CH_ENABLE28 | SOC_ETM_CH_ENABLE27 | SOC_ETM_CH_ENABLE26 | SOC_ETM_CH_ENABLE25 | SOC_ETM_CH_ENABLE24 | SOC_ETM_CH_ENABLE23 | SOC_ETM_CH_ENABLE22 | SOC_ETM_CH_ENABLE21 | SOC_ETM_CH_ENABLE20 | SOC_ETM_CH_ENABLE19 | SOC_ETM_CH_ENABLE18 | SOC_ETM_CH_ENABLE17 | SOC_ETM_CH_ENABLE16 | SOC_ETM_CH_ENABLE15 | SOC_ETM_CH_ENABLE14 | SOC_ETM_CH_ENABLE13 | SOC_ETM_CH_ENABLE12 | SOC_ETM_CH_ENABLE11 | SOC_ETM_CH_ENABLE10 | SOC_ETM_CH_ENABLE9 | SOC_ETM_CH_ENABLE8 | SOC_ETM_CH_ENABLE7 | SOC_ETM_CH_ENABLE6 | SOC_ETM_CH_ENABLE5 | SOC_ETM_CH_ENABLE4 | SOC_ETM_CH_ENABLE3 | SOC_ETM_CH_ENABLE2 | SOC_ETM_CH_ENABLE1 | SOC_ETM_CH_ENABLE0 |
| 31                  | 30                  | 29                  | 28                  | 27                  | 26                  | 25                  | 24                  | 23                  | 22                  | 21                  | 20                  | 19                  | 18                  | 17                  | 16                  | 15                  | 14                  | 13                  | 12                  | 11                  | 10                  | 9                  | 8                  | 7                  | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                  |
| 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  | 0                  |

Reset

**SOC\_ETM\_CH\_ENABLE<sub>n</sub>** (**n**: 0-31) Configures whether to enable channel<sub>n</sub>.

0: Invalid. No effect

1: Enable

(WT)

**Register 12.19. SOC\_ETM\_CH\_ENA\_ADO\_CLR\_REG (0x0008)**

|                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                      |                     |                     |                     |                     |                     |                     |                     |                     |                     |                     |
|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|----------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|
| SOC_ETM_CH_DISABLE31 | SOC_ETM_CH_DISABLE30 | SOC_ETM_CH_DISABLE29 | SOC_ETM_CH_DISABLE28 | SOC_ETM_CH_DISABLE27 | SOC_ETM_CH_DISABLE26 | SOC_ETM_CH_DISABLE25 | SOC_ETM_CH_DISABLE24 | SOC_ETM_CH_DISABLE23 | SOC_ETM_CH_DISABLE22 | SOC_ETM_CH_DISABLE21 | SOC_ETM_CH_DISABLE20 | SOC_ETM_CH_DISABLE19 | SOC_ETM_CH_DISABLE18 | SOC_ETM_CH_DISABLE17 | SOC_ETM_CH_DISABLE16 | SOC_ETM_CH_DISABLE15 | SOC_ETM_CH_DISABLE14 | SOC_ETM_CH_DISABLE13 | SOC_ETM_CH_DISABLE12 | SOC_ETM_CH_DISABLE11 | SOC_ETM_CH_DISABLE10 | SOC_ETM_CH_DISABLE9 | SOC_ETM_CH_DISABLE8 | SOC_ETM_CH_DISABLE7 | SOC_ETM_CH_DISABLE6 | SOC_ETM_CH_DISABLE5 | SOC_ETM_CH_DISABLE4 | SOC_ETM_CH_DISABLE3 | SOC_ETM_CH_DISABLE2 | SOC_ETM_CH_DISABLE1 | SOC_ETM_CH_DISABLE0 |
| 31                   | 30                   | 29                   | 28                   | 27                   | 26                   | 25                   | 24                   | 23                   | 22                   | 21                   | 20                   | 19                   | 18                   | 17                   | 16                   | 15                   | 14                   | 13                   | 12                   | 11                   | 10                   | 9                   | 8                   | 7                   | 6                   | 5                   | 4                   | 3                   | 2                   | 1                   | 0                   |
| 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                    | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | 0                   | Reset               |

**SOC\_ETM\_CH\_DISABLE $n$**  ( $n$ : 0-31) Configures whether to disable channel 0.

0: Invalid. No effect

1: Disable

(WT)

**Register 12.20. SOC\_ETM\_CH\_ENA\_AD1\_SET\_REG (0x0010)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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 |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  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 |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_CH\_ENABLE $n$**  ( $n$ : 32-49) Configures whether to enable channel $n$ .

0: Invalid. No effect

1: Enable

(WT)



## Register 12.21. SOC\_ETM\_CH\_ENA\_AD1\_CLR\_REG (0x0014)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|---|---|---|-------|---|---|---|---|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_CH_DISABLE49<br>SOC_ETM_CH_DISABLE48<br>SOC_ETM_CH_DISABLE47<br>SOC_ETM_CH_DISABLE46<br>SOC_ETM_CH_DISABLE45<br>SOC_ETM_CH_DISABLE44<br>SOC_ETM_CH_DISABLE43<br>SOC_ETM_CH_DISABLE42<br>SOC_ETM_CH_DISABLE41<br>SOC_ETM_CH_DISABLE40<br>SOC_ETM_CH_DISABLE39<br>SOC_ETM_CH_DISABLE38<br>SOC_ETM_CH_DISABLE37<br>SOC_ETM_CH_DISABLE36<br>SOC_ETM_CH_DISABLE35<br>SOC_ETM_CH_DISABLE34<br>SOC_ETM_CH_DISABLE33 |    |    |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 18   | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6     | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | Reset |   |   |   |   |   |   |  |  |

**SOC\_ETM\_CH\_DISABLE $n$**  ( $n$ : 32-49) Configures whether to disable channel $n$ .

0: Invalid. No effect

1: Disable

(WT)

Register 12.22. SOC\_ETM\_CH $n$ \_EVT\_ID\_REG ( $n$ : 0-49) (0x0018+0x8\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_CH <sup>n</sup> _EVT_ID |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                               | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                               |   |   |  |  |  |  |  | Reset |  |

**SOC\_ETM\_CH $n$ \_EVT\_ID** ( $n$ : 0-49) Configures the event ID of channel $n$ . See Table 12.3-1. (R/W)

Register 12.23. SOC\_ETM\_CH $n$ \_TASK\_ID\_REG ( $n$ : 0-49) (0x001C+0x8\* $n$ )

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SOC_ETM_CH <sub>n</sub> _TASK_ID |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                                | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                |   |   |  |  |  |  |  | Reset |  |

**SOC\_ETM\_CH $n$ \_TASK\_ID** ( $n$ : 0-49) Configures the task ID of channel $n$ . See Table 12.3-2. (R/W)

Register 12.24. SOC\_ETM\_EVT\_STO\_CLR\_REG (0x01AC)

| Soc                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| Soc ETM LEDC EVT DUTY CHNG_END_CH3_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM LEDC EVT DUTY CHNG_END_CH2_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM LEDC EVT DUTY CHNG_END_CH1_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_ZERO_DET_NEG1_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_ZERO_DET_POS1_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_ZERO_DET_NEG0_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH7_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH6_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH5_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH4_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH3_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH2_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH1_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CHO_ANY_EDGE_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH7_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH6_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH5_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH4_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH3_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH2_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH1_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CHO_FALL_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH7_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH6_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH5_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH4_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH3_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CH2_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Soc ETM GPIO EVT_CHO_RISE_EDGE_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_GPIO\_EVT\_CHO\_RISE\_EDGE\_ST\_CLR** Configures whether to clear GPIO\_EVT\_CHO\_RISE\_EDGE.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_GPIO\_EVT\_CH1\_RISE\_EDGE\_ST\_CLR** Configures whether to clear GPIO\_EVT\_CH1\_RISE\_EDGE.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_GPIO\_EVT\_CH2\_RISE\_EDGE\_ST\_CLR** Configures whether to clear GPIO\_EVT\_CH2\_RISE\_EDGE.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_GPIO\_EVT\_CH3\_RISE\_EDGE\_ST\_CLR** Configures whether to clear GPIO\_EVT\_CH3\_RISE\_EDGE.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_GPIO\_EVT\_CH4\_RISE\_EDGE\_ST\_CLR** Configures whether to clear GPIO\_EVT\_CH4\_RISE\_EDGE.  
 0: Invalid. No effect  
 1: Clear (WT)

Continued on the next page...

**Register 12.24. SOC\_ETM\_EVT\_STO\_CLR\_REG (0x01AC)**

Continued from the previous page...

|  |   |         |    |       |
|--|---|---------|----|-------|
| <b>SOC_ETM_GPIO_EVT_CH5_RISE_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH5_RISE_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH6_RISE_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH6_RISE_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH7_RISE_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH7_RISE_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH0_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH0_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH1_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH1_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH2_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH2_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH3_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH3_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |

Continued on the next page...

**Register 12.24. SOC\_ETM\_EVT\_STO\_CLR\_REG (0x01AC)**

Continued from the previous page...

|  |   |         |    |       |
|--|---|---------|----|-------|
| <b>SOC_ETM_GPIO_EVT_CH4_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH4_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH5_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH5_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH6_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH6_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH7_FALL_EDGE_ST_CLR</b> | Configures GPIO_EVT_CH7_FALL_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CHO_ANY_EDGE_ST_CLR</b>  | Configures GPIO_EVT_CHO_ANY_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT)  | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH1_ANY_EDGE_ST_CLR</b>  | Configures GPIO_EVT_CH1_ANY_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT)  | whether | to | clear |
| <b>SOC_ETM_GPIO_EVT_CH2_ANY_EDGE_ST_CLR</b>  | Configures GPIO_EVT_CH2_ANY_EDGE.<br>0: Invalid. No effect<br>1: Clear<br>(WT)  | whether | to | clear |

Continued on the next page...

**Register 12.24. SOC\_ETM\_EVT\_STO\_CLR\_REG (0x01AC)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_GPIO_EVT_CH3_ANY_EDGE_ST_CLR</b>  | Configures | whether | to | clear |
| GPIO_EVT_CH3_ANY_EDGE.                       |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_CH4_ANY_EDGE_ST_CLR</b>  | Configures | whether | to | clear |
| GPIO_EVT_CH4_ANY_EDGE.                       |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_CH5_ANY_EDGE_ST_CLR</b>  | Configures | whether | to | clear |
| GPIO_EVT_CH5_ANY_EDGE.                       |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_CH6_ANY_EDGE_ST_CLR</b>  | Configures | whether | to | clear |
| GPIO_EVT_CH6_ANY_EDGE.                       |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_CH7_ANY_EDGE_ST_CLR</b>  | Configures | whether | to | clear |
| GPIO_EVT_CH7_ANY_EDGE.                       |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_ZERO_DET_POS0_ST_CLR</b> | Configures | whether | to | clear |
| GPIO_EVT_ZERO_DET_POS0.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_ZERO_DET_NEG0_ST_CLR</b> | Configures | whether | to | clear |
| GPIO_EVT_ZERO_DET_NEG0.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |

Continued on the next page...

**Register 12.24. SOC\_ETM\_EVT\_STO\_CLR\_REG (0x01AC)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_GPIO_EVT_ZERO_DET_POS1_ST_CLR</b>     | Configures | whether | to | clear |
| GPIO_EVT_ZERO_DET_POS1.                          |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GPIO_EVT_ZERO_DET_NEG1_ST_CLR</b>     | Configures | whether | to | clear |
| GPIO_EVT_ZERO_DET_NEG1.                          |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CHO_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_DUTY_CHNG_END_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_DUTY_CHNG_END_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_DUTY_CHNG_END_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_DUTY_CHNG_END_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |

## Register 12.25. SOC\_ETM\_EVT\_ST1\_CLR\_REG (0x01B4)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SOC_ETM_MCPWMO_EVT_TIMER1_TEZ_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_EVT_TIMER2_TEZ_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_EVT_TIMER2_STOP_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_EVT_TIMER0_STOP_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_SYSTIMER_EVT_TIMER0_STOP_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_SYSTIMER_EVT_CNT_CMP2_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_SYSTIMER_EVT_CNT_CMP1_ST_CLR      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_TG1_EVT_CNT_CMP_TMR0_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_TG1_EVT_CNT_CMP_TMR1_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_TG0_EVT_CNT_CMP_TMR0_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIMER3_CMP_ST_CLR        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIMER2_CMP_ST_CLR        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIMER1_CMP_ST_CLR        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIMER0_CMP_ST_CLR        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIME_OVF_TMR3_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIME_OVF_TMR2_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_TIME_OVF_TMR1_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH7_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH6_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH5_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH4_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH3_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH2_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH1_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH7_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH6_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH5_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_LEDC_EVT_DUTY_CHNG_END_CH4_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH4\_ST\_CLR** Configures whether to clear LEDC\_EVT\_DUTY\_CHNG\_END\_CH4.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH5\_ST\_CLR** Configures whether to clear LEDC\_EVT\_DUTY\_CHNG\_END\_CH5.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH6\_ST\_CLR** Configures whether to clear LEDC\_EVT\_DUTY\_CHNG\_END\_CH6.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_LEDC\_EVT\_DUTY\_CHNG\_END\_CH7\_ST\_CLR** Configures whether to clear LEDC\_EVT\_DUTY\_CHNG\_END\_CH7.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_LEDC\_EVT\_OVF\_CNT\_PLS\_CHO\_ST\_CLR** Configures whether to clear LEDC\_EVT\_OVF\_CNT\_PLS\_CHO.  
 0: Invalid. No effect  
 1: Clear (WT)

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**Register 12.25. SOC\_ETM\_EVT\_ST1\_CLR\_REG (0x01B4)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH4_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH4.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH5_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH5.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH6_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH6.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_OVF_CNT_PLS_CH7_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_OVF_CNT_PLS_CH7.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |

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**Register 12.25. SOC\_ETM\_EVT\_ST1\_CLR\_REG (0x01B4)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_EVT_TIME_OVF_TIMER0_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_TIME_OVF_TIMER0.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIME_OVF_TIMER1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_TIME_OVF_TIMER1.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIME_OVF_TIMER2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_TIME_OVF_TIMER2.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIME_OVF_TIMER3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_EVT_TIME_OVF_TIMER3.                      |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIMER0_CMP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_EVT_TIMER0_CMP.                           |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIMER1_CMP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_EVT_TIMER1_CMP.                           |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_LEDC_EVT_TIMER2_CMP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_EVT_TIMER2_CMP.                           |            |         |    |       |
| 0: Invalid. No effect                          |            |         |    |       |
| 1: Clear                                       |            |         |    |       |
| (WT)   |            |         |    |       |

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## Register 12.25. SOC\_ETM\_EVT\_ST1\_CLR\_REG (0x01B4)

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|  |            |         |    |       |      |
|--|------------|---------|----|-------|------|
| <b>SOC_ETM_LEDC_EVT_TIMER3_CMP_ST_CLR</b>    | Configures | whether | to | clear |      |
| LEDC_EVT_TIMER3_CMP.                         |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_TGO_EVT_CNT_CMP_TIMER0_ST_CLR</b> | Configures | whether | to | clear |      |
| TGO_EVT_CNT_CMP_TIMER0.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_TGO_EVT_CNT_CMP_TIMER1_ST_CLR</b> | Configures | whether | to | clear |      |
| TGO_EVT_CNT_CMP_TIMER1.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_TG1_EVT_CNT_CMP_TIMER0_ST_CLR</b> | Configures | whether | to | clear |      |
| TG1_EVT_CNT_CMP_TIMER0.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_TG1_EVT_CNT_CMP_TIMER1_ST_CLR</b> | Configures | whether | to | clear |      |
| TG1_EVT_CNT_CMP_TIMER1.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_SYSTIMER_EVT_CNT_CMPO_ST_CLR</b>  | Configures | whether | to | clear | SYS- |
| TIMER_EVT_CNT_CMPO.                          |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_SYSTIMER_EVT_CNT_CMP1_ST_CLR</b>  | Configures | whether | to | clear | SYS- |
| TIMER_EVT_CNT_CMP1.                          |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |

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## Register 12.25. SOC\_ETM\_EVT\_ST1\_CLR\_REG (0x01B4)

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|  |            |         |    |       |      |
|--|------------|---------|----|-------|------|
| <b>SOC_ETM_SYSTIMER_EVT_CNT_CMP2_ST_CLR</b>  | Configures | whether | to | clear | SYS- |
| TIMER_EVT_CNT_CMP2.                          |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_MCPWMO_EVT_TIMER0_STOP_ST_CLR</b> | Configures | whether | to | clear |      |
| MCPWMO_EVT_TIMER0_STOP.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_MCPWMO_EVT_TIMER1_STOP_ST_CLR</b> | Configures | whether | to | clear |      |
| MCPWMO_EVT_TIMER1_STOP.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_MCPWMO_EVT_TIMER2_STOP_ST_CLR</b> | Configures | whether | to | clear |      |
| MCPWMO_EVT_TIMER2_STOP.                      |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_MCPWMO_EVT_TIMER0_TEZ_ST_CLR</b>  | Configures | whether | to | clear |      |
| MCPWMO_EVT_TIMER0_TEZ.                       |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |
| <b>SOC_ETM_MCPWMO_EVT_TIMER1_TEZ_ST_CLR</b>  | Configures | whether | to | clear |      |
| MCPWMO_EVT_TIMER1_TEZ.                       |            |         |    |       |      |
| 0: Invalid. No effect                        |            |         |    |       |      |
| 1: Clear                                     |            |         |    |       |      |
| (WT)   |            |         |    |       |      |

Register 12.26. SOC\_ETM\_EVT\_ST2\_CLR\_REG (0x01BC)

|                                       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SOC_ETM_MCPWM1_EVT_TIMER0_STOP_ST_CLR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP2_TEE2_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP1_TEE2_ST_CLR    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP0_TEE2_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP2_TEE1_ST_CLR    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP1_TEE1_ST_CLR   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP0_TEE1_ST_CLR    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_CAP2_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_CAP1_ST_CLR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_CAPO_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_TZ2_OST_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_TZ1_OST_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_TZ0_OST_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_TZ2_CBC_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_TZ1_CBC_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_TZ0_CBC_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_F2_CLR_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_F1_CLR_ST_CLR     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_F0_CLR_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_F2_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_F1_ST_CLR          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_F0_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP2_TEB_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP1_TEB_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP0_TEB_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP2_TEA_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_OP1_TEA_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_OP0_TEA_ST_CLR    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_TIMER2_TEP_ST_CLR  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_TIMER1_TEP_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM0_EVT_TIMER0_TEP_ST_CLR  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM0_EVT_TIMER2_TEZ_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                                    | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_MCPWM0\_EVT\_TIMER2\_TEZ\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_TIMER2\_TEZ.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER0\_TEP\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_TIMER0\_TEP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER1\_TEP\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_TIMER1\_TEP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM0\_EVT\_TIMER2\_TEP\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_TIMER2\_TEP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM0\_EVT\_OPO\_TEA\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_OPO\_TEA.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM0\_EVT\_OP1\_TEA\_ST\_CLR** Configures whether to clear

MCPWM0\_EVT\_OP1\_TEA.

0: Invalid. No effect

1: Clear

(WT)

**Register 12.26. SOC\_ETM\_EVT\_ST2\_CLR\_REG (0x01BC)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEA\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_OP2\_TEA.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEB\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_OPO\_TEB.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEB\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_OP1\_TEB.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEB\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_OP2\_TEB.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_F0\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_F0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_F1\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_F1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_F2\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_F2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_F0\_CLR\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_F0\_CLR.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

## Register 12.26. SOC\_ETM\_EVT\_ST2\_CLR\_REG (0x01BC)

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_F1\_CLR\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_F1\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_F2\_CLR\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_F2\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ0\_CBC\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ0\_CBC.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ1\_CBC\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ1\_CBC.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ2\_CBC\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ2\_CBC.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ0\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ0\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ1\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ1\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_TZ2\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_TZ2\_OST.

0: Invalid. No effect

1: Clear

(WT)

**Register 12.26. SOC\_ETM\_EVT\_ST2\_CLR\_REG (0x01BC)****Continued from the previous page...****SOC\_ETM\_MCPWMO\_EVT\_CAP0\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_CAP0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_CAP1\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_CAP1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_CAP2\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_CAP2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEE1\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_OPO\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEE1\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_OP1\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEE1\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_OP2\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OPO\_TEE2\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_OPO\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_EVT\_OP1\_TEE2\_ST\_CLR** Configures whether to clear MCPWMO\_EVT\_OP1\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**Continued on the next page...**

**Register 12.26. SOC\_ETM\_EVT\_ST2\_CLR\_REG (0x01BC)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_EVT\_OP2\_TEE2\_ST\_CLR** Configures whether to clear  
MCPWMO\_EVT\_OP2\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_STOP\_ST\_CLR** Configures whether to clear  
MCPWM1\_EVT\_TIMER0\_STOP.

0: Invalid. No effect

1: Clear

(WT)



SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEE1\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEE1\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEE1\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_CAP2\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_CAP1\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_CAP0\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ2\_OST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ1\_OST\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ0\_OST\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ2\_CBC\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ1\_CBC\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TZ0\_CBC\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F2\_CLR\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F1\_CLR\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F0\_CLR\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F2\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F1\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_F0\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEB\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEB\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEA\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OPI\_TEA\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEA\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_TEP\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_TEP\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_TEP\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_TEZ\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_TEZ\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER0\_TEZ\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER2\_STOP\_ST\_CLR  
SOC\_ETM\_MCPWM1\_EVT\_TIMER1\_STOP\_ST\_CLR

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER1_STOP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_EVT_TIMER1_STOP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER2_STOP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_EVT_TIMER2_STOP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER0_TZ_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_EVT_TIMER0_TZ.                      |            |         |    |       |
| 0: Invalid. No effect                      |            |         |    |       |
| 1: Clear                                   |            |         |    |       |
| (WT)                                       |            |         |    |       |

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER1_TEZ_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_EVT_TIMER1_TEZ.                      |            |         |    |       |
| 0: Invalid. No effect                       |            |         |    |       |
| 1: Clear                                    |            |         |    |       |
| (WT)  |            |         |    |       |

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER2_TEZ_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_EVT_TIMER2_TEZ.                      |            |         |    |       |
| 0: Invalid. No effect                       |            |         |    |       |
| 1: Clear                                    |            |         |    |       |
| (WT)  |            |         |    |       |

|   |  |
|---|--|
| <b>SOC_ETM_MCPWM1_EVT_TIMER0_TEP_ST_CLR</b> | Configures whether to clear MCPWM1_EVT_TIMER0_TEP. |
| 0:  | Invalid. No effect                                 |
| 1:  | Clear  |
| ic (AWT)                                    | 700  |
|   | 50000 D4 TPM (D                                    |

## Register 12.27. SOC\_ETM\_EVT\_ST3\_CLR\_REG (0x01C4)

Continued from the previous page...

|   |                                   |         |    |       |
|---|-----------------------------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_EVT_TIMER1_TEP_ST_CLR</b> | Configures MCPWM1_EVT_TIMER1_TEP. | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_TIMER2_TEP_ST_CLR</b> | Configures MCPWM1_EVT_TIMER2_TEP. | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_OPO_TEA_ST_CLR</b>    | Configures MCPWM1_EVT_OPO_TEA.    | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_OP1_TEA_ST_CLR</b>    | Configures MCPWM1_EVT_OP1_TEA.    | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_OP2_TEA_ST_CLR</b>    | Configures MCPWM1_EVT_OP2_TEA.    | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_OPO_TEB_ST_CLR</b>    | Configures MCPWM1_EVT_OPO_TEB.    | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |
| <b>SOC_ETM_MCPWM1_EVT_OP1_TEB_ST_CLR</b>    | Configures MCPWM1_EVT_OP1_TEB.    | whether | to | clear |
| 0: Invalid. No effect                       |                                   |         |    |       |
| 1: Clear (WT)                               |                                   |         |    |       |

Continued on the next page...

**Register 12.27. SOC\_ETM\_EVT\_ST3\_CLR\_REG (0x01C4)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEB\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_OP2\_TEB.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F0\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F1\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F2\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F0\_CLR\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F0\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F1\_CLR\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F1\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_F2\_CLR\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_F2\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TZO\_CBC\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_TZO\_CBC.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.27. SOC\_ETM\_EVT\_ST3\_CLR\_REG (0x01C4)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_EVT\_TZ1\_CBC\_ST\_CLR** Configures whether to clear  
MCPWM1\_EVT\_TZ1\_CBC.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TZ2\_CBC\_ST\_CLR** Configures whether to clear  
MCPWM1\_EVT\_TZ2\_CBC.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TZ0\_OST\_ST\_CLR** Configures whether to clear  
MCPWM1\_EVT\_TZ0\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TZ1\_OST\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_TZ1\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_TZ2\_OST\_ST\_CLR** Configures whether to clear  
MCPWM1\_EVT\_TZ2\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_CAPO\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_CAPO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_CAP1\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_CAP1.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.27. SOC\_ETM\_EVT\_ST3\_CLR\_REG (0x01C4)**

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_EVT\_CAP2\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_CAP2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEE1\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_OPO\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEE1\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_OP1\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEE1\_ST\_CLR** Configures whether to clear MCPWM1\_EVT\_OP2\_TEE1.

0: Invalid. No effect

1: Clear

(WT)

Register 12.28. SOC\_ETM\_EVT\_ST4\_CLR\_REG (0x01CC)

|                                      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SOC_ETM_I2S2_EVT_X_WORDS_SENT_ST_CLR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_X_WORDS_RECEIVED_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_TX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S2_EVT_RX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_X_WORDS_SENT_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_TX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S1_EVT_RX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_X_WORDS_SENT_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_TX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_I2S0_EVT_RX_DONE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_TMPSNSR_EVT_OVER_LIMIT_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR3_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR2_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR1_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_ERR0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE3_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE2_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_REGDMA_EVT_DONE1_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_STARTED0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_STOPPED0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_RESULT_DONE0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_BELOW_THRESH0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_ADC_EVT_EQ_ABOVE_THRESH0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_CONV_THRESH0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP2_TEE2_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OP1_TEE2_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_MCPWM1_EVT_OPO_TEE2_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                                   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                                    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**SOC\_ETM\_MCPWM1\_EVT\_OPO\_TEE2\_ST\_CLR** Configures whether to clear

MCPWM1\_EVT\_OPO\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_OP1\_TEE2\_ST\_CLR** Configures whether to clear

MCPWM1\_EVT\_OP1\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_EVT\_OP2\_TEE2\_ST\_CLR** Configures whether to clear

MCPWM1\_EVT\_OP2\_TEE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_CONV\_CMPLTO\_ST\_CLR** Configures whether to clear

ADC\_EVT\_CONV\_CMPLTO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_EQ\_ABOVE\_THRESH0\_ST\_CLR** Configures whether to clear

ADC\_EVT\_EQ\_ABOVE\_THRESH0.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.28. SOC\_ETM\_EVT\_ST4\_CLR\_REG (0x01CC)**

Continued from the previous page...

**SOC\_ETM\_ADC\_EVT\_EQ\_ABOVE\_THRESH1\_ST\_CLR** Configures whether to clear

ADC\_EVT\_EQ\_ABOVE\_THRESH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_EQ\_BELOW\_THRESH0\_ST\_CLR** Configures whether to clear

ADC\_EVT\_EQ\_BELOW\_THRESH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_EQ\_BELOW\_THRESH1\_ST\_CLR** Configures whether to clear

ADC\_EVT\_EQ\_BELOW\_THRESH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_RESULT\_DONE0\_ST\_CLR** Configures whether to clear

ADC\_EVT\_RESULT\_DONE0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_STOPPED0\_ST\_CLR** Configures whether to clear ADC\_EVT\_STOPPED0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_EVT\_STARTED0\_ST\_CLR** Configures whether to clear ADC\_EVT\_STARTED0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_DONE0\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_DONE0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_DONE1\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_DONE1.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.28. SOC\_ETM\_EVT\_ST4\_CLR\_REG (0x01CC)**

Continued from the previous page...

**SOC\_ETM\_REGDMA\_EVT\_DONE2\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_DONE2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_DONE3\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_DONE3.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_ERR0\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_ERR0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_ERR1\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_ERR1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_ERR2\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_ERR2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_EVT\_ERR3\_ST\_CLR** Configures whether to clear REGDMA\_EVT\_ERR3.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_TMPSNSR\_EVT\_OVER\_LIMIT\_ST\_CLR** Configures whether to clear TMP-SNSR\_EVT\_OVER\_LIMIT.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...



**Register 12.28. SOC\_ETM\_EVT\_ST4\_CLR\_REG (0x01CC)**

Continued from the previous page...

**SOC\_ETM\_I2SO\_EVT\_RX\_DONE\_ST\_CLR** Configures whether to clear I2SO\_EVT\_RX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_EVT\_TX\_DONE\_ST\_CLR** Configures whether to clear I2SO\_EVT\_TX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_EVT\_X\_WORDS\_RECEIVED\_ST\_CLR** Configures whether to clear I2SO\_EVT\_X\_WORDS\_RECEIVED.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_EVT\_X\_WORDS\_SENT\_ST\_CLR** Configures whether to clear I2SO\_EVT\_X\_WORDS\_SENT.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_EVT\_RX\_DONE\_ST\_CLR** Configures whether to clear I2S1\_EVT\_RX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_EVT\_TX\_DONE\_ST\_CLR** Configures whether to clear I2S1\_EVT\_TX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_EVT\_X\_WORDS\_RECEIVED\_ST\_CLR** Configures whether to clear I2S1\_EVT\_X\_WORDS\_RECEIVED.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.28. SOC\_ETM\_EVT\_ST4\_CLR\_REG (0x01CC)**

Continued from the previous page...

**SOC\_ETM\_I2S1\_EVT\_X\_WORDS\_SENT\_ST\_CLR** Configures whether to clear I2S1\_EVT\_X\_WORDS\_SENT.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_EVT\_RX\_DONE\_ST\_CLR** Configures whether to clear I2S2\_EVT\_RX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_EVT\_TX\_DONE\_ST\_CLR** Configures whether to clear I2S2\_EVT\_TX\_DONE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_EVT\_X\_WORDS\_RECEIVED\_ST\_CLR** Configures whether to clear I2S2\_EVT\_X\_WORDS\_RECEIVED.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_EVT\_X\_WORDS\_SENT\_ST\_CLR** Configures whether to clear I2S2\_EVT\_X\_WORDS\_SENT.

0: Invalid. No effect

1: Clear

(WT)

**Register 12.29. SOC\_ETM\_EVT\_ST5\_CLR\_REG (0x01D4)**

|   |  |  |  |   |   |   |   |   |   |  |  |   |  |  |   |   |   |  |  |  |                                    |                                    |                            |                             |                                   |                             |                                 |   |   |   |   |       |
|---|--|--|--|---|---|---|---|---|---|--|--|---|--|--|---|---|---|--|--|--|------------------------------------|------------------------------------|----------------------------|-----------------------------|-----------------------------------|-----------------------------|---------------------------------|---|---|---|---|-------|
| SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_EMPTY_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_TOTAL_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_TOTAL_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_TOTAL_EOF_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_EOF_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_DONE_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_DONE_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_FULL_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_FULL_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CH1_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH1_ST_CLR | SOC_ETM_RTC_EVT_IN_DONE_CH0_ST_CLR | SOC_ETM_RTC_EVT_IN_DONE_CH2_ST_CLR | SOC_ETM_RTC_EVT_OVF_ST_CLR | SOC_ETM_ULP_EVT_TICK_ST_CLR | SOC_ETM_ULP_EVT_START_INTR_ST_CLR | SOC_ETM_ULP_EVT_HALT_ST_CLR | SOC_ETM_ULP_EVT_ERR_INTR_ST_CLR |   |   |   |   |       |
| 31  | 30   | 29   | 28   | 27  | 26  | 25  | 24                                      | 23                                      | 22                                      | 21                                       | 20                                       | 19                                      | 18   | 17   | 16  | 15  | 14  | 13   | 12   | 11   | 10                                 | 9                                  | 8                          | 7                           | 6                                 | 5                           | 4                               | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0   | 0   | 0   | 0                                       | 0                                       | 0                                       | 0  | 0  | 0                                       | 0  | 0  | 0   | 0   | 0   | 0  | 0  | 0  | 0                                  | 0                                  | 0                          | 0                           | 0                                 | 0                           | 0                               | 0 | 0 | 0 | 0 | Reset |

**SOC\_ETM\_ULP\_EVT\_ERR\_INTR\_ST\_CLR** Configures whether to clear ULP\_EVT\_ERR\_INTR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ULP\_EVT\_HALT\_ST\_CLR** Configures whether to clear ULP\_EVT\_HALT.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ULP\_EVT\_START\_INTR\_ST\_CLR** Configures whether to clear ULP\_EVT\_START\_INTR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_EVT\_TICK\_ST\_CLR** Configures whether to clear RTC\_EVT\_TICK.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_EVT\_OVF\_ST\_CLR** Configures whether to clear RTC\_EVT\_OVF.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_EVT\_CMP\_ST\_CLR** Configures whether to clear RTC\_EVT\_CMP.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.29. SOC\_ETM\_EVT\_ST5\_CLR\_REG (0x01D4)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AHB_EVT_IN_DONE_CHO_ST_CLR</b>       | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_DONE_CHO.                            |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_DONE_CH1_ST_CLR</b>       | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_DONE_CH1.                            |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_DONE_CH2_ST_CLR</b>       | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_DONE_CH2.                            |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CHO_ST_CLR</b>    | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_SUC_EOF_CHO.                         |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH1_ST_CLR</b>    | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_SUC_EOF_CH1.                         |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_SUC_EOF_CH2_ST_CLR</b>    | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_SUC_EOF_CH2.                         |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_EVT_IN_FIFO_EMPTY_CHO_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AHB_EVT_IN_FIFO_EMPTY_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                                |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |

Continued on the next page...

**Register 12.29. SOC\_ETM\_EVT\_ST5\_CLR\_REG (0x01D4)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_IN\_FIFO\_EMPTY\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CHO\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_IN\_FIFO\_FULL\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CHO\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_DONE\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_DONE\_CH1.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.29. SOC\_ETM\_EVT\_ST5\_CLR\_REG (0x01D4)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_DONE\_CH2\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_DONE\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CHO\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_EOF\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CH1\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_EOF\_CH2\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CHO\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH1\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH2\_ST\_CLR** Configures whether to clear

GDMA\_AHB\_EVT\_OUT\_TOTAL\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.29. SOC\_ETM\_EVT\_ST5\_CLR\_REG (0x01D4)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CHO\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_FIFO\_EMPTY\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CHO\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**Register 12.30. SOC\_ETM\_EVT\_ST6\_CLR\_REG (0x01DC)**

|   |                                      |                                      |                                     |   |  |  |  |   |   |   |   |   |   |  |  |  |  |   |   |  |  |  |   |   |   |   |   |   |   |   |       |
|---|--------------------------------------|--------------------------------------|-------------------------------------|---|--|--|--|---|---|---|---|---|---|--|--|--|--|---|---|--|--|--|---|---|---|---|---|---|---|---|-------|
| SOC_ETM_DMA2D_EVT_IN_SUC_EOF_CHO_ST_CLR | SOC_ETM_DMA2D_EVT_IN_DONE_CH1_ST_CLR | SOC_ETM_DMA2D_EVT_IN_DONE_CH0_ST_CLR | SOC_ETM_PMU_EVT_SLEEP_WEEKUP_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_FULL_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_FIFO_EMPTY_CH0_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_TOTAL_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_EMPTY_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_FIFO_EMPTY_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH0_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH2_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_SUC_EOF_CH1_ST_CLR | SOC_ETM_GDMA_AXI_EVT_IN_DONE_CH0_ST_CLR | SOC_ETM_GDMA_AHB_EVT_OUT_FIFO_FULL_CH2_ST_CLR |   |   |   |   |   |   |       |
| 31                                      | 30                                   | 29                                   | 28                                  | 27  | 26   | 25   | 24   | 23  | 22  | 21  | 20                                      | 19                                      | 18                                      | 17                                       | 16                                       | 15   | 14   | 13  | 12  | 11   | 10   | 9  | 8                                       | 7   | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0                                       | 0                                    | 0                                    | 0                                   | 0   | 0  | 0  | 0  | 0   | 0   | 0   | 0                                       | 0                                       | 0                                       | 0  | 0  | 0  | 0  | 0   | 0   | 0  | 0  | 0  | 0                                       | 0   | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

Reset

**SOC\_ETM\_GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CH2\_ST\_CLR** Configures whether to clear GDMA\_AHB\_EVT\_OUT\_FIFO\_FULL\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_DONE\_CH0\_ST\_CLR** Configures whether to clear GDMA\_AXI\_EVT\_IN\_DONE\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_DONE\_CH1\_ST\_CLR** Configures whether to clear GDMA\_AXI\_EVT\_IN\_DONE\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_DONE\_CH2\_ST\_CLR** Configures whether to clear GDMA\_AXI\_EVT\_IN\_DONE\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CHO\_ST\_CLR** Configures whether to clear GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CHO.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...



**Register 12.30. SOC\_ETM\_EVT\_ST6\_CLR\_REG (0x01DC)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH1\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH2\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_SUC\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH0\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH1\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH2\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_FIFO\_EMPTY\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH0\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH1\_ST\_CLR** Configures whether to clear

GDMA\_AXI\_EVT\_IN\_FIFO\_FULL\_CH1.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.30. SOC\_ETM\_EVT\_ST6\_CLR\_REG (0x01DC)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AXI_EVT_IN_FIFO_FULL_CH2_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AXI_EVT_IN_FIFO_FULL_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH0_ST_CLR</b>     | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_DONE_CH0.                          |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH1_ST_CLR</b>     | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_DONE_CH1.                          |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_DONE_CH2_ST_CLR</b>     | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_DONE_CH2.                          |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH0_ST_CLR</b>      | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_EOF_CH0.                           |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH1_ST_CLR</b>      | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_EOF_CH1.                           |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_EVT_OUT_EOF_CH2_ST_CLR</b>      | Configures | whether | to | clear |
| GDMA_AXI_EVT_OUT_EOF_CH2.                           |            |         |    |       |
| 0: Invalid. No effect                               |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.30. SOC\_ETM\_EVT\_ST6\_CLR\_REG (0x01DC)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH0\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_TOTAL\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH0\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_EMPTY\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH0\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH0.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.30. SOC\_ETM\_EVT\_ST6\_CLR\_REG (0x01DC)**

Continued from the previous page...

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH1\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH2\_ST\_CLR** Configures whether to clear  
GDMA\_AXI\_EVT\_OUT\_FIFO\_FULL\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_PMU\_EVT\_SLEEP\_WEEKUP\_ST\_CLR** Configures whether to clear  
PMU\_EVT\_SLEEP\_WEEKUP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_IN\_DONE\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_IN\_DONE\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_IN\_DONE\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_IN\_DONE\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_IN\_SUC\_EOF\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_IN\_SUC\_EOF\_CHO.

0: Invalid. No effect

1: Clear

(WT)

## Register 12.31. SOC\_ETM\_EVT\_ST7\_CLR\_REG (0x01E4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   | SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH2_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH1_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_TOTAL_EOF_CH0_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH2_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH1_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_EOF_CH0_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_DONE_CH2_ST_CLR<br>SOC_ETM_DMA2D_EVT_OUT_DONE_CH1_ST_CLR<br>SOC_ETM_DMA2D_EVT_IN_SUC_EOF_CH1_ST_CLR |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10 | 9 | 8   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 |   |   |   |   |   |   |   |   |   |       |

**SOC\_ETM\_DMA2D\_EVT\_IN\_SUC\_EOF\_CH1\_ST\_CLR** Configures whether to clear DMA2D\_EVT\_IN\_SUC\_EOF\_CH1.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH0\_ST\_CLR** Configures whether to clear DMA2D\_EVT\_OUT\_DONE\_CH0.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH1\_ST\_CLR** Configures whether to clear DMA2D\_EVT\_OUT\_DONE\_CH1.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_DONE\_CH2\_ST\_CLR** Configures whether to clear DMA2D\_EVT\_OUT\_DONE\_CH2.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH0\_ST\_CLR** Configures whether to clear DMA2D\_EVT\_OUT\_EOF\_CH0.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

Continued on the next page...

**Register 12.31. SOC\_ETM\_EVT\_ST7\_CLR\_REG (0x01E4)**

Continued from the previous page...

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_OUT\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_EOF\_CH2\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_OUT\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH2\_ST\_CLR** Configures whether to clear  
DMA2D\_EVT\_OUT\_TOTAL\_EOF\_CH2.

0: Invalid. No effect

1: Clear

(WT)

Register 12.32. SOC\_ETM\_TASK\_STO\_CLR\_REG (0x01EC)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |  |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--|-------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH3_ST_CLR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH2_ST_CLR |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH1_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_TASK_TIMER3_RES_UPDATE_CH0_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_TASK_TIMER2_RES_UPDATE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_LEDC_TASK_TIMER1_RES_UPDATE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH7_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH6_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH5_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH4_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH3_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH2_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH1_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH0_TOGGLE_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH7_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH6_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH5_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH4_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH3_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH2_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH1_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH0_CLEAR_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH7_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH6_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH5_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH4_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH3_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH2_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH1_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SOC_ETM_GPIO_TASK_CH0_SET_ST_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0  | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**SOC\_ETM\_GPIO\_TASK\_CH0\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH0\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH1\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH1\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH2\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH2\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH3\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH3\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH4\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH4\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH5\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH5\_SET.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.32. SOC\_ETM\_TASK\_STO\_CLR\_REG (0x01EC)****Continued from the previous page...****SOC\_ETM\_GPIO\_TASK\_CH6\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH6\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH7\_SET\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH7\_SET.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CHO\_CLEAR\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CHO\_CLEAR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH1\_CLEAR\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH1\_CLEAR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH2\_CLEAR\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH2\_CLEAR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH3\_CLEAR\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH3\_CLEAR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GPIO\_TASK\_CH4\_CLEAR\_ST\_CLR** Configures whether to clear GPIO\_TASK\_CH4\_CLEAR.

0: Invalid. No effect

1: Clear

(WT)

**Continued on the next page...**



## Register 12.32. SOC\_ETM\_TASK\_STO\_CLR\_REG (0x01EC)

Continued from the previous page...

|  |  |         |    |       |
|--|--|---------|----|-------|
| <b>SOC_ETM_GPIO_TASK_CH5_CLEAR_ST_CLR</b>  | Configures                                       | whether | to | clear |
| GPIO_TASK_CH5_CLEAR.                       |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH6_CLEAR_ST_CLR</b>  | Configures                                       | whether | to | clear |
| GPIO_TASK_CH6_CLEAR.                       |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH7_CLEAR_ST_CLR</b>  | Configures whether to clear GPIO_TASK_CH7_CLEAR. |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CHO_TOGGLE_ST_CLR</b> | Configures                                       | whether | to | clear |
| GPIO_TASK_CHO_TOGGLE.                      |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH1_TOGGLE_ST_CLR</b> | Configures                                       | whether | to | clear |
| GPIO_TASK_CH1_TOGGLE.                      |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH2_TOGGLE_ST_CLR</b> | Configures                                       | whether | to | clear |
| GPIO_TASK_CH2_TOGGLE.                      |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH3_TOGGLE_ST_CLR</b> | Configures                                       | whether | to | clear |
| GPIO_TASK_CH3_TOGGLE.                      |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH4_TOGGLE_ST_CLR</b> | Configures                                       | whether | to | clear |
| GPIO_TASK_CH4_TOGGLE.                      |  |         |    |       |
| 0: Invalid. No effect                      |  |         |    |       |
| 1: Clear                                   |  |         |    |       |
| (WT)                                       |  |         |    |       |

**Register 12.32. SOC\_ETM\_TASK\_STO\_CLR\_REG (0x01EC)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GPIO_TASK_CH5_TOGGLE_ST_CLR</b>        | Configures | whether | to | clear |
| GPIO_TASK_CH5_TOGGLE.                             |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH6_TOGGLE_ST_CLR</b>        | Configures | whether | to | clear |
| GPIO_TASK_CH6_TOGGLE.                             |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GPIO_TASK_CH7_TOGGLE_ST_CLR</b>        | Configures | whether | to | clear |
| GPIO_TASK_CH7_TOGGLE.                             |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER0_RES_UPDATE_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER0_RES_UPDATE.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER1_RES_UPDATE_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER1_RES_UPDATE.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER2_RES_UPDATE_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER2_RES_UPDATE.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER3_RES_UPDATE_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER3_RES_UPDATE.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.32. SOC\_ETM\_TASK\_STO\_CLR\_REG (0x01EC)**

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CHO\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH1\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH2\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH3\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH3.

0: Invalid. No effect

1: Clear

(WT)

Register 12.33. SOC\_ETM\_TASK\_ST1\_CLR\_REG (0x01F4)

|  |  |  |  |                                     |                                     |                                     |                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |                                     |                                     |                                     |                                     |  |  |  |   |   |   |       |
|--|--|--|--|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|--|--|--|---|---|---|-------|
| SOC_ETM_LEDC_TASK_TIMER3_RESUME_ST_CLR | SOC_ETM_LEDC_TASK_TIMER2_RESUME_ST_CLR | SOC_ETM_LEDC_TASK_TIMER1_RESUME_ST_CLR | SOC_ETM_LEDC_TASK_TIMER0_RESUME_ST_CLR | SOC_ETM_LEDC_TASK_TIMER3_RST_ST_CLR | SOC_ETM_LEDC_TASK_TIMER2_RST_ST_CLR | SOC_ETM_LEDC_TASK_TIMER1_RST_ST_CLR | SOC_ETM_LEDC_TASK_TIMER0_RST_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH7_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH6_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH5_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH4_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH3_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH2_ST_CLR | SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH1_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH7_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH6_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH5_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH4_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH3_ST_CLR | SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH2_ST_CLR | SOC_ETM_LEDC_TASK_TIMER3_CAP_ST_CLR | SOC_ETM_LEDC_TASK_TIMER2_CAP_ST_CLR | SOC_ETM_LEDC_TASK_TIMER1_CAP_ST_CLR | SOC_ETM_LEDC_TASK_TIMER0_CAP_ST_CLR | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH7_ST_CLR | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH6_ST_CLR | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH5_ST_CLR | SOC_ETM_LEDC_TASK_DUTY_SCALE_UPDATE_CH4_ST_ST_CLR |   |   |       |
| 31                                     | 30                                     | 29                                     | 28                                     | 27                                  | 26                                  | 25                                  | 24                                  | 23                                       | 22                                       | 21                                       | 20                                       | 19                                       | 18                                       | 17                                       | 16                                       | 15                                       | 14                                       | 13                                       | 12                                       | 11                                       | 10                                  | 9                                   | 8                                   | 7                                   | 6  | 5  | 4  | 3   | 2 | 1 | 0     |
| 0                                      | 0                                      | 0                                      | 0                                      | 0                                   | 0                                   | 0                                   | 0                                   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0                                   | 0                                   | 0                                   | 0                                   | 0  | 0  | 0  | 0   | 0 | 0 | Reset |

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH4\_ST\_CLR** Configures whether to clear LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH4.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH5\_ST\_CLR** Configures whether to clear LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH5.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH6\_ST\_CLR** Configures whether to clear LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH6.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH7\_ST\_CLR** Configures whether to clear LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH7.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_CAP\_ST\_CLR** Configures whether to clear LEDC\_TASK\_TIMER0\_CAP.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.33. SOC\_ETM\_TASK\_ST1\_CLR\_REG (0x01F4)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_TIMER1_CAP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_TASK_TIMER1_CAP.                           |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER2_CAP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_TASK_TIMER2_CAP.                           |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER3_CAP_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_TASK_TIMER3_CAP.                           |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CHO_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_SIG_OUT_DIS_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_SIG_OUT_DIS_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_SIG_OUT_DIS_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_SIG_OUT_DIS_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.33. SOC\_ETM\_TASK\_ST1\_CLR\_REG (0x01F4)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH4_ST_CLR</b><br>LEDC_TASK_SIG_OUT_DIS_CH4.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH5_ST_CLR</b><br>LEDC_TASK_SIG_OUT_DIS_CH5.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH6_ST_CLR</b><br>LEDC_TASK_SIG_OUT_DIS_CH6.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_SIG_OUT_DIS_CH7_ST_CLR</b><br>LEDC_TASK_SIG_OUT_DIS_CH7.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH0_ST_CLR</b><br>LEDC_TASK_OVF_CNT_RST_CH0.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH1_ST_CLR</b><br>LEDC_TASK_OVF_CNT_RST_CH1.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH2_ST_CLR</b><br>LEDC_TASK_OVF_CNT_RST_CH2.<br>0: Invalid. No effect<br>1: Clear<br>(WT) | Configures | whether | to | clear |

Continued on the next page...

**Register 12.33. SOC\_ETM\_TASK\_ST1\_CLR\_REG (0x01F4)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_OVF_CNT_RST_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH4_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_OVF_CNT_RST_CH4.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH5_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_OVF_CNT_RST_CH5.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH6_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_OVF_CNT_RST_CH6.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_OVF_CNT_RST_CH7_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_OVF_CNT_RST_CH7.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER0_RST_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_TASK_TIMER0_RST.                           |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER1_RST_ST_CLR</b>      | Configures | whether | to | clear |
| LEDC_TASK_TIMER1_RST.                           |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

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## Register 12.33. SOC\_ETM\_TASK\_ST1\_CLR\_REG (0x01F4)

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_TIMER2_RST_ST_CLR</b>    | Configures | whether | to | clear |
| LEDC_TASK_TIMER2_RST.                         |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER3_RST_ST_CLR</b>    | Configures | whether | to | clear |
| LEDC_TASK_TIMER3_RST.                         |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER0_RESUME_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER0_RESUME.                      |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER1_RESUME_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER1_RESUME.                      |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER2_RESUME_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER2_RESUME.                      |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_TIMER3_RESUME_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_TIMER3_RESUME.                      |            |         |    |       |
| 0: Invalid. No effect                         |            |         |    |       |
| 1: Clear                                      |            |         |    |       |
| (WT)  |            |         |    |       |



Register 12.34. SOC\_ETM\_TASK\_ST2\_CLR\_REG (0x01FC)

| Soc  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| Soc_ETM_TGO_TASK_CNT_RELOAD_TIMER0_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_TGO_TASK_CNT_STOP_TIMER0_ST_CLR        |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_TGO_TASK_CNT_ALARM_START_TIMER0_ST_CLR |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH7_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH6_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH5_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH4_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH3_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH2_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESUME_CH1_ST_CLR      |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH0_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH7_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH6_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH5_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH4_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH3_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH2_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_PAUSE_CH1_ST_CLR       |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH0_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH7_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH6_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH5_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH4_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_GAMMA_RESTART_CH3_ST_CLR     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_TIMER3_PAUSE_ST_CLR          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_TIMER2_PAUSE_ST_CLR          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_TIMER1_PAUSE_ST_CLR          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| Soc_ETM_LEDC_TASK_TIMER0_PAUSE_ST_CLR          |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |

**SOC\_ETM\_LEDC\_TASK\_TIMER0\_PAUSE\_ST\_CLR** Configures whether to clear LEDC\_TASK\_TIMER0\_PAUSE.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_LEDC\_TASK\_TIMER1\_PAUSE\_ST\_CLR** Configures whether to clear LEDC\_TASK\_TIMER1\_PAUSE.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_LEDC\_TASK\_TIMER2\_PAUSE\_ST\_CLR** Configures whether to clear LEDC\_TASK\_TIMER2\_PAUSE.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_LEDC\_TASK\_TIMER3\_PAUSE\_ST\_CLR** Configures whether to clear LEDC\_TASK\_TIMER3\_PAUSE.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESTART\_CHO\_ST\_CLR** Configures whether to clear LEDC\_TASK\_GAMMA\_RESTART\_CHO.  
 0: Invalid. No effect  
 1: Clear  
 (WT)

Continued on the next page...

**Register 12.34. SOC\_ETM\_TASK\_ST2\_CLR\_REG (0x01FC)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH4_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH4.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH5_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH5.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH6_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH6.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESTART_CH7_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESTART_CH7.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.34. SOC\_ETM\_TASK\_ST2\_CLR\_REG (0x01FC)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CHO_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH1_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH2_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH3_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH3.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH4_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH4.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH5_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH5.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_PAUSE_CH6_ST_CLR</b> | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_PAUSE_CH6.                      |            |         |    |       |
| 0: Invalid. No effect                           |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.34. SOC\_ETM\_TASK\_ST2\_CLR\_REG (0x01FC)**

Continued from the previous page...

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_PAUSE\_CH7\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_PAUSE\_CH7.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH0\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH1\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH2\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH3\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH3.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH4\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH4.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_LEDC\_TASK\_GAMMA\_RESUME\_CH5\_ST\_CLR** Configures whether to clear  
LEDC\_TASK\_GAMMA\_RESUME\_CH5.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.34. SOC\_ETM\_TASK\_ST2\_CLR\_REG (0x01FC)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH6_ST_CLR</b>  | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESUME_CH6.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_LEDC_TASK_GAMMA_RESUME_CH7_ST_CLR</b>  | Configures | whether | to | clear |
| LEDC_TASK_GAMMA_RESUME_CH7.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TGO_TASK_CNT_START_TIMER0_ST_CLR</b>   | Configures | whether | to | clear |
| TGO_TASK_CNT_START_TIMER0.                        |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TGO_TASK_ALARM_START_TIMER0_ST_CLR</b> | Configures | whether | to | clear |
| TGO_TASK_ALARM_START_TIMER0.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TGO_TASK_CNT_STOP_TIMER0_ST_CLR</b>    | Configures | whether | to | clear |
| TGO_TASK_CNT_STOP_TIMER0.                         |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TGO_TASK_CNT_RELOAD_TIMER0_ST_CLR</b>  | Configures | whether | to | clear |
| TGO_TASK_CNT_RELOAD_TIMER0.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

[illegible]

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_TGO_TASK_CNT_RELOAD_TIMER1_ST_CLR</b> | Configures | whether | to | clear |
| TGO_TASK_CNT_RELOAD_TIMER1.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |

PRELIMINARY

## Register 12.35. SOC\_ETM\_TASK\_ST3\_CLR\_REG (0x0204)

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_TGO_TASK_CNT_CAP_TIMER1_ST_CLR</b>     | Configures | whether | to | clear |
| TGO_TASK_CNT_CAP_TIMER1.                          |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_START_TIMER0_ST_CLR</b>   | Configures | whether | to | clear |
| TG1_TASK_CNT_START_TIMER0.                        |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_ALARM_START_TIMER0_ST_CLR</b> | Configures | whether | to | clear |
| TG1_TASK_ALARM_START_TIMER0.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_STOP_TIMER0_ST_CLR</b>    | Configures | whether | to | clear |
| TG1_TASK_CNT_STOP_TIMER0.                         |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_RELOAD_TIMER0_ST_CLR</b>  | Configures | whether | to | clear |
| TG1_TASK_CNT_RELOAD_TIMER0.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_CAP_TIMER0_ST_CLR</b>     | Configures | whether | to | clear |
| TG1_TASK_CNT_CAP_TIMER0.                          |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_START_TIMER1_ST_CLR</b>   | Configures | whether | to | clear |
| TG1_TASK_CNT_START_TIMER1.                        |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...

**Register 12.35. SOC\_ETM\_TASK\_ST3\_CLR\_REG (0x0204)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_TG1_TASK_ALARM_START_TIMER1_ST_CLR</b> | Configures | whether | to | clear |
| TG1_TASK_ALARM_START_TIMER1.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_STOP_TIMER1_ST_CLR</b>    | Configures | whether | to | clear |
| TG1_TASK_CNT_STOP_TIMER1.                         |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_RELOAD_TIMER1_ST_CLR</b>  | Configures | whether | to | clear |
| TG1_TASK_CNT_RELOAD_TIMER1.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_TG1_TASK_CNT_CAP_TIMER1_ST_CLR</b>     | Configures | whether | to | clear |
| TG1_TASK_CNT_CAP_TIMER1.                          |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_CMPRO_A_UP_ST_CLR</b>      | Configures | whether | to | clear |
| MCPWMO_TASK_CMPRO_A_UP.                           |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_CMPR1_A_UP_ST_CLR</b>      | Configures | whether | to | clear |
| MCPWMO_TASK_CMPR1_A_UP.                           |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_CMPR2_A_UP_ST_CLR</b>      | Configures | whether | to | clear |
| MCPWMO_TASK_CMPR2_A_UP.                           |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

Continued on the next page...



**Register 12.35. SOC\_ETM\_TASK\_ST3\_CLR\_REG (0x0204)**

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_MCPWMO_TASK_CMPRO_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_CMPRO_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_CMPR1_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_CMPR1_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_CMPR2_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_CMPR2_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_GEN_STOP_ST_CLR</b>   | Configures | whether | to | clear |
| MCPWMO_TASK_GEN_STOP.                        |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_TIMER0_SYN_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_TIMER0_SYN.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_TIMER1_SYN_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_TIMER1_SYN.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWMO_TASK_TIMER2_SYN_ST_CLR</b> | Configures | whether | to | clear |
| MCPWMO_TASK_TIMER2_SYN.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |

Continued on the next page...

**Register 12.35. SOC\_ETM\_TASK\_ST3\_CLR\_REG (0x0204)**

Continued from the previous page...

**SOC\_ETM\_MCPWMO\_TASK\_TIMER0\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TIMER0\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER1\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TIMER1\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_TASK\_TIMER2\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TIMER2\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_TASK\_TZO\_OST\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TZO\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_TASK\_TZ1\_OST\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TZ1\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWMO\_TASK\_TZ2\_OST\_ST\_CLR** Configures whether to clear  
MCPWMO\_TASK\_TZ2\_OST.

0: Invalid. No effect

1: Clear

(WT)

Register 12.36. SOC\_ETM\_TASK\_ST4\_CLR\_REG (0x020C)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SOC_ETM_ADC_TASK_STOPO_ST_CLR               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ADC_TASK_STARTO_ST_CLR              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_ADC_TASK_SAMPLE0_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CAP2_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CAP1_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CAP0_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CLR2_OST_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CLR1_OST_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CLR0_OST_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TZ2_OST_ST_CLR          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TZ1_OST_ST_CLR          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TZ0_OST_ST_CLR          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER2_PERIOD_UP_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER1_PERIOD_UP_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER0_PERIOD_UP_ST_CLR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER2_SYN_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER1_SYN_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_TIMER0_SYN_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_GEN_STOP_ST_CLR         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CMPR2_B_UP_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CMPR1_B_UP_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CMPR2_A_UP_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWM1_TASK_CMPR1_A_UP_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_TASK_CMPR0_A_UP_ST_CLR       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_TASK_CAP2_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_TASK_CAP1_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| SOC_ETM_MCPWMO_TASK_CAP0_ST_CLR             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SOC\_ETM\_MCPWMO\_TASK\_CLR0\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CLR0\_OST.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_MCPWMO\_TASK\_CLR1\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CLR1\_OST.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_MCPWMO\_TASK\_CLR2\_OST\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CLR2\_OST.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_MCPWMO\_TASK\_CAPO\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CAPO.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_MCPWMO\_TASK\_CAP1\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CAP1.  
 0: Invalid. No effect  
 1: Clear (WT)

**SOC\_ETM\_MCPWMO\_TASK\_CAP2\_ST\_CLR** Configures whether to clear MCPWMO\_TASK\_CAP2.  
 0: Invalid. No effect  
 1: Clear (WT)

## Register 12.36. SOC\_ETM\_TASK\_ST4\_CLR\_REG (0x020C)

Continued from the previous page...

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_MCPWM1_TASK_CMPRO_A_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPRO_A_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_CMPR1_A_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPR1_A_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_CMPR2_A_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPR2_A_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_CMPRO_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPRO_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_CMPR1_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPR1_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_CMPR2_B_UP_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_CMPR2_B_UP.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_GEN_STOP_ST_CLR</b>   | Configures | whether | to | clear |
| MCPWM1_TASK_GEN_STOP.                        |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |
| <b>SOC_ETM_MCPWM1_TASK_TIMER0_SYN_ST_CLR</b> | Configures | whether | to | clear |
| MCPWM1_TASK_TIMER0_SYN.                      |            |         |    |       |
| 0: Invalid. No effect                        |            |         |    |       |
| 1: Clear                                     |            |         |    |       |
| (WT)   |            |         |    |       |

## Register 12.36. SOC\_ETM\_TASK\_ST4\_CLR\_REG (0x020C)

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_TASK\_TIMER1\_SYN\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TIMER1\_SYN.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER2\_SYN\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TIMER2\_SYN.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER0\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TIMER0\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER1\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TIMER1\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TIMER2\_PERIOD\_UP\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TIMER2\_PERIOD\_UP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TZO\_OST\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TZO\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TZ1\_OST\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TZ1\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_TZ2\_OST\_ST\_CLR** Configures whether to clear  
MCPWM1\_TASK\_TZ2\_OST.

0: Invalid. No effect

1: Clear

(WT)

## Register 12.36. SOC\_ETM\_TASK\_ST4\_CLR\_REG (0x020C)

Continued from the previous page...

**SOC\_ETM\_MCPWM1\_TASK\_CLRO\_OST\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CLRO\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_CLR1\_OST\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CLR1\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_CLR2\_OST\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CLR2\_OST.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_CAPO\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CAPO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_CAP1\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CAP1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_MCPWM1\_TASK\_CAP2\_ST\_CLR** Configures whether to clear MCPWM1\_TASK\_CAP2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_TASK\_SAMPLEO\_ST\_CLR** Configures whether to clear ADC\_TASK\_SAMPLEO.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.36. SOC\_ETM\_TASK\_ST4\_CLR\_REG (0x020C)**

Continued from the previous page...

**SOC\_ETM\_ADC\_TASK\_STARTO\_ST\_CLR** Configures whether to clear ADC\_TASK\_STARTO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ADC\_TASK\_STOPO\_ST\_CLR** Configures whether to clear ADC\_TASK\_STOPO.

0: Invalid. No effect

1: Clear

(WT)

Register 12.37. SOC\_ETM\_TASK\_ST5\_CLR\_REG (0x0214)

|   |  |  |  |   |   |                                    |                              |                               |                                 |                                     |                                  |                                  |                                   |                                  |                                  |                                   |                                  |                                  |                                      |                                     |   |                                   |                                   |                                   |                                   |   |   |   |   |   |       |
|---|--|--|--|---|---|------------------------------------|------------------------------|-------------------------------|---------------------------------|-------------------------------------|----------------------------------|----------------------------------|-----------------------------------|----------------------------------|----------------------------------|-----------------------------------|----------------------------------|----------------------------------|--------------------------------------|-------------------------------------|---|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|---|---|---|---|---|-------|
| SOC_ETM_GDMA_AXI_TASK_IN_START_CH1_ST_CLR | SOC_ETM_GDMA_AXI_TASK_OUT_START_CH0_ST_CLR | SOC_ETM_GDMA_AHB_TASK_OUT_START_CH2_ST_CLR | SOC_ETM_GDMA_AHB_TASK_OUT_START_CH1_ST_CLR | SOC_ETM_GDMA_AHB_TASK_IN_START_CH0_ST_CLR | SOC_ETM_GDMA_AHB_TASK_IN_START_CH2_ST_CLR | SOC_ETM_RTC_TASK_TRIGGERFLW_ST_CLR | SOC_ETM_RTC_TASK_STOP_ST_CLR | SOC_ETM_ULP_TASK_START_ST_CLR | SOC_ETM_ULP_TASK_INT_CPU_ST_CLR | SOC_ETM_I2S2_TASK_WAKEUP_CPU_ST_CLR | SOC_ETM_I2S2_TASK_STOP_TX_ST_CLR | SOC_ETM_I2S2_TASK_STOP_RX_ST_CLR | SOC_ETM_I2S1_TASK_START_TX_ST_CLR | SOC_ETM_I2S1_TASK_STOP_RX_ST_CLR | SOC_ETM_I2S1_TASK_STOP_TX_ST_CLR | SOC_ETM_I2S0_TASK_START_TX_ST_CLR | SOC_ETM_I2S0_TASK_STOP_RX_ST_CLR | SOC_ETM_I2S0_TASK_STOP_TX_ST_CLR | SOC_ETM_TMPSNSR_TASK_START_TX_ST_CLR | SOC_ETM_TMPSNSR_TASK_STOP_RX_ST_CLR | SOC_ETM_REGDMA_TASK_START_SAMPLE_ST_CLR | SOC_ETM_REGDMA_TASK_START3_ST_CLR | SOC_ETM_REGDMA_TASK_START2_ST_CLR | SOC_ETM_REGDMA_TASK_START1_ST_CLR | SOC_ETM_REGDMA_TASK_START0_ST_CLR |   |   |   |   |   |       |
| 31  | 30   | 29   | 28   | 27  | 26  | 25                                 | 24                           | 23                            | 22                              | 21                                  | 20                               | 19                               | 18                                | 17                               | 16                               | 15                                | 14                               | 13                               | 12                                   | 11                                  | 10                                      | 9                                 | 8                                 | 7                                 | 6                                 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0   | 0  | 0  | 0  | 0   | 0   | 0                                  | 0                            | 0                             | 0                               | 0                                   | 0                                | 0                                | 0                                 | 0                                | 0                                | 0                                 | 0                                | 0                                | 0                                    | 0                                   | 0                                       | 0                                 | 0                                 | 0                                 | 0                                 | 0 | 0 | 0 | 0 | 0 | Reset |

Reset

**SOC\_ETM\_REGDMA\_TASK\_START0\_ST\_CLR** Configures whether to clear REGDMA\_TASK\_START0.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_TASK\_START1\_ST\_CLR** Configures whether to clear REGDMA\_TASK\_START1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_TASK\_START2\_ST\_CLR** Configures whether to clear REGDMA\_TASK\_START2.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_REGDMA\_TASK\_START3\_ST\_CLR** Configures whether to clear REGDMA\_TASK\_START3.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_TMPSNSR\_TASK\_START\_SAMPLE\_ST\_CLR** Configures whether to clear TMP-SNSR\_TASK\_START\_SAMPLE.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...



**Register 12.37. SOC\_ETM\_TASK\_ST5\_CLR\_REG (0x0214)**

Continued from the previous page...

**SOC\_ETM\_TMPSNSR\_TASK\_STOP\_SAMPLE\_ST\_CLR** Configures whether to clear TMP-SNSR\_TASK\_STOP\_SAMPLE.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_TASK\_START\_RX\_ST\_CLR** Configures whether to clear I2SO\_TASK\_START\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_TASK\_START\_TX\_ST\_CLR** Configures whether to clear I2SO\_TASK\_START\_TX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_TASK\_STOP\_RX\_ST\_CLR** Configures whether to clear I2SO\_TASK\_STOP\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2SO\_TASK\_STOP\_TX\_ST\_CLR** Configures whether to clear I2SO\_TASK\_STOP\_TX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_TASK\_START\_RX\_ST\_CLR** Configures whether to clear I2S1\_TASK\_START\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_TASK\_START\_TX\_ST\_CLR** Configures whether to clear I2S1\_TASK\_START\_TX.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.37. SOC\_ETM\_TASK\_ST5\_CLR\_REG (0x0214)**

Continued from the previous page...

**SOC\_ETM\_I2S1\_TASK\_STOP\_RX\_ST\_CLR** Configures whether to clear I2S1\_TASK\_STOP\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S1\_TASK\_STOP\_TX\_ST\_CLR** Configures whether to clear I2S1\_TASK\_STOP\_TX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_TASK\_START\_RX\_ST\_CLR** Configures whether to clear I2S2\_TASK\_START\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_TASK\_START\_TX\_ST\_CLR** Configures whether to clear I2S2\_TASK\_START\_TX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_TASK\_STOP\_RX\_ST\_CLR** Configures whether to clear I2S2\_TASK\_STOP\_RX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_I2S2\_TASK\_STOP\_TX\_ST\_CLR** Configures whether to clear I2S2\_TASK\_STOP\_TX.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_ULP\_TASK\_WAKEUP\_CPU\_ST\_CLR** Configures whether to clear  
ULP\_TASK\_WAKEUP\_CPU.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.37. SOC\_ETM\_TASK\_ST5\_CLR\_REG (0x0214)**

Continued from the previous page...

**SOC\_ETM\_ULP\_TASK\_INT\_CPU\_ST\_CLR** Configures whether to clear ULP\_TASK\_INT\_CPU.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_TASK\_START\_ST\_CLR** Configures whether to clear RTC\_TASK\_START.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_TASK\_STOP\_ST\_CLR** Configures whether to clear RTC\_TASK\_STOP.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_TASK\_CLR\_ST\_CLR** Configures whether to clear RTC\_TASK\_CLR.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_RTC\_TASK\_TRIGGERFLW\_ST\_CLR** Configures whether to clear RTC\_TASK\_TRIGGERFLW.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CHO\_ST\_CLR** Configures whether to clear GDMA\_AHB\_TASK\_IN\_START\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CH1\_ST\_CLR** Configures whether to clear GDMA\_AHB\_TASK\_IN\_START\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_GDMA\_AHB\_TASK\_IN\_START\_CH2\_ST\_CLR** Configures whether to clear GDMA\_AHB\_TASK\_IN\_START\_CH2.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

**Register 12.37. SOC\_ETM\_TASK\_ST5\_CLR\_REG (0x0214)**

Continued from the previous page...

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AHB_TASK_OUT_START_CHO_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AHB_TASK_OUT_START_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_TASK_OUT_START_CH1_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AHB_TASK_OUT_START_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AHB_TASK_OUT_START_CH2_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AHB_TASK_OUT_START_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_TASK_IN_START_CHO_ST_CLR</b>  | Configures | whether | to | clear |
| GDMA_AXI_TASK_IN_START_CHO.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |
| <b>SOC_ETM_GDMA_AXI_TASK_IN_START_CH1_ST_CLR</b>  | Configures | whether | to | clear |
| GDMA_AXI_TASK_IN_START_CH1.                       |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

### Register 12.38. SOC\_ETM\_TASK\_ST6\_CLR\_REG (0x021C)

[illegible]

|  |            |         |    |       |
|--|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AXI_TASK_IN_START_CH2_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AXI_TASK_IN_START_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                            |            |         |    |       |
| 1: Clear   |            |         |    |       |
| (WT)   |            |         |    |       |

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CHO_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AXI_TASK_OUT_START_CHO.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CH1_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AXI_TASK_OUT_START_CH1.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

|   |            |         |    |       |
|---|------------|---------|----|-------|
| <b>SOC_ETM_GDMA_AXI_TASK_OUT_START_CH2_ST_CLR</b> | Configures | whether | to | clear |
| GDMA_AXI_TASK_OUT_START_CH2.                      |            |         |    |       |
| 0: Invalid. No effect                             |            |         |    |       |
| 1: Clear  |            |         |    |       |
| (WT)  |            |         |    |       |

**SOC\_ETM\_PMU\_TASK\_SLEEP\_REQ\_ST\_CLR** Configures whether to clear PMU\_TASK\_SLEEP\_REQ.  
0: Invalid. No effect  
1: Clear  
(WT)

Continued on the next page...

**Register 12.38. SOC\_ETM\_TASK\_ST6\_CLR\_REG (0x021C)**

Continued from the previous page...

**SOC\_ETM\_DMA2D\_TASK\_IN\_START\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_IN\_START\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_IN\_START\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_IN\_START\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_IN\_DSCR\_READY\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_IN\_DSCR\_READY\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_IN\_DSCR\_READY\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_IN\_DSCR\_READY\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CHO\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_OUT\_START\_CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CH1\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_OUT\_START\_CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_START\_CH2\_ST\_CLR** Configures whether to clear  
DMA2D\_TASK\_OUT\_START\_CH2.

0: Invalid. No effect

1: Clear

(WT)

Continued on the next page...

### Register 12.38. SOC\_ETM\_TASK\_ST6\_CLR\_REG (0x021C)

Continued from the previous page...

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CHO\_ST\_CLR** Configures whether to clear DMA2D TASK OUT DSCR READY CHO.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CH1\_ST\_CLR** Configures whether to clear DMA2D TASK OUT DSCR READY CH1.

0: Invalid. No effect

1: Clear

(WT)

**SOC\_ETM\_DMA2D\_TASK\_OUT\_DSCR\_READY\_CH2\_ST\_CLR** Configures whether to clear DMA2D TASK\_OUT DSCR\_READY\_CH2.

0: Invalid. No effect

1: Clear

(WT)

### Register 12.39. SOC\_ETM\_CLK\_EN\_REG (0x0220)

[illegible]

**SOC\_ETM\_CLK\_EN** Configures resister clock gating.

0: Support clock only when application writes registers

1: Force on clock gating for registers

(R/W)

Register 12.40. SOC\_ETM\_DATE\_REG (0x0224)

|                       |    |    |   |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|-----------------------|----|----|---|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| <div>(reserved)</div> |    |    |   | <div>SOC_ETM_DATE</div> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31                    | 28 | 27 | 0 |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0                     | 0  | 0  | 0 | 0x2303031               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

SOC\_ETM\_DATE Version control register. (R/W)



## Chapter 13

# Low-Power Management

### 13.1 Overview

ESP32-P4 features an advanced low-power management system that optimizes the chip's power consumption while maintaining its high performance.

The low-power management system employs various power-saving techniques such as sleep modes, dynamic voltage and frequency scaling, and peripheral power gating to minimize the chip's power consumption.

At the core of this low-power management system is the power management unit (PMU) hardware component. The PMU powers up and down different power domains of the chip to achieve the best balance between chip performance, power consumption, and wake-up latency.

### 13.2 Terminology

The following terms related to low-power management are defined in the context of the *ESP32-P4 Technical Reference Manual* to help readers better understand this document:

|                                    |   |
|------------------------------------|---|
| <b>Low-power management</b>        | Refers to the whole system that manages the chip's power consumption.   |
| <b>Power management unit (PMU)</b> | Refers to the specific hardware module that controls power up and down for power domains, clocks, and power-related logic.                      |
| <b>Power domain</b>                | Refers to the smallest unit that can be independently powered up or down. A power domain can contain one or multiple modules within the chip.   |
| <b>PMU states</b>                  | Refers to the states of the PMU's state machine. Users can configure the clock gating and power gating of a power domain in each of the states. |
| <b>Power modes</b>                 | Refers to the preset power modes that power up different domains for typical application scenarios.   |

### 13.3 Features

The PMU has the following features:

- Supports three configurable PMU states. Software can flexibly configure them according to the needs.
  - HP\_ACTIVE
  - HP\_SLEEP

- LP\_SLEEP
- Supports four preset power modes that suit various typical usage scenarios:
  - Active
  - Light-sleep0 (This mode does not power down the peripherals, but only stops the clock, resulting in higher power consumption and a smaller wake-up delay.)
  - Light-sleep1 (This mode powers down the peripherals and needs data backup and restoration, resulting in lower power consumption and a larger wake-up delay.)
  - Deep-sleep
- LP SRAM (32 KB): Keep power up in all modes, can store HP CPU's non-volatile data, and LP CPU's instructions and data.
- Supports a programmable retention DMA that backs up and restores the CPU and peripherals status when the chip switches between PMU states.
- Supports a power controller that controls the power and clocks depending on the power modes.

## 13.4 Functional Description

ESP32-P4's low-power management involves the following components:

- **Power scheme:** The power scheme of ESP32-P4 includes power regulators, digital power domains, analog power domains, etc.
- **PMU controller:** It is the core part of the PMU, controlling the power up and down of power domains, clocks, etc.
- **One RTC timer:** For more information, please refer to Chapter [17 RTC Timer](#).
- **16 LP GPIO pins (GPIO0–GPIO15):** These pins are always powered up and are not affected by any low-power modes, which makes them suitable for working as wake-up sources when the chip is in low-power modes. These pins can also work as regular GPIOs. For more information on LP GPIOs, refer to Chapter [8 GPIO Matrix and IO MUX](#).
- **32 KB SRAM:** The 32 KB SRAM is accessible to both HP CPU and LP CPU. It works under the HP CPU clock when accessed by the HP CPU and under the LP CPU clock when accessed by the LP CPU.
- **Brownout detector:** Monitors the power of the voltage supply pins, ensuring stable chip operation and preventing the SoC from potential malfunction if it is subject to glitches or under-voltage. For more information, refer to Chapter [21 Brown-out Detector](#).

The following sections provide a detailed description of the components mentioned above.

### 13.4.1 Power Scheme

Figure [13.4-1](#) shows the power scheme of ESP32-P4 that mainly includes:

- A DCDC voltage regulation feedback system
- Two internal regulators
- Four output regulators (EXT\_LDO)

- Analog power domains
- Digital power domains
- Battery power domain

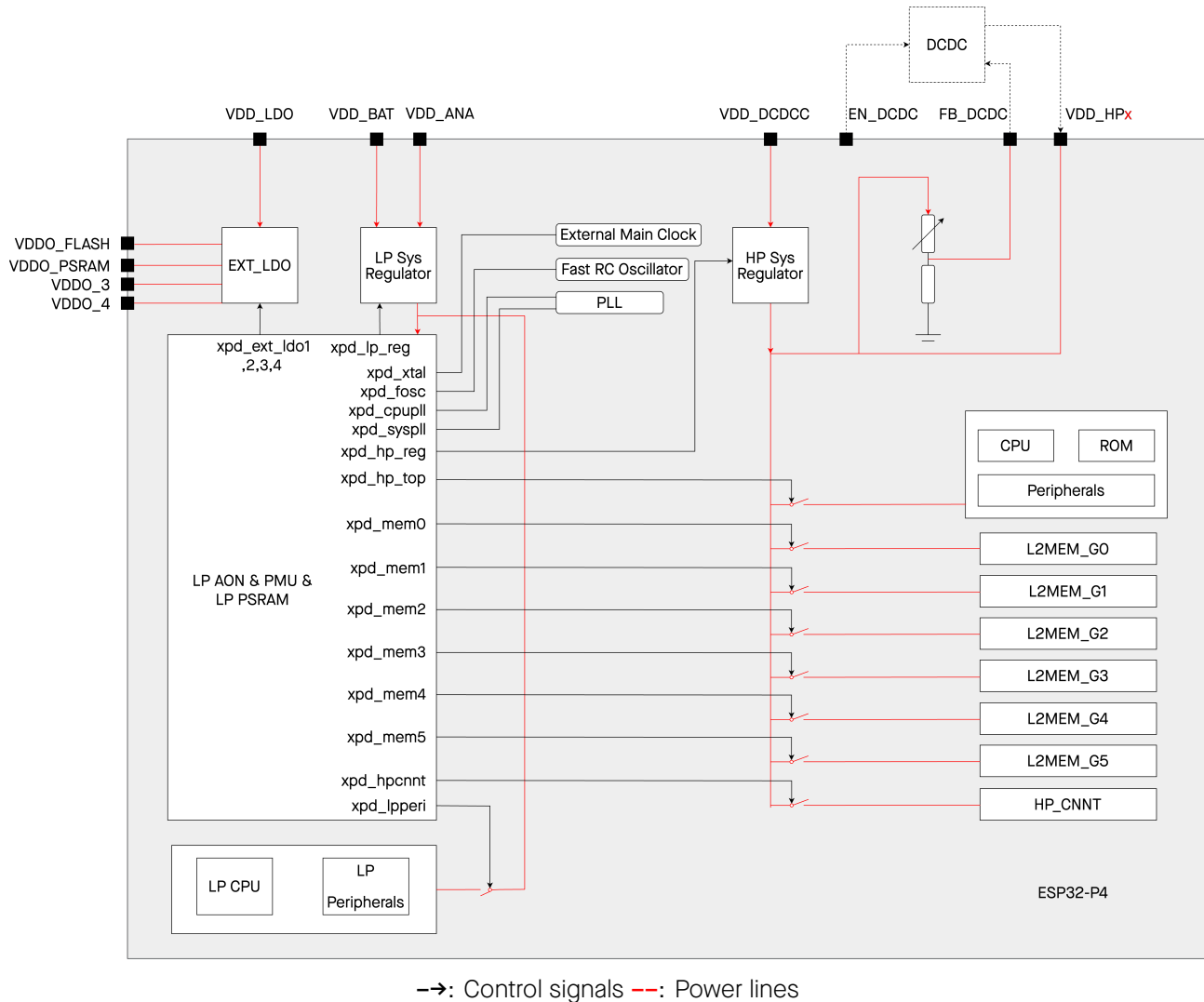


Figure 13.4-1. ESP32-P4 Power Scheme

### 13.4.1.1 Regulators

As shown in Figure 13.4-1, the analog section of ESP32-P4 includes one external DCDC with feedback regulation and two internal HP/LP system regulators, responsible for regulating the power supply for different power domains.

- The **DCDC voltage regulation feedback system** adjusts the voltage of the external DCDC.
- The **HP (high-performance) system regulator** has strong drive capability, higher power consumption, and adjustable output voltage. It is only suitable for power-up and sleep modes.
- The **LP (low-power) system regulator** regulates the power supply of low-power modules. Its output voltage is also adjustable.

The DCDC voltage regulation feedback system and the HP system regulator are responsible for powering the HP system. The external DCDC can adjust its output voltage through the internal voltage feedback system. By

default, the chip is powered by the HP system regulator when powered up. After power-up is complete, it is recommended to switch to the DCDC power supply for better efficiency and load capacity.

### 13.4.1.2 Digital Power Domains

- The HP system contains the following digital power domains:
  - **Peripherals + ROM + CPU (PD\_TOP)**: Mainly includes the bus and HP peripherals.
  - **L2MEM\_G0–G5**: It is divided into six sub-power domains, as shown in Figure 13.4-1.
  - **HP\_CNNT (PD\_HP\_CNNT)**: Mainly includes USB and SDIO modules.

There is an independent power switch between the regulator and each power domain, enabling up/down control of the digital power domain.

- The LP system contains the following digital power domains:
  - **LP PD peripherals (PD\_LP\_PERI)**: Mainly includes LP CPU and LP peripherals.
  - **LP always-on (PD\_AON)**: It mainly includes LP always-on peripherals (e.g., RTC timer) and PMU controller. This power domain keeps powered up all the time.

### 13.4.1.3 Analog Power Domains

- The HP system contains the following analog power domains:
  - CPLL\_CLK
  - SPLL\_CLK
  - Audio PLL
  - SDIO PLL
- The LP system contains the following analog power domains:
  - External Main Clock
  - Fast RC Oscillator

### 13.4.1.4 Battery Power Domain

The battery power domain (VDD\_BAT) serves as a backup power domain. When all external power supplies (VDD\_ANA) are turned off, the low-power system regulators, LP\_SLOW\_CLK, and LP\_FAST\_CLK can all be powered by the VDD\_BAT supply.

## 13.4.2 PMU

The PMU of ESP32-P4 controls power consumption-related components of each power domain, such as power and clock. PMU consists of the following major parts:

- **PMU main state machine**: It records and switches the PMU states.
- **Sleep/wake-up controller**: It sends sleep or wake-up requests to the PMU main state machine.
- **Power controllers**: They control the power and clock signals depending on the power modes of the chip. The power controllers include:

- **Digital power controller:** It powers up or down the digital power domains.
- **Analog power controller:** It enables the analog modules, such as the regulators, analog clocks, etc.
- **Clock controller:** It manages the clock gating of peripherals and selects analog clock sources for digital clocks.
- **Data backup controller:** It controls the data backup and restore process when the chip switches between PMU states.
- **System controller:** It controls some system-level modules, such as suspending watchdog functionality in sleep mode (when the CPU is unavailable).

The PMU workflow involves the following steps:

- The sleep/wake-up controller sends sleep or wake-up requests to the PMU main state machine.
- The PMU main state machine generates power gating, clock gating, and reset signals.
- The power controllers and clock controllers power up or down different power domains and clocks based on the signals generated by the PMU main state machine, allowing the chip to enter or exit different low-power modes.

The PMU workflow is shown in Figure [13.4-2](#). The definitions of HP\_SWITCH and LP\_SWITCH are as follows:

- **HP\_SWITCH:** The intermediate state for the HP system transitioning between HP\_ACTIVE and HP\_SLEEP. The hardware completes the control switching of various controllers in this state.
- **LP\_SWITCH:** The intermediate state for the LP system transitioning between HP\_SLEEP and LP\_SLEEP. The hardware completes the control switching of various controllers in this state.

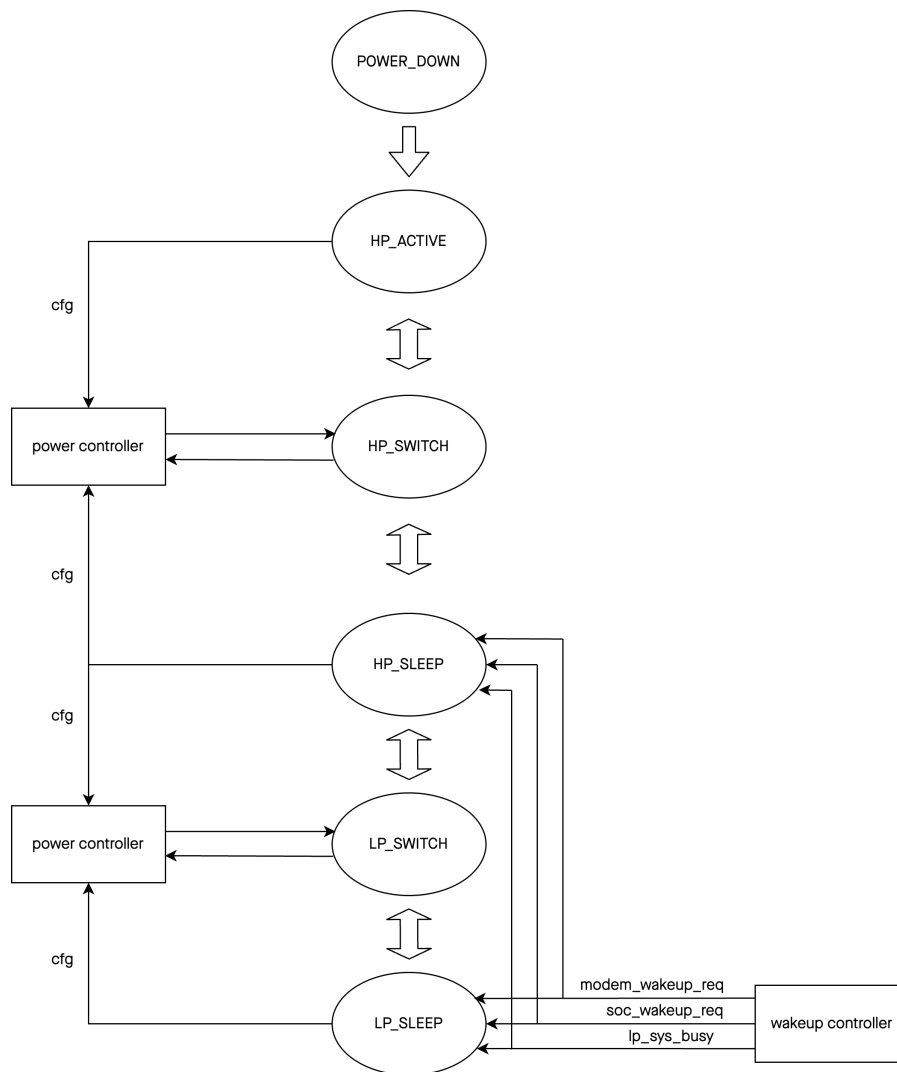


Figure 13.4-2. PMU Workflow

The following sections describe the main parts of PMU.

### 13.4.2.1 PMU Main State Machine

The PMU main state machine receives sleep and wake-up signals, changes the state of power and clock through the power controllers, thereby switching PMU states, and achieving a balance between performance and power consumption of the chip.

The PMU main state machine supports three PMU states, each controlled by different sleep and wake-up signals, supporting software customization of power and clocks. These PMU states allow the software to expand power modes for various application scenarios. The three PMU states are:

- **HP\_ACTIVE:** The circuits on the chip are powered up to a maximum, supporting the HP system and LP system operation.
- **HP\_SLEEP:** The HP system is in sleep, supporting LP peripherals operation.
- **LP\_SLEEP:** The HP system and LP peripherals are in sleep, while the always-on circuits remain operational.

**Note:**

The division of the HP and LP systems is as follows:

- LP system (peripherals): LP RISC-V 32-bit Microprocessor, LP GPIO, LP UART, LP I2C, LP I2S, touch sensor, temperature sensor, LP ADC, LP SPI
- LP system (always-on circuits): PMU, RTC Watchdog Timer, Super Watchdog
- HP system: All peripherals except those belonging to the LP system.

For more details, please refer to [ESP32-P4 Datasheet](#) > *Functional Block Diagram*.

HP\_ACTIVE is the operating state of the HP system, HP\_SLEEP is the sleep state of the HP system, LP\_SLEEP is the sleep state of the LP system. The operating state of the LP system reuses the HP\_SLEEP state and is therefore also referred to as HP\_SLEEP.

- If a module belongs to the HP system, its power up/down can be configured in the HP\_ACTIVE/HP\_SLEEP states. It reuses the HP\_SLEEP state in the LP\_SLEEP state.
- If a module belongs to the LP system, its power up/down can be configured in the HP\_SLEEP/LP\_SLEEP state. It reuses the HP\_SLEEP state in the HP\_ACTIVE state.

Take the HP CPU as an example. The HP CPU belongs to the HP system, so it can be configured to power up/down in the HP\_ACTIVE/HP\_SLEEP states through the following registers and reuse the HP\_SLEEP configurations in LP\_SLEEP.

- HP\_ACTIVE: [PMU\\_HP\\_ACTIVE\\_PD\\_TOP\\_PD\\_EN](#)
- HP\_SLEEP: [PMU\\_HP\\_SLEEP\\_PD\\_TOP\\_PD\\_EN](#)

Similarly, users can configure the power up and down for other power domains in different PMU states. For the configuration registers, please refer to Section 13.8.

**Note:**

In the following text, all such configuration registers are collectively referred to as PMU\_*n1*\_PD\_*POWERDOMAIN*\_PD\_EN, where *n1* represents the three PMU states.

Once the configuration is done, the PMU uses various controllers to make these configurations effective, as described in the following sections.

### 13.4.2.2 Sleep/Wake-up Controller

The sleep/wake-up controller initiates sleep and wake-up requests to the PMU main state machine. ESP32-P4 supports multiple wake-up sources to wake the CPU from different power modes. Table 13.4-1 lists all the wake-up sources.

All the wake-up sources in Table 13.4-1 can wake up both the HP CPU and the LP CPU. Users can configure [PMU\\_WAKEUP\\_ENA](#) to set the target to the HP CPU, and configure [PMU\\_LP\\_CPU\\_WAKEUP\\_EN](#) to set the target to the LP CPU. Configuring both registers simultaneously can wake up both the HP CPU and the LP CPU.

Table 13.4-1. Wake-up Sources

| Bit in <a href="#">PMU_WAKEUP_ENA/PMU_LP_CPU_WAKEUP_EN</a> | Wake-up Sources   | Source Power Domains |
|--|-------------------|----------------------|
| 0  | HP_SDIO           | PD_HP_CNNT           |
| 1  | Software wakeup   | PD_LP_PERI           |
| 2  | HP GPIO           | PD_TOP               |
| 3  | HP USB            | PD_HP_CNNT           |
| 4  | HP UART4          | PD_TOP               |
| 5  | HP UART3          | PD_TOP               |
| 6  | HP UART2          | PD_TOP               |
| 7  | HP UART1          | PD_TOP               |
| 8  | HP UART0          | PD_TOP               |
| 9  | LP GPIO           | PD_LP_PERI           |
| 10   | LP UART           | PD_LP_PERI           |
| 11   | LP TOUCH          | PD_LP_PERI           |
| 12   | EXT IO            | PD_LP_PERI           |
| 13   | RTC_TIMER_TARO    | PD_AON               |
| 14   | BROWN OUT         | PD_AON               |
| 15   | VBAT_UNDERVOLTAGE | PD_AON               |
| 16   | LP CORE EXCEPTION | PD_LP_PERI           |
| 17   | ETM               | PD_TOP               |
| 18   | RTC_TIMER_TAR1    | PD_AON               |
| 19   | LP I2S            | PD_LP_PERI           |

ESP32-P4 provides a hardware mechanism that can reject sleep, meaning if some peripherals are in an un interruptible working state and the HP CPU tries to sleep, the peripherals will send a wake-up signal to prevent the HP CPU from sleeping, thus ensuring the peripherals work normally.

The wake-up sources in Table 13.4-1 can all be configured as events to reject sleep. Users can configure the following registers to implement sleep rejection. The configuration values of [PMU\\_SLEEP\\_REJECT\\_ENA](#) and [PMU\\_SLP\\_REJECT\\_CAUSE\\_REG](#) and the corresponding wake-up sources are the same as shown in Table 13.4-1.

- Enable sleep rejection feature:
  - Set [PMU\\_SLP\\_REJECT\\_EN](#) to 1 to enable the sleep rejection feature.
  - Configure [PMU\\_SLEEP\\_REJECT\\_ENA](#) to select the sleep rejection signal source.
- Read [PMU\\_SLP\\_REJECT\\_CAUSE\\_REG](#) for the source of sleep rejection event.

### 13.4.2.3 Analog Power Controller

The analog power controller controls the power up and down of the analog circuits (including voltage regulators, high-speed clocks, and slow-speed clocks) in the PMU states.

The configuration of the regulators is as follows:

- Configure [PMU\\_n1\\_HP\\_REGULATOR\\_XPD](#) or [PMU\\_n1\\_LP\\_REGULATOR\\_XPD](#) to enable or disable the output voltage of the HP/LP sys regulator in the target PMU state. Turning off the LP sys regulator is not



recommended, as it may cause the PMU itself to power down, resulting in chip malfunction.

The configuration of the high-speed clocks (XTAL\_CLK and PLL clocks) is as follows:

- XTAL\_CLK: Configure [PMU\\_HP\\_SLEEP\\_XPD\\_XTAL](#) to 1 to enable XTAL\_CLK when the chip switches the PMU state to HP\_SLEEP.

Note: To avoid the instability in XTAL\_CLK during startup, users have the option to configure [PMU\\_WAIT\\_XTL\\_STABLE](#) to delay the gate opening for XTAL\_CLK. This delay ensures that the gate opening is enabled after [PMU\\_WAIT\\_XTL\\_STABLE](#) CLK\_DYN\_FAST\_CLK cycles following the power-up of XTAL\_CLK.

- CPLL\_CLK: PMU can enable CPLL\_CLK in different PMU states by configuring [PMU\\_n1\\_XPD\\_PLL\[0\]](#) to 1. For example, configuring [PMU\\_HP\\_ACTIVE\\_XPD\\_PLL\[0\]](#) to 1 enables the CPLL\_CLK clock when the chip is in HP\_ACTIVE state.
- SPLL\_CLK: PMU can enable SPLL\_CLK in different PMU states by configuring [PMU\\_n1\\_XPD\\_PLL\[1\]](#) to 1. For example, configuring [PMU\\_HP\\_ACTIVE\\_XPD\\_PLL\[1\]](#) to 1 enables the SPLL\_CLK clock when the chip is in HP\_ACTIVE state.
- Audio PLL: PMU can enable Audio PLL in different PMU states by configuring [PMU\\_n1\\_XPD\\_PLL\[2\]](#) to 1. For example, configuring [PMU\\_HP\\_ACTIVE\\_XPD\\_PLL\[2\]](#) to 1 enables the Audio PLL clock when the chip is in HP\_ACTIVE state.
- SDIO PLL: PMU can enable SDIO PLL in different PMU states by configuring [PMU\\_n1\\_XPD\\_PLL\[3\]](#) to 1. For example, configuring [PMU\\_HP\\_ACTIVE\\_XPD\\_PLL\[3\]](#) to 1 enables the SDIO PLL clock when the chip is in HP\_ACTIVE state.

Note:

- Before enabling the PLL clocks please ensure that XTAL\_CLK is stable.
- To avoid the instability in the PLL clocks during startup, users have the option to configure [PMU\\_WAIT\\_PLL\\_STABLE](#) to delay the gate opening for the PLL clocks. This delay ensures that the gate opening is enabled after [PMU\\_WAIT\\_PLL\\_STABLE](#) CLK\_DYN\_FAST\_CLK cycles following the power-up of the PLL clocks.

Slow-speed clocks (RC\_FAST\_CLK and XTAL32K\_CLK) operate with low power. The power up and down of the slow-speed clocks in HP\_ACTIVE and HP\_SLEEP states are controlled by [PMU\\_HP\\_SLEEP\\_XPD\\_FOSC\\_CLK](#). In LP\_SLEEP state, the power up and down of the slow-speed clocks are controlled by [PMU\\_LP\\_SLEEP\\_XPD\\_FOSC\\_CLK](#).

#### 13.4.2.4 Digital Power Controller

The digital power controller controls the power up and down of digital power domains in different PMU states. Unlike the analog power controller, the digital power controller does not directly control the regulator but instead controls the power switch connected to the regulator to power up and down the digital power domains.

The LP PD Peripherals domain can only be powered up and down while the PMU state switches between HP\_SLEEP and LP\_SLEEP. The other digital power domains can only be powered up and down while the PMU state switches between HP\_SLEEP and HP\_ACTIVE.

When the chip switches between PMU states, if the power configuration of a power domain in the current

PMU state does not match the power configuration it is about to switch to, then the power up-down process will be activated. Take the power up-to-down process of the CPU power domain as an example. Configure [PMU\\_HP\\_SLEEP\\_PD\\_TOP\\_PD\\_EN](#) to 1 or 0 to power down or up the CPU power domain in HP\_SLEEP. PMU will perform the following configurations:

- Enable the digital isolation unit to ensure that the powered-down modules do not output unstable voltage levels to the powered-up modules. When a power domain loses power, the output of this module will be clamped to a fixed value.
- Enable reset. When the CPU power domain loses power, its global reset signal is set to a reset state, which persists for a period after the CPU power domain is re-powered. This mechanism guarantees a reset-to-release process for the CPU power domain during power-up, effectively mitigating any instability caused by power up-down transitions.

The following explains the power up and down of each digital power domain:

- L2MEM\_GO–G5

Configure [PMU\\_n1\\_PD\\_HP\\_MEM\\_PD\\_EN](#) to power up or down L2MEM\_GO–G5.

- HP\_CNNT

Configure [PMU\\_n1\\_PD\\_CNNT\\_PD\\_EN](#) to power up or down HP\_CNNT.

- Peripherals + ROM + CPU (PD\_TOP)

Configure [PMU\\_n1\\_PD\\_TOP\\_PD\\_EN](#) to power or down PD\_TOP.

When the Peripherals domain is powered down, the following features are configurable:

- Powering down the Peripherals domain may cause instability in GPIOs. This can be addressed by maintaining the state of the GPIOs (excluding the LP GPIOs) through PMU. For example, configuring [PMU\\_HP\\_SLEEP\\_HP\\_PAD\\_HOLD\\_ALL](#) can keep GPIOs in the same state as before Peripherals was powered down in HP\_SLEEP.
- In the HP\_ACTIVE state, Memory Deep-sleep mode is supported under a standard power supply. The memory cannot be read or written in this mode, but data can be retained. Configure [PMU\\_n1\\_HP\\_MEM\\_DSLP](#) to enable this mode.

- LP PD Peripherals

The LP PD Peripherals power domain remains powered up when the chip is in HP\_ACTIVE state. The power state of LP PD Peripherals is configurable only in HP\_SLEEP and LP\_SLEEP states. The LP PD Peripherals power domain has an independent digital power switch, and its power control is not dependent on the power state of other digital power domains.

### 13.4.2.5 Clock Controller

The clock controller mainly controls the high-performance system clocks and LP system clocks when the chip switches between PMU states.

The high-performance system clocks include ROOT\_CLK and high-performance system peripherals clocks. When the chip switches between HP\_ACTIVE and HP\_SLEEP states, PMU can switch, power up/down, and divide the frequency of ROOT\_CLK, as well as power up/down high-performance system peripherals clocks.

- ROOT\_CLK can be controlled as follows:
  - Configure PMU\_*n1*\_SYS\_CLK\_SLP\_SEL to 1 to indicate that when the chip enters the corresponding PMU state, the clock source is controlled by PMU.
  - Configure PMU\_*n1*\_ICG\_SYS\_CLOCK\_EN to 0 to disable ROOT\_CLK in the corresponding PMU state.
  - Configure PMU\_*n1*\_DIG\_SYS\_CLK\_SEL to select the clock source after the chip enters the corresponding PMU state. For details, please refer to Chapter 9 *Reset and Clock* > Table 9.2-1.
- High-performance system peripheral clocks can be controlled as follows:
  - Configure PMU\_*n1*\_ICG\_SLP\_SEL to 1 so that the clock gating in the target state is controlled by PMU. Configure this register to 0 so that the clock gating is controlled by PCR registers.
  - Configure PMU\_*n1*\_DIG\_ICG\_FUNC\_EN to power up/down the function clock in the target PMU state. For detailed configuration please see Table 13.4-2.

**Table 13.4-2. HP System Peripherals' Function Clocks**

| Bit in PMU_ <i>n1</i> _DIG_ICG_FUNC_EN | Clock              |
|--|--------------------|
| bit 0                                  | HP_CPU0_CLK        |
| bit 1                                  | HP_CPU1_CLK        |
| bit 2                                  | HP_CPU0_CLIC_CLK   |
| bit 3                                  | HP_CPU1_CLIC_CLK   |
| bit 4                                  | MISC_CPU_CLK       |
| bit 5                                  | MISC_SYS_CLK       |
| bit 6                                  | ICM_CPU_CLK        |
| bit 7                                  | ICM_SYS_CLK        |
| bit 8                                  | ICM_MEM_CLK        |
| bit 9                                  | ICM_APB_CLK        |
| bit 10                                 | SPM_CPU_CLK        |
| bit 11                                 | L2MEM_MEM_CLK      |
| bit 12                                 | L2MEM_SYS_CLK      |
| bit 13                                 | L1CACHE_CPU_CLK    |
| bit 14                                 | L1CACHE_D_CPU_CLK  |
| bit 15                                 | L1CACHE_IO_CPU_CLK |
| bit 16                                 | L1CACHE_I1_CPU_CLK |
| bit 17                                 | L1CACHE_MEM_CLK    |
| bit 18                                 | L1CACHE_D_MEM_CLK  |
| bit 19                                 | L1CACHE_IO_MEM_CLK |
| bit 20                                 | L1CACHE_I1_MEM_CLK |
| bit 21                                 | L2CACHE_MEM_CLK    |
| bit 22                                 | L2CACHE_SYS_CLK    |
| bit 23                                 | REGDMA_SYS_CLK     |
| bit 24                                 | HP_CLKRST_APB_CLK  |
| bit 25                                 | SYSREG_APB_CLK     |
| bit 26                                 | INTRMTX_CLK        |
| bit 27                                 | N/A                |

| PMU_ <i>n1</i> _DIG_ICG_FUNC_EN Bit | Clock |
|-------------------------------------|-------|
| bit 28                              | N/A   |
| bit 29                              | N/A   |
| bit 30                              | N/A   |
| bit 31                              | N/A   |

The LP system clocks are mainly used in the low-power system and include the following clocks:

- LP\_SLOW\_CLK
- LP\_FAST\_CLK
- LP\_DYN\_SLOW\_CLK
- LP\_DYN\_FAST\_CLK
- XTAL\_D2\_CLK

The clock frequency of LP\_DYN\_FAST\_CLK is controlled by hardware as follows, depending on the PMU state (and cannot be changed by the user):

- LP\_SLEEP: The LP\_DYN\_FAST\_CLK frequency is the same as LP\_SLOW\_CLK.
- HP\_ACTIVE, HP\_SLEEP: The LP\_DYN\_FAST\_CLK frequency is the same as LP\_FAST\_CLK.

#### 13.4.2.6 Backup Controller

ESP32-P4 has a Retention DMA module that can transfer data between memory and peripherals when the chip switches between PMU states. In this way, the data is backed up when the power domain is powered down and restored when the power domain is powered up again.

Data transfer is implemented in the Peripherals power domain. PMU only generates relevant control signals. It is important to note that the data transfer control registers are directional, as unlike other control registers, these control behaviors are determined by both the original PMU state and the target PMU state.

For example, the control registers for transitioning from HP\_ACTIVE to HP\_SLEEP and from HP\_SLEEP to HP\_ACTIVE are different. The possible PMU state switches are listed below, collectively represented by *n2* in the register names:

- HP\_SLEEP2ACTIVE
- HP\_ACTIVE2SLEEP

The following section introduces how PMU controls the Retention DMA:

- Enable data transfer: Configure PMU\_*n2*\_BACKUP\_EN to 1 to enable data transfer when the corresponding PMU state switch is performed.
- Enable corresponding clocks: Before data transfer starts, configure PMU\_*n2*\_BACKUP\_CLK\_SEL to select the clock source of the Retention DMA, and configure PMU\_*n1*\_BACKUP\_ICG\_FUNC\_EN to enable the clock.

After the data transfer is completed, the value of PMU\_*n1*\_BACKUP\_ICG\_FUNC\_EN is determined by the configuration of PMU\_*n1*\_DIG\_ICG\_FUNC\_EN in the target PMU state.

- Configure data transfer direction: Configure the highest bit of PMU\_*n2*\_BACKUP\_MODE:

- 1: From peripheral to memory
- 0: From memory to peripheral
- Select linked list pointer: Configure the lower two bits of PMU\_*n2*\_BACKUP\_MODE to select the linked list pointer, specifically:
  - 0: PAU\_LINK\_ADDR\_0
  - 1: PAU\_LINK\_ADDR\_1
  - 2: PAU\_LINK\_ADDR\_2
  - 3: PAU\_LINK\_ADDR\_3

### 13.4.2.7 System Controller

The system controller controls some functional modules when the chip switches PMU states, to achieve stable and low-power chip performance. Specifically, the system controller supports:

- **Pausing the watchdog function:** Configuring PMU\_*n1*\_DIG\_PAUSE\_WDT to 1 disables the RTC watchdog timer (RWDT) function when the chip switches to the corresponding target PMU state. Note that if this register is configured to 0 in any sleep mode, the watchdog function is not disabled, and RWDT will reset as the CPU does not feed the watchdog.
- **Switching GPIO to sleep mode,** where the configuration of the GPIO holds. Consider a GPIO pin working in low-drive mode as an input and a wake-up pin. Setting PMU\_*n1*\_HP\_PAD\_HOLD\_ALL to 1 latches the current configuration of the GPIO pin as the sleep configuration when the chip transitions to the corresponding PMU state. For more information on the hold function of GPIO, please refer to Chapter 8 [GPIO Matrix and IO MUX](#) > Section 8.9.
- **Disabling UART wake-up function:** Configuring PMU\_*n1*\_UART\_WAKEUP\_EN to 0 disables the four UART wake-up modes in the corresponding PMU state. For more information on UART wake-up modes, please refer to Chapter 37 [UART Controller \(UART\)](#).
- **Pausing CPU:** Setting PMU\_*n1*\_DIG\_CPU\_STALL to 1 suspends the CPU in the corresponding PMU state.

### 13.4.2.8 Battery Power Controller

As shown in Figure 13.4-1, the low-power system regulator can be powered by VDD\_BAT (battery) or VDD\_ANA (analog). PMU\_*n1*\_VDDBAT\_MODE controls whether to enable the battery power. When PMU\_*n1*\_VDDBAT\_MODE is 0, the battery power is not enabled, and the low-power system regulator is powered by VDD\_ANA and can be used in Active mode or Light-sleep0/1 modes. When PMU\_*n1*\_VDDBAT\_MODE is 1, the battery power is enabled and can be used in Deep-sleep mode, where the main power, including VDD\_ANA, is cut off, and only the LP AON & PMU power domains are powered up.

### 13.4.2.9 Output Regulator Control

As shown in Figure 13.4-1, ESP32-P4 has four output regulators:

- VDDO\_FLASH (VO1), typically used for on-chip flash voltage regulation
- VDDO\_PSRAM (VO2), typically used for on-chip PSRAM voltage regulation
- VDDO\_3 (VO3) and VDDO\_4 (VO4), which convert the input VDD\_LDO (typically 3.3 V) into the voltages needed by peripherals such as flash, PSRAM, MIPI, and SDIO.

The regulators support the following features:

- **Supports LDO mode and bypass mode.** LDO mode supports an output of 0.5 V – 2.7 V, while bypass mode outputs the voltage of VDD\_LDO. Mode selection is controlled by a hardware state machine or a register, with the control authority managed by a register. The flash regulator (VO1) also supports eFuse control.
- The mode control for VO1 is shown in Figure 13.4-3. In the figure, TIEH\_SEL on the right being 0 selects LDO mode; being 1 selects bypass mode.

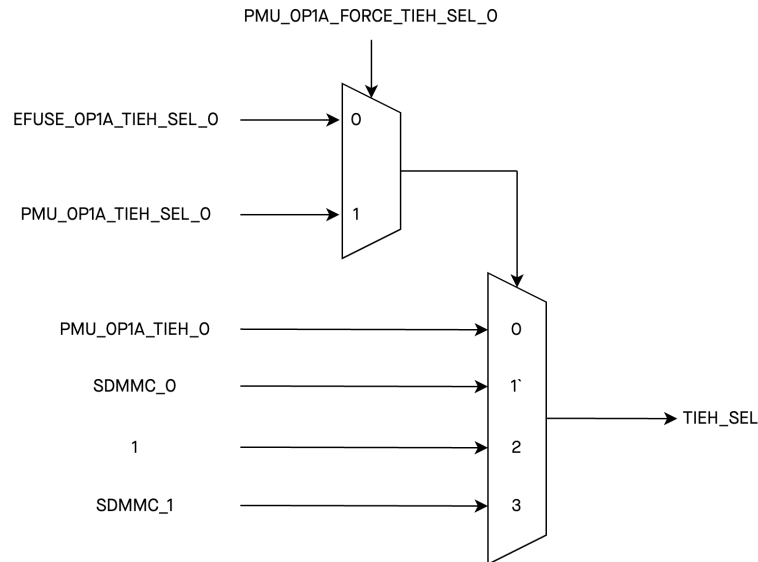


Figure 13.4-3. VO1 Mode Control

- The mode control for VO2/3/4 is shown in Figure 13.4-4. In the figure, TIEH\_SEL on the right being 0 selects LDO mode; being 1 selects bypass mode.

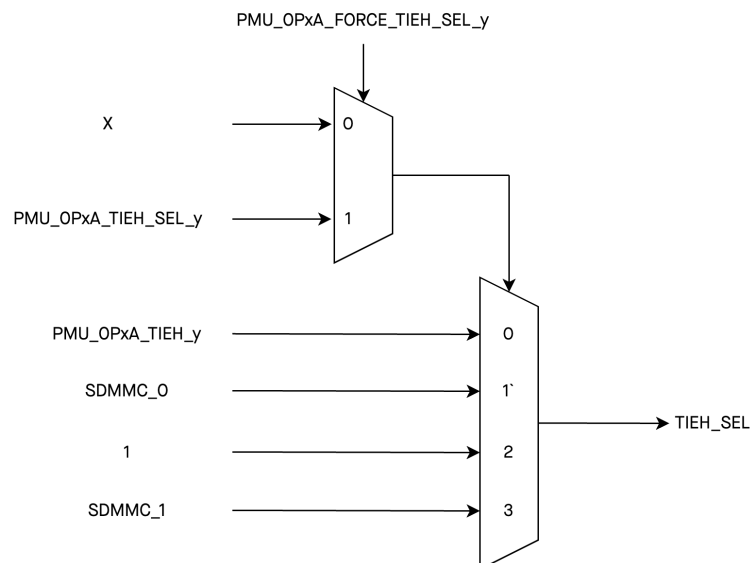


Figure 13.4-4. VO2/3/4 Mode Control

**Table 13.4-3. VO2/3/4 Registers**

| Regulators | PMU_OPxA_FORCE_TIEH_SEL_y                 | PMU_OPxA_TIEH_SEL_y                 | PMU_OPxA_TIEH_y                 |
|------------|---|-------------------------------------|---------------------------------|
| VO2        | <a href="#">PMU_OP1A_FORCE_TIEH_SEL_1</a> | <a href="#">PMU_OP1A_TIEH_SEL_1</a> | <a href="#">PMU_OP1A_TIEH_1</a> |
| VO3        | <a href="#">PMU_OP2A_FORCE_TIEH_SEL_0</a> | <a href="#">PMU_OP2A_TIEH_SEL_0</a> | <a href="#">PMU_OP2A_TIEH_0</a> |
| VO4        | <a href="#">PMU_OP2A_FORCE_TIEH_SEL_1</a> | <a href="#">PMU_OP2A_TIEH_SEL_1</a> | <a href="#">PMU_OP2A_TIEH_1</a> |

- **Supports switch control.** Only the flash voltage regulator (VO1) supports power control by the PMU state machine, the other regulators only support power control by software. The regulator is enabled when the register in Table 13.4-4 is set to 1; otherwise, the regulator is disabled.

**Table 13.4-4. Regulator Power Control**

| Regulator | Power Control                  |
|-----------|--------------------------------|
| VO1       | PMU_01_REGULATOR_VO1_XPD       |
| VO2       | <a href="#">PMU_OP1A_XPD_1</a> |
| VO3       | <a href="#">PMU_OP2A_XPD_0</a> |
| VO4       | <a href="#">PMU_OP2A_XPD_1</a> |

- **Over current protection:** Before powering up the regulators, users have the option to enable the over current protection function to prevent excessive transient current that may damage the capacitor. After the capacitor charging is complete, the over current protection should be disabled. The capacitor charging time depends on the load capacitance and voltage. The calculation formula is:  $T_{ms} = C_F \times V_V / 50$ . Table 13.4-5 provides the over current protection enable register; when the register is set to 1, the function is enabled; otherwise, it is disabled.

**Table 13.4-5. Over Current Protection Control**

| Regulators | Over Current Protection Control                  |
|------------|--|
| VO1        | FSM or <a href="#">PMU_ANA_OP1A_EN_CUR_LIM_0</a> |
| VO2        | <a href="#">PMU_ANA_OP1A_EN_CUR_LIM_1</a>        |
| VO3        | <a href="#">PMU_ANA_OP2A_EN_CUR_LIM_0</a>        |
| VO4        | <a href="#">PMU_ANA_OP2A_EN_CUR_LIM_1</a>        |

Due to the long power-up time, a waiting counter is provided for each regulator. Once the regulator is powered up, the counter is triggered and starts counting. The counter has two stages, and each stage triggers different interrupts. Typically, the waiting value for the first stage can be configured as the over-current protection value (counter target 1), and the second stage can be configured as the waiting stabilization value (counter target 2). The configuration of the counter is shown in the table below:

**Table 13.4-6. Regulator Waiting Counter**

| Regulators | Counter Target 1                        | Counter Target 2                        |
|------------|---|---|
| VO1        | <a href="#">PMU_OP1A_TARGET0_0[6:0]</a> | <a href="#">PMU_OP1A_TARGET1_0[7:0]</a> |
| VO2        | <a href="#">PMU_OP1A_TARGET0_1[7:0]</a> | <a href="#">PMU_OP1A_TARGET1_1[7:0]</a> |
| VO3        | <a href="#">PMU_OP2A_TARGET0_0[7:0]</a> | <a href="#">PMU_OP2A_TARGET1_0[7:0]</a> |
| VO4        | <a href="#">PMU_OP2A_TARGET0_1[7:0]</a> | <a href="#">PMU_OP2A_TARGET1_1[7:0]</a> |

**Note:**

1. The bit 7 of [PMU\\_OP1A\\_TARGETO\\_0](#) clears the counter. Setting bit 7 to 1 resets the counter.
2. The counter clock is derived from LP\_DYN\_SLOW\_CLK, which is divided by a factor of 16.

## 13.5 Power Modes

ESP32-P4 has three configurable PMU states. Based on the PMU states, the chip has defined four power modes for common application scenarios, as shown in Table 13.5-1.

**Table 13.5-1. Preset Power Modes**

| Power Modes  | Power Domains   |                      |     |        |             |          |        |
|--------------|-----------------|----------------------|-----|--------|-------------|----------|--------|
|              | LP<br>always-on | LP PD<br>peripherals | TOP | HPCNNT | RC_FAST_CLK | XTAL_CLK | PLL    |
| Active       | ON              | ON                   | ON  | ON     | ON          | ON       | ON     |
| Light-sleep0 | ON              | ON                   | ON  | ON     | ON/OFF      | ON/OFF   | ON/OFF |
| Light-sleep1 | ON              | ON/OFF               | OFF | ON     | ON/OFF      | ON/OFF   | ON/OFF |
| Deep-sleep   | ON              | OFF                  | OFF | OFF    | OFF         | OFF      | OFF    |

**Note:**

1. For power consumption data, please refer to [ESP32-P4 Datasheet](#) > Section *Current Consumption*.
2. For supported wake-up sources, please refer to Table 13.4-1.

## 13.6 Event Task Matrix Feature

The low-power management system on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows the low-power management system's ETM tasks to be triggered by any peripherals' ETM events, or the low-power management system's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to the low-power management system. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

The low-power management system can receive the following ETM tasks:

- PMU\_TASK\_SLEEP\_REQ: Triggers PMU's sleep process.

The low-power management system can generate the following ETM events:

- PMU\_EVT\_SLEEP\_WAKEUP: Indicates that PMU is woken up to the HP\_ACTIVE state.

## 13.7 Interrupts

ESP32-P4's low-power management system can generate the following interrupt signals:

- PMU\_INTR
- PMU\_LP\_INT



Among these interrupt signals, PMU\_INTR is sent to the [Interrupt Matrix](#), while PMU\_LP\_INT is sent to the LP CPU.

The interrupt signals are generated by the internal interrupt sources of each module, specifically:

PMU\_INTR:

- PMU\_SOC\_WAKEUP\_INT: Triggered when the chip is woken up to the HP\_ACTIVE state.
- PMU\_SOC\_SLEEP\_REJECT\_INT: Triggered when a sleep-rejection source rejects a sleep request.
- PMU\_SW\_INT: Triggered when LP CPU is used as a wake-up source and wakes up the chip to HP\_ACTIVE state.
- PMU\_SDIO\_IDLE\_INT: Triggered when SDIO is in idle state.
- PMU\_LP\_CPU\_EXC\_INT: Triggered when there are LP CPU exceptions.
- PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_INT: Triggered when VO4 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_INT: Triggered when VO4 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET1\_REACH\_0\_INT: Triggered when VO3 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET0\_REACH\_0\_INT: Triggered when VO3 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_INT: Triggered when VO2 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_INT: Triggered when VO2 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET1\_REACH\_0\_INT: Triggered when VO1 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET0\_REACH\_0\_INT: Triggered when VO1 regulator's waiting counter target 0 reaches timeout.

PMU\_LP\_INT:

- PMU\_LP\_CPU\_SLEEP\_REJECT\_INT: Triggered when the LP sleep request is rejected.
- PMU\_HP\_SW\_TRIGGER\_INT: Triggered when HP CPU wakes up LP CPU.
- PMU\_ACTIVE\_SWITCH\_SLEEP\_START\_INT: Triggered when the PMU state starts to switch from HP\_ACTIVE to HP\_SLEEP.
- PMU\_SLEEP\_SWITCH\_ACTIVE\_START\_INT: Triggered when the PMU state starts to switch from HP\_SLEEP to HP\_ACTIVE.
- PMU\_ACTIVE\_SWITCH\_SLEEP\_END\_INT: Triggered when the PMU state finishes switching from HP\_ACTIVE to HP\_SLEEP.
- PMU\_SLEEP\_SWITCH\_ACTIVE\_END\_INT: Triggered when the PMU state finishes switching from HP\_SLEEP to HP\_ACTIVE.

- PMU\_LP\_CPU\_WAKEUP\_INT: Triggered when LP CPU is woken up.
- PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_LP\_INT: Triggered when VO4 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_LP\_INT: Triggered when VO4 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET1\_REACH\_0\_LP\_INT: Triggered when VO3 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP2A\_CNT\_TARGET0\_REACH\_0\_LP\_INT: Triggered when VO3 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_LP\_INT: Triggered when VO2 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_LP\_INT: Triggered when VO2 regulator's waiting counter target 0 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET1\_REACH\_0\_LP\_INT: Triggered when VO1 regulator's waiting counter target 1 reaches timeout.
- PMU\_OP1A\_CNT\_TARGET0\_REACH\_0\_LP\_INT: Triggered when VO1 regulator's waiting counter target 0 reaches timeout.

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [13.8 Register Summary](#).

## 13.8 Register Summary

The addresses in this section are relative to the PMU base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Configuration Registers</b>                  |   |         |        |
| <a href="#">PMU_HP_ACTIVE_DIG_POWER_REG</a>     | Digital power domain control register in HP_ACTIVE state                  | 0x0000  | R/W    |
| <a href="#">PMU_HP_ACTIVE_ICG_HP_FUNC_REG</a>   | HP system peripheral's function clock control register in HP_ACTIVE state | 0x0004  | R/W    |
| <a href="#">PMU_HP_ACTIVE_HP_SYS_CNTL_REG</a>   | System control register in HP_ACTIVE state                                | 0x0010  | R/W    |
| <a href="#">PMU_HP_ACTIVE_HP_CK_POWER_REG</a>   | Clock source power control register in HP_ACTIVE state                    | 0x0014  | R/W    |
| <a href="#">PMU_HP_ACTIVE_BIAS_REG</a>          | BIAS control register in HP_ACTIVE state                                  | 0x0018  | R/W    |
| <a href="#">PMU_HP_ACTIVE_BACKUP_REG</a>        | Backup module control register in HP_ACTIVE state                         | 0x001C  | R/W    |
| <a href="#">PMU_HP_ACTIVE_BACKUP_CLK_REG</a>    | Backup module's function clock control register in HP_ACTIVE state        | 0x0020  | R/W    |
| <a href="#">PMU_HP_ACTIVE_SYSCLK_REG</a>        | System clock control register in HP_ACTIVE state                          | 0x0024  | R/W    |
| <a href="#">PMU_HP_ACTIVE_HP_REGULATORO_REG</a> | Regulator power control register in HP_ACTIVE state                       | 0x0028  | varies |
| <a href="#">PMU_HP_ACTIVE_XTAL_REG</a>          | XTAL_CLK power control register in HP_ACTIVE state                        | 0x0030  | R/W    |
| <a href="#">PMU_HP_SLEEP_DIG_POWER_REG</a>      | Digital power domain control register in HP_SLEEP state                   | 0x0068  | R/W    |
| <a href="#">PMU_HP_SLEEP_ICG_HP_FUNC_REG</a>    | HP system peripheral's function clock control register in HP_SLEEP state  | 0x006C  | R/W    |
| <a href="#">PMU_HP_SLEEP_HP_SYS_CNTL_REG</a>    | System control register in HP_SLEEP state                                 | 0x0078  | R/W    |
| <a href="#">PMU_HP_SLEEP_HP_CK_POWER_REG</a>    | Clock source power control register in HP_SLEEP state                     | 0x007C  | R/W    |
| <a href="#">PMU_HP_SLEEP_BIAS_REG</a>           | BIAS control register in HP_SLEEP state                                   | 0x0080  | R/W    |
| <a href="#">PMU_HP_SLEEP_BACKUP_REG</a>         | Backup module control register in HP_SLEEP state                          | 0x0084  | R/W    |
| <a href="#">PMU_HP_SLEEP_BACKUP_CLK_REG</a>     | Backup module's function clock control register in HP_SLEEP state         | 0x0088  | R/W    |
| <a href="#">PMU_HP_SLEEP_SYSCLK_REG</a>         | System clock control register in HP_SLEEP state                           | 0x008C  | R/W    |
| <a href="#">PMU_HP_SLEEP_HP_REGULATORO_REG</a>  | Regulator power control register in HP_SLEEP state                        | 0x0090  | R/W    |

| Name   | Description  | Address | Access   |
|--|--|---------|----------|
| <a href="#">PMU_HP_SLEEP_XTAL_REG</a>          | XTAL_CLK power control register in HP_SLEEP state                  | 0x0098  | R/W      |
| <a href="#">PMU_HP_SLEEP_LP_REGULATOR0_REG</a> | LP sys regulator control register in HP_SLEEP state                | 0x009C  | R/W      |
| <a href="#">PMU_HP_SLEEP_LP_DIG_POWER_REG</a>  | LP system digital power domains control register in HP_SLEEP state | 0x00A8  | R/W      |
| <a href="#">PMU_HP_SLEEP_LP_CK_POWER_REG</a>   | Low-speed clock power control register in HP_ACTIVE/HP_SLEEP state | 0x00AC  | R/W      |
| <a href="#">PMU_LP_SLEEP_LP_REGULATOR0_REG</a> | LP sys regulator control register in HP_SLEEP state                | 0x00B4  | R/W      |
| <a href="#">PMU_LP_SLEEP_XTAL_REG</a>          | XTAL_CLK power control register in LP_SLEEP state                  | 0x00BC  | R/W      |
| <a href="#">PMU_LP_SLEEP_LP_DIG_POWER_REG</a>  | Digital power domain control register in LP_SLEEP state            | 0x00C0  | R/W      |
| <a href="#">PMU_LP_SLEEP_LP_CK_POWER_REG</a>   | Low-speed clock power control register in LP_SLEEP state           | 0x00C4  | R/W      |
| <a href="#">PMU_IMM_HP_CK_POWER_REG</a>        | Software control register for clock power                          | 0x00CC  | WT       |
| <a href="#">PMU_IMM_SLEEP_SYSCLK_REG</a>       | Software control register for system clock                         | 0x00D0  | WT       |
| <a href="#">PMU_IMM_HP_FUNC_ICG_REG</a>        | Software control register for peripheral clock                     | 0x00D4  | WT       |
| <a href="#">PMU_IMM_HP_APB_ICG_REG</a>         | Software control register for APB clock                            | 0x00D8  | WT       |
| <a href="#">PMU_IMM_PAD_HOLD_ALL_REG</a>       | Software control register for PAD hold function                    | 0x00E4  | varies   |
| <a href="#">PMU_POWER_CK_WAIT_CNTL_REG</a>     | Clock gating wait time configuration register                      | 0x011C  | R/W      |
| <a href="#">PMU_SLP_WAKEUP_CNTL0_REG</a>       | Sleep request register   | 0x0120  | WT       |
| <a href="#">PMU_SLP_WAKEUP_CNTL1_REG</a>       | Sleep reject register  | 0x0124  | R/W      |
| <a href="#">PMU_SLP_WAKEUP_CNTL2_REG</a>       | Wake up source enable register                                     | 0x0128  | R/W      |
| <a href="#">PMU_SLP_WAKEUP_CNTL3_REG</a>       | Minimum sleep time control register                                | 0x012C  | R/W      |
| <a href="#">PMU_SLP_WAKEUP_CNTL4_REG</a>       | Sleep reject cause clear register                                  | 0x0130  | WT       |
| <a href="#">PMU_SLP_WAKEUP_STATUS0_REG</a>     | Wake up cause register   | 0x0144  | RO       |
| <a href="#">PMU_SLP_WAKEUP_STATUS1_REG</a>     | Reset reject cause register  | 0x0148  | RO       |
| <a href="#">PMU_HP_CK_CNTL_REG</a>             | HP system clock control register                                   | 0x0154  | R/W      |
| <a href="#">PMU_RF_PWC_REG</a>                 | SAR ADC power up register  | 0x015C  | R/W      |
| <a href="#">PMU_INT_RAW_REG</a>                | PMU sleep/wake-up raw interrupt                                    | 0x0164  | R/WTC/SS |
| <a href="#">PMU_HP_INT_ST_REG</a>              | PMU sleep/wake-up state interrupt                                  | 0x0168  | RO       |
| <a href="#">PMU_HP_INT_ENA_REG</a>             | PMU sleep/wake-up interrupt enable register                        | 0x016C  | R/W      |
| <a href="#">PMU_HP_INT_CLR_REG</a>             | PMU sleep/wake-up interrupt clear register                         | 0x0170  | WT       |
| <a href="#">PMU_LP_INT_RAW_REG</a>             | PMU sleep/wake-up raw interrupt                                    | 0x0174  | R/WTC/SS |
| <a href="#">PMU_LP_INT_ST_REG</a>              | PMU sleep/wake-up state interrupt                                  | 0x0178  | RO       |

| Name  | Description                                 | Address | Access |
|---|---|---------|--------|
| <a href="#">PMU_LP_INT_ENA_REG</a>          | PMU sleep/wake-up interrupt enable register | 0x017C  | R/W    |
| <a href="#">PMU_LP_INT_CLR_REG</a>          | PMU sleep/wake-up interrupt clear register  | 0x0180  | varies |
| <a href="#">PMU_LP_CPU_PWR0_REG</a>         | LP CPU sleep/wake-up control register       | 0x0184  | varies |
| <a href="#">PMU_LP_CPU_PWR1_REG</a>         | LP CPU sleep/wake-up control register       | 0x0188  | WT     |
| <a href="#">PMU_LP_CPU_PWR2_REG</a>         | LP CPU sleep/wake-up control register       | 0x018C  | R/W    |
| <a href="#">PMU_LP_CPU_PWR3_REG</a>         | LP CPU sleep/wake-up control register       | 0x0190  | RO     |
| <a href="#">PMU_LP_CPU_PWR4_REG</a>         | LP CPU sleep/wake-up control register       | 0x0194  | R/W    |
| <a href="#">PMU_LP_CPU_PWR5_REG</a>         | LP CPU sleep/wake-up control register       | 0x0198  | RO     |
| <a href="#">PMU_HP_LP_CPU_COMM_REG</a>      | LP CPU sleep/wake-up control register       | 0x019C  | WT     |
| <a href="#">PMU_EXT_LDO_PO_OP1A_REG</a>     | VO1 regulator control register              | 0x01B8  | R/W    |
| <a href="#">PMU_EXT_LDO_PO_OP1A_ANA_REG</a> | VO1 regulator control register              | 0x01BC  | R/W    |
| <a href="#">PMU_EXT_LDO_PO_OP2A_REG</a>     | VO2 regulator control register              | 0x01C0  | R/W    |
| <a href="#">PMU_EXT_LDO_PO_OP2A_ANA_REG</a> | VO2 regulator control register              | 0x01C4  | R/W    |
| <a href="#">PMU_EXT_LDO_P1_OP1A_REG</a>     | VO3 regulator control register              | 0x01D0  | R/W    |
| <a href="#">PMU_EXT_LDO_P1_OP1A_ANA_REG</a> | VO3 regulator control register              | 0x01D4  | R/W    |
| <a href="#">PMU_EXT_LDO_P1_OP2A_REG</a>     | VO4 regulator control register              | 0x01D8  | R/W    |
| <a href="#">PMU_EXT_LDO_P1_OP2A_ANA_REG</a> | VO4 regulator control register              | 0x01DC  | R/W    |
| <a href="#">PMU_EXT_WAKEUP_LV_REG</a>       | EXT wake-up level control register          | 0x01E8  | R/W    |
| <a href="#">PMU_EXT_WAKEUP_SEL_REG</a>      | EXT wake-up IO control register             | 0x01EC  | R/W    |
| <a href="#">PMU_EXT_WAKEUP_ST_REG</a>       | EXT wake-up status register                 | 0x01F0  | RO     |
| <a href="#">PMU_EXT_WAKEUP_CNTL_REG</a>     | EXT wake-up control register                | 0x01F4  | R/W    |
| <a href="#">PMU_SDIO_WAKEUP_CNTL_REG</a>    | SDIO wake-up control register               | 0x01F8  | R/W    |
| <a href="#">PMU_TOUCH_PWR_CNTL_REG</a>      | TOUCH sleep/wake-up control register        | 0x0210  | R/W    |
| <a href="#">PMU_DATE_REG</a>                | Version control register                    | 0x03FC  | R/W    |

## 13.9 Registers

The addresses in this section are relative to the PMU base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

### Register 13.1. PMU HP ACTIVE DIG POWER REG (0x0000)

[illegible]

|  |  |
|--|--|
| <b>PMU_HP_ACTIVE_DCDC_SWITCH_PD_EN</b> | Configures whether to cut off the power from external DCDC in HP_ACTIVE state.<br>0: Do not cut off<br>1: Cut off<br>(R/W) |
|--|--|

**PMU\_HP\_ACTIVE\_HP\_MEM\_DSLP** Configures whether to put L2MEM\_G0-G5 into Deep-sleep mode in HP\_ACTIVE state.

0: Do not put L2MEM\_G0-G5 into Deep-sleep

1: Put L2MEM\_G0-G5 into Deep-sleep

(R/W)

**PMU\_HP\_ACTIVE\_PD\_HP\_MEM\_PD\_EN** Configures whether to power down L2MEM\_GO-G5 in HP\_ACTIVE state.

0: Power up

1: Power down

(R/W)

**PMU\_HP\_ACTIVE\_PD\_CNNT\_PD\_EN** Configures whether to power down HP\_CNNT in HP\_ACTIVE state.

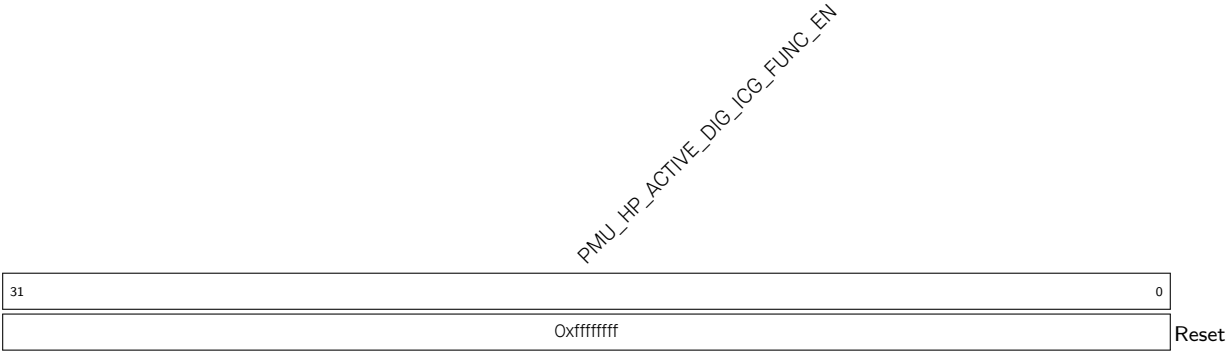
0: Power up

1: Power down

(R/W)

|                                   |   |
|-----------------------------------|---|
| <b>PMU_HP_ACTIVE_PD_TOP_PD_EN</b> | Configures whether to power down PD_TOP power domain in HP_ACTIVE state.<br>0: Power up<br>1: Power down<br>(R/W) |
|-----------------------------------|---|

Register 13.2. PMU\_HP\_ACTIVE\_ICG\_HP\_FUNC\_REG (0x0004)



**PMU\_HP\_ACTIVE\_DIG\_ICG\_FUNC\_EN** Configures whether to enable HP system peripheral's function clock in HP\_ACTIVE state. For detailed configuration please see Table 13.4-2.

0: Disable

1: Enable

(R/W)

### Register 13.3. PMU\_HP\_ACTIVE\_HP\_SYS\_CNTL\_REG (0x0010)

Diagram illustrating the PMU\_CTL register structure. The register is 32 bits wide, with bits 31 down to 23 labeled as (reserved). Bits 22 down to 0 are labeled with various PMU control signals: PMU\_HP\_ACTIVE\_DIG\_CPU\_STALL, PMU\_HP\_ACTIVE\_DIG\_PAUSE\_WDT, PMU\_HP\_ACTIVE\_DIG\_PAD\_SLP\_SEL, PMU\_HP\_ACTIVE\_LP\_PAD\_HOLD\_ALL, and PMU\_HP\_ACTIVE\_UART\_WAKEUP\_EN. A 'Reset' label is at the bottom right.

**PMU\_HP\_ACTIVE\_UART\_WAKEUP\_EN** Configures whether to enable UART wake up function in HP\_ACTIVE state.

0: Disable wake-up function

## 1: Enable wake-up function

(R/W)

**PMU\_HP\_ACTIVE\_LP\_PAD\_HOLD\_ALL** Configures whether to hold LP GPIO's configuration in HP\_ACTIVE state.

0: Do not hold

1: Hold

(R/W)

**PMU\_HP\_ACTIVE\_HP\_PAD\_HOLD\_ALL** Configures whether to hold GPIO's configuration in HP\_ACTIVE state.

0: Do not hold

1: Hold

(R/W)

**PMU\_HP\_ACTIVE\_DIG\_PAD\_SLP\_SEL** Configures whether to use Light-sleep mode configuration for GPIO in HP\_ACTIVE state.

0: Use normal configuration

1: Use Light-sleep mode configuration. For details please refer to Chapter 8 *GPIO Matrix and IO MUX* > Section 8.8 *Pin Functions in Light-sleep*.

(R/W)

**PMU\_HP\_ACTIVE\_DIG\_PAUSE\_WDT** Configures whether to pause watchdog in HP\_ACTIVE state.

0: Do not pause

1: Pause

(R/W)

**PMU\_HP\_ACTIVE\_DIG\_CPU\_STALL** Configures whether to stall the CPU in HP\_ACTIVE state.

0: Do not stall

1: Stall

(R/W)



#### Register 13.4. PMU\_HP\_ACTIVE\_HP\_CK\_POWER\_REG (0x0014)

[illegible]

**PMU\_HP\_ACTIVE\_I2C\_ISO\_EN** Configure whether to power up ANALOG\_I2C in HP\_ACTIVE state.

0: Power down

1: Power up

(R/W)

**PMU\_HP\_ACTIVE\_I2C\_RETENTION** Configures whether to enable ANALOG\_I2C retention status in HP ACTIVE state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_ACTIVE\_XPD\_PLL\_I2C** Configures whether to enable PLL I2C controllers in HP\_ACTIVE state. Each bit controls a PLL I2C register group.

0: Disable

1: Enable

(R/W)

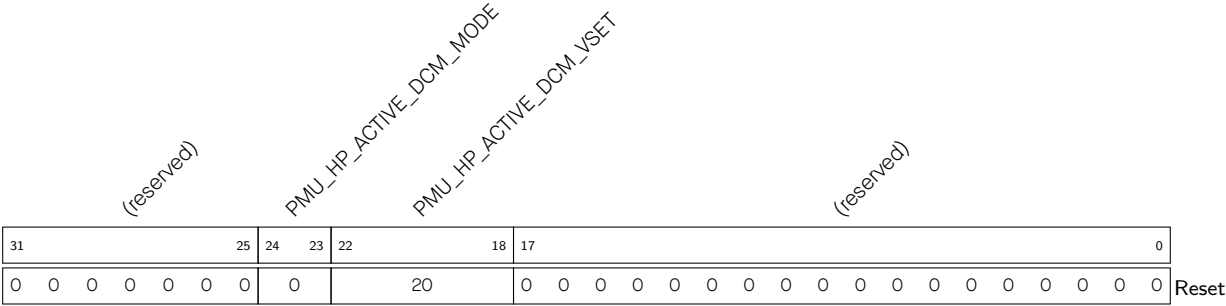
**PMU\_HP\_ACTIVE\_XPD\_PLL** Configures whether to enable the analog power domains in HP system in HP\_ACTIVE state. Bit 0 controls CPLL\_CLK, bit 1 controls SPPL\_CLK, bit 2 controls Audio PLL, bit 3 controls SDIO PLL.

0: Disable

1: Enable

(R/W)

Register 13.5. PMU\_HP\_ACTIVE\_BIAS\_REG (0x0018)



**PMU\_HP\_ACTIVE\_DCM\_VSET** Regulates the DCDC voltage in HP\_ACTIVE state. (R/W)

**PMU\_HP\_ACTIVE\_DCM\_MODE** Configures whether to enable DCDC status in HP\_ACTIVE state.

- 0: Disable
- 1: Enable
- 2, 3: Reserved

(R/W)

### Register 13.6. PMU\_HP\_ACTIVE\_BACKUP\_REG (0x001C)

[illegible]

**PMU\_HP\_SLEEP2ACTIVE\_BACKUP\_CLK\_SEL** Configures the backup module's function clock source when PMU state switches from HP\_SLEEP to HP\_ACTIVE.

0: Select XTAL

1: Select PLL CLK

2: Select RC FAST CLK

3: Invalid value

(R/W)

**PMU\_HP\_SLEEP2ACTIVE\_BACKUP\_MODE** Configures the backup direction and link list when PMU state switches switch from HP\_SLEEP to HP\_ACTIVE.

Highest bit:

0: From peripheral to memory

1: From memory to peripheral

Lower two bits:

0: PAU\_LINK\_ADDR\_0

1: PAU\_LINK\_ADDR\_1

2: PAU\_LINK\_ADDR\_2

3: PAU\_LINK\_ADDR\_3

(R/W)

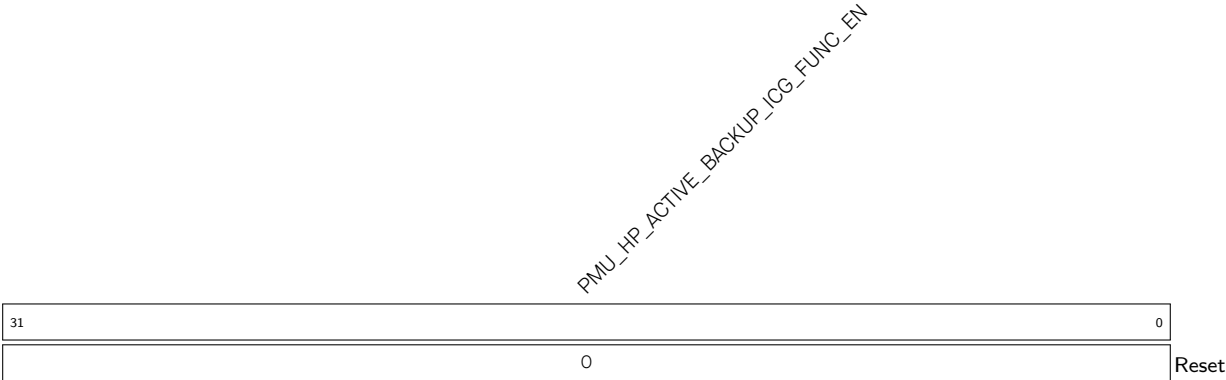
**PMU\_HP\_SLEEP2ACTIVE\_BACKUP\_EN** Configures whether to enable the backup flow when PMU state switches from HP\_SLEEP to HP\_ACTIVE.

0: Disable backup

### 1: Enable backup

(R/W)

Register 13.7. PMU\_HP\_ACTIVE\_BACKUP\_CLK\_REG (0x0020)



**PMU\_HP\_ACTIVE\_BACKUP\_ICG\_FUNC\_EN** Configures whether to enable each peripheral's function clock when the target state is HP\_ACTIVE. For details, please refer to Table 13.4-2.

0: Disable

1: Enable

(R/W)

### Register 13.8. PMU\_HP\_ACTIVE\_SYSCLK\_REG (0x0024)

[illegible]

**PMU\_HP\_ACTIVE\_ICG\_SYS\_CLOCK\_EN** Configures whether to enable ROOT\_CLK in HP\_ACTIVE state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_ACTIVE\_SYS\_CLK\_SLP\_SEL** Configures whether to allow PMU to control clock source in HP ACTIVE state.

0: Controlled by PCR registers

1: Controlled by PMU

(R/W)

**PMU\_HP\_ACTIVE\_ICG\_SLP\_SEL** Configures whether to allow PMU to control the clock gating in HP ACTIVE state.

0: Controlled by PCR registers

1: Controlled by PMU

(R/W)

**PMU\_HP\_ACTIVE\_DIG\_SYS\_CLK\_SEL** Configures the source of ROOT\_CLK in HP\_ACTIVE state.

O: XTAL

1: PLL CLK

2: RC\_FAST\_CLK

3: Invalid value

(R/W)

### Register 13.9. PMU\_HP\_ACTIVE\_HP\_REGULATOR0\_REG (0x0028)

|                                  |    |    |    |            |    |    |    |                                 |    |    |    |            |   |   |   |                                |   |    |   |            |   |   |   |                    |   |   |   |                              |   |   |   |            |    |   |   |                  |   |       |  |            |  |  |  |                  |  |  |  |            |  |  |  |
|----------------------------------|----|----|----|------------|----|----|----|---------------------------------|----|----|----|------------|---|---|---|--------------------------------|---|----|---|------------|---|---|---|--------------------|---|---|---|------------------------------|---|---|---|------------|----|---|---|------------------|---|-------|--|------------|--|--|--|------------------|--|--|--|------------|--|--|--|
| PMU_HP_ACTIVE_HP_REGULATOR_DBIAS |    |    |    | (reserved) |    |    |    | PMU_HP_ACTIVE_REGULATOR_VO1_XPD |    |    |    | (reserved) |   |   |   | PMU_HP_ACTIVE_HP_REGULATOR_XPD |   |    |   | (reserved) |   |   |   | PMU_DIG_DBIAS_INIT |   |   |   | PMU_DIG_REGULATORO_DBIAS_SEL |   |   |   | (reserved) |    |   |   | PMU_HP_DBIAS_VOL |   |       |  | (reserved) |  |  |  | PMU_LP_DBIAS_VOL |  |  |  | (reserved) |  |  |  |
| 31                               | 27 | 26 | 23 | 22         | 21 | 19 | 18 | 17                              | 16 | 15 | 14 | 13         | 9 | 8 | 4 | 3                              | 0 | 24 | 0 | 0          | 0 | 0 | 1 | 0                  | 0 | 0 | 1 | 0                            | 0 | 0 | 1 | 24         | 24 | 0 | 0 | 0                | 0 | Reset |  |            |  |  |  |                  |  |  |  |            |  |  |  |

**PMU\_LP\_DBIAS\_VOL** Indicates the current voltage of the LP system regulator. (RO)

**PMU\_HP\_DBIAS\_VOL** Indicates the current voltage of the HP system regulator. (RO)

**PMU\_DIG\_REGULATORO\_DBIAS\_SEL** Configures which of the following regulates the HP system regulator voltage.

0: Regulated by Hardware automatically

## 1: Regulated by Software

(R/W)

**PMU\_DIG\_DBIAS\_INIT** Initializes the PVT voltage configurations. (WT)

**PMU\_HP\_ACTIVE\_HP\_REGULATOR\_XPD** Configures whether to enable the HP sys regulator in HP ACTIVE state.

0: Disable the HP sys regulator

### 1: Enable the HP sys regulator

(R/W)

**PMU\_HP\_ACTIVE\_REGULATOR\_VO1\_XPD** Configures whether to enable VO1 regulator in HP\_ACTIVE state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_ACTIVE\_HP\_REGULATOR\_DBIAS** Regulates the voltage of the HP sys regulator in HP\_ACTIVE state. The higher the value, the higher the voltage. (R/W)

PMU\_HP\_ACTIVE\_XPD\_XTAL

(reserved)

[illegible]

(R/W)

### Register 13.11. PMU\_HP\_SLEEP\_DIG\_POWER\_REG (0x0068)

[illegible]

**PMU\_HP\_SLEEP\_DCDC\_SWITCH\_PD\_EN** Configures whether to cut off the power from external DCDC in HP SLEEP state.

0: Do not cut off

1: Cut off

(R/W)

**PMU\_HP\_SLEEP\_HP\_MEM\_DSLP** Configures whether to put L2MEM\_G0-G5 into Deep-sleep mode in HP\_SLEEP state.

0: Do not put L2MEM\_G0-G5 into Deep-sleep

1: Put L2MEM\_G0-G5 into Deep-sleep

(R/W)

**PMU\_HP\_SLEEP\_PD\_HP\_MEM\_PD\_EN** Configures whether to power down L2MEM\_G0-G5 in HP SLEEP state.

0: Power up

1: Power down

(R/W)

**PMU\_HP\_SLEEP\_PD\_CNNT\_PD\_EN** Configures whether to power down HP\_CNNT in HP\_SLEEP state.

0: Power up

1: Power down

(R/W)

**PMU\_HP\_SLEEP\_PD\_TOP\_PD\_EN** Configures whether to power down PD\_TOP power domain in HP SLEEP state.

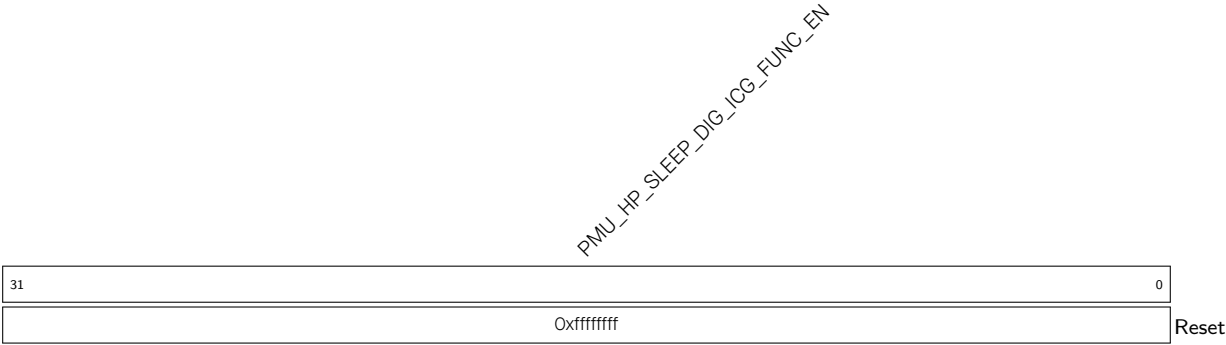
0: Power up

1: Power down

(R/W)



Register 13.12. PMU\_HP\_SLEEP\_ICG\_HP\_FUNC\_REG (0x006C)



**PMU\_HP\_SLEEP\_DIG\_ICG\_FUNC\_EN** Configures whether to enable HP system peripheral's function clock in HP\_SLEEP state. For detailed configuration please see Table 13.4-2.

0: Disable

1: Enable

(R/W)

### Register 13.13. PMU\_HP\_SLEEP\_HP\_SYS\_CNTL\_REG (0x0078)

[illegible]

**PMU\_HP\_SLEEP\_UART\_WAKEUP\_EN** Configures whether to enable UART wake up function in HP SLEEP state.

0: Disable wake-up function

### 1: Enable wake-up function

(R/W)

**PMU\_HP\_SLEEP\_LP\_PAD\_HOLD\_ALL** Configures whether to hold LP GPIO's configuration in HP SLEEP state.

0: Do not hold

1: Hold

(R/W)

**PMU\_HP\_SLEEP\_HP\_PAD\_HOLD\_ALL** Configures whether to hold GPIO's configuration in HP SLEEP state.

0: Do not hold

1: Hold

(R/W)

**PMU\_HP\_SLEEP\_DIG\_PAD\_SLP\_SEL** Configures whether to use Light-sleep mode configuration for GPIO in HP\_SLEEP state.

0: Use normal configuration

1: Use Light-sleep mode configuration. For details please refer to Chapter 8 *GPIO Matrix and IO MUX* > Section 8.8 *Pin Functions in Light-sleep*.

(R/W)

**PMU\_HP\_SLEEP\_DIG\_PAUSE\_WDT** Configures whether to pause watchdog in HP\_SLEEP state.

0: Do not pause

1: Pause

(R/W)

**PMU\_HP\_SLEEP\_DIG\_CPU\_STALL** Configures whether to stall the CPU in HP\_SLEEP state.

0: Do not stall

1: Stall

(R/W)

### Register 13.14. PMU\_HP\_SLEEP\_HP\_CK\_POWER\_REG (0x007C)

[illegible]

**PMU\_HP\_SLEEP\_I2C\_ISO\_EN** Configure whether to power up ANALOG\_I2C in HP\_SLEEP state.

0: Power down

1: Power up

(R/W)

**PMU\_HP\_SLEEP\_I2C\_RETENTION** Configures whether to enable ANALOG\_I2C retention status in HP SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_XPD\_PLL\_I2C** Configures whether to enable PLL I2C controllers in HP\_SLEEP state. Each bit controls a PLL I2C register group.

0: Disable

1: Enable

(R/W)

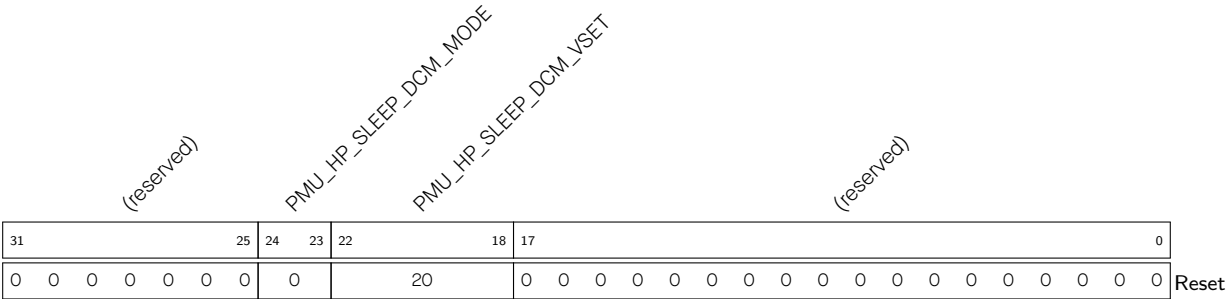
**PMU\_HP\_SLEEP\_XPD\_PLL** Configures whether to enable the analog power domains in HP system in HP\_SLEEP state. Bit 0 controls CPLL\_CLK, bit 1 controls SPPLL\_CLK, bit 2 controls Audio PLL, bit 3 controls SDIO PLL.

0: Disable

1: Enable

(R/W)

Register 13.15. PMU\_HP\_SLEEP\_BIAS\_REG (0x0080)



PMU\_HP\_SLEEP\_DCM\_VSET   Regulates the DCDC voltage in HP\_SLEEP state. (R/W)

PMU\_HP\_SLEEP\_DCM\_MODE   Configures whether to enable DCDC status in HP\_SLEEP state.

0: Disable  
1: Enable  
2, 3: Reserved  
(R/W)

**Register 13.16. PMU\_HP\_SLEEP\_BACKUP\_REG (0x0084)**

|   |    |    |    |   |    |    |    |  |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|---|----|----|----|--|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| PMU_HP_ACTIVE2SLEEP_BACKUP_EN<br>(reserved) |    |    |    | PMU_HP_ACTIVE2SLEEP_BACKUP_MODE<br>(reserved) |    |    |    | PMU_HP_ACTIVE2SLEEP_BACKUP_CLK_SEL<br>(reserved) |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 28 | 26  | 25 | 20 | 19 | 18   | 17 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0   | 0  | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PMU\_HP\_ACTIVE2SLEEP\_BACKUP\_CLK\_SEL** Configures the backup module function clock source when PMU state switches from HP\_ACTIVE to HP\_SLEEP.

0: Select XTAL

1: Select PLL\_CLK

2: Select RC\_FAST\_CLK

3: Invalid value

(R/W)

**PMU\_HP\_ACTIVE2SLEEP\_BACKUP\_MODE** Configures the backup direction and link list when PMU state switches from HP\_ACTIVE to HP\_SLEEP.

Highest bit:

0: From memory to peripheral

1: From peripheral to memory

Lower two bits:

0: PAU\_LINK\_ADDR\_0

1: PAU\_LINK\_ADDR\_1

2: PAU\_LINK\_ADDR\_2

3: PAU\_LINK\_ADDR\_3

(R/W)

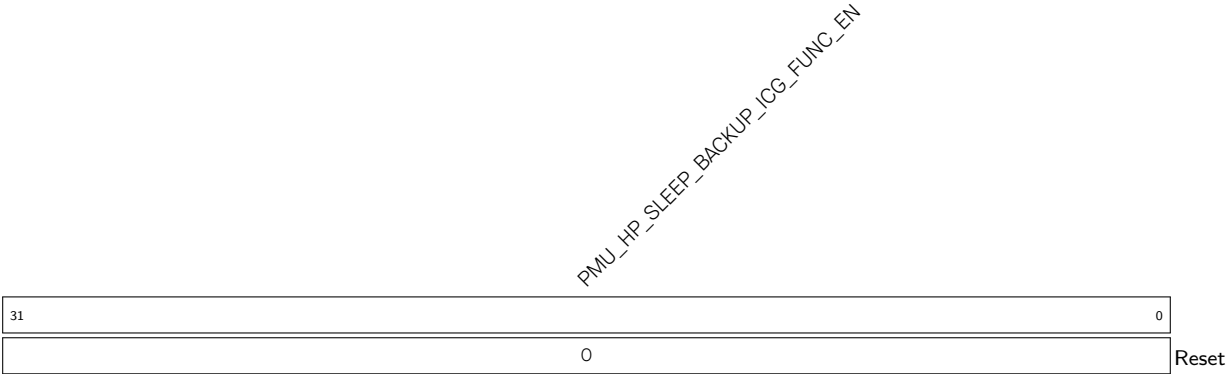
**PMU\_HP\_ACTIVE2SLEEP\_BACKUP\_EN** Configures whether to enable the backup flow when PMU state switches from HP\_ACTIVE to HP\_SLEEP.

0: Disable backup

1: Enable backup

(R/W)

Register 13.17. PMU\_HP\_SLEEP\_BACKUP\_CLK\_REG (0x0088)



**PMU\_HP\_SLEEP\_BACKUP\_ICG\_FUNC\_EN** Configures whether to enable each peripheral's function clock when the target state is HP\_SLEEP. For details, please refer to Table 13.4-2.

0: Disable

1: Enable

(R/W)

### Register 13.18. PMU\_HP\_SLEEP\_SYSCLK\_REG (0x008C)

Diagram illustrating the PMU\_HP\_SLEEP\_ICG\_SYS\_CLK\_SEL register structure. The register is 32 bits wide. Bits 31, 30, 29, and 28 are labeled PMU\_HP\_SLEEP\_ICG\_SYS\_CLK\_SEL. Bit 27 is labeled PMU\_HP\_SLEEP\_ICG\_SYS\_CLK\_SEL. Bit 26 is labeled PMU\_HP\_SLEEP\_ICG\_SYS\_CLK\_SEL. Bits 25 through 0 are labeled (reserved).

**PMU\_HP\_SLEEP\_ICG\_SYS\_CLOCK\_EN** Configures whether to enable ROOT\_CLK in HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_SYS\_CLK\_SLP\_SEL** Configures whether to allow PMU to control the clock source in HP\_SLEEP state.

0: Controlled by PCR registers

1: Controlled by PMU

(R/W)

**PMU\_HP\_SLEEP\_ICG\_SLP\_SEL** Configures whether to allow PMU to control the clock gating in HP SLEEP state.

0: Controlled by PCR registers

1: Controlled by PMU

(R/W)

**PMU\_HP\_SLEEP\_DIG\_SYS\_CLK\_SEL** Configures the source of ROOT\_CLK in HP\_SLEEP state.

O: XTAL

1: PLL\_CLK

2: RC\_FAST\_CLK

3: Invalid value

(R/W)

Register 13.19. PMU\_HP\_SLEEP\_HP\_REGULATORO\_REG (0x0090)

|                                 |    |    |    |            |    |    |    |                                |   |   |   |            |   |   |   |                               |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------------------------|----|----|----|------------|----|----|----|--------------------------------|---|---|---|------------|---|---|---|-------------------------------|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|
| PMU_HP_SLEEP_HP_REGULATOR_DBIAS |    |    |    | (reserved) |    |    |    | PMU_HP_SLEEP_REGULATOR_VO1_XPD |   |   |   | (reserved) |   |   |   | PMU_HP_SLEEP_HP_REGULATOR_XPD |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   | 0 |
| 31                              | 27 | 26 | 23 | 22         | 21 | 19 | 18 | 17                             |   |   |   |            |   |   |   |                               |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |
| 24                              |    |    |    | 0          | 0  | 0  | 0  | 1                              | 0 | 0 | 0 | 1          | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**PMU\_HP\_SLEEP\_HP\_REGULATOR\_XPD** Configures whether to enable the HP sys regulator in HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_REGULATOR\_VO1\_XPD** Configures whether to enable VO1 regulator in HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_HP\_REGULATOR\_DBIAS** Regulates the voltage of the HP sys regulator in HP\_SLEEP state. The higher the value, the higher the voltage. (R/W)

Register 13.20. PMU\_HP\_SLEEP\_XTAL\_REG (0x0098)

|                       |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|-----------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMU_HP_SLEEP_XPD_XTAL |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |
| 31                    | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 1                     | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**PMU\_HP\_SLEEP\_XPD\_XTAL** Configures whether to enable XTAL\_CLK analog source in HP\_SLEEP state.

0: Disable

1: Enable

(R/W)



Register 13.21. PMU\_HP\_SLEEP\_LP\_REGULATORO\_REG (0x009C)

|                                 |    |    |    |            |    |   |   |                               |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|----|----|----|------------|----|---|---|-------------------------------|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| PMU_HP_SLEEP_LP_REGULATOR_DBIAS |    |    |    | (reserved) |    |   |   | PMU_HP_SLEEP_LP_REGULATOR_XPD |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31                              | 27 | 26 | 23 | 22         | 21 |   |   |                               |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 24                              |    |    |    | 0          | 0  | 0 | 0 | 1                             | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PMU\_HP\_SLEEP\_LP\_REGULATOR\_XPD** Configures whether to enable LP sys regulator in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_LP\_REGULATOR\_DBIAS** Regulates the voltage of the LP sys regulator in HP\_ACTIVE/HP\_SLEEP state. The higher the value, the higher the voltage. (R/W)

### Register 13.22. PMU\_HP\_SLEEP\_LP\_DIG\_POWER\_REG (0x00A8)

Diagram illustrating the structure of the **PMU\_SLEEP\_LP\_PAD\_SLP\_SEL** register. The register is 32 bits wide, with bits 31 down to 25 labeled as **PMU\_HP\_SLEEP\_PD\_LP\_PERI\_PD\_EN**, **PMU\_HP\_SLEEP\_LP\_MEM\_DSLP**, **PMU\_HP\_SLEEP\_VDDBAT\_MODE**, **PMU\_HP\_SLEEP\_BOD\_SOURCE\_SEL**, and **PMU\_HP\_SLEEP\_LP\_PAD\_SLP\_SEL**. Bits 24 down to 0 are labeled as **(reserved)**.

**PMU\_HP\_SLEEP\_LP\_PAD\_SLP\_SEL** Configures whether to enable LP GPIO function in HP ACTIVE/HP SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_BOD\_SOURCE\_SEL** Configures whether to enable brown-out detection in HP\_ACTIVE/HP\_SLEEP. (R/W)

**PMU\_HP\_SLEEP\_VDDBAT\_MODE** Configures whether to enable VBAT power in HP ACTIVE/HP SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_LP\_MEM\_DSLP** Configures whether to enable Memory Deep-sleep mode for the LP SRAM in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_PD\_LP\_PERI\_PD\_EN** Configures whether to power down LP PD Peripherals in HP ACTIVE/HP SLEEP state.

0: Power up

1: Power down

(R/W)

**Register 13.23. PMU\_HP\_SLEEP\_LP\_CLK\_POWER\_REG (0x00AC)**

|   |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div><div>PMU_HP_SLEEP_PD_OSC_CLK<br/>PMU_HP_SLEEP_XPD_FOSC_CLK<br/>PMU_HP_SLEEP_XPD_RC32K<br/>PMU_HP_SLEEP_XPD_XTAL32K<br/>PMU_HP_SLEEP_XPD_LPPLL</div><div>(reserved)</div></div> |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 28 | 27 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 0   | 1  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PMU\_HP\_SLEEP\_XPD\_LPPLL** Configures whether to enable PLL\_LP\_CLK in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_XPD\_XTAL32K** Configures whether to enable XTAL32K\_CLK in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_XPD\_RC32K** Configures whether to enable RC32K\_CLK in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_HP\_SLEEP\_XPD\_FOSC\_CLK** Configures whether to enable RC\_FAST\_CLK in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

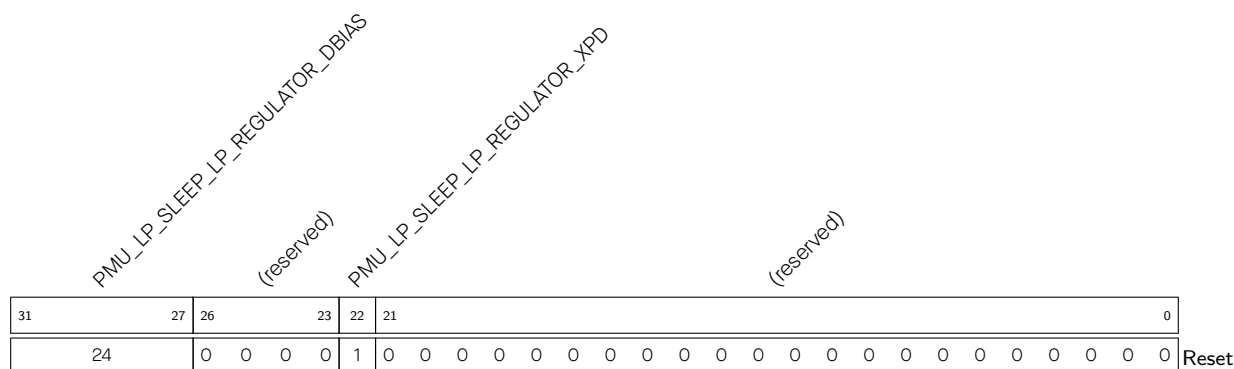
**PMU\_HP\_SLEEP\_PD\_OSC\_CLK** Configures whether to enable RC\_SLOW\_CLK in HP\_ACTIVE/HP\_SLEEP state.

0: Disable

1: Enable

(R/W)

### Register 13.24. PMU\_LP\_SLEEP\_LP\_REGULATOR0\_REG (0x00B4)



**PMU\_LP\_SLEEP\_LP\_REGULATOR\_XPD** Configures whether to enable the LP sys regulator in LP\_SLEEP state.

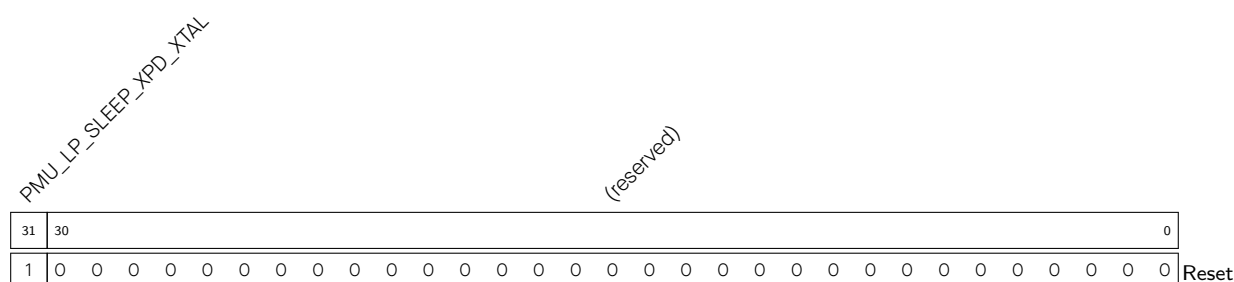
0: Disable

1: Enable

(R/W)

**PMU\_LP\_SLEEP\_LP\_REGULATOR\_DBIAS** Regulates the voltage of the LP sys regulator in LP\_SLEEP state. The higher the value, the higher the voltage. (R/W)

### Register 13.25. PMU\_LP\_SLEEP\_XTAL\_REG (0x00BC)



**PMU\_LP\_SLEEP\_XPD\_XTAL** Configures whether to enable XTAL\_CLK analog source in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

### Register 13.26. PMU\_LP\_SLEEP\_LP\_DIG\_POWER\_REG (0x00C0)

[illegible]

|                             |  |
|-----------------------------|--|
| PMU_LP_SLEEP_LP_PAD_SLP_SEL | Configures whether to enable LP GPIO function in LP_SLEEP state.<br>0: Disable<br>1: Enable<br>(R/W) |
|-----------------------------|--|

**PMU\_LP\_SLEEP\_BOD\_SOURCE\_SEL** Configures whether to enable brown-out detection in LP\_SLEEP state. (R/W)

|                                 |  |
|---------------------------------|--|
| <b>PMU_LP_SLEEP_VDDBAT_MODE</b> | Configures whether to enable VBAT power in LP_SLEEP state. |
| 0: Disable                      |  |
| 1: Enable                       |  |
| (R/W)                           |  |

|                                 |  |
|---------------------------------|--|
| <b>PMU_LP_SLEEP_LP_MEM_DSLP</b> | Configures whether to enable Memory Deep-sleep mode for the LP SRAM in LP_SLEEP state.<br>0: Disable<br>1: Enable<br>(R/W) |
|---------------------------------|--|

**PMU\_LP\_SLEEP\_PD\_LP\_PERI\_PD\_EN** Configures whether to power down LP PD Peripherals in LP\_SLEEP state.

0: Power up

1: Power down

(R/W)

### Register 13.27. PMU\_LP\_SLEEP\_LP\_CK\_POWER\_REG (0x00C4)

[illegible]

**PMU\_LP\_SLEEP\_XPD\_LPPLL** Configures whether to enable PLL\_LP\_CLK in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_LP\_SLEEP\_XPD\_XTAL32K** Configures whether to enable XTAL32K\_CLK in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_LP\_SLEEP\_XPD\_RC32K** Configures whether to enable RC32K\_CLK in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_LP\_SLEEP\_XPD\_FOSC\_CLK** Configures whether to enable RC\_FAST\_CLK in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

**PMU\_LP\_SLEEP\_PD\_OSC\_CLK** Configures whether to enable RC\_SLOW\_CLK in LP\_SLEEP state.

0: Disable

1: Enable

(R/W)

Register 13.28. PMU\_IMM\_HP\_CK\_POWER\_REG (0x00CC)

|                       |    |                      |    |                          |    |                            |    |                              |    |          |    |                      |    |                     |   |                         |   |                           |   |                             |  |          |  |
|-----------------------|----|----------------------|----|--------------------------|----|----------------------------|----|------------------------------|----|----------|----|----------------------|----|---------------------|---|-------------------------|---|---------------------------|---|-----------------------------|--|----------|--|
| PMU_TIE_HIGH_XPD_XTAL |    | PMU_TIE_HIGH_XPD_PLL |    | PMU_TIE_HIGH_XPD_PLL_I2C |    | PMU_TIE_HIGH_I2C_RETENTION |    | PMU_TIE_HIGH_GLOBAL_XTAL_ICG |    | reserved |    | PMU_TIE_LOW_XPD_XTAL |    | PMU_TIE_LOW_XPD_PLL |   | PMU_TIE_LOW_XPD_PLL_I2C |   | PMU_TIE_LOW_I2C_RETENTION |   | PMU_TIE_LOW_GLOBAL_XTAL_ICG |  | reserved |  |
| 31                    | 30 | 27                   | 26 | 23                       | 22 | 21                         | 20 | 17                           | 16 | 15       | 14 | 11                   | 10 | 7                   | 6 | 5                       | 4 | 1                         | 0 |                             |  |          |  |
| 0                     | 0  | 0                    | 0  | 0                        | 0  | 0                          | 0  | 0                            | 0  | 0        | 0  | 0                    | 0  | 0                   | 0 | 0                       | 0 | 0                         | 0 | Reset                       |  |          |  |

**PMU\_TIE\_LOW\_GLOBAL\_PLL\_ICG** Configures whether to power down global PLL clock gating bitmap.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_LOW\_GLOBAL\_XTAL\_ICG** Configures whether to power down XTAL clock.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_LOW\_I2C\_RETENTION** Configures whether to power down ANALOG I2C retention.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_LOW\_XPD\_PLL\_I2C** Configures whether to power down global PLL I2C clock power bitmap.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_LOW\_XPD\_PLL** Configures whether to power down global PLL clock power bitmap.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_LOW\_XPD\_XTAL** Configures whether to power down XTAL clock power.

0: No effect

1: Power down  
(WT)

**PMU\_TIE\_HIGH\_GLOBAL\_PLL\_ICG** Configures whether to enable PLL clock gating bitmap.

0: No effect

1: Enable  
(WT)

Continued on the next page...

**Register 13.28. PMU\_IMM\_HP\_CK\_POWER\_REG (0x00CC)**

Continued from the previous page...

**PMU\_TIE\_HIGH\_GLOBAL\_XTAL\_ICG** Configures whether to enable global XTAL clock.

0: No effect

1: Enable

(WT)

**PMU\_TIE\_HIGH\_I2C\_RETENTION** Configures whether to enable ANALOG I2C retention.

0: No effect

1: Enable

(WT)

**PMU\_TIE\_HIGH\_XPD\_PLL\_I2C** Configures whether to enable PLL I2C clock power bitmap.

0: No effect

1: Enable

(WT)

**PMU\_TIE\_HIGH\_XPD\_PLL** Configures whether to enable global PLL clock power bitmap.

0: No effect

1: Enable

(WT)

**PMU\_TIE\_HIGH\_XPD\_XTAL** Configures whether to enable global XTAL clock power.

0: No effect

1: Enable

(WT)



Register 13.29. PMU\_IMM\_SLEEP\_SYSCLK\_REG (0x00D0)

|                            |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|----------------------------|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| PMU_UPDATE_DIG_SYS_CLK_SEL |    |    |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31                         | 30 | 29 | 28 | 27         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0                          | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PMU\_UPDATE\_DIG\_ICG\_SWITCH** Immediately updates function clock gating status. (WT)

**PMU\_TIE\_LOW\_ICG\_SLP\_SEL** Configures whether to disable PMU control of function clock.

0: No effect

1: Disable

(WT)

**PMU\_TIE\_HIGH\_ICG\_SLP\_SEL** Configures whether to enable PMU control of function clock.

0: No effect

1: Enable

(WT)

**PMU\_UPDATE\_DIG\_SYS\_CLK\_SEL** Immediately updates system clock.

0: No effect

1: Updates the configurations of SYS\_CLK\_SEL in the current PMU state to the application side.

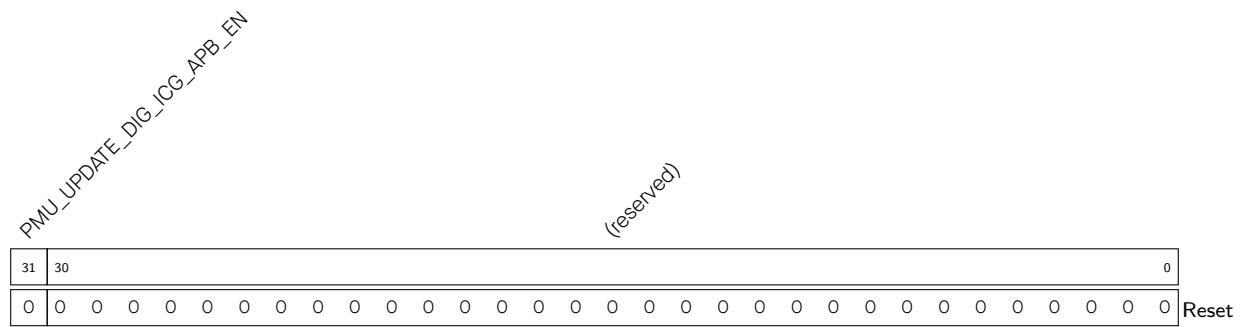
(WT)

Register 13.30. PMU\_IMM\_HP\_FUNC\_ICG\_REG (0x00D4)

|                            |    |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|----------------------------|----|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| PMU_UPDATE_DIG_ICG_FUNC_EN |    |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31                         | 30 |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |       |
| 0                          | 0  | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PMU\_UPDATE\_DIG\_ICG\_FUNC\_EN** Immediately updates function clock gating bitmap. (WT)

Register 13.31. PMU\_IMM\_HP\_APB\_ICG\_REG (0x00D8)



**PMU\_UPDATE\_DIG\_ICG\_APB\_EN** Immediately updates APB clock gating bitmap. (WT)

**Register 13.32. PMU\_IMM\_PAD\_HOLD\_ALL\_REG (0x00E4)**

|                              |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |       |
|------------------------------|----|----|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|-------|
| PMU_TIE_LOW_HP_PAD_HOLD_ALL  |    |    |    |    |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMU_HP_PAD_HOLD_ALL |   |   |       |
| PMU_TIE_HIGH_HP_PAD_HOLD_ALL |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMU_LP_PAD_HOLD_ALL |   |   |       |
| PMU_TIE_LOW_LP_PAD_HOLD_ALL  |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMU_PAD_SLP_SEL     |   |   |       |
| PMU_TIE_HIGH_LP_PAD_HOLD_ALL |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |       |
| PMU_TIE_LOW_HP_PAD_SLP_SEL   |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |       |
| PMU_TIE_HIGH_HP_PAD_SLP_SEL  |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |       |
| 31                           | 30 | 29 | 28 | 27 | 26 | 25         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3                   | 2 | 1 | 0     |
| 0                            | 0  | 0  | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | Reset |

**PMU\_PAD\_SLP\_SEL** Indicates whether the current GPIO function uses sleep configurations.

0: No

1: Yes

(RO)

**PMU\_LP\_PAD\_HOLD\_ALL** Indicates whether the LP PAD is in the HOLD status.

0: No

1: Yes

(RO)

**PMU\_HP\_PAD\_HOLD\_ALL** Represents whether the HP PAD is in the HOLD status.

0: No

1: Yes

(RO)

**PMU\_TIE\_HIGH\_PAD\_SLP\_SEL** Immediately configures GPIO function to use sleep configurations.

(WT)

**PMU\_TIE\_LOW\_PAD\_SLP\_SEL** Immediately releases GPIO function from using sleep configuration.

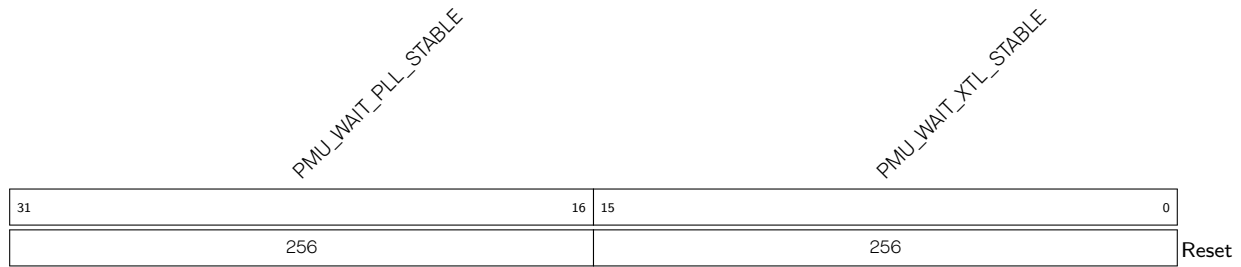
(WT)

**PMU\_TIE\_HIGH\_LP\_PAD\_HOLD\_ALL** Immediately configure LP PAD to enter HOLD state. (WT)

**PMU\_TIE\_LOW\_LP\_PAD\_HOLD\_ALL** Immediately releases LP PAD from HOLD state. (WT)

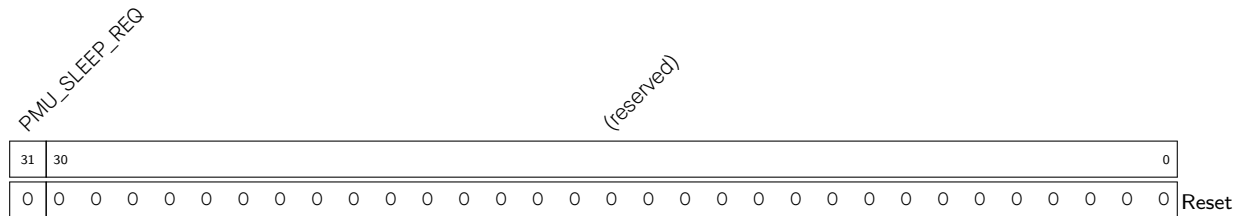
**PMU\_TIE\_HIGH\_HP\_PAD\_HOLD\_ALL** Immediately configures HP PAD to enter HOLD state. (WT)

**PMU\_TIE\_LOW\_HP\_PAD\_HOLD\_ALL** Immediately releases HP PAD from HOLD state. (WT)

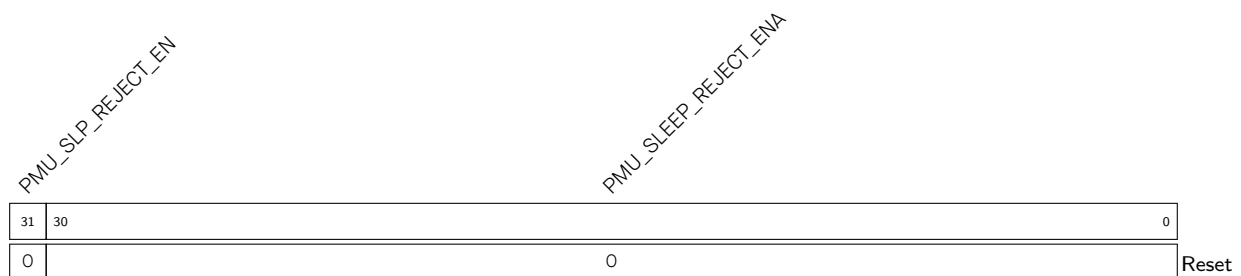
**Register 13.33. PMU\_POWER\_CK\_WAIT\_CNTL\_REG (0x011C)**

**PMU\_WAIT\_XTL\_STABLE** Configures the wait time for enabling XTAL global clock gating after the XTAL power supply is enabled. The unit is LP\_DYN\_FAST\_CLK. (R/W)

**PMU\_WAIT\_PLL\_STABLE** Configures the wait time for enabling PLL global clock gating after the PLL power supply is enabled. The unit is LP\_DYN\_FAST\_CLK. (R/W)

**Register 13.34. PMU\_SLP\_WAKEUP\_CNTL0\_REG (0x0120)**

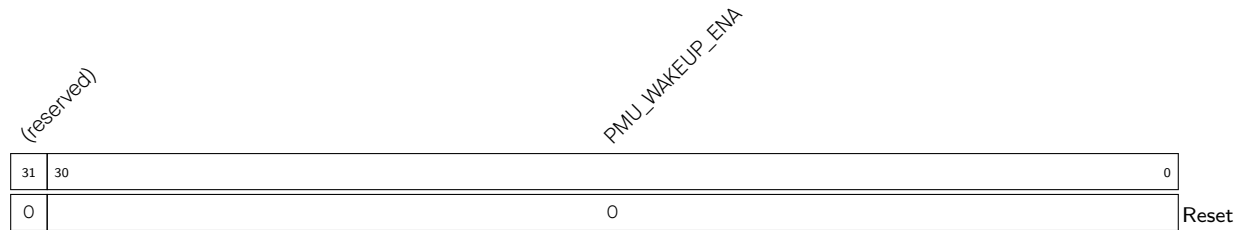
**PMU\_SLEEP\_REQ** Configures whether to switch the PMU state to HP\_SLEEP or LP\_SLEEP.  
 0: Do not switch  
 1: Switch to HP\_SLEEP or LP\_SLEEP, depending on the state of the LP CPU.  
 (WT)

**Register 13.35. PMU\_SLP\_WAKEUP\_CNTL1\_REG (0x0124)**

**PMU\_SLEEP\_REJECT\_ENA** Configures the sleep rejection source. For the mapping between values and sources please refer to Table 13.4-1. (R/W)

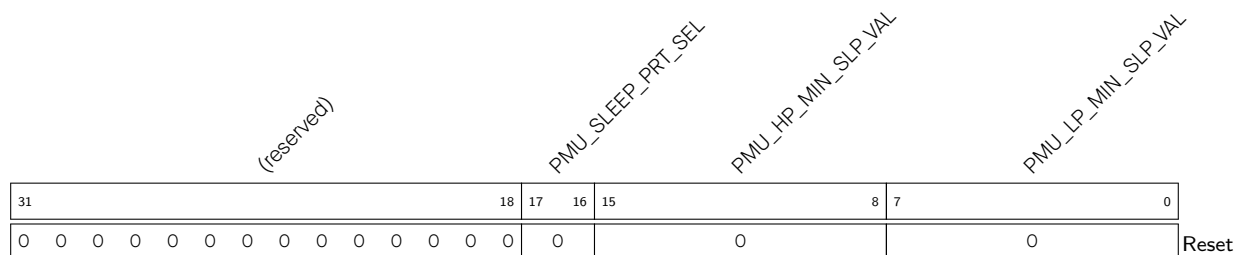
**PMU\_SLP\_REJECT\_EN** Configures whether to enable sleep rejection function.  
 0: Disable  
 1: Enable  
 (R/W)

### Register 13.36. PMU\_SLP\_WAKEUP\_CNTL2\_REG (0x0128)



**PMU\_WAKEUP\_ENA** Configures wake-up source. For the mapping between values and sources please refer to Table 13.4-1. (R/W)

### Register 13.37. PMU\_SLP\_WAKEUP\_CNTL3\_REG (0x012C)

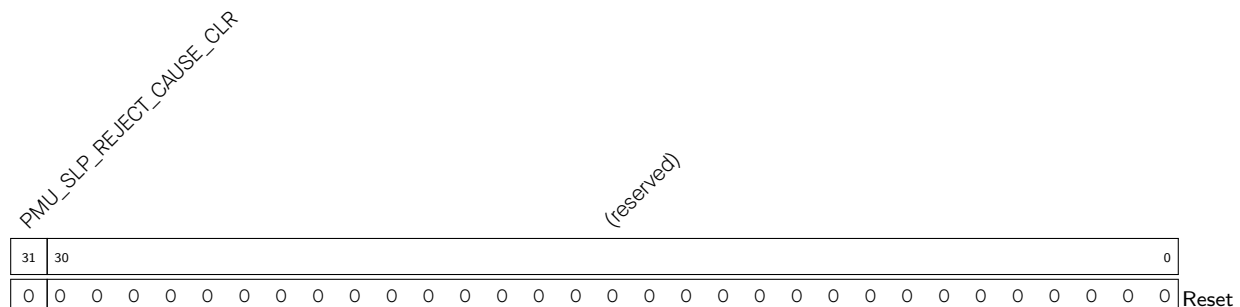


**PMU\_LP\_MIN\_SLP\_VAL** Configures the minimum sleep time to enter LP\_SLEEP. The unit is LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_HP\_MIN\_SLP\_VAL** Configures the minimum sleep time to enter HP\_SLEEP. The unit is LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_SLEEP\_PRT\_SEL** Configures the minimum sleep time mode.  
0, 1, 3: Reserved  
2: Protects both LP\_SLEEP and HP\_SLEEP simultaneously  
(R/W)

### Register 13.38. PMU\_SLP\_WAKEUP\_CNTL4\_REG (0x0130)



**PMU\_SLP\_REJECT\_CAUSE\_CLR** Write 1 to clear **PMU\_REJECT\_CAUSE**. (WT)

### Register 13.39. PMU\_SLP\_WAKEUP\_STATUS0\_REG (0x0144)

Diagram illustrating the structure of the PMU\_WakeupCause register:

- Bit 31: (reserved)
- Bit 0: Reset

**PMU\_WAKEUP\_CAUSE** Indicates the wake-up source. For the mapping between values and sources please refer to Table 13.4-1. (RO)

### Register 13.40. PMU\_SLP\_WAKEUP\_STATUS1\_REG (0x0148)

|    |    |       |
|----|----|-------|
| 31 | 30 | 0     |
| 0  | 0  | Reset |

**PMU\_REJECT\_CAUSE** Indicates the wake-up rejection source. For the mapping between values and sources please refer to Table 13.4-1. (RO)

### Register 13.41. PMU\_HP\_CK\_CNTL\_REG (0x0154)

|                                 |    |    |                          |   |                          |
|---------------------------------|----|----|--------------------------|---|--------------------------|
| 31                              | 16 | 15 | 8                        | 7 | 0                        |
| (reserved)                      |    |    | PMU_SWITCH_ICG_ONTL_WAIT |   | PMU_MODIFY_ICG_ONTL_WAIT |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    | 10                       |   | 10                       |
| Reset                           |    |    |                          |   |                          |

**PMU\_MODIFY\_ICG\_CNTL\_WAIT** Configures the wait time for modifying the functional module clock gating. The unit is LP\_DYN\_FAST\_CLK. (R/W)

**PMU\_SWITCH\_ICG\_CNTL\_WAIT** Configures the wait time for switching the functional module clock gating. The unit is LP\_DYN\_FAST\_CLK. (R/W)

### Register 13.42. PMU\_RF\_PWC\_REG (0x015C)

[illegible]

**PMU\_MSPI\_PHY\_XPD** Configures whether to enable MSPI PHY.

0: Disable

1: Enable

(R/W)

**PMU\_SDIO\_PLL\_XPD** Configures whether to enable SDIO PLL.

0: Disable

1: Enable

(R/W)

**PMU\_PERIF\_I2C\_RSTB** Configures whether to enable reset for PERI I2C.

0: Reset

1: Release

(R/W)

**PMU\_XPD\_PERIF\_I2C** Configures whether to enable the power for PERI ADC.

0: Disable

1: Enable

(R/W)





### Register 13.44. PMU\_HP\_INT\_ST\_REG (0x0168)

[illegible]

**PMU\_OP1A\_CNT\_TARGET0\_REACH\_O\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET0\\_REACH\\_O\\_INT](#). (RO)

**PMU\_OP1A\_CNT\_TARGET1\_REACH\_O\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_O\\_INT](#). (RO)

**PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET0\\_REACH\\_1\\_INT](#). (RO)

**PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_1\\_INT](#). (RO)

**PMU\_OP2A\_CNT\_TARGET0\_REACH\_O\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP2A\\_CNT\\_TARGET0\\_REACH\\_O\\_INT](#). (RO)

**PMU\_OP2A\_CNT\_TARGET1\_REACH\_O\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP2A\\_CNT\\_TARGET1\\_REACH\\_O\\_INT](#). (RO)

**PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP2A\\_CNT\\_TARGET0\\_REACH\\_1\\_INT](#). (RO)

**PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_ST** The masked interrupt status of [PMU\\_OP2A\\_CNT\\_TARGET1\\_REACH\\_1\\_INT](#). (RO)

**PMU\_LP\_CPU\_EXC\_INT\_ST** The masked interrupt status of **PMU\_LP\_CPU\_EXC\_INT**. (RO)

**PMU\_SDIO\_IDLE\_INT\_ST** The masked interrupt status of **PMU\_SDIO\_IDLE\_INT**. (RO)

**PMU\_SW\_INT\_ST** The masked interrupt status of [PMU\\_SW\\_INT](#). (RO)

**PMU\_SOC\_SLEEP\_REJECT\_INT\_ST** The masked interrupt status of [PMU\\_SOC\\_SLEEP\\_REJECT\\_INT](#).  
(RO)

**PMU\_SOC\_WAKEUP\_INT\_ST** The masked interrupt status of [PMU\\_SOC\\_WAKEUP\\_INT](#). (RO)

Register 13.45. PMU\_HP\_INT\_ENA\_REG (0x016C)

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div>PMU_SOC_WAKEUP_INT_ENA<br/>PMU_SOC_SLEEP_REJECT_INT_ENA<br/>PMU_SW_INT_ENA<br/>PMU_SDIO_IDLE_INT_ENA<br/>PMU_LP_CPU_EXC_INT_ENA<br/>(reserved)<br/>reserved<br/>reserved<br/>reserved<br/>reserved<br/>PMU_OP2A_CNT_TARGET0_REACH_0_HP_INT_ENA<br/>PMU_OP2A_CNT_TARGET0_REACH_1_HP_INT_ENA<br/>PMU_OP2A_CNT_TARGET1_REACH_0_HP_INT_ENA<br/>PMU_OP2A_CNT_TARGET1_REACH_1_HP_INT_ENA<br/>PMU_OP1A_CNT_TARGET0_REACH_0_HP_INT_ENA<br/>PMU_OP1A_CNT_TARGET0_REACH_1_HP_INT_ENA<br/>PMU_OP1A_CNT_TARGET1_REACH_0_HP_INT_ENA<br/>PMU_OP1A_CNT_TARGET1_REACH_1_HP_INT_ENA<br/><br/>(reserved)</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

PMU\_OP1A\_CNT\_TARGET0\_REACH\_0\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP1A\\_CNT\\_TARGET0\\_REACH\\_0\\_INT](#). (R/W)

PMU\_OP1A\_CNT\_TARGET1\_REACH\_0\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_0\\_INT](#). (R/W)

PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP1A\\_CNT\\_TARGET0\\_REACH\\_1\\_INT](#). (R/W)

PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_1\\_INT](#). (R/W)

PMU\_OP2A\_CNT\_TARGET0\_REACH\_0\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP2A\\_CNT\\_TARGET0\\_REACH\\_0\\_INT](#). (R/W)

PMU\_OP2A\_CNT\_TARGET1\_REACH\_0\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP2A\\_CNT\\_TARGET1\\_REACH\\_0\\_INT](#). (R/W)

PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP2A\\_CNT\\_TARGET0\\_REACH\\_1\\_INT](#). (R/W)

PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_ENA Write 1 to enable  
[PMU\\_OP2A\\_CNT\\_TARGET1\\_REACH\\_1\\_INT](#). (R/W)

PMU\_LP\_CPU\_EXC\_INT\_ENA Write 1 to enable [PMU\\_LP\\_CPU\\_EXC\\_INT](#). (R/W)

PMU\_SDIO\_IDLE\_INT\_ENA Write 1 to enable [PMU\\_SDIO\\_IDLE\\_INT](#). (R/W)

PMU\_SW\_INT\_ENA Write 1 to enable [PMU\\_SW\\_INT](#). (R/W)

PMU\_SOC\_SLEEP\_REJECT\_INT\_ENA Write 1 to enable [PMU\\_SOC\\_SLEEP\\_REJECT\\_INT](#). (R/W)

PMU\_SOC\_WAKEUP\_INT\_ENA Write 1 to enable [PMU\\_SOC\\_WAKEUP\\_INT](#). (R/W)

### Register 13.46. PMU\_HP\_INT\_CLR\_REG (0x0170)

[illegible]

PMU\_OP1A\_CNT\_TARGETO\_REACH\_O\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP1A\_CNT\_TARGETO\_REACH\_O\_INT. (WT)

PMU\_OP1A\_CNT\_TARGET1\_REACH\_O\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP1A\_CNT\_TARGET1\_REACH\_O\_INT. (WT)

PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP1A\_CNT\_TARGET0\_REACH\_1\_INT. (WT)

PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_INT. (WT)

PMU\_OP2A\_CNT\_TARGETO\_REACH\_O\_HP\_INT\_CLR Write 1 to clear  
VPMU\_OP2A\_CNT\_TARGETO\_REACH\_O\_INT. (WT)

PMU\_OP2A\_CNT\_TARGET1\_REACH\_O\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP2A\_CNT\_TARGET1\_REACH\_O\_INT. (WT)

PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP2A\_CNT\_TARGET0\_REACH\_1\_INT. (WT)

PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_HP\_INT\_CLR Write 1 to clear  
PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_INT. (WT)

**PMU\_LP\_CPU\_EXC\_INT\_CLR** Write 1 to clear **PMU\_LP\_CPU\_EXC\_INT**. (WT)

**PMU\_SDIO\_IDLE\_INT\_CLR** Write 1 to clear **PMU\_SDIO\_IDLE\_INT**. (WT)

**PMU\_SW\_INT\_CLR** Write 1 to clear **PMU\_SW\_INT**. (WT)

**PMU\_SOC\_SLEEP\_REJECT\_INT\_CLR** Write 1 to clear **PMU\_SOC\_SLEEP\_REJECT\_INT**. (WT)

**PMU SOC WAKEUP INT CLR** Write 1 to clear **PMU SOC WAKEUP INT.** (WT)

### Register 13.47. PMU\_LP\_INT\_RAW\_REG (0x0174)

[illegible]

**PMU\_LP\_CPU\_SLEEP\_REJECT\_INT\_RAW** The raw interrupt status of [PMU\\_LP\\_CPU\\_SLEEP\\_REJECT\\_INT](#). (R/WTC/SS)

**PMU\_OP1A\_CNT\_TARGETO\_REACH\_O\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP1A\\_CNT\\_TARGETO\\_REACH\\_O\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP1A\_CNT\_TARGET1\_REACH\_O\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_O\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP1A\_CNT\_TARGETO\_REACH\_1\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP1A\\_CNT\\_TARGETO\\_REACH\\_1\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP1A\_CNT\_TARGET1\_REACH\_1\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP1A\\_CNT\\_TARGET1\\_REACH\\_1\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP2A\_CNT\_TARGETO\_REACH\_O\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP2A\\_CNT\\_TARGETO\\_REACH\\_O\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP2A\_CNT\_TARGET1\_REACH\_O\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP2A\\_CNT\\_TARGET1\\_REACH\\_O\\_LP\\_INT](#). (R/WTC/SS)

**PMU\_OP2A\_CNT\_TARGETO\_REACH\_1\_LP\_INT\_RAW** The raw interrupt status of [PMU\\_OP2A\\_CNT\\_TARGETO\\_REACH\\_1\\_LP\\_INT](#). (R/WTC/SS)

PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_LP\_INT\_RAW The raw interrupt status of PMU\_OP2A\_CNT\_TARGET1\_REACH\_1\_LP\_INT. (R/WTC/SS)

**PMU\_LP\_CPU\_WAKEUP\_INT\_RAW** The raw interrupt status of **PMU\_LP\_CPU\_WAKEUP\_INT**.  
(R/WTC/SS)

**PMU\_SLEEP\_SWITCH\_ACTIVE\_END\_INT\_RAW** The raw interrupt status of [PMU\\_SLEEP\\_SWITCH\\_ACTIVE\\_END\\_INT](#). (R/WTC/SS)

**PMU\_ACTIVE\_SWITCH\_SLEEP\_END\_INT\_RAW** The raw interrupt status of  
PMU\_ACTIVE\_SWITCH\_SLEEP\_END\_INT. (R/WTC/SS)

**PMU\_SLEEP\_SWITCH\_ACTIVE\_START\_INT\_RAW** The raw interrupt status of  
PMU\_SLEEP\_SWITCH\_ACTIVE\_START\_INT. (R/WTC/SS)

Continued on the next page...

## Register 13.47. PMU\_LP\_INT\_RAW\_REG (0x0174)

Continued from the previous page...

**PMU\_ACTIVE\_SWITCH\_SLEEP\_START\_INT\_RAW** The raw interrupt status of [PMU\\_ACTIVE\\_SWITCH\\_SLEEP\\_START\\_INT](#). (R/WTC/SS)

**PMU\_HP\_SW\_TRIGGER\_INT\_RAW** The raw interrupt status of [PMU\\_HP\\_SW\\_TRIGGER\\_INT](#). (R/WTC/SS)



## Register 13.48. PMU\_LP\_INT\_ST\_REG (0x0178)

Continued from the previous page...

**PMU\_ACTIVE\_SWITCH\_SLEEP\_START\_INT\_ST** The masked interrupt status of [PMU\\_ACTIVE\\_SWITCH\\_SLEEP\\_START\\_INT](#). (RO)

**PMU\_HP\_SW\_TRIGGER\_INT\_ST** The masked interrupt status of [PMU\\_HP\\_SW\\_TRIGGER\\_INT](#). (RO)





## Register 13.49. PMU\_LP\_INT\_ENA\_REG (0x017C)

Continued from the previous page...

PMU\_ACTIVE\_SWITCH\_SLEEP\_START\_INT\_ENA Write 1 to enable  
[PMU\\_ACTIVE\\_SWITCH\\_SLEEP\\_START\\_INT](#). (R/W)

PMU\_HP\_SW\_TRIGGER\_INT\_ENA Write 1 to enable [PMU\\_HP\\_SW\\_TRIGGER\\_INT](#). (R/W)



**Register 13.50. PMU\_LP\_INT\_CLR\_REG (0x0180)**

Continued from the previous page...

**PMU\_ACTIVE\_SWITCH\_SLEEP\_START\_INT\_CLR** Write 1 to clear [PMU\\_ACTIVE\\_SWITCH\\_SLEEP\\_START\\_INT](#).  
(WT)

**PMU\_HP\_SW\_TRIGGER\_INT\_CLR** Write 1 to clear [PMU\\_HP\\_SW\\_TRIGGER\\_INT](#). (WT)

**Register 13.51. PMU\_LP\_CPU\_PWRO\_REG (0x0184)**

|                               |    |    |      |                              |  |  |  |  |  |  |   |                        |   |   |   |   |   |   |   |                      |   |   |       |
|-------------------------------|----|----|------|------------------------------|--|--|--|--|--|--|---|------------------------|---|---|---|---|---|---|---|----------------------|---|---|-------|
| PMU_LP_CPU_SLP_BYPASS_INTR_EN |    |    |      | PMU_LP_CPU_SLP_STALL_WAIT    |  |  |  |  |  |  |   | (reserved)             |   |   |   |   |   |   |   | PMU_LP_CPU_STALL_RDY |   |   |       |
| PMU_LP_CPU_SLP_RESET_EN       |    |    |      | PMU_LP_CPU_SLP_WAITI_FLAG_EN |  |  |  |  |  |  |   | PMU_LP_CPU_FORCE_STALL |   |   |   |   |   |   |   | PMU_LP_CPU_WAITI_RDY |   |   |       |
| 31                            | 30 | 29 | 28   | 21                           |  |  |  |  |  |  |   | 17                     | 2 |   |   |   |   |   |   |                      | 1 | 0 |       |
| 0                             | 0  | 0  | Oxff |                              |  |  |  |  |  |  | 1 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | Reset |

**PMU\_LP\_CPU\_WAITI\_RDY** Indicates whether the LP CPU is in the waiti state.

0: Does not enter the state

1: Enters the state

(RO)

**PMU\_LP\_CPU\_STALL\_RDY** Indicates whether the LP CPU is in the stall state.

0: Does not enter the state

1: Enters the state

(RO)

**PMU\_LP\_CPU\_FORCE\_STALL** Configures the LP CPU to enter the stall state.

0: Does not enter the state

1: Enters the state

(R/W)

**PMU\_LP\_CPU\_SLP\_WAITI\_FLAG\_EN** Configures whether the LP CPU needs to enter the waiti state when entering sleep mode.

0: Does not enter the state

1: Enters the state

(R/W)

**PMU\_LP\_CPU\_SLP\_STALL\_FLAG\_EN** Configures whether the LP CPU needs to enter the stall state when entering sleep mode.

0: Does not enter the state

1: Enters the state

(R/W)

**PMU\_LP\_CPU\_SLP\_STALL\_WAIT** Configures the time to wait for the stall to take effect after enabling stall state when the LP CPU enters sleep mode. The unit is LP\_DYN\_FAST\_CLK. (R/W)

**PMU\_LP\_CPU\_SLP\_STALL\_EN** Configures whether to pause the LP CPU in sleep mode.

0: Do not pause

1: Pause

(R/W)

Continued on the next page...

Register 13.51. PMU\_LP\_CPU\_PWRO\_REG (0x0184)

Continued from the previous page...

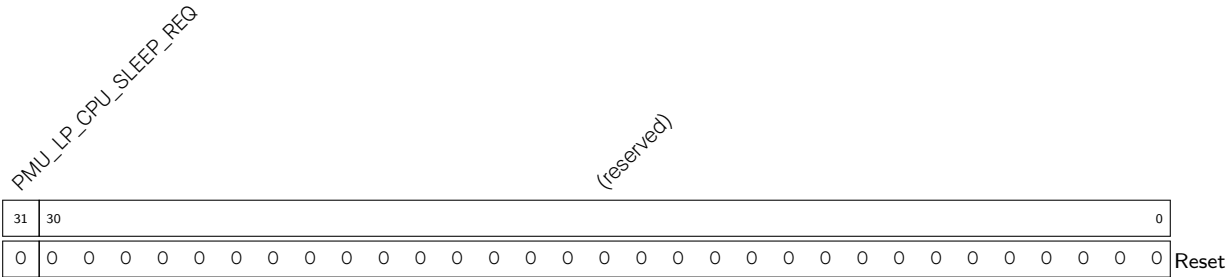
**PMU\_LP\_CPU\_SLP\_RESET\_EN** Configures whether to reset the LP CPU in sleep mode.

- 0: Do not reset
  - 1: Reset
- (R/W)

**PMU\_LP\_CPU\_SLP\_BYPASS\_INTR\_EN** Configures whether to enable interrupt signals for the LP CPU in sleep mode.

- 0: Disable interrupt signals
  - 1: Enable interrupt signals
- (R/W)

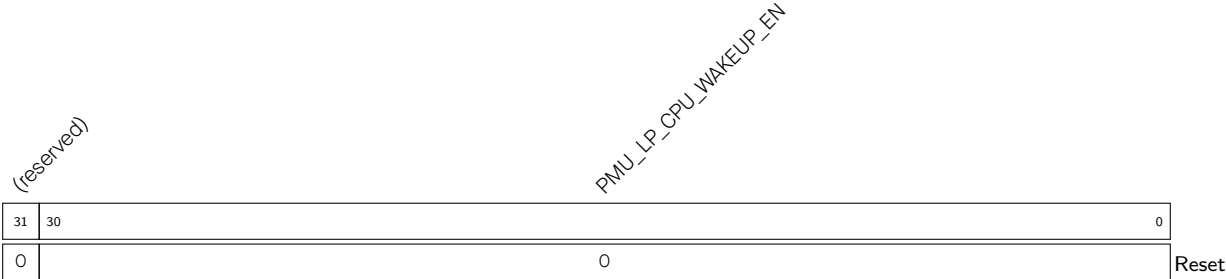
Register 13.52. PMU\_LP\_CPU\_PWR1\_REG (0x0188)



**PMU\_LP\_CPU\_SLEEP\_REQ** Configures whether the LP CPU enters sleep.

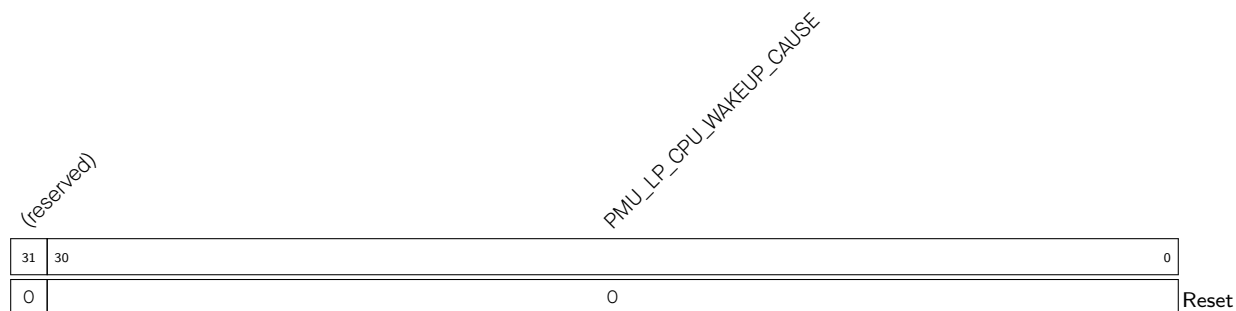
- 0: Does not enter sleep
  - 1: Enters sleep
- (WT)

Register 13.53. PMU\_LP\_CPU\_PWR2\_REG (0x018C)



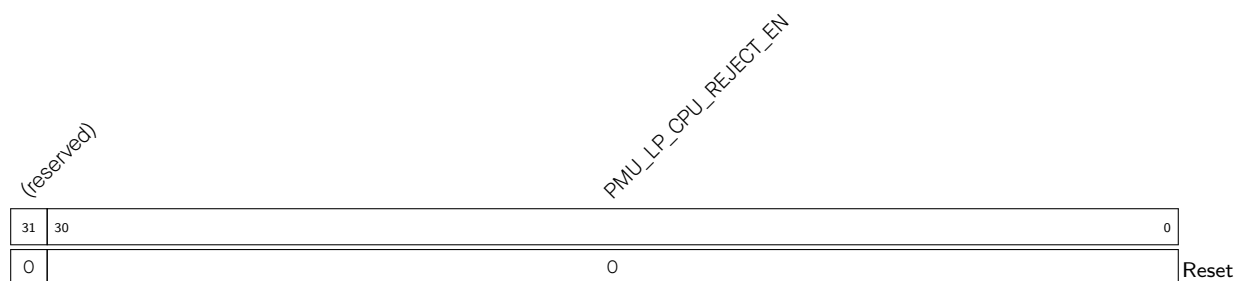
**PMU\_LP\_CPU\_WAKEUP\_EN** Configures the wake-up source for LP CPU. For details please refer to Table 13.4-1 *Wake-up Sources*. (R/W)

Register 13.54. PMU\_LP\_CPU\_PWR3\_REG (0x0190)



**PMU\_LP\_CPU\_WAKEUP\_CAUSE** Indicates the wake-up cause of LP CPU. (RO)

Register 13.55. PMU\_LP\_CPU\_PWR4\_REG (0x0194)



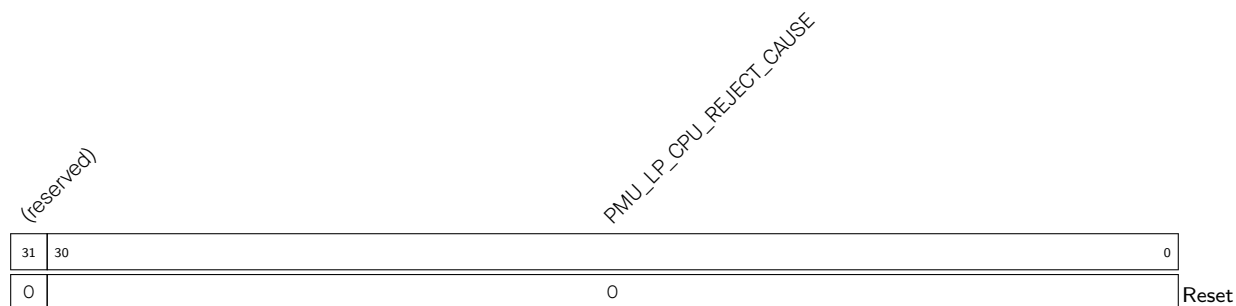
**PMU\_LP\_CPU\_REJECT\_EN** Configures whether to enable sleep rejection function for the LP CPU.

0: Disable

1: Enable

(R/W)

Register 13.56. PMU\_LP\_CPU\_PWR5\_REG (0x0198)



**PMU\_LP\_CPU\_REJECT\_CAUSE** Indicates the sleep rejection cause of LP CPU. (RO)

### Register 13.57. PMU\_HP\_LP\_CPU\_COMM\_REG (0x019C)

Diagram illustrating the structure of the PMU\_HP\_TRIGGER\_LP register. The register is 32 bits wide, with bits 31 and 30 labeled PMU\_HP\_TRIGGER\_LP and PMU\_LP\_TRIGGER\_HP respectively. Bit 29 is labeled (reserved). The remaining bits (0-28) are labeled 0. A Reset signal is shown at the bottom right.

**PMU\_LP\_TRIGGER\_HP** When the LP CPU sets this register to 1, the chip is woken up. (WT)

**PMU\_HP\_TRIGGER\_LP** When the HP CPU sets this register to 1, the LP CPU is woken up. (WT)

### Register 13.58. PMU\_EXT\_LDO\_PO\_OP1A\_REG (0x01B8)

[illegible]

**PMU\_OP1A\_FORCE\_TIEH\_SEL\_0** Configures which of the following controls the mode selection for V01 regulator.

1: Mode selection is controlled by `PMU_OP1A_TIEH_SEL_0`

0: Mode selection is controlled by eFuse

(R/W)

PMU\_OP1A\_TIEH\_SEL\_0 Configures mode for VO1.

0: Mode is controlled by PMU\_OP1A\_TIEH\_0.

1: Mode is controlled by SDMMC\_0

## 2: Bypass mode

3: Mode is controlled by SDMMC\_1

(R/W)

PMU\_OP1A\_TIEH\_0 Configures mode for V01.

0: LDO mode

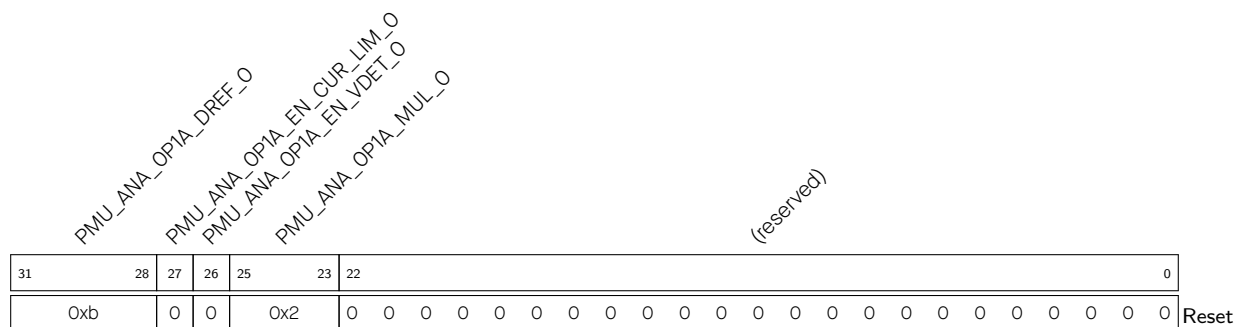
### 1: Bypass mode

(R/W)

**PMU\_OP1A\_TARGET1\_0** Configures the timeout for stage 2 of the VO1 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_OP1A\_TARGETO\_0** Configures the timeout for stage 1 of the VO1 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

### Register 13.59. PMU\_EXT\_LDO\_PO\_OP1A\_ANA\_REG (0x01BC)



**PMU\_ANA\_OP1A\_MUL\_0** Configures the MUL, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-7: MUL ranges from 1 to 2.75, with a step of 0.25.  
(R/W)

**PMU\_ANA\_OP1A\_EN\_VDET\_0** Configures whether to enable VO1 voltage detection.

0: Do not enable  
1: Enable  
(R/W)

**PMU\_ANA\_OP1A\_EN\_CUR\_LIM\_0** Configures whether to enable over current protection for VO1.

0: Do not enable  
1: Enable  
(R/W)

**PMU\_ANA\_OP1A\_DREF\_O** Configures the LDO Vref, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-8:  $V_{ref} = 0.5\text{ V} - 0.9\text{ V}$ , with a step of 50 mV  
9-15:  $V_{ref} = 1.0\text{ V} - 1.6\text{ V}$ , with a step of 100 mV  
(R/W)



### Register 13.60. PMU\_EXT\_LDO\_PO\_OP2A\_REG (0x01C0)

[illegible]

**PMU\_OP2A\_FORCE\_TIEH\_SEL\_0** Configures which of the following controls the mode selection for VO3 regulator.

- 1: Mode selection is controlled by PMU\_OP2A\_TIEH\_SEL\_0
- 1: Mode selection is controlled by SDMMC\_0
- 2: Bypass mode
- 3: Mode selection is controlled by SDMMC\_1
- (R/W)

**PMU\_OP2A\_XPD\_0** Configures whether software enables V03 regulator.

- 0: Disable  
1: Enable  
(R/W)

**PMU\_OP2A\_TIEH\_SEL\_0** Configures mode for VO3.

- 0: Mode is controlled by PMU\_OP2A\_TIEH\_O.  
1: Mode is controlled by SDMMC\_0  
2: Bypass mode  
3: Mode is controlled by SDMMC\_1  
(R/W)

PMU\_OP2A\_TIEH\_0 Configures mode for VO3.

- 0: LDO mode  
1: Bypass mode  
(R/W)

**PMU\_OP2A\_TARGET1\_0** Configures the timeout for stage 2 of the VO3 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_OP2A\_TARGET0\_0** Configures the timeout for stage 1 of the VO3 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

### Register 13.61. PMU\_EXT\_LDO\_PO\_OP2A\_ANA\_REG (0x01C4)

Diagram illustrating the structure of the PMU\_Ana\_Op2A register (32 bits):

- Bit 31: Reset value (0)
- Bits 28-27: PMU\_Ana\_Op2A\_Dref\_O (0)
- Bits 26-25: PMU\_Ana\_Op2A\_En\_Cur\_Lim\_O (0x2)
- Bits 24-0: PMU\_Ana\_Op2A\_En\_Vdet\_O (0xb)
- Bits 23-22: (reserved)

**PMU\_ANA\_OP2A\_MUL\_0** Configures the MUL, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-7: MUL ranges from 1 to 2.75, with a step of 0.25.

(R/W)

**PMU\_ANA\_OP2A\_EN\_VDET\_0** Configures whether to enable VO3 voltage detection.

0: Do not enable

1: Enable

(R/W)

**PMU\_ANA\_OP2A\_EN\_CUR\_LIM\_0** Configures whether to enable over current protection for V03.

0: Do not enable

1: Enable

(R/W)

**PMU\_ANA\_OP2A\_DREF\_0** Configures the LDO Vref, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-8:  $V_{ref} = 0.5 \text{ V} - 0.9 \text{ V}$ , with a step of  $50 \text{ mV}$

9-15:  $V_{ref} = 1.0 \text{ V} - 1.6 \text{ V}$ , with a step of  $100 \text{ mV}$

(R/W)

### Register 13.62. PMU\_EXT\_LDO\_P1\_OP1A\_REG (0x01D0)

[illegible]

**PMU\_OP1A\_FORCE\_TIEH\_SEL\_1** Configures which of the following controls the mode selection for VO2 regulator.

- 1: Mode selection is controlled by PMU\_OP1A\_TIEH\_SEL\_1
- 1: Mode selection is controlled by SDMMC\_0
- 2: Bypass mode
- 3: Mode selection is controlled by SDMMC\_1
- (R/W)

**PMU\_OP1A\_XPD\_1** Configures whether software enables VO2 regulator.

- 0: Disable  
1: Enable  
(R/W)

PMU\_OP1A\_TIEH\_SEL\_1 Configures mode for VO2.

- 0: Mode is controlled by [PMU\\_OP1A\\_TIEH\\_1](#).  
 1: Mode is controlled by SDMMC\_0  
 2: Bypass mode  
 3: Mode is controlled by SDMMC\_1  
 (R/W)

PMU\_OP1A\_TIEH\_1 Configures mode for V02.

- 0: LDO mode  
1: Bypass mode  
(R/W)

**PMU\_OP1A\_TARGET1\_1** Configures the timeout for stage 2 of the VO2 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_OP1A\_TARGET0\_1** Configures the timeout for stage 1 of the VO2 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

### Register 13.63. PMU\_EXT\_LDO\_P1\_OP1A\_ANA\_REG (0x01D4)

Diagram illustrating the structure of the PMU\_Ana\_Op1A register (32 bits total):

- Bits 31-24: PMU\_Ana\_Op1A\_DREF\_1
- Bits 23-16: PMU\_Ana\_Op1A\_EN\_CUR\_LIM\_1
- Bits 15-8: PMU\_Ana\_Op1A\_EN\_VDET\_1
- Bits 7-0: PMU\_Ana\_Op1A\_MUL\_1 (reserved)

**PMU\_ANA\_OP1A\_MUL\_1** Configures the MUL, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-7: MUL ranges from 1 to 2.75, with a step of 0.25.

(R/W)

**PMU\_ANA\_OP1A\_EN\_VDET\_1** Configures whether to enable VO2 voltage detection.

0: Do not enable

1: Enable

(R/W)

**PMU\_ANA\_OP1A\_EN\_CUR\_LIM\_1** Configures whether to enable over current protection for V02.

0: Do not enable

1: Enable

(R/W)

**PMU\_ANA\_OP1A\_DREF\_1** Configures the LDO Vref, where the output voltage of the regulator is MUL × Vref.

0-8:  $V_{ref} = 0.5 \text{ V} - 0.9 \text{ V}$ , with a step of  $50 \text{ mV}$

9-15:  $V_{ref} = 1.0\text{ V} - 1.6\text{ V}$ , with a step of  $100\text{ mV}$

(R/W)

**Register 13.64. PMU\_EXT\_LDO\_P1\_OP2A\_REG (0x01D8)**

|          |      |                    |  |  |  |  |  |  |  |  |  |      |                    |    |  |  |  |  |  |  |  |  |   |                 |    |    |    |          |   |   |   |                     |   |   |   |                |   |   |   |                           |   |   |       |            |  |  |  |
|----------|------|--------------------|--|--|--|--|--|--|--|--|--|------|--------------------|----|--|--|--|--|--|--|--|--|---|-----------------|----|----|----|----------|---|---|---|---------------------|---|---|---|----------------|---|---|---|---------------------------|---|---|-------|------------|--|--|--|
| reserved |      | PMU_OP2A_TARGET0_1 |  |  |  |  |  |  |  |  |  |      | PMU_OP2A_TARGET1_1 |    |  |  |  |  |  |  |  |  |   | PMU_OP2A_TIEH_1 |    |    |    | reserved |   |   |   | PMU_OP2A_TIEH_SEL_1 |   |   |   | PMU_OP2A_XPD_1 |   |   |   | PMU_OP2A_FORCE_TIEH_SEL_1 |   |   |       | (reserved) |  |  |  |
| 31       | 30   | 23                 |  |  |  |  |  |  |  |  |  |      | 22                 | 15 |  |  |  |  |  |  |  |  |   |                 | 14 | 13 | 12 | 11       | 9 |   |   |                     | 8 | 7 | 6 | 0              |   |   |   |                           |   |   |       |            |  |  |  |
| 0        | 0x80 |                    |  |  |  |  |  |  |  |  |  | 0x40 |                    |    |  |  |  |  |  |  |  |  | 0 | 0               | 0  | 0  |    |          |   | 1 | 0 | 0                   | 0 | 0 | 0 | 0              | 0 | 0 | 0 | 0                         | 0 | 0 | Reset |            |  |  |  |

**PMU\_OP2A\_FORCE\_TIEH\_SEL\_1** Configures which of the following controls the mode selection for VO4 regulator.

- 1: Mode selection is controlled by [PMU\\_OP2A\\_TIEH\\_SEL\\_1](#)
  - 1: Mode selection is controlled by SDMMC\_0
  - 2: Bypass mode
  - 3: Mode selection is controlled by SDMMC\_1
- (R/W)

**PMU\_OP2A\_XPD\_1** Configures whether software enables VO4 regulator.

- 0: Disable
  - 1: Enable
- (R/W)

**PMU\_OP2A\_TIEH\_SEL\_1** Configures mode for VO4.

- 0: Mode is controlled by [PMU\\_OP2A\\_TIEH\\_1](#).
  - 1: Mode is controlled by SDMMC\_0
  - 2: Bypass mode
  - 3: Mode is controlled by SDMMC\_1
- (R/W)

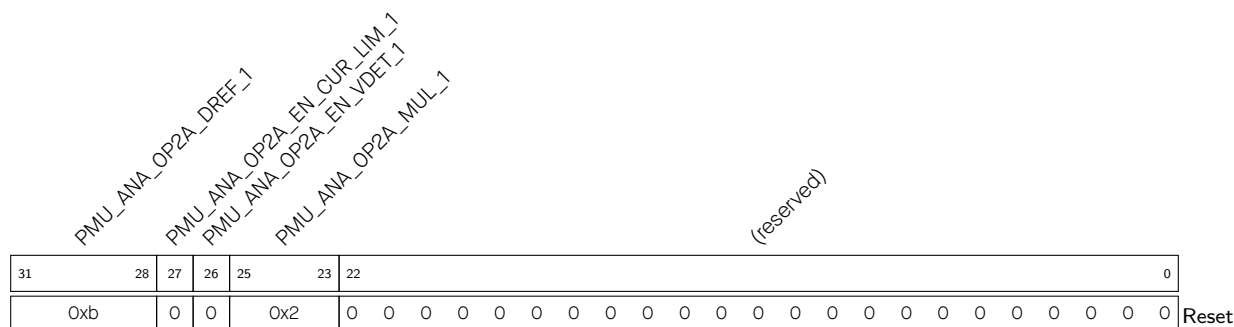
**PMU\_OP2A\_TIEH\_1** Configures mode for VO4.

- 0: LDO mode
  - 1: Bypass mode
- (R/W)

**PMU\_OP2A\_TARGET1\_1** Configures the timeout for stage 2 of the VO4 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_OP2A\_TARGET0\_1** Configures the timeout for stage 1 of the VO4 regulator wait counter, with the unit being a 16 division of LP\_DYN\_SLOW\_CLK. (R/W)

### Register 13.65. PMU\_EXT\_LDO\_P1\_OP2A\_ANA\_REG (0x01DC)



**PMU\_ANA\_OP2A\_MUL\_1** Configures the MUL, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-7: MUL ranges from 1 to 2.75, with a step of 0.25.

(R/W)

**PMU\_ANA\_OP2A\_EN\_VDET\_1** Configures whether to enable VO4 voltage detection.

0: Do not enable

1: Enable

(R/W)

**PMU\_ANA\_OP2A\_EN\_CUR\_LIM\_1** Configures whether to enable over current protection for VO4.

0: Do not enable

1: Enable

(R/W)

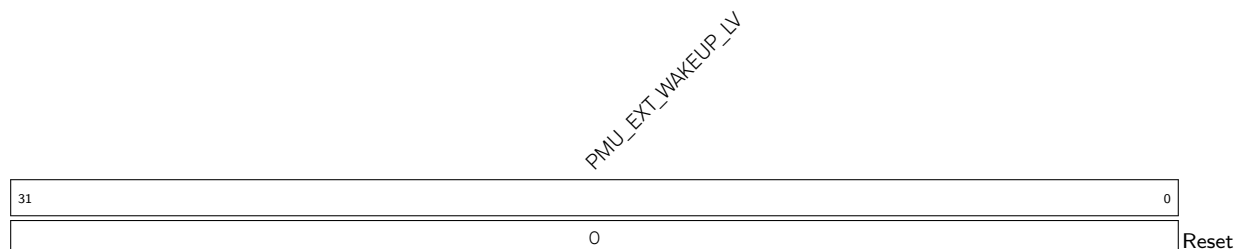
**PMU\_ANA\_OP2A\_DREF\_1** Configures the LDO Vref, where the output voltage of the regulator is  $MUL \times V_{ref}$ .

0-8:  $V_{ref} = 0.5 \text{ V} - 0.9 \text{ V}$ , with a step of 50 mV

9-15:  $V_{ref} = 1.0\text{ V} - 1.6\text{ V}$ , with a step of  $100\text{ mV}$

(R/W)

### Register 13.66. PMU\_EXT\_WAKEUP\_LV\_REG (0x01E8)

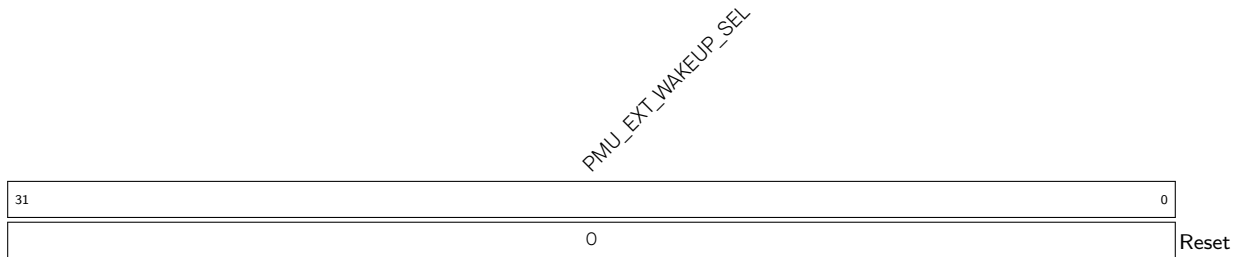


**PMU\_EXT\_WAKEUP\_LV** Configures the wake level for EXT wake-up.

0: Low level wake-up

1: High level wake-up

(R/W)

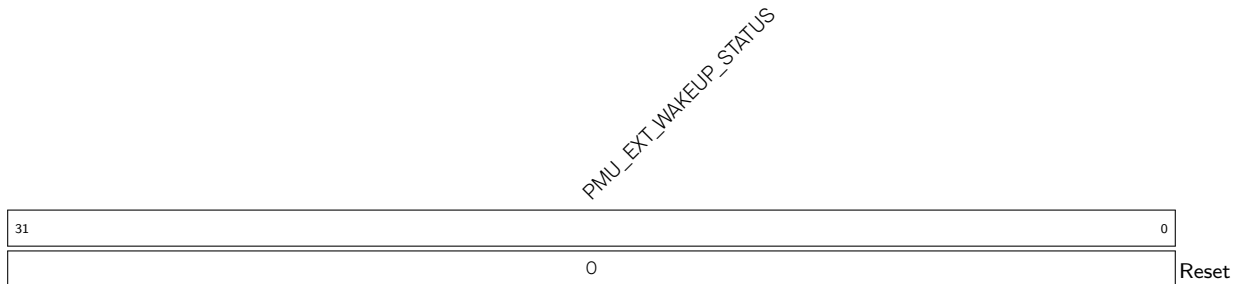
**Register 13.67. PMU\_EXT\_WAKEUP\_SEL\_REG (0x01EC)**

**PMU\_EXT\_WAKEUP\_SEL** Configures whether to enable EXT wake-up.

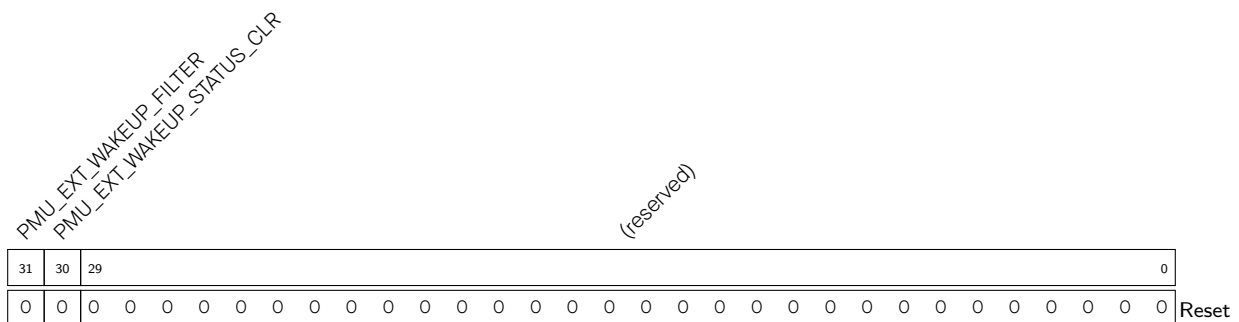
0: Disable

1: Enable

(R/W)

**Register 13.68. PMU\_EXT\_WAKEUP\_ST\_REG (0x01F0)**

**PMU\_EXT\_WAKEUP\_STATUS** Gets the GPIO number for wake-up. 0 corresponds to GPIO0, 1 corresponds to GPIO1, and so on. (RO)

**Register 13.69. PMU\_EXT\_WAKEUP\_CNTL\_REG (0x01F4)**

**PMU\_EXT\_WAKEUP\_STATUS\_CLR** Clears the wake-up records. (R/W)

**PMU\_EXT\_WAKEUP\_FILTER** Configures whether to enable the wake-up filter.

0: Disable

1: Enable

(R/W)

**Register 13.70. PMU\_SDIO\_WAKEUP\_CNTL\_REG (0x01F8)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  | 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 |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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**PMU\_SDIO\_ACT\_DNUM** Configures the duration for maintaining the working state of SDIO. The unit is LP\_DYN\_FAST\_CLK. (R/W)

**Register 13.71. PMU\_TOUCH\_PWR\_CNTL\_REG (0x0210)**

|  |    |     |  |  |  |  |  |  |  |                        |  |    |  |  |  |  |  |  |  |                       |  |    |   |  |  |  |   |   |   |            |   |       |   |   |  |  |  |  |
|--|----|-----|--|--|--|--|--|--|--|------------------------|--|----|--|--|--|--|--|--|--|-----------------------|--|----|---|--|--|--|---|---|---|------------|---|-------|---|---|--|--|--|--|
| PMU_TOUCH_SLEEP_TIMER_EN<br>PMU_TOUCH_FORCE_DONE |    |     |  |  |  |  |  |  |  | PMU_TOUCH_SLEEP_CYCLES |  |    |  |  |  |  |  |  |  | PMU_TOUCH_WAIT_CYCLES |  |    |   |  |  |  |   |   |   | (reserved) |   |       |   |   |  |  |  |  |
| 31   | 30 | 29  |  |  |  |  |  |  |  |                        |  | 14 |  |  |  |  |  |  |  |                       |  | 13 | 5 |  |  |  |   |   |   |            |   |       | 4 | 0 |  |  |  |  |
| 0  | 0  | 100 |  |  |  |  |  |  |  |                        |  | 10 |  |  |  |  |  |  |  |                       |  | 0  |   |  |  |  | 0 | 0 | 0 | 0          | 0 | Reset |   |   |  |  |  |  |

**PMU\_TOUCH\_WAIT\_CYCLES** Configures the waiting time for the PMU to wake up from the TOUCH timer, with the unit of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_TOUCH\_SLEEP\_CYCLES** Configure the sleep time for TOUCH, with the unit of LP\_DYN\_SLOW\_CLK. (R/W)

**PMU\_TOUCH\_FORCE\_DONE** Force return to the working state of the TOUCH timer. (R/W)

**PMU\_TOUCH\_SLEEP\_TIMER\_EN** Enables the TOUCH timer to start working. (R/W)

**Register 13.72. PMU\_DATE\_REG (0x03FC)**

|            |           |              |       |
|------------|-----------|--------------|-------|
| PMU_CLK_EN |           | PMU_PMU_DATE |       |
| 31         | 30        | 0            |       |
| 0          | 0x2303140 |              | Reset |

**PMU\_PMU\_DATE** Version control register. (R/W)

**PMU\_CLK\_EN** Force enables the automatic clock gating of the register. (R/W)



## Chapter 14

## System Timer

### 14.1 Overview

ESP32-P4 provides a 52-bit system timer, which can be used to generate tick interrupts for the operating system, or be used as a general timer to generate periodic interrupts or one-time interrupts.

### 14.2 Features

The system timer has the following features:

- Two 52-bit counters and three 52-bit comparators
- Software accessing registers clocked by APB\_CLK
- CNT\_CLK used for counting, with an average frequency of 16 MHz in two counting cycles
- 40 MHz XTAL\_CLK as the clock source of CNT\_CLK
- 52-bit alarm values (t) and 26-bit alarm periods ( $\delta t$ )
- Two modes to generate alarms:
  - Target mode: only a one-time alarm is generated based on the alarm value (t)
  - Period mode: periodic alarms are generated based on the alarm period ( $\delta t$ )
- Three comparators generating three independent interrupts based on configured alarm value (t) or alarm period ( $\delta t$ )
- Software configuring the reference count value. For example, the system timer is able to load back the sleep time recorded by RTC timer via software after Light-sleep
- Able to stall or continue running when CPU stalls or enters the on-chip-debugging mode
- Alarm for Event Task Matrix (ETM) event

## 14.3 System Timer Structure

The timer consists of two counters: UNIT0 and UNIT1. The count values can be monitored by three comparators, COMP0, COMP1, and COMP2. See the timer block diagram in Figure 14.3-1.

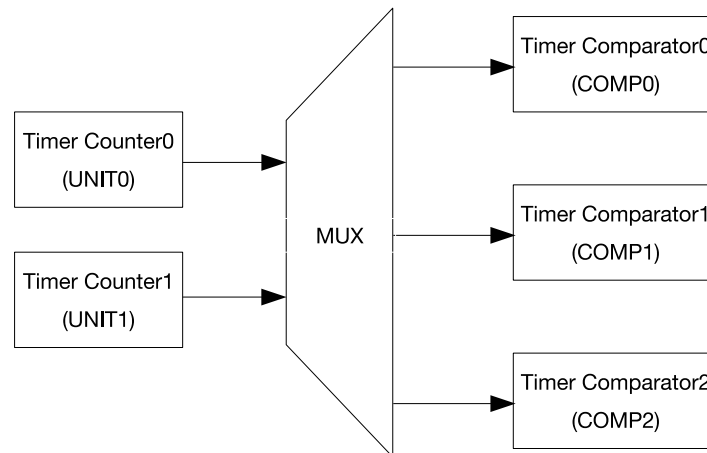


Figure 14.3-1. System Timer Structure

## 14.4 Clock Source Selection

The counters and comparators use XTAL\_CLK or RC\_FAST\_CLK as the clock sources. The clock source can be selected by configuring field HP\_SYS\_CLKRST\_REG\_SYSTIMER\_CLK\_SRC\_SEL in register [HP\\_SYS\\_CLKRST\\_PERI\\_CLK\\_CTRL21\\_REG](#). After XTAL\_CLK is scaled by 2.5, a counter clock signal CNT\_CLK is generated with a frequency of  $f_{XTAL\_CLK}/2.5$ . The average clock frequency of CNT\_CLK is 16 MHz, as shown in Figure 14.5-1. The timer counter is incremented by  $1/16\ \mu s$  on each CNT\_CLK cycle.

Software operation such as configuring registers is clocked by APB\_CLK. For more information about APB\_CLK, see Chapter 9 [Reset and Clock](#).

The following two bits of system registers are also used to control the system timer:

- Set HP\_SYS\_CLKRST\_REG\_SYSTIMER\_APB\_CLK\_EN in register [HP\\_SYS\\_CLKRST\\_SOC\\_CLK\\_CTRL2\\_REG](#) to enable APB\_CLK signal to the system timer.
- Set HP\_SYS\_CLKRST\_REG\_RST\_EN\_SYSTIMER in register [HP\\_SYS\\_CLKRST\\_HP\\_RST\\_EN1\\_REG](#) to reset the system timer.

Note that if the timer is reset, its registers will be restored to their default values. For more information, please refer to Chapter 9 [Reset and Clock](#).

## 14.5 Functional Description

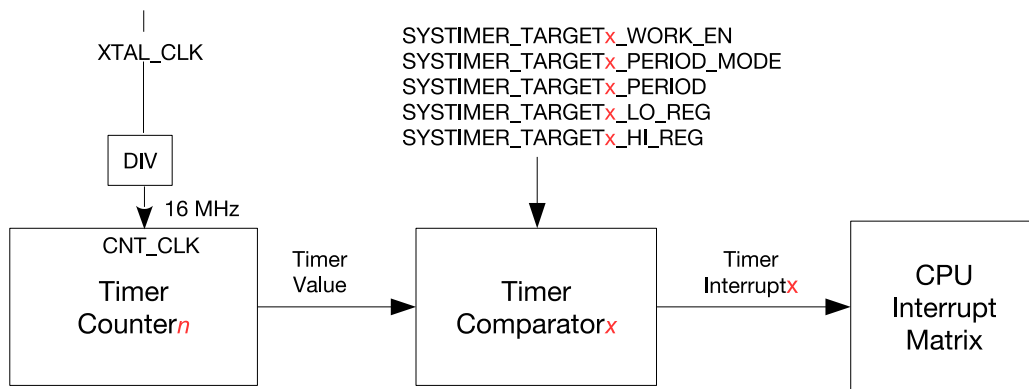


Figure 14.5-1. System Timer Alarm Generation

Figure 14.5-1 shows the procedure to generate alarm in system timer. In this process, one timer counter and one timer comparator are used. An alarm interrupt will be generated accordingly based on the comparison result in the comparator.

### 14.5.1 Counter

The system timer has two 52-bit timer counters, shown as UNIT $n$  ( $n = 0$  or  $1$ ). Their counting clock source is a 16 MHz clock, i.e., CNT\_CLK. Whether UNIT $n$  works or not is controlled by three bits in register SYSTIMER\_CONF\_REG:

- SYSTIMER\_TIMER\_UNIT $n$ \_WORK\_EN: set this bit to enable the counter UNIT $n$  in the system timer.
- SYSTIMER\_TIMER\_UNIT $n$ \_CORE0\_STALL\_EN: if this bit is set, the counter UNIT $n$  stops when CPU0 is stalled. The counter continues its counting after the CPU resumes.
- SYSTIMER\_TIMER\_UNIT $n$ \_CORE1\_STALL\_EN: if this bit is set, the counter UNIT $n$  stops when CPU1 is stalled. The counter continues its counting after the CPU resumes.

The configuration of the bits to control the counter UNIT $n$  is shown below, assuming that CPU is stalled.

Table 14.5-1. UNIT $n$  Configuration Bits

| SYSTIMER_TIMER_UNIT $n$ _WORK_EN | SYSTIMER_TIMER_UNIT $n$ _CORE0_STALL_EN | SYSTIMER_TIMER_UNIT $n$ _CORE1_STALL_EN | Counter UNIT $n$   |
|----------------------------------|---|---|--|
| 0                                | x <sup>*</sup>                          | x <sup>*</sup>                          | Not at work  |
| 1                                | 1                                       | x                                       | Stop counting, but will continue its counting after the CPU0 resumes |
| 1                                | x                                       | 1                                       | Stop counting, but will continue its counting after the CPU1 resumes |
| 1                                | 0                                       | 0                                       | Keep counting  |

<sup>\*</sup> x: Don't-care.

When the counter UNIT $n$  is at work, the count value is incremented on each counting cycle. When the counter UNIT $n$  is stopped, the count value stops increasing and keeps unchanged.

The lower 32 and higher 20 bits of the initial count value are loaded from the registers SYSTIMER\_TIMER\_UNIT $n$ \_LOAD\_LO and SYSTIMER\_TIMER\_UNIT $n$ \_LOAD\_HI. Writing 1 to the bit SYSTIMER\_TIMER\_UNIT $n$ \_LOAD will trigger a reload event, and the current count value will be changed immediately. If UNIT $n$  is at work, the counter will continue to count up from the new reloaded value.

Writing 1 to SYSTIMER\_TIMER\_UNIT $n$ \_UPDATE will trigger an update event. The lower 32 and higher 20 bits of the current count value will be locked into the registers SYSTIMER\_TIMER\_UNIT $n$ \_VALUE\_LO and SYSTIMER\_TIMER\_UNIT $n$ \_VALUE\_HI, and then SYSTIMER\_TIMER\_UNIT $n$ \_VALUE\_VALID is asserted. Before the next update event, the values of SYSTIMER\_TIMER\_UNIT $n$ \_VALUE\_LO and SYSTIMER\_TIMER\_UNIT $n$ \_VALUE\_HI remain unchanged.

## 14.5.2 Comparator and Alarm

The system timer has three 52-bit comparators, shown as COMP $x$  ( $x = 0, 1, \text{ or } 2$ ). The comparators can generate independent interrupts based on different alarm values ( $t$ ) or alarm periods ( $\delta t$ ).

Configure SYSTIMER\_TARGET $x$ \_PERIOD\_MODE to choose from the two alarm modes for each COMP $x$ :

- 1: period mode
- 0: target mode

In period mode, the alarm period ( $\delta t$ ) is provided by the register SYSTIMER\_TARGET $x$ \_PERIOD. Assuming that current count value is  $t_1$ , when it reaches  $(t_1 + \delta t)$ , an alarm interrupt will be generated. When the count value reaches  $(t_1 + 2 * \delta t)$ , another alarm interrupt also will be generated. By such way, periodic alarms are generated.

In target mode, the lower 32 bits and higher 20 bits of the alarm value ( $t$ ) are provided by SYSTIMER\_TIMER\_TARGET $x$ \_LO and SYSTIMER\_TIMER\_TARGET $x$ \_HI. Assuming that current count value is  $t_2$  ( $t_2 \leq t$ ), an alarm interrupt will be generated when the count value reaches the alarm value ( $t$ ). Unlike in period mode, only one alarm interrupt is generated in target mode.

SYSTIMER\_TARGET $x$ \_TIMER\_UNIT\_SEL is used to choose the count value from which timer counter to be compared to generate alarms:

- 1: Use the count value from UNIT1
- 0: Use the count value from UNIT0

Finally, set SYSTIMER\_TARGET $x$ \_WORK\_EN and COMP $x$  starts to compare the count value:

- In target mode, COMP $x$  compares it with the alarm value ( $t$ ).
- In period mode, COMP $x$  compares it with the alarm period ( $t_1 + n * \delta t$ ).

An alarm is generated when the count value equals to the alarm value ( $t$ ) in target mode or to the start value +  $n * \text{alarm period } \delta t$  ( $n = 1, 2, 3 \dots$ ) in period mode. But if the alarm value ( $t$ ) set in registers is less than the current count value, i.e., the target has already passed, when the current count value is larger than the alarm value ( $t$ ) within a range ( $0 \sim 2^{51} - 1$ ), an alarm interrupt will also be generated immediately. No matter in target mode or period mode, the low 32 bits and high 20 bits of the real alarm value can always be read from SYSTIMER\_TARGET $x$ \_LO\_RO and SYSTIMER\_TARGET $x$ \_HI\_RO. The alarm trigger point and the relationship between current count value  $t_c$  and the alarm value  $t_t$  are shown below.

Table 14.5-2. Trigger Point

| Relationship Between $t_c$ and $t_t$   | Trigger Point   |
|--|---|
| $t_c - t_t \leq 0$   | $t_c = t_t$ , an alarm is triggered.  |
| $0 \leq t_c - t_t < 2^{51} - 1$<br>( $t_c < 2^{51}$ and $t_t < 2^{51}$ ,<br>or $t_c \geq 2^{51}$ and $t_t \geq 2^{51}$ ) | An alarm is triggered immediately.  |
| $t_c - t_t \geq 2^{51} - 1$  | $t_c$ overflows after counting to its maximum value 52'hffffffffffff, and then starts counting up from 0. When its value reaches $t_t$ , an alarm is triggered. |

### 14.5.3 Event Task Matrix

The system timer on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows the system timer's ETM tasks to be triggered by any peripherals' ETM events, or system timer's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to the system timer. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

The system timer can generate the following ETM event:

- SYSTIMER\_EVT\_CNT\_CMP $x$ : Indicates the alarm events generated by COMP $x$ .

When [SYSTIMER\\_ETM\\_EN](#) is set to 1, the alarm events can trigger the ETM event.

### 14.5.4 Synchronization Operation

The frequency of the clock used for software configuration is different from that of the clock driving the timer counters and comparators. Therefore, synchronization is required for configuring some registers. The steps are as follows:

1. Software writes specific values to configuration fields. See the first column in Table 14.5-3.
2. Software writes 1 to corresponding bits to start synchronization. See the second column in Table 14.5-3.

Table 14.5-3. Synchronization Operation for Configuration Registers

| Configuration Fields  | Synchronization Enable Bit    |
|---|-------------------------------|
| SYSTIMER_TIMER_UNIT $n$ _LOAD_LO<br>SYSTIMER_TIMER_UNIT $n$ _LOAD_HI                          | SYSTIMER_TIMER_UNIT $n$ _LOAD |
| SYSTIMER_TARGET $x$ _PERIOD<br>SYSTIMER_TIMER_TARGET $x$ _HI<br>SYSTIMER_TIMER_TARGET $x$ _LO | SYSTIMER_TIMER_COMP $x$ _LOAD |

The frequency of the clock used for software reading is different from that of the clock driving the timer counters and comparators. Therefore, synchronization is also needed for reading some registers. The steps are as follows:

1. Software writes specific values to the updating register [SYSTIMER\\_TIMER\\_UNIT \$n\$ \\_UPDATE](#).

2. Software reads the corresponding bit `SYSTIMER_TIMER_UNIT $n$ _VALUE_VALID` to be valid to confirm synchronization is done.
3. Software reads the corresponding status registers `SYSTIMER_TIMER_UNIT $n$ _VALUE_HI` and `SYSTIMER_TIMER_UNIT $n$ _VALUE_LO`.

## 14.6 Interrupts

ESP32-P4's system timer can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- SYSTIMER\_TARGET0\_INT
- SYSTIMER\_TARGET1\_INT
- SYSTIMER\_TARGET2\_INT

There are several internal interrupt sources from the system timer that can generate the above interrupt signals. The interrupt sources from the system timer are listed with their trigger conditions and the resulted interrupt signals in Table 14.6-1.

Table 14.6-1. System Timer's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition | Interrupt Signal     |
|---------------------------|-------------------|----------------------|
| SYSTIMER_INT0             | When COMPO alarms | SYSTIMER_TARGET0_INT |
| SYSTIMER_INT1             | When COMP1 alarms | SYSTIMER_TARGET1_INT |
| SYSTIMER_INT2             | When COMP2 alarms | SYSTIMER_TARGET2_INT |

The above interrupts are level-type alarm interrupts. The interrupt signal is asserted high when the comparator starts to alarm. Until the software clears the interrupt, it remains high. To enable interrupts, set the bit `SYSTIMER_TARGET $x$ _INT_ENA`.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section 14.8 [Register Summary](#).

## 14.7 Programming Procedure

When configuring COMP $x$  and UNIT $n$ , please ensure the corresponding COMP and UNIT are at work.

### 14.7.1 Read Current Count Value

1. Set `SYSTIMER_TIMER_UNIT $n$ _UPDATE` to fill the current count value of COMP $x$  into `SYSTIMER_TIMER_UNIT $n$ _VALUE_HI` and `SYSTIMER_TIMER_UNIT $n$ _VALUE_LO`.

2. Poll the reading of `SYSTIMER_TIMER_UNIT $n$ _VALUE_VALID` till it is 1. Then, user can read the count value from `SYSTIMER_TIMER_UNIT $n$ _VALUE_HI` and `SYSTIMER_TIMER_UNIT $n$ _VALUE_LO`.
3. Read the lower 32 bits and higher 20 bits from `SYSTIMER_TIMER_UNIT $n$ _VALUE_LO` and `SYSTIMER_TIMER_UNIT $n$ _VALUE_HI` respectively.

## 14.7.2 Configure a One-Time Alarm in Target Mode

1. Set `SYSTIMER_TARGET $x$ _TIMER_UNIT_SEL` to select the counter (UNIT $0$  or UNIT $1$ ) used for comparison with COMP $x$ .
2. Read the current count value with reference to Section 14.7.1. This value will be used to calculate the alarm value (t) in Step 4.
3. Clear `SYSTIMER_TARGET $x$ _PERIOD_MODE` to enable target mode.
4. Set an alarm value (t), and fill its lower 32 bits into `SYSTIMER_TIMER_TARGET $x$ _LO`, and the higher 20 bits into `SYSTIMER_TIMER_TARGET $x$ _HI`.
5. Set `SYSTIMER_TIMER_COMP $x$ _LOAD` to synchronize the alarm value (t) to COMP $x$ , i.e., load the alarm value (t) to the COMP $x$ .
6. Set `SYSTIMER_TARGET $x$ _WORK_EN` to enable the selected COMP $x$ . COMP $x$  starts comparing the count value with the alarm value (t).
7. Set `SYSTIMER_TARGET $x$ _INT_ENA` to enable the timer interrupt. When UNIT $n$  reaches the alarm value (t), a `SYSTIMER_TARGET $x$ _INT` interrupt is triggered.

## 14.7.3 Configure Periodic Alarms in Period Mode

1. Set `SYSTIMER_TARGET $x$ _TIMER_UNIT_SEL` to select the counter (UNIT $0$  or UNIT $1$ ) used for comparison with COMP $x$ .
2. Set an alarm period ( $\delta t$ ), and fill it into `SYSTIMER_TARGET $x$ _PERIOD`.
3. Set `SYSTIMER_TIMER_COMP $x$ _LOAD` to synchronize the alarm period ( $\delta t$ ) to COMP $x$ , i.e., load the alarm period ( $\delta t$ ) to COMP $x$ .
4. Clear and then set `SYSTIMER_TARGET $x$ _PERIOD_MODE` to configure COMP $x$  into period mode.
5. Set `SYSTIMER_TARGET $x$ _WORK_EN` to enable the selected COMP $x$ . COMP $x$  starts comparing the count value with the sum of (start value +  $n \cdot \delta t$ ) ( $n = 1, 2, 3, \dots$ ).
6. Set `SYSTIMER_TARGET $x$ _INT_ENA` to enable the timer interrupt. A `SYSTIMER_TARGET $x$ _INT` interrupt is triggered when UNIT $n$  reaches start value +  $n \cdot \delta t$  ( $n = 1, 2, 3, \dots$ ) set in Step 2.

## 14.7.4 Update After Light-sleep

1. Configure RTC timer before the chip goes to Light-sleep mode, to record the exact sleep time. For more information, see Chapter 13 *Low-Power Management*.
2. Read the sleep time from the RTC timer when the chip wakes up from Light-sleep mode.
3. Read the current count value of system timer, see Section 14.7.1.

4. Convert the time value recorded by RTC timer from the clock cycles based on RTC\_SLOW\_CLK to that based on 16 MHz CNT\_CLK. For example, if the frequency of RTC\_SLOW\_CLK is 32 kHz, the recorded RTC timer value should be converted by multiplying by 500.
5. Add the converted RTC value to the current count value of system timer:
  - Fill the new value into SYSTIMER\_TIMER\_UNIT $n$ \_LOAD\_LO (low 32 bits) and SYSTIMER\_TIMER\_UNIT $n$ \_LOAD\_HI (high 20 bits).
  - Set SYSTIMER\_TIMER\_UNIT $n$ \_LOAD to load the new timer value into the system timer. By such way, the system timer is updated.



## 14.8 Register Summary

The addresses in this section are relative to system timer base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description                                     | Address | Access    |
|--|---|---------|-----------|
| <b>Clock Control Register</b>                          |   |         |           |
| <a href="#">SYSTIMER_CONF_REG</a>                      | Configure system timer clock                    | 0x0000  | R/W       |
| <b>UNIT0 Control and Configuration Registers</b>       |   |         |           |
| <a href="#">SYSTIMER_UNIT0_OP_REG</a>                  | Read UNIT0 value to registers                   | 0x0004  | varies    |
| <a href="#">SYSTIMER_UNIT0_LOAD_HI_REG</a>             | High 20 bits to be loaded to UNIT0              | 0x000C  | R/W       |
| <a href="#">SYSTIMER_UNIT0_LOAD_LO_REG</a>             | Low 32 bits to be loaded to UNIT0               | 0x0010  | R/W       |
| <a href="#">SYSTIMER_UNIT0_VALUE_HI_REG</a>            | UNIT0 value, high 20 bits                       | 0x0040  | RO        |
| <a href="#">SYSTIMER_UNIT0_VALUE_LO_REG</a>            | UNIT0 value, low 32 bits                        | 0x0044  | RO        |
| <a href="#">SYSTIMER_UNIT0_LOAD_REG</a>                | UNIT0 synchronization register                  | 0x005C  | WT        |
| <b>UNIT1 Control and Configuration Registers</b>       |   |         |           |
| <a href="#">SYSTIMER_UNIT1_OP_REG</a>                  | Read UNIT1 value to registers                   | 0x0008  | varies    |
| <a href="#">SYSTIMER_UNIT1_LOAD_HI_REG</a>             | High 20 bits to be loaded to UNIT1              | 0x0014  | R/W       |
| <a href="#">SYSTIMER_UNIT1_LOAD_LO_REG</a>             | Low 32 bits to be loaded to UNIT1               | 0x0018  | R/W       |
| <a href="#">SYSTIMER_UNIT1_VALUE_HI_REG</a>            | UNIT1 value, high 20 bits                       | 0x0048  | RO        |
| <a href="#">SYSTIMER_UNIT1_VALUE_LO_REG</a>            | UNIT1 value, low 32 bits                        | 0x004C  | RO        |
| <a href="#">SYSTIMER_UNIT1_LOAD_REG</a>                | UNIT1 synchronization register                  | 0x0060  | WT        |
| <b>Comparator0 Control and Configuration Registers</b> |   |         |           |
| <a href="#">SYSTIMER_TARGET0_HI_REG</a>                | Alarm value to be loaded to COMPO, high 20 bits | 0x001C  | R/W       |
| <a href="#">SYSTIMER_TARGET0_LO_REG</a>                | Alarm value to be loaded to COMPO, low 32 bits  | 0x0020  | R/W       |
| <a href="#">SYSTIMER_TARGET0_CONF_REG</a>              | Configure COMPO alarm mode                      | 0x0034  | R/W       |
| <a href="#">SYSTIMER_COMPO_LOAD_REG</a>                | COMPO synchronization register                  | 0x0050  | WT        |
| <b>Comparator1 Control and Configuration Registers</b> |   |         |           |
| <a href="#">SYSTIMER_TARGET1_HI_REG</a>                | Alarm value to be loaded to COMP1, high 20 bits | 0x0024  | R/W       |
| <a href="#">SYSTIMER_TARGET1_LO_REG</a>                | Alarm value to be loaded to COMP1, low 32 bits  | 0x0028  | R/W       |
| <a href="#">SYSTIMER_TARGET1_CONF_REG</a>              | Configure COMP1 alarm mode                      | 0x0038  | R/W       |
| <a href="#">SYSTIMER_COMP1_LOAD_REG</a>                | COMP1 synchronization register                  | 0x0054  | WT        |
| <b>Comparator2 Control and Configuration Registers</b> |   |         |           |
| <a href="#">SYSTIMER_TARGET2_HI_REG</a>                | Alarm value to be loaded to COMP2, high 20 bits | 0x002C  | R/W       |
| <a href="#">SYSTIMER_TARGET2_LO_REG</a>                | Alarm value to be loaded to COMP2, low 32 bits  | 0x0030  | R/W       |
| <a href="#">SYSTIMER_TARGET2_CONF_REG</a>              | Configure COMP2 alarm mode                      | 0x003C  | R/W       |
| <a href="#">SYSTIMER_COMP2_LOAD_REG</a>                | COMP2 synchronization register                  | 0x0058  | WT        |
| <b>Interrupt Registers</b>                             |   |         |           |
| <a href="#">SYSTIMER_INT_ENA_REG</a>                   | Interrupt enable register of system timer       | 0x0064  | R/W       |
| <a href="#">SYSTIMER_INT_RAW_REG</a>                   | Interrupt raw register of system timer          | 0x0068  | R/W/TC/SS |
| <a href="#">SYSTIMER_INT_CLR_REG</a>                   | Interrupt clear register of system timer        | 0x006C  | WT        |

| Name   | Description                                | Address | Access |
|--|--|---------|--------|
| <a href="#">SYSTIMER_INT_ST_REG</a>          | Interrupt status register of system timer  | 0x0070  | RO     |
| <b>COMP0 Status Registers</b>                |  |         |        |
| <a href="#">SYSTIMER_REAL_TARGET0_LO_REG</a> | Actual target value of COMP0, low 32 bits  | 0x0074  | RO     |
| <a href="#">SYSTIMER_REAL_TARGET0_HI_REG</a> | Actual target value of COMP0, high 20 bits | 0x0078  | RO     |
| <b>COMP1 Status Registers</b>                |  |         |        |
| <a href="#">SYSTIMER_REAL_TARGET1_LO_REG</a> | Actual target value of COMP1, low 32 bits  | 0x007C  | RO     |
| <a href="#">SYSTIMER_REAL_TARGET1_HI_REG</a> | Actual target value of COMP1, high 20 bits | 0x0080  | RO     |
| <b>COMP2 Status Registers</b>                |  |         |        |
| <a href="#">SYSTIMER_REAL_TARGET2_LO_REG</a> | Actual target value of COMP2, low 32 bits  | 0x0084  | RO     |
| <a href="#">SYSTIMER_REAL_TARGET2_HI_REG</a> | Actual target value of COMP2, high 20 bits | 0x0088  | RO     |
| <b>Version Register</b>                      |  |         |        |
| <a href="#">SYSTIMER_DATE_REG</a>            | Version control register                   | 0x00FC  | R/W    |

## 14.9 Registers

The addresses in this section are relative to system timer base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

### Register 14.1. SYSTIMER\_CONF\_REG (0x0000)

[illegible]

**SYSTIMER\_ETM\_EN** Configures whether to enable generation of ETM events.

0: Disable

1: Enable

(R/W)

**SYSTIMER\_TARGET2\_WORK\_EN** Configures whether to enable COMP2.

0: Disable

1: Enable

(R/W)

**SYSTIMER\_TARGET1\_WORK\_EN** Configures whether to enable COMP1. See details in [SYSTIMER\\_TARGET2\\_WORK\\_EN](#). (R/W)

**SYSTIMER\_TARGET0\_WORK\_EN** Configures whether to enable COMPO. See details in [SYSTIMER\\_TARGET2\\_WORK\\_EN](#). (R/W)

**SYSTIMER\_TIMER\_UNIT1\_CORE1\_STALL\_EN** Configures whether UNIT1 is stalled when CORE1 is stalled.

0: UNIT1 is not stalled.

1: UNIT1 is stalled.

(R/W)

**SYSTIMER\_TIMER\_UNIT1\_CORE0\_STALL\_EN** Configures whether UNIT1 is stalled when CORE0 is stalled. See details in [SYSTIMER\\_TIMER\\_UNIT1\\_CORE1\\_STALL\\_EN](#). (R/W)

**SYSTIMER\_TIMER\_UNIT0\_CORE1\_STALL\_EN** Configures whether UNIT0 is stalled when CORE1 is stalled. See details in [SYSTIMER\\_TIMER\\_UNIT1\\_CORE1\\_STALL\\_EN](#). (R/W)

**SYSTIMER\_TIMER\_UNIT0\_CORE0\_STALL\_EN** Configures whether UNIT0 is stalled when CORE0 is stalled. See details in [SYSTIMER\\_TIMER\\_UNIT1\\_CORE1\\_STALL\\_EN](#). (R/W)

Continued on the next page...

### Register 14.1. SYSTIMER\_CONF\_REG (0x0000)

Continued from the previous page...

**SYSTIMER\_TIMER\_UNIT1\_WORK\_EN** Configures whether to enable UNIT1.

0: Disable

1: Enable

(R/W)

**SYSTIMER\_TIMER\_UNITO\_WORK\_EN** Configures whether to enable UNITO.

0: Disable

1: Enable

(R/W)

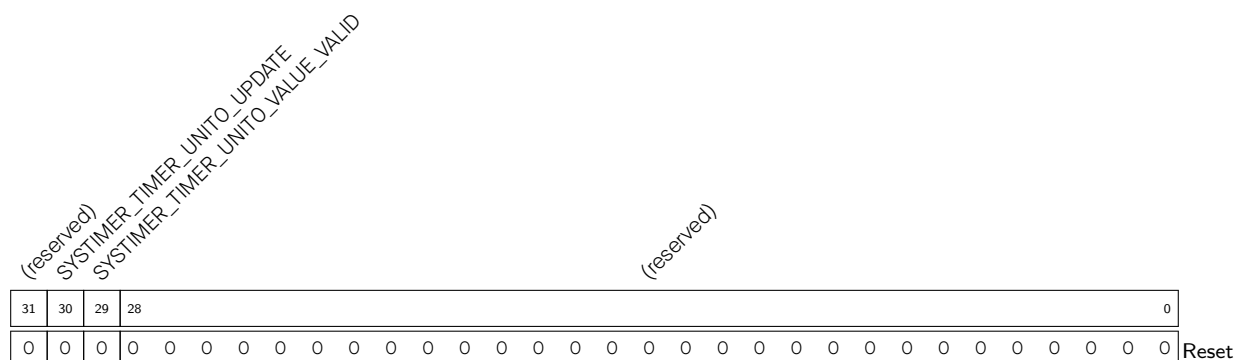
**SYSTIMER\_CLK\_EN** Configures register clock gating.

0: Only enable needed clock for register read or write operations.

1: Register clock is always enabled for read and write operations.

(R/W)

### Register 14.2. SYSTIMER\_UNIT0\_OP\_REG (0x0004)



**SYSTIMER\_TIMER\_UNITO\_VALUE\_VALID** Represents whether UNITO value is synchronized and valid.

0: UNIT0 value is neither synchronized nor valid

1: UNIT0 value is synchronized and valid

(R/SS/WTC)

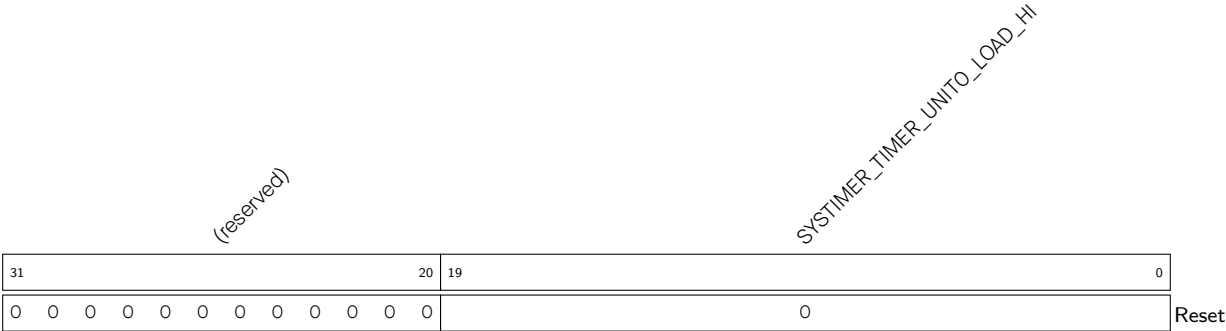
**SYSTIMER\_TIMER\_UNITO\_UPDATE** Configures whether to update timer UNITO, i.e., reads the UNITO count value to **SYSTIMER\_TIMER\_UNITO\_VALUE\_HI** and **SYSTIMER\_TIMER\_UNITO\_VALUE\_LO**.

0: No effect

1: Update timer UNITO

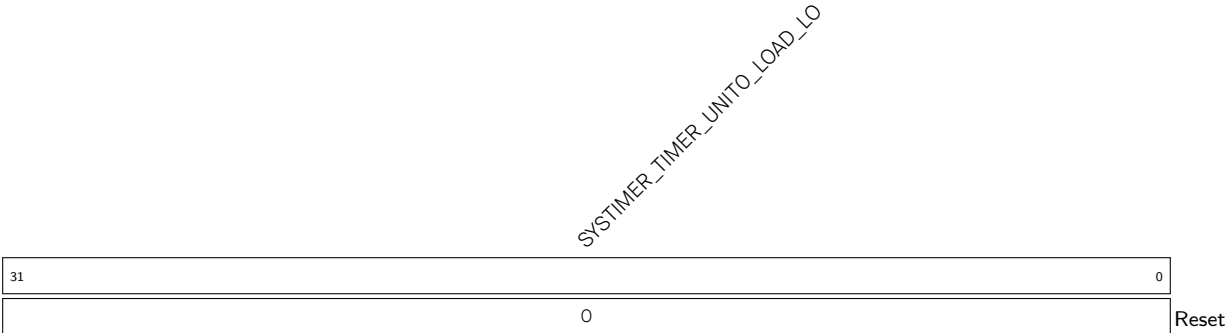
(WT)

Register 14.3. SYSTIMER\_UNITO\_LOAD\_HI\_REG (0x000C)



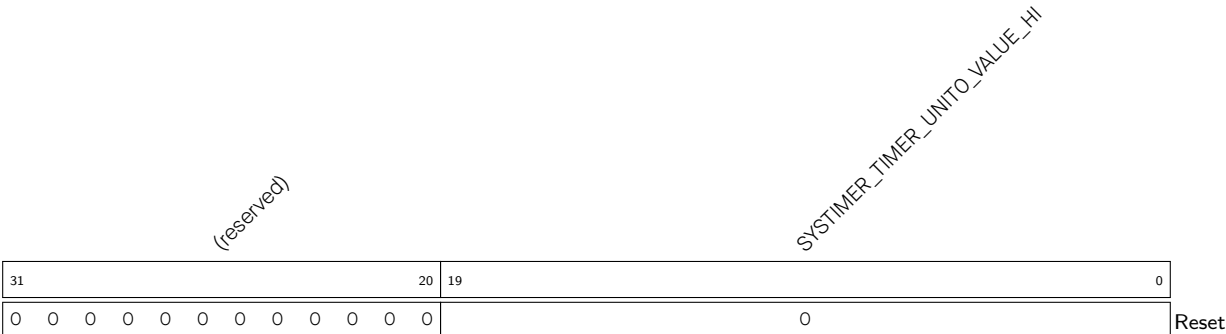
**SYSTIMER\_TIMER\_UNITO\_LOAD\_HI** Configures the value to be loaded to UNITO, high 20 bits. (R/W)

Register 14.4. SYSTIMER\_UNITO\_LOAD\_LO\_REG (0x0010)



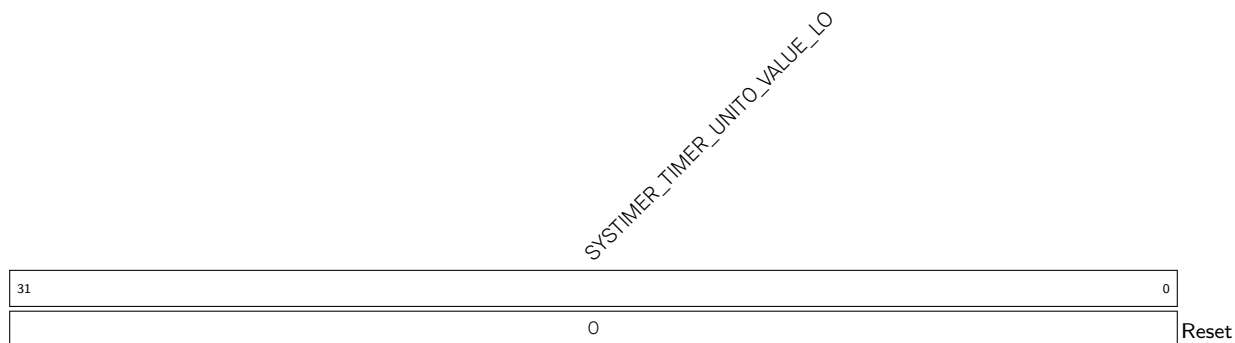
**SYSTIMER\_TIMER\_UNITO\_LOAD\_LO** Configures the value to be loaded to UNITO, low 32 bits. (R/W)

Register 14.5. SYSTIMER\_UNITO\_VALUE\_HI\_REG (0x0040)



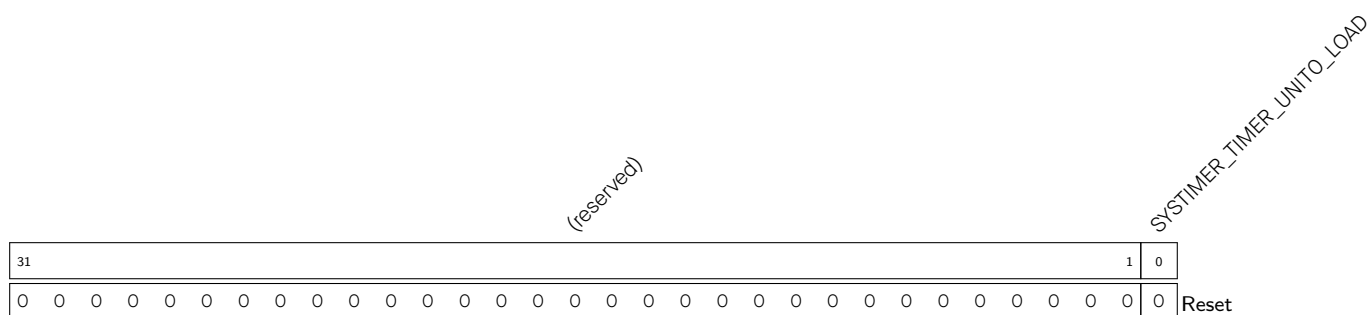
**SYSTIMER\_TIMER\_UNITO\_VALUE\_HI** Represents UNITO read value, high 20 bits. (RO)

### Register 14.6. SYSTIMER\_UNIT0\_VALUE\_LO\_REG (0x0044)



**SYSTIMER\_TIMER\_UNIT0\_VALUE\_LO** Represents UNIT0 read value, low 32 bits. (RO)

### Register 14.7. SYSTIMER\_UNIT0\_LOAD\_REG (0x005C)



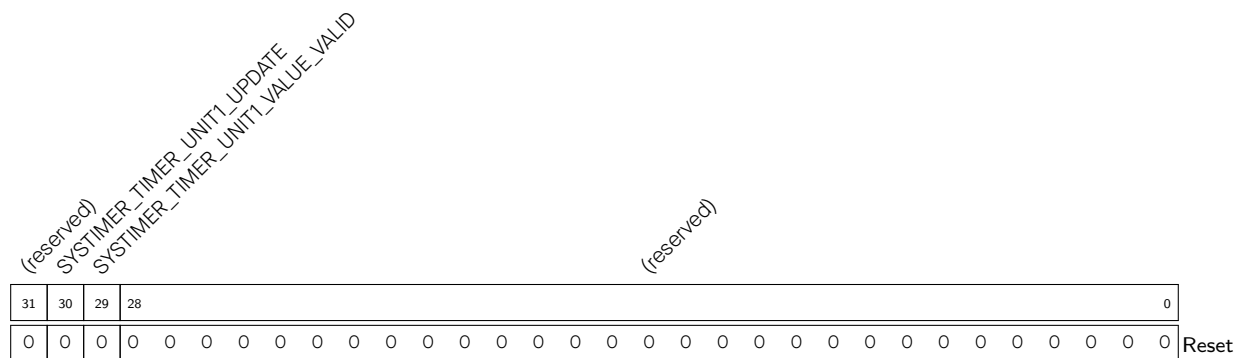
**SYSTIMER\_TIMER\_UNITO\_LOAD** Configures whether to reload the value of UNITO, i.e., reloads the values of **SYSTIMER\_TIMER\_UNITO\_VALUE\_HI** and **SYSTIMER\_TIMER\_UNITO\_VALUE\_LO** to UNITO.

0: No effect

1: Reload the value of UNIT0

(WT)

### Register 14.8. SYSTIMER\_UNIT1\_OP\_REG (0x0008)



**SYSTIMER\_TIMER\_UNIT1\_VALUE\_VALID** Represents UNIT1 value is synchronized and valid.  
(R/SS/WTC)

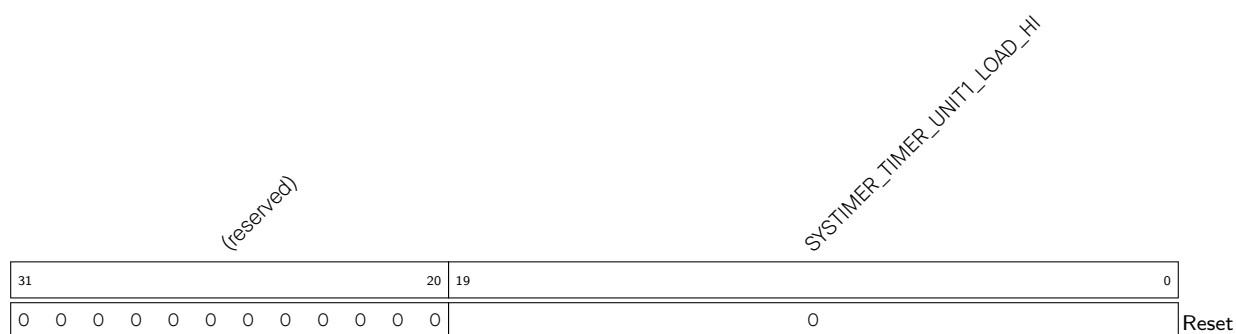
**SYSTIMER\_TIMER\_UNIT1\_UPDATE** Configures whether to update timer UNIT1, i.e., reads the UNIT1 count value to [SYSTIMER\\_TIMER\\_UNIT1\\_VALUE\\_HI](#) and [SYSTIMER\\_TIMER\\_UNIT1\\_VALUE\\_LO](#).

0: No effect

1: Update timer UNIT1

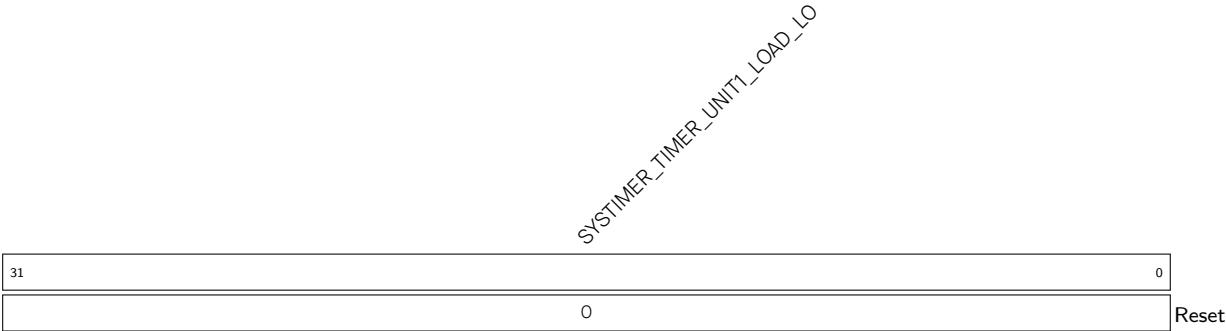
(WT)

### Register 14.9. SYSTIMER\_UNIT1\_LOAD\_HI\_REG (0x0014)



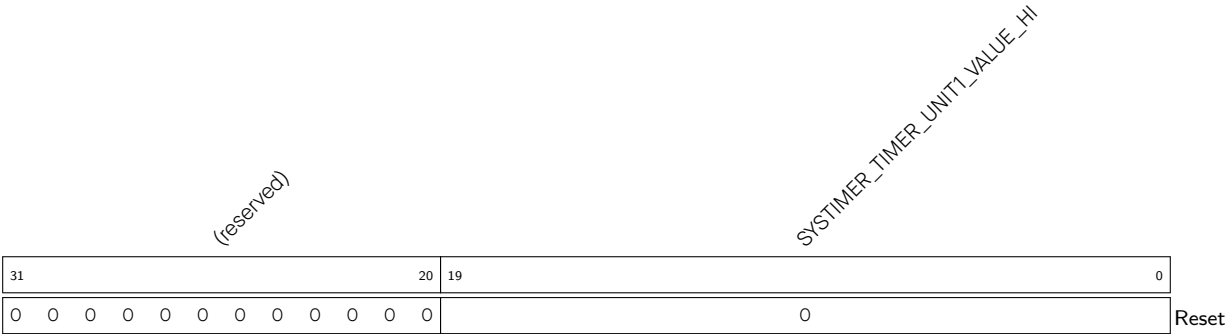
**SYSTIMER\_TIMER\_UNIT1\_LOAD\_HI** Configures the value to be loaded to UNIT1, high 20 bits. (R/W)

Register 14.10. SYSTIMER\_UNIT1\_LOAD\_LO\_REG (0x0018)



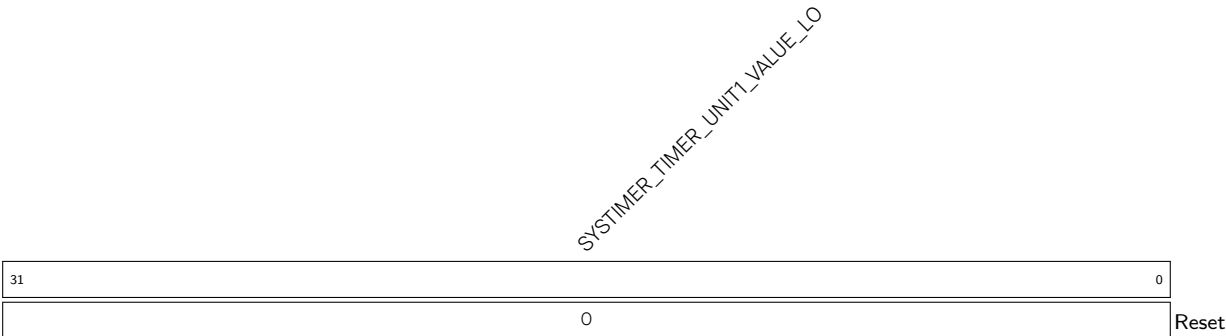
**SYSTIMER\_TIMER\_UNIT1\_LOAD\_LO** Configures the value to be loaded to UNIT1, low 32 bits. (R/W)

Register 14.11. SYSTIMER\_UNIT1\_VALUE\_HI\_REG (0x0048)



**SYSTIMER\_TIMER\_UNIT1\_VALUE\_HI** Represents UNIT1 read value, high 20 bits. (RO)

Register 14.12. SYSTIMER\_UNIT1\_VALUE\_LO\_REG (0x004C)



**SYSTIMER\_TIMER\_UNIT1\_VALUE\_LO** Represents UNIT1 read value, low 32 bits. (RO)



### Register 14.13. SYSTIMER\_UNIT1\_LOAD\_REG (0x0060)

Diagram of the SYSTIMER\_TIMER\_LOAD register structure:

- Bit 31: (reserved)
- Bits 31-1: (reserved)
- Bit 0: SYSTIMER\_TIMER\_UNIT1\_LOAD
- Reset value: 0

**SYSTIMER\_TIMER\_UNIT1\_LOAD** Configures whether to reload the value of UNIT1, i.e., reload the values of [SYSTIMER\\_TIMER\\_UNIT1\\_VALUE\\_HI](#) and [SYSTIMER\\_TIMER\\_UNIT1\\_VALUE\\_LO](#) to UNIT1.

0: No effect

1: Reload the value of UNIT1

(WT)

#### Register 14.14. SYSTIMER\_TARGETO\_HI\_REG (0x001C)

Diagram illustrating the structure of the SYSTIMER\_TMR register:

- Bits 31 to 20: (reserved)
- Bits 19 to 0: SYSTIMER\_TIMER\_TARGET0\_HI

The register is shown as a horizontal bar with bit positions 31, 20, 19, and 0 marked. The reserved field contains 12 zeros. The SYSTIMER\_TIMER\_TARGET0\_HI field contains a single zero in bit 19 and zeros in bits 18-0.

**SYSTIMER\_TIMER\_TARGETO\_HI** Configures the alarm value to be loaded to COMPO, high 20 bits.

(R/W)

### Register 14.15. SYSTIMER\_TARGET0\_LO\_REG (0x0020)

31 0

Reset

SYSTIMER\_TMR\_TARGET0\_LO

**SYSTIMER\_TIMER\_TARGETO\_LO** Configures the alarm value to be loaded to COMPO, low 32 bits.

(R/W)

Register 14.16. SYSTIMER\_TARGETO\_CONF\_REG (0x0034)

|    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |         |  |  |
|----|--|--|----|--|--|----|--|--|----|--|--|----|--|--|---------|--|--|
| 31 |  |  | 30 |  |  | 29 |  |  | 26 |  |  | 25 |  |  | 0       |  |  |
|    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |         |  |  |
| 0  |  |  | 0  |  |  | 0  |  |  | 0  |  |  | 0  |  |  | 0x00000 |  |  |
|    |  |  |    |  |  |    |  |  |    |  |  |    |  |  |         |  |  |

SYSTIMER\_TARGETO\_TIMER\_UNIT\_SEL

SYSTIMER\_TARGETO\_PERIOD\_MODE

(reserved)

SYSTIMER\_TARGETO\_PERIOD

Reset

- SYSTIMER\_TARGETO\_PERIOD** Configures COMPO alarm period. (R/W)
- SYSTIMER\_TARGETO\_PERIOD\_MODE** Selects the two alarm modes for COMPO.

0: Target mode

1: Period mode

(R/W)
- SYSTIMER\_TARGETO\_TIMER\_UNIT\_SEL** Chooses the count value for comparison with COMPO.

0: Use the count value from UNIT0

1: Use the count value from UNIT1

(R/W)

Register 14.17. SYSTIMER\_COMPO\_LOAD\_REG (0x0050)

|    |  |  |   |  |  |   |  |  |
|----|--|--|---|--|--|---|--|--|
| 31 |  |  | 1 |  |  | 0 |  |  |
|    |  |  |   |  |  |   |  |  |
| 0  |  |  | 0 |  |  | 0 |  |  |
|    |  |  |   |  |  |   |  |  |

(reserved)

SYSTIMER\_TIMER\_COMPO\_LOAD

Reset

- SYSTIMER\_TIMER\_COMPO\_LOAD** Configures whether to enable COMPO synchronization, i.e., reload the alarm value/period to COMPO.

0: No effect

1: Enable COMPO synchronization

(WT)

Register 14.18. SYSTIMER\_TARGET1\_HI\_REG (0x0024)

|            |   |   |   |   |   |   |   |   |   |   |    |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|----|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |    | SYSTIMER_TIMER_TARGET1_HI |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   | 20 | 0                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**SYSTIMER\_TIMER\_TARGET1\_HI** Configures the alarm value to be loaded to COMP1, high 20 bits.  
(R/W)

Register 14.19. SYSTIMER\_TARGET1\_LO\_REG (0x0028)

|                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| SYSTIMER_TIMER_TARGET1_LO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**SYSTIMER\_TIMER\_TARGET1\_LO** Configures the alarm value to be loaded to COMP1, low 32 bits.  
(R/W)

Register 14.20. SYSTIMER\_TARGET1\_CONF\_REG (0x0038)

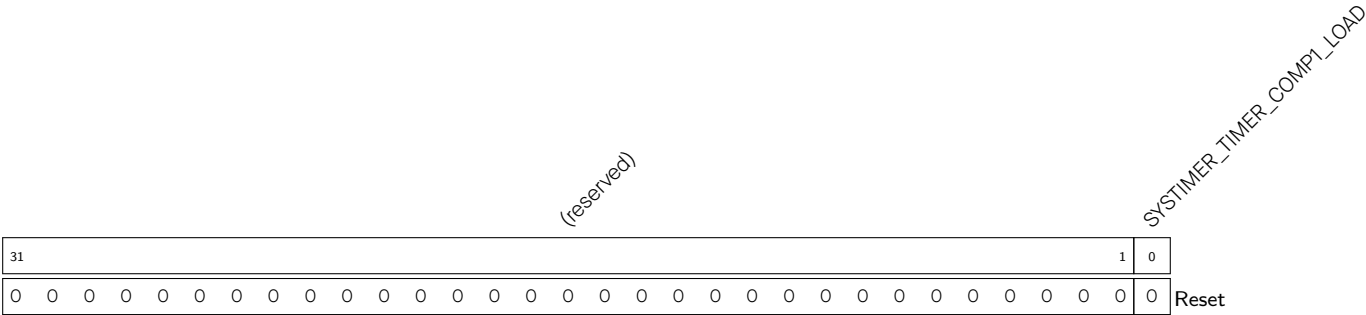
|                                 |    |    |            |   |   |                              |  |  |  |  |  |  |    |    |  |                         |         |  |  |  |  |  |  |  |  |  |  |  |       |
|---------------------------------|----|----|------------|---|---|------------------------------|--|--|--|--|--|--|----|----|--|-------------------------|---------|--|--|--|--|--|--|--|--|--|--|--|-------|
| SYSTIMER_TARGET1_TIMER_UNIT_SEL |    |    |            |   |   | SYSTIMER_TARGET1_PERIOD_MODE |  |  |  |  |  |  |    |    |  | SYSTIMER_TARGET1_PERIOD |         |  |  |  |  |  |  |  |  |  |  |  |       |
| 31                              | 30 | 29 | (reserved) |   |   |                              |  |  |  |  |  |  | 26 | 25 |  |                         |         |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0                               | 0  | 0  | 0          | 0 | 0 | 0                            |  |  |  |  |  |  |    |    |  |                         | 0x00000 |  |  |  |  |  |  |  |  |  |  |  | Reset |

**SYSTIMER\_TARGET1\_PERIOD** Configures COMP1 alarm period. (R/W)

**SYSTIMER\_TARGET1\_PERIOD\_MODE** Selects the two alarm modes for COMP1. See details in [SYSTIMER\\_TARGET0\\_PERIOD\\_MODE](#). (R/W)

**SYSTIMER\_TARGET1\_TIMER\_UNIT\_SEL** Chooses the count value for comparison with COMP1. See details in [SYSTIMER\\_TARGET0\\_TIMER\\_UNIT\\_SEL](#). (R/W)

Register 14.21. SYSTIMER\_COMP1\_LOAD\_REG (0x0054)

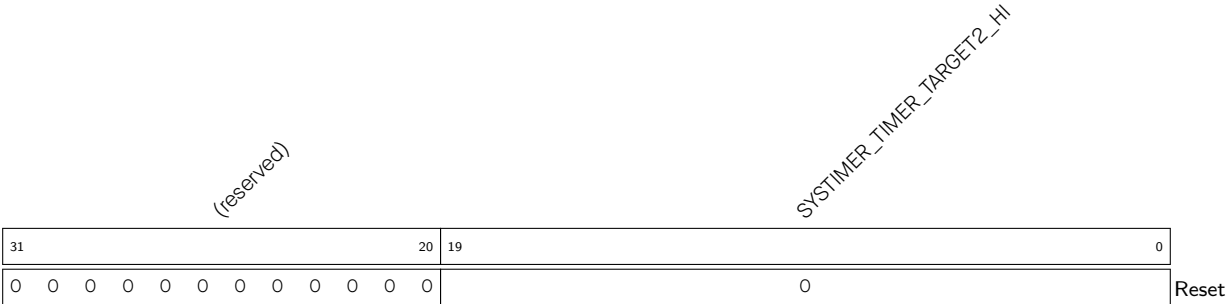


**SYSTIMER\_TIMER\_COMP1\_LOAD** Configures whether to enable COMP1 synchronization, i.e., reload the alarm value/period to COMP1.

0: No effect

1: Enable COMP1 synchronization (WT)

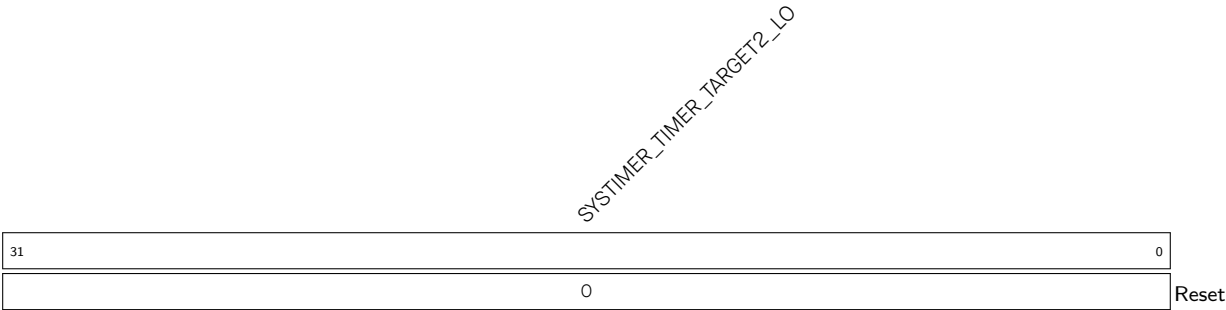
Register 14.22. SYSTIMER\_TARGET2\_HI\_REG (0x002C)



**SYSTIMER\_TIMER\_TARGET2\_HI** Configures the alarm value to be loaded to COMP2, high 20 bits.

(R/W)

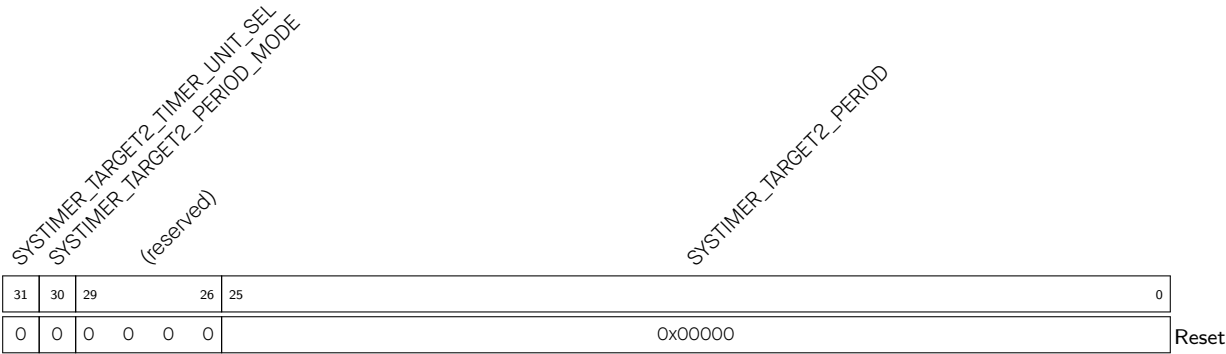
Register 14.23. SYSTIMER\_TARGET2\_LO\_REG (0x0030)



**SYSTIMER\_TIMER\_TARGET2\_LO** Configures the alarm value to be loaded to COMP2, low 32 bits.

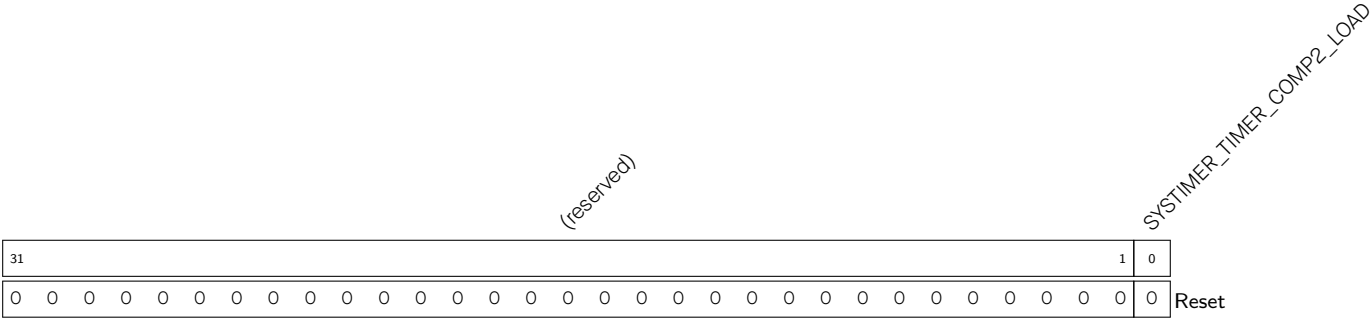
(R/W)

Register 14.24. SYSTIMER\_TARGET2\_CONF\_REG (0x003C)

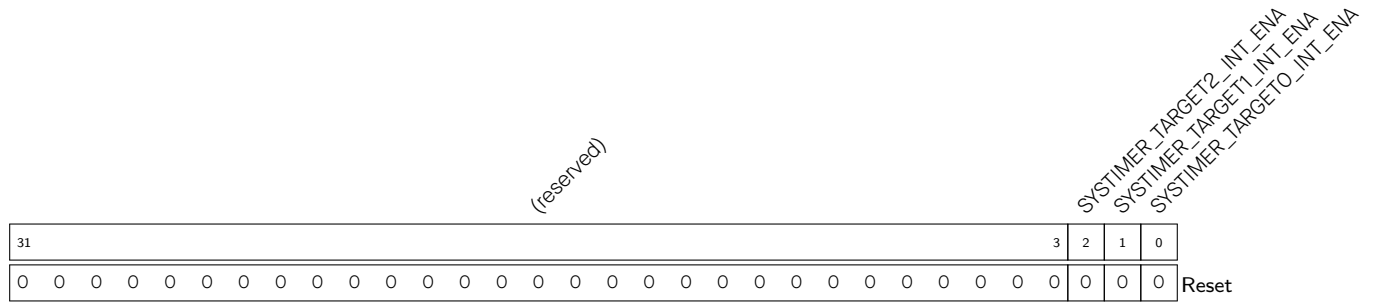


- SYSTIMER\_TARGET2\_PERIOD** Configures COMP2 alarm period. (R/W)
- SYSTIMER\_TARGET2\_PERIOD\_MODE** Configures Configures the two alarm modes for COMP2. See details in [SYSTIMER\\_TARGET2\\_PERIOD\\_MODE](#). (R/W)
- SYSTIMER\_TARGET2\_TIMER\_UNIT\_SEL** Chooses the count value for comparison with COMP2. See details in [SYSTIMER\\_TARGET2\\_TIMER\\_UNIT\\_SEL](#). (R/W)

Register 14.25. SYSTIMER\_COMP2\_LOAD\_REG (0x0058)



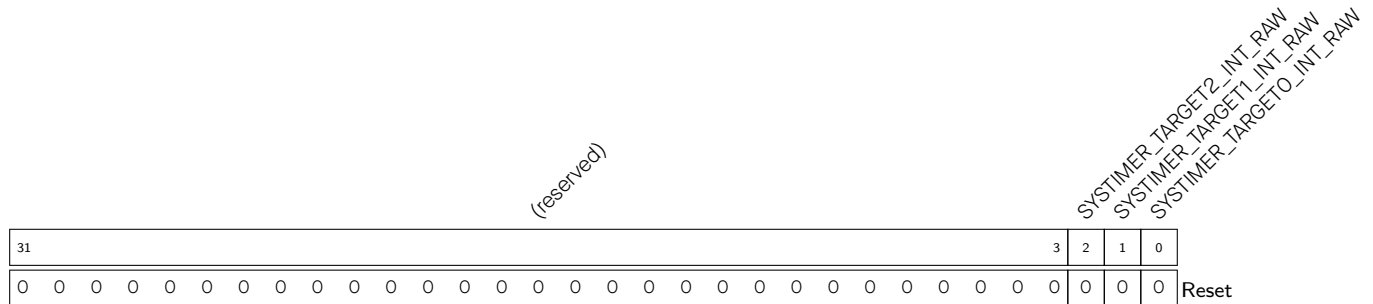
- SYSTIMER\_TIMER\_COMP2\_LOAD** Configures whether to enable COMP2 synchronization, i.e., reload the alarm value/period to COMP2.  
0: No effect  
1: Enable COMP2 synchronization (WT)

**Register 14.26. SYSTIMER\_INT\_ENA\_REG (0x0064)**

**SYSTIMER\_TARGET0\_INT\_ENA** Write 1 to enable SYSTIMER\_TARGET0\_INT. (R/W)

**SYSTIMER\_TARGET1\_INT\_ENA** Write 1 to enable SYSTIMER\_TARGET1\_INT. (R/W)

**SYSTIMER\_TARGET2\_INT\_ENA** Write 1 to enable SYSTIMER\_TARGET2\_INT. (R/W)

**Register 14.27. SYSTIMER\_INT\_RAW\_REG (0x0068)**

**SYSTIMER\_TARGET0\_INT\_RAW** The raw interrupt status of SYSTIMER\_TARGET0\_INT. (R/WTC/SS)

**SYSTIMER\_TARGET1\_INT\_RAW** The raw interrupt status of SYSTIMER\_TARGET1\_INT. (R/WTC/SS)

**SYSTIMER\_TARGET2\_INT\_RAW** The raw interrupt status of SYSTIMER\_TARGET2\_INT. (R/WTC/SS)

Register 14.28. SYSTIMER\_INT\_CLR\_REG (0x006C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SYSTIMER_TARGET2_INT_CLR<br>SYSTIMER_TARGET1_INT_CLR<br>SYSTIMER_TARGET0_INT_CLR |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 |

Reset

**SYSTIMER\_TARGET0\_INT\_CLR** Write 1 to clear SYSTIMER\_TARGET0\_INT. (WT)

**SYSTIMER\_TARGET1\_INT\_CLR** Write 1 to clear SYSTIMER\_TARGET1\_INT. (WT)

**SYSTIMER\_TARGET2\_INT\_CLR** Write 1 to clear SYSTIMER\_TARGET2\_INT. (WT)

Register 14.29. SYSTIMER\_INT\_ST\_REG (0x0070)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SYSTIMER_TARGET2_INT_ST<br>SYSTIMER_TARGET1_INT_ST<br>SYSTIMER_TARGET0_INT_ST |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3   | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 |

Reset

**SYSTIMER\_TARGET0\_INT\_ST** The masked interrupt status of SYSTIMER\_TARGET0\_INT. (RO)

**SYSTIMER\_TARGET1\_INT\_ST** The masked interrupt status of SYSTIMER\_TARGET1\_INT. (RO)

**SYSTIMER\_TARGET2\_INT\_ST** The masked interrupt status of SYSTIMER\_TARGET2\_INT. (RO)

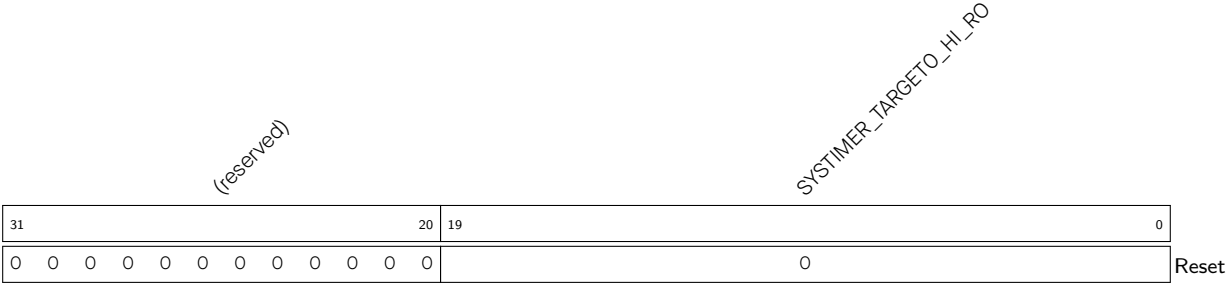
Register 14.30. SYSTIMER\_REAL\_TARGET0\_LO\_REG (0x0074)

|                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| SYSTIMER_TARGET0_LO_RO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

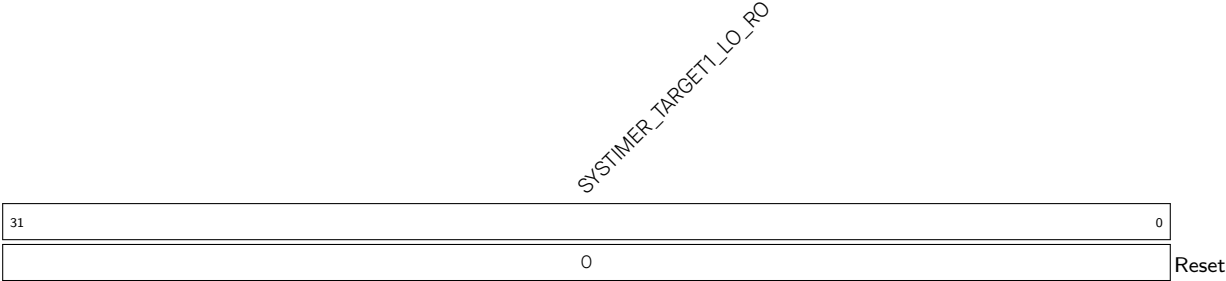
**SYSTIMER\_TARGET0\_LO\_RO** Represents the actual target value of COMPO, low 32 bits. (RO)

Register 14.31. SYSTIMER\_REAL\_TARGET0\_HI\_REG (0x0078)



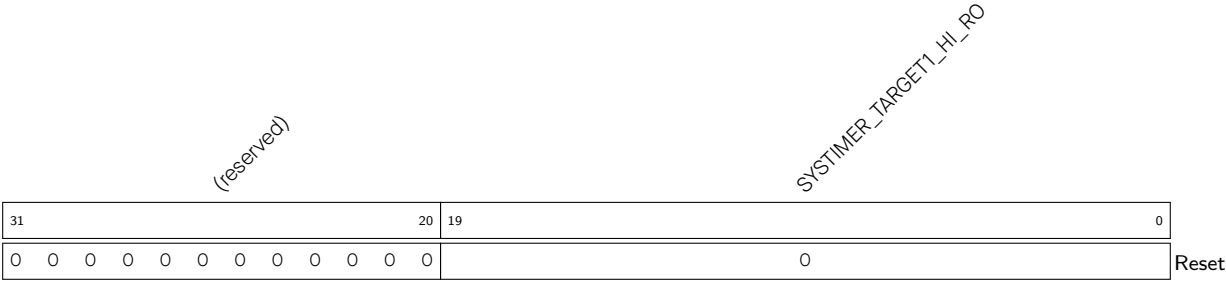
**SYSTIMER\_TARGET0\_HI\_RO** Represents the actual target value of COMP0, high 20 bits. (RO)

Register 14.32. SYSTIMER\_REAL\_TARGET1\_LO\_REG (0x007C)



**SYSTIMER\_TARGET1\_LO\_RO** Represents the actual target value of COMP1, low 32 bits. (RO)

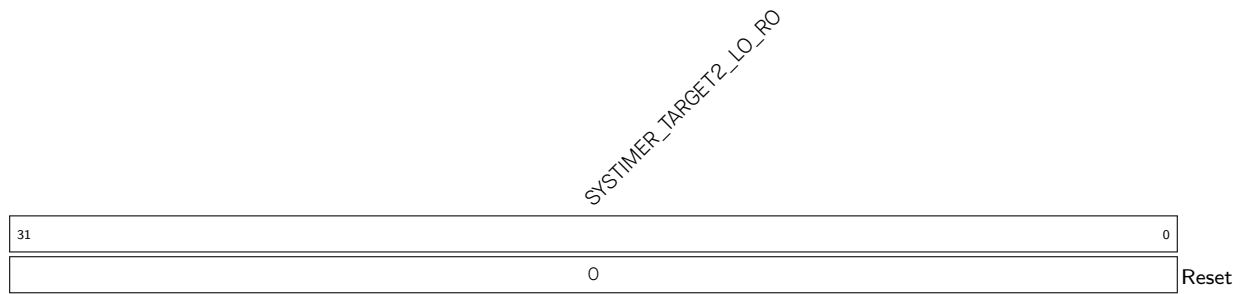
Register 14.33. SYSTIMER\_REAL\_TARGET1\_HI\_REG (0x0080)



**SYSTIMER\_TARGET1\_HI\_RO** Represents the actual target value of COMP1, high 20 bits. (RO)



### Register 14.34. SYSTIMER\_REAL\_TARGET2\_LO\_REG (0x0084)



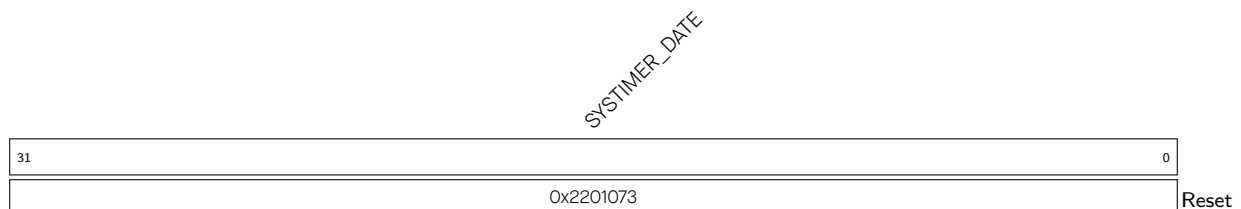
**SYSTIMER\_TARGET2\_LO\_RO** Represents the actual target value of COMP2, low 32 bits. (RO)

### Register 14.35. SYSTIMER\_REAL\_TARGET2\_HI\_REG (0x0088)



**SYSTIMER\_TARGET2\_HI\_RO** Represents the actual target value of COMP2, high 20 bits. (RO)

### Register 14.36. SYSTIMER\_DATE\_REG (0x00FC)



**SYSTIMER\_DATE** Version control register. (R/W)

## Chapter 15

### Timer Group (TIMG)

#### 15.1 Overview

General-purpose timers can be used to precisely time an interval, trigger an interrupt after a particular interval (periodically and aperiodically), or act as a hardware clock. As shown in Figure 15.1-1, the ESP32-P4 chip contains two timer groups, namely timer group 0 and timer group 1 (hereinafter referred to as TIMG $n$ , where  $n$  can be 0 or 1). Each timer group consists of two general-purpose timers (hereinafter referred to as T $x$ , where  $x$  can be 0 or 1) and one Main System Watchdog Timer (MWDT). The general-purpose timer is based on a 16-bit prescaler and a 54-bit auto-reload-capable up-down counter.

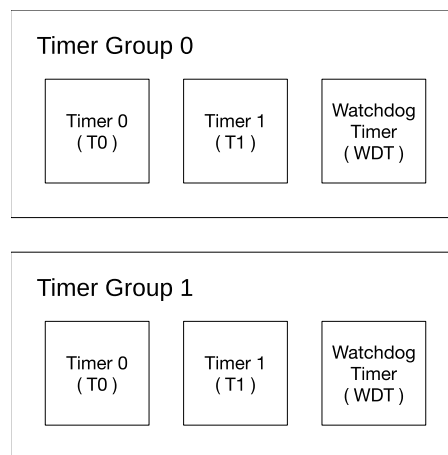


Figure 15.1-1. Timer Group Overview

Note that while the Main System Watchdog Timer registers are described in this chapter, their functional description is included in Chapter 16 [Watchdog Timers \(WDT\)](#). Therefore, the term “timer” within this chapter refers to the general-purpose timer.

#### 15.2 Features

The timer’s features are summarized as follows:

- A 54-bit time-base counter programmable to incrementing or decrementing
- Three clock sources: PLL\_F80M\_CLK or XTAL\_CLK or RC\_FAST\_CLK
- A 16-bit clock prescaler, from 2 to 65536
- Able to read real-time value of the time-base counter
- Able to halt and resume the time-base counter

- Programmable alarm generation
- Timer value reload — Auto-reload at alarm or software-controlled instant reload
- Calculate clock frequency — Calculate the measured frequency of the clock, which can be called TIMGO\_CALI\_CLK, based on the crystal clock
- Level interrupt generation
- Support several ETM tasks and events

## 15.3 Functional Description

Figure 15.3-1 shows Timer Tx in timer group TIMGn. Tx contains a 16-bit integer divider as a prescaler, a timer-based counter, and a comparator for alarm generation.

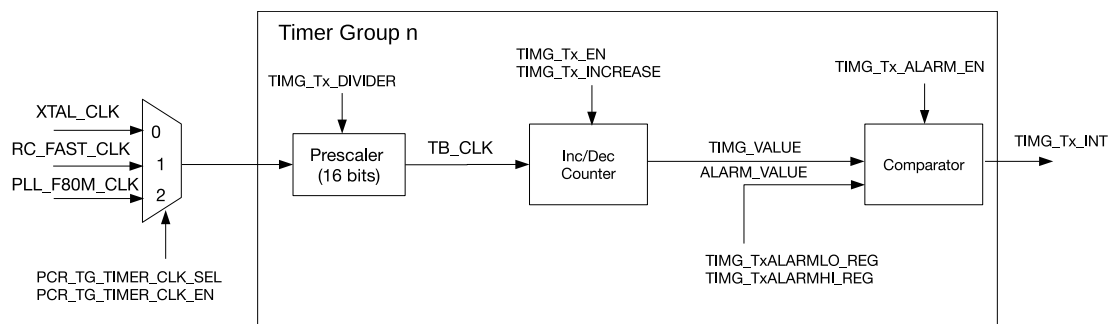


Figure 15.3-1. Timer Group Architecture

### 15.3.1 16-bit Prescaler and Clock Selection

Take the Timer Tx in timer group TIMGn as an example:

- The timer can select its clock source by setting the HP\_SYS\_CLKRST\_TIMERGRPn\_Tx\_SRC\_SEL field of the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL20\_REG register or the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL21\_REG register. When the field is 0, XTAL\_CLK is selected; when the field is 1, RC\_FAST\_CLK is selected and when the field is 2, PLL\_F80M\_CLK is selected.
- The selected clock can be switched on by setting HP\_SYS\_CLKRST\_TIMERGRPn\_Tx\_CLK\_EN field of the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL20\_REG register or the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL21\_REG register to 1 and switched off by setting it to 0. The clock is then divided by a 16-bit prescaler to generate the time-base counter clock (TB\_CLK) used by the time-base counter. The divisor of the prescaler can be configured through the TIMG\_Tx\_DIVIDER field.

TIMG\_Tx\_DIVIDER field can be configured as 0 ~ 65535 for a divisor range of 2 ~ 65536. To be more specific, when TIMG\_Tx\_DIVIDER is configured as:

- 0: the divisor is 65536
- 1: the divisor is 2
- 2: the divisor is also 2
- 3 ~ 65535: the divisor is 3 ~ 65535

To modify the 16-bit prescaler, please first configure the `TIMG_Tx_DIVIDER` field, and then set `TIMG_Tx_DIVCNT_RST` to 1. Meanwhile, the timer must be disabled (i.e., `TIMG_Tx_EN` should be cleared). Otherwise, the result can be unpredictable.

### 15.3.2 54-bit Time-base Counter

The 54-bit time-base counter is based on `TB_CLK` and can be configured to increment or decrement via the `TIMG_Tx_INCREASE` field. The time-base counter can be enabled or disabled by setting or clearing the `TIMG_Tx_EN` field, respectively. When enabled, the time-base counter increments or decrements on each cycle of `TB_CLK`. When disabled, the time-base counter is essentially frozen. Note that the `TIMG_Tx_INCREASE` field can be changed no matter whether `TIMG_Tx_EN` is set or not, and this will cause the time-base counter to change direction instantly.

To read the 54-bit value of the time-base counter, the timer value must be latched to two registers before being read by the CPU (due to the CPU being 32-bit). By writing any value to the `TIMG_TxUPDATE_REG`, the current value of the 54-bit timer starts to be latched into the `TIMG_TxLO_REG` and `TIMG_TxHI_REG` registers containing the lower 32-bits and higher 22-bits, respectively. When `TIMG_TxUPDATE_REG` is cleared by hardware, it indicates the latch operation has been completed and current timer value can be read from the `TIMG_TxLO_REG` and `TIMG_TxHI_REG` registers. `TIMG_TxLO_REG` and `TIMG_TxHI_REG` registers will remain unchanged for the CPU to read in its own time until `TIMG_TxUPDATE_REG` is written to again.

### 15.3.3 Alarm Generation

A timer can be configured to trigger an alarm when the timer's current value matches the alarm value. An alarm will cause an interrupt to occur and (optionally) an automatic reload of the timer's current value (see Section 15.3.4).

The 54-bit alarm value is configured using `TIMG_TxALARMLO_REG` and `TIMG_TxALARMHI_REG`, which represent the lower 32-bits and higher 22-bits of the alarm value, respectively. However, the configured alarm value is ineffective until the alarm is enabled by setting the `TIMG_Tx_ALARM_EN` field. To avoid alarm being enabled "too late" (i.e., the timer value has already passed the alarm value when the alarm is enabled), the hardware will trigger the alarm immediately if the current timer value is:

- higher than the alarm value (within a defined range) when the up-down counter increments
- lower than the alarm value (within a defined range) when the up-down counter decrements

Table 15.3-1 and Table 15.3-2 show the relationship between the current value of the timer, the alarm value, and when an alarm is triggered. The current time value and the alarm value are defined as follows:

- `TIMG_VALUE` = {`TIMG_TxHI_REG`, `TIMG_TxLO_REG`}
- `ALARM_VALUE` = {`TIMG_TxALARMHI_REG`, `TIMG_TxALARMLO_REG`}

Table 15.3-1. Alarm Generation When Up-Down Counter Increments

| Scenario | Range  | Alarm   |
|----------|--|---|
| 1        | $\text{ALARM\_VALUE} - \text{TIMG\_VALUE} > 2^{53}$        | Triggered   |
| 2        | $0 < \text{ALARM\_VALUE} - \text{TIMG\_VALUE} \leq 2^{53}$ | Triggered when the up-down counter counts TIMG_VALUE up to ALARM_VALUE  |
| 3        | $0 \leq \text{TIMG\_VALUE} - \text{ALARM\_VALUE} < 2^{53}$ | Triggered   |
| 4        | $\text{TIMG\_VALUE} - \text{ALARM\_VALUE} \geq 2^{53}$     | Triggered when the up-down counter restarts counting up from 0 after reaching the timer's maximum value and counts TIMG_VALUE up to ALARM_VALUE |

Table 15.3-2. Alarm Generation When Up-Down Counter Decrements

| Scenario | Range  | Alarm   |
|----------|--|---|
| 5        | $\text{TIMG\_VALUE} - \text{ALARM\_VALUE} > 2^{53}$        | Triggered   |
| 6        | $0 < \text{TIMG\_VALUE} - \text{ALARM\_VALUE} \leq 2^{53}$ | Triggered when the up-down counter counts TIMG_VALUE down to ALARM_VALUE  |
| 7        | $0 \leq \text{ALARM\_VALUE} - \text{TIMG\_VALUE} < 2^{53}$ | Triggered   |
| 8        | $\text{ALARM\_VALUE} - \text{TIMG\_VALUE} \geq 2^{53}$     | Triggered when the up-down counter restarts counting down from the timer's maximum value after reaching the minimum value and counts TIMG_VALUE down to ALARM_VALUE |

When an alarm occurs, the [TIMG\\_Tx\\_ALARM\\_EN](#) field is automatically cleared and no alarm will occur again until the [TIMG\\_Tx\\_ALARM\\_EN](#) is set next time.

### 15.3.4 Timer Reload

A timer is reloaded when a timer's current value is overwritten with a reload value stored in the [TIMG\\_Tx\\_LOAD\\_LO](#) and [TIMG\\_Tx\\_LOAD\\_HI](#) fields that correspond to the lower 32-bits and higher 22-bits of the timer's new value, respectively. However, writing a reload value to [TIMG\\_Tx\\_LOAD\\_LO](#) and [TIMG\\_Tx\\_LOAD\\_HI](#) will not cause the timer's current value to change. Instead, the reload value is ignored by the timer until a reload event occurs. A reload event can be triggered either by a software instant reload or an auto-reload at alarm.

A software instant reload is triggered by the CPU writing any value to [TIMG\\_TxLOAD\\_REG](#), which causes the timer's current value to be instantly reloaded. If [TIMG\\_Tx\\_EN](#) is set, the timer will continue incrementing or decrementing from the new value. In this case if [TIMG\\_Tx\\_ALARM\\_EN](#) is set, the timer will still trigger alarms in scenarios listed in Table 15.3-1 and 15.3-2. If [TIMG\\_Tx\\_EN](#) is cleared, the timer will remain frozen at the new value until counting is re-enabled.

An auto-reload at alarm will cause a timer reload when an alarm occurs, thus allowing the timer to continue incrementing or decrementing from the reload value. This is generally useful for resetting the timer's value when using periodic alarms. To enable auto-reload at alarm, the [TIMG\\_Tx\\_AUTORELOAD](#) field should be set. If not enabled, the timer's value will continue to increment or decrement past the alarm value after an alarm.

### 15.3.5 Event Task Matrix Feature

The TIMG<sub>n</sub> on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows TIMG<sub>n</sub>'s ETM tasks to be triggered by any peripherals' ETM events, or TIMG<sub>n</sub>'s ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to TIMG<sub>n</sub>. For more information, please refer to [Chapter 12 Event Task Matrix \(ETM\)](#).

TIMG<sub>n</sub> can receive the following ETM tasks:

- TGO\_TASK\_CNT\_START\_TIMER0: When triggered, it will enable the time-base counter.
- TG1\_TASK\_CNT\_START\_TIMER0: When triggered, it will enable the time-base counter.
- TGO\_TASK\_CNT\_STOP\_TIMER0: When triggered, it will disable the time-base counter.
- TG1\_TASK\_CNT\_STOP\_TIMER0: When triggered, it will disable the time-base counter.

**Note:**

The above two ETM tasks have the same function as the APB configuration [TIMG\\_TO\\_EN](#). When these operations occur at the same time, the priority of each operation from high to low is as follows:

1. TGO\_TASK\_CNT\_START\_TIMER0 and TG1\_TASK\_CNT\_START\_TIMER0: When triggered, it will enable the time-base counter;
2. TGO\_TASK\_CNT\_STOP\_TIMER0 and TG1\_TASK\_CNT\_STOP\_TIMER0: When triggered, it will disable the time-base counter;
3. APB configuration [TIMG\\_TO\\_EN](#): Enable or disable the time-base counter.

- TGO\_TASK\_ALARM\_START\_TIMER0: When triggered, it will enable the alarm generation.
- TG1\_TASK\_ALARM\_START\_TIMER0: When triggered, it will enable the alarm generation.

**Note:**

Alarm generation can also be enabled through APB method configuring [TIMG\\_TO\\_ALARM\\_EN](#) and hardware events. When these operations occur at the same time, the priority of each operation from high to low is as follows:

1. TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0: When triggered, it will enable the alarm generation;
2. Alarm events: When triggered, it will disable the alarm generation;
3. APB configuration [TIMG\\_TO\\_ALARM\\_EN](#): Enable or disable the alarm generation.

- TGO\_TASK\_CNT\_CAP\_TIMER0: When triggered, it will update the current counter value to the [TIMG\\_TOLO\\_REG](#) and [TIMG\\_TOHI\\_REG](#) registers.
- TG1\_TASK\_CNT\_CAP\_TIMER0: When triggered, it will update the current counter value to the [TIMG\\_TOLO\\_REG](#) and [TIMG\\_TOHI\\_REG](#) registers.
- TGO\_TASK\_CNT\_RELOAD\_TIMER0: When triggered, it will overwrite the current counter value with the reload value stored in [TIMG\\_TO\\_LOAD\\_LO](#) and [TIMG\\_TO\\_LOAD\\_HI](#).
- TG1\_TASK\_CNT\_RELOAD\_TIMER0: When triggered, it will overwrite the current counter value with the

reload value stored in [TIMG\\_TO\\_LOAD\\_LO](#) and [TIMG\\_TO\\_LOAD\\_HI](#).

TIMG $n$  can generate the following ETM events:

- TGO\_EVT\_CNT\_CMP\_TIMER0: Indicates the interrupt event of T0 in TIMG0.
- TG1\_EVT\_CNT\_CMP\_TIMER0: Indicates the interrupt event of T0 in TIMG1.

**Note:**

All the ETM tasks and events of TIMG $n$  will not take effect until the [TIMG \$n\$ \\_ETM\\_EN](#) is set to 1.

In practical applications, timer groups' ETM events can trigger their own ETM tasks.

For example, TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0 can be triggered respectively by TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0 to realize periodic alarm. For configuration steps, please refer to [15.4.4 Timer as Periodic Alarm by ETM](#).

### 15.3.6 RTC\_SLOW\_CLK Frequency Calculation

Using XTAL\_CLK as a reference, it is possible to calculate the frequency of clock sources for RTC\_SLOW\_CLK (i.e., RC\_SLOW\_CLK, RC\_FAST\_DIV\_CLK, and XTAL32K\_CLK) as follows:

1. Start periodic or one-shot frequency calculation (see Section [15.4.5](#) for details);
2. Once receiving the signal to start calculation, the counter of XTAL\_CLK and the counter of RTC\_SLOW\_CLK begin to work at the same time. When the counter of RTC\_SLOW\_CLK counts to CO, the two counters stop counting simultaneously;
3. Assume the value of XTAL\_CLK's counter is C1, and the frequency of RTC\_SLOW\_CLK would be calculated as:  $f_{rtc} = \frac{C0 \times f_{XTAL\_CLK}}{C1}$

### 15.3.7 Interrupts

ESP32-P4's TIMG $n$  can generate the following interrupt signal(s) that will be sent to the [Interrupt Matrix](#).

- TG $n$ \_Tx\_INT
- TG $n$ \_WDT\_INT

There are several internal interrupt sources from TIMG $n$  that can generate the above interrupt signal(s). The interrupt sources from TIMG $n$  are listed with their trigger conditions and the resulted interrupt signal(s) in Table [15.3-3](#).

**Table 15.3-3. TIMG $n$ 's Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition        | Interrupt Signal   |
|---------------------------|--------------------------|--------------------|
| TIMG_T $x$ _INT           | Alarm generated by T $x$ | TG $n$ _T $x$ _INT |
| TIMG_WDT_INT              | Alarm generated by WDT   | TG $n$ _WDT_INT    |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [15.5 Register Summary](#).

## 15.4 Configuration and Usage

### 15.4.1 Timer as a Simple Clock

1. Configure the time-base counter
  - Select clock source by configuring the HP\_SYS\_CLKRST\_TIMERGRPO\_TGRT\_CLK\_SRC\_SEL field of the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL21\_REG register.
  - Configure the 16-bit prescaler by setting [TIMG\\_Tx\\_DIVIDER](#).
  - Configure the timer direction by setting or clearing [TIMG\\_Tx\\_INCREASE](#).
  - Set the timer's starting value by writing the starting value to [TIMG\\_Tx\\_LOAD\\_LO](#) and [TIMG\\_Tx\\_LOAD\\_HI](#), then reloading it into the timer by writing any value to [TIMG\\_TxLOAD\\_REG](#).
2. Start the timer by setting [TIMG\\_Tx\\_EN](#).
3. Get the timer's current value.
  - Write any value to [TIMG\\_TxUPDATE\\_REG](#) to latch the timer's current value.
  - Wait until [TIMG\\_TxUPDATE\\_REG](#) is cleared by hardware.
  - Read the latched timer value from [TIMG\\_TxLO\\_REG](#) and [TIMG\\_TxHI\\_REG](#).

### 15.4.2 Timer as One-shot Alarm

1. Configure the time-base counter following step 1 of Section [15.4.1](#).
2. Configure the alarm.
  - Configure the alarm value by setting [TIMG\\_TxALARMLO\\_REG](#) and [TIMG\\_TxALARMHI\\_REG](#).
  - Enable interrupt by setting [TIMG\\_Tx\\_INT\\_ENA](#).
3. Disable auto reload by clearing [TIMG\\_Tx\\_AUTORELOAD](#).
4. Start the alarm by setting [TIMG\\_Tx\\_ALARM\\_EN](#).
5. Handle the alarm interrupt.
  - Clear the interrupt by setting the timer's corresponding bit in [TIMG\\_Tx\\_INT\\_CLR](#).
  - Disable the timer by clearing [TIMG\\_Tx\\_EN](#).

### 15.4.3 Timer as Periodic Alarm by APB

1. Configure the time-base counter following step 1 in Section [15.4.1](#).
2. Configure the alarm following step 2 in Section [15.4.2](#).
3. Enable auto reload by setting [TIMG\\_Tx\\_AUTORELOAD](#) and configure the reload value via [TIMG\\_Tx\\_LOAD\\_LO](#) and [TIMG\\_Tx\\_LOAD\\_HI](#).



4. Start the alarm by setting [TIMG\\_Tx\\_ALARM\\_EN](#).
5. Handle the alarm interrupt (repeat on each alarm iteration).
  - Clear the interrupt by setting the timer's corresponding bit in [TIMG\\_Tx\\_INT\\_CLR](#).
  - If the next alarm requires a new alarm value and reload value (i.e., different alarm interval per iteration), then [TIMG\\_TxALARMLO\\_REG](#), [TIMG\\_TxALARMHI\\_REG](#), [TIMG\\_Tx\\_LOAD\\_LO](#), and [TIMG\\_Tx\\_LOAD\\_HI](#) should be reconfigured as needed. Otherwise, the aforementioned registers should remain unchanged.
  - Re-enable the alarm by setting [TIMG\\_Tx\\_ALARM\\_EN](#).
6. Stop the timer (on final alarm iteration).
  - Clear the interrupt by setting the timer's corresponding bit in [TIMG\\_Tx\\_INT\\_CLR](#).
  - Disable the timer by clearing [TIMG\\_Tx\\_EN](#).

#### 15.4.4 Timer as Periodic Alarm by ETM

1. Enable the ETM module's clock
2. Map ETM event to ETM task (which means using the event to trigger the task)
  - If [TIMG\\_TO\\_AUTORELOAD](#) is set to 1, map TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0 to the TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0 respectively by one ETM channel.
  - If [TIMG\\_TO\\_AUTORELOAD](#) is set to 0, in addition to mapping TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0 to the TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0, the TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0 should also be mapped to TGO\_TASK\_CNT\_RELOAD\_TIMER0 and TG1\_TASK\_CNT\_RELOAD\_TIMER0 by another ETM channel.
3. Choose to enable the one or two ETM channels.
4. Set [TIMER\\_ETM\\_EN](#) to 1 to enable timer group's ETM events and tasks.
5. Configure the time-base counter following step 1 in Section [15.4.1](#).
6. Configure the alarm following step 2 in Section [15.4.2](#).
7. Configure the reload value via [TIMG\\_TO\\_LOAD\\_LO](#) and [TIMG\\_TO\\_LOAD\\_HI](#).
8. Handle the TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0.
  - When alarm generates, the TGO\_EVT\_CNT\_CMP\_TIMER0 and TG1\_EVT\_CNT\_CMP\_TIMER0 also generate, and the alarm generation will be disabled by the alarm.
  - If [TIMG\\_TO\\_AUTORELOAD](#) is 1, the current counter value is overwritten by the reloaded value. The alarm generation will be reopened by TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0.
  - If [TIMG\\_TO\\_AUTORELOAD](#) is 0, the current counter value is overwritten by the reloaded value because of the TGO\_TASK\_CNT\_RELOAD\_TIMER0 and TG1\_TASK\_CNT\_RELOAD\_TIMER0. The alarm generation will be reopened by TGO\_TASK\_ALARM\_START\_TIMER0 and TG1\_TASK\_ALARM\_START\_TIMER0.

9. Stop the timer (on final alarm iteration).

- Disable the ETM channels used to map timer group's event and task
- Set `TIMER_ETM_EN` to 0.
- Clear the interrupt by setting the timer's corresponding bit in `TIMG_TO_INT_CLR`.
- Disable the timer by clearing `TIMG_TO_EN`.

### 15.4.5 RTC\_SLOW\_CLK Frequency Calculation

1. One-shot frequency calculation

- Configure `HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_EN` to enable clock gate of `TIMG0_CALI_CLK`.
- Configure `HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_SRC_SEL` to select one clock as the clock source of `TIMG0_CALI_CLK`.
- Configure `HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_DIV_NUM` to output `TIMG0_CALI_CLK` after integer prescaler.
- Configure the time of calculation via `TIMG_RTC_CALI_MAX`.
- Select one-shot frequency calculation by clearing `TIMG_RTC_CALI_START_CYCLING`, and enable the two counters via `TIMG_RTC_CALI_START`.
- Once `TIMG_RTC_CALI_RDY` becomes 1, read `TIMG_RTC_CALI_VALUE` to get the value of `XTAL_CLK`'s counter, and calculate the frequency of `RTC_SLOW_CLK` according to the formula in Section 15.3.6.

2. Periodic frequency calculation

- Select the clock whose frequency is to be calculated (clock source of `RTC_SLOW_CLK`) via `HP_SYS_CLKRST_TIMERGRPO_TGRT_CLK_SRC_SEL`, and configure the time of calculation via `TIMG_RTC_CALI_MAX`.
- Select periodic frequency calculation by enabling `TIMG_RTC_CALI_START_CYCLING`.
- When `TIMG_RTC_CALI_CYCLING_DATA_VLD` is 1, `TIMG_RTC_CALI_VALUE` is valid.

3. Timeout

If the counter of `RTC_SLOW_CLK` cannot finish counting in `TIMG_RTC_CALI_TIMEOUT_RST_CNT` cycles, `TIMG_RTC_CALI_TIMEOUT` will be set to indicate a timeout.

## 15.5 Register Summary

The addresses in this section are relative to Timer Group base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>T0 Control and configuration registers</b>       |   |         |        |
| <a href="#">TIMG_TOCONFIG_REG</a>                   | Timer 0 configuration register  | 0x0000  | varies |
| <a href="#">TIMG_TOLO_REG</a>                       | Timer 0 current value, low 32 bits  | 0x0004  | RO     |
| <a href="#">TIMG_TOHI_REG</a>                       | Timer 0 current value, high 22 bits   | 0x0008  | RO     |
| <a href="#">TIMG_TOUUPDATE_REG</a>                  | Write to copy current timer value to <a href="#">TIMG_TOLO_REG</a> or <a href="#">TIMG_TOHI_REG</a> | 0x000C  | R/W/SC |
| <a href="#">TIMG_TOALARMLO_REG</a>                  | Timer 0 alarm value, low 32 bits  | 0x0010  | R/W    |
| <a href="#">TIMG_TOALARMHI_REG</a>                  | Timer 0 alarm value, high 22 bits   | 0x0014  | R/W    |
| <a href="#">TIMG_TOLOADLO_REG</a>                   | Timer 0 reload value, low 32 bits   | 0x0018  | R/W    |
| <a href="#">TIMG_TOLOADHI_REG</a>                   | Timer 0 reload value, high 22 bits  | 0x001C  | R/W    |
| <a href="#">TIMG_TOLOAD_REG</a>                     | Write to reload timer from <a href="#">TIMG_TOLOADLO_REG</a> or <a href="#">TIMG_TOLOADHI_REG</a>   | 0x0020  | WT     |
| <b>T1 Control and configuration registers</b>       |   |         |        |
| <a href="#">TIMG_T1CONFIG_REG</a>                   | Timer 1 configuration register  | 0x0024  | varies |
| <a href="#">TIMG_T1LO_REG</a>                       | Timer 1 current value, low 32 bits  | 0x0028  | RO     |
| <a href="#">TIMG_T1HI_REG</a>                       | Timer 1 current value, high 22 bits   | 0x002C  | RO     |
| <a href="#">TIMG_T1UPDATE_REG</a>                   | Write to copy current timer value to <a href="#">TIMG_T1LO_REG</a> or <a href="#">TIMG_T1HI_REG</a> | 0x0030  | R/W/SC |
| <a href="#">TIMG_T1ALARMLO_REG</a>                  | Timer 1 alarm value, low 32 bits  | 0x0034  | R/W    |
| <a href="#">TIMG_T1ALARMHI_REG</a>                  | Timer 1 alarm value, high 22 bits   | 0x0038  | R/W    |
| <a href="#">TIMG_T1LOADLO_REG</a>                   | Timer 1 reload value, low 32 bits   | 0x003C  | R/W    |
| <a href="#">TIMG_T1LOADHI_REG</a>                   | Timer 1 reload value, high 22 bits  | 0x0040  | R/W    |
| <a href="#">TIMG_T1LOAD_REG</a>                     | Write to reload timer from <a href="#">TIMG_T1LOADLO_REG</a> or <a href="#">TIMG_T1LOADHI_REG</a>   | 0x0044  | WT     |
| <b>WDT Control and configuration registers</b>      |   |         |        |
| <a href="#">TIMG_WDTCONFIG0_REG</a>                 | Watchdog timer configuration register   | 0x0048  | varies |
| <a href="#">TIMG_WDTCONFIG1_REG</a>                 | Watchdog timer prescaler register   | 0x004C  | varies |
| <a href="#">TIMG_WDTCONFIG2_REG</a>                 | Watchdog timer stage 0 timeout value  | 0x0050  | R/W    |
| <a href="#">TIMG_WDTCONFIG3_REG</a>                 | Watchdog timer stage 1 timeout value  | 0x0054  | R/W    |
| <a href="#">TIMG_WDTCONFIG4_REG</a>                 | Watchdog timer stage 2 timeout value  | 0x0058  | R/W    |
| <a href="#">TIMG_WDTCONFIG5_REG</a>                 | Watchdog timer stage 3 timeout value  | 0x005C  | R/W    |
| <a href="#">TIMG_WDTFEED_REG</a>                    | Write to feed the watchdog timer  | 0x0060  | WT     |
| <a href="#">TIMG_WDTWPROTECT_REG</a>                | Watchdog write protect register   | 0x0064  | R/W    |
| <b>RTC CALI Control and configuration registers</b> |   |         |        |
| <a href="#">TIMG_RTCCALICFG_REG</a>                 | RTC calibration configure register  | 0x0068  | varies |
| <a href="#">TIMG_RTCCALICFG1_REG</a>                | RTC calibration configure register 1  | 0x006C  | RO     |
| <a href="#">TIMG_RTCCALICFG2_REG</a>                | RTC calibration configure register 2  | 0x0080  | varies |

| Name                                    | Description                     | Address | Access   |
|---|---------------------------------|---------|----------|
| <b>Interrupt registers</b>              |                                 |         |          |
| <a href="#">TIMG_INT_ENA_TIMERS_REG</a> | Interrupt enable bits           | 0x0070  | R/W      |
| <a href="#">TIMG_INT_RAW_TIMERS_REG</a> | Raw interrupt status            | 0x0074  | R/SS/WTC |
| <a href="#">TIMG_INT_ST_TIMERS_REG</a>  | Masked interrupt status         | 0x0078  | RO       |
| <a href="#">TIMG_INT_CLR_TIMERS_REG</a> | Interrupt clear bits            | 0x007C  | WT       |
| <b>Version register</b>                 |                                 |         |          |
| <a href="#">TIMG_NTIMERS_DATE_REG</a>   | Timer version control register  | 0x00F8  | R/W      |
| <b>Clock configuration registers</b>    |                                 |         |          |
| <a href="#">TIMG_REGCLK_REG</a>         | Timer group clock gate register | 0x00FC  | R/W      |

## 15.6 Registers

The addresses in this section are relative to Timer Group base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 15.1. TIMG\_T<sub>x</sub>CONFIG\_REG (x: 0-1) (0x0000+0x24\*x)**

|   |    |    |    |                              |  |  |  |  |  |  |  |  |    |    |   |            |   |   |   |
|---|----|----|----|------------------------------|--|--|--|--|--|--|--|--|----|----|---|------------|---|---|---|
| TIMG_T <sub>x</sub> _EN<br>TIMG_T <sub>x</sub> _INCREASE<br>TIMG_T <sub>x</sub> _AUTORELOAD |    |    |    | TIMG_T <sub>x</sub> _DIVIDER |  |  |  |  |  |  |  | TIMG_T <sub>x</sub> _DIVCNT_RST<br>(reserved)<br>TIMG_T <sub>x</sub> _ALARM_EN |    |    |   | (reserved) |   |   |   |
| 31  | 30 | 29 | 28 | 13                           |  |  |  |  |  |  |  | 12   | 11 | 10 | 9 | 0          |   |   |   |
| 0   | 1  | 1  |    | 0x01                         |  |  |  |  |  |  |  | 0  | 0  | 0  | 0 | 0          | 0 | 0 | 0 |

Reset

**TIMG\_T<sub>x</sub>\_ALARM\_EN** Configures whether to enable Timer T<sub>x</sub> alarm function. This bit will be automatically cleared once an alarm occurs.

0: Disable

1: Enable

(R/W/SC)

**TIMG\_T<sub>x</sub>\_DIVCNT\_RST** Configures to reset Timer T<sub>x</sub>'s clock divider counter.

0: No effect

1: Reset

(WT)

**TIMG\_T<sub>x</sub>\_DIVIDER** Represents Timer x clock (T<sub>x</sub>\_clk) prescaler value. (R/W)

**TIMG\_T<sub>x</sub>\_AUTORELOAD** Configures to enable Timer T<sub>x</sub> auto-reload function at the time of alarm.

0: No effect

1: Enable

(R/W)

**TIMG\_T<sub>x</sub>\_INCREASE** Configures the counting direction of Timer T<sub>x</sub> time-base counter.

0: Decrement

1: Increment

(R/W)

**TIMG\_T<sub>x</sub>\_EN** Configures whether to enable Timer T<sub>x</sub> time-base counter.

0: Disable

1: Enable

(R/W/SS/SC)

**Register 15.2. TIMG\_T<sub>x</sub>LO\_REG (x: 0-1) (0x0004+0x24\*x)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| TIMG_Tx_LO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**TIMG\_T<sub>x</sub>LO** Represents the low 32 bits of the time-base counter of Timer T<sub>x</sub>. Valid only after writing to **TIMG\_T<sub>x</sub>UPDATE\_REG**.  
 Measurement unit: T<sub>x</sub>\_clk.  
 (RO)

**Register 15.3. TIMG\_T<sub>x</sub>HI\_REG (x: 0-1) (0x0008+0x24\*x)**

|                     |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |   |
|---------------------|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|---|
| (reserved)          |  |  |  |  |  |  |  |  |  |  | TIMG_TO_HI |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |   |
| 31                  |  |  |  |  |  |  |  |  |  |  | 22         |  |  |  |  |  |  |  |  |  |  | 21 |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  | 0 |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  | 0x0000     |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |   |

**TIMG\_T<sub>x</sub>HI** Represents the high 22 bits of the time-base counter of Timer T<sub>x</sub>. Valid only after writing to **TIMG\_T<sub>x</sub>UPDATE\_REG**.  
 Measurement unit: T<sub>x</sub>\_clk.  
 (RO)

**Register 15.4. TIMG\_T<sub>x</sub>UPDATE\_REG (x: 0-1) (0x000C+0x24\*x)**

|                            |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|----------------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TIMG_T <sub>x</sub> UPDATE |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                         | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset                      |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**TIMG\_T<sub>x</sub>UPDATE** Configures to latch the counter value.  
 0: Latch  
 1: Latch  
 (R/W/SC)

**Register 15.5. TIMG\_T<sub>x</sub>ALARMLO\_REG (x: 0-1) (0x0010+0x24\*x)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| TIMG_T <sub>x</sub> _ALARM_LO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**TIMG\_T<sub>x</sub>\_ALARM\_LO** Configures the low 32 bits of Timer T<sub>x</sub> alarm trigger time-base counter value.

Valid only when **TIMG\_T<sub>x</sub>\_ALARM\_EN** is 1.

Measurement unit: T<sub>x</sub>\_clk.

(R/W)

**Register 15.6. TIMG\_T<sub>x</sub>ALARMHI\_REG (x: 0-1) (0x0014+0x24\*x)**

|                         |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |
|-------------------------|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved)              |  |  |  |  |  |  |  |  |  |  |  | TIMG_T <sub>x</sub> _ALARM_HI |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                      |  |  |  |  |  |  |  |  |  |  |  | 22                            |  |  |  |  |  |  |  |  |  |  |  | 21 |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  | 0x0000                        |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |   |

**TIMG\_T<sub>x</sub>\_ALARM\_HI** Configures the high 22 bits of Timer T<sub>x</sub> alarm trigger time-base counter value.

Valid only when **TIMG\_T<sub>x</sub>\_ALARM\_EN** is 1.

Measurement unit: T<sub>x</sub>\_clk.

(R/W)

**Register 15.7. TIMG\_T<sub>x</sub>LOADLO\_REG (x: 0-1) (0x0018+0x24\*x)**

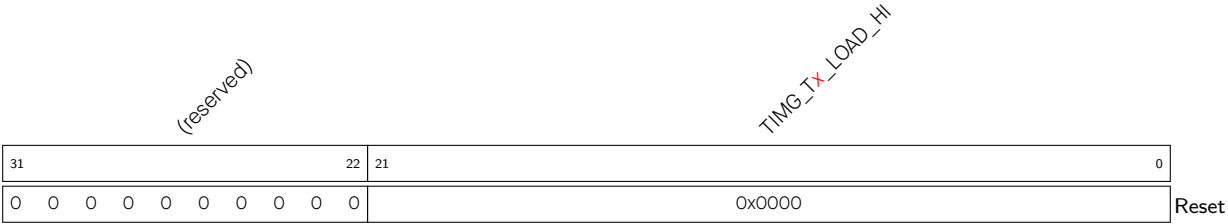
|                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| TIMG_T <sub>x</sub> _LOAD_LO |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**TIMG\_T<sub>x</sub>\_LOAD\_LO** Configures low 32 bits of the value that a reload will load onto Timer T<sub>x</sub> time-base counter.

Measurement unit: T<sub>x</sub>\_clk.

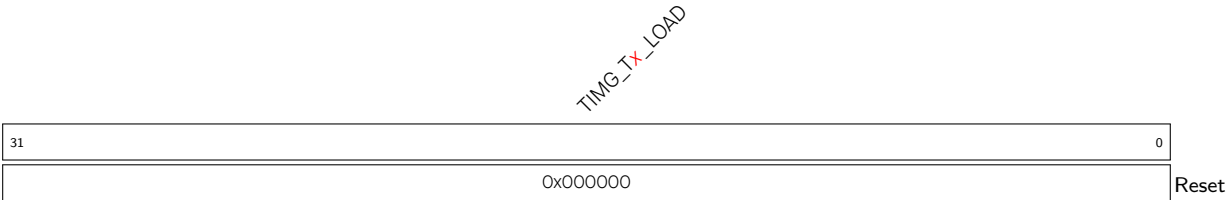
(R/W)

Register 15.8. TIMG\_TxLOADHI\_REG (x: 0-1) (0x001C+0x24\*x)



**TIMG\_Tx\_LOAD\_HI** Configures high 22 bits of the value that a reload will load onto Timer Tx time-base counter.  
Measurement unit: Tx\_clk.  
(R/W)

Register 15.9. TIMG\_TxLOAD\_REG (x: 0-1) (0x0020+0x24\*x)



**TIMG\_Tx\_LOAD** Write any value to trigger Timer Tx time-base counter reload. (WT)



Register 15.10. TIMG\_WDTCONFIG0\_REG (0x0048)

|             |    |               |    |               |    |               |    |               |    |                         |    |                           |     |                           |    |                           |    |                          |   |                          |   |            |   |   |   |   |   |   |   |   |   |       |
|-------------|----|---------------|----|---------------|----|---------------|----|---------------|----|-------------------------|----|---------------------------|-----|---------------------------|----|---------------------------|----|--------------------------|---|--------------------------|---|------------|---|---|---|---|---|---|---|---|---|-------|
| TIMG_WDT_EN |    | TIMG_WDT_STG0 |    | TIMG_WDT_STG1 |    | TIMG_WDT_STG2 |    | TIMG_WDT_STG3 |    | TIMG_WDT_CONF_UPDATE_EN |    | TIMG_WDT_CPU_RESET_LENGTH |     | TIMG_WDT_SYS_RESET_LENGTH |    | TIMG_WDT_FLASHBOOT_MOD_EN |    | TIMG_WDT_PROCPU_RESET_EN |   | TIMG_WDT_APPCPU_RESET_EN |   | (reserved) |   |   |   |   |   |   |   |   |   |       |
| 31          | 30 | 29            | 28 | 27            | 26 | 25            | 24 | 23            | 22 | 21                      | 20 | 18                        | 17  | 15                        | 14 | 13                        | 12 | 11                       |   |                          |   |            |   |   |   |   |   |   |   |   |   | 0     |
| 0           | 0  | 0             | 0  | 0             | 0  | 0             | 0  | 0             | 0  | 0                       | 0  | 0x1                       | 0x1 | 1                         | 0  | 0                         | 0  | 0                        | 0 | 0                        | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**TIMG\_WDT\_APPCPU\_RESET\_EN** Configures whether to mask the APP CPU reset generated by MWDT. Valid only when write protection is disabled.

0: Mask

1: Unmask

(R/W)

**TIMG\_WDT\_PROCPU\_RESET\_EN** Configures whether to mask the PRO CPU reset generated by MWDT. Valid only when write protection is disabled.

0: Mask

1: Unmask

(R/W)

**TIMG\_WDT\_FLASHBOOT\_MOD\_EN** Configures whether to enable flash boot protection.

0: Disable

1: Enable

(R/W)

**TIMG\_WDT\_SYS\_RESET\_LENGTH** Configures the system reset signal length. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

0: 100 ns

4: 500 ns

1: 200 ns

5: 800 ns

2: 300 ns

6: 1.6  $\mu$ s

3: 400 ns

7: 3.2  $\mu$ s

(R/W)

Continued on the next page...

**Register 15.10. TIMG\_WDTCONFIG0\_REG (0x0048)**

Continued from the previous page...

**TIMG\_WDT\_CPU\_RESET\_LENGTH** Configures the CPU reset signal length. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

|           |                |
|-----------|----------------|
| 0: 100 ns | 4: 500 ns      |
| 1: 200 ns | 5: 800 ns      |
| 2: 300 ns | 6: 1.6 $\mu$ s |
| 3: 400 ns | 7: 3.2 $\mu$ s |

(R/W)

**TIMG\_WDT\_CONF\_UPDATE\_EN** Configures to update the WDT configuration registers.

0: No effect

1: Update

(WT)

**TIMG\_WDT\_STG3** Configures the timeout action of stage 3. Valid only when write protection is disabled.

0: No effect

1: Interrupt

2: Reset CPU

3: Reset system

(R/W)

**TIMG\_WDT\_STG2** Configures the timeout action of stage 2. Valid only when write protection is disabled.

0: No effect

1: Interrupt

2: Reset CPU

3: Reset system

(R/W)

**TIMG\_WDT\_STG1** Configures the timeout action of stage 1. Valid only when write protection is disabled.

0: No effect

1: Interrupt

2: Reset CPU

3: Reset system

(R/W)

Continued on the next page...

**Register 15.10. TIMG\_WDTCONFIGO\_REG (0x0048)**

Continued from the previous page...

**TIMG\_WDT\_STGO** Configures the timeout action of stage 0. Valid only when write protection is disabled.

0: No effect

1: Interrupt

2: Reset CPU

3: Reset system

(R/W)

**TIMG\_WDT\_EN** Configures whether or not to enable the MWDT. Valid only when write protection is disabled.

0: Disable

1: Enable

(R/W)

### Register 15.11. TIMG\_WDTCONFIG1\_REG (0x004C)

[illegible]

**TIMG\_WDT\_DIVCNT\_RST** Configures whether to reset WDT's clock divider counter.

0: No effect

1: Reset

(WT)

**TIMG\_WDT\_CLK\_PRESCALE** Configures MWDAT clock prescaler value. Valid only when write protection is disabled.

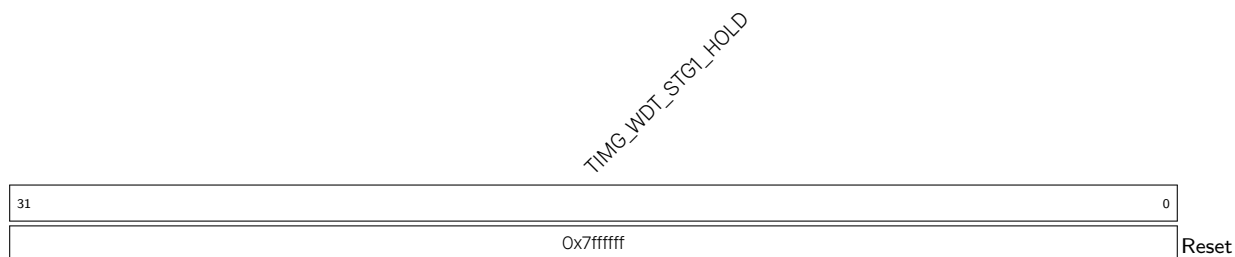
MWDT clock period = 12.5 ns \*TIMG\_WDT\_CLK\_PRESCALE. (R/W)

### Register 15.12. TIMG\_WDTCONFIG2\_REG (0x0050)

**TIMG\_WDT\_STGO\_HOLD** Configures the stage 0 timeout value. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

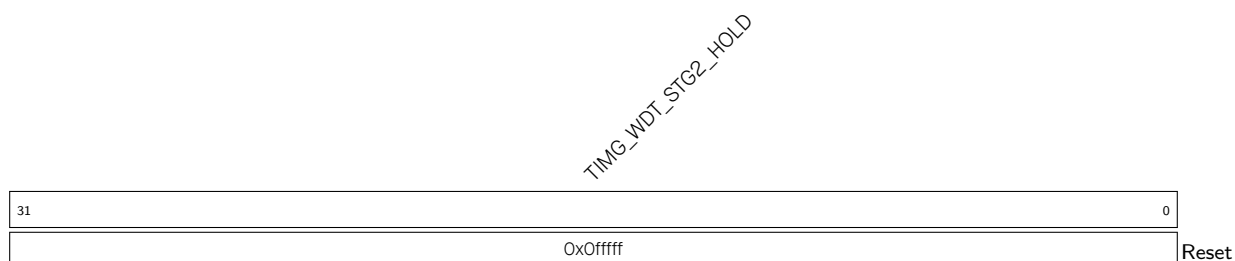
(R/W)

**Register 15.13. TIMG\_WDTCONFIG3\_REG (0x0054)**

**TIMG\_WDT\_STG1\_HOLD** Configures the stage 1 timeout value. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

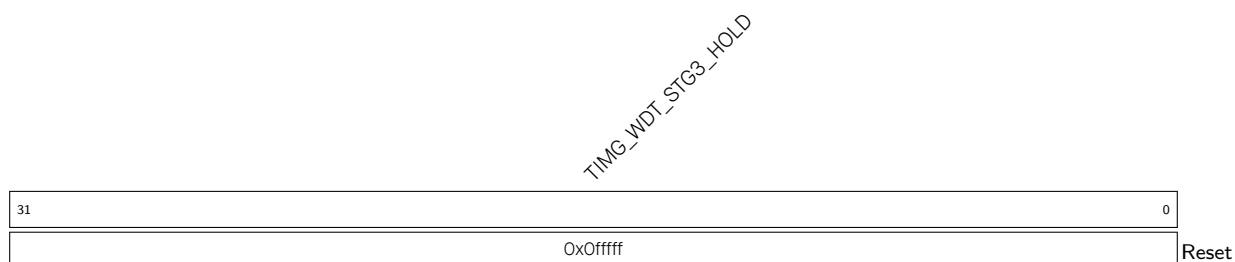
(R/W)

**Register 15.14. TIMG\_WDTCONFIG4\_REG (0x0058)**

**TIMG\_WDT\_STG2\_HOLD** Configures the stage 2 timeout value. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

(R/W)

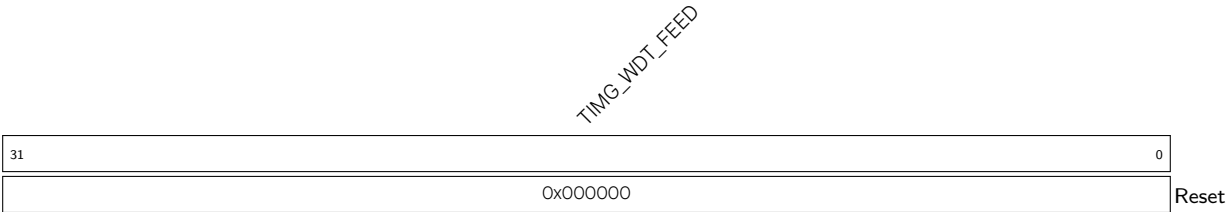
**Register 15.15. TIMG\_WDTCONFIG5\_REG (0x005C)**

**TIMG\_WDT\_STG3\_HOLD** Configures the stage 3 timeout value. Valid only when write protection is disabled.

Measurement unit: mwdt\_clk.

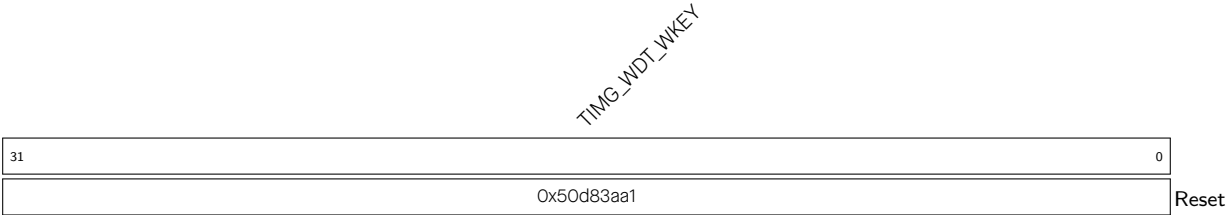
(R/W)

Register 15.16. TIMG\_WDTFEED\_REG (0x0060)



**TIMG\_WDT\_FEED** Write any value to feed the MWDT. Valid only when write protection is disabled. (WT)

Register 15.17. TIMG\_WDTWPROTECT\_REG (0x0064)



**TIMG\_WDT\_WKEY** Configures a different value than its reset value to enable write protection. (R/W)

Register 15.18. TIMG\_RTCCALICFG\_REG (0x0068)

|                     |      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|-------|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| TIMG_RTC_CALI_START |      |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TIMG_RTC_CALI_MAX |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | TIMG_RTC_CALI_RDY<br>(reserved) |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  | TIMG_RTC_CALI_START_CYCLING<br>(reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                  | 30   |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                | 15 | 14 | 13 | 12 | 11 |   |   |   |   |   |   |   |   |   | 0 |                                 |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                   | 0x01 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                 | 0  | 0  | 1  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**TIMG\_RTC\_CALI\_START\_CYCLING** Configures the frequency calculation mode.

- 0: One-shot frequency calculation
- 1: Periodic frequency calculation.

(R/W)

**TIMG\_RTC\_CALI\_RDY** Represents whether one-shot frequency calculation is done.

- 0: Not done
- 1: Done

(RO)

**TIMG\_RTC\_CALI\_MAX** Configures the time to calculate RTC slow clock’s frequency.

Measurement unit: XTAL\_CLK.

(R/W)

**TIMG\_RTC\_CALI\_START** Configures whether to enable one-shot frequency calculation.

- 0: Disable
- 1: Enable

(R/W)

Register 15.19. TIMG\_RTCCALICFG1\_REG (0x006C)

|                     |  |  |  |  |  |  |   |   |   |            |   |   |   |                                |  |  |  |
|---------------------|--|--|--|--|--|--|---|---|---|------------|---|---|---|--------------------------------|--|--|--|
| TIMG_RTC_CALI_VALUE |  |  |  |  |  |  |   |   |   | (reserved) |   |   |   | TIMG_RTC_CALI_CYCLING_DATA_VLD |  |  |  |
| 31                  |  |  |  |  |  |  | 7 | 6 | 1 |            |   |   | 0 |                                |  |  |  |
| 0x00000             |  |  |  |  |  |  | 0 | 0 | 0 | 0          | 0 | 0 | 0 | Reset                          |  |  |  |

**TIMG\_RTC\_CALI\_CYCLING\_DATA\_VLD** Represents whether periodic frequency calculation is done.

0: Not done

1: Done

(RO)

**TIMG\_RTC\_CALI\_VALUE** Represents the value countered by XTAL\_CLK when one-shot or periodic frequency calculation is done. It is used to calculate RTC slow clock's frequency. (RO)

Register 15.20. TIMG\_RTCCALICFG2\_REG (0x0080)

|                             |  |  |  |  |  |  |                               |   |   |   |            |       |                       |  |
|-----------------------------|--|--|--|--|--|--|-------------------------------|---|---|---|------------|-------|-----------------------|--|
| TIMG_RTC_CALI_TIMEOUT_THRES |  |  |  |  |  |  | TIMG_RTC_CALI_TIMEOUT_RST_CNT |   |   |   | (reserved) |       | TIMG_RTC_CALI_TIMEOUT |  |
| 31                          |  |  |  |  |  |  | 7                             | 6 | 3 | 2 | 1          | 0     |                       |  |
| 0x1ffffff                   |  |  |  |  |  |  | 3                             |   | 0 | 0 | 0          | Reset |                       |  |

**TIMG\_RTC\_CALI\_TIMEOUT** Represents whether RTC frequency calculation is timeout.

0: No timeout

1: Timeout

(RO)

**TIMG\_RTC\_CALI\_TIMEOUT\_RST\_CNT** Configures the cycles that reset frequency calculation timeout.

Measurement unit: XTAL\_CLK.

(R/W)

**TIMG\_RTC\_CALI\_TIMEOUT\_THRES** Configures the threshold value for the RTC frequency calculation timer. If the timer's value exceeds this threshold, a timeout is triggered.

Measurement unit: XTAL\_CLK.

(R/W)



Register 15.21. TIMG\_INT\_ENA\_TIMERS\_REG (0x0070)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TIMG_WDT_INT_ENA<br>TIMG_T1_INT_ENA<br>TIMG_TO_INT_ENA |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | Reset |

**TIMG\_T<sub>x</sub>\_INT\_ENA** (**x**: 0-1) Write 1 to enable the TIMG\_T<sub>x</sub>\_INT interrupt. (R/W)

**TIMG\_WDT\_INT\_ENA** Write 1 to enable the TIMG\_WDT\_INT interrupt. (R/W)

Register 15.22. TIMG\_INT\_RAW\_TIMERS\_REG (0x0074)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TIMG_WDT_INT_RAW<br>TIMG_T1_INT_RAW<br>TIMG_TO_INT_RAW |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | Reset |

**TIMG\_T<sub>x</sub>\_INT\_RAW** (**x**: 0-1) The raw interrupt status bit of the TIMG\_T<sub>x</sub>\_INT interrupt. (R/SS/WTC)

**TIMG\_WDT\_INT\_RAW** The raw interrupt status bit of the TIMG\_WDT\_INT interrupt. (R/SS/WTC)

Register 15.23. TIMG\_INT\_ST\_TIMERS\_REG (0x0078)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TIMG_WDT_INT_ST<br>TIMG_T1_INT_ST<br>TIMG_TO_INT_ST |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3   | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | Reset |

**TIMG\_T<sub>x</sub>\_INT\_ST** (**x**: 0-1) The masked interrupt status bit of the TIMG\_T<sub>x</sub>\_INT interrupt. (RO)

**TIMG\_WDT\_INT\_ST** The masked interrupt status bit of the TIMG\_WDT\_INT interrupt. (RO)

## Register 15.24. TIMG\_INT\_CLR\_TIMERS\_REG (0x007C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TIMG_WDT_INT_CLR<br>TIMG_T1_INT_CLR<br>TIMG_TO_INT_CLR |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | Reset |

**TIMG\_T<sub>x</sub>\_INT\_CLR** (**x**: 0-1) Write 1 to clear the TIMG\_T<sub>x</sub>\_INT interrupt. (WT)

**TIMG\_WDT\_INT\_CLR** Write 1 to clear the TIMG\_WDT\_INT interrupt. (WT)

## Register 15.25. TIMG\_NTIMERS\_DATE\_REG (0x00F8)

|            |  |    |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|------------|--|----|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved) |  |    |  | TIMG_NTIMGS_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31         |  | 28 |  | 27               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |
| 0 0 0 0    |  |    |  | 0x2209142        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TIMG\_NTIMGS\_DATE** Version control register (R/W)

## Register 15.26. TIMG\_REGCLK\_REG (0x00FC)

|             |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |   |   |       |
|-------------|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|---|---|-------|
| TIMG_CLK_EN |    |    |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TIMG_ETM_EN |   |   |       |
| 31          | 30 | 29 | 28 | 27         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |   |   | 0     |
| 0           | 0  | 0  | 1  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0           | 0 | 0 | Reset |

**TIMG\_ETM\_EN** Configures whether to enable timer's ETM task and event.

0: Disable

1: Enable

(R/W)

**TIMG\_CLK\_EN** Configures whether to enable gate clock signal for registers.

0: Force clock on for registers

1: Support clock only when registers are read or written to by software.

(R/W)

## Chapter 16

# Watchdog Timers (WDT)

## 16.1 Overview

Watchdog timers are hardware timers used to detect and recover from malfunctions. They must be periodically fed (reset) to prevent a timeout. A system/software that is behaving unexpectedly (e.g., is stuck in a software loop or in overdue events) will fail to feed the watchdog, thus the watchdog timer will time out and trigger an interrupt or reset, directing the system to a known state for exception handling or a restart. Therefore, watchdog timers are useful for detecting and handling erroneous system/software behavior.

As shown in Figure 16.1-1, ESP32-P4 contains three digital watchdog timers: one in each of the two timer groups in Chapter 15 *Timer Group (TIMG)* (called Main System Watchdog Timers, or MWDT) and one in the LP system (called the RTC Watchdog Timer, or RWDT). Each digital watchdog timer allows for four separately configurable stages, and each stage can be programmed to take one action upon timeout, unless the watchdog is fed or disabled. MWDT supports three timeout actions: interrupt, HP CPU reset, and HP core reset, while RWDT supports four timeout actions: interrupt, HP CPU reset, HP core reset, and system reset (see details in Section 16.2.2.2 *Stages and Timeout Actions*). A timeout value can be set for each stage individually.

In SPI Boot mode, RWDT and the MWDT in timer group 0 are enabled automatically in order to detect errors that may occur during the flash boot process and facilitate recovery.

ESP32-P4 also has one analog watchdog timer: Super watchdog (SWD). It is an ultra-low-power circuit in analog domain that helps to prevent the system from operating in a sub-optimal state and resets the system if required.

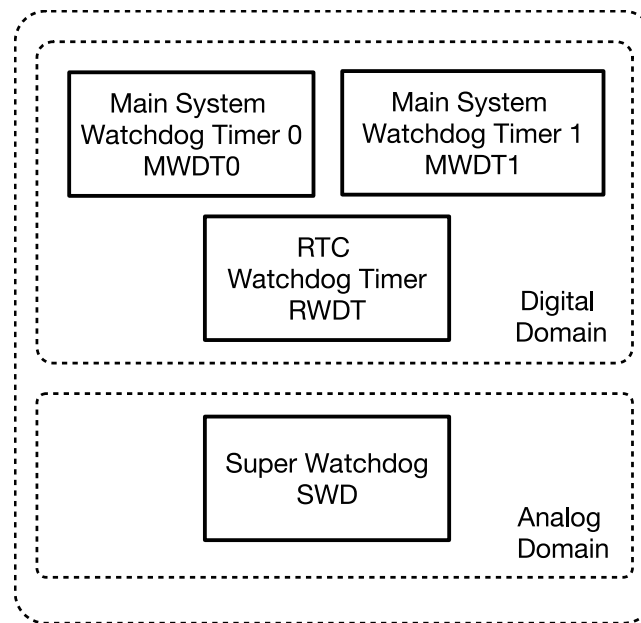


Figure 16.1-1. Watchdog Timers Overview

Note that while this chapter provides the functional descriptions of the watchdog timer's, MWDT register descriptions are detailed in Chapter 15 *Timer Group (TIMG)*, and the RWDT and SWD register descriptions are detailed in Section 16.5 *Register Summary*.

## 16.2 Digital Watchdog Timers

### 16.2.1 Features

Watchdog timers have the following features:

- Four stages, each with a separately programmable timeout value and timeout action
- Timeout actions:
  - MWDT: interrupt, HP CPU reset, HP core reset
  - RWDT: interrupt, HP CPU reset, HP core reset, system reset
- Flash boot protection under SPI Boot mode at stage 0:
  - MWDT0: HP core reset upon timeout
  - RWDT: system reset upon timeout
- Write protection that makes WDT register read only unless unlocked
- 32-bit timeout counter
- Clock source:
  - MWDT: PLL\_F80M\_CLK, RC\_FAST\_CLK or XTAL\_CLK
  - RWDT: LP\_DYN\_SLOW\_CLK

## 16.2.2 Functional Description

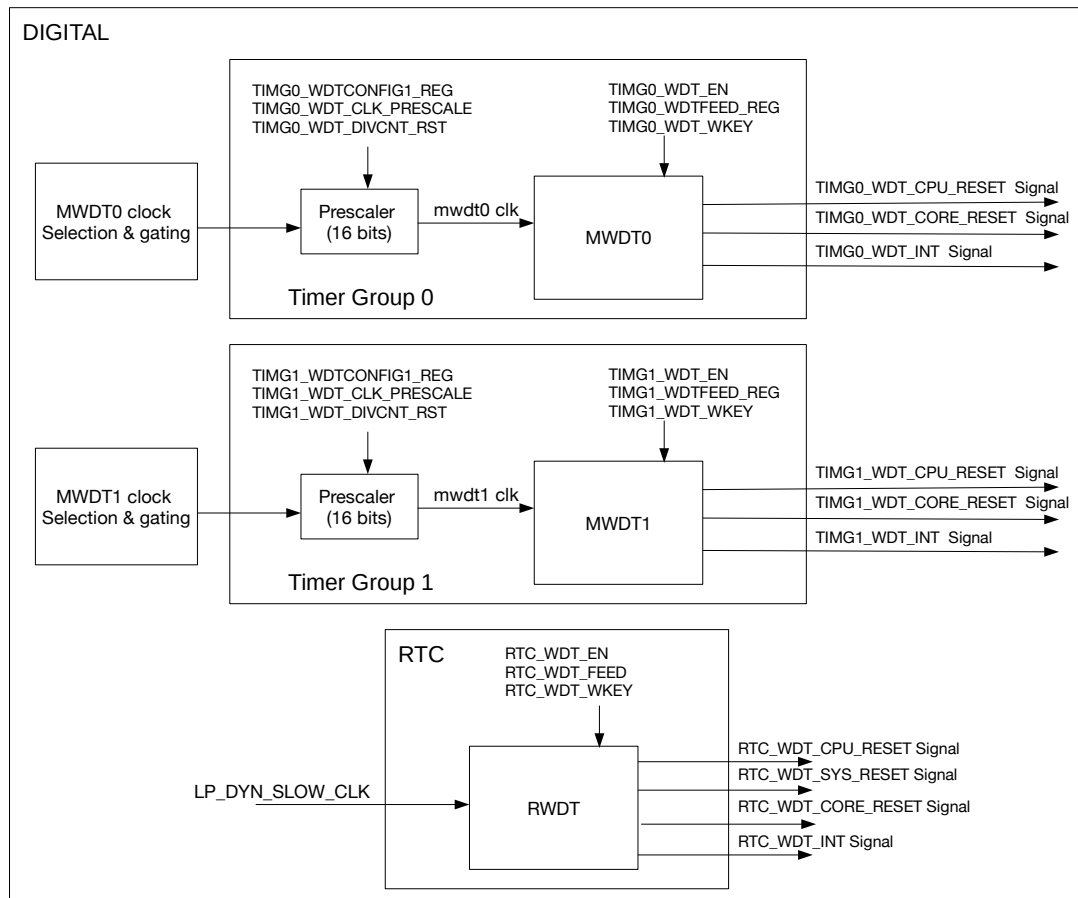


Figure 16.2-1. Digital Watchdog Timers in ESP32-P4

Figure 16.2-1 shows the three watchdog timers in ESP32-P4 digital systems.

### 16.2.2.1 Clock Source and 32-Bit Counter

At the core of each watchdog timer is a 32-bit counter.

Take MWDTO as an example:

- MWDTO can select between the `PLL_F80M_CLK`, `RC_FAST_CLK` or `XTAL_CLK` (external) clock as its clock source by setting the `HP_SYS_TIMERGRPO_WDT_SRC_SEL` field of the `HP_SYS_CLKRST_PERI_CLK_CTRL20_REG` register.
- The selected clock is switched on by setting `HP_SYS_TIMERGRPO_WDT_CLK_EN` field of the `HP_SYS_CLKRST_PERI_CLK_CTRL20_REG` register to 1 and switched off by setting it to 0. Then the selected clock is divided by a 16-bit configurable prescaler. See more details in Table 9.2-1 of Chapter 9.
- The 16-bit prescaler for MWDT is configured via the `TIMG_WDT_CLK_PRESCALE` field of `TIMG_WDTCONFIG1_REG`. When `TIMG_WDT_DIVCNT_RST` field is set, the prescaler is reset and it can be re-configured at once.

In contrast, the clock source of RWDT is derived directly from `LP_DYN_SLOW_CLK` (see details in Chapter 9

*Reset and Clock*).

MWDT and RWDT are enabled by setting the [TIMG\\_WDT\\_EN](#) and [RTC\\_WDT\\_EN](#) fields respectively. When enabled, the 32-bit counters of the watchdog will increment on each source clock cycle until the timeout value of the current stage is reached (i.e., timeout of the current stage). When this occurs, the current counter value is reset to zero and the next stage will become active. If a watchdog timer is fed by software, the timer will return to stage 0 and reset its counter value to zero. Software can feed a watchdog timer by writing any value to [TIMG\\_WDTFEED\\_REG](#) for MDWT and by writing 1 to [RTC\\_WDT\\_FEED](#) for RWDT.

### 16.2.2.2 Stages and Timeout Actions

Timer stages allow for a timer to have a series of different timeout values and corresponding timeout action. When one stage times out, the timeout action is triggered, the counter value is reset to zero, and the next stage becomes active.

MWDT/RWDT offers four stages (referred to as stages 0 to 3). The watchdog timers will progress through each stage in a loop (i.e., from stage 0 to 3, then back to stage 0).

Timeout values of each stage for MWDT are configured in [TIMG\\_WDTCONFIG<sub>i</sub>\\_REG](#) (where *i* ranges from 2 to 5), whilst timeout values for RWDT are configured using [RTC\\_WDT\\_STG<sub>j</sub>\\_HOLD](#) field (where *j* ranges from 0 to 3).

Please note that the timeout value of stage 0 for RWDT ( $Thold_0$ ) is determined by the combination of the [EFUSE\\_WDT\\_DELAY\\_SEL](#) field of eFuse register [EFUSE\\_RD\\_REPEAT\\_DATA0\\_REG](#) and [RTC\\_WDT\\_STG0\\_HOLD](#) field. The relationship is as follows:

$$T_{hold0} = \text{RTC\_WDT\_STG0\_HOLD} \ll (\text{EFUSE\_WDT\_DELAY\_SEL} + 1)$$

where  $\ll$  is a left-shift operator. For example, if [RTC\\_WDT\\_STG0\\_HOLD](#) is configured as 100 and [EFUSE\\_WDT\\_DELAY\\_SEL](#) is 1, the  $Thold_0$  will be 400 cycles.

Upon the timeout of each stage, one of the following timeout actions will be executed:

**Table 16.2-1. Timeout Actions**

| Timeout Action | Description  |
|----------------|--|
| Interrupt      | Trigger an interrupt   |
| HP CPU reset   | Reset the HP CPU0 and HP CPU1  |
| HP core reset  | HP core reset resets HP CPU0, HP CPI1, HP peripherals, HP GPIO, etc. |
| System reset   | Reset the whole digital system, including the LP system.             |
| Disabled       | No effect on the system  |

For MWDT, the timeout action of all stages is configured in [TIMG\\_WDTCONFIG0\\_REG](#). Likewise for RWDT, the timeout action is configured in [RTC\\_WDT\\_CONFIG0\\_REG](#).

### 16.2.2.3 Write Protection

Watchdog timers are critical to detecting and handling erroneous system/software behavior, thus should not be disabled easily (e.g., due to a misplaced register write). Therefore, MWDT and RWDT incorporate a write

protection mechanism that prevent the watchdogs from being disabled or tampered with due to an accidental write.

The write protection mechanism is implemented using a write-key field for each timer ([TIMG\\_WDT\\_WKEY](#) for MWDT, [RTC\\_WDT\\_WKEY](#) for RWDT). The value 0x50D83AA1 must be written to the watchdog timer's write-key field before any other register of the same watchdog timer can be changed. Any attempts to write to a watchdog timer's registers (other than the write-key field itself) whilst the write-key field's value is not 0x50D83AA1 will be ignored. The recommended procedure for accessing a watchdog timer is as follows:

1. Disable the write protection by writing the value 0x50D83AA1 to the timer's write-key field.
2. Make the required modification of the watchdog such as feeding or changing its configuration.
3. Re-enable write protection by writing any value other than 0x50D83AA1 to the timer's write-key field.

#### 16.2.2.4 Flash Boot Protection

Under the SPI boot mode, MWDT0 as well as RWDT, are automatically enabled. Stage 0 for the enabled MWDT0 is automatically configured as HP core reset action upon timeout, known as HP core reset. Likewise, stage 0 for RWDT is configured to system reset, which resets the main system and RTC when it times out. After SPI booting, [TIMG\\_WDT\\_FLASHBOOT\\_MOD\\_EN](#) and [RTC\\_WDT\\_FLASHBOOT\\_MOD\\_EN](#) should be cleared to stop the flash boot protection procedure for both MWDT0 and RWDT respectively. After this, MWDT0 and RWDT can be configured by software.

## 16.3 Super Watchdog

Super watchdog (SWD) is an ultra-low-power circuit in analog domain that helps to prevent the system from operating in a sub-optimal state and resets the system (system reset) if required. SWD contains a watchdog circuit that needs to be fed for at least once during its timeout period, which is slightly less than one second. About 100 ms before watchdog timeout, it will also send out a WD\_INTR signal as a request to remind the system to feed the watchdog.

If the system doesn't respond to SWD feed request and watchdog finally times out, SWD will generate a system level signal SWD\_RSTB to reset whole digital circuits on the chip (system reset) .

The source of the clock for SWD is constant and can not be selected.

### 16.3.1 Features

SWD has the following features:

- Ultra-low power
- Interrupt to indicate that the SWD is about to time out
- Various dedicated methods for software to feed SWD, which enables SWD to monitor the working state of the whole operating system

### 16.3.2 Super Watchdog Controller

### 16.3.2.1 Structure

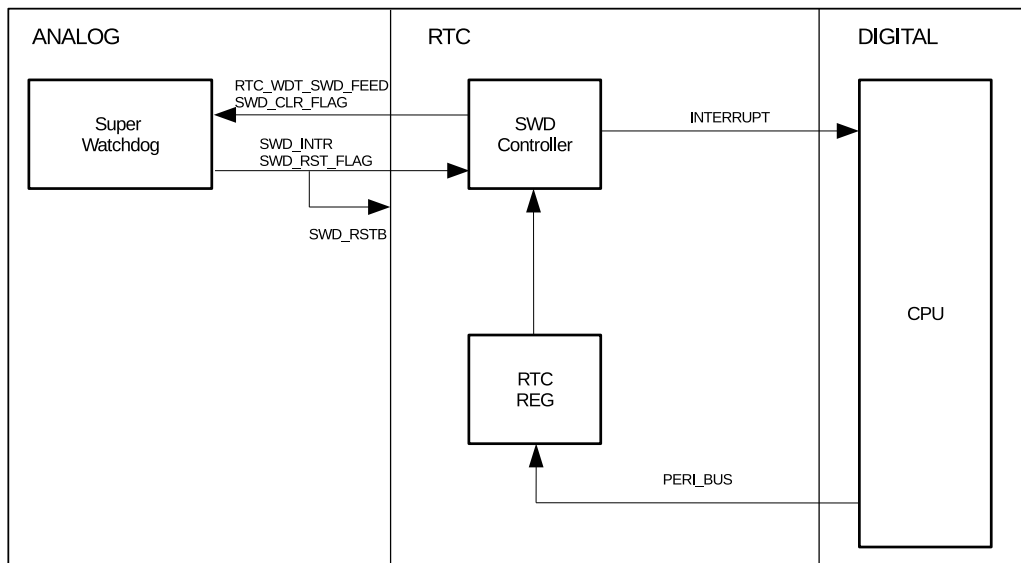


Figure 16.3-1. Super Watchdog Controller Structure

### 16.3.2.2 Workflow

In normal state:

- SWD controller receives feed request from SWD.
- SWD controller can send an interrupt to main CPU.
- Main CPU can feed SWD directly by setting [RTC\\_WDT\\_SWD\\_FEED](#).
- When trying to feed SWD, CPU needs to disable SWD controller's write protection by writing 0x50D83AA1 to [RTC\\_WDT\\_SWD\\_WKEY](#). This prevents SWD from being fed by mistake when the system is operating in sub-optimal state.
- If setting [RTC\\_WDT\\_SWD\\_AUTO\\_FEED\\_EN](#) to 1, SWD controller can also feed SWD itself without any interaction with CPU.

After reset:

- Check `LP_AONCLKRST_LPCORE_RESET_CAUSE[4:0]` for the cause of HP CPU reset.  
If `LP_AONCLKRST_LPCORE_RESET_CAUSE[4:0] == 0x12`, it indicates that the cause is SWD reset.
- Set [RTC\\_WDT\\_SWD\\_RST\\_FLAG\\_CLR](#) to clear the SWD reset flag.

## 16.4 Interrupts

For watchdog timer interrupts, please refer to Section [15.3.7 Interrupts](#) in Chapter [15 Timer Group \(TIMG\)](#).



## 16.5 Register Summary

The addresses in this section are relative to RTC\_WDT base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                     | Description                                     | Address | Access   |
|--|---|---------|----------|
| <b>configuration register</b>            |   |         |          |
| <a href="#">RTC_WDT_CONFIG0_REG</a>      | Configure the RWDT operation                    | 0x0000  | R/W      |
| <a href="#">RTC_WDT_CONFIG1_REG</a>      | Configure the RWDT timeout time of stage0       | 0x0004  | R/W      |
| <a href="#">RTC_WDT_CONFIG2_REG</a>      | Configure the RWDT timeout time of stage1       | 0x0008  | R/W      |
| <a href="#">RTC_WDT_CONFIG3_REG</a>      | Configure the RWDT timeout time of stage2       | 0x000C  | R/W      |
| <a href="#">RTC_WDT_CONFIG4_REG</a>      | Configure the RWDT timeout time of stage3       | 0x0010  | R/W      |
| <a href="#">RTC_WDT_FEED_REG</a>         | Configure the feed function of RWDT             | 0x0014  | WT       |
| <a href="#">RTC_WDT_WPROTECT_REG</a>     | Configure the lock function of RWDT             | 0x0018  | R/W      |
| <a href="#">RTC_WDT_SWD_CONFIG_REG</a>   | Configure the SWD operation                     | 0x001C  | varies   |
| <a href="#">RTC_WDT_SWD_WPROTECT_REG</a> | Configure the lock function of SWD              | 0x0020  | R/W      |
| <a href="#">RTC_WDT_INT_RAW_REG</a>      | Configure whether to generate timeout interrupt | 0x0024  | R/WTC/SS |
| <a href="#">RTC_WDT_INT_ST_REG</a>       | The interrupt status register of WDT            | 0x0028  | RO       |
| <a href="#">RTC_WDT_INT_ENA_REG</a>      | The interrupt enable register of WDT            | 0x002C  | R/W      |
| <a href="#">RTC_WDT_INT_CLR_REG</a>      | The interrupt clear register of WDT             | 0x0030  | WT       |
| <a href="#">RTC_WDT_DATE_REG</a>         | Version control register                        | 0x03FC  | R/W      |

## 16.6 Registers

MWDT registers are part of the timer submodule and are described in Section 15.5 *Register Summary* in Chapter 15 *Timer Group (TIMG)*.

The addresses of RWDT and SWD registers in this section are relative to RTC\_WDT base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

**Register 16.1. RTC\_WDT\_CONFIG0\_REG (0x0000)**

|            |     |              |     |              |     |              |     |              |     |                          |     |                          |    |                          |    |                         |   |                      |   |            |   |            |   |   |   |   |   |   |   |       |  |   |
|------------|-----|--------------|-----|--------------|-----|--------------|-----|--------------|-----|--------------------------|-----|--------------------------|----|--------------------------|----|-------------------------|---|----------------------|---|------------|---|------------|---|---|---|---|---|---|---|-------|--|---|
| RTC_WDT_EN |     | RTC_WDT_STG0 |     | RTC_WDT_STG1 |     | RTC_WDT_STG2 |     | RTC_WDT_STG3 |     | RTC_WDT_CPU_RESET_LENGTH |     | RTC_WDT_SYS_RESET_LENGTH |    | RTC_WDT_FLASHBOOT_MOD_EN |    | RTC_WDT_PROCPU_RESET_EN |   | RTC_WDT_PAUSE_IN_SLP |   | (reserved) |   | (reserved) |   |   |   |   |   |   |   |       |  |   |
| 31         | 30  | 28           | 27  | 25           | 24  | 22           | 21  | 19           | 18  | 16                       | 15  | 13                       | 12 | 11                       | 10 | 9                       | 8 |                      |   |            |   |            |   |   |   |   |   |   |   |       |  | 0 |
| 0          | 0x0 |              | 0x0 |              | 0x0 |              | 0x0 |              | 0x1 |                          | 0x1 |                          | 1  | 0                        | 0  | 1                       | 0 | 0                    | 0 | 0          | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |   |

**RTC\_WDT\_PAUSE\_IN\_SLP** Configure whether or not pause RWDT when chip is in sleep mode.

0: Enable

1: Disable

(R/W)

**RTC\_WDT\_PROCPU\_RESET\_EN** Configure whether or not to enable RWDT to reset CPU.

0: Disable

1: Enable

(R/W)

**RTC\_WDT\_FLASHBOOT\_MOD\_EN** Configure whether or not to enable RWDT when chip is in SPI boot mode.

0: Disable

1: Enable

(R/W)

**RTC\_WDT\_SYS\_RESET\_LENGTH** Configure the HP core reset time.

Measurement unit: LP\_DYN\_FAST\_CLK

(R/W)

**RTC\_WDT\_CPU\_RESET\_LENGTH** Configure the HP CPU reset time.

Measurement unit: LP\_DYN\_FAST\_CLK

(R/W)

**RTC\_WDT\_STG3** Configure the timeout action of stage3.

0: No operation

1: Generate interrupt

2: Generate HP CPU reset

3: Generate HP core reset

4: Generate system reset

(R/W)

Continued on the next page...

**Register 16.1. RTC\_WDT\_CONFIG0\_REG (0x0000)****Continued from the previous page...****RTC\_WDT\_STG2** Configure the timeout action of stage2.

- 0: No operation
- 1: Generate interrupt
- 2: Generate HP CPU reset
- 3: Generate HP core reset
- 4: Generate system reset
- (R/W)

**RTC\_WDT\_STG1** Configure the timeout action of stage1.

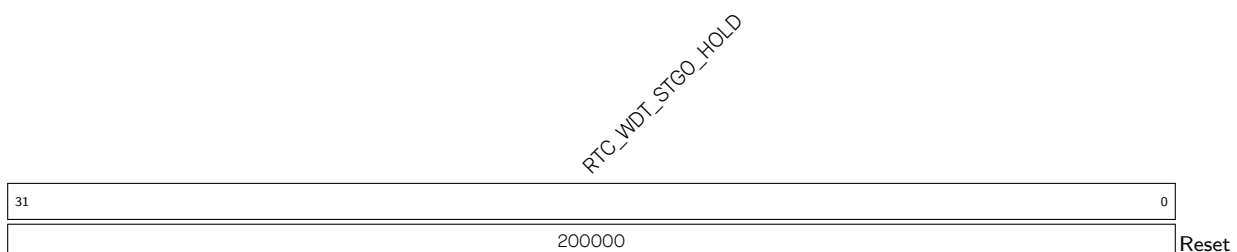
- 0: No operation
- 1: Generate interrupt
- 2: Generate HP CPU reset
- 3: Generate HP core reset
- 4: Generate system reset
- (R/W)

**RTC\_WDT\_STG0** Configure the timeout action of stage0.

- 0: No operation
- 1: Generate interrupt
- 2: Generate HP CPU reset
- 3: Generate HP core reset
- 4: Generate system reset
- (R/W)

**RTC\_WDT\_EN** Configure whether or not enable RWDT.

- 0: Disable RWDT
- 1: Enable RWDT
- (R/W)

**Register 16.2. RTC\_WDT\_CONFIG1\_REG (0x0004)****RTC\_WDT\_STGO\_HOLD** Configure the timeout time for stage0.

- Measurement unit: LP\_DYN\_SLOW\_CLK
- (R/W)

**Register 16.3. RTC\_WDT\_CONFIG2\_REG (0x0008)**

RTC\_WDT\_STG1\_HOLD

|       |   |
|-------|---|
| 31    | 0 |
| 80000 |   |
| Reset |   |

**RTC\_WDT\_STG1\_HOLD** Configure the timeout time for stage1.

Measurement unit: LP\_DYN\_SLOW\_CLK

(R/W)

**Register 16.4. RTC\_WDT\_CONFIG3\_REG (0x000C)**

RTC\_WDT\_STG2\_HOLD

|          |   |
|----------|---|
| 31       | 0 |
| 0x000fff |   |
| Reset    |   |

**RTC\_WDT\_STG2\_HOLD** Configure the timeout time for stage2.

Measurement unit: LP\_DYN\_SLOW\_CLK

(R/W)

**Register 16.5. RTC\_WDT\_CONFIG4\_REG (0x0010)**

RTC\_WDT\_STG3\_HOLD

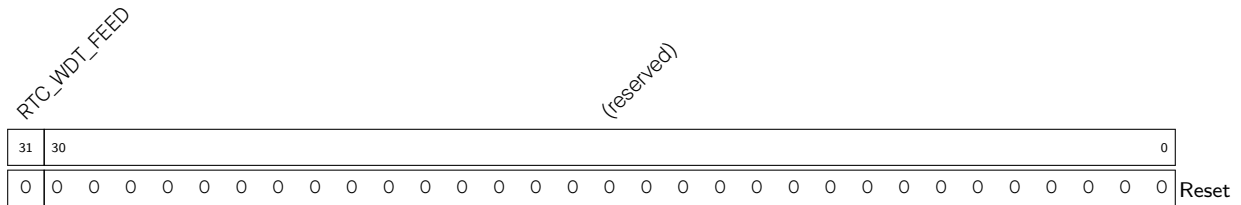
|          |   |
|----------|---|
| 31       | 0 |
| 0x000fff |   |
| Reset    |   |

**RTC\_WDT\_STG3\_HOLD** Configure the timeout time for stage3.

Measurement unit: LP\_DYN\_SLOW\_CLK

(R/W)

### Register 16.6. RTC\_WDT\_FEED\_REG (0x0014)



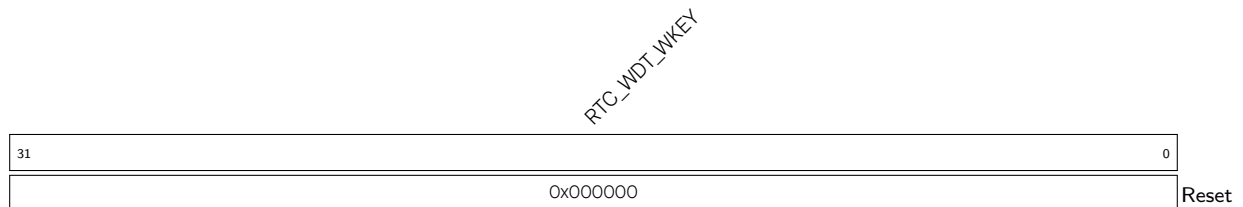
**RTC\_WDT\_FEED** Configure this bit to feed the RWDT.

0: Invalid

1: Feed RWDT

(WT)

### Register 16.7. RTC\_WDT\_WPROTECT\_REG (0x0018)



**RTC\_WDT\_WKEY** Configure this field to lock or unlock RWD's configuration registers.

0x50D83AA1: unlock the RWDt configuration register

Others value: lock the RWDT configuration register which can't be modified by software.

(R/W)

**Register 16.8. RTC\_WDT\_SWD\_CONFIG\_REG (0x001C)**

|   |    |     |                          |  |  |  |  |   |  |    |    |   |   |   |            |   |   |   |   |   |                        |   |   |   |       |
|---|----|-----|--------------------------|--|--|--|--|---|--|----|----|---|---|---|------------|---|---|---|---|---|------------------------|---|---|---|-------|
| RTC_WDT_SWD_FEED<br>RTC_WDT_SWD_DISABLE |    |     | RTC_WDT_SWD_SIGNAL_WIDTH |  |  |  |  |   | RTC_WDT_SWD_RST_FLAG_CLR<br>RTC_WDT_SWD_AUTO_FEED_EN |    |    |   |   |   | (reserved) |   |   |   |   |   | RTC_WDT_SWD_RESET_FLAG |   |   |   |       |
| 31                                      | 30 | 29  | 20                       |  |  |  |  |   | 19   | 18 | 17 |   |   |   |            |   |   | 1 | 0 |   |                        |   |   |   |       |
| 0                                       | 0  | 300 |                          |  |  |  |  | 0 | 0  | 0  | 0  | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | Reset |

**RTC\_WDT\_SWD\_RESET\_FLAG** Represents the SWD whether has generated the reset signal

0: No

1: Yes

(RO)

**RTC\_WDT\_SWD\_AUTO\_FEED\_EN** Configure this bit to enable to feed SWD automatically by hardware.

0: Disable

1: Enable

(R/W)

**RTC\_WDT\_SWD\_RST\_FLAG\_CLR** Configure this bit to clear SWD reset flag

0: Invalid

1: Clear the reset flag

(WT)

**RTC\_WDT\_SWD\_SIGNAL\_WIDTH** Configure the SWD signal length that output to analog circuit.

Measurement unit: LP\_DYN\_FAST\_CLK (R/W)

**RTC\_WDT\_SWD\_DISABLE** Configure this bit to disable the SWD.

0: Enable the SWD

1: Disable the SWD

(R/W)

**RTC\_WDT\_SWD\_FEED** Configure this bit to feed the SWD.

0: Invalid

1: Feed SWD

(WT)

Register 16.9. RTC\_WDT\_SWD\_WPROTECT\_REG (0x0020)

|                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| RTC_WDT_SWD_WKEY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**RTC\_WDT\_SWD\_WKEY** Configure this field to lock or unlock SWD's configuration registers.  
0x50D83AA1: unlock the SWD configuration register.  
Others value: lock the SWD configuration register which can't be modified by the software.  
(R/W)

Register 16.10. RTC\_WDT\_INT\_RAW\_REG (0x0024)

|  |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| RTC_WDT_SWDT_INT_RAW<br>RTC_WDT_RWDT_INT_RAW<br>(reserved) |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**RTC\_WDT\_SWDT\_INT\_RAW** Represents the SWD whether or not has generated timeout interrupt.  
0: No  
1: Yes  
(R/WTC/SS)

**RTC\_WDT\_RWDT\_INT\_RAW** Represents the RWDT whether or not generates timeout interrupt.  
0: No  
1: Yes  
(R/WTC/SS)

### Register 16.11. RTC\_WDT\_INT\_ST\_REG (0x0028)

[illegible]

**RTC\_WDT\_SWDT\_INT\_ST** Represents the SWD whether or not has generated and sent timeout interrupt to CPU.

0: No

1: Yes

(RO)

**RTC\_WDT\_RWDT\_INT\_ST** Represents the RWDT whether or not generates and sends timeout interrupt to CPU.

0: No

1: Yes

(RO)

### Register 16.12. RTC\_WDT\_INT\_ENA\_REG (0x002C)

Diagram of the 32-bit RWDW register structure:

- Bit 31: RTC\_WDT\_SWDT\_INT\_ENA
- Bit 30: RTC\_WDT\_SWDT\_INT\_ENA
- Bits 29-0: (reserved)
- Bit 0: Reset

**RTC\_WDT\_SWDT\_INT\_ENA** Configure whether or not to enable the SWD to send timeout interrupt.

0: Disable

1: Enable

(R/W)

**RTC\_WDT\_RWDT\_INT\_ENA** Configure whether or not to enable the RWDT to send timeout interrupt.

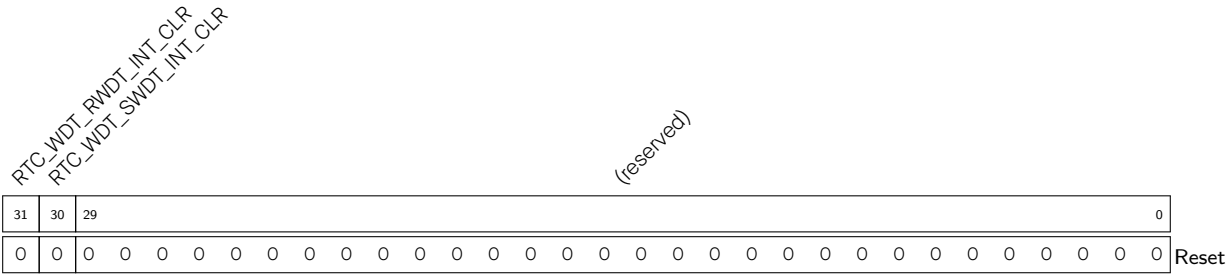
0: Disable

1: Enable

(R/W)



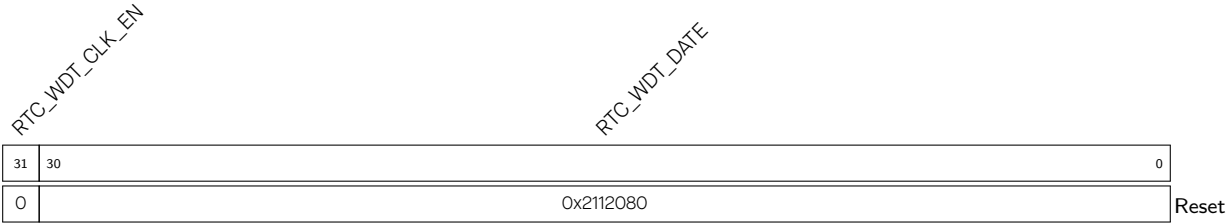
Register 16.13. RTC\_WDT\_INT\_CLR\_REG (0x0030)



**RTC\_WDT\_SWDT\_INT\_CLR** Configure whether to clear the timeout interrupt signal sent by SWD to CPU.  
0: No  
1: Yes  
(WT)

**RTC\_WDT\_RWDT\_INT\_CLR** Configure whether to clear the timeout interrupt signal sent by RWDT to CPU.  
0: No  
1: Yes  
(WT)

Register 16.14. RTC\_WDT\_DATE\_REG (0x03FC)



**RTC\_WDT\_DATE** Version control register. (R/W)  
**RTC\_WDT\_CLK\_EN** Reserved. (R/W)

## Chapter 17

### RTC Timer

#### 17.1 Introduction

RTC Timer is an important module for implementing low power management of ESP32-P4. Based on a 48-bit readable counter, RTC Timer is mainly used as a system timer in low power mode when the timer peripheral in the HP system is unavailable. It also allows for configuring timer interrupts and logging the time when specific events happen in the system. The supported events are described in the [17.3 Functional Description](#).

#### 17.2 Feature List

RTC Timer has the following features:

- 48-bit counter
- Time logging when one of the following events happens:
  - HP system reset
  - CPU enters stall state
  - CPU exits stall state
  - Crystal powers up
  - Crystal powers down
- Time logging through register configuration
- Occurrence time cached of the most recent two specific events
- Generation of interrupts at target times, which are configurable. It is also possible to configure two target times simultaneously.
- Uninterrupted operation during any reset or sleep mode, except for power-on reset of LP system.

#### 17.3 Functional Description

- 48-bit counter
  - The implementation of the RTC Timer is based on a 48-bit counter, driven by the RC\_SLOW\_CLK in the AlwaysOn power domain. It uses continuous loop counting (except during LP system reset), and an overflow interrupt is generated when the 48-bit counter overflows.
- Log the occurrence time of specific events
  - RTC Timer supports logging the occurrence time of three types of events:

- \* HP system reset
  - \* CPU enters or exits stall state
  - \* Crystal powers up or down
- The above three types of events have their own independent configuration registers. When the configuration registers are enabled, if the corresponding events occur, the hardware pulse generated will trigger the RTC Timer to log the current time. The corresponding configuration registers are shown in the table below.

**Table 17.3-1. Configure RTC Timer to Log the Occurrence Time of Specific Events**

| Configuration Register                         | Description  |
|--|--|
| <a href="#">RTC_TIMER_MAIN_TIMER_SYS_RST</a>   | Enable the RTC Timer to log the time of system reset.                              |
| <a href="#">RTC_TIMER_MAIN_TIMER_SYS_STALL</a> | Enable the RTC Timer to log the time when the CPU enters or exits the stall state. |
| <a href="#">RTC_TIMER_MAIN_TIMER_XTAL_OFF</a>  | Enable the RTC Timer to log the time when the crystal powers up or down.           |

- Log the current time through software configuration.
  - In addition to the above three specific events that can trigger the RTC Timer to log the time, the RTC Timer can also record the current time through the configuration register [RTC\\_TIMER\\_MAIN\\_TIMER\\_UPDATE](#).
  - A pulse signal will be generated by configuring the [RTC\\_TIMER\\_MAIN\\_TIMER\\_UPDATE](#), which will trigger the RTC Timer to record the current time.
- Generate counting interrupts at target times
  - RTC Timer supports configuring two target times simultaneously, referred to as target time 0 and target time 1. When the timer reaches target time 0, it will trigger the [RTC\\_TIMER\\_CMPO\\_INT](#) interrupt. Similarly, when the timer reaches Target Moment 1, it will trigger the [RTC\\_TIMER\\_CMP1\\_INT](#) interrupt.
  - Configure the target times through the registers below:

**Table 17.3-2. Target times Configuration**

| Configuration Register                                      | Description   |
|---|---|
| <a href="#">RTC_TIMER_MAIN_TIMER_TAR_EN<math>n</math></a>   | $n = 0$ or $1$ , enable target time configuration.              |
| <a href="#">RTC_TIMER_MAIN_TIMER_TAR_LOW<math>n</math></a>  | $n = 0$ or $1$ , configure the low 32 bits of the target time.  |
| <a href="#">RTC_TIMER_MAIN_TIMER_TAR_HIGH<math>n</math></a> | $n = 0$ or $1$ , configure the high 16 bits of the target time. |

- Read the time cached in the RTC Timer
  - There are two sets of registers used to cache the occurrence time of specific events, namely register group 0 and register group 1.
  - Register group 0 includes register [RTC\\_TIMER\\_MAIN\\_BUFO\\_LOW\\_REG](#) and [RTC\\_TIMER\\_MAIN\\_BUF1\\_HIGH\\_REG](#) which are used to cache the count value of the RTC Timer under the current trigger.

- Register group 1 includes register [RTC\\_TIMER\\_MAIN\\_BUF1\\_LOW\\_REG](#) and [RTC\\_TIMER\\_MAIN\\_BUF1\\_HIGH\\_REG](#), which are used to cache the count value of the RTC Timer from the last trigger.
- On a new trigger, the record from the previous trigger will be moved from register group 0 to register group 1 (and the previous record in register group 1 will be overwritten), and the record of this trigger will be stored in register group 0. Therefore, only the last two triggers can be logged at any time.

## 17.4 Event Task Matrix Feature

The RTC Timer on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows RTC Timer's ETM tasks to be triggered by any peripherals' ETM events, or RTC Timer's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to RTC Timer. For more information, please refer to Chapter [12 Event Task Matrix \(ETM\)](#).

RTC Timer doesn't receive any ETM tasks:

RTC Timer can generate the following ETM events:

- [RTC\\_EVT\\_CMP](#): Indicate that the RTC Timer reaches the target time 0 configured by [RTC\\_TIMER\\_MAIN\\_TIMER\\_TAR\\_LOW0](#) and [RTC\\_TIMER\\_MAIN\\_TIMER\\_TAR\\_HIGH0](#).
- [RTC\\_EVT\\_OVF](#): Indicate the 48-bit counter overflow.
- [RTC\\_EVT\\_TICK](#): Indicates the event that occurs when the RTC timer increments by 1.

## 17.5 Interrupts

ESP32-P4's RTC Timer can generate the following interrupt signal(s) that will be sent to the [Interrupt Matrix](#).

- [LP\\_TIMER\\_REG\\_O\\_INTR](#)
- [LP\\_TIMER\\_REG\\_1\\_INTR](#)

There are several internal interrupt sources from RTC Timer that can generate the above interrupt signal(s). The interrupt sources from RTC Timer are listed with their trigger conditions and the resulted interrupt signal(s) in Table [17.5-1](#).

**Table 17.5-1. RTC Timer's Internal Interrupt Sources**

| Internal Interrupt Source              | Trigger Condition                   | Interrupt Signal   |
|--|-------------------------------------|--|
| <a href="#">RTC_TIMER_CMPO_INT</a>     | RTC Timer reaches the target time 0 | <a href="#">LP_TIMER_REG_O_INTR</a>  |
| <a href="#">RTC_TIMER_CMP1_INT</a>     | RTC Timer reaches the target time 1 | <a href="#">LP_TIMER_REG_1_INTR</a>  |
| <a href="#">RTC_TIMER_OVERFLOW_INT</a> | 48-bit counter overflow             | <a href="#">LP_TIMER_REG_O_INTR</a><br><a href="#">LP_TIMER_REG_1_INTR</a> |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [17.6 Register Summary](#).

## 17.6 Register Summary

The addresses in this section are relative to RTC Timer base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

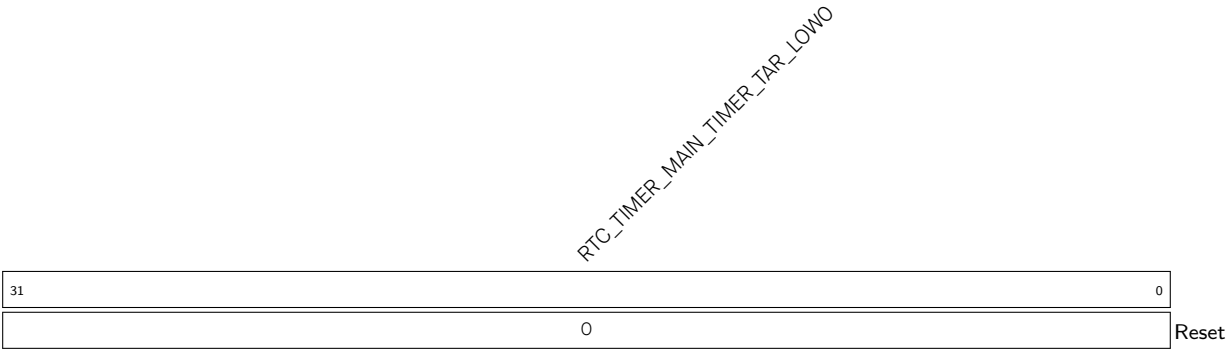
| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Configuration Registers</b>               |  |         |        |
| <a href="#">RTC_TIMER_TARO_LOW_REG</a>       | Configure the low 32 bits of the target time 0                                 | 0x0000  | R/W    |
| <a href="#">RTC_TIMER_TARO_HIGH_REG</a>      | Configure the high 16 bits of the target time 0                                | 0x0004  | varies |
| <a href="#">RTC_TIMER_TAR1_LOW_REG</a>       | Configure the low 32 bits of the target time 1                                 | 0x0008  | R/W    |
| <a href="#">RTC_TIMER_TAR1_HIGH_REG</a>      | Configure the high 16 bits of the target time 1                                | 0x000C  | varies |
| <a href="#">RTC_TIMER_UPDATE_REG</a>         | Configure to enable the RTC Timer to latch current value                       | 0x0010  | varies |
| <a href="#">RTC_TIMER_MAIN_BUFO_LOW_REG</a>  | The low 32 bits of the cached value 0 in RTC Timer                             | 0x0014  | RO     |
| <a href="#">RTC_TIMER_MAIN_BUFO_HIGH_REG</a> | The high 16 bits of the cached value 0 in RTC Timer                            | 0x0018  | RO     |
| <a href="#">RTC_TIMER_MAIN_BUF1_LOW_REG</a>  | The low 32 bits of the cached value 1 in RTC Timer                             | 0x001C  | RO     |
| <a href="#">RTC_TIMER_MAIN_BUF1_HIGH_REG</a> | The high 16 bits of the cached value 1 in RTC Timer                            | 0x0020  | RO     |
| <b>Interrupt Registers</b>                   |  |         |        |
| <a href="#">RTC_TIMER_INT_RAW_REG</a>        | The interrupt raw status register for the RTC Timer reaching the target time 0 | 0x0028  | RO     |
| <a href="#">RTC_TIMER_INT_ST_REG</a>         | The interrupt status register for the RTC Timer reaching the target time 0     | 0x002C  | RO     |
| <a href="#">RTC_TIMER_INT_ENA_REG</a>        | The interrupt enable register for the RTC Timer reaching the target time 0     | 0x0030  | R/W    |
| <a href="#">RTC_TIMER_INT_CLR_REG</a>        | The interrupt clear register for the RTC Timer reaching the target time 0      | 0x0034  | WO     |
| <a href="#">RTC_TIMER_LP_INT_RAW_REG</a>     | The interrupt raw status register for RTC Timer reaching the target time 1     | 0x0038  | RO     |
| <a href="#">RTC_TIMER_LP_INT_ST_REG</a>      | The interrupt status register for the RTC Timer reaching the target time 1     | 0x003C  | RO     |
| <a href="#">RTC_TIMER_LP_INT_ENA_REG</a>     | The interrupt enable register for the RTC Timer reaching the target time 1     | 0x0040  | R/W    |
| <a href="#">RTC_TIMER_LP_INT_CLR_REG</a>     | The interrupt clear register for the RTC Timer reaching the target time 1      | 0x0044  | WO     |
| <b>Version Register</b>                      |  |         |        |
| <a href="#">RTC_TIMER_DATE_REG</a>           | Version control register   | 0x03FC  | R/W    |

## 17.7 Registers

The addresses in this section are relative to RTC Timer base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

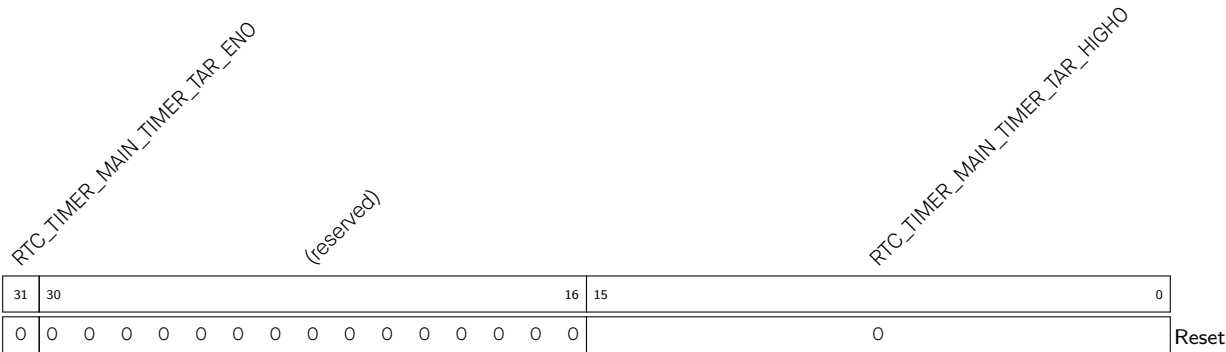
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 17.1. RTC\_TIMER\_TARO\_LOW\_REG (0x0000)



**RTC\_TIMER\_MAIN\_TIMER\_TAR\_LOWO** Configure the low 32 bits of the target time 0 of the RTC Timer. (R/W)

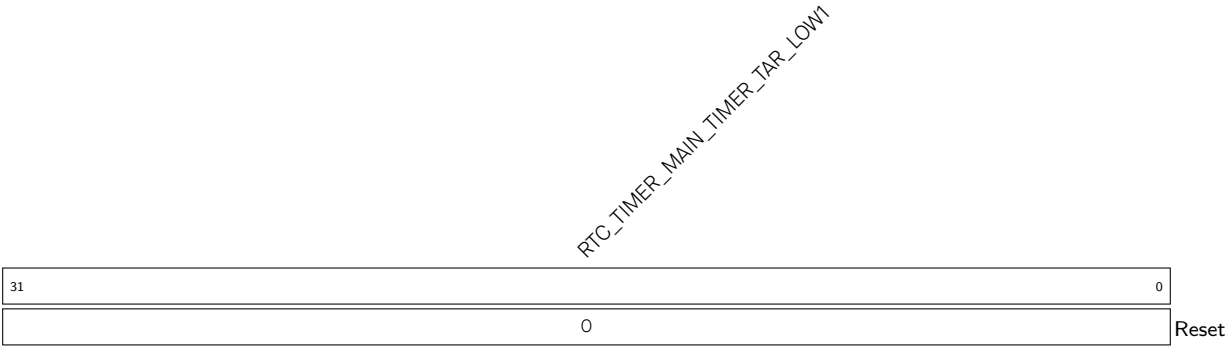
Register 17.2. RTC\_TIMER\_TARO\_HIGH\_REG (0x0004)



**RTC\_TIMER\_MAIN\_TIMER\_TAR\_HIGHO** Configure the high 16 bits of the target time 0. (R/W)

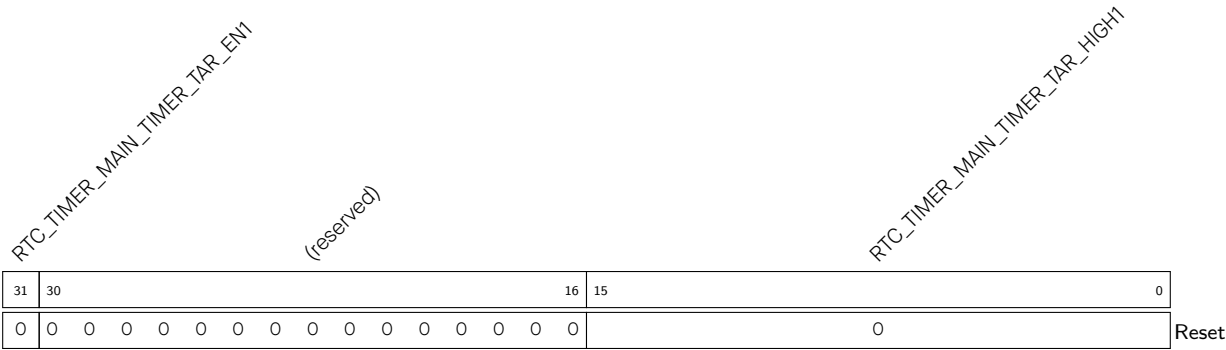
**RTC\_TIMER\_MAIN\_TIMER\_TAR\_ENO** Configure to enable the target time 0 of the RTC Timer. (WO)

Register 17.3. RTC\_TIMER\_TAR1\_LOW\_REG (0x0008)



**RTC\_TIMER\_MAIN\_TIMER\_TAR\_LOW1** Configure the low 32 bits of the target time 1. (R/W)

Register 17.4. RTC\_TIMER\_TAR1\_HIGH\_REG (0x000C)



**RTC\_TIMER\_MAIN\_TIMER\_TAR\_HIGH1** Configure the high 16 bits of the target time 1. (R/W)

**RTC\_TIMER\_MAIN\_TIMER\_TAR\_EN1** Configure to enable the target time 1 of the RTC Timer. (WO)



### Register 17.5. RTC\_TIMER\_UPDATE\_REG (0x0010)

Diagram of the 32-bit register structure for `RTC_TIMER_MAIN_TIMER_SYS_RST`:

- Bits 31-24: `RTC_TIMER_MAIN_TIMER_SYS_RST`
- Bits 23-16: `RTC_TIMER_MAIN_TIMER_SYS_STALL`
- Bits 15-8: `RTC_TIMER_MAIN_TIMER_XTAL_OFF`
- Bits 7-0: `RTC_TIMER_MAIN_TIMER_UPDATE`

The register is shown as a single large '0', indicating it is a read-only register. A 'Reset' label is present at the bottom right.

**RTC\_TIMER\_MAIN\_TIMER\_UPDATE** Configure to log the current time through software configuration. (WO)

**RTC\_TIMER\_MAIN\_TIMER\_XTAL\_OFF** Configure to enable RTC Timer to log the time when the crystal powers up or down. (R/W)

**RTC\_TIMER\_MAIN\_TIMER\_SYS\_STALL** Configure to enable the RTC Timer to log the time when the CPU enters or exits the stall state. (R/W)

|                                     |   |
|-------------------------------------|---|
| <b>RTC_TIMER_MAIN_TIMER_SYS_RST</b> | Configure to enable RTC Timer to log the time of system reset.<br>(R/W) |
|-------------------------------------|---|

### Register 17.6. RTC\_TIMER\_MAIN\_BUFO\_LOW\_REG (0x0014)

31

RTC\_TIMER\_MAIN\_TIMER\_BUFO\_LOW

0

Reset

**RTC\_TIMER\_MAIN\_TIMER\_BUFO\_LOW** Represent the low 32 bits of the cached value 0 in RTC Timer. (RO)

Register 17.7. RTC\_TIMER\_MAIN\_BUFO\_HIGH\_REG (0x0018)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|----|---|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RTC_TIMER_MAIN_TIMER_BUFO_HIGH |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                             | 15 |   |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0  | 0 |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**RTC\_TIMER\_MAIN\_TIMER\_BUFO\_HIGH** Represent the high 16 bits of the cached value 0 in RTC Timer. (RO)

Register 17.8. RTC\_TIMER\_MAIN\_BUF1\_LOW\_REG (0x001C)

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| RTC_TIMER_MAIN_TIMER_BUF1_LOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

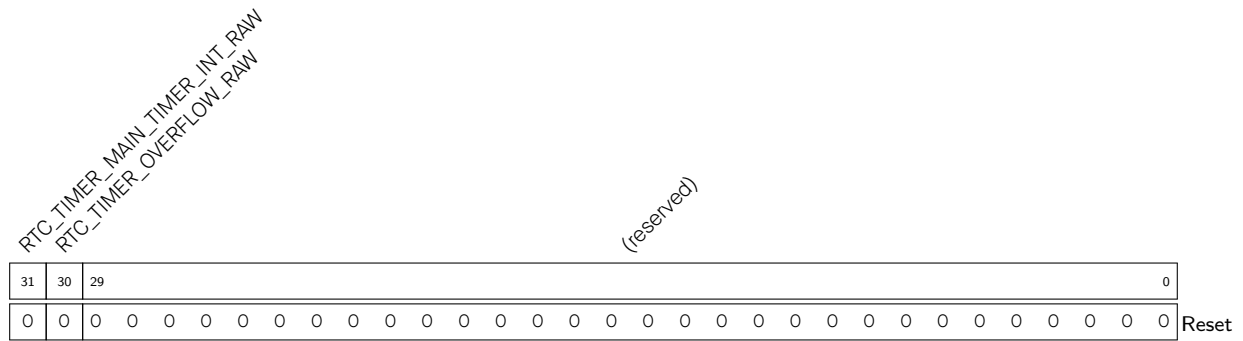
**RTC\_TIMER\_MAIN\_TIMER\_BUF1\_LOW** Represent the low 32 bits of the cached value 1 in RTC Timer. (RO)

Register 17.9. RTC\_TIMER\_MAIN\_BUF1\_HIGH\_REG (0x0020)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|----|---|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RTC_TIMER_MAIN_TIMER_BUF1_HIGH |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                             | 15 |   |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0  | 0 |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**RTC\_TIMER\_MAIN\_TIMER\_BUF1\_HIGH** Represent the high 16 bits of the cached value 1 in RTC Timer. (RO)

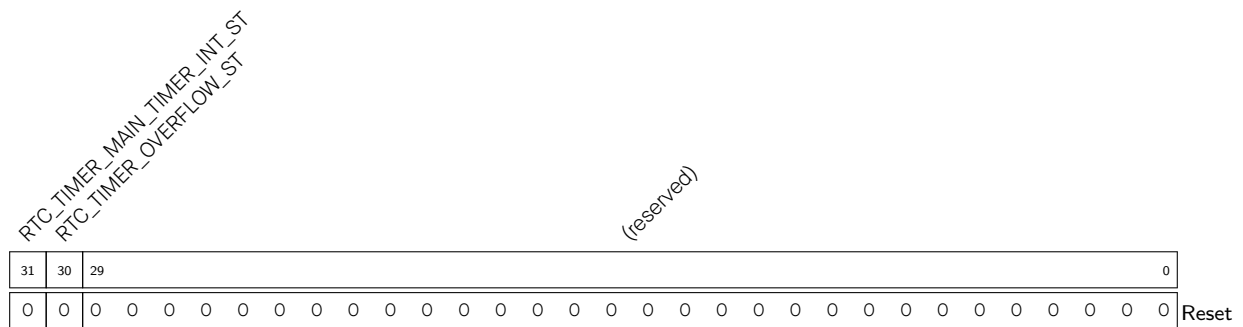
## Register 17.10. RTC\_TIMER\_INT\_RAW\_REG (0x0028)



**RTC\_TIMER\_OVERFLOW\_RAW** The interrupt raw status for the 48-bit counter overflow. (RO)

**RTC\_TIMER\_MAIN\_TIMER\_INT\_RAW** The interrupt raw status for the RTC Timer reaching the target time 0. (RO)

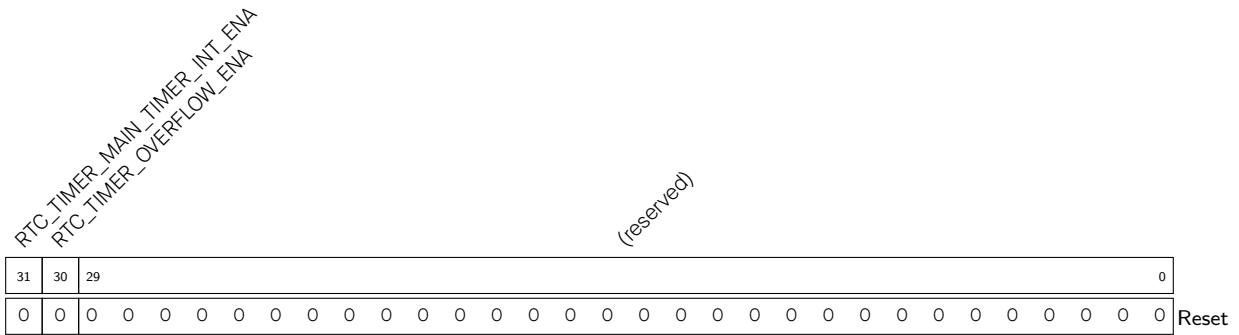
## Register 17.11. RTC\_TIMER\_INT\_ST\_REG (0x002C)



**RTC\_TIMER\_OVERFLOW\_ST** The interrupt status for the 48-bit counter overflow. (RO)

**RTC\_TIMER\_MAIN\_TIMER\_INT\_ST** The interrupt status for the RTC Timer reaching the target time 0. (RO)

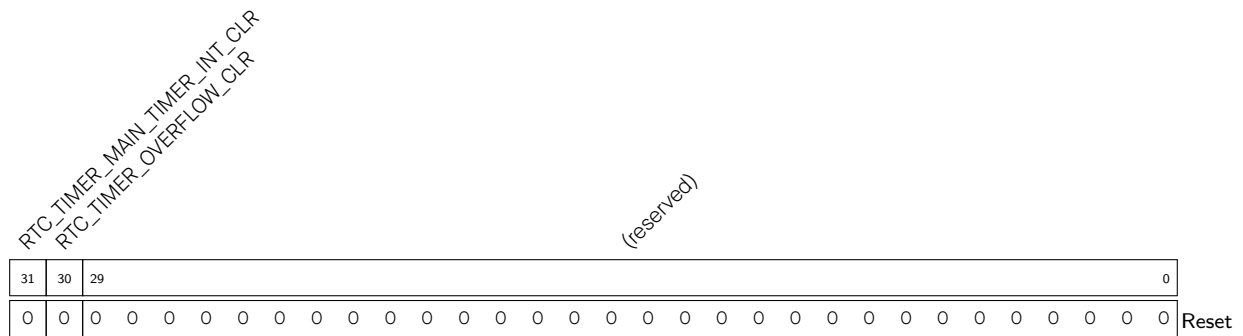
## Register 17.12. RTC\_TIMER\_INT\_ENA\_REG (0x0030)



**RTC\_TIMER\_OVERFLOW\_ENA** Configure to enable the interrupt for 48-bit counter overflow. (R/W)

**RTC\_TIMER\_MAIN\_TIMER\_INT\_ENA** Configure to enable the interrupt for the RTC Timer reaching the target time 0. (R/W)

## Register 17.13. RTC\_TIMER\_INT\_CLR\_REG (0x0034)



**RTC\_TIMER\_OVERFLOW\_CLR** Configure to clear the interrupt for 48-bit counter overflow. (WO)

**RTC\_TIMER\_MAIN\_TIMER\_INT\_CLR** Configure to clear the interrupt for the RTC Timer reaching the target time 0. (WO)

### Register 17.14. RTC\_TIMER\_LP\_INT\_RAW\_REG (0x0038)

Diagram of the RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_RAW register. The register is 32 bits wide, with bits 31 and 30 labeled 'RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_RAW' and bit 29 labeled 'RTC\_TIMER\_MAIN\_TIMER\_OVERFLOW\_LP\_INT\_RAW'. The remaining bits (0-28) are labeled '(reserved)'. The register is shown as a horizontal bar with a 'Reset' button on the right.

**RTC\_TIMER\_MAIN\_TIMER\_OVERFLOW\_LP\_INT\_RAW** The interrupt raw status for the 48-bit counter overflow. (RO)

**RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_RAW** The interrupt raw status for the RTC Timer reaching the target time 1.(RO)

### Register 17.15. RTC\_TIMER\_LP\_INT\_ST\_REG (0x003C)

Diagram illustrating the structure of the RTC\_CR register (32 bits):

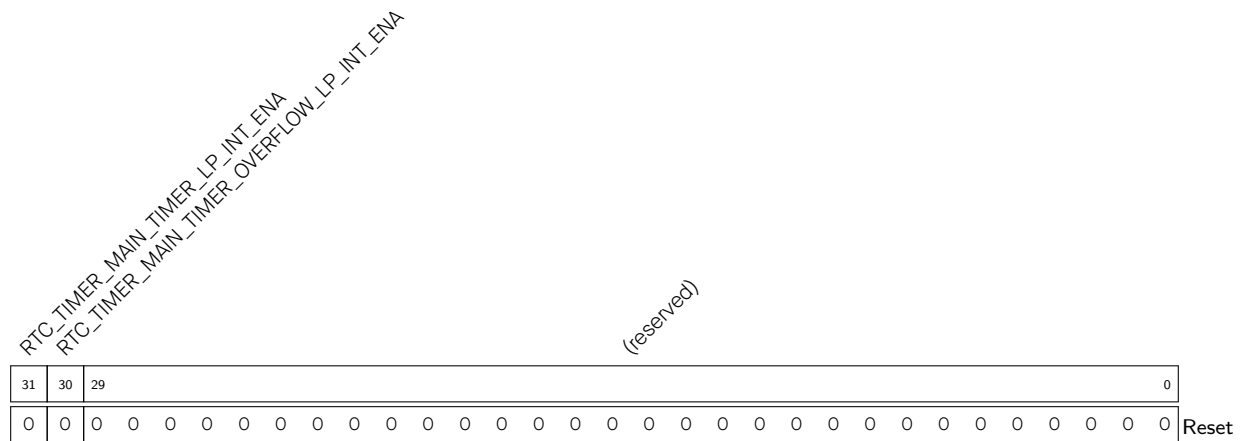
- Bit 31: RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_ST
- Bit 30: RTC\_TIMER\_MAIN\_TIMER\_OVERFLOW\_LP\_INT\_ST
- Bits 29-0: (reserved)

The register is shown as a horizontal bar with bit positions 31, 30, and 29 marked at the left end, and a '0' at the right end. Below the bar, the bits are shown as a sequence of 0s and 1s, with the last bit being 0.

|  |  |
|--|--|
| <b>RTC_TIMER_MAIN_TIMER_OVERFLOW_LP_INT_ST</b> | The interrupt status for the 48-bit counter overflow. (RO) |
|--|--|

|                                       |  |
|---------------------------------------|--|
| <b>RTC_TIMER_MAIN_TIMER_LP_INT_ST</b> | The interrupt status for the RTC Timer reaching the target time 1.(RO) |
|---------------------------------------|--|

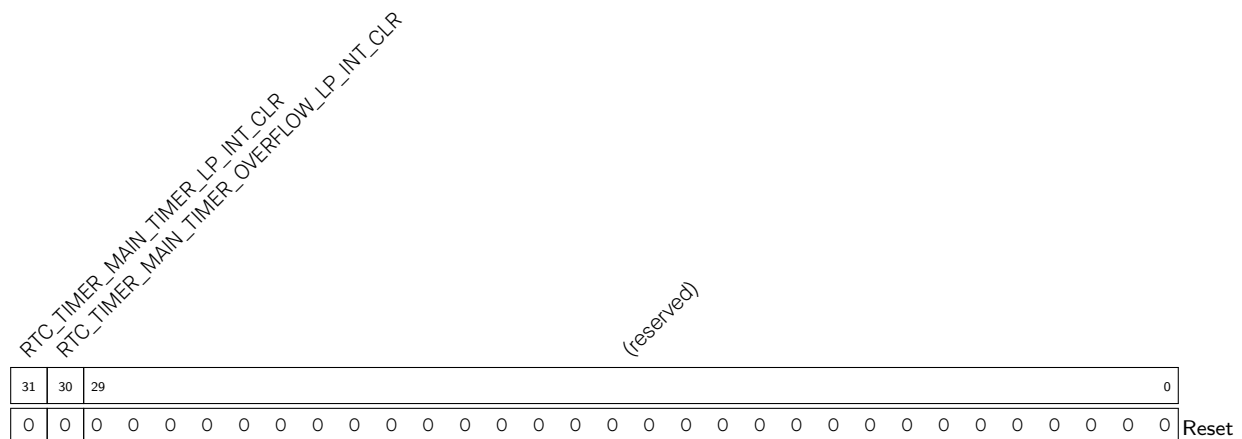
Register 17.16. RTC\_TIMER\_LP\_INT\_ENA\_REG (0x0040)



**RTC\_TIMER\_MAIN\_TIMER\_OVERFLOW\_LP\_INT\_ENA** Configure to enable the interrupt for the 48-bit counter overflow. (R/W)

**RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_ENA** Configure to enable the interrupt for the RTC Timer reaching the target time 1. (R/W)

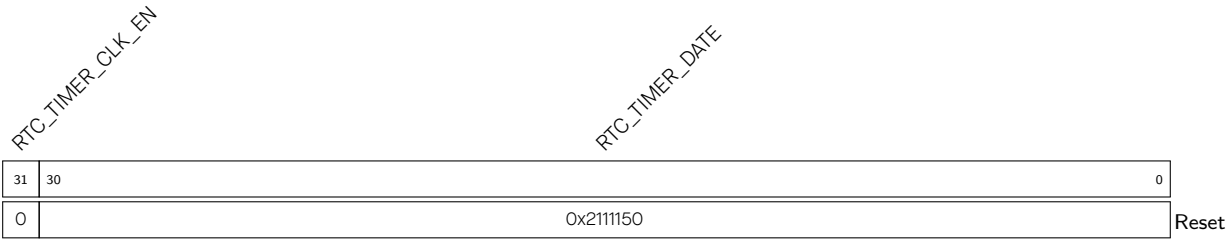
Register 17.17. RTC\_TIMER\_LP\_INT\_CLR\_REG (0x0044)



**RTC\_TIMER\_MAIN\_TIMER\_OVERFLOW\_LP\_INT\_CLR** Configure to clear the interrupt for 48-bit counter overflow. (WO)

**RTC\_TIMER\_MAIN\_TIMER\_LP\_INT\_CLR** Configure to clear the interrupt for the RTC Timer reaching the target time 1. (WO)

Register 17.18. RTC\_TIMER\_DATE\_REG (0x03FC)



- RTC\_TIMER\_DATE** Version control register. (R/W)
- RTC\_TIMER\_CLK\_EN** Configure to enable the register read/write clock. (R/W)

## Chapter 18

### Permission Control (PMS)

#### 18.1 Overview

The permission control of ESP32-P4 consists of two parts: PMP (Physical Memory Protection) and APM (Access Permission Management).

PMP is located inside the HP CPUs and can control the HP CPUs' access to all address spaces. APM is an access permission management module located at the bus port, which can manage the permissions for the CPU (HP CPU0/1, LP CPU) to access the registers of all on-chip peripherals (see HP CPU PERI, HP PERI, and LP PERI in Table 18.1-1) and part of internal and external memory. The APM can also manage DMA masters like VDMA, USB OTG 2.0, to access parts of internal and external memory.

The APM module compares the configurable address range or the fixed address range, the access permissions of each address range, and the information carried on the bus like master ID, security mode, access address, access type, etc, to determine whether the access is allowed. With APM, users can precisely control the access of all masters to the memory and peripheral registers.

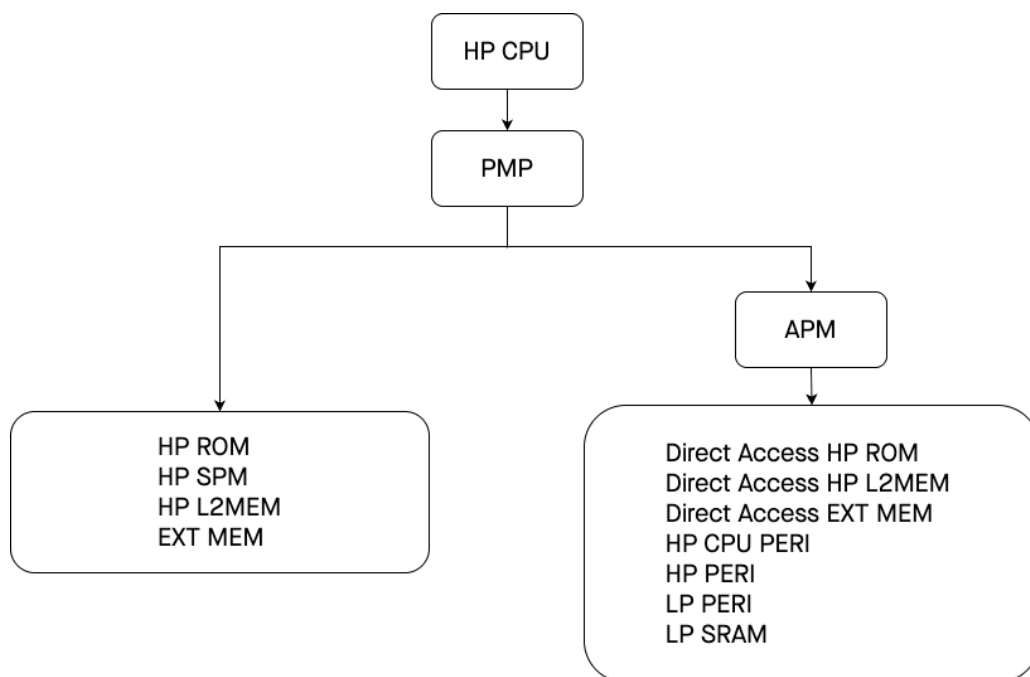
The distribution of management areas by PMP and APM is shown in Table 18.1-1. For HP CPU0/1, the control relationship between PMP and APM is shown in Figure 18.1-1.

**Table 18.1-1. Management Areas by PMP and APM**

| Master<br>Slave                     | HP CPU0      | HP CPU1      | LP CPU | DMA Masters <sup>1</sup> |
|-------------------------------------|--------------|--------------|--------|--------------------------|
| HP ROM <sup>2</sup>                 | PMP          | PMP          | HP APM | DMA APM                  |
| HP SPM                              | PMP          | PMP          | N/A    | N/A                      |
| HP L2MEM <sup>2</sup>               | PMP          | PMP          | HP APM | DMA APM                  |
| EXT MEM <sup>2</sup>                | PMP          | PMP          | HP APM | DMA APM                  |
| Direct Access HP ROM <sup>3</sup>   | PMP + HP APM | PMP + HP APM | N/A    | N/A                      |
| Direct Access HP L2MEM <sup>3</sup> | PMP + HP APM | PMP + HP APM | N/A    | N/A                      |
| Direct Access EXT MEM <sup>3</sup>  | PMP + HP APM | PMP + HP APM | N/A    | N/A                      |
| HP CPU PERI <sup>4</sup>            | PMP + HP APM | PMP + HP APM | HP APM | N/A                      |
| HP PERI <sup>5</sup>                | PMP + HP APM | PMP + HP APM | HP APM | N/A                      |
| LP PERI <sup>6</sup>                | PMP + LP APM | PMP + LP APM | LP APM | N/A                      |
| LP ROM                              | N/A          | N/A          | N/A    | N/A                      |
| LP SRAM                             | PMP + LP APM | PMP + LP APM | N/A    | N/A                      |



- <sup>1</sup> DMA masters that support DMA transfers, such as VDMA, USB 2.0 OTG, MEM\_MONITOR, etc.
- <sup>2</sup>
- HP ROM (0x4FC0\_0000 - 0x4FC1\_FFFF)
  - HP L2MEM (0x4FF0\_0000 - 0x4FFB\_FFFF)
  - EXT MEM, including external flash (0x4000\_0000 - 0x43FF\_FFFF) and external RAM (0x4800\_0000 - 0x4BFF\_FFFF)
- <sup>3</sup> “Direct access” means HP CPU0/1 accesses internal and external memory mapped into the following address spaces without going through the cache:
- HP ROM (0x8FC0\_0000 - 0x8FC1\_FFFF)
  - HP L2MEM (0x8FF0\_0000 - 0x8FFB\_FFFF)
  - EXT MEM, including external flash (0x8000\_0000 - 0x83FF\_FFFF) and external RAM (0x8800\_0000 - 0x8BFF\_FFFF)
- <sup>4</sup> HP CPU peripheral registers (0x3FF0\_0000 - 0x3FF1\_FFFF)
- <sup>5</sup> HP system peripheral registers (0x5000\_0000 - 0x500F\_FFFF)
- <sup>6</sup> LP system peripheral registers (0x5011\_0000 - 0x5012\_FFFF)
- <sup>7</sup> As can be seen from the table, APM includes HP APM, LP APM, and DMA APM, which will be described in the following sections.



**Figure 18.1-1. PMP-APM Management Relation**

The diagram illustrates that when the HP CPUs access HP ROM, HP SPM, HP L2MEM, and EXT MEM, the access paths are solely managed by PMP. On the other hand, when the HP CPUs access the peripheral registers, HP ROM, HP L2MEM, and EXT MEM without going through the cache, the access paths are controlled by both PMP and APM. If the PMP check fails, the APM permission control will not be triggered.

PMP-related registers are located inside the HP CPUs and can be read or configured with special instructions. For how to configure PMP, please refer to Chapter 1 [High-Performance CPU \[to be added later\]](#) > 1.2 [Physical Memory Protection \[to be added later\]](#).

The following sections will provide a detailed introduction to the features, functions, and configurations of the APM module. When referring to HP CPU0/1, accessing HP ROM/HP L2MEM/EXT MEM always means direct access to HP ROM/HP L2MEM/EXT MEM.

## 18.2 Features

The APM module has the following features:

- Up to 32 configurable address ranges for each DMA master
- Access permission management for each CPU core to access internal memory, external memory, and peripheral registers
- Support for interrupts
- Support for exception information record

## 18.3 Functional Description

### 18.3.1 Architecture

The APM module contains three parts and five register modules as follows:

- **DMA APM**, containing register group [HP\\_DMA\\_PMS\\_REG](#), responsible for:
  - configuring up to 32 address regions for DMA masters
  - managing the access permission to each address region for each DMA master
- **HP APM**, containing register groups [HP\\_PERI\\_PMS\\_REG](#) and [LP2HP\\_PERI\\_PMS\\_REG](#), responsible for managing the access permissions to peripheral registers (HP CPU PERI, HP PERI), internal memory (HP ROM, HP L2MEM), and external memory (EXT MEM) in the HP system, specifically,
  - managing the access permissions for HP CPU0/1 in user mode to access all the above-mentioned slaves
  - managing the access permissions for HP CPU0/1 in machine mode to access all the above-mentioned slaves
  - managing the access permissions for LP CPU in machine mode to access all the above-mentioned slaves
- **LP APM**, containing register groups [LP\\_PERI\\_PMS\\_REG](#) and [HP2LP\\_PERI\\_PMS\\_REG](#), responsible for managing the access permissions to peripheral registers (LP PERI) and internal memory (LP SRAM) in the LP system, specifically,
  - managing the access permissions for HP CPU0/1 in user mode to access LP PERI and LP SRAM
  - managing the access permissions for HP CPU0/1 in machine mode to access LP PERI and LP SRAM
  - managing the access permissions for LP CPU in machine mode to access LP PERI

Figure [18.3-1](#) shows the access paths managed by APM and the corresponding register groups.

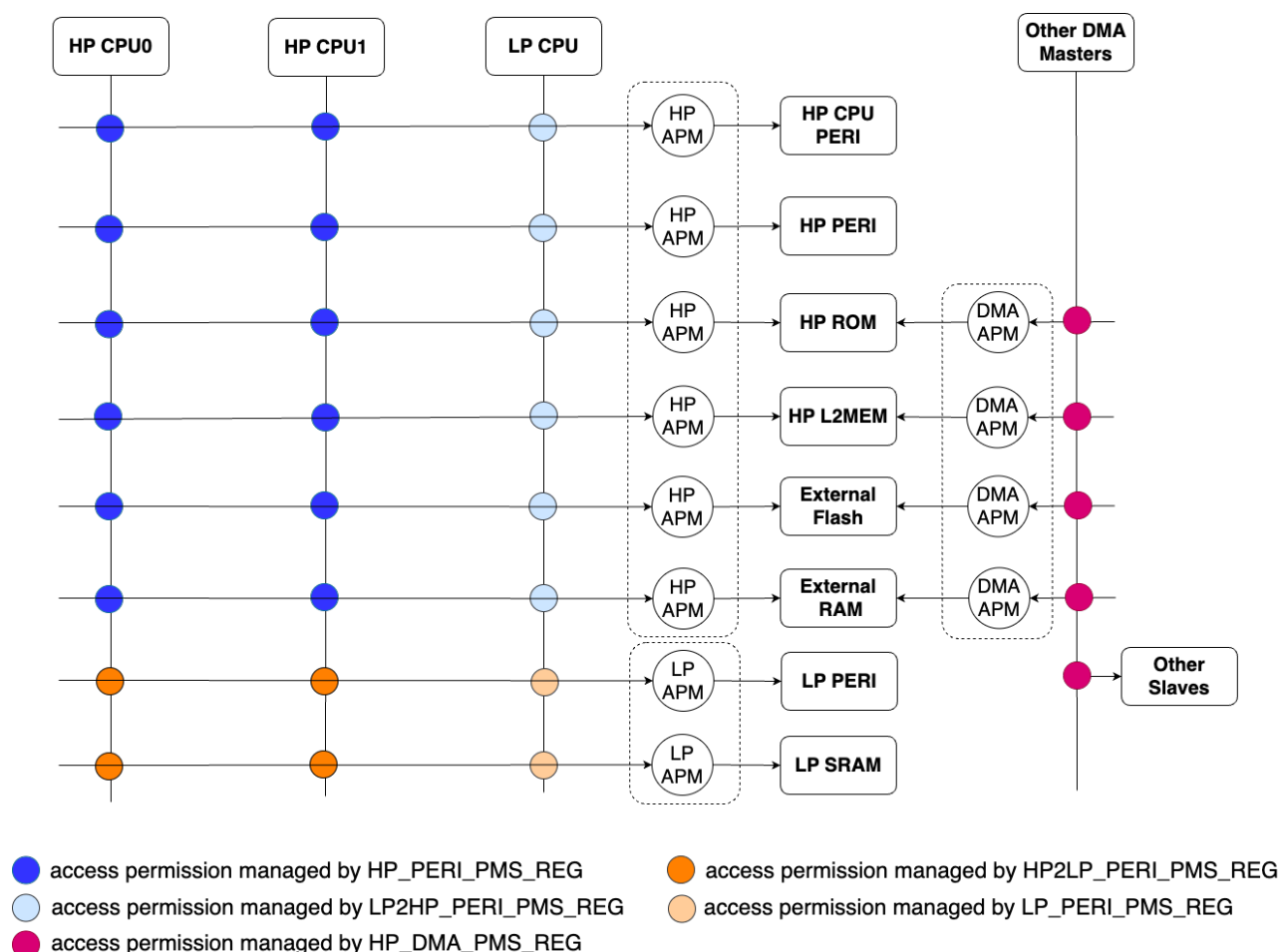


Figure 18.3-1. APM Architecture

**Note:**

- For register group names “HP2LP” and “LP2HP”, the “HP” refers to HP CPU0/1, and “LP” refers to LP CPU.
- From Table 18.1-1, it can be seen that HP CPU and LP CPU access different address spaces of HP ROM, HP L2MEM, external flash, and external RAM. For HP CPU0/1, HP APM manages their direct access to internal and external memory without going through the cache.
- LP\_PERI\_PMS\_REG includes two additional configurable address ranges for HP APM and LP APM to manage the access permissions to peripheral registers, including HP CPU PERI, HP PERI, and LP PERI.

## 18.3.2 Address Ranges and Permissions Management

APM manages address ranges, which can be fixed or configurable. DMA APM can manage up to 32 configurable address ranges. In addition to the fixed address ranges, HP APM and LP APM can also manage in total two configurable address ranges.

### 18.3.2.1 Address Ranges Managed by HP APM and LP APM

In the access paths controlled by HP APM and LP APM, the internal memory and external memory use fixed address ranges for access control, while peripheral registers not only support fixed address ranges permission control but also support two configurable address ranges.

- Fixed address ranges
  - The fixed address ranges are the valid address spaces of peripheral registers, internal memory, and external memory. See the table notes under Table 18.1-1 for the address ranges of internal and external memory. Refer to Chapter 6 *System and Memory* > Table 6.3-2 for the address ranges of each peripheral.
  - To manage access to the fixed address ranges, please refer to Figure 18.3-1 for the access paths and their corresponding register groups.
- Configurable Address Range
  - APM can configure two address ranges with `PMS_PERI_REGION $n$ _LOW_REG` and `PMS_PERI_REGION $n$ _HIGH_REG` ( $n = 0 \sim 1$ ) in `LP_PERI_PMS_REG`. These two configurable address ranges can be used by HP CPUs and LP CPU to access all on-chip peripheral registers (HP CPU PERI, HP PERI, LP PERI).
  - The access permissions are managed by `PMS_PERI_REGION_PMS_REG` in `LP_PERI_PMS_REG`.

When managing access permissions to peripheral registers, the permission management for the configurable address range should precede that of the fixed address range. Specifically:

- If the access address is within the configurable address range, then APM will check if this access is permitted to access the configurable address range.
  - If permitted, APM will continue to check if the access is permitted to the fixed address range.
  - If not permitted, the access will be denied and skip the permission check to the fixed address range.
- If the access address is outside the configurable address range, then it will skip the configurable address range check, but will continue to the fixed address range check.
- The management of configurable address ranges is a supplement to the management of fixed address ranges. For example, users can configure access permissions for a fixed address range, and deny access to two configurable ranges within the fixed range, resulting in a fixed address range containing two access-disabled address ranges.

### 18.3.2.2 Address Ranges Managed by DMA APM

The register group `HP_DMA_PMS_REG` provides 32 sets of registers (`PMS_DMA_REGION $n$ _LOW_REG` ~ `PMS_DMA_REGION $n$ _HIGH_REG`,  $n = 0 \sim 31$ ) to configure address ranges for DMA masters to access. Note that since the address must be aligned to 4K bytes, the lowest 12 bits are set to 0.

`HP_DMA_PMS_REG` provides separate read and write permissions for each DMA master to access each address range.

## 18.4 Programming Procedure

As HP CPUs can work in either user mode or machine mode, HP APM and LP APM grant specific access permissions for each work mode. Therefore, users need to configure the work mode for HP CPUs first in order for the HP CPUs to access internal memory, external memory, and peripheral registers.

Since LP CPU only supports machine mode, HP APM and LP APM grant access permissions for the machine mode of LP CPU.

DMA masters can access slaves regardless of the CPUs' work mode. DMA APM provides separate read and write permissions for each DMA master.

### 18.4.1 Configuring Access Permissions for HP CPU0/1

The configuration process for HP CPU0/1 accessing internal memory, external memory, or peripheral registers is as follows:

1. Configure user mode or machine mode for HP CPU0/1. For how to configure the work mode, please refer to RISC-V Instruction Set Manual, Volume II: Privileged Architecture, Version 1.10.
2. If accessing peripheral registers, two additional address ranges can be configured, please refer to Section 18.3.2 for details.
3. Configure access permissions:
  - Configure the access permissions to internal memory (HP L2MEM and HP ROM), external memory (External RAM and flash), and peripheral registers (HP PERI and HP CPU PERI) in the HP system through `HP_PERI_PMS_REG`:
    - Configure the permission of HP CPU $n$  accessing the `MODULE_NAME` module in `MODE_NAME` mode using `PMS_CORE $n$ _MODE_NAME_MODULE_NAME_ALLOW`, for example `PMS_CORE $n$ _MM_PSRAM_ALLOW`.
  - Configure the access permissions to LP SRAM and LP PERI through `HP2LP_PERI_PMS_REG`:
    - Configure the permission of HP CPU $n$  accessing the `MODULE_NAME` module in `MODE_NAME` mode using `PMS_HP_CORE $n$ _MODE_NAME_MODULE_NAME_ALLOW`, for example `PMS_HP_CORE $n$ _MM_LP_SYSREG_ALLOW`.

### 18.4.2 Configuring Access Permissions for LP CPU

LP CPU only supports machine mode. The configuration process for LP CPU accessing internal memory, external memory, or peripheral registers is as follows:

1. If accessing peripheral registers, two additional address ranges can be configured, please refer to Section 18.3.2 for details.
2. Configure access permissions:
  - Configure the access permissions to internal memory (HP L2MEM and HP ROM), external memory (External RAM and flash), and peripheral registers (HP PERI and HP CPU PERI) in the HP system through `LP2HP_PERI_PMS_REG`:
    - Configure the permission of LP CPU accessing the `MODULE_NAME` module in machine mode using `PMS_LP_MM_MODULE_NAME_ALLOW`, for example `PMS_LP_MM_PSRAM_ALLOW`.
  - Configure the access permissions to peripheral registers (LP PERI) in the LP system through `LP_PERI_PMS_REG`:
    - Configure the permission of LP CPU accessing the `MODULE_NAME` module in machine mode using `PMS_LP_MM_MODULE_NAME_ALLOW`, for example `PMS_LP_MM_LP_SYSREG_ALLOW`.

### 18.4.3 Configuring Access Permission for DMA Masters

The configuration process for DMA masters accessing internal memory, external memory, and other address spaces is as follows:

1. Configure the address ranges accessible to all DMA masters:
  - Configure the high 20 bits of the starting address of region *n* using `PMS_DMA_REGIONn_LOW_REG`.
  - Configure the high 20 bits of the ending address of region *n* using `PMS_DMA_REGIONn_HIGH_REG`.
2. Configure the read and write permissions for each DMA master (*DMA\_MASTER*) to access each address range:
  - Configure the read permissions using `PMS_DMA_MASTER_PMS_R_REG`, such as `PMS_DMA_GMAC_PMS_R_REG`.
  - Configure the write permissions using `PMS_DMA_MASTER_PMS_W_REG`, such as `PMS_DMA_GMAC_PMS_W_REG`.

## 18.5 Illegal Access and Interrupts

When the APM module manages access paths, it parses the information carried on the bus (e.g., master ID, access direction (read or write), access address, and working mode) and then determines the access permission. When the APM module confirms that the access lacks permission, ESP32-P4 will consider it as an unauthorized access and will take the following actions:

- Reject the access request and provide an error response.
- HP APM will trigger `ICM_SYS_REG_INT` interrupt signal.
- DMA APM will trigger `ICM_SYS_REG_INT` interrupt signal.
- LP APM will trigger `LP_SYSREG_INT` interrupt signal.

These interrupt signals are generated by the internal interrupt sources of the APM module. Table 18.5-1 lists the internal interrupt sources, interrupt trigger conditions, and the generated interrupt signals.

**Table 18.5-1. APM Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition   | Interrupt Signal |
|---------------------------|---|------------------|
| ICM_CPU_ADDRHOLE_INTR     | Triggered when HP APM detects unauthorized access; or when DMA APM detects unauthorized access from high-speed USB 2.0 OTG, full-speed USB 2.0 OTG, EMAC, SDMMC, Trace0/1, GDMA-AHB, L2MEM Monitor, or SPM Monitor. | ICM_SYS_REG_INT  |
| ICM_SYS_ADDRHOLE_INTR     | Triggered when DMA APM detects unauthorized access from VDMA, GDMA-AXI, 2D-DMA, or H264 DMA.  | ICM_SYS_REG_INT  |
| LP_ADDRHOLE_INTR          | Triggered when LP APM detects unauthorized access.  | LP_SYSREG_INTR   |

APM automatically records relevant information about illegal accesses, including master ID, access direction (read or write), access address, illegal access flags, etc. All this information can be retrieved from the relevant registers described in Chapter 3 *System Registers [to be added later]*.

## 18.6 Register Summary

### 18.6.1 HP\_DMA\_PMS\_REG

The addresses in this section are relative to the HP\_DMA\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                     | Description                                  | Address | Access |
|--|--|---------|--------|
| <b>Version Control Registers</b>         |  |         |        |
| <a href="#">PMS_DMA_DATE_REG</a>         | Version control register                     | 0x0000  | R/W    |
| <b>Clock Gating Registers</b>            |  |         |        |
| <a href="#">PMS_DMA_CLK_EN_REG</a>       | Clock gating register                        | 0x0004  | R/W    |
| <b>Region Configuration Registers</b>    |  |         |        |
| <a href="#">PMS_DMA_REGION0_LOW_REG</a>  | Region0 start address configuration register | 0x0008  | R/W    |
| <a href="#">PMS_DMA_REGION0_HIGH_REG</a> | Region0 end address configuration register   | 0x000C  | R/W    |
| <a href="#">PMS_DMA_REGION1_LOW_REG</a>  | Region1 start address configuration register | 0x0010  | R/W    |
| <a href="#">PMS_DMA_REGION1_HIGH_REG</a> | Region1 end address configuration register   | 0x0014  | R/W    |
| <a href="#">PMS_DMA_REGION2_LOW_REG</a>  | Region2 start address configuration register | 0x0018  | R/W    |
| <a href="#">PMS_DMA_REGION2_HIGH_REG</a> | Region2 end address configuration register   | 0x001C  | R/W    |
| <a href="#">PMS_DMA_REGION3_LOW_REG</a>  | Region3 start address configuration register | 0x0020  | R/W    |
| <a href="#">PMS_DMA_REGION3_HIGH_REG</a> | Region3 end address configuration register   | 0x0024  | R/W    |
| <a href="#">PMS_DMA_REGION4_LOW_REG</a>  | Region4 start address configuration register | 0x0028  | R/W    |
| <a href="#">PMS_DMA_REGION4_HIGH_REG</a> | Region4 end address configuration register   | 0x002C  | R/W    |
| <a href="#">PMS_DMA_REGION5_LOW_REG</a>  | Region5 start address configuration register | 0x0030  | R/W    |
| <a href="#">PMS_DMA_REGION5_HIGH_REG</a> | Region5 end address configuration register   | 0x0034  | R/W    |
| <a href="#">PMS_DMA_REGION6_LOW_REG</a>  | Region6 start address configuration register | 0x0038  | R/W    |
| <a href="#">PMS_DMA_REGION6_HIGH_REG</a> | Region6 end address configuration register   | 0x003C  | R/W    |
| <a href="#">PMS_DMA_REGION7_LOW_REG</a>  | Region7 start address configuration register | 0x0040  | R/W    |

| Name                                      | Description                                   | Address | Access |
|---|---|---------|--------|
| <a href="#">PMS_DMA_REGION7_HIGH_REG</a>  | Region7 end address configuration register    | 0x0044  | R/W    |
| <a href="#">PMS_DMA_REGION8_LOW_REG</a>   | Region8 start address configuration register  | 0x0048  | R/W    |
| <a href="#">PMS_DMA_REGION8_HIGH_REG</a>  | Region8 end address configuration register    | 0x004C  | R/W    |
| <a href="#">PMS_DMA_REGION9_LOW_REG</a>   | Region9 start address configuration register  | 0x0050  | R/W    |
| <a href="#">PMS_DMA_REGION9_HIGH_REG</a>  | Region9 end address configuration register    | 0x0054  | R/W    |
| <a href="#">PMS_DMA_REGION10_LOW_REG</a>  | Region10 start address configuration register | 0x0058  | R/W    |
| <a href="#">PMS_DMA_REGION10_HIGH_REG</a> | Region10 end address configuration register   | 0x005C  | R/W    |
| <a href="#">PMS_DMA_REGION11_LOW_REG</a>  | Region11 start address configuration register | 0x0060  | R/W    |
| <a href="#">PMS_DMA_REGION11_HIGH_REG</a> | Region11 end address configuration register   | 0x0064  | R/W    |
| <a href="#">PMS_DMA_REGION12_LOW_REG</a>  | Region12 start address configuration register | 0x0068  | R/W    |
| <a href="#">PMS_DMA_REGION12_HIGH_REG</a> | Region12 end address configuration register   | 0x006C  | R/W    |
| <a href="#">PMS_DMA_REGION13_LOW_REG</a>  | Region13 start address configuration register | 0x0070  | R/W    |
| <a href="#">PMS_DMA_REGION13_HIGH_REG</a> | Region13 end address configuration register   | 0x0074  | R/W    |
| <a href="#">PMS_DMA_REGION14_LOW_REG</a>  | Region14 start address configuration register | 0x0078  | R/W    |
| <a href="#">PMS_DMA_REGION14_HIGH_REG</a> | Region14 end address configuration register   | 0x007C  | R/W    |
| <a href="#">PMS_DMA_REGION15_LOW_REG</a>  | Region15 start address configuration register | 0x0080  | R/W    |
| <a href="#">PMS_DMA_REGION15_HIGH_REG</a> | Region15 end address configuration register   | 0x0084  | R/W    |
| <a href="#">PMS_DMA_REGION16_LOW_REG</a>  | Region16 start address configuration register | 0x0088  | R/W    |
| <a href="#">PMS_DMA_REGION16_HIGH_REG</a> | Region16 end address configuration register   | 0x008C  | R/W    |
| <a href="#">PMS_DMA_REGION17_LOW_REG</a>  | Region17 start address configuration register | 0x0090  | R/W    |
| <a href="#">PMS_DMA_REGION17_HIGH_REG</a> | Region17 end address configuration register   | 0x0094  | R/W    |
| <a href="#">PMS_DMA_REGION18_LOW_REG</a>  | Region18 start address configuration register | 0x0098  | R/W    |



| Name                                      | Description                                   | Address | Access |
|---|---|---------|--------|
| <a href="#">PMS_DMA_REGION18_HIGH_REG</a> | Region18 end address configuration register   | 0x009C  | R/W    |
| <a href="#">PMS_DMA_REGION19_LOW_REG</a>  | Region19 start address configuration register | 0x00A0  | R/W    |
| <a href="#">PMS_DMA_REGION19_HIGH_REG</a> | Region19 end address configuration register   | 0x00A4  | R/W    |
| <a href="#">PMS_DMA_REGION20_LOW_REG</a>  | Region20 start address configuration register | 0x00A8  | R/W    |
| <a href="#">PMS_DMA_REGION20_HIGH_REG</a> | Region20 end address configuration register   | 0x00AC  | R/W    |
| <a href="#">PMS_DMA_REGION21_LOW_REG</a>  | Region21 start address configuration register | 0x00B0  | R/W    |
| <a href="#">PMS_DMA_REGION21_HIGH_REG</a> | Region21 end address configuration register   | 0x00B4  | R/W    |
| <a href="#">PMS_DMA_REGION22_LOW_REG</a>  | Region22 start address configuration register | 0x00B8  | R/W    |
| <a href="#">PMS_DMA_REGION22_HIGH_REG</a> | Region22 end address configuration register   | 0x00BC  | R/W    |
| <a href="#">PMS_DMA_REGION23_LOW_REG</a>  | Region23 start address configuration register | 0x00C0  | R/W    |
| <a href="#">PMS_DMA_REGION23_HIGH_REG</a> | Region23 end address configuration register   | 0x00C4  | R/W    |
| <a href="#">PMS_DMA_REGION24_LOW_REG</a>  | Region24 start address configuration register | 0x00C8  | R/W    |
| <a href="#">PMS_DMA_REGION24_HIGH_REG</a> | Region24 end address configuration register   | 0x00CC  | R/W    |
| <a href="#">PMS_DMA_REGION25_LOW_REG</a>  | Region25 start address configuration register | 0x00D0  | R/W    |
| <a href="#">PMS_DMA_REGION25_HIGH_REG</a> | Region25 end address configuration register   | 0x00D4  | R/W    |
| <a href="#">PMS_DMA_REGION26_LOW_REG</a>  | Region26 start address configuration register | 0x00D8  | R/W    |
| <a href="#">PMS_DMA_REGION26_HIGH_REG</a> | Region26 end address configuration register   | 0x00DC  | R/W    |
| <a href="#">PMS_DMA_REGION27_LOW_REG</a>  | Region27 start address configuration register | 0x00E0  | R/W    |
| <a href="#">PMS_DMA_REGION27_HIGH_REG</a> | Region27 end address configuration register   | 0x00E4  | R/W    |
| <a href="#">PMS_DMA_REGION28_LOW_REG</a>  | Region28 start address configuration register | 0x00E8  | R/W    |
| <a href="#">PMS_DMA_REGION28_HIGH_REG</a> | Region28 end address configuration register   | 0x00EC  | R/W    |
| <a href="#">PMS_DMA_REGION29_LOW_REG</a>  | Region29 start address configuration register | 0x00F0  | R/W    |

| Name   | Description                                     | Address | Access |
|--|---|---------|--------|
| <a href="#">PMS_DMA_REGION29_HIGH_REG</a>                      | Region29 end address configuration register     | 0x00F4  | R/W    |
| <a href="#">PMS_DMA_REGION30_LOW_REG</a>                       | Region30 start address configuration register   | 0x00F8  | R/W    |
| <a href="#">PMS_DMA_REGION30_HIGH_REG</a>                      | Region30 end address configuration register     | 0x00FC  | R/W    |
| <a href="#">PMS_DMA_REGION31_LOW_REG</a>                       | Region31 start address configuration register   | 0x0100  | R/W    |
| <a href="#">PMS_DMA_REGION31_HIGH_REG</a>                      | Region31 end address configuration register     | 0x0104  | R/W    |
| <b>DMA Masters Read and Write Permission Control Registers</b> |   |         |        |
| <a href="#">PMS_DMA_GDMA_CH0_R_PMS_REG</a>                     | GDMA ch0 read permission control register       | 0x0108  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH0_W_PMS_REG</a>                     | GDMA ch0 write permission control register      | 0x010C  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH1_R_PMS_REG</a>                     | GDMA ch1 read permission control register       | 0x0110  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH1_W_PMS_REG</a>                     | GDMA ch1 write permission control register      | 0x0114  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH2_R_PMS_REG</a>                     | GDMA ch2 read permission control register       | 0x0118  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH2_W_PMS_REG</a>                     | GDMA ch2 write permission control register      | 0x011C  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH3_R_PMS_REG</a>                     | GDMA ch3 read permission control register       | 0x0120  | R/W    |
| <a href="#">PMS_DMA_GDMA_CH3_W_PMS_REG</a>                     | GDMA ch3 write permission control register      | 0x0124  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_ADC_R_PMS_REG</a>                 | GDMA-AHB ADC read permission control register   | 0x0128  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_ADC_W_PMS_REG</a>                 | GDMA-AHB ADC write permission control register  | 0x012C  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S0_R_PMS_REG</a>                | GDMA-AHB I2S0 read permission control register  | 0x0130  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S0_W_PMS_REG</a>                | GDMA-AHB I2S0 write permission control register | 0x0134  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S1_R_PMS_REG</a>                | GDMA-AHB I2S1 read permission control register  | 0x0138  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S1_W_PMS_REG</a>                | GDMA-AHB I2S1 write permission control register | 0x013C  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S2_R_PMS_REG</a>                | GDMA-AHB I2S2 read permission control register  | 0x0140  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I2S2_W_PMS_REG</a>                | GDMA-AHB I2S2 write permission control register | 0x0144  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">PMS_DMA_AHB_PDMA_I3C_MST_R_PMS_REG</a> | GDMA-AHB I3C MST read permission control register        | 0x0148  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_I3C_MST_W_PMS_REG</a> | GDMA-AHB I3C MST write permission control register       | 0x014C  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_UHCIO_R_PMS_REG</a>   | GDMA-AHB UHCI read permission control register           | 0x0150  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_UHCIO_W_PMS_REG</a>   | GDMA-AHB UHCI write permission control register          | 0x0154  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_RMT_R_PMS_REG</a>     | GDMA-AHB RMT read permission control register            | 0x0158  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_RMT_W_PMS_REG</a>     | GDMA-AHB RMT write permission control register           | 0x0170  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_LCDCAM_R_PMS_REG</a>  | GDMA-AXI LCD_CAM read permission control register        | 0x0174  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_LCDCAM_W_PMS_REG</a>  | GDMA-AXI LCD_CAM write permission control register       | 0x0178  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_GPSPI2_R_PMS_REG</a>  | GDMA-AXI GPSPI2 read permission control register         | 0x017C  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_GPSPI2_W_PMS_REG</a>  | GDMA-AXI GPSPI2 write permission control register        | 0x0180  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_GPSPI3_R_PMS_REG</a>  | GDMA-AXI GPSPI3 read permission control register         | 0x0184  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_GPSPI3_W_PMS_REG</a>  | GDMA-AXI GPSPI3 write permission control register        | 0x0188  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_PARLIO_R_PMS_REG</a>  | GDMA-AXI PARLIO read permission control register         | 0x018C  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_PARLIO_W_PMS_REG</a>  | GDMA-AXI PARLIO write permission control register        | 0x0190  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_AES_R_PMS_REG</a>     | GDMA-AXI AES read permission control register            | 0x0194  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_AES_W_PMS_REG</a>     | GDMA-AXI AES write permission control register           | 0x0198  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_SHA_R_PMS_REG</a>     | GDMA-AXI SHA read permission control register            | 0x019C  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_SHA_W_PMS_REG</a>     | GDMA-AXI SHA write permission control register           | 0x01A0  | R/W    |
| <a href="#">PMS_DMA_DMA2D_JPEG_PMS_R_REG</a>       | 2D-DMA JPEG read permission control register             | 0x01A4  | R/W    |
| <a href="#">PMS_DMA_DMA2D_JPEG_PMS_W_REG</a>       | 2D-DMA JPEG write permission control register            | 0x01A8  | R/W    |
| <a href="#">PMS_DMA_USB_PMS_R_REG</a>              | High-speed USB 2.0 OTG read permission control register  | 0x01AC  | R/W    |
| <a href="#">PMS_DMA_USB_PMS_W_REG</a>              | High-speed USB 2.0 OTG write permission control register | 0x01B0  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">PMS_DMA_GMAC_PMS_R_REG</a>           | EMAC read permission control register                    | 0x01B4  | R/W    |
| <a href="#">PMS_DMA_GMAC_PMS_W_REG</a>           | EMAC write permission control register                   | 0x01B8  | R/W    |
| <a href="#">PMS_DMA_SDMMC_PMS_R_REG</a>          | SDMMC read permission control register                   | 0x01BC  | R/W    |
| <a href="#">PMS_DMA_SDMMC_PMS_W_REG</a>          | SDMMC write permission control register                  | 0x01C0  | R/W    |
| <a href="#">PMS_DMA_USBOTG11_PMS_R_REG</a>       | Full-speed USB 2.0 OTG read permission control register  | 0x01C4  | R/W    |
| <a href="#">PMS_DMA_USBOTG11_PMS_W_REG</a>       | Full-speed USB 2.0 OTG write permission control register | 0x01C8  | R/W    |
| <a href="#">PMS_DMA_TRACE0_PMS_R_REG</a>         | TRACE0 read permission control register                  | 0x01CC  | R/W    |
| <a href="#">PMS_DMA_TRACE0_PMS_W_REG</a>         | TRACE0 write permission control register                 | 0x01D0  | R/W    |
| <a href="#">PMS_DMA_TRACE1_PMS_R_REG</a>         | TRACE1 read permission control register                  | 0x01D4  | R/W    |
| <a href="#">PMS_DMA_TRACE1_PMS_W_REG</a>         | TRACE1 write permission control register                 | 0x01D8  | R/W    |
| <a href="#">PMS_DMA_L2MEM_MON_PMS_W_REG</a>      | L2MEM Monitor write permission control register          | 0x01E0  | R/W    |
| <a href="#">PMS_DMA_SPM_MON_PMS_W_REG</a>        | SPM Monitor write permission control register            | 0x01E8  | R/W    |
| <a href="#">PMS_DMA_H264_PMS_R_REG</a>           | H264 DMA read permission control register                | 0x01FC  | R/W    |
| <a href="#">PMS_DMA_H264_PMS_W_REG</a>           | H264 DMA write permission control register               | 0x0200  | R/W    |
| <a href="#">PMS_DMA_DMA2D_PPA_PMS_R_REG</a>      | 2D-DMA PPA read permission control register              | 0x0204  | R/W    |
| <a href="#">PMS_DMA_DMA2D_PPA_PMS_W_REG</a>      | 2D-DMA PPA write permission control register             | 0x0208  | R/W    |
| <a href="#">PMS_DMA_DMA2D_DUMMY_PMS_R_REG</a>    | 2D-DMA Dummy read permission control register            | 0x020C  | R/W    |
| <a href="#">PMS_DMA_DMA2D_DUMMY_PMS_W_REG</a>    | 2D-DMA Dummy write permission control register           | 0x0210  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_DUMMY_R_PMS_REG</a> | GDMA-AHB Dummy read permission control register          | 0x0214  | R/W    |
| <a href="#">PMS_DMA_AHB_PDMA_DUMMY_W_PMS_REG</a> | GDMA-AHB Dummy write permission control register         | 0x0218  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_DUMMY_R_PMS_REG</a> | GDMA-AXI Dummy read permission control register          | 0x021C  | R/W    |
| <a href="#">PMS_DMA_AXI_PDMA_DUMMY_W_PMS_REG</a> | GDMA-AXI Dummy write permission control register         | 0x0220  | R/W    |

## 18.6.2 HP\_PERI\_PMS\_REG

The addresses in this section are relative to the HP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <b>Version Control Registers</b>                  |  |         |        |
| <a href="#">PMS_HP_PERI_PMS_DATE_REG</a>          | Version control register                                 | 0x0000  | R/W    |
| <b>Clock Gating Registers</b>                     |  |         |        |
| <a href="#">PMS_HP_PERI_PMS_CLK_EN_REG</a>        | Clock gating register                                    | 0x0004  | R/W    |
| <b>HP CPU Permission Control Registers</b>        |  |         |        |
| <a href="#">PMS_CORE0_MM_HP_PERI_PMS_REG0_REG</a> | Permission control register0 for HP CPU0 in machine mode | 0x0008  | R/W    |
| <a href="#">PMS_CORE0_MM_HP_PERI_PMS_REG1_REG</a> | Permission control register1 for HP CPU0 in machine mode | 0x000C  | R/W    |
| <a href="#">PMS_CORE0_MM_HP_PERI_PMS_REG2_REG</a> | Permission control register2 for HP CPU0 in machine mode | 0x0010  | R/W    |
| <a href="#">PMS_CORE0_MM_HP_PERI_PMS_REG3_REG</a> | Permission control register3 for HP CPU0 in machine mode | 0x0014  | R/W    |
| <a href="#">PMS_CORE0_UM_HP_PERI_PMS_REG0_REG</a> | Permission control register0 for HP CPU0 in user mode    | 0x0018  | R/W    |
| <a href="#">PMS_CORE0_UM_HP_PERI_PMS_REG1_REG</a> | Permission control register1 for HP CPU0 in user mode    | 0x001C  | R/W    |
| <a href="#">PMS_CORE0_UM_HP_PERI_PMS_REG2_REG</a> | Permission control register2 for HP CPU0 in user mode    | 0x0020  | R/W    |
| <a href="#">PMS_CORE0_UM_HP_PERI_PMS_REG3_REG</a> | Permission control register3 for HP CPU0 in user mode    | 0x0024  | R/W    |
| <a href="#">PMS_CORE1_MM_HP_PERI_PMS_REG0_REG</a> | Permission control register0 for HP CPU1 in machine mode | 0x0028  | R/W    |
| <a href="#">PMS_CORE1_MM_HP_PERI_PMS_REG1_REG</a> | Permission control register1 for HP CPU1 in machine mode | 0x002C  | R/W    |
| <a href="#">PMS_CORE1_MM_HP_PERI_PMS_REG2_REG</a> | Permission control register2 for HP CPU1 in machine mode | 0x0030  | R/W    |
| <a href="#">PMS_CORE1_MM_HP_PERI_PMS_REG3_REG</a> | Permission control register3 for HP CPU1 in machine mode | 0x0034  | R/W    |
| <a href="#">PMS_CORE1_UM_HP_PERI_PMS_REG0_REG</a> | Permission control register0 for HP CPU1 in user mode    | 0x0038  | R/W    |
| <a href="#">PMS_CORE1_UM_HP_PERI_PMS_REG1_REG</a> | Permission control register1 for HP CPU1 in user mode    | 0x003C  | R/W    |
| <a href="#">PMS_CORE1_UM_HP_PERI_PMS_REG2_REG</a> | Permission control register2 for HP CPU1 in user mode    | 0x0040  | R/W    |
| <a href="#">PMS_CORE1_UM_HP_PERI_PMS_REG3_REG</a> | Permission control register3 for HP CPU1 in user mode    | 0x0044  | R/W    |

### 18.6.3 LP2HP\_PERI\_PMS\_REG

The addresses in this section are relative to the LP2HP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Version Control Registers</b>              |   |         |        |
| <a href="#">PMS_LP2HP_PERI_PMS_DATE_REG</a>   | Version control register                                    | 0x0000  | R/W    |
| <b>Clock Gating Registers</b>                 |   |         |        |
| <a href="#">PMS_LP2HP_PERI_PMS_CLK_EN_REG</a> | Clock gating register                                       | 0x0004  | R/W    |
| <b>LP CPU Permission Control Registers</b>    |   |         |        |
| <a href="#">PMS_LP_MM_PMS_REG0_REG</a>        | Permission control register0 for the LP CPU in machine mode | 0x0008  | R/W    |
| <a href="#">PMS_LP_MM_PMS_REG1_REG</a>        | Permission control register1 for the LP CPU in machine mode | 0x0030  | R/W    |
| <a href="#">PMS_LP_MM_PMS_REG2_REG</a>        | Permission control register2 for the LP CPU in machine mode | 0x00A4  | R/W    |
| <a href="#">PMS_LP_MM_PMS_REG3_REG</a>        | Permission control register3 for the LP CPU in machine mode | 0x011C  | R/W    |

### 18.6.4 LP\_PERI\_PMS\_REG

The addresses in this section are relative to the LP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description   | Address | Access |
|---|---|---------|--------|
| <b>Version Control Registers</b>                          |   |         |        |
| <a href="#">PMS_LP_PERI_PMS_DATE_REG</a>                  | Version control register                                | 0x0000  | R/W    |
| <b>Clock Gating Registers</b>                             |   |         |        |
| <a href="#">PMS_LP_PERI_PMS_CLK_EN_REG</a>                | Clock gating register                                   | 0x0004  | R/W    |
| <b>LP CPU Permission Control Registers</b>                |   |         |        |
| <a href="#">PMS_LP_MM_LP_PERI_PMS_REG0_REG</a>            | Permission control register0 for LP CPU in machine mode | 0x0008  | R/W    |
| <b>Configurable Address Range Configuration Registers</b> |   |         |        |
| <a href="#">PMS_PERI_REGION0_LOW_REG</a>                  | Region0 start address configuration register            | 0x000C  | R/W    |
| <a href="#">PMS_PERI_REGION0_HIGH_REG</a>                 | Region0 end address configuration register              | 0x0010  | R/W    |
| <a href="#">PMS_PERI_REGION1_LOW_REG</a>                  | Region1 start address configuration register            | 0x0014  | R/W    |
| <a href="#">PMS_PERI_REGION1_HIGH_REG</a>                 | Region1 end address configuration register              | 0x0018  | R/W    |

### 18.6.5 HP2LP\_PERI\_PMS\_REG

The addresses in this section are relative to the HP2LP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <b>Version Control Registers</b>              |  |         |        |
| <a href="#">PMS_HP2LP_PERI_PMS_DATE_REG</a>   | Version control register                                 | 0x0000  | R/W    |
| <b>Clock Gating Registers</b>                 |  |         |        |
| <a href="#">PMS_HP2LP_PERI_PMS_CLK_EN_REG</a> | Clock gating register                                    | 0x0004  | R/W    |
| <b>HP CPU Permission Control Registers</b>    |  |         |        |
| <a href="#">PMS_HP_CORE0_MM_PMS_REGO_REG</a>  | Permission control register0 for HP CPU0 in machine mode | 0x0008  | R/W    |
| <a href="#">PMS_HP_CORE0_UM_PMS_REGO_REG</a>  | Permission control register0 for HP CPU0 in user mode    | 0x000C  | R/W    |
| <a href="#">PMS_HP_CORE1_MM_PMS_REGO_REG</a>  | Permission control register0 for HP CPU1 in machine mode | 0x0010  | R/W    |
| <a href="#">PMS_HP_CORE1_UM_PMS_REGO_REG</a>  | Permission control register0 for HP CPU1 in user mode    | 0x0014  | R/W    |

## 18.7 Registers

### 18.7.1 HP\_DMA\_PMS\_REG

The addresses in this section are relative to the HP\_DMA\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 18.1. PMS\_DMA\_DATE\_REG (0x0000)

|                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| PMS_DMA_DATE    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 310             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x20230314Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**PMS\_DMA\_DATE** Version control register. (R/W)

Register 18.2. PMS\_DMA\_CLK\_EN\_REG (0x0004)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PMS_DMA_CLK_EN |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1              | 0 |       |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                | 1 | Reset |

**PMS\_DMA\_CLK\_EN** Configures whether to keep the clock always on.

0: Enable automatic clock gating.

1: Keep the clock always on.

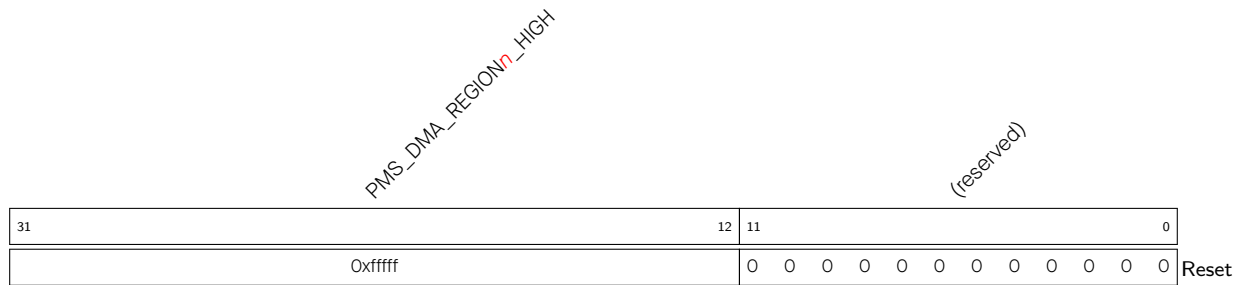
(R/W)

Register 18.3. PMS\_DMA\_REGION $n$ \_LOW\_REG ( $n$ : 0-31) (0x0008+0x8\* $n$ )

|                                  |  |  |  |  |  |  |  |  |  |  |  |                                   |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|-----------------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|---|
| PMS_DMA_REGION <sub>n</sub> _LOW |  |  |  |  |  |  |  |  |  |  |  | (reserved)                        |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
| 31                               |  |  |  |  |  |  |  |  |  |  |  | 12                                | 11 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  | 0 |
| 0x000                            |  |  |  |  |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |   |

**PMS\_DMA\_REGION $n$ \_LOW** Configures the high 20 bits of the start address for region $n$ . (R/W)



**Register 18.4. PMS\_DMA\_REGION $n$ \_HIGH\_REG ( $n$ : 0-31) (0x000C+0x8\* $n$ )**

**PMS\_DMA\_REGION $n$ \_HIGH** Configures the high 20 bits of the end address for region $n$ . (R/W)

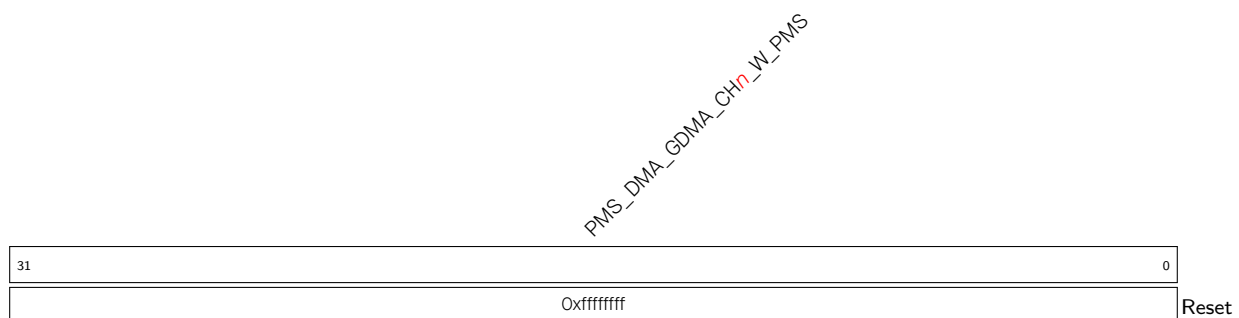
**Register 18.5. PMS\_DMA\_GDMA\_CH $n$ \_R\_PMS\_REG ( $n$ : 0-3) (0x0108+0x8\* $n$ )**

**PMS\_DMA\_GDMA\_CH $n$ \_R\_PMS** Configures the permission for GDMA ch $n$  to read 32 address regions. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

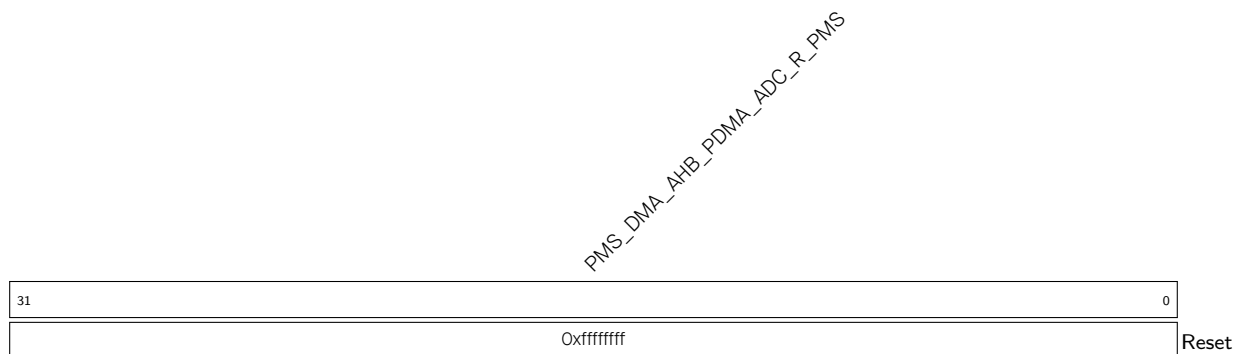
**Register 18.6. PMS\_DMA\_GDMA\_CH $n$ \_W\_PMS\_REG ( $n$ : 0-3) (0x010C+0x8\* $n$ )**

**PMS\_DMA\_GDMA\_CH $n$ \_W\_PMS** Configures the permission for GDMA ch $n$  to write 32 address regions. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

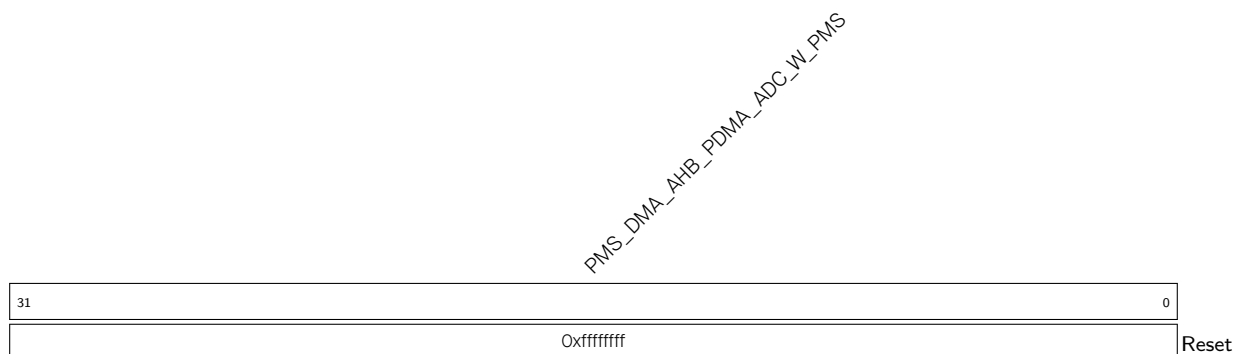
**Register 18.7. PMS\_DMA\_AHB\_PDMA\_ADC\_R\_PMS\_REG (0x0128)**

**PMS\_DMA\_AHB\_PDMA\_ADC\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by ADC. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.8. PMS\_DMA\_AHB\_PDMA\_ADC\_W\_PMS\_REG (0x012C)**

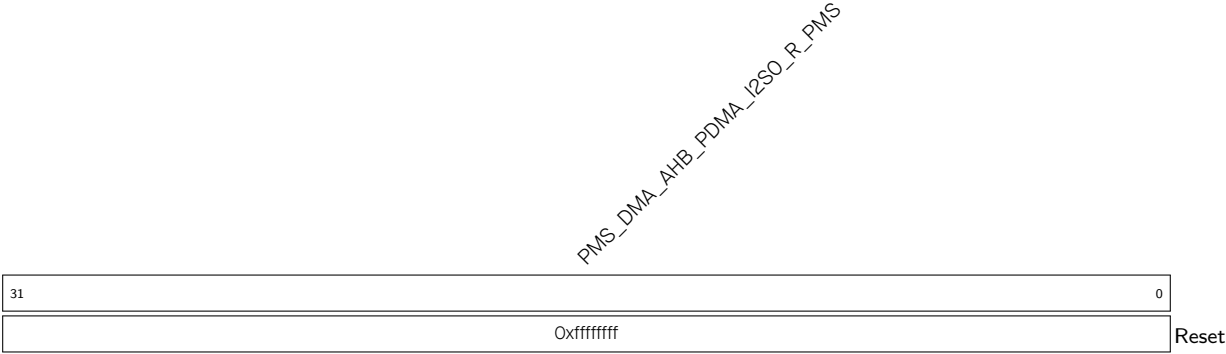
**PMS\_DMA\_AHB\_PDMA\_ADC\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by ADC. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.9. PMS\_DMA\_AHB\_PDMA\_I2SO\_R\_PMS\_REG (0x0130)



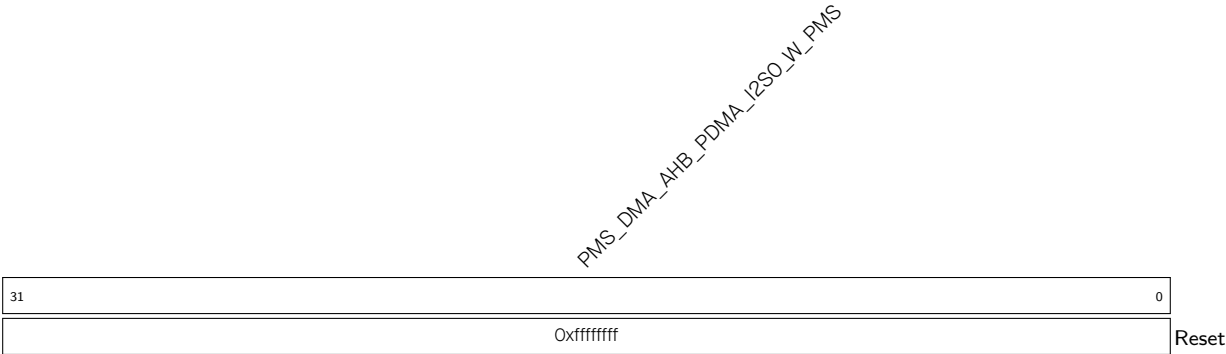
**PMS\_DMA\_AHB\_PDMA\_I2SO\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by I2SO. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

Register 18.10. PMS\_DMA\_AHB\_PDMA\_I2SO\_W\_PMS\_REG (0x0134)



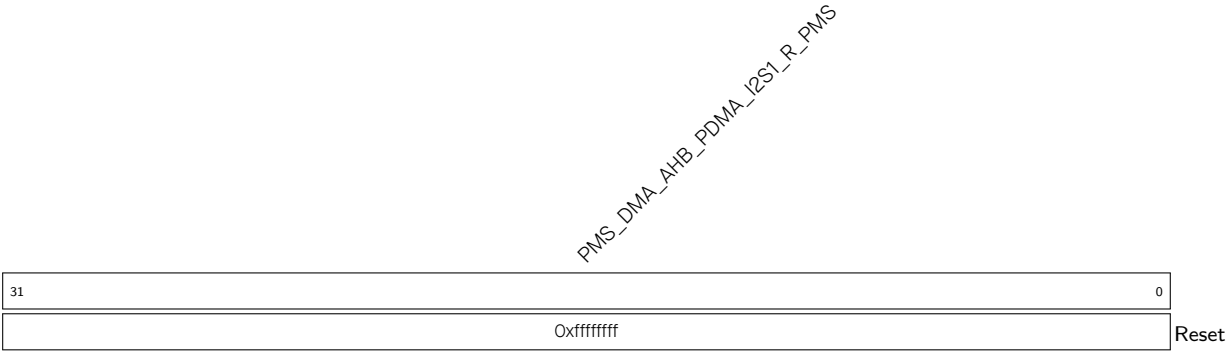
**PMS\_DMA\_AHB\_PDMA\_I2SO\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by I2SO. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.11. PMS\_DMA\_AHB\_PDMA\_I2S1\_R\_PMS\_REG (0x0138)

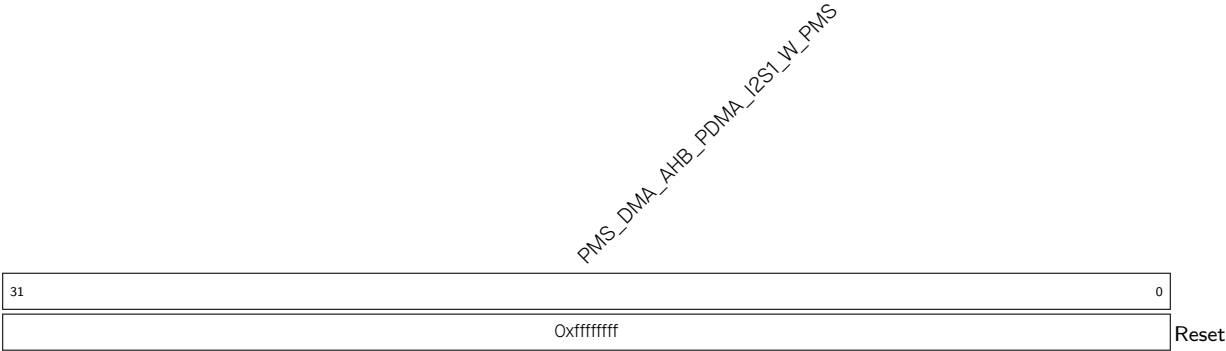


**PMS\_DMA\_AHB\_PDMA\_I2S1\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by I2S1. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.12. PMS\_DMA\_AHB\_PDMA\_I2S1\_W\_PMS\_REG (0x013C)

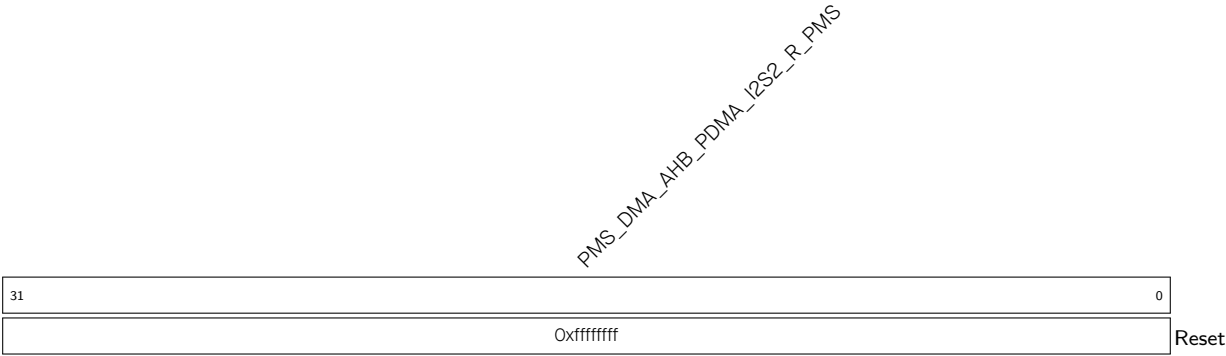


**PMS\_DMA\_AHB\_PDMA\_I2S1\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by I2S1. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.13. PMS\_DMA\_AHB\_PDMA\_I2S2\_R\_PMS\_REG (0x0140)

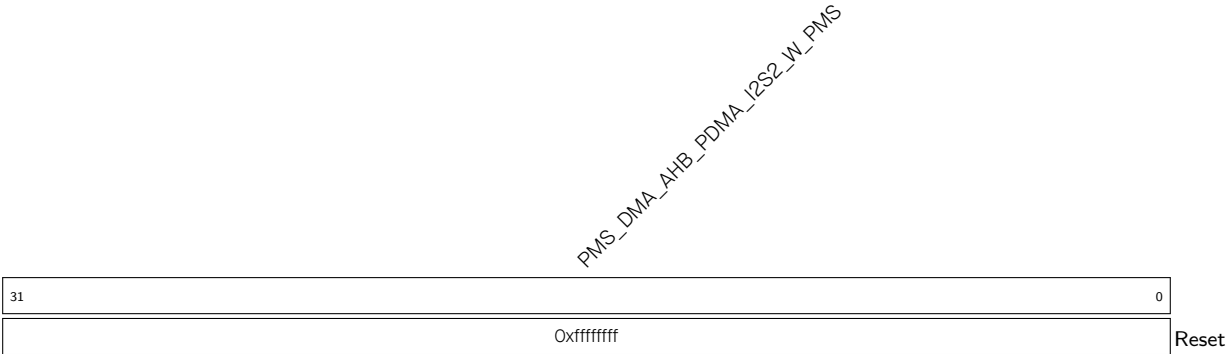


**PMS\_DMA\_AHB\_PDMA\_I2S2\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by I2S2. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

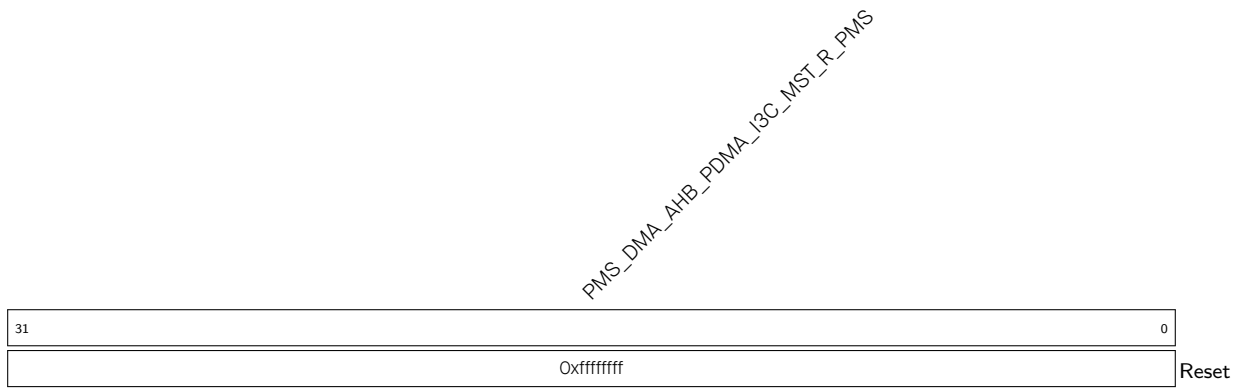
Register 18.14. PMS\_DMA\_AHB\_PDMA\_I2S2\_W\_PMS\_REG (0x0144)



**PMS\_DMA\_AHB\_PDMA\_I2S2\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by I2S2. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

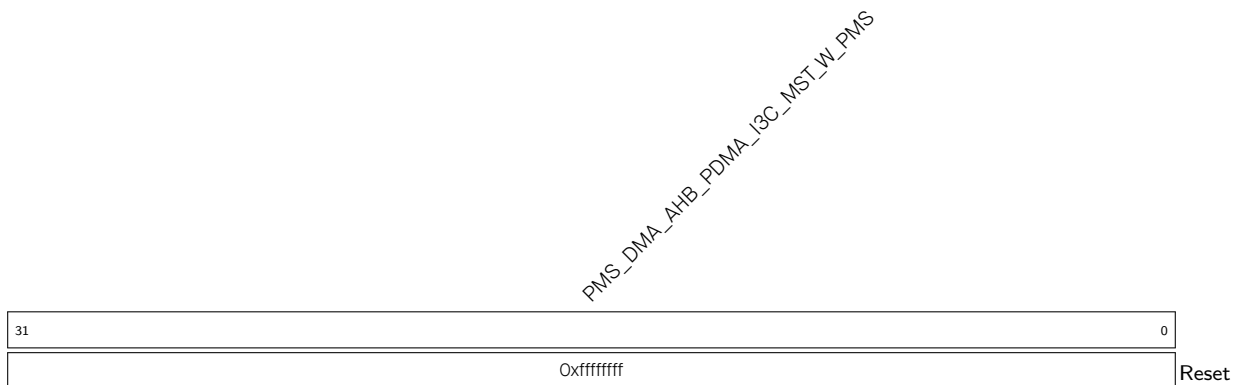
**Register 18.15. PMS\_DMA\_AHB\_PDMA\_I3C\_MST\_R\_PMS\_REG (0x0148)**

**PMS\_DMA\_AHB\_PDMA\_I3C\_MST\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by I3C master. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.16. PMS\_DMA\_AHB\_PDMA\_I3C\_MST\_W\_PMS\_REG (0x014C)**

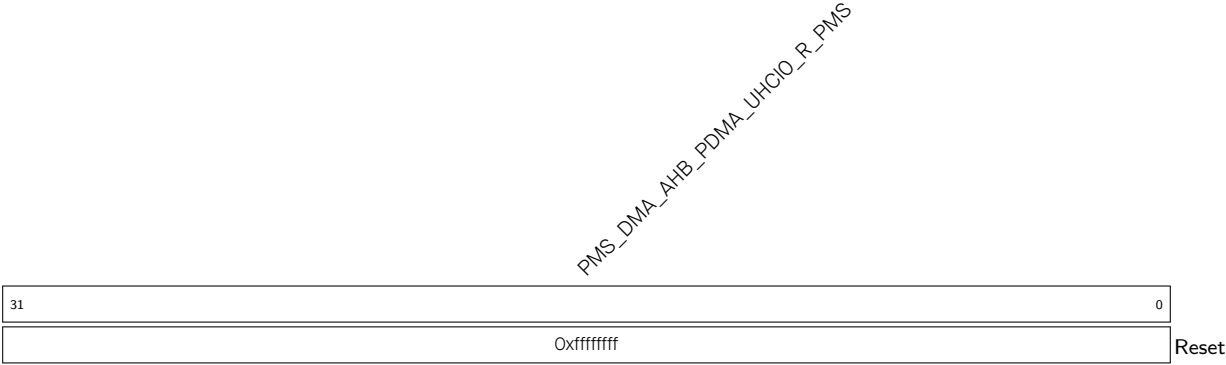
**PMS\_DMA\_AHB\_PDMA\_I3C\_MST\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by I3C master. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.17. PMS\_DMA\_AHB\_PDMA\_UHCIO\_R\_PMS\_REG (0x0150)

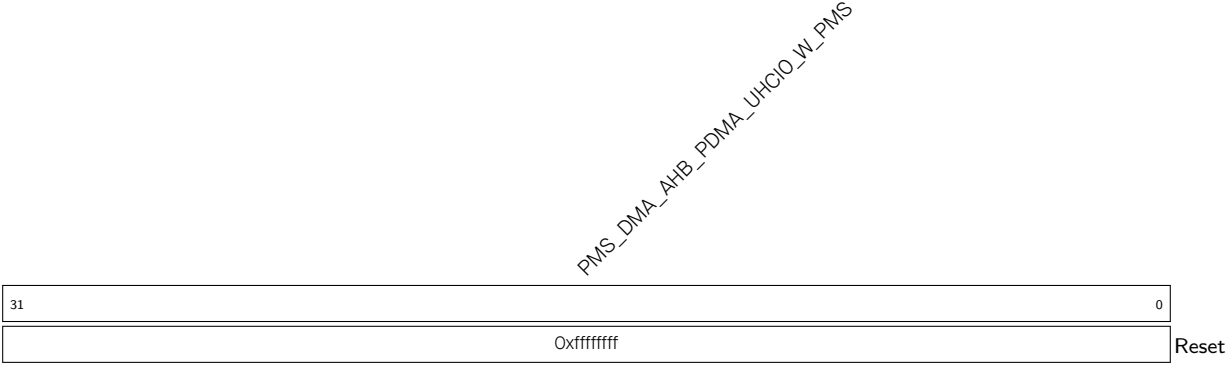


**PMS\_DMA\_AHB\_PDMA\_UHCIO\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by UHCI. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.18. PMS\_DMA\_AHB\_PDMA\_UHCIO\_W\_PMS\_REG (0x0154)

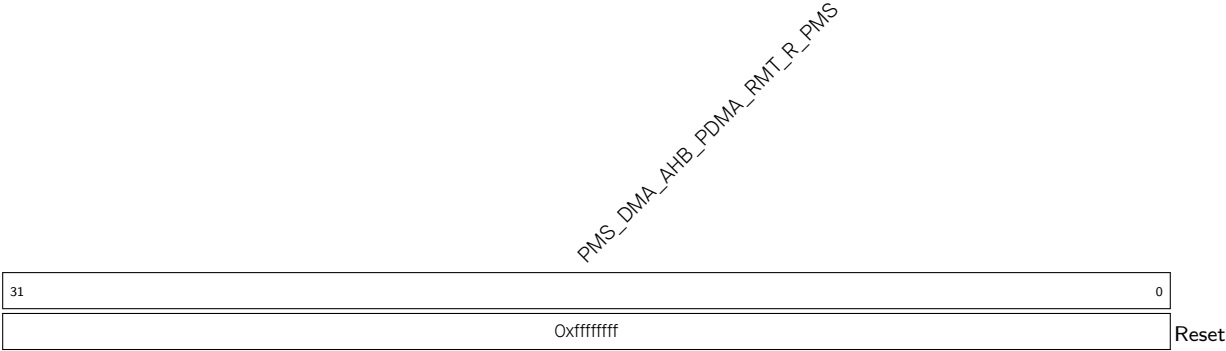


**PMS\_DMA\_AHB\_PDMA\_UHCIO\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by UHCI. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.19. PMS\_DMA\_AHB\_PDMA\_RMT\_R\_PMS\_REG (0x0158)

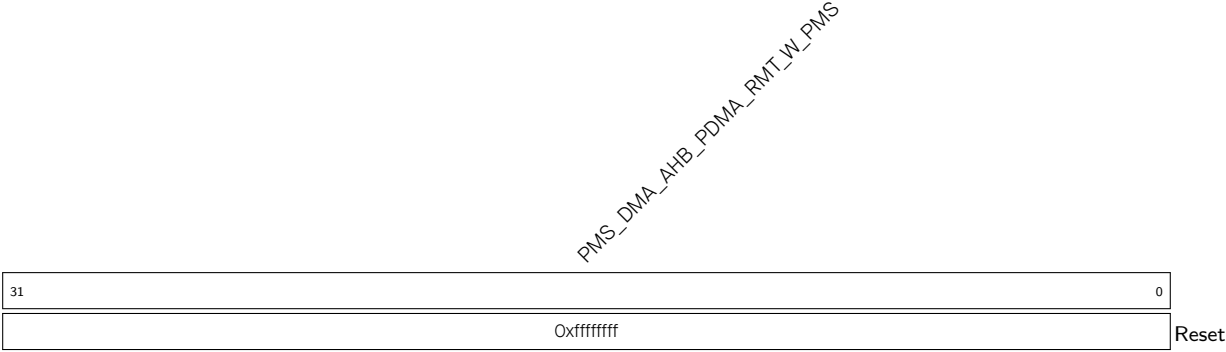


**PMS\_DMA\_AHB\_PDMA\_RMT\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by RMT. Bit 0 corresponds to region0, and so on.

0: Disable read permission.  
1: Enable read permission.

(R/W)

Register 18.20. PMS\_DMA\_AHB\_PDMA\_RMT\_W\_PMS\_REG (0x0170)



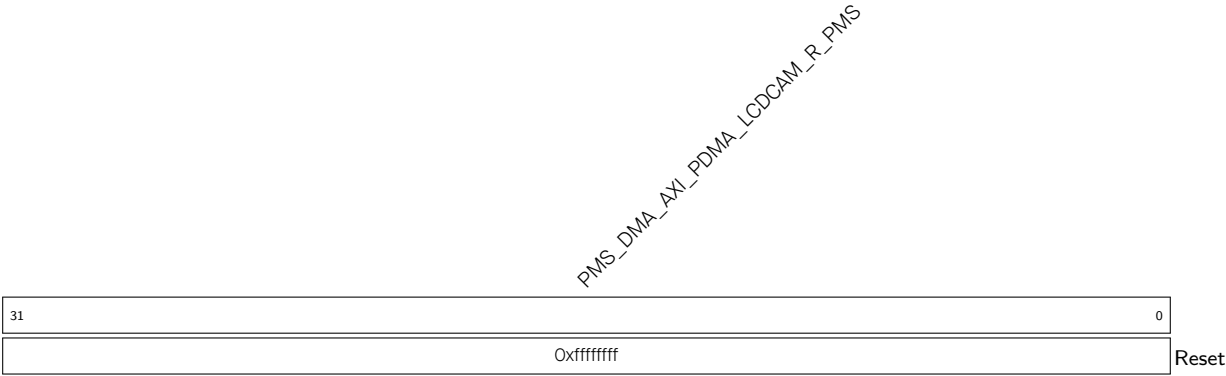
**PMS\_DMA\_AHB\_PDMA\_RMT\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by RMT. Bit 0 corresponds to region0, and so on.

0: Disable write permission.  
1: Enable write permission.

(R/W)



Register 18.21. PMS\_DMA\_AXI\_PDMA\_LCDCAM\_R\_PMS\_REG (0x0174)



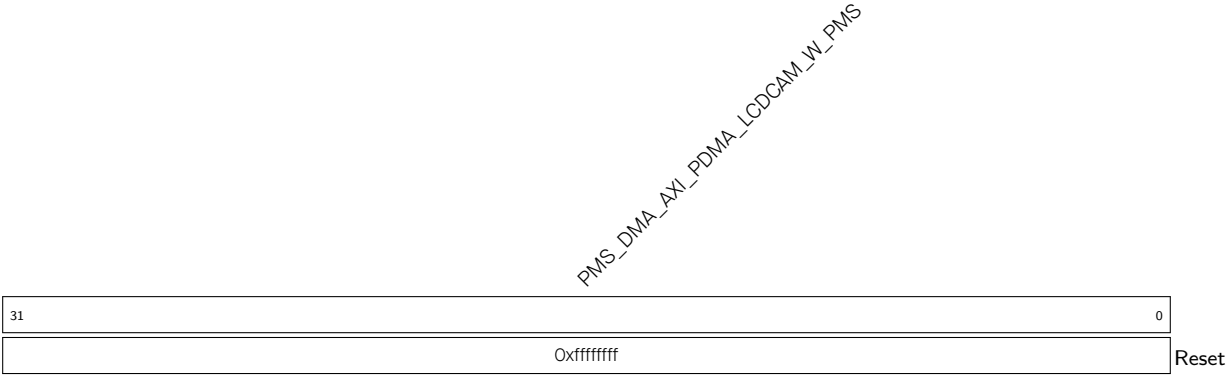
**PMS\_DMA\_AXI\_PDMA\_LCDCAM\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by LCD\_CAM. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

Register 18.22. PMS\_DMA\_AXI\_PDMA\_LCDCAM\_W\_PMS\_REG (0x0178)



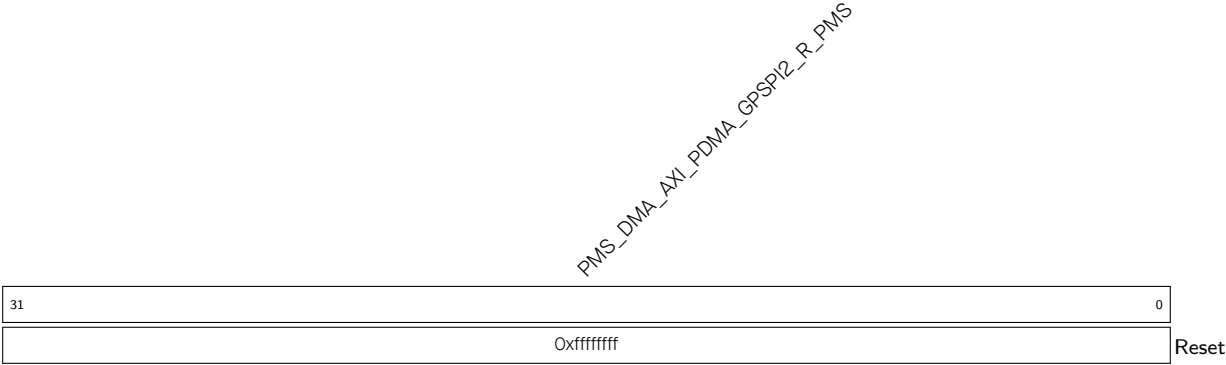
**PMS\_DMA\_AXI\_PDMA\_LCDCAM\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by LCD\_CAM. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

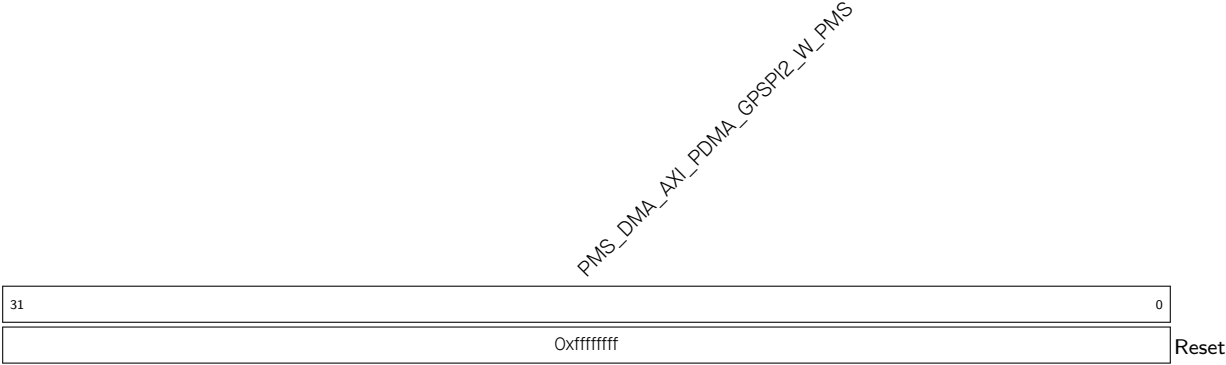
(R/W)

Register 18.23. PMS\_DMA\_AXI\_PDMA\_GPSPI2\_R\_PMS\_REG (0x017C)



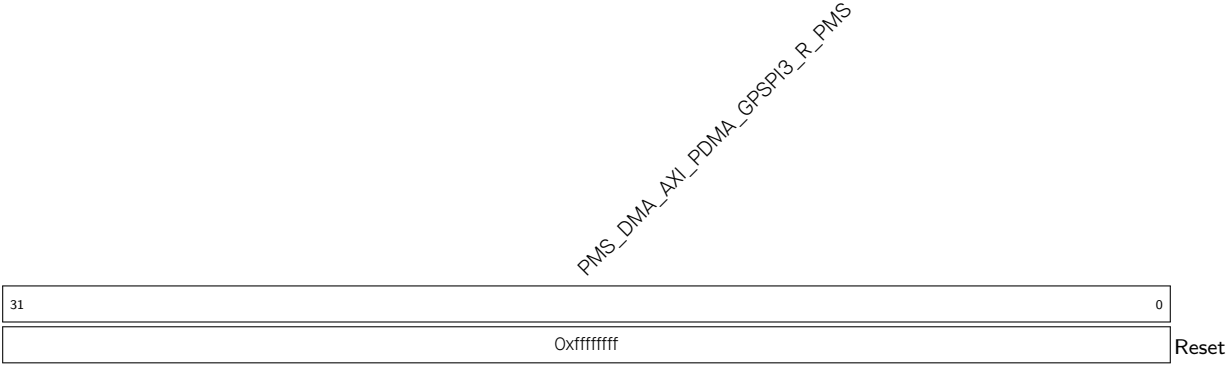
**PMS\_DMA\_AXI\_PDMA\_GPSPI2\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by GP-SPI2. Bit 0 corresponds to region0, and so on.  
0: Disable read permission.  
1: Enable read permission.  
(R/W)

Register 18.24. PMS\_DMA\_AXI\_PDMA\_GPSPI2\_W\_PMS\_REG (0x0180)



**PMS\_DMA\_AXI\_PDMA\_GPSPI2\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by GP-SPI2. Bit 0 corresponds to region0, and so on.  
0: Disable write permission.  
1: Enable write permission.  
(R/W)

Register 18.25. PMS\_DMA\_AXI\_PDMA\_GPSPI3\_R\_PMS\_REG (0x0184)



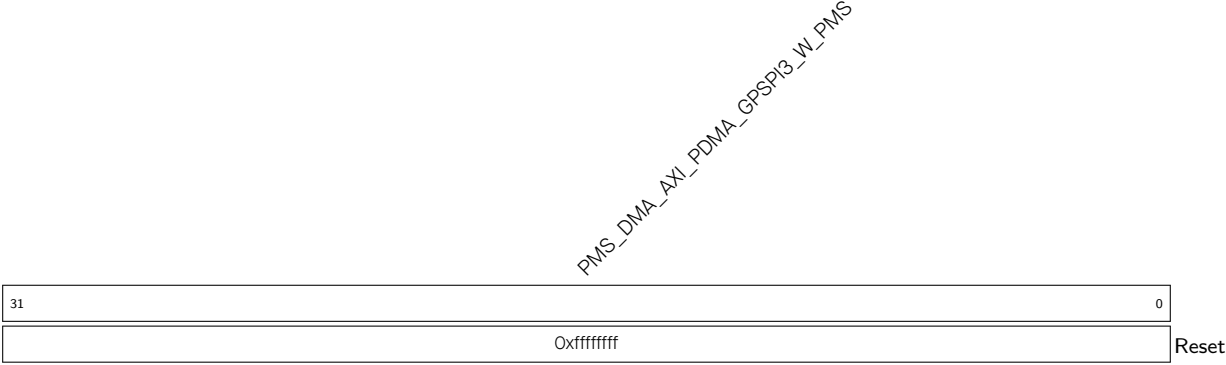
**PMS\_DMA\_AXI\_PDMA\_GPSPI3\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by GP-SPI3. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

Register 18.26. PMS\_DMA\_AXI\_PDMA\_GPSPI3\_W\_PMS\_REG (0x0188)



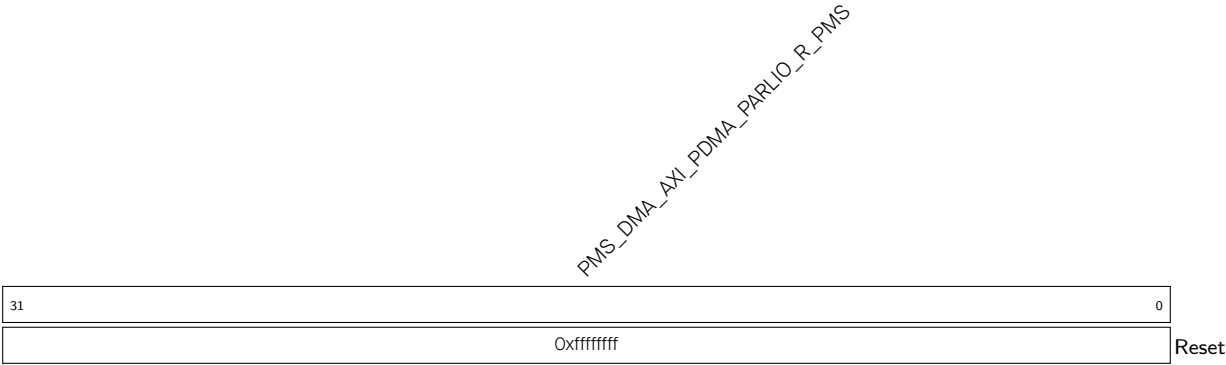
**PMS\_DMA\_AXI\_PDMA\_GPSPI3\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by GP-SPI3. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.27. PMS\_DMA\_AXI\_PDMA\_PARLIO\_R\_PMS\_REG (0x018C)

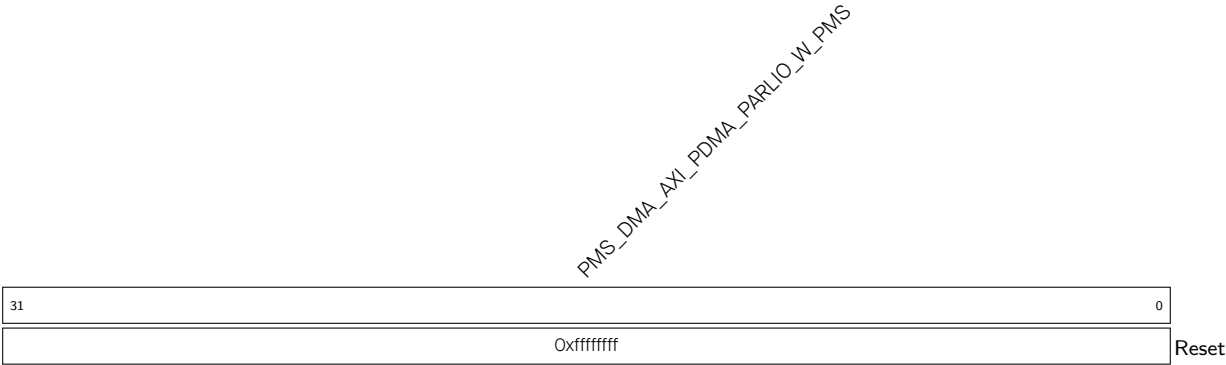


**PMS\_DMA\_AXI\_PDMA\_PARLIO\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by PARLIO (Parallel IO Controller). Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.28. PMS\_DMA\_AXI\_PDMA\_PARLIO\_W\_PMS\_REG (0x0190)

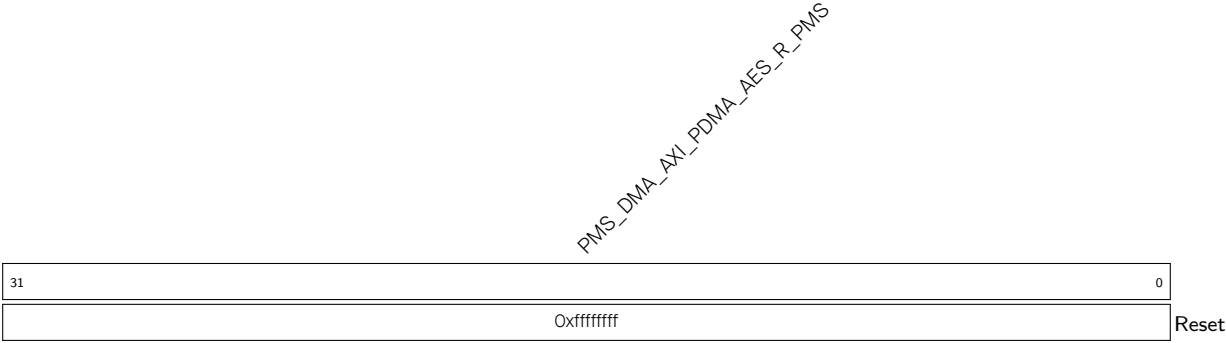


**PMS\_DMA\_AXI\_PDMA\_PARLIO\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by PARLIO. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.29. PMS\_DMA\_AXI\_PDMA\_AES\_R\_PMS\_REG (0x0194)

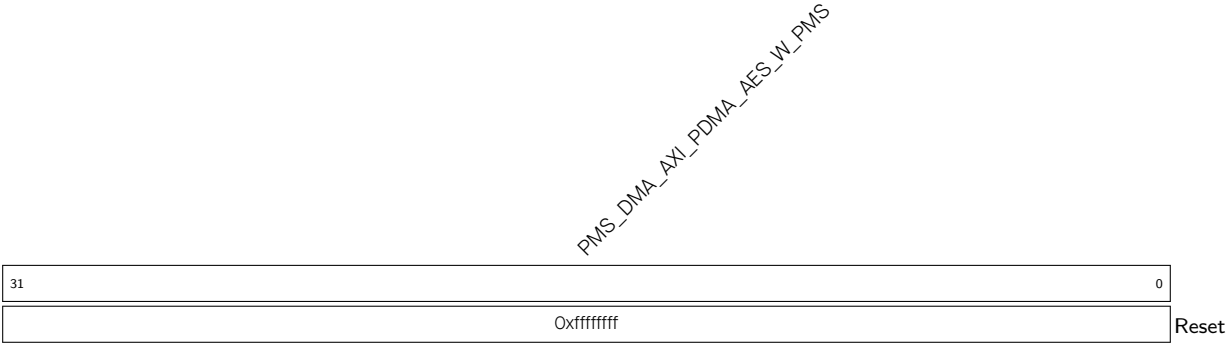


**PMS\_DMA\_AXI\_PDMA\_AES\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by AES. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.30. PMS\_DMA\_AXI\_PDMA\_AES\_W\_PMS\_REG (0x0198)

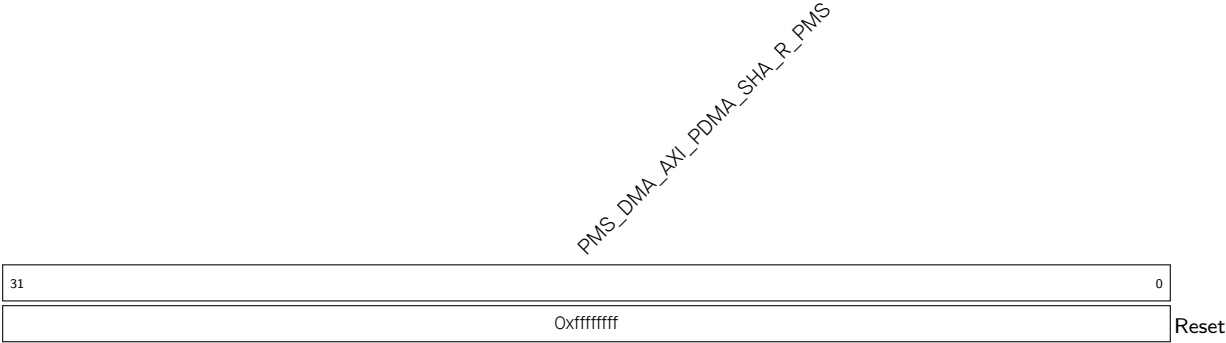


**PMS\_DMA\_AXI\_PDMA\_AES\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by AES. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.31. PMS\_DMA\_AXI\_PDMA\_SHA\_R\_PMS\_REG (0x019C)

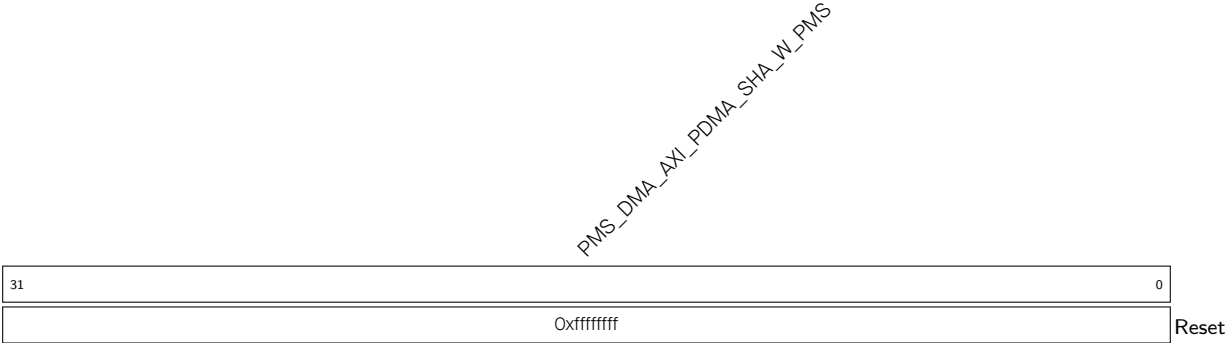


**PMS\_DMA\_AXI\_PDMA\_SHA\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by SHA. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.32. PMS\_DMA\_AXI\_PDMA\_SHA\_W\_PMS\_REG (0x01A0)

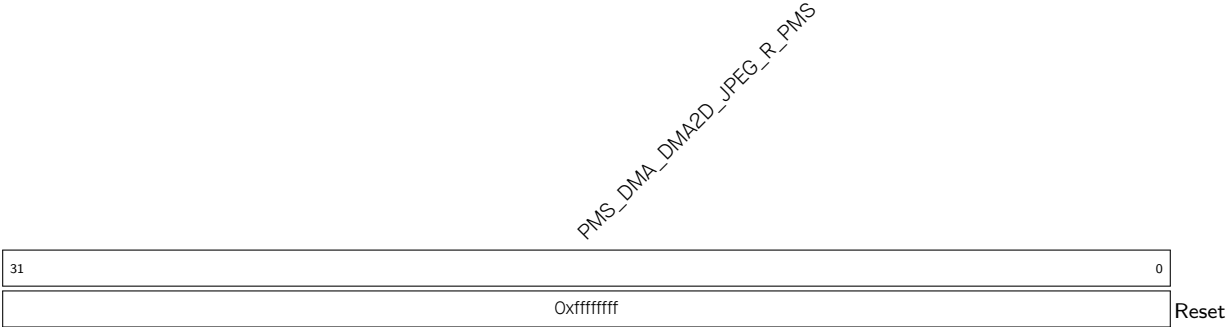


**PMS\_DMA\_AXI\_PDMA\_SHA\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by SHA. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.33. PMS\_DMA\_DMA2D\_JPEG\_PMS\_R\_REG (0x01A4)

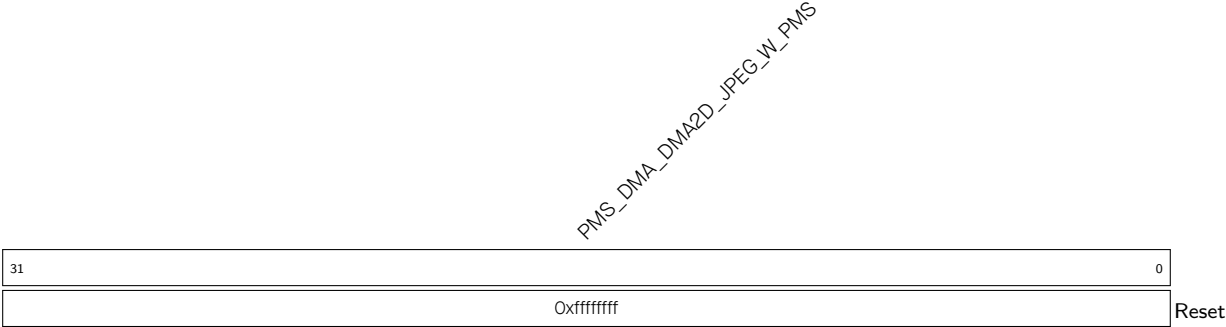


**PMS\_DMA\_DMA2D\_JPEG\_R\_PMS** Configures 2D-DMA permission to read 32 address ranges requested by JPEG. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

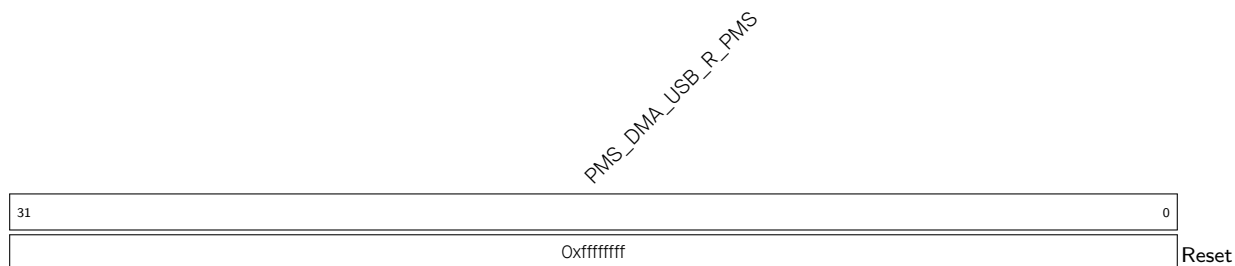
Register 18.34. PMS\_DMA\_DMA2D\_JPEG\_PMS\_W\_REG (0x01A8)



**PMS\_DMA\_DMA2D\_JPEG\_W\_PMS** Configures 2D-DMA permission to write 32 address ranges requested by JPEG. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

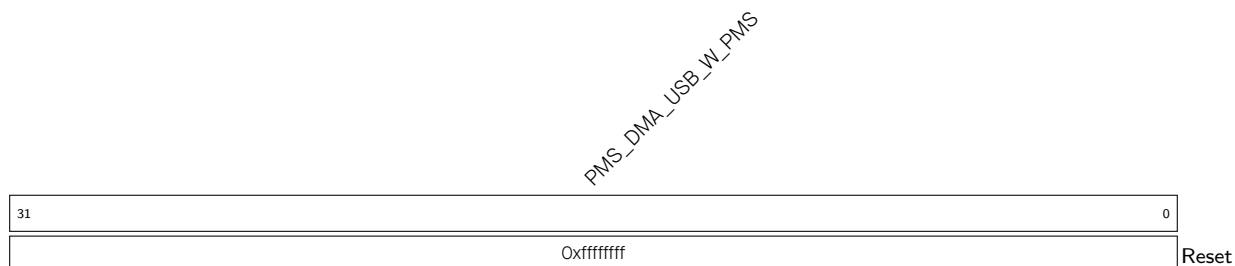
**Register 18.35. PMS\_DMA\_USB\_PMS\_R\_REG (0x01AC)**

**PMS\_DMA\_USB\_R\_PMS** Configures read permission for high-speed USB 2.0 OTG to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.36. PMS\_DMA\_USB\_PMS\_W\_REG (0x01B0)**

**PMS\_DMA\_USB\_W\_PMS** Configures write permission for high-speed USB 2.0 OTG to access 32 address ranges. Bit 0 corresponds to region0, and so on.

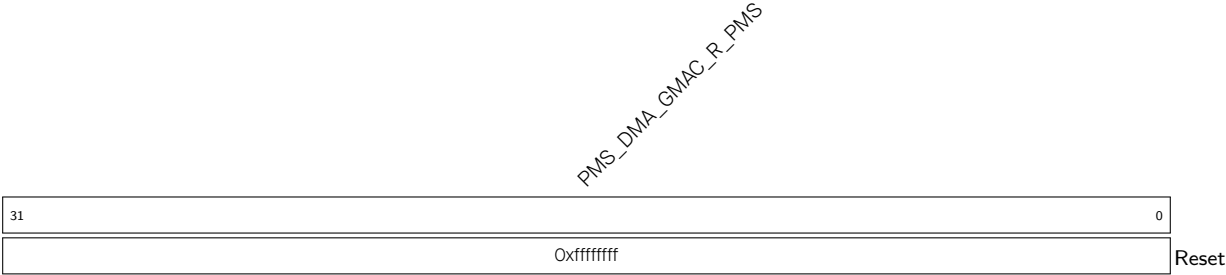
0: Disable write permission.

1: Enable write permission.

(R/W)

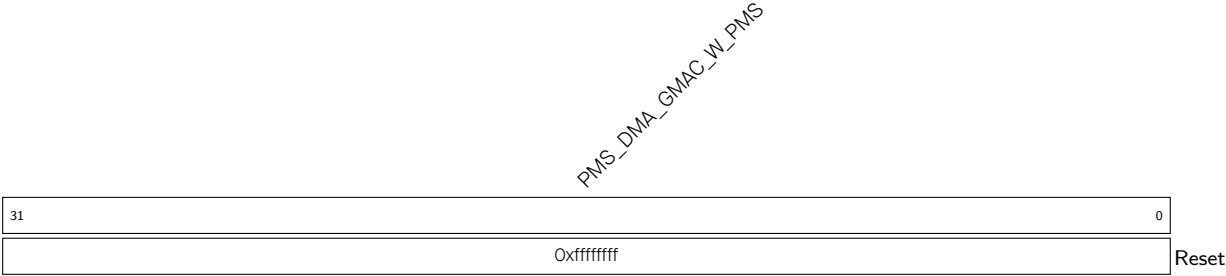


Register 18.37. PMS\_DMA\_GMAC\_PMS\_R\_REG (0x01B4)

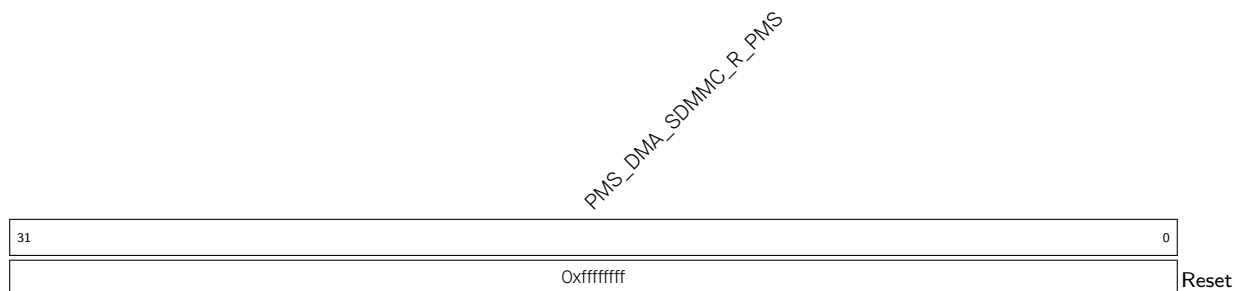


**PMS\_DMA\_GMAC\_R\_PMS** Configures read permission for EMAC to access 32 address ranges. Bit 0 corresponds to region0, and so on.  
0: Disable read permission.  
1: Enable read permission.  
(R/W)

Register 18.38. PMS\_DMA\_GMAC\_PMS\_W\_REG (0x01B8)



**PMS\_DMA\_GMAC\_W\_PMS** Configures write permission for EMAC to access 32 address ranges. Bit 0 corresponds to region0, and so on.  
0: Disable write permission.  
1: Enable write permission.  
(R/W)

**Register 18.39. PMS\_DMA\_SDMMC\_PMS\_R\_REG (0x01BC)**

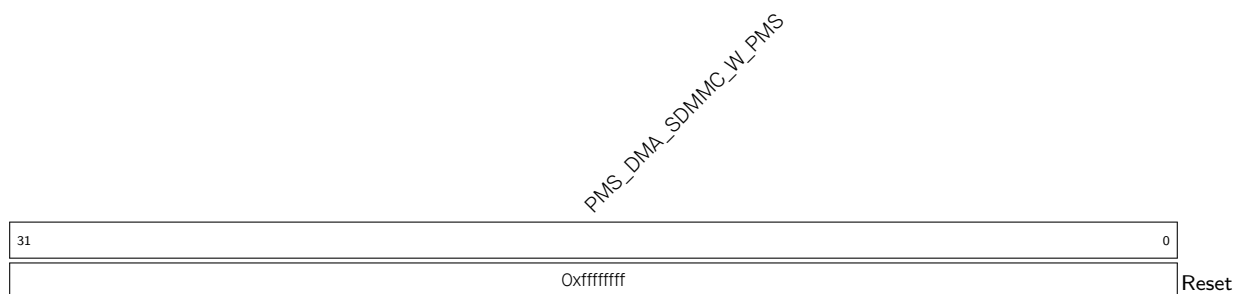
**PMS\_DMA\_SDMMC\_R\_PMS** Configures read permission for SDMMC to access 32 address ranges.

Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.40. PMS\_DMA\_SDMMC\_PMS\_W\_REG (0x01C0)**

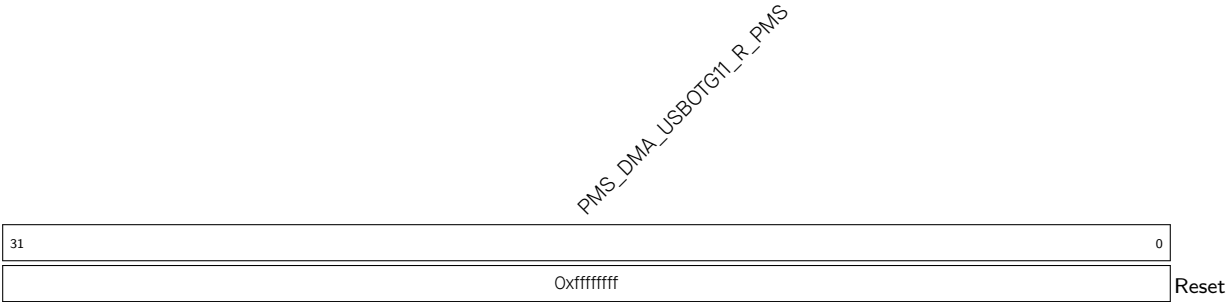
**PMS\_DMA\_SDMMC\_W\_PMS** Configures write permission for SDMMC to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.41. PMS\_DMA\_USBOTG11\_PMS\_R\_REG (0x01C4)



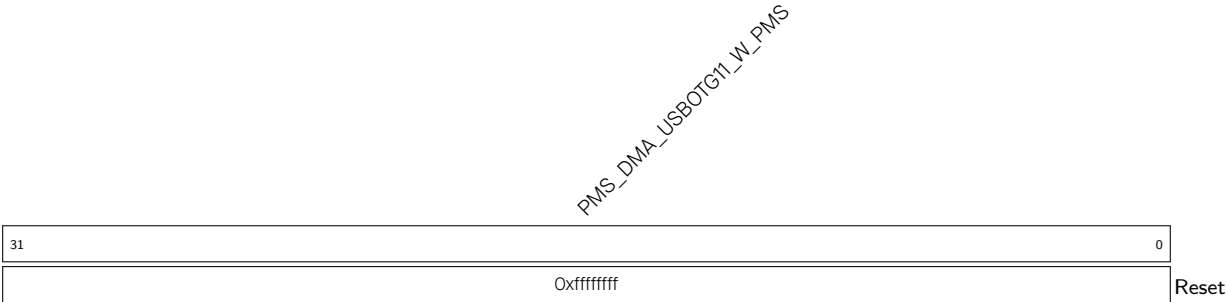
**PMS\_DMA\_USBOTG11\_R\_PMS** Configures read permission for full-speed USB 2.0 OTG to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

Register 18.42. PMS\_DMA\_USBOTG11\_PMS\_W\_REG (0x01C8)



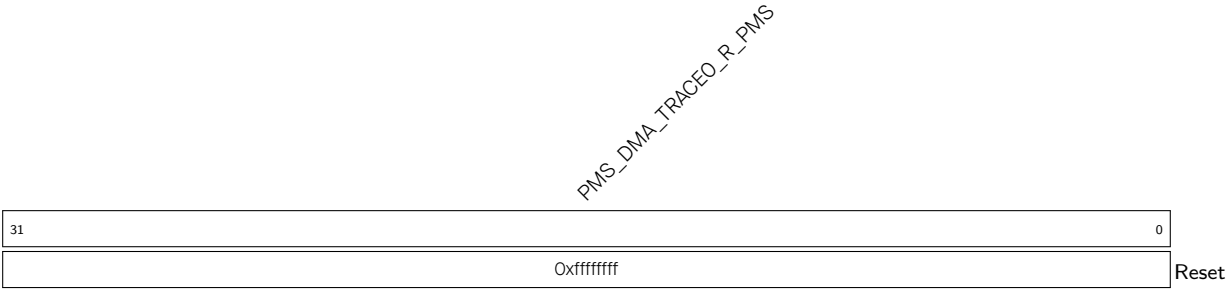
**PMS\_DMA\_USBOTG11\_W\_PMS** Configures write permission for full-speed USB 2.0 OTG to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

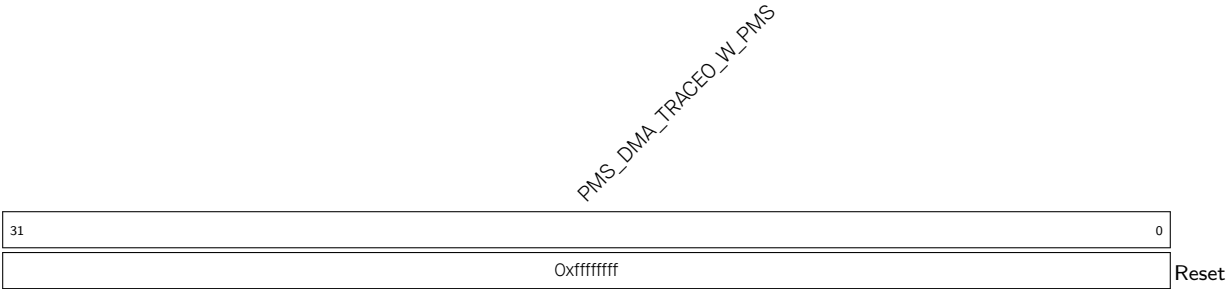
(R/W)

Register 18.43. PMS\_DMA\_TRACE0\_PMS\_R\_REG (0x01CC)

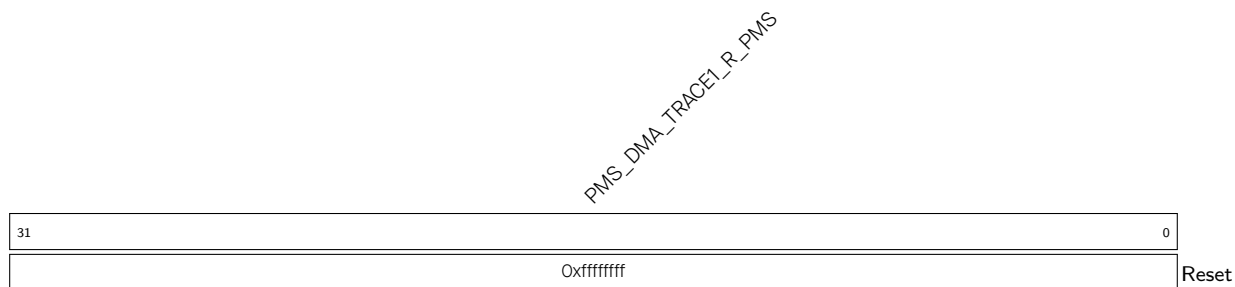


**PMS\_DMA\_TRACE0\_R\_PMS** Configures read permission for TRACE0 to access 32 address ranges.  
Bit 0 corresponds to region0, and so on.  
0: Disable read permission.  
1: Enable read permission.  
(R/W)

Register 18.44. PMS\_DMA\_TRACE0\_PMS\_W\_REG (0x01D0)



**PMS\_DMA\_TRACE0\_W\_PMS** Configures write permission for TRACE0 to access 32 address ranges.  
Bit 0 corresponds to region0, and so on.  
0: Disable write permission.  
1: Enable write permission.  
(R/W)

**Register 18.45. PMS\_DMA\_TRACE1\_PMS\_R\_REG (0x01D4)**

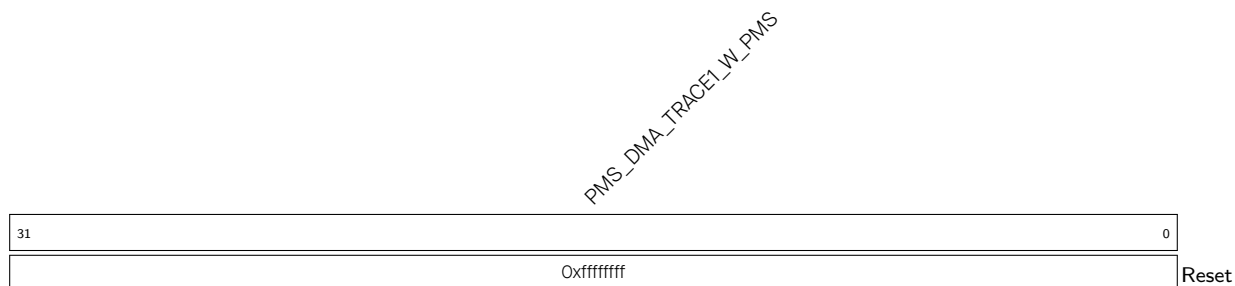
**PMS\_DMA\_TRACE1\_R\_PMS** Configures read permission for TRACE1 to access 32 address ranges.

Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.46. PMS\_DMA\_TRACE1\_PMS\_W\_REG (0x01D8)**

**PMS\_DMA\_TRACE1\_W\_PMS** Configures write permission for TRACE1 to access 32 address ranges.

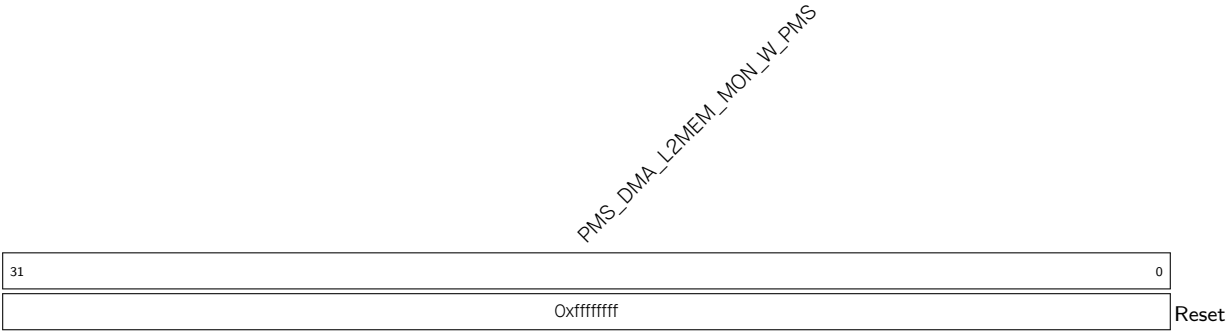
Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.47. PMS\_DMA\_L2MEM\_MON\_PMS\_W\_REG (0x01E0)



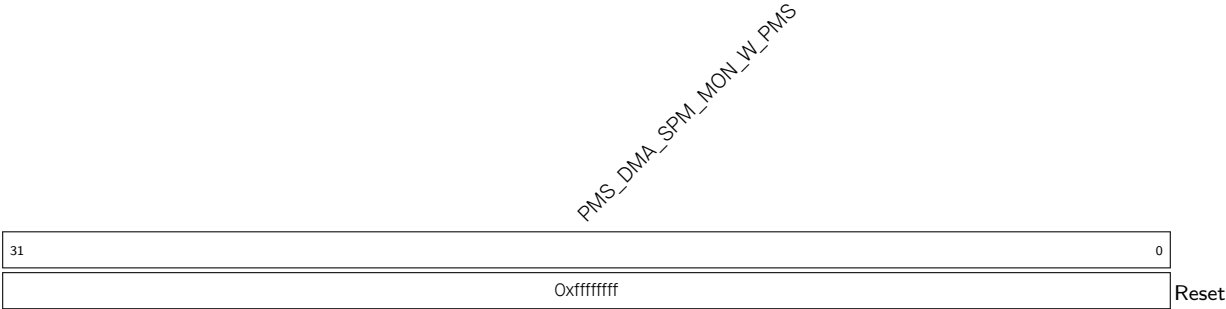
**PMS\_DMA\_L2MEM\_MON\_W\_PMS** Configures write permission for L2MEM monitor to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.48. PMS\_DMA\_SPM\_MON\_PMS\_W\_REG (0x01E8)



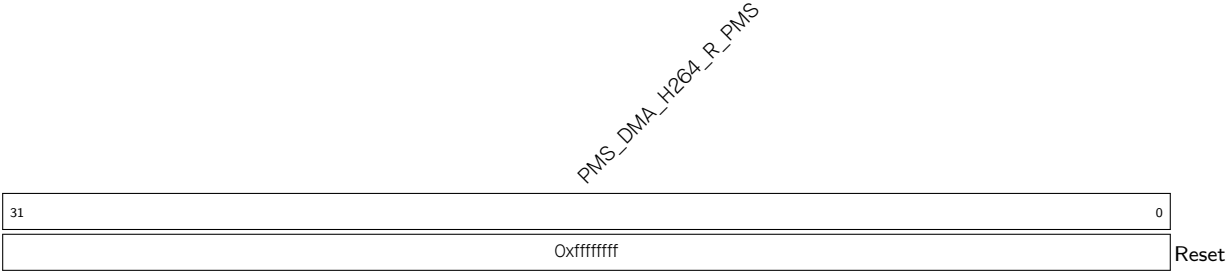
**PMS\_DMA\_SPM\_MON\_W\_PMS** Configures write permission for SPM monitor to access 32 address ranges. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

(R/W)

Register 18.49. PMS\_DMA\_H264\_PMS\_R\_REG (0x01FC)



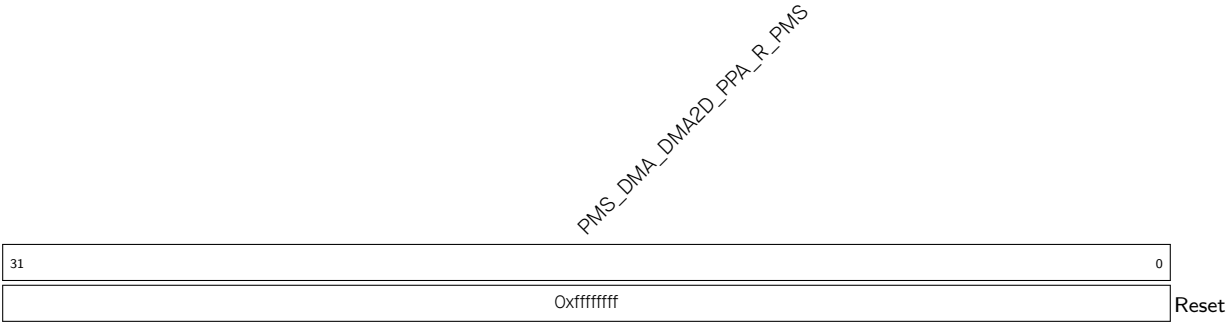
**PMS\_DMA\_H264\_R\_PMS** Configures read permission for H264 DMA to access 32 address ranges.  
Bit 0 corresponds to region0, and so on.  
0: Disable read permission.  
1: Enable read permission.  
(R/W)

Register 18.50. PMS\_DMA\_H264\_PMS\_W\_REG (0x0200)



**PMS\_DMA\_H264\_W\_PMS** Configures write permission for H264 DMA to access 32 address ranges.  
Bit 0 corresponds to region0, and so on.  
0: Disable write permission.  
1: Enable write permission.  
(R/W)

Register 18.51. PMS\_DMA\_DMA2D\_PPA\_PMS\_R\_REG (0x0204)

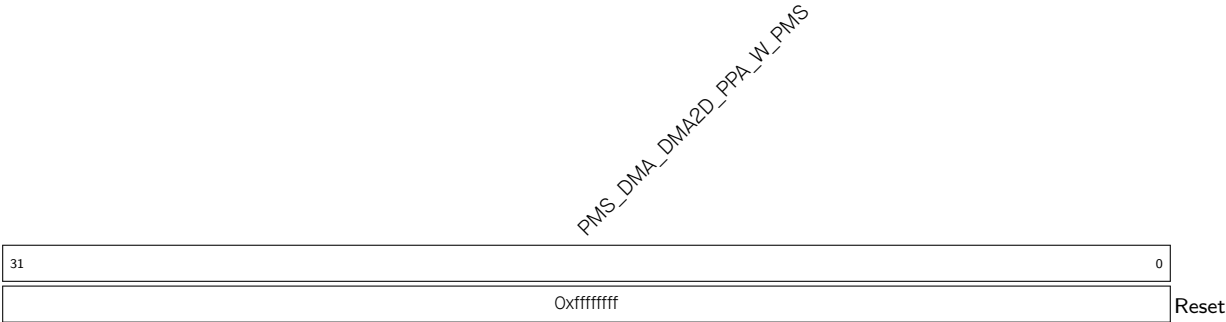


**PMS\_DMA\_DMA2D\_PPA\_R\_PMS** Configures 2D-DMA permission to read 32 address ranges requested by PPA (Pixel-Processing Accelerator). Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.52. PMS\_DMA\_DMA2D\_PPA\_PMS\_W\_REG (0x0208)



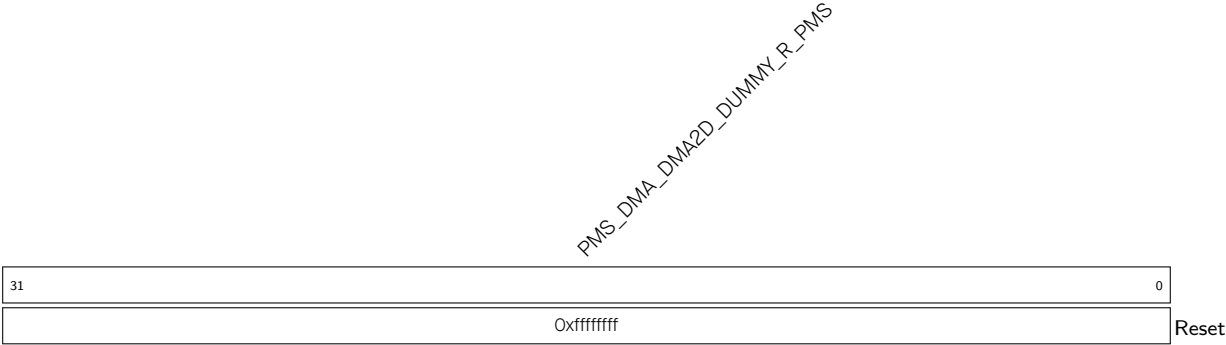
**PMS\_DMA\_DMA2D\_PPA\_W\_PMS** Configures 2D-DMA permission to write 32 address ranges requested by PPA. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)



Register 18.53. PMS\_DMA\_DMA2D\_DUMMY\_PMS\_R\_REG (0x020C)

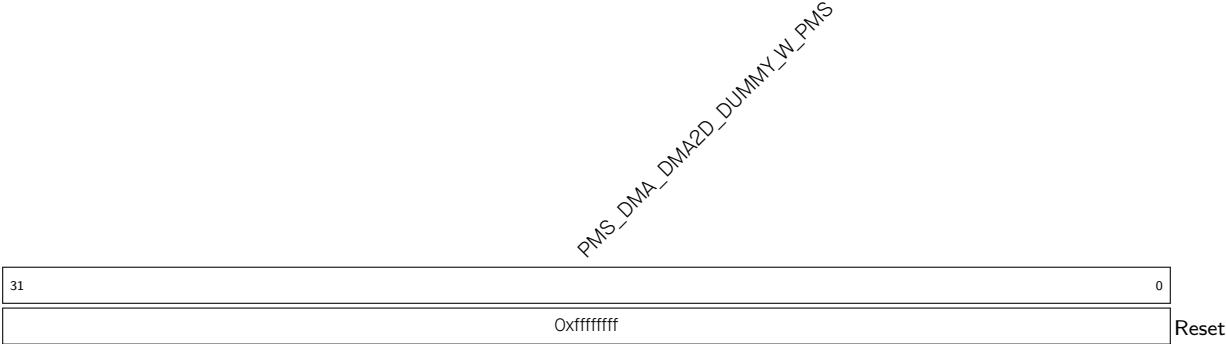


**PMS\_DMA\_DMA2D\_DUMMY\_R\_PMS** Configures 2D-DMA permission to read 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

Register 18.54. PMS\_DMA\_DMA2D\_DUMMY\_PMS\_W\_REG (0x0210)

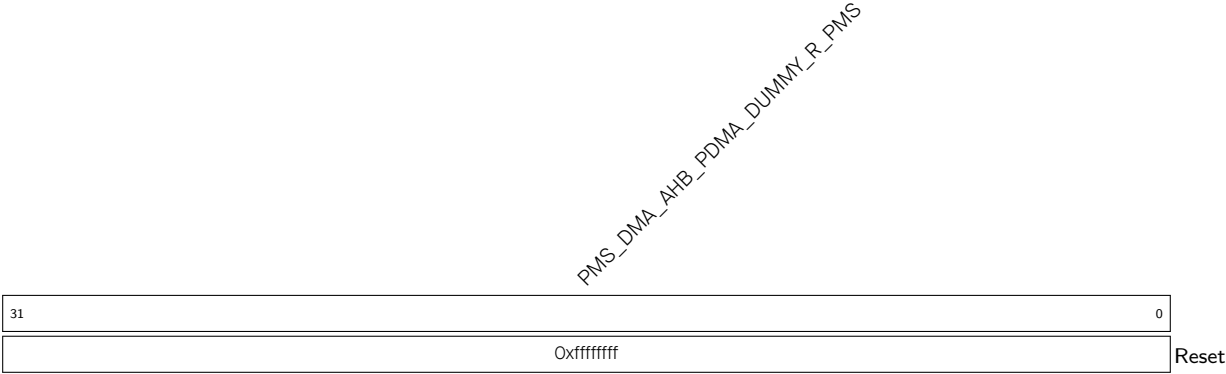


**PMS\_DMA\_DMA2D\_DUMMY\_W\_PMS** Configures 2D-DMA permission to write 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

Register 18.55. PMS\_DMA\_AHB\_PDMA\_DUMMY\_R\_PMS\_REG (0x0214)

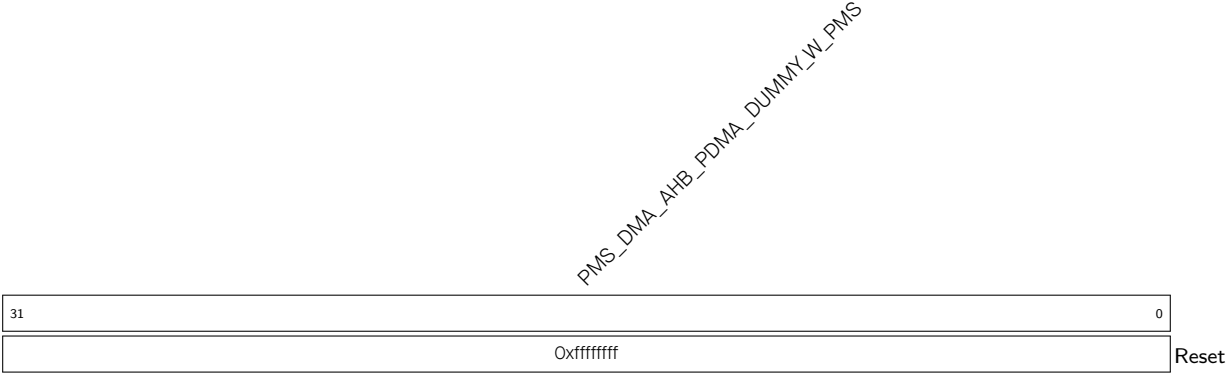


**PMS\_DMA\_AHB\_PDMA\_DUMMY\_R\_PMS** Configures GDMA-AHB permission to read 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

- 0: Disable read permission.
- 1: Enable read permission.

(R/W)

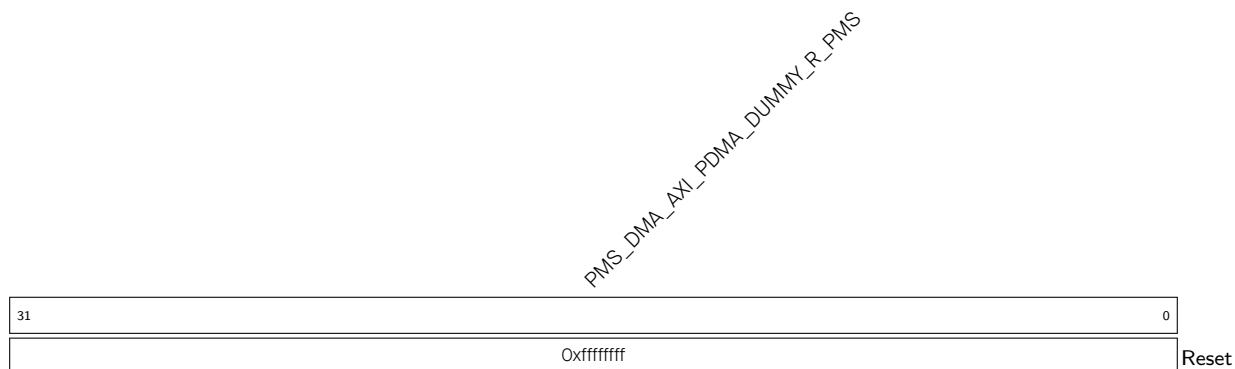
Register 18.56. PMS\_DMA\_AHB\_PDMA\_DUMMY\_W\_PMS\_REG (0x0218)



**PMS\_DMA\_AHB\_PDMA\_DUMMY\_W\_PMS** Configures GDMA-AHB permission to write 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

- 0: Disable write permission.
- 1: Enable write permission.

(R/W)

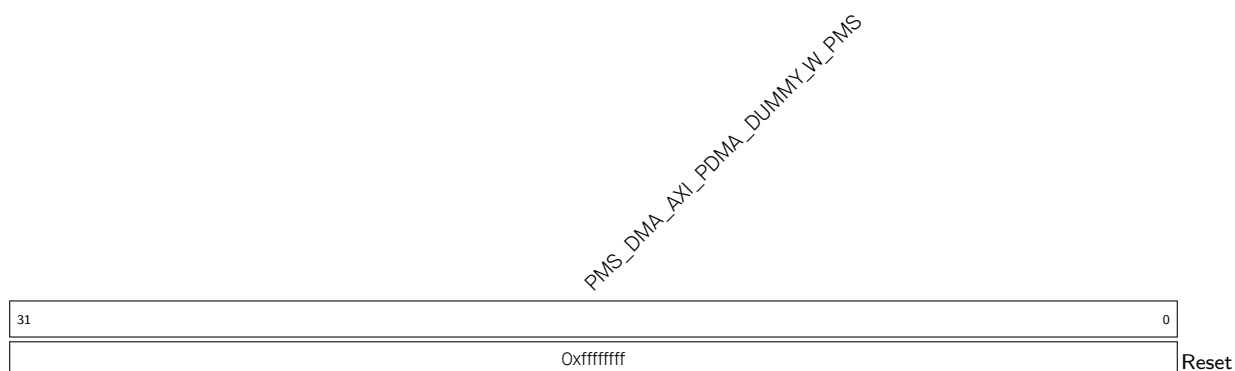
**Register 18.57. PMS\_DMA\_AXI\_PDMA\_DUMMY\_R\_PMS\_REG (0x021C)**

**PMS\_DMA\_AXI\_PDMA\_DUMMY\_R\_PMS** Configures GDMA-AXI permission to read 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

0: Disable read permission.

1: Enable read permission.

(R/W)

**Register 18.58. PMS\_DMA\_AXI\_PDMA\_DUMMY\_W\_PMS\_REG (0x0220)**

**PMS\_DMA\_AXI\_PDMA\_DUMMY\_W\_PMS** Configures GDMA-AXI permission to write 32 address ranges requested by Dummy. Bit 0 corresponds to region0, and so on.

0: Disable write permission.

1: Enable write permission.

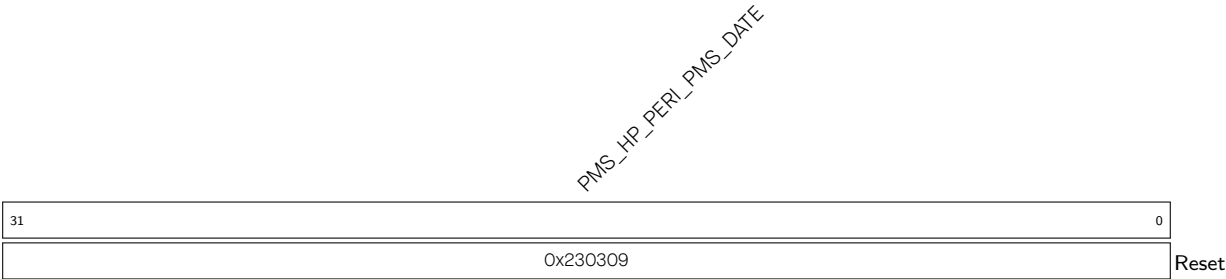
(R/W)

## 18.7.2 HP\_PERI\_PMS\_REG

The addresses in this section are relative to the HP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

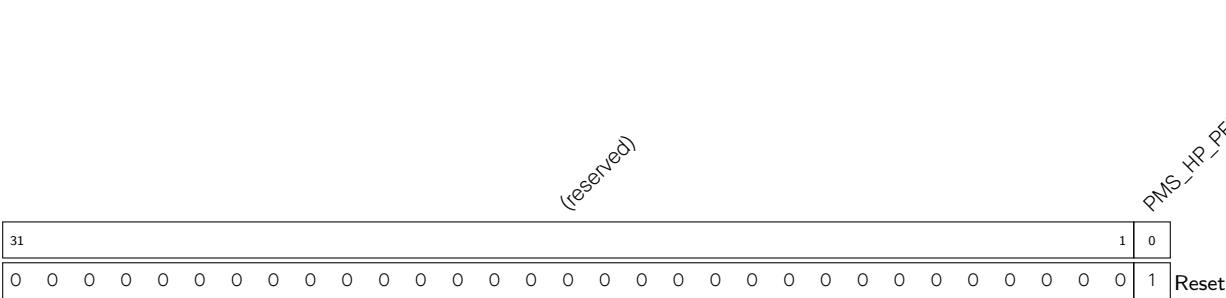
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 18.59. PMS\_HP\_PERI\_PMS\_DATE\_REG (0x0000)



PMS\_HP\_PERI\_PMS\_DATE Version control register. (R/W)

Register 18.60. PMS\_HP\_PERI\_PMS\_CLK\_EN\_REG (0x0004)



PMS\_HP\_PERI\_PMS\_CLK\_EN Configures whether to keep the clock always on.

- 0: Enable automatic clock gating
- 1: Keep the clock always on

(R/W)

Register 18.61. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x20\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |       |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---|---|---|---|---|---|---|---|-------|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | <div>PMS_CORE<math>n</math>_MM_CACHE_ALLOW<br/>PMS_CORE<math>n</math>_MM_SPM_MON_ALLOW<br/>PMS_CORE<math>n</math>_MM_L2MEM_MON_ALLOW<br/>PMS_CORE<math>n</math>_MM_CPU_TRACE1_ALLOW<br/>PMS_CORE<math>n</math>_MM_TRACE0_ALLOW<br/>(reserved)<br/>PMS_CORE<math>n</math>_MM_L2ROM_ALLOW<br/>PMS_CORE<math>n</math>_MM_L2MEM_ALLOW<br/>PMS_CORE<math>n</math>_MM_FLASH_ALLOW<br/>PMS_CORE<math>n</math>_MM_PSRAM_ALLOW</div> |   |    |    |   |   |   |   |   |   |   |   |       |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 12  |   | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1   | 1 | 1  | 1  | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Reset |   |  |

**PMS\_CORE $n$ \_MM\_PSRAM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access external RAM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_FLASH\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access external flash without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_L2MEM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP L2MEM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_L2ROM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP ROM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_TRACE0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access TRACE0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_TRACE1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access TRACE1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.61. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_CPU\_BUS\_MON\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access CPU bus monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_L2MEM\_MON\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access L2MEM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_SPM\_MON\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access SPM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_CACHE\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access cache.

0: Not allowed

1: Allowed

(R/W)

**Register 18.62. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>PMS_CORE<math>n</math>_MM_HP_H264_DMA2D_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_DMA_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_LP2HP_PERI_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_PERI_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_AXI_ICM_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_BITSAMPLER_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_H264_CORE_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_ISP_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_DSI_HOST_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_CSI_HOST_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_USB_PHY_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_GMAC_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_CRYPTO_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_PSRAM_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_FLASH_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_AXI_PDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_DMA2D_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_PPA_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_JPEG_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_AHB_PDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_SDMMC_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_GDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_USBOTG11_WRAP_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_USBOTG11_ALLOW</div> <div>PMS_CORE<math>n</math>_MM_HP_USBOTG_ALLOW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

Reset

**PMS\_CORE $n$ \_MM\_HP\_USBOTG\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP high-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_USBOTG11\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP full-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_USBOTG11\_WRAP\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP full-speed USB 2.0 OTG's wrap.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_GDMA\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP VDMA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_SDMMC\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP SDMMC.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.62. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_AHB\_PDMA\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access GDMA-AHB.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_JPEG\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP JPEG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_PPA\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP PPA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_DMA2D\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP 2D-DMA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_AXI\_PDMA\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP GDMA-AXI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_FLASH\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP flash MSPI controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_PSRAM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP PSRAM MSPI controller.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...



**Register 18.62. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_CRYPTO\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP CRYPTO (including AES/SHA/RSA/HMAC Accelerators).

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_GMAC\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP EMAC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_USB\_PHY\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP high-speed USB 2.0 OTG PHY.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_CSI\_HOST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP MIPI CSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_DSI\_HOST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP MIPI DSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_ISP\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP ISP (Image Signal Processor).

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_H264\_CORE\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP H264 Encoder.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.62. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_RMT\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP RMT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_BITSRAMBLER\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP bit scrambler.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_AXI\_ICM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP AXI ICM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_LP2HP\_PERI\_PMS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP2HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_DMA\_PMS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP\_DMA\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_H264\_DMA2D\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access 2D-DMA.

0: Not allowed

1: Allowed

(R/W)

**Register 18.63. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0010+0x20\* $n$ )**

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PMS_CORE $n$ _MM_HP_UHCI_ALLOW<br>PMS_CORE $n$ _MM_HP_ADC_ALLOW<br>(reserved)<br>PMS_CORE $n$ _MM_HP_LCDAM_ALLOW<br>PMS_CORE $n$ _MM_HP_I3C_SIV_ALLOW<br>PMS_CORE $n$ _MM_HP_I3C_MST_ALLOW<br>PMS_CORE $n$ _MM_HP_TWAI2_ALLOW<br>PMS_CORE $n$ _MM_HP_TWAI1_ALLOW<br>(reserved)<br>PMS_CORE $n$ _MM_HP_INTRMTX_ALLOW<br>PMS_CORE $n$ _MM_HP_ETM_ALLOW<br>PMS_CORE $n$ _MM_HP_LEDC_ALLOW<br>PMS_CORE $n$ _MM_HP_USBDEVICE_ALLOW<br>PMS_CORE $n$ _MM_HP_GSPi3_ALLOW<br>PMS_CORE $n$ _MM_HP_GSPi2_ALLOW<br>PMS_CORE $n$ _MM_HP_PARLIO_ALLOW<br>PMS_CORE $n$ _MM_HP_UART4_ALLOW<br>PMS_CORE $n$ _MM_HP_UART3_ALLOW<br>PMS_CORE $n$ _MM_HP_UART2_ALLOW<br>PMS_CORE $n$ _MM_HP_UART1_ALLOW<br>PMS_CORE $n$ _MM_HP_PCNT_ALLOW<br>PMS_CORE $n$ _MM_HP_I2S2_ALLOW<br>PMS_CORE $n$ _MM_HP_I2S1_ALLOW<br>PMS_CORE $n$ _MM_HP_I2S0_ALLOW<br>PMS_CORE $n$ _MM_HP_I2C1_ALLOW<br>PMS_CORE $n$ _MM_HP_I2C0_ALLOW<br>PMS_CORE $n$ _MM_HP_TIMER_GROUP1_ALLOW<br>PMS_CORE $n$ _MM_HP_TIMER_GROUP0_ALLOW<br>PMS_CORE $n$ _MM_HP_MCPWM1_ALLOW<br>PMS_CORE $n$ _MM_HP_MCPWM0_ALLOW |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1   | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Reset

**PMS\_CORE $n$ \_MM\_HP\_MCPWM0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP MCPWM0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_MCPWM1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP MCPWM1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_TIMER\_GROUP0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP timer group0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_TIMER\_GROUP1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP timer group1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I2C0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I2C0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I2C1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I2C1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.63. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_I2S0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I2S0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I2S1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I2S1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I2S2\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I2S2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_PCNT\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP PCNT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_UART0\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UART0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_UART1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UART1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_UART2\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UART2.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.63. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_UART3\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UART3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_UART4\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UART4.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_PARLIO\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP PARLIO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_GPSPI2\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP GP-SPI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_GPSPI3\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP GP-SPI3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_USBDEVICE\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP USB Serial/JTAG Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_LEDC\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP LEDC.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.63. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_ETM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP ETM (Event Task Matrix).

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_INTRMTX\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP interrupt matrix.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_TWAIO\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP TWAIO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_TWAI1\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP TWAI1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_TWAI2\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP TWAI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I3C\_MST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I3C master controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_I3C\_SLV\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP I3C slave controller.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.63. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_MM\_HP\_LCDCAM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP LCD\_CAM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_ADC\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP ADC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_UHCI\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP UHCI.

0: Not allowed

1: Allowed

(R/W)

Register 18.64. PMS\_CORE $n$ \_MM\_HP\_PERI\_PMS\_REG3\_REG ( $n$ : 0-1) (0x0014+0x20\* $n$ )

Diagram illustrating the structure of the `PMS_CORE_n_MM_HP_CLKRST_ALLOW` register. The register is 32 bits wide. Bits 31-5 are reserved. Bits 4-0 are the `PMS_CORE_n_MM_HP_CLKRST_ALLOW` field, which is 5 bits wide and contains the value 11111. The register is reset to 11111.

**PMS\_CORE $n$ \_MM\_HP\_GPIO\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP GPIO Matrix.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_IOMUX\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP IO MUX.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_SYSTIMER\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP system timer.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_SYS\_REG\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP system register.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_MM\_HP\_CLKRST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP\_SYS\_CLKRST.

0: Not allowed

1: Allowed

(R/W)



**Register 18.65. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0018+0x20\* $n$ )**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PMS_CORE $n$ _UM_CACHE_ALLOW<br>PMS_CORE $n$ _UM_SPM_MON_ALLOW<br>PMS_CORE $n$ _UM_L2MEM_MON_ALLOW<br>PMS_CORE $n$ _UM_CPU_BUS_MON_ALLOW<br>PMS_CORE $n$ _UM_TRACE1_ALLOW<br>PMS_CORE $n$ _UM_TRACE0_ALLOW<br>(reserved)<br>PMS_CORE $n$ _UM_L2ROM_ALLOW<br>PMS_CORE $n$ _UM_L2MEM_ALLOW<br>PMS_CORE $n$ _UM_FLASH_ALLOW<br>PMS_CORE $n$ _UM_PSRAM_ALLOW |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12   |   |   |   |   |   |   |   |   |   |   |   | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Reset |

Reset

**PMS\_CORE $n$ \_UM\_PSRAM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access external RAM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_FLASH\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access external flash without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_L2MEM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP L2MEM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_L2ROM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP ROM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_TRACE0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access TRACE0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_TRACE1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access TRACE1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.65. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REGO\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_CPU\_BUS\_MON\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access CPU bus monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_L2MEM\_MON\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access L2MEM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_SPM\_MON\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access SPM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_CACHE\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access cache.

0: Not allowed

1: Allowed

(R/W)

**Register 18.66. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x001C+0x20\* $n$ )**

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>PMS_CORE<math>n</math>_UM_HP_H264_DMA2D_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_DMA_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_LP2HP_PERI_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_PERI_PMS_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_AXI_ICM_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_RMT_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_H264_CORE_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_ISP_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_DSI_HOST_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_CSI_HOST_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_USB_PHY_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_GMAC_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_CRYPTO_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_PSRAM_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_FLASH_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_AXI_PDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_DMA2D_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_PPA_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_JPEG_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_AHB_PDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_SDMMC_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_GDMA_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_USBOTG1_WRAP_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_USBOTG1_ALLOW</div> <div>PMS_CORE<math>n</math>_UM_HP_USBOTG_ALLOW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

Reset

**PMS\_CORE $n$ \_UM\_HP\_USBOTG\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP high-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_USBOTG11\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP full-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_USBOTG11\_WRAP\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP full-speed USB 2.0 OTG's wrap.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_GDMA\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP VDMA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_SDMMC\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP SDMMC.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.66. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_AHB\_PDMA\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access GDMA-AHB.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_JPEG\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP JPEG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_PPA\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP PPA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_DMA2D\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP 2D-DMA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_AXI\_PDMA\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP GDMA-AXI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_FLASH\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP flash MSPI controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_PSRAM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP PSRAM MSPI controller.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.66. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_CRYPTO\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP CRYPTO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_GMAC\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP EMAC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_USB\_PHY\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP high-speed USB 2.0 OTG PHY.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_CSI\_HOST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP MIPI CSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_DSI\_HOST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP MIPI DSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_ISP\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP ISP.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_H264\_CORE\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP H264 Encoder.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.66. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG1\_REG ( $n$ : 0-1) (0x000C+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_RMT\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP RMT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_BITSRAMBLER\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP bit scrambler.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_AXI\_ICM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP AXI ICM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_LP2HP\_PERI\_PMS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP2HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_DMA\_PMS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP\_DMA\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_H264\_DMA2D\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access 2D-DMA.

0: Not allowed

1: Allowed

(R/W)

**Register 18.67. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0020+0x20\* $n$ )**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| PMS_CORE $n$ _UM_HP_UHCL_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_ADC_ALLOW          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_LCDAM_ALLOW        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I3C_SIV_ALLOW      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I3C_MST_ALLOW      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_TWA2_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_TWA1_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_INTRMTX_ALLOW      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_ETM_ALLOW          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_LEDC_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_USBDDEVICE_ALLOW   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_GPSP13_ALLOW       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_GPSP12_ALLOW       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_PARLIO_ALLOW       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_UART4_ALLOW        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_UART3_ALLOW        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_UART2_ALLOW        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_UART1_ALLOW        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_PCNT_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I2S2_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I2S1_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I2S0_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I2C1_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_I2C0_ALLOW         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_TIMER_GROUP1_ALLOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_TIMER_GROUP0_ALLOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_MCPWM1_ALLOW       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| PMS_CORE $n$ _UM_HP_MCPWM0_ALLOW       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

**PMS\_CORE $n$ \_UM\_HP\_MCPWM0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP MCPWM0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_MCPWM1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP MCPWM1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_TIMER\_GROUP0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP timer group0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_TIMER\_GROUP1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP timer group1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I2C0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I2C0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I2C1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I2C1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.67. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0020+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_I2S0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I2S0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I2S1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I2S1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I2S2\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I2S2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_PCNT\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP PCNT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_UART0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UART0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_UART1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UART1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_UART2\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UART2.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...



**Register 18.67. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0020+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_UART3\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UART3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_UART4\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UART4.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_PARLIO\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP PARLIO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_GPSPI2\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP GP-SPI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_GPSPI3\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP GP-SPI3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_USBDEVICE\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP USB/Serial JTAG Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_LEDC\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP LEDC.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.67. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0020+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_ETM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP ETM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_INTRMTX\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP interrupt matrix.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_TWAI0\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP TWAI0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_TWAI1\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP TWAI1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_TWAI2\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP TWAI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I3C\_MST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I3C master controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_I3C\_SLV\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP I3C slave controller.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.67. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG2\_REG ( $n$ : 0-1) (0x0020+0x20\* $n$ )**

Continued from the previous page...

**PMS\_CORE $n$ \_UM\_HP\_LCD\_CAM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP LCD\_CAM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_ADC\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP ADC.

0: Not allowed

1: Allowed

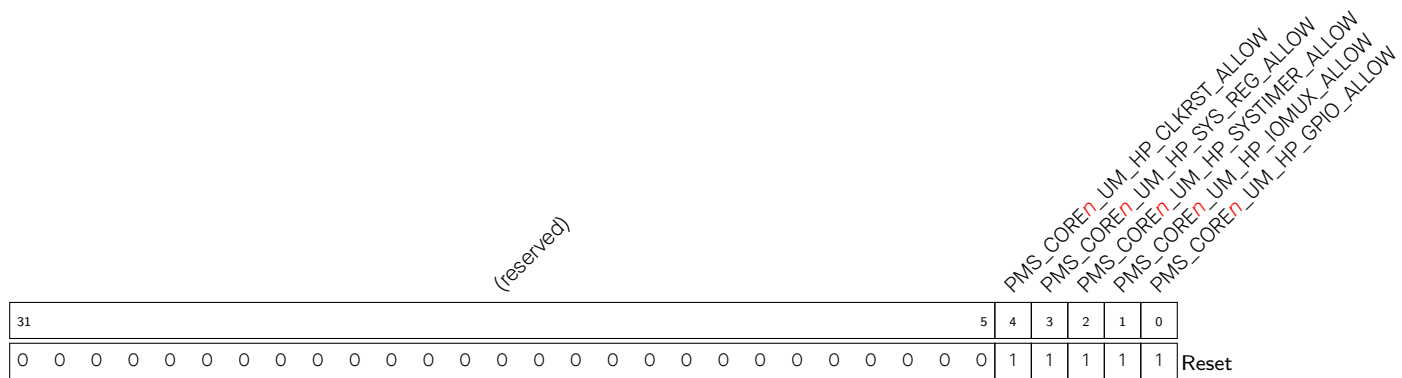
(R/W)

**PMS\_CORE $n$ \_UM\_HP\_UHCI\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP UHCI.

0: Not allowed

1: Allowed

(R/W)

**Register 18.68. PMS\_CORE $n$ \_UM\_HP\_PERI\_PMS\_REG3\_REG ( $n$ : 0-1) (0x0024+0x20\* $n$ )**

**PMS\_CORE $n$ \_UM\_HP\_GPIO\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP GPIO Matrix.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_IOMUX\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP IO MUX.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_SYSTIMER\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP system timer.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_SYS\_REG\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP system register.

0: Not allowed

1: Allowed

(R/W)

**PMS\_CORE $n$ \_UM\_HP\_CLKRST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP\_SYS\_CLKRST.

0: Not allowed

1: Allowed

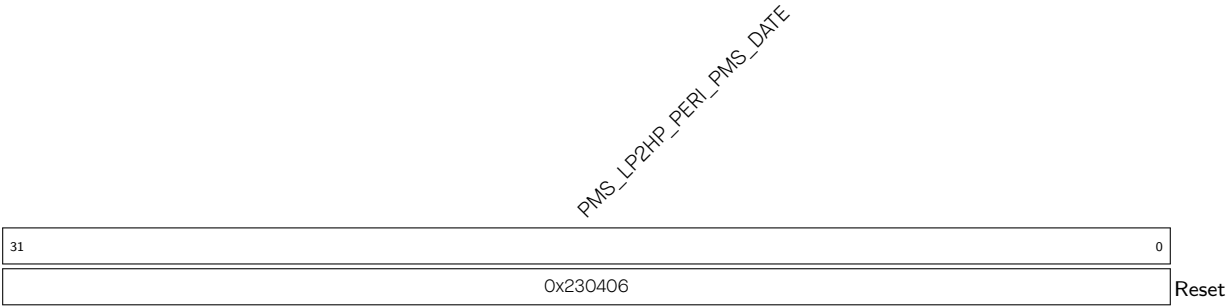
(R/W)

### 18.7.3 LP2HP\_PERI\_PMS\_REG

The addresses in this section are relative to the LP2HP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

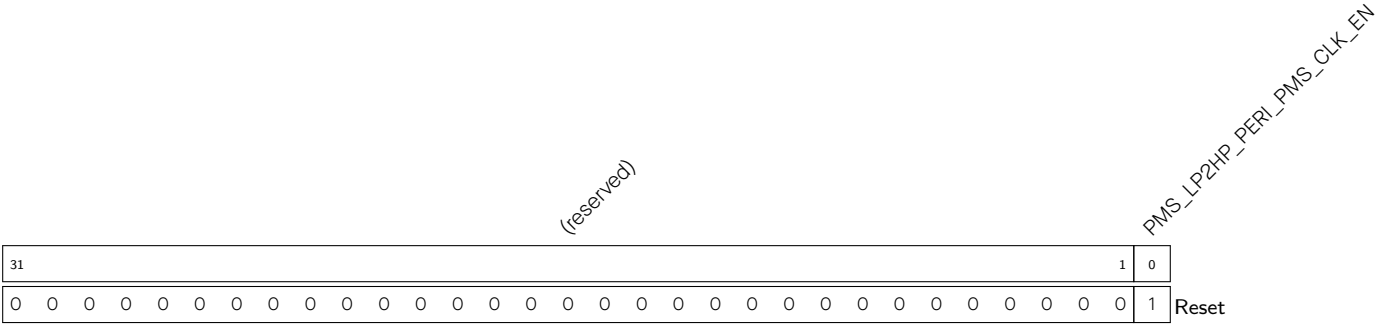
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 18.69. PMS\_LP2HP\_PERI\_PMS\_DATE\_REG (0x0000)



PMS\_LP2HP\_PERI\_PMS\_DATE Version control register. (R/W)

Register 18.70. PMS\_LP2HP\_PERI\_PMS\_CLK\_EN\_REG (0x0004)



PMS\_LP2HP\_PERI\_PMS\_CLK\_EN Configures whether to keep the clock always on.

- 0: Enable automatic clock gating.
- 1: Keep the clock always on.

(R/W)

Register 18.71. PMS\_LP\_MM\_PMS\_REGO\_REG (0x0008)

|            |   |   |   |   |   |   |   |   |   |   |   |    |    |    |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|----|----|----|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |    |    |    |   |   |   |   |   | PMS_LP_MM_CACHE_ALLOW<br>PMS_LP_MM_SPM_MON_ALLOW<br>PMS_LP_MM_L2MEM_MON_ALLOW<br>PMS_LP_MM_CPU_BUS_MON_ALLOW<br>PMS_LP_MM_TRACE1_ALLOW<br>(reserved)<br>PMS_LP_MM_L2ROM_ALLOW<br>PMS_LP_MM_L2MEM_ALLOW<br>PMS_LP_MM_FLASH_ALLOW<br>PMS_LP_MM_PSRAM_ALLOW |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4  | 3 | 2 | 1 | 0 |   |   |   |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 1 | 1  | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | Reset |

**PMS\_LP\_MM\_PSRAM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access external RAM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_FLASH\_ALLOW** Configures whether the LP CPU in machine mode has permission to access external flash without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_L2MEM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP L2M2M without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_L2ROM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP ROM without going through cache.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_TRACE0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access TRACE0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_TRACE1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access TRACE1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.71. PMS\_LP\_MM\_PMS\_REGO\_REG (0x0008)**

Continued from the previous page...

**PMS\_LP\_MM\_CPU\_BUS\_MON\_ALLOW** Configures whether the LP CPU in machine mode has permission to access CPU bus monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_L2MEM\_MON\_ALLOW** Configures whether the LP CPU in machine mode has permission to access L2MEM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_SPM\_MON\_ALLOW** Configures whether the LP CPU in machine mode has permission to access SPM monitor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_CACHE\_ALLOW** Configures whether the LP CPU in machine mode has permission to access cache.

0: Not allowed

1: Allowed

(R/W)

**Register 18.72. PMS\_LP\_MM\_PMS\_REG1\_REG (0x0030)**

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>PMS_LP_MM_HP_H264_DMA2D_ALLOW</div> <div>PMS_LP_MM_DMA_PMS_ALLOW</div> <div>PMS_LP_MM_LP2HP_PERI_PMS_ALLOW</div> <div>PMS_LP_MM_HP_AXI_ICM_ALLOW</div> <div>PMS_LP_MM_HP_BITRAMBLER_ALLOW</div> <div>PMS_LP_MM_HP_H264_CORE_ALLOW</div> <div>PMS_LP_MM_HP_ISP_ALLOW</div> <div>(reserved)</div> <div>PMS_LP_MM_HP_DSI_HOST_ALLOW</div> <div>PMS_LP_MM_HP_CSI_HOST_ALLOW</div> <div>PMS_LP_MM_HP_USB_PHY_ALLOW</div> <div>PMS_LP_MM_HP_GMAC_ALLOW</div> <div>PMS_LP_MM_HP_CRYPTO_ALLOW</div> <div>PMS_LP_MM_HP_PSRAM_ALLOW</div> <div>PMS_LP_MM_HP_FLASH_ALLOW</div> <div>PMS_LP_MM_HP_AXI_PDMA_ALLOW</div> <div>PMS_LP_MM_HP_DMA2D_ALLOW</div> <div>PMS_LP_MM_HP_PPA_ALLOW</div> <div>PMS_LP_MM_HP_JPEG_ALLOW</div> <div>PMS_LP_MM_HP_AHB_PDMA_ALLOW</div> <div>(reserved)</div> <div>PMS_LP_MM_HP_SDMMC_ALLOW</div> <div>PMS_LP_MM_HP_GDMA_ALLOW</div> <div>PMS_LP_MM_HP_USBOTG1_WRAP_ALLOW</div> <div>PMS_LP_MM_HP_USBOTG1_ALLOW</div> <div>PMS_LP_MM_HP_USBOTG_ALLOW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| O  | O  | O  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

Reset

**PMS\_LP\_MM\_HP\_USBOTG\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP high-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_USBOTG1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP full-speed USB 2.0 OTG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_USBOTG1\_WRAP\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP full-speed USB 2.0 OTG's wrap.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_GDMA\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP VDMA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_SDMMC\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP SDMMC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_AHB\_PDMA\_ALLOW** Configures whether the LP CPU in machine mode has permission to access GDMA-AHB.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...



**Register 18.72. PMS\_LP\_MM\_PMS\_REG1\_REG (0x0030)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_JPEG\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP JPEG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_PPA\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP PPA.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_DMA2D\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP 2D-DMA.

0: Not allowed 1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_AXI\_PDMA\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP GDMA-AXI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_FLASH\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP flash MSPI controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_PSRAM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP PSRAM MSPI controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_CRYPTO\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP CRYPTO.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.72. PMS\_LP\_MM\_PMS\_REG1\_REG (0x0030)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_GMAC\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP EMAC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_USB\_PHY\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP high-speed USB 2.0 OTG PHY.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_CSI\_HOST\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP MIPI CSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_DSI\_HOST\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP MIPI DSI host.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_ISP\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP ISP.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_H264\_CORE\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP H264 Encoder.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_RMT\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP RMT.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.72. PMS\_LP\_MM\_PMS\_REG1\_REG (0x0030)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_BITSRAMBLER\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP bit scrambler.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_AXI\_ICM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP AXI ICM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_PERI\_PMS\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP2HP\_PERI\_PMS\_ALLOW** Configures whether the LP CPU in machine mode has permission to access LP2HP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_DMA\_PMS\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP\_DMA\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_H264\_DMA2D\_ALLOW** Configures whether the LP CPU in machine mode has permission to access 2D-DMA.

0: Not allowed

1: Allowed

(R/W)

**Register 18.73. PMS\_LP\_MM\_PMS\_REG2\_REG (0x00A4)**

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| PMS_LP_MM_HP_UHCI_ALLOW<br>PMS_LP_MM_HP_ADC_ALLOW<br>PMS_LP_MM_HP_I2C_ALLOW<br>PMS_LP_MM_HP_I2C_SLV_ALLOW<br>PMS_LP_MM_HP_I2C_MST_ALLOW<br>PMS_LP_MM_HP_I2C_TWI2_ALLOW<br>PMS_LP_MM_HP_I2C_TWI1_ALLOW<br>PMS_LP_MM_HP_INTRMTX_ALLOW<br>PMS_LP_MM_HP_ETM_ALLOW<br>PMS_LP_MM_HP_I2C_ALLOW<br>PMS_LP_MM_HP_USBDEVICE_ALLOW<br>PMS_LP_MM_HP_GSPI3_ALLOW<br>PMS_LP_MM_HP_GSPI2_ALLOW<br>PMS_LP_MM_HP_PARLIO_ALLOW<br>PMS_LP_MM_HP_UART4_ALLOW<br>PMS_LP_MM_HP_UART3_ALLOW<br>PMS_LP_MM_HP_UART2_ALLOW<br>PMS_LP_MM_HP_UART1_ALLOW<br>PMS_LP_MM_HP_PCNT_ALLOW<br>PMS_LP_MM_HP_I2S2_ALLOW<br>PMS_LP_MM_HP_I2S1_ALLOW<br>PMS_LP_MM_HP_I2S0_ALLOW<br>PMS_LP_MM_HP_I2C1_ALLOW<br>PMS_LP_MM_HP_I2C0_ALLOW<br>PMS_LP_MM_HP_TIMER_GROUP1_ALLOW<br>PMS_LP_MM_HP_TIMER_GROUP0_ALLOW<br>PMS_LP_MM_HP_MCPWM1_ALLOW<br>PMS_LP_MM_HP_MCPWM0_ALLOW |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Reset

**PMS\_LP\_MM\_HP\_MCPWM0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP MCPWM0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_MCPWM1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP MCPWM1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_TIMER\_GROUP0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP timer group0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_TIMER\_GROUP1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP timer group1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I2C0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I2C0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I2C1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I2C1.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.73. PMS\_LP\_MM\_PMS\_REG2\_REG (0x00A4)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_I2S0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I2S0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I2S1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I2S1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I2S2\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I2S2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_PCNT\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP PCNT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_UART0\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UART0.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_UART1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UART1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_UART2\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UART2.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.73. PMS\_LP\_MM\_PMS\_REG2\_REG (0x00A4)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_UART3\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UART3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_UART4\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UART4.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_PARLIO\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP PARLIO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_GPSPI2\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP GP-SPI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_GPSPI3\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP GP-SPI3.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_USBDEVICE\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP USB/Serial JTAG Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_LEDC\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP LEDC.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.73. PMS\_LP\_MM\_PMS\_REG2\_REG (0x00A4)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_ETM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP ETM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_INTRMTX\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP interrupt matrix.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_TWAIO\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP TWAIO.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_TWAI1\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP TWAI1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_TWAI2\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP TWAI2.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I3C\_MST\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I3C master controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_I3C\_SLV\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP I3C slave controller.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.73. PMS\_LP\_MM\_PMS\_REG2\_REG (0x00A4)**

Continued from the previous page...

**PMS\_LP\_MM\_HP\_LCDCAM\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP LCD\_CAM.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_ADC\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP ADC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP\_UHCI\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP UHCI.

0: Not allowed

1: Allowed

(R/W)



Register 18.74. PMS\_LP\_MM\_PMS\_REG3\_REG (0x011C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMS_LP_MM_HP_CLKRST_ALLOW<br>PMS_LP_MM_HP_SYS_REG_ALLOW<br>PMS_LP_MM_HP_SYSTIMER_ALLOW<br>PMS_LP_MM_HP_IOMUX_ALLOW<br>PMS_LP_MM_HP_GPIO_ALLOW |   |   |       |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5   | 4 | 3 | 2     | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1   | 1 | 1 | Reset |   |   |  |

**PMS\_LP\_MM\_HP\_GPIO\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP GPIO Matrix.  
 0: Not allowed  
 1: Allowed  
 (R/W)

**PMS\_LP\_MM\_HP\_IOMUX\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP IO MUX.  
 0: Not allowed  
 1: Allowed  
 (R/W)

**PMS\_LP\_MM\_HP\_SYSTIMER\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP system timer.  
 0: Not allowed  
 1: Allowed  
 (R/W)

**PMS\_LP\_MM\_HP\_SYS\_REG\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP system register.  
 0: Not allowed  
 1: Allowed  
 (R/W)

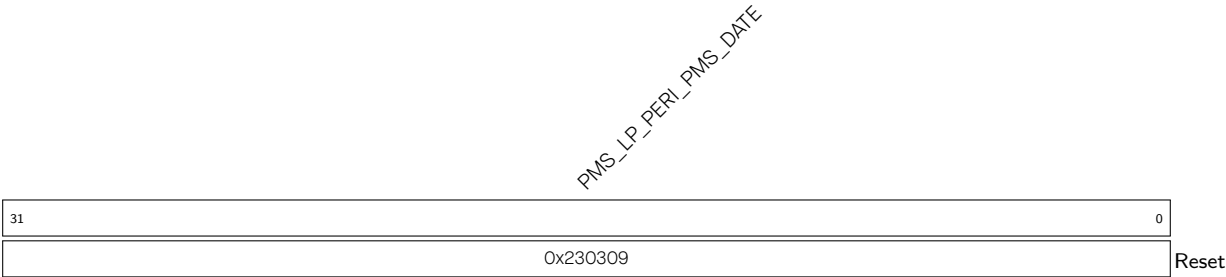
**PMS\_LP\_MM\_HP\_CLKRST\_ALLOW** Configures whether the LP CPU in machine mode has permission to access HP\_SYS\_CLKRST.  
 0: Not allowed  
 1: Allowed  
 (R/W)

## 18.7.4 LP\_PERI\_PMS\_REG

The addresses in this section are relative to the LP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

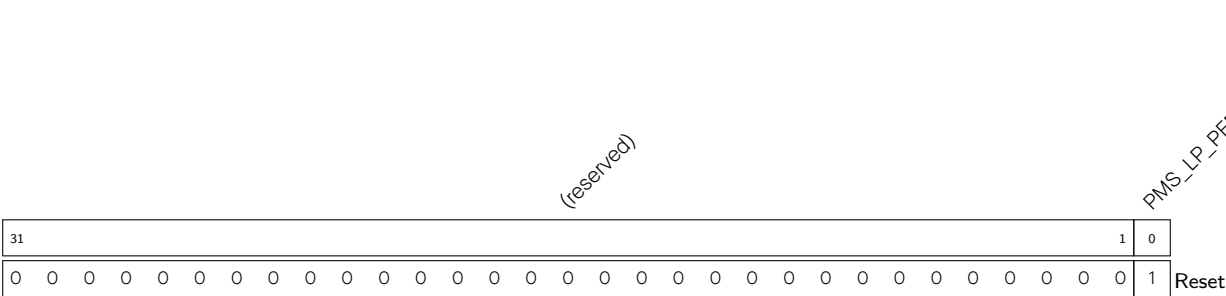
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 18.75. PMS\_LP\_PERI\_PMS\_DATE\_REG (0x0000)



PMS\_LP\_PERI\_PMS\_DATE Version control register (R/W)

Register 18.76. PMS\_LP\_PERI\_PMS\_CLK\_EN\_REG (0x0004)



PMS\_LP\_PERI\_PMS\_CLK\_EN Configures whether to keep the clock always on.  
0: Enable automatic clock gating  
1: Keep the clock always on  
(R/W)

**Register 18.77. PMS\_LP\_MM\_LP\_PERI\_PMS\_REGO\_REG (0x0008)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMS_LP_MM_LP_TSNS_ALLOW<br>PMS_LP_MM_LP_HP2LP_PMS_ALLOW<br>PMS_LP_MM_LP_PMS_ALLOW<br>PMS_LP_MM_LP_EFUSE_ALLOW<br>PMS_LP_MM_LP_INTR_ALLOW<br>PMS_LP_MM_LP_IOMUX_ALLOW<br>PMS_LP_MM_LP_TOUCH_ALLOW<br>PMS_LP_MM_LP_ADC_ALLOW<br>PMS_LP_MM_LP_I2S_ALLOW<br>PMS_LP_MM_LP_I2CMST_ALLOW<br>PMS_LP_MM_LP_I2C_ALLOW<br>PMS_LP_MM_LP_UART_ALLOW<br>(reserved)<br>PMS_LP_MM_LP_PERICKRST_ALLOW<br>PMS_LP_MM_LP_MAILBOX_ALLOW<br>PMS_LP_MM_LP_WDT_ALLOW<br>PMS_LP_MM_LP_PMU_ALLOW<br>PMS_LP_MM_LP_ANAPERI_ALLOW<br>PMS_LP_MM_LP_TIMER_ALLOW<br>PMS_LP_MM_LP_AONCLKRST_ALLOW<br>PMS_LP_MM_LP_SYSREG_ALLOW |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |

**PMS\_LP\_MM\_LP\_SYSREG\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP system registers.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_AONCLKRST\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP\_AONCLKRST (LP always-on clock and reset).

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_TIMER\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP timer.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_ANAPERI\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP ANAPERI (analog peripherals).

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_PMU\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP PMU (Power Management Unit).

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_WDT\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP WDT (watchdog timer).

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.77. PMS\_LP\_MM\_LP\_PERI\_PMS\_REGO\_REG (0x0008)**

Continued from the previous page...

**PMS\_LP\_MM\_LP\_MAILBOX\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP Mailbox Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_PERICKRST\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP PREICKRST (peripheral clock and reset).

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_UART\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP UART.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_I2C\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP I2S.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_SPI\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP SPI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_I2CMST\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP I2C master.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_I2S\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP I2S.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.77. PMS\_LP\_MM\_LP\_PERI\_PMS\_REGO\_REG (0x0008)**

Continued from the previous page...

**PMS\_LP\_MM\_LP\_ADC\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP ADC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_TOUCH\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP touch sensor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_IOMUX\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP IO MUX.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_INTR\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP INTR (interrupt).

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_EFUSE\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP eFuse.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_LP\_PMS\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_LP\_MM\_HP2LP\_PMS\_ALLOW** Configures whether LP CPU in machine mode has permission to access HP2LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

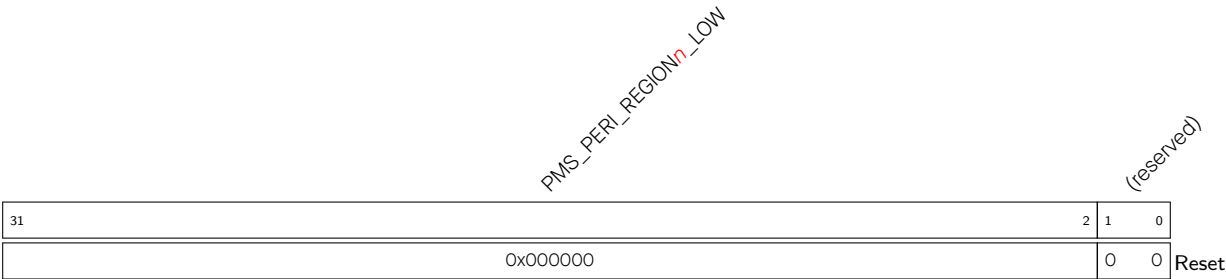
Continued on the next page...

Register 18.77. PMS\_LP\_MM\_LP\_PERI\_PMS\_REGO\_REG (0x0008)

Continued from the previous page...

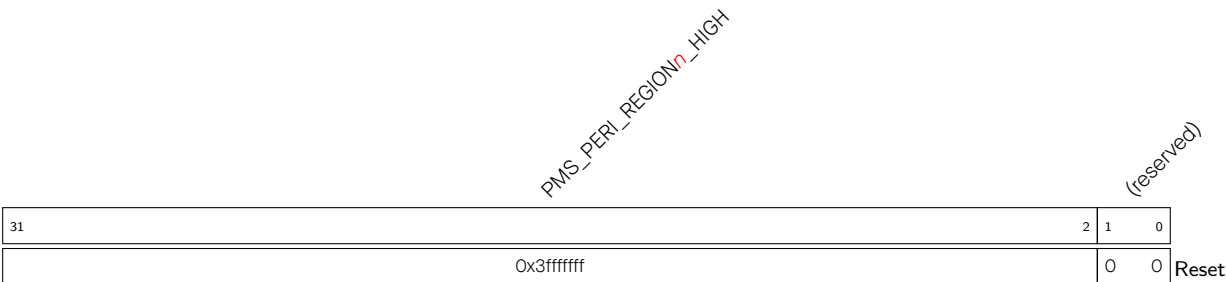
**PMS\_LP\_MM\_LP\_TSENS\_ALLOW** Configures whether LP CPU in machine mode has permission to access LP temperature sensor.  
0: Not allowed  
1: Allowed  
(R/W)

Register 18.78. PMS\_PERI\_REGION $n$ \_LOW\_REG ( $n$ : 0-1) (0x000C+0x8\* $n$ )



**PMS\_PERI\_REGION $n$ \_LOW** Configures the high 30 bits of the start address of peripheral register's region $n$ . (R/W)

Register 18.79. PMS\_PERI\_REGION $n$ \_HIGH\_REG ( $n$ : 0-1) (0x0010+0x8\* $n$ )



**PMS\_PERI\_REGION $n$ \_HIGH** Configures the high 30 bits of the end address of peripheral register's region $n$ . (R/W)

Register 18.80. PMS\_PERI\_REGION\_PMS\_REG (0x001C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                            |   |   |   |   |                            |   |   |   |   |                            |   |  |  |  |                            |  |  |  |  |                        |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------------|---|---|---|---|----------------------------|---|---|---|---|----------------------------|---|--|--|--|----------------------------|--|--|--|--|------------------------|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PMS_HP_CORE1_MM_REGION_PMS |   |   |   |   | PMS_HP_CORE1_UM_REGION_PMS |   |   |   |   | PMS_HP_CORE0_MM_REGION_PMS |   |  |  |  | PMS_HP_CORE0_UM_REGION_PMS |  |  |  |  | PMS_LP_CORE_REGION_PMS |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10                         |   | 9 | 8 | 7 | 6                          | 5 | 4 | 3 | 2 | 1                          | 0 |  |  |  |                            |  |  |  |  |                        |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 3                          | 3 | 3 | 3 | 3 | Reset                      |   |   |   |   |                            |   |  |  |  |                            |  |  |  |  |                        |  |  |  |  |

**PMS\_LP\_CORE\_REGION\_PMS** Configures whether LP core in machine mode has permission to access address region0 and address region1. Bit0 corresponds to region0 and bit1 corresponds to region1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE0\_UM\_REGION\_PMS** Configures whether HP CPU0 in user mode has permission to access address region0 and address region1. Bit2 corresponds to region0 and bit3 corresponds to region1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE0\_MM\_REGION\_PMS** Configures whether HP CPU0 in machine mode has permission to access address region0 and address region1. Bit4 corresponds to region0 and bit5 corresponds to region1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE1\_UM\_REGION\_PMS** Configures whether HP CPU1 in user mode has permission to access address region0 and address region1. Bit6 corresponds to region0 and bit7 corresponds to region1.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE1\_MM\_REGION\_PMS** Configures whether HP CPU1 in machine mode has permission to access address region0 and address region1. Bit8 corresponds to region0 and bit9 corresponds to region1.

0: Not allowed

1: Allowed

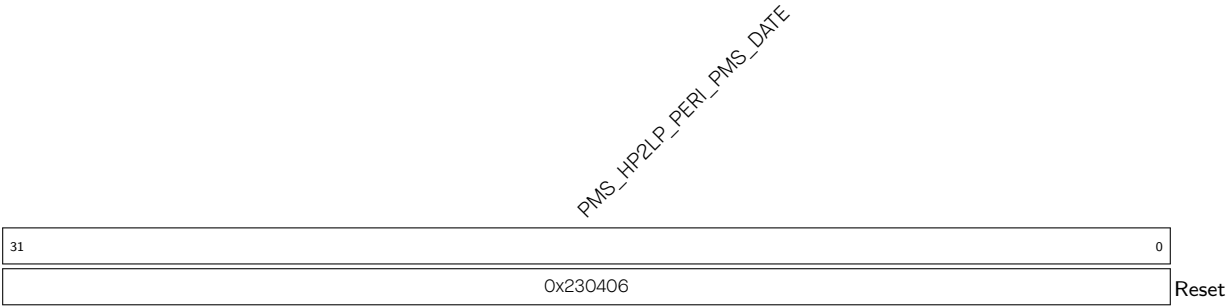
(R/W)

18.7.5 HP2LP\_PERI\_PMS\_REG

The addresses in this section are relative to the H2LP\_PERI\_PMS base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

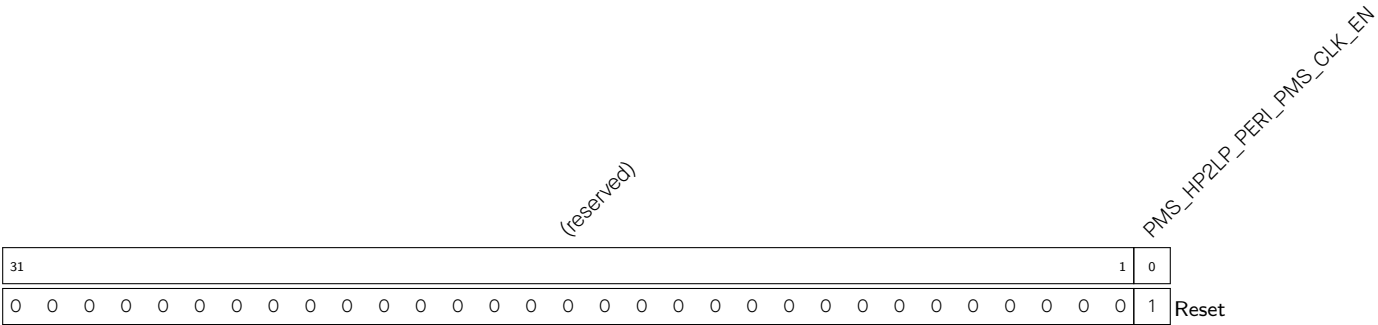
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 18.81. PMS\_HP2LP\_PERI\_PMS\_DATE\_REG (0x0000)



PMS\_HP2LP\_PERI\_PMS\_DATE Version control register (R/W)

Register 18.82. PMS\_HP2LP\_PERI\_PMS\_CLK\_EN\_REG (0x0004)



PMS\_HP2LP\_PERI\_PMS\_CLK\_EN Configures whether to keep the clock always on.  
0: Enable automatic clock gating  
1: Keep the clock always on  
(R/W)



Register 18.83. PMS\_HP\_CORE $n$ \_MM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x8\* $n$ )

[illegible]

**PMS\_HP\_CORE<sub>*n*</sub>\_MM\_LP\_SYSREG\_ALLOW** Configures whether HP CPU<sub>*n*</sub> in machine mode has permission to access LP System Registers.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_AONCLKRST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP\_AONCLKRST.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_TIMER\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP timer.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE<sub>n</sub>\_MM\_LP\_ANAPERI\_ALLOW** Configures whether HP CPU<sub>n</sub> in machine mode has permission to access LP ANAPERI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE<sub>n</sub>\_MM\_LP\_PMU\_ALLOW** Configures whether HP CPU<sub>n</sub> in machine mode has permission to access LP PMU.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.83. PMS\_HP\_CORE $n$ \_MM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_MM\_LP\_WDT\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP WDT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_MAILBOX\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP Mailbox Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_PERICKRST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP PERICKRST.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_UART\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP UART.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_I2C\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP I2C.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_SPI\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP SPI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_I2CMST\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP I2C master.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.83. PMS\_HP\_CORE $n$ \_MM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_MM\_LP\_I2S\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP I2S.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_ADC\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP ADC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_TOUCH\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP touch sensor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_IOMUX\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP IO MUX.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_INTR\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP INTR.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_EFUSE\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP eFuse.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_PMS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.83. PMS\_HP\_CORE $n$ \_MM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x0008+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_MM\_HP2LP\_PMS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access HP2LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_TSENS\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP temperature sensor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_MM\_LP\_SRAM\_ALLOW** Configures whether HP CPU $n$  in machine mode has permission to access LP SRAM.

0: Not allowed

1: Allowed

(R/W)

Register 18.84. PMS\_HP\_CORE $n$ \_UM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x000C+0x8\* $n$ )

|            |    |    |    |    |    |    |    |  |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|----|----|----|----|----|----|--|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |    |    |    |    |    |    | PMS_HP_CORE $n$ _UM_LP_SRAM_ALLOW<br>(reserved)<br>PMS_HP_CORE $n$ _UM_LP_TSENS_ALLOW<br>PMS_HP_CORE $n$ _UM_HP2LP_PMS_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_PMS_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_EFUSE_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_INTR_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_IOMUX_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_TOUCH_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_ADC_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_I2S_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_I2CMST_ALLOW<br>(reserved)<br>PMS_HP_CORE $n$ _UM_LP_UART_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_PERICLKST_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_MAILBOX_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_WDT_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_PMU_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_ANAPERI_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_TIMER_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_AONCLKRST_ALLOW<br>PMS_HP_CORE $n$ _UM_LP_SYSREG_ALLOW |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17   | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |       |

**PMS\_HP\_CORE $n$ \_UM\_LP\_SYSREG\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP System Registers.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_AONCLKRST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP\_AONCLKRST.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_TIMER\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP timer.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_ANAPERI\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP ANAPERI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_PMU\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP PMU.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.84. PMS\_HP\_CORE $n$ \_UM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x000C+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_UM\_LP\_WDT\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP WDT.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_MAILBOX\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP Mailbox Controller.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_PERICKRST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP PERICKRST.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_UART\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP UART.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_I2C\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP I2C.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_SPI\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP SPI.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_I2CMST\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP I2C master.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.84. PMS\_HP\_CORE $n$ \_UM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x000C+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_UM\_LP\_I2S\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP I2S.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_ADC\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP ADC.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_TOUCH\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP touch sensor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_IOMUX\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP IO MUX.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_INTR\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP INTR.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_EFUSE\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP eFuse.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_PMS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

Continued on the next page...

**Register 18.84. PMS\_HP\_CORE $n$ \_UM\_PMS\_REGO\_REG ( $n$ : 0-1) (0x000C+0x8\* $n$ )**

Continued from the previous page...

**PMS\_HP\_CORE $n$ \_UM\_HP2LP\_PMS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access HP2LP\_PERI\_PMS\_REG.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_TSENS\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP temperature sensor.

0: Not allowed

1: Allowed

(R/W)

**PMS\_HP\_CORE $n$ \_UM\_LP\_SRAM\_ALLOW** Configures whether HP CPU $n$  in user mode has permission to access LP SRAM.

0: Not allowed

1: Allowed

(R/W)



## Chapter 19

### Debug Assistant

#### 19.1 Overview

Debug Assistant is an auxiliary module that features a set of functions to help locate bugs and issues during software debugging.

#### 19.2 Features

- **Read/write monitoring:** Monitors whether the High-Performance dual-core CPU (HP CPU0 and HP CPU1) bus reads from or writes to a specified memory address space. A detected read or write in the monitored address space will trigger an interrupt.
- **Stack pointer (SP) monitoring:** Monitors whether the SP exceeds the specified address space. A bounds violation will trigger an interrupt.
- **Program counter (PC) logging:** Records the PC value. The developer can get the last PC value at the most recent reset of HP CPU0 or HP CPU1.
- **Bus access logging:** Records the information about bus access. When the HP CPU0, HP CPU1, or the Direct Memory Access controller (DMA) writes a specified value, the Debug Assistant module will record the data type, address of this write operation, and additionally the PC value when the write is performed by HP CPU0 or HP CPU1, and push such information to the HP L2MEM.

#### 19.3 Functional Description

##### 19.3.1 Region Read/Write Monitoring

The Debug Assistant module can monitor reads/writes performed by HP CPU0 bus in a certain address space, i.e., memory region. Whenever the bus reads or writes in the specified address space, an interrupt will be triggered. Please refer to Table 6 in Chapter 1 *High-Performance CPU [to be added later]*. In this chapter, when HP CPU0 bus accesses the data space, it is referred to as the Data bus, and when HP CPU0 bus accesses the AHB peripheral space, it is referred to as the Peripheral bus. The Data bus can monitor two memory regions (assuming they are HP CPU0 region 0 and HP CPU0 region 1, defined by developers' needs) at the same time, and so can Peripheral bus.

This is also the case for HP CPU1.

### 19.3.2 SP Monitoring

The Debug Assistant module can monitor the SP so as to prevent stack overflow or erroneous push/pop in HP CPU0. When the HP CPU0 SP goes below or beyond the lower or upper bound of the HP CPU0 SP monitored region, the module will record the PC pointer and generate an interrupt. The bound is configured by software.

This is also the case for HP CPU1.

### 19.3.3 PC Logging

In some cases, software developers want to know the PC at the last reset of HP CPU0. For instance, when the program is stuck and can only be reset, the developer may want to know where the program got stuck in order to debug. The Debug Assistant module can record the PC at the last reset of HP CPU0, which can be then read for software debugging.

This is also the case for HP CPU1.

### 19.3.4 CPU/DMA Bus Access Logging

The Debug Assistant module can record the information about the HP CPU0 Data bus's, HP CPU1 bus's, and DMA bus's write behaviors in real time. When a write operation occurs in or a specific value is written to a specified address space, the module will record the bus type, the address, PC (only when the write is performed by the HP CPU0 or HP CPU1, will PC be recorded), and other information, and then store the data in the HP L2MEM in a certain format. The specified address range must fall within the permitted memory regions of HP SPM or HP L2MEM.

## 19.4 Interrupts

The following interrupt sources from the Debug Assistant module can generate the interrupt signal ASSIST\_DEBUG\_INT.

- ASSIST\_DEBUG\_CORE\_0\_AREA\_DRAMO\_0\_RD\_INT: Triggered when the HP CPU0 Data bus reads in HP CPU0 region 0.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_DRAMO\_0\_WR\_INT: Triggered when the HP CPU0 Data bus writes in HP CPU0 region 0.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_DRAMO\_1\_RD\_INT: Triggered when the HP CPU0 Data bus reads in HP CPU0 region 1.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_DRAMO\_1\_WR\_INT: Triggered when the HP CPU0 Data bus writes in HP CPU0 region 1.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_PIF\_0\_RD\_INT: Triggered when the HP CPU0 Peripheral bus reads in HP CPU0 region 0.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_PIF\_0\_WR\_INT: Triggered when the HP CPU0 Peripheral bus writes in HP CPU0 region 0.
- ASSIST\_DEBUG\_CORE\_0\_AREA\_PIF\_1\_RD\_INT: Triggered when the HP CPU0 Peripheral bus reads in HP CPU0 region 1.

- ASSIST\_DEBUG\_CORE\_0\_AREA\_PIF\_1\_WR\_INT: Triggered when the HP CPU0 Peripheral bus writes in HP CPU0 region 1.
- ASSIST\_DEBUG\_CORE\_0\_SP\_SPILL\_MIN\_INT: Triggered when the HP CPU0 SP goes below the lower bound of the HP CPU0 SP monitored region.
- ASSIST\_DEBUG\_CORE\_0\_SP\_SPILL\_MAX\_INT: Triggered when the HP CPU0 SP goes beyond the upper bound of the HP CPU0 SP monitored region.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_RD\_INT: Triggered when the HP CPU1 Data bus reads in HP CPU1 region 0.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_WR\_INT: Triggered when the HP CPU1 Data bus writes in HP CPU1 region 0.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_RD\_INT: Triggered when the HP CPU1 Data bus reads in HP CPU1 region 1.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_WR\_INT: Triggered when the HP CPU1 Data bus writes in HP CPU1 region 1.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_RD\_INT: Triggered when the HP CPU1 Peripheral bus reads in HP CPU1 region 0.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_WR\_INT: Triggered when the HP CPU1 Peripheral bus writes in HP CPU1 region 0.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_RD\_INT: Triggered when the HP CPU1 Peripheral bus reads in HP CPU1 region 1.
- ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_WR\_INT: Triggered when the HP CPU1 Peripheral bus writes in HP CPU1 region 1.
- ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MIN\_INT: Triggered when the HP CPU1 SP goes below the lower bound of the HP CPU1 SP monitored region.
- ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MAX\_INT: Triggered when the HP CPU1 SP goes beyond the upper bound of the HP CPU1 SP monitored region.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [19.6 Register Summary](#).

## 19.5 Recommended Operation

### 19.5.1 Region Monitoring and SP Monitoring Configuration

The Debug Assistant module can monitor reads and writes performed by the Data bus and Peripheral bus of HP CPU0 and HP CPU1. Two memory regions on each bus can be monitored at the same time. All the

monitoring modes supported by the Debug Assistant module are listed below:

- Monitoring the read/write operations performed by Data bus
  - HP CPU0 Data bus reads in HP CPU0 region 0
  - HP CPU0 Data bus writes in HP CPU0 region 0
  - HP CPU0 Data bus reads in HP CPU0 region 1
  - HP CPU0 Data bus writes in HP CPU0 region 1
  - HP CPU1 Data bus reads in HP CPU1 region 0
  - HP CPU1 Data bus writes in HP CPU1 region 0
  - HP CPU1 Data bus reads in HP CPU1 region 1
  - HP CPU1 Data bus writes in HP CPU1 region 1
- Monitoring the read/write operations performed by Peripheral bus
  - HP CPU0 Peripheral bus reads in HP CPU0 region 0
  - HP CPU0 Peripheral bus writes in HP CPU0 region 0
  - HP CPU0 Peripheral bus reads in HP CPU0 region 1
  - HP CPU0 Peripheral bus writes in HP CPU0 region 1
  - HP CPU1 Peripheral bus reads in HP CPU1 region 0
  - HP CPU1 Peripheral bus writes in HP CPU1 region 0
  - HP CPU1 Peripheral bus reads in HP CPU1 region 1
  - HP CPU1 Peripheral bus writes in HP CPU1 region 1
- Monitoring SP bounds violations
  - HP CPU0 SP goes beyond the upper bound of the HP CPU0 SP monitored region
  - HP CPU0 SP goes below the lower bound of the HP CPU0 SP monitored region
  - HP CPU1 SP goes beyond the upper bound of the HP CPU1 SP monitored region
  - HP CPU1 SP goes below the lower bound of the HP CPU1 SP monitored region

The configuration process for region monitoring and SP monitoring is as follows:

1. Configure the monitored region and SP bounds.

- Configure HP CPU0 Data bus region 0 with [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_0\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_0\\_MAX\\_REG](#).
- Configure HP CPU0 Data bus region 1 with [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_1\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_1\\_MAX\\_REG](#).
- Configure HP CPU0 Peripheral bus region 0 with [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_PIF\\_0\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_PIF\\_0\\_MAX\\_REG](#).
- Configure HP CPU0 Peripheral bus region 1 with [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_PIF\\_1\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_PIF\\_1\\_MAX\\_REG](#).

- Configure HP CPU0 SP bounds with [ASSIST\\_DEBUG\\_CORE\\_0\\_SP\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_0\\_SP\\_MAX\\_REG](#).
- Configure HP CPU1 Data bus region 0 with [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_0\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_0\\_MAX\\_REG](#).
- Configure HP CPU1 Data bus region 1 with [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_MAX\\_REG](#).
- Configure HP CPU1 Peripheral bus region 0 with [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_0\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_0\\_MAX\\_REG](#).
- Configure HP CPU1 Peripheral bus region 1 with [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_MAX\\_REG](#).
- Configure HP CPU1 SP bounds with [ASSIST\\_DEBUG\\_CORE\\_1\\_SP\\_MIN\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_SP\\_MAX\\_REG](#).

## 2. Configure interrupts.

- Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_INTR\\_ENA\\_REG](#) or [ASSIST\\_DEBUG\\_CORE\\_1\\_INTR\\_ENA\\_REG](#) to enable the interrupt of a monitoring mode.
- Read [ASSIST\\_DEBUG\\_CORE\\_0\\_INTR\\_RAW\\_REG](#) or [ASSIST\\_DEBUG\\_CORE\\_1\\_INTR\\_RAW\\_REG](#) to get the raw interrupt status of a monitoring mode.
- Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_INTR\\_CLR\\_REG](#) or [ASSIST\\_DEBUG\\_CORE\\_1\\_INTR\\_CLR\\_REG](#) to clear the interrupt of a monitoring mode.

## 3. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_MONTR\\_ENA\\_REG](#) or [ASSIST\\_DEBUG\\_CORE\\_1\\_MONTR\\_ENA\\_REG](#) to enable the monitoring mode(s). Various monitoring modes can be enabled at the same time.

Assuming that Debug Assistant module needs to monitor whether HP CPU0 Data bus has written to [A ~ B] address space, the user can enable monitoring in either HP CPU0 Data bus region 0 or region 1. The following configuration process is based on region 0:

1. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_RCD\\_PDEBUGEN](#) to 1 to enable HP CPU0 to update the PC signals to the Debug Assistant module.
2. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_0\\_MIN\\_REG](#) to Address A.
3. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_AREA\\_DRAMO\\_0\\_MAX\\_REG](#) to Address B.
4. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_INTR\\_ENA\\_REG](#) bit[1] to enable the interrupt for write operations by HP CPU0 Data bus in region 0.
5. Configure [ASSIST\\_DEBUG\\_CORE\\_0\\_MONTR\\_ENA\\_REG](#) bit[1] to enable monitoring write operations by HP CPU0 Data bus in region 0.
6. Configure interrupt matrix to map [ASSIST\\_DEBUG\\_INTR](#) into HP CPU0/1 interrupt (please refer to Chapter [11 Interrupt Matrix](#)).
7. After the interrupt is triggered:
  - Read [ASSIST\\_DEBUG\\_CORE\\_0\\_INTR\\_RAW\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_INTR\\_RAW\\_REG](#) to learn which operation triggered the interrupt.

- If the interrupt is triggered by HP CPU0 region monitoring, read [ASSIST\\_DEBUG\\_CORE\\_O\\_AREA\\_PC\\_REG](#) for the HP CPU0 PC value, and [ASSIST\\_DEBUG\\_CORE\\_O\\_AREA\\_SP\\_REG](#) for the HP CPU0 SP.
- If the interrupt is triggered by SP monitoring, read [ASSIST\\_DEBUG\\_CORE\\_O\\_SP\\_PC\\_REG](#) for the HP CPU0 PC value.
- Write 1 to the corresponding bits of [ASSIST\\_DEBUG\\_CORE\\_O\\_INTR\\_RAW\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_1\\_INTR\\_CLR\\_REG](#) to clear the interrupts.

## 19.5.2 PC Logging Configuration

Configure [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGEN](#) to 1 to enable HP CPU0 to update the PC signals to the Debug Assistant module. If [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_RECORDEN](#) is also configured to 1, [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGPC\\_REG](#) will record the HP CPU0's PC signal and [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGSP\\_REG](#) will record the HP CPU0 SP value. Otherwise, the two registers keep the original values.

When the HP CPU0 resets, [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_EN\\_REG](#) will reset, while [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGPC\\_REG](#) and [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGSP\\_REG](#) will not. Therefore, the two registers will keep the PC value and SP value at the HP CPU0 reset.

This is also the case for HP CPU1.

## 19.5.3 CPU/DMA Bus Access Logging Configuration

### 19.5.3.1 HP CPU0/1 Bus Access Logging Configuration

The configuration process for HP CPU0/1 bus access logging (SPM Monitor) is described below.

1. Configure monitored address space.
  - Configure [SPM\\_MEM\\_MONITOR\\_LOG\\_MIN\\_REG](#) and [SPM\\_MEM\\_MONITOR\\_LOG\\_MAX\\_REG](#) to specify monitored address space. The monitored address space should range from 0x3010\_0000 to 0x3010\_1FFF.
2. Configure the monitoring mode with [SPM\\_MEM\\_MONITOR\\_LOG\\_MODE](#):
  - Write monitoring (whether the bus has write operations)
  - Word monitoring (whether the bus writes a specific word)
  - Halfword monitoring (whether the bus writes a specific halfword)
  - Byte monitoring (whether the bus writes a specific byte)
3. Configure the specific values to be monitored.
  - In word monitoring mode, [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#) specifies the monitored word.
  - In halfword monitoring mode, [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#)[15:0] specifies the monitored halfword.
  - In byte monitoring mode, [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#)[7:0] specifies the monitored byte.

- [SPM\\_MEM\\_MONITOR\\_LOG\\_DATA\\_MASK\\_REG](#) is used to mask the byte specified in [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#). A masked byte can be any value. For example, in word monitoring, if [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#) is configured to 0x01020304 and [SPM\\_MEM\\_MONITOR\\_LOG\\_DATA\\_MASK\\_REG](#) is configured to 0x1, then any writes of the data matching the 0x010203XX pattern by the bus will be recorded.

#### 4. Configure the storage space for recorded data.

- [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) and [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_END\\_REG](#) specify the storage space for recorded data. The storage space must be in the range of 0x4080\_0000 ~ 0x4087\_FFFF.
- Set [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_ADDR\\_UPDATE\\_REG](#) to update the value in [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) to [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#).
- Configure the permission for the SPM Monitor function of Debug Assistant module to access the HP L2MEM. Only when the access permission is enabled can the Debug Assistant module access the HP L2MEM. For more information, please refer to [TEE\\_DMA\\_SPM\\_MON\\_PMS\\_W\\_REG](#) and other relevant registers in Chapter 18 *Permission Control (PMS)*.

#### 5. Configure the writing mode for the recorded data: loop mode or non-loop mode.

- In loop mode, writing to the specified address space is performed in loops. When writing reaches the end address, it will return to the starting address and continue, overwriting the previously recorded data. Set [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_LOOP\\_ENABLE](#) to enable loop mode. For example, there are 10 write operations (1 ~ 10) to address space 0 ~ 4 during bus access. After the 5th operation writes to address 4, the 6th operation will start writing from address 0. The 6th to 10th operations will overwrite the previous data written by the 1th to 5th operations.
- In non-loop mode, when writing reaches the end address, it will stop at the end address and dump the remaining data, not overwriting the previously recorded data. Clear [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_LOOP\\_ENABLE](#) to use non-loop mode. For example, there are 10 write operations (1 ~ 10) to address space 0 ~ 4 during bus access. After the 5th operation writes to address 4, the 6th to 10th write operations will stop at address 4 and will not be performed any more. Therefore, the address 0 ~ 4 stores the values written by the 1 ~ 5 operations and the values of the 6 ~ 10 operations are dumped.

#### 6. Configure bus enable registers.

- Enable HP CPU0 or HP CPU1 bus access logging with [SPM\\_MEM\\_MONITOR\\_LOG\\_CORE\\_ENA](#). They can be enabled at the same time.

The Debug Assistant module first writes the recorded data of HP CPU0 or HP CPU1 to the internal buffer A, and then fetches the data from the buffer and writes it to the configured memory space. When the monitored behaviors are triggered continuously, the generated recording packets may fully occupy the buffer, making it unable to take any incoming packets. At this time, the module dumps these incoming packets and buffers a HP CPU LOST packet instead before the buffer reaches its capacity. However, it is only possible to know the bus type of the dumped packets when the HP CPU LOST packet was generated, but not the number of the dumped packets before the generation.

When bus access logging is finished, the recorded data can be read from memory for decoding. The recorded data is in three packet formats, namely HP CPU0 packet (corresponding to HP CPU0 Data bus), HP

CPU1 packet (corresponding to HP CPU1 Data bus), and HP CPU LOST packet. The packet formats are shown in Table 19.5-1 and 19.5-2.

**Table 19.5-1. HP CPU0/1 Packet Format**

| Bit[63:33] | Bit[32]      | Bit[31:3]   | Bit[2:1] | Bit[0]       |
|------------|--------------|-------------|----------|--------------|
| pc_offset  | anchored (1) | addr_offset | format   | anchored (0) |

**Table 19.5-2. HP CPU LOST Packet Format**

| Bit[31:7] | Bit[6:3]    | Bit[2:1] | Bit[0]       |
|-----------|-------------|----------|--------------|
| reserved  | lost_source | format   | anchored (0) |

It can be seen from the data packet formats that the size of the HP CPU0/1 packet is 64 bits and that of the HP CPU LOST packet is 32 bits. These packets contain the following fields:

- **format** – the packet type. 0: HP CPU0 packet; 1: HP CPU1 packet; 2: HP CPU LOST packet; 3: Reserved.
- **pc\_offset** - the offset of the HP CPU0/1 PC register at the time of access. Actual PC = pc\_offset + 0x0000\_0000.
- **addr\_offset** - the address offset of a write operation. Actual address = addr\_offset + [SPM\\_MEM\\_MONITOR\\_LOG\\_MIN\\_REG](#)[31:4], 4'h0.
- **lost\_source** - the dumped packets when the HP CPU LOST packet was generated.
  - Bit[4:3]: 0 indicates HP CPU0 packets were not dumped. 3 indicates HP CPU0 packets were dumped. Other values are reserved.
  - Bit[6:5]: 0 indicates HP CPU1 packets were not dumped. 3 indicates HP CPU1 packets were dumped. Other values are reserved.
- **anchored** - the location of the 32 bits in the data packet. 0: Lower 32 bits. 1: Higher 32 bits.

The internal buffer of the module is 32 bits wide. When the HP CPU0 and HP CPU1 bus access loggings are both enabled and the record data is generated at the same time, the HP CPU0 data packets are first buffered, then the HP CPU1 packets. The Debug Assistant will automatically fetch the buffered data and store it in 32-bit data width into the specified memory space.

In loop mode, data looping several times in the storage memory may cause residual data, which can interfere with packet parsing. For example, the lower 32 bits of a HP CPU0/1 packet are overwritten, thus making its higher 32 bits residual data. Therefore, users need to filter out the possible residual data in order to determine the starting position of the first valid packet with [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#). Once the starting position of the packet is identified, check the anchored bit value of the packet. If it is 0, the data will be retained. If it is 1, it will be dumped.

The process of packet parsing is described below:

- Determine whether there is a data overflow with [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_FULL\\_FLAG](#).
  - If no, the address space to read is [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) ~ [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) - 4.



- If yes and the loop mode is enabled, the address space is  
`SPM_MEM_MONITOR_LOG_MEM_CURRENT_ADDR_REG ~`  
`SPM_MEM_MONITOR_LOG_MEM_END_REG` and `SPM_MEM_MONITOR_LOG_MEM_START_REG ~`  
`SPM_MEM_MONITOR_LOG_MEM_CURRENT_ADDR_REG - 4`.
- If yes and loop mode is not enabled, the address space is  
`SPM_MEM_MONITOR_LOG_MEM_START_REG ~ SPM_MEM_MONITOR_LOG_MEM_END_REG`.

- Read and parse data from the starting address. Read 32 bits each time.

After packet parsing is completed, clear the `SPM_MEM_MONITOR_LOG_MEM_FULL_FLAG` flag bit by setting `SPM_MEM_MONITOR_CLR_LOG_MEM_FULL_FLAG`.

### 19.5.3.2 DMA Bus Access Logging Configuration

The Debug Assistant module supports a total of four DMA bus channel groups, DMA\_0, DMA\_1, DMA\_2, and DMA\_3 channel groups. DMA\_0 and DMA\_1 channel groups are reserved and cannot be used. The DMA bus for the DMA\_2 channel group is the bus on which the AXI matrix accesses the HP L2MEM. The DMA bus for the DMA\_3 channel group is the bus on which the AHB matrix accesses the HP L2MEM. For more information, see Chapter 6 *System and Memory* > Section 6.3.2. The configuration process for DMA bus access logging (L2MEM Monitor) is described below.

1. Configure monitored address space.
  - Configure `L2_MEM_MONITOR_LOG_MIN_REG` and `L2_MEM_MONITOR_LOG_MAX_REG` to specify monitored address space. The monitored address space should range from `0x4FF0_0000` to `0x4FFB_FFFF` or from `0x8FF0_0000` to `0x8FFB_FFFF`.
2. Configure the monitoring mode with `L2_MEM_MONITOR_LOG_MODE`:
  - Write monitoring (whether the bus has write operations)
  - Word monitoring (whether the bus writes a specific word)
  - Halfword monitoring (whether the bus writes a specific halfword)
  - Byte monitoring (whether the bus writes a specific byte)
3. Configure the specific values to be monitored.
  - In word monitoring mode, `L2_MEM_MONITOR_LOG_CHECK_DATA_REG` specifies the monitored word.
  - In halfword monitoring mode, `L2_MEM_MONITOR_LOG_CHECK_DATA_REG[15:0]` specifies the monitored halfword.
  - In byte monitoring mode, `L2_MEM_MONITOR_LOG_CHECK_DATA_REG[7:0]` specifies the monitored byte.
  - `L2_MEM_MONITOR_LOG_DATA_MASK_REG` is used to mask the byte specified in `L2_MEM_MONITOR_LOG_CHECK_DATA_REG`. A masked byte can be any value. For example, in word monitoring, if `L2_MEM_MONITOR_LOG_CHECK_DATA_REG` is configured to `0x01020304` and `L2_MEM_MONITOR_LOG_DATA_MASK_REG` is configured to `0x1`, then any writes of the data matching the `0x010203XX` pattern by the bus will be recorded.
4. Configure the storage space for recorded data.

- [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) and [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_END\\_REG](#) specify the storage space for recorded data. The storage space must be in the range of 0x4080\_0000 ~ 0x4087\_FFFF.
- Set [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_ADDR\\_UPDATE\\_REG](#) to update the value in [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) to [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#).
- Configure the permission for the L2MEM Monitor function of Debug Assistant module to access the HP L2MEM. Only when the access permission is enabled can the Debug Assistant module access the HP L2MEM. For more information, please refer to [TEE\\_DMA\\_L2MEM\\_MON\\_PMS\\_W\\_REG](#) and other relevant registers in Chapter 18 *Permission Control (PMS)*.

5. Configure the writing mode for the recorded data: loop mode or non-loop mode.

- In loop mode, writing to the specified address space is performed in loops. When writing reaches the end address, it will return to the starting address and continue, overwriting the previously recorded data. Set [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_LOOP\\_ENABLE](#) to enable loop mode. For example, there are 10 write operations (1 ~ 10) to address space 0 ~ 4 during bus access. After the 5th operation writes to address 4, the 6th operation will start writing from address 0. The 6th to 10th operations will overwrite the previous data written by the 1th to 5th operations.
- In non-loop mode, when writing reaches the end address, it will stop at the end address and dump the remaining data, not overwriting the previously recorded data. Clear [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_LOOP\\_ENABLE](#) to use non-loop mode. For example, there are 10 write operations (1 ~ 10) to address space 0 ~ 4 during bus access. After the 5th operation writes to address 4, the 6th to 10th write operations will stop at address 4 and will not be performed any more. Therefore, the address 0 ~ 4 stores the values written by the 1 ~ 5 operations and the values of the 6 ~ 10 operations are dumped.
- See the example in [19.5.3.1](#) > step 5.

6. Configure bus enable registers.

- Enable DMA\_2 and DMA\_3 channel groups bus access logging with [L2\\_MEM\\_MONITOR\\_LOG\\_DMA\\_2\\_ENA](#) and [L2\\_MEM\\_MONITOR\\_LOG\\_DMA\\_3\\_ENA](#) respectively. They can be enabled at the same time.

The Debug Assistant module first writes the DMA recorded data to the internal buffer B, and then fetches the data from the buffer and writes it to the configured memory space. When the monitored behaviors are triggered continuously, the generated recording packets may fully occupy the buffer, making it unable to take any incoming packets. At this time, the module dumps these incoming packets and buffers a DMA LOST packet instead before the buffer reaches its capacity. However, it is only possible to know the bus type of the dumped packets when the DMA LOST packet was generated, but not the number of the dumped packets before the generation.

When bus access logging is finished, the recorded data can be read from memory for decoding. The recorded data is in three packet formats, namely DMA\_2 packet (corresponding to DMA\_2 Data bus), DMA\_3 packet (corresponding to DMA\_3 Data bus), and DMA LOST packet. The packet formats are shown in Table [19.5-3](#), [19.5-4](#), and [19.5-5](#).

Table 19.5-3. DMA\_2 Packet Format

| Bit[31:9]    | Bit[8:4] | Bit[3:1] | Bit[0]       |
|--------------|----------|----------|--------------|
| addr_offset0 | reserved | format   | anchored (0) |

Table 19.5-4. DMA\_3 Packet Format

| Bit[31:9]    | Bit[8:4] | Bit[3:1] | Bit[0]       |
|--------------|----------|----------|--------------|
| addr_offset1 | reserved | format   | anchored (0) |

Table 19.5-5. DMA LOST Packet Format

| Bit[31:10] | Bit[9:8]    | Bit[7:4] | Bit[3:1] | Bit[0]       |
|------------|-------------|----------|----------|--------------|
| reserved   | lost_source | reserved | format   | anchored (0) |

It can be seen from the data packet formats that the size of the DMA\_2, DMA\_3, and DMA LOST packet is 32 bits. These packets contain the following fields:

- **format** – the packet type. 4: DMA\_2 packet; 5: DMA\_3 packet; 6: DMA LOST packet; other values: Reserved.
- **addr\_offset0** - the address offset of a write operation. Actual address = addr\_offset0 + [L2\\_MEM\\_MONITOR\\_LOG\\_MIN\\_REG](#)[31:5], 5'h0.
- **addr\_offset1** - the address offset of a write operation. Actual address = addr\_offset1 + [L2\\_MEM\\_MONITOR\\_LOG\\_MIN\\_REG](#)[31:2], 2'h0.
- **lost\_source** - the dumped packets when the DMA LOST packet was generated.
  - Bit[8]: 0 indicates DMA\_2 packets were not dumped. 1 indicates DMA\_2 packets were dumped.
  - Bit[9]: 0 indicates DMA\_3 packets were not dumped. 1 indicates DMA\_3 packets were dumped.
- **anchored** - the location of the 32 bits in the data packet. 0: Lower 32 bits. 1: Higher 32 bits.

The internal buffer of the module is 32 bits wide. When the bus access loggings of DMA\_2 and DMA\_3 channel groups are both enabled and the record data is generated at the same time, the DMA\_2 data packets are first buffered, then the DMA\_3 packets. The Debug Assistant will automatically fetch the buffered data and store it in 32-bit data width into the specified memory space.

The process of packet parsing is described below:

- Determine whether there is a data overflow with [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_FULL\\_FLAG](#).
  - If no, the address space to read is [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) ~ [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) - 4.
  - If yes and the loop mode is enabled, the address space is [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) ~ [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_END\\_REG](#) and [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) ~ [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_CURRENT\\_ADDR\\_REG](#) - 4.
  - If yes and loop mode is not enabled, the address space is [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_START\\_REG](#) ~ [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_END\\_REG](#).

- Read and parse data from the starting address. Read 32 bits each time.

After packet parsing is completed, clear the [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_FULL\\_FLAG](#) flag bit by setting [L2\\_MEM\\_MONITOR\\_CLR\\_LOG\\_MEM\\_FULL\\_FLAG](#).

## 19.6 Register Summary

The addresses of **HP CPU bus logging configuration registers** (see 19.6.1) in this section are relative to the **SPM Monitor** base address. The addresses of **DMA bus logging configuration registers** (see 19.6.2) in this section are relative to the **L2MEM Monitor** base address. The addresses of other registers (see 19.6.3) are relative to the **Bus Monitor** base address. All base addresses are provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

### 19.6.1 HP CPU Bus Logging Configuration Register Summary

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>HP CPU bus logging configuration registers</b>        |  |         |        |
| <a href="#">SPM_MEM_MONITOR_LOG_SETTING_REG</a>          | Configures bus access logging  | 0x0000  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_CHECK_DATA_REG</a>       | Configures monitored data in bus access logging                                      | 0x0008  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_DATA_MASK_REG</a>        | Configures masked data in bus access logging   | 0x000C  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_MIN_REG</a>              | Configures monitored address space in bus access logging                             | 0x0010  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_MAX_REG</a>              | Configures monitored address space in bus access logging                             | 0x0014  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_MEM_START_REG</a>        | Configures the starting address of the memory for recorded data                      | 0x0018  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_MEM_END_REG</a>          | Configures the end address of the memory for recorded data                           | 0x001C  | R/W    |
| <a href="#">SPM_MEM_MONITOR_LOG_MEM_CURRENT_ADDR_REG</a> | Represents the address for the next write  | 0x0020  | RO     |
| <a href="#">SPM_MEM_MONITOR_LOG_MEM_ADDR_UPDATE_REG</a>  | Updates the address for the next write to the starting address for the recorded data | 0x0024  | WT     |
| <a href="#">SPM_MEM_MONITOR_LOG_MEM_FULL_FLAG_REG</a>    | Represents the logging overflow status   | 0x0028  | varies |
| <b>Clock control register</b>                            |  |         |        |
| <a href="#">SPM_MEM_MONITOR_CLOCK_GATE_REG</a>           | Clock control register   | 0x002C  | R/W    |
| <b>Version control register</b>                          |  |         |        |
| <a href="#">SPM_MEM_MONITOR_DATE_REG</a>                 | Version control register   | 0x03FC  | R/W    |

### 19.6.2 DMA Bus Logging Configuration Register Summary

| Name   | Description | Address | Access |
|--|-------------|---------|--------|
| <b>DMA bus logging configuration registers</b> |             |         |        |

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">L2_MEM_MONITOR_LOG_SETTING_REG</a>          | Configures bus access logging  | 0x0000  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_SETTING1_REG</a>         | Configures bus access logging  | 0x0004  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_CHECK_DATA_REG</a>       | Configures monitored data in bus access logging                                      | 0x0008  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_DATA_MASK_REG</a>        | Configures masked data in bus access logging   | 0x000C  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_MIN_REG</a>              | Configures monitored address space in bus access logging                             | 0x0010  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_MAX_REG</a>              | Configures monitored address space in bus access logging                             | 0x0014  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_MEM_START_REG</a>        | Configures the starting address of the memory for recorded data                      | 0x0018  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_MEM_END_REG</a>          | Configures the end address of the memory for recorded data                           | 0x001C  | R/W    |
| <a href="#">L2_MEM_MONITOR_LOG_MEM_CURRENT_ADDR_REG</a> | Represents the address for the next write  | 0x0020  | RO     |
| <a href="#">L2_MEM_MONITOR_LOG_MEM_ADDR_UPDATE_REG</a>  | Updates the address for the next write to the starting address for the recorded data | 0x0024  | WT     |
| <a href="#">L2_MEM_MONITOR_LOG_MEM_FULL_FLAG_REG</a>    | Represents the logging overflow status   | 0x0028  | varies |
| <b>Clock control register</b>                           |  |         |        |
| <a href="#">L2_MEM_MONITOR_CLOCK_GATE_REG</a>           | Clock control register   | 0x002C  | R/W    |
| <b>Version control register</b>                         |  |         |        |
| <a href="#">L2_MEM_MONITOR_DATE_REG</a>                 | Version control register   | 0x03FC  | R/W    |

### 19.6.3 Summary of Other Registers

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Monitor configuration registers</b>                   |  |         |        |
| <a href="#">ASSIST_DEBUG_CORE_O_MONTR_ENA_REG</a>        | Configures whether to enable HP CPU0 monitoring                              | 0x0000  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_MIN_REG</a> | Configures the lower bound address of region 0 monitored on HP CPU0 Data bus | 0x0010  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_MAX_REG</a> | Configures the upper bound address of region 0 monitored on HP CPU0 Data bus | 0x0014  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_MIN_REG</a> | Configures the lower bound address of region 1 monitored on HP CPU0 Data bus | 0x0018  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_MAX_REG</a> | Configures the upper bound address of region 1 monitored on HP CPU0 Data bus       | 0x001C  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_PIF_O_MIN_REG</a>   | Configures the lower bound address of region 0 monitored on HP CPU0 Peripheral bus | 0x0020  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_PIF_O_MAX_REG</a>   | Configures the upper bound address of region 0 monitored on HP CPU0 Peripheral bus | 0x0024  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_PIF_1_MIN_REG</a>   | Configures the lower bound address of region 1 monitored on HP CPU0 Peripheral bus | 0x0028  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_PIF_1_MAX_REG</a>   | Configures the upper bound address of region 1 monitored on HP CPU0 Peripheral bus | 0x002C  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_PC_REG</a>          | Represents the PC status under HP CPU0 region monitoring                           | 0x0030  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_O_AREA_SP_REG</a>          | Represents the SP status under HP CPU0 region monitoring                           | 0x0034  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_O_SP_MIN_REG</a>           | Configures the lower bound address of the HP CPU0 SP monitored region              | 0x0038  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_SP_MAX_REG</a>           | Configures the upper bound address of the HP CPU0 SP monitored region              | 0x003C  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_O_SP_PC_REG</a>            | Represents the PC status under HP CPU0 SP monitoring                               | 0x0040  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_MONTR_ENA_REG</a>        | Configures whether to enable HP CPU1 monitoring                                    | 0x0080  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_DRAMO_O_MIN_REG</a> | Configures the lower bound address of region 0 monitored on HP CPU1 Data bus       | 0x0090  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_DRAMO_O_MAX_REG</a> | Configures the upper bound address of region 0 monitored on HP CPU1 Data bus       | 0x0094  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_MIN_REG</a> | Configures the lower bound address of region 1 monitored on HP CPU1 Data bus       | 0x0098  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_MAX_REG</a> | Configures the upper bound address of region 1 monitored on HP CPU1 Data bus       | 0x009C  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_PIF_O_MIN_REG</a>   | Configures the lower bound address of region 0 monitored on HP CPU1 Peripheral bus | 0x00A0  | R/W    |

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_PIF_0_MAX_REG</a>          | Configures the upper bound address of region 0 monitored on HP CPU1 Peripheral bus | 0x00A4  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_PIF_1_MIN_REG</a>          | Configures the lower bound address of region 1 monitored on HP CPU1 Peripheral bus | 0x00A8  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_PIF_1_MAX_REG</a>          | Configures the upper bound address of region 1 monitored on HP CPU1 Peripheral bus | 0x00AC  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_PC_REG</a>                 | Represents the PC status under HP CPU1 region monitoring                           | 0x00B0  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_AREA_SP_REG</a>                 | Represents the SP status under HP CPU1 region monitoring                           | 0x00B4  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_SP_MIN_REG</a>                  | Configures the lower bound address of the HP CPU1 SP monitored region              | 0x00B8  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_SP_MAX_REG</a>                  | Configures the upper bound address of the HP CPU1 SP monitored region              | 0x00BC  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_SP_PC_REG</a>                   | Represents the PC status under HP CPU1 SP monitoring                               | 0x00C0  | RO     |
| <b>Interrupt configuration registers</b>                        |  |         |        |
| <a href="#">ASSIST_DEBUG_CORE_0_INTR_RAW_REG</a>                | HP CPU0 raw interrupt status register  | 0x0004  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_0_INTR_ENA_REG</a>                | HP CPU0 interrupt enable register  | 0x0008  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_0_INTR_CLR_REG</a>                | HP CPU0 interrupt clear register   | 0x000C  | WT     |
| <a href="#">ASSIST_DEBUG_CORE_1_INTR_RAW_REG</a>                | HP CPU1 raw interrupt status register  | 0x0084  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_INTR_ENA_REG</a>                | HP CPU1 interrupt enable register  | 0x0088  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_INTR_CLR_REG</a>                | HP CPU1 interrupt clear register   | 0x008C  | WT     |
| <b>PC logging configuration register</b>                        |  |         |        |
| <a href="#">ASSIST_DEBUG_CORE_0_RCD_EN_REG</a>                  | HP CPU0 PC logging enable register   | 0x0044  | R/W    |
| <a href="#">ASSIST_DEBUG_CORE_1_RCD_EN_REG</a>                  | HP CPU1 PC logging enable register   | 0x00C4  | R/W    |
| <b>PC logging status registers</b>                              |  |         |        |
| <a href="#">ASSIST_DEBUG_CORE_0_RCD_PDEBUGPC_REG</a>            | HP CPU0 PC logging register  | 0x0048  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_0_RCD_PDEBUGSP_REG</a>            | HP CPU0 SP logging register  | 0x004C  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_RCD_PDEBUGPC_REG</a>            | HP CPU1 PC logging register  | 0x00C8  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_RCD_PDEBUGSP_REG</a>            | HP CPU1 SP logging register  | 0x00CC  | RO     |
| <b>CPU status registers</b>                                     |  |         |        |
| <a href="#">ASSIST_DEBUG_CORE_0_LASTPC_BEFORE_EXCEPTION_REG</a> | PC of the last command before HP CPU0 enters exception                             | 0x0070  | RO     |



| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">ASSIST_DEBUG_CORE_0_DEBUG_MODE_REG</a>              | HP CPU0 debug mode status register                     | 0x0074  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_LASTPC_BEFORE_EXCEPTION_REG</a> | PC of the last command before HP CPU1 enters exception | 0x00F0  | RO     |
| <a href="#">ASSIST_DEBUG_CORE_1_DEBUG_MODE_REG</a>              | HP CPU1 debug mode status register                     | 0x00F4  | RO     |
| <b>Clock control register</b>                                   |  |         |        |
| <a href="#">ASSIST_DEBUG_CLOCK_GATE_REG</a>                     | Clock control register                                 | 0x0108  | R/W    |
| <b>Version control register</b>                                 |  |         |        |
| <a href="#">ASSIST_DEBUG_DATE_REG</a>                           | Version control register                               | 0x03FC  | R/W    |



Register 19.1. SPM\_MEM\_MONITOR\_LOG\_SETTING\_REG (0x0000)

Continued from the previous page...

**SPM\_MEM\_MONITOR\_LOG\_CORE\_ENA** Configures whether to enable HP CPU0 or HP CPU1 bus access logging.

bit[0]: Configures whether to enable HP CPU0 bus access logging.

0: Disable

1: Enable

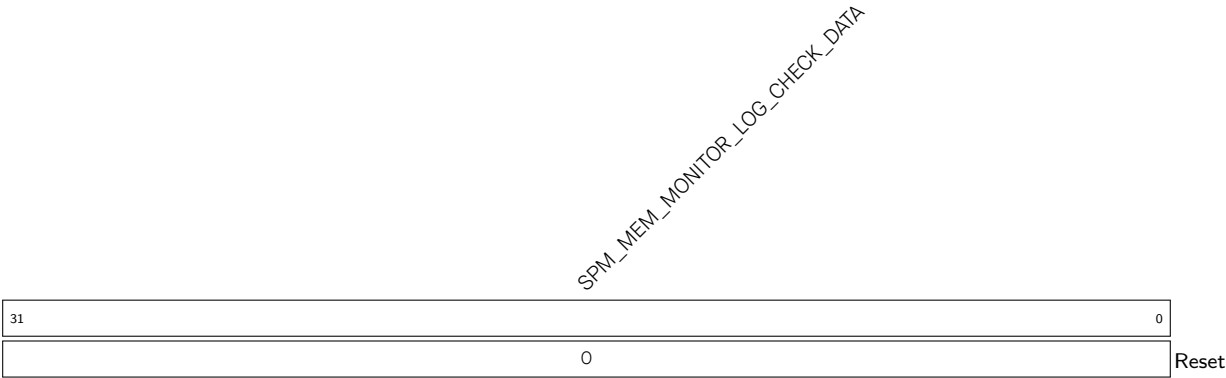
bit[1]: Configures whether to enable HP CPU1 bus access logging.

0: Disable

1: Enable

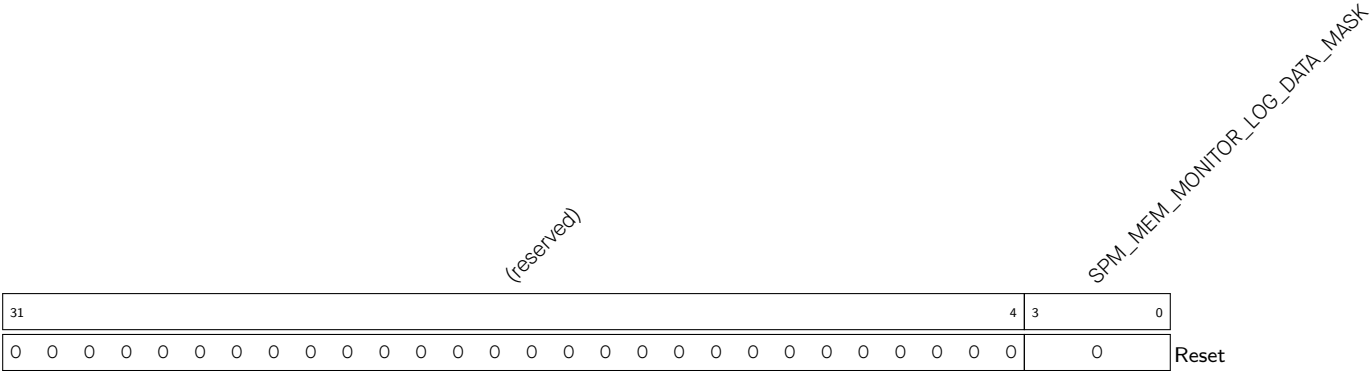
(R/W)

Register 19.2. SPM\_MEM\_MONITOR\_LOG\_CHECK\_DATA\_REG (0x0008)



**SPM\_MEM\_MONITOR\_LOG\_CHECK\_DATA** Configures the data to be monitored during bus access-  
ing. (R/W)

Register 19.3. SPM\_MEM\_MONITOR\_LOG\_DATA\_MASK\_REG (0x000C)



**SPM\_MEM\_MONITOR\_LOG\_DATA\_MASK** Configures which byte(s) in [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#) to mask.

bit[0]: Configures whether to mask the least significant byte of [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

bit[1]: Configures whether to mask the second least significant byte of [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

bit[2]: Configures whether to mask the second most significant byte of [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

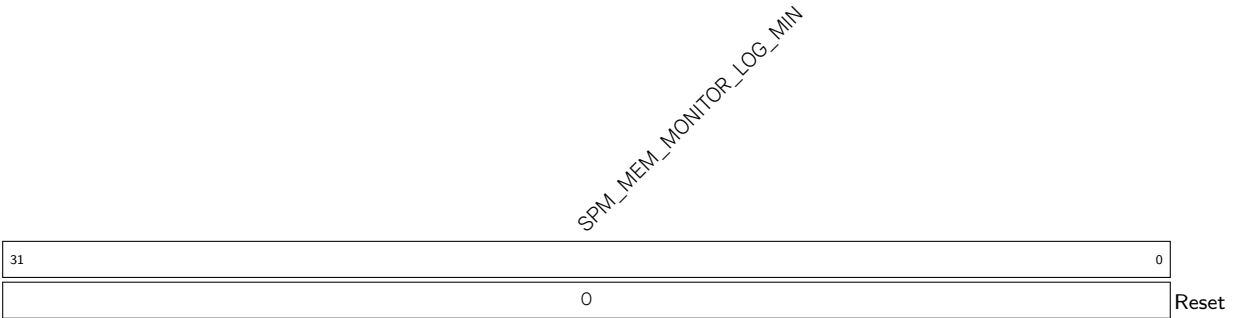
bit[3]: Configures whether to mask the most significant byte of [SPM\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

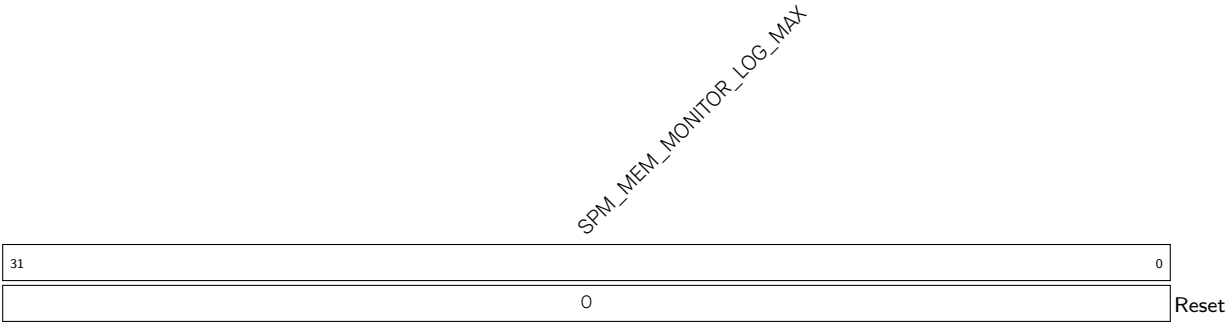
(R/W)

Register 19.4. SPM\_MEM\_MONITOR\_LOG\_MIN\_REG (0x0010)



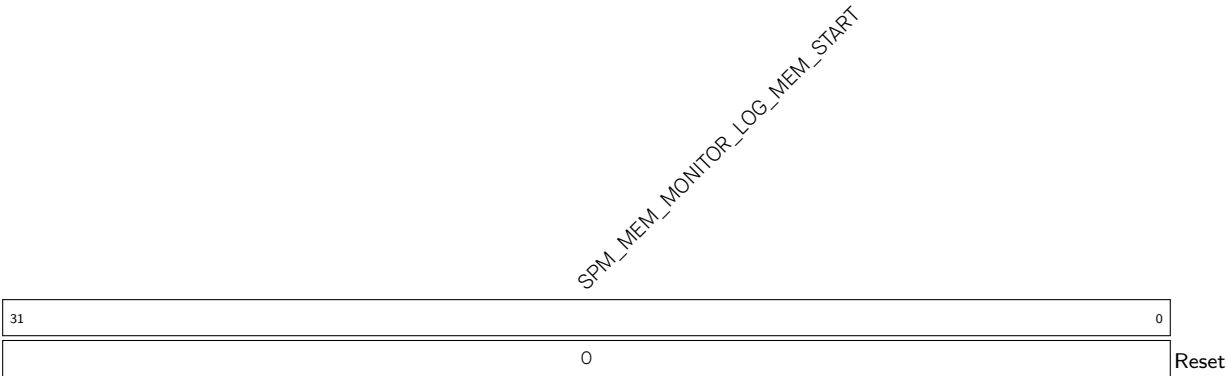
**SPM\_MEM\_MONITOR\_LOG\_MIN** Configures the lower bound address of the monitored address space. (R/W)

Register 19.5. SPM\_MEM\_MONITOR\_LOG\_MAX\_REG (0x0014)



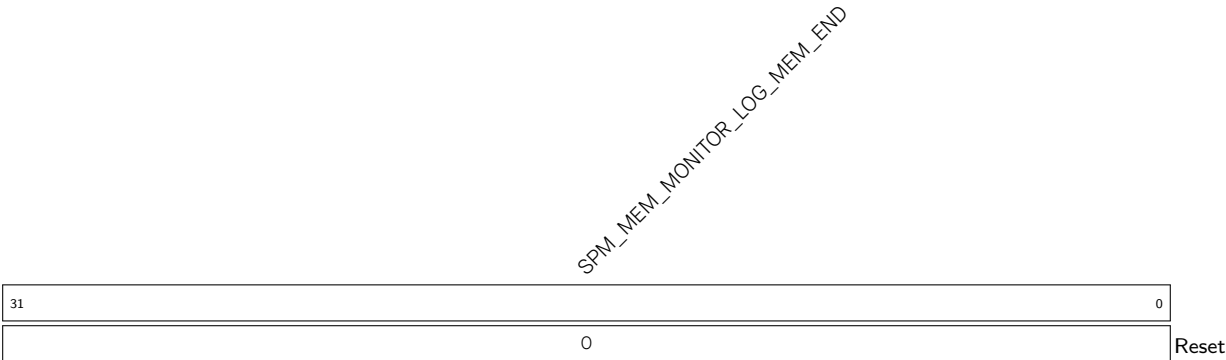
**SPM\_MEM\_MONITOR\_LOG\_MAX** Configures the upper bound address of the monitored address space. (R/W)

Register 19.6. SPM\_MEM\_MONITOR\_LOG\_MEM\_START\_REG (0x0018)



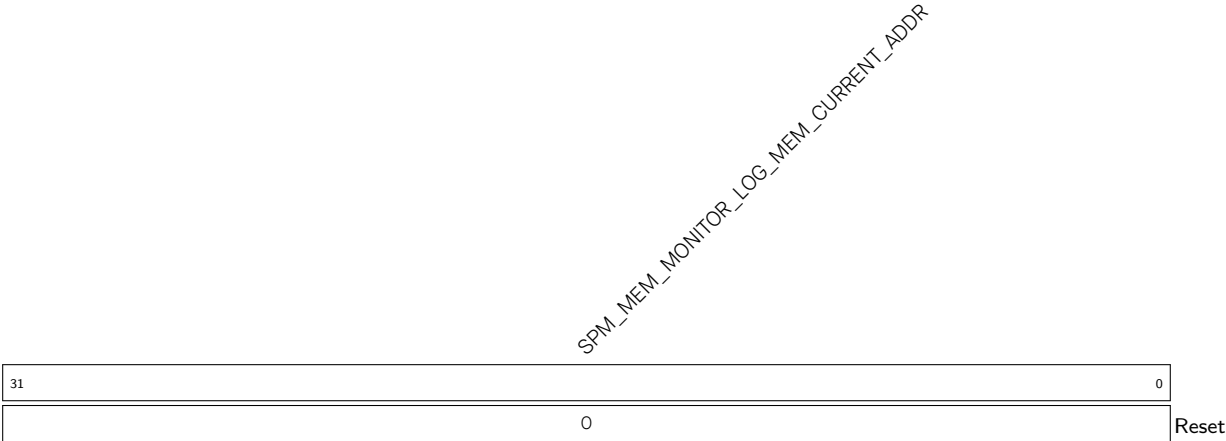
**SPM\_MEM\_MONITOR\_LOG\_MEM\_START** Configures the starting address of the storage space for recorded data. (R/W)

Register 19.7. SPM\_MEM\_MONITOR\_LOG\_MEM\_END\_REG (0x001C)



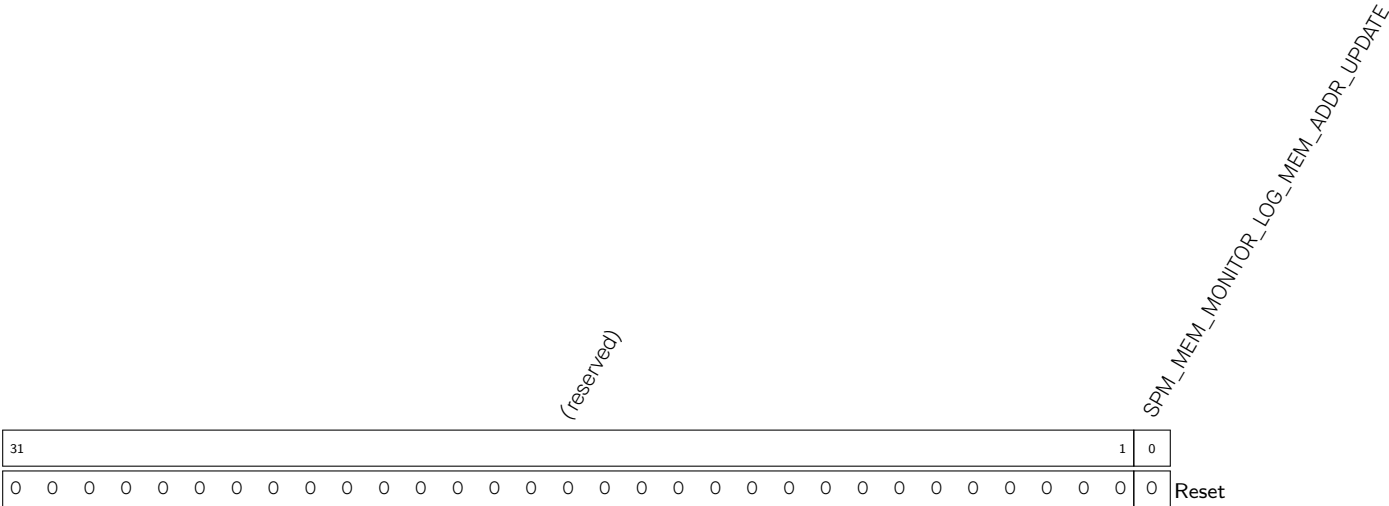
**SPM\_MEM\_MONITOR\_LOG\_MEM\_END** Configures the ending address of the storage space for recorded data. (R/W)

Register 19.8. SPM\_MEM\_MONITOR\_LOG\_MEM\_CURRENT\_ADDR\_REG (0x0020)



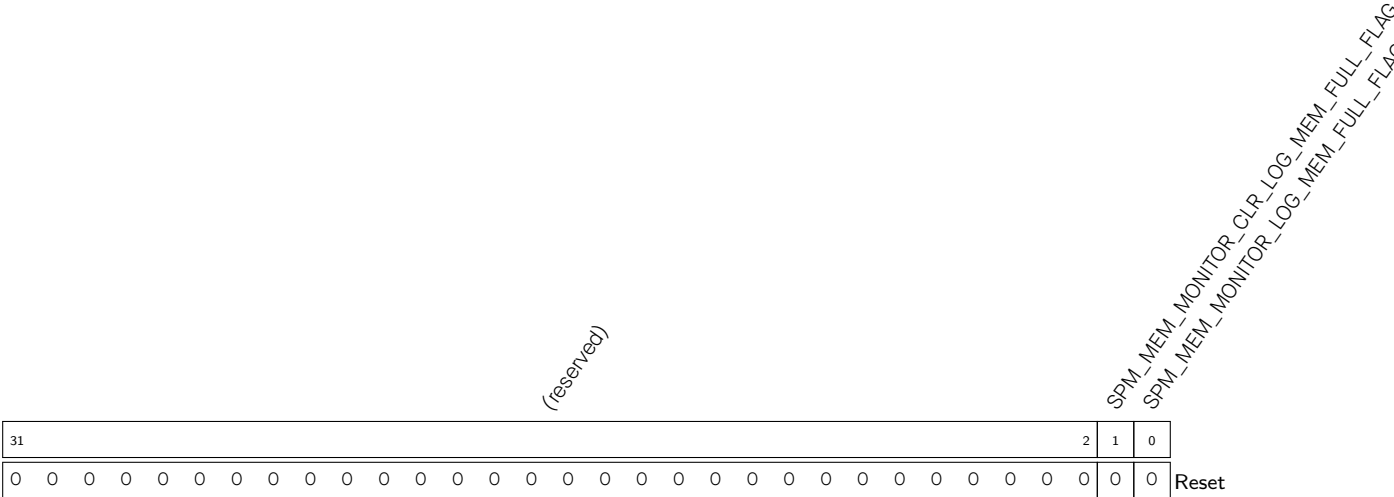
`SPM_MEM_MONITOR_LOG_MEM_CURRENT_ADDR` Represents the address of the next write.  
(RO)

Register 19.9. SPM\_MEM\_MONITOR\_LOG\_MEM\_ADDR\_UPDATE\_REG (0x0024)



`SPM_MEM_MONITOR_LOG_MEM_ADDR_UPDATE` Configures whether to update the value in `SPM_MEM_MONITOR_LOG_MEM_START_REG` to `SPM_MEM_MONITOR_LOG_MEM_CURRENT_ADDR_REG`.  
1: Update  
0: Not update  
(WT)

Register 19.10. SPM\_MEM\_MONITOR\_LOG\_MEM\_FULL\_FLAG\_REG (0x0028)



**SPM\_MEM\_MONITOR\_LOG\_MEM\_FULL\_FLAG** Represents whether data overflows the storage space.

0: Not overflow

1: Overflow

(RO)

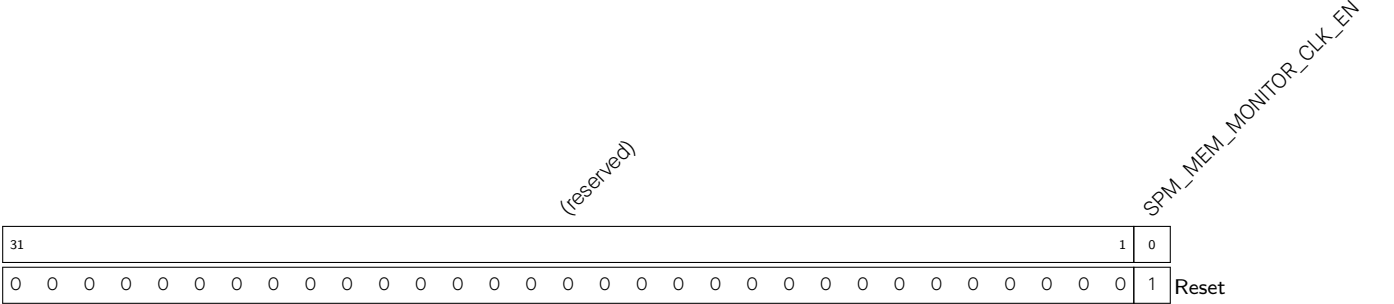
**SPM\_MEM\_MONITOR\_CLR\_LOG\_MEM\_FULL\_FLAG** Configures whether to clear the [SPM\\_MEM\\_MONITOR\\_LOG\\_MEM\\_FULL\\_FLAG](#) flag bit.

0: Not clear (default)

1: Clear

(WT)

Register 19.11. SPMMEM\_MONITOR\_CLOCK\_GATE\_REG (0x002C)



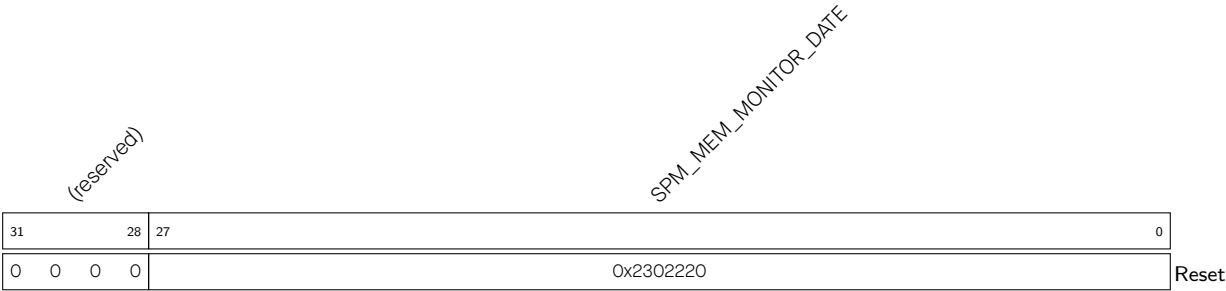
**SPM\_MEM\_MONITOR\_CLK\_EN** Configures whether to enable the register clock gating.

0: Disable

1: Enable

(R/W)

Register 19.12. SPM\_MEM\_MONITOR\_DATE\_REG (0x03FC)

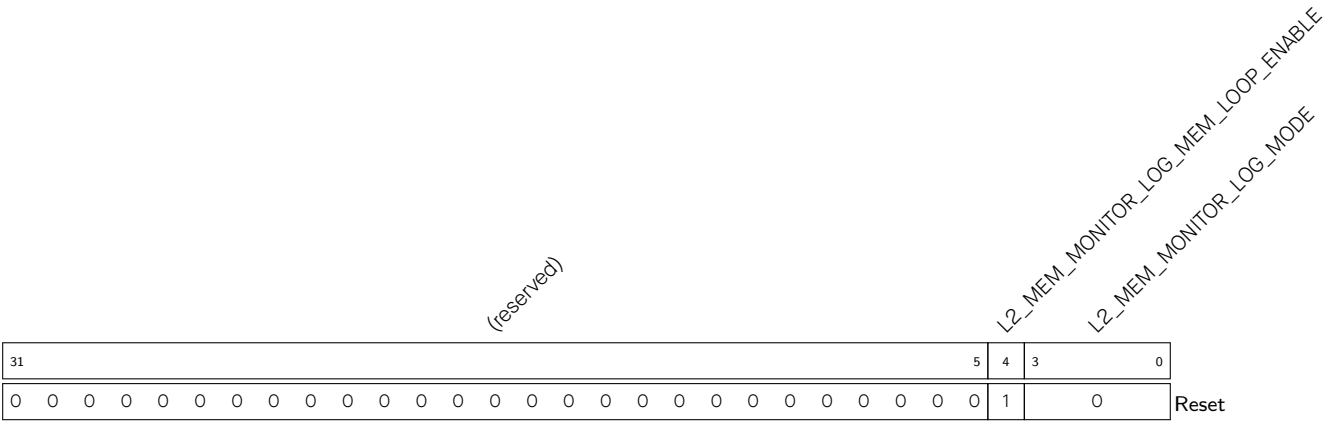


SPM\_MEM\_MONITOR\_DATE   Version control register. (R/W)



19.7.2   DMA Bus Logging Configuration Registers

Register 19.13. L2\_MEM\_MONITOR\_LOG\_SETTING\_REG (0x0000)



**L2\_MEM\_MONITOR\_LOG\_MODE**   Configures monitoring modes.

bit[0]: Configures write monitoring.

- 0: Disable
- 1: Enable

bit[1]: Configures word monitoring.

- 0: Disable
- 1: Enable

bit[2]: Configures halfword monitoring.

- 0: Disable
- 1: Enable

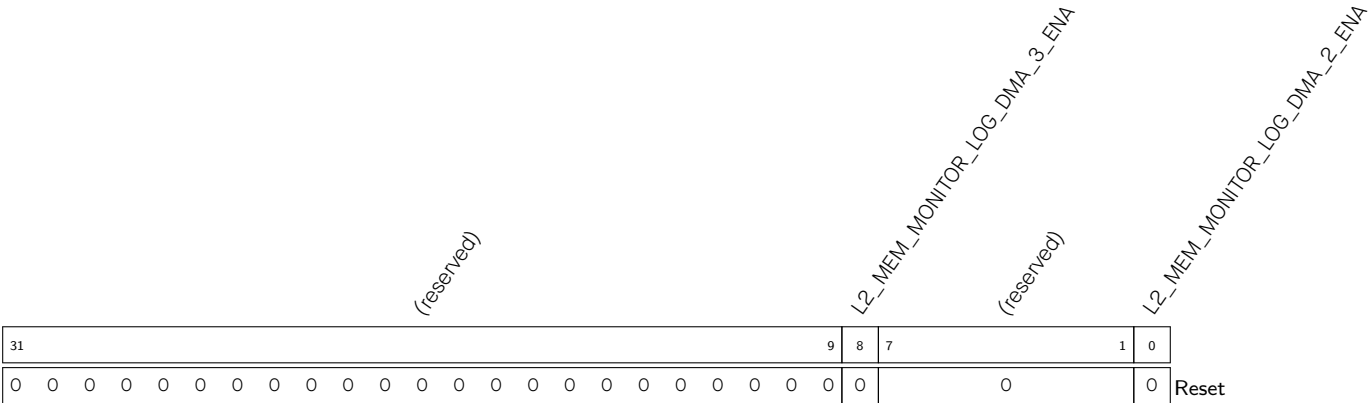
bit[3]: Configures byte monitoring.

- 0: Disable
  - 1: Enable
- (R/W)

**L2\_MEM\_MONITOR\_LOG\_MEM\_LOOP\_ENABLE**   Configures the writing mode for recorded data.

- 1: Loop mode
  - 0: Non-loop mode
- (R/W)

Register 19.14. L2\_MEM\_MONITOR\_LOG\_SETTING1\_REG (0x0004)



**L2\_MEM\_MONITOR\_LOG\_DMA\_2\_ENA** Configures whether to enable DMA\_2 bus access logging.

- 0: Disable
- 1: Enable

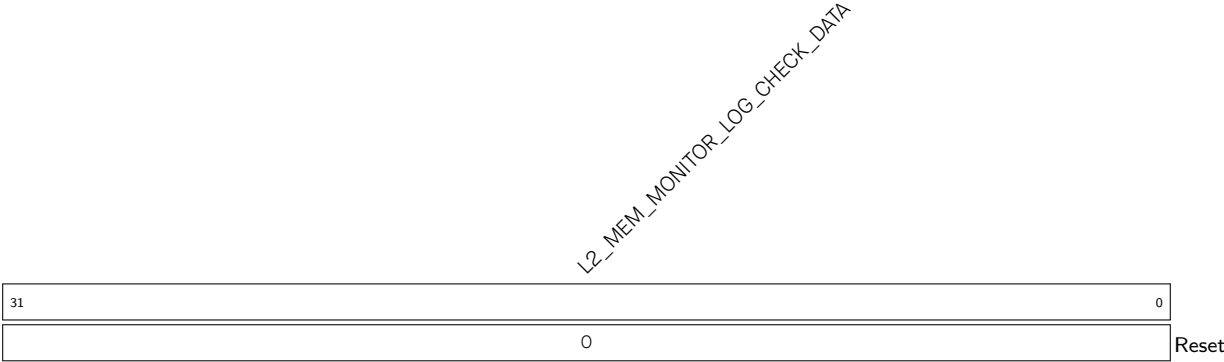
(R/W)

**L2\_MEM\_MONITOR\_LOG\_DMA\_3\_ENA** Configures whether to enable DMA\_3 bus access logging.

- 0: Disable
- 1: Enable

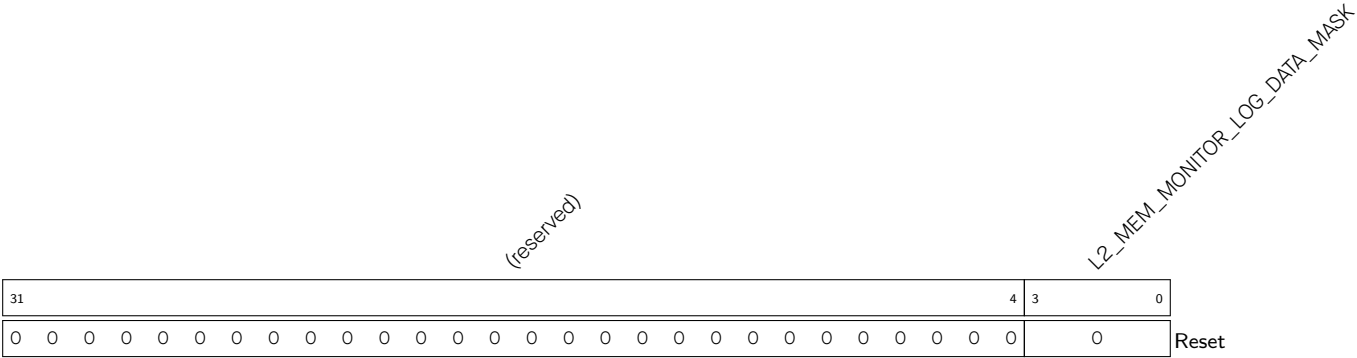
(R/W)

Register 19.15. L2\_MEM\_MONITOR\_LOG\_CHECK\_DATA\_REG (0x0008)



**L2\_MEM\_MONITOR\_LOG\_CHECK\_DATA** Configures the data to be monitored during bus access-  
ing. (R/W)

Register 19.16. L2\_MEM\_MONITOR\_LOG\_DATA\_MASK\_REG (0x000C)



**L2\_MEM\_MONITOR\_LOG\_DATA\_MASK** Configures which byte(s) in [L2\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#) to mask.

bit[0]: Configures whether to mask the least significant byte of [L2\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

bit[1]: Configures whether to mask the second least significant byte of [L2\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

bit[2]: Configures whether to mask the second most significant byte of [L2\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

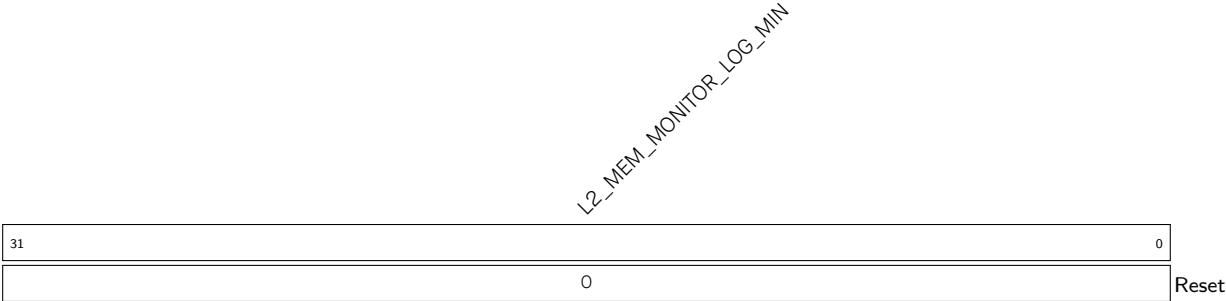
bit[3]: Configures whether to mask the most significant byte of [L2\\_MEM\\_MONITOR\\_LOG\\_CHECK\\_DATA\\_REG](#).

0: Not mask

1: Mask

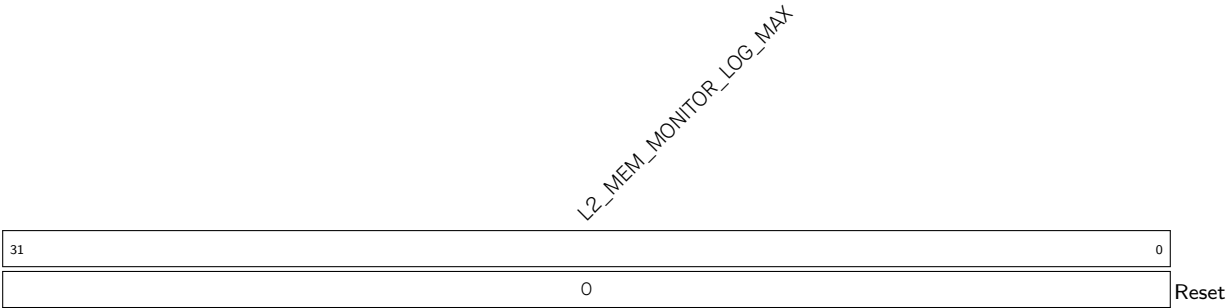
(R/W)

Register 19.17. L2\_MEM\_MONITOR\_LOG\_MIN\_REG (0x0010)



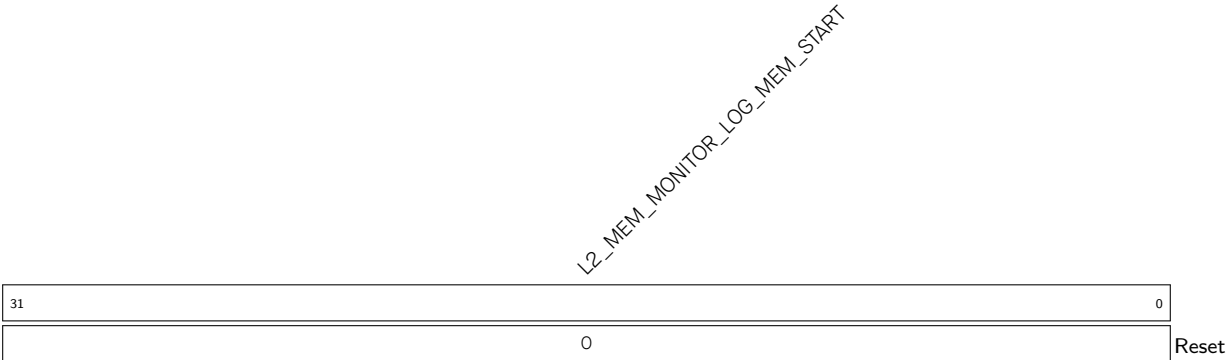
**L2\_MEM\_MONITOR\_LOG\_MIN** Configures the lower bound address of the monitored address space. (R/W)

Register 19.18. L2\_MEM\_MONITOR\_LOG\_MAX\_REG (0x0014)



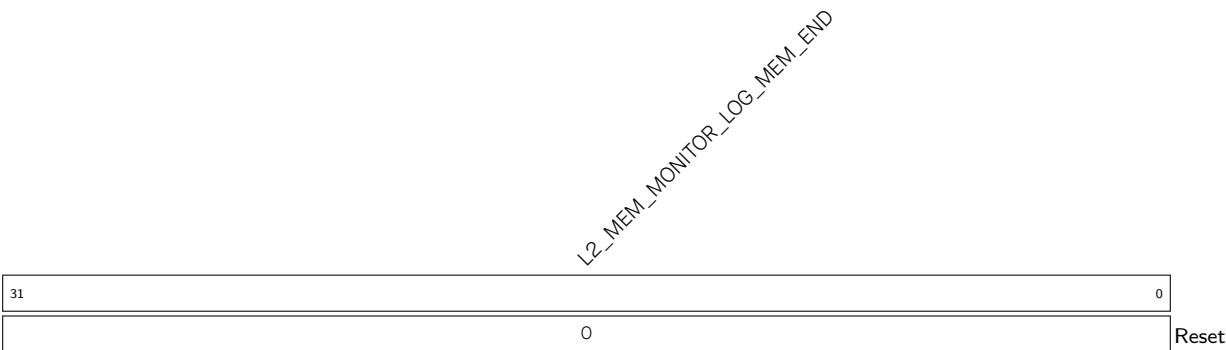
**L2\_MEM\_MONITOR\_LOG\_MAX** Configures the upper bound address of the monitored address space. (R/W)

Register 19.19. L2\_MEM\_MONITOR\_LOG\_MEM\_START\_REG (0x0018)



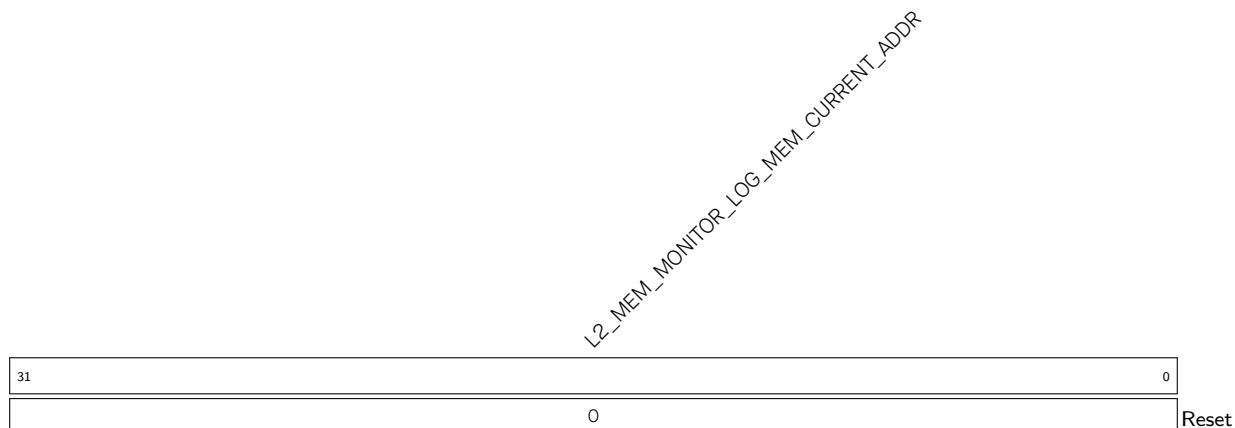
**L2\_MEM\_MONITOR\_LOG\_MEM\_START** Configures the starting address of the storage space for recorded data. (R/W)

Register 19.20. L2\_MEM\_MONITOR\_LOG\_MEM\_END\_REG (0x001C)



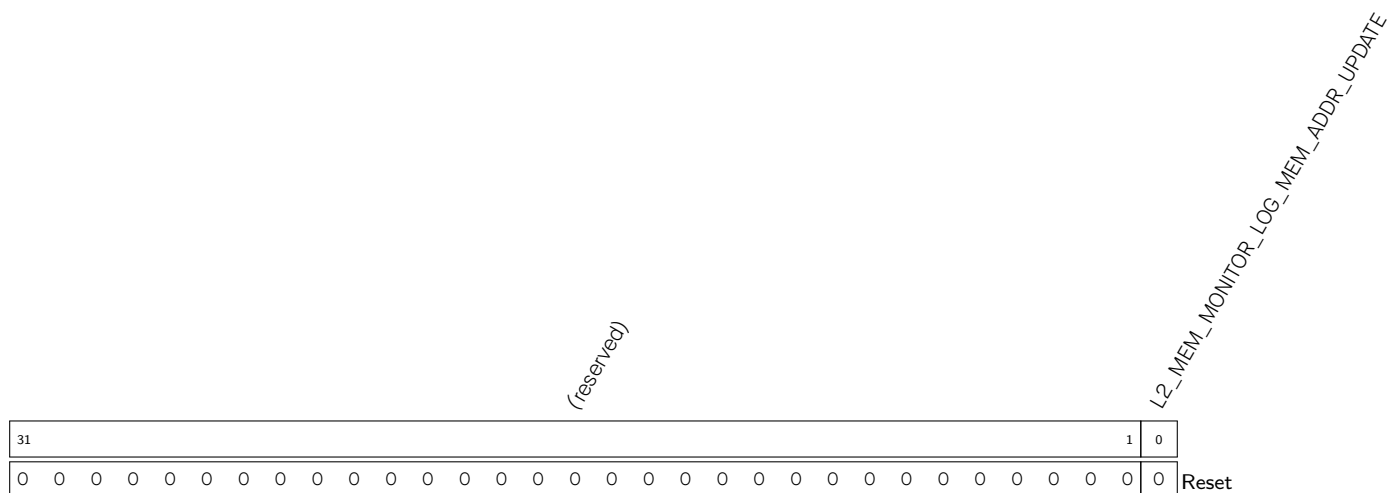
**L2\_MEM\_MONITOR\_LOG\_MEM\_END** Configures the ending address of the storage space for recorded data. (R/W)

Register 19.21. L2\_MEM\_MONITOR\_LOG\_MEM\_CURRENT\_ADDR\_REG (0x0020)



**L2\_MEM\_MONITOR\_LOG\_MEM\_CURRENT\_ADDR** Represents the address of the next write. (RO)

### Register 19.22. L2\_MEM\_MONITOR\_LOG\_MEM\_ADDR\_UPDATE\_REG (0x0024)



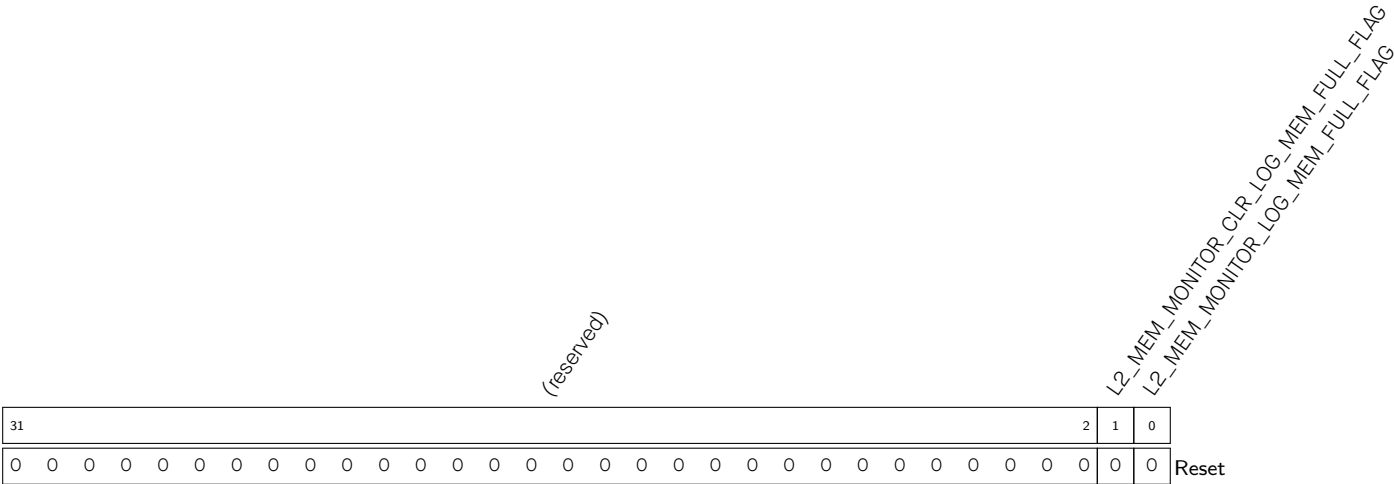
**L2\_MEM\_MONITOR\_LOG\_MEM\_ADDR\_UPDATE** Configures whether to update the value in **L2\_MEM\_MONITOR\_LOG\_MEM\_START\_REG** to **L2\_MEM\_MONITOR\_LOG\_MEM\_CURRENT\_ADDR\_REG**.

1: Update

0: Not update (default)

(WT)

Register 19.23. L2\_MEM\_MONITOR\_LOG\_MEM\_FULL\_FLAG\_REG (0x0028)



**L2\_MEM\_MONITOR\_LOG\_MEM\_FULL\_FLAG** Represents whether data overflows the storage space.

0: Not overflow

1: Overflow

(RO)

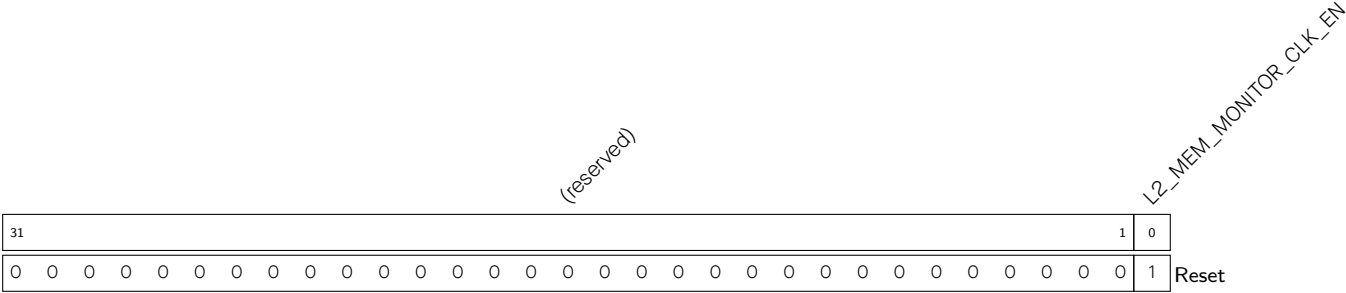
**L2\_MEM\_MONITOR\_CLR\_LOG\_MEM\_FULL\_FLAG** Configures whether to clear the [L2\\_MEM\\_MONITOR\\_LOG\\_MEM\\_FULL\\_FLAG](#) flag bit.

0: Not clear (default)

1: Clear

(WT)

Register 19.24. L2\_MEM\_MONITOR\_CLOCK\_GATE\_REG (0x002C)



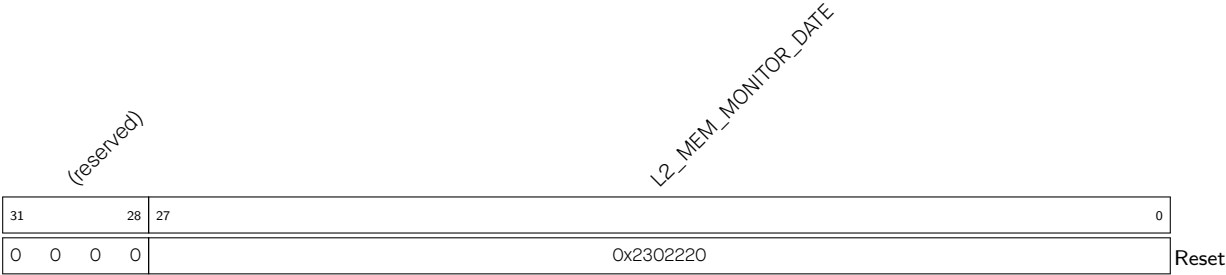
**L2\_MEM\_MONITOR\_CLK\_EN** Configures whether to enable the register clock gating.

0: Disable

1: Enable

(R/W)

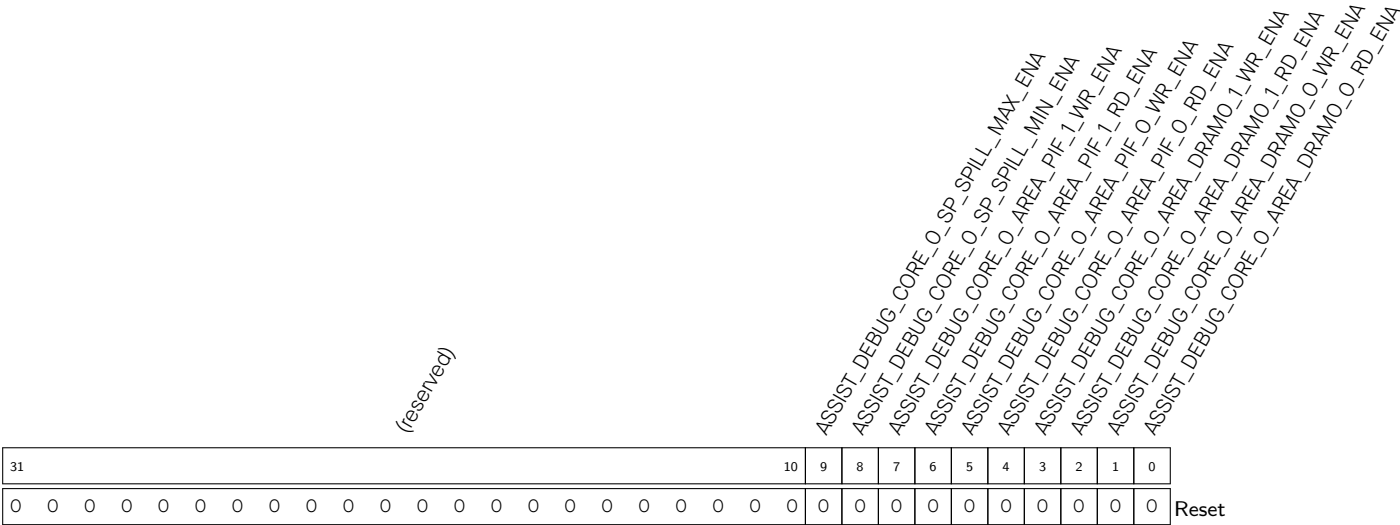
Register 19.25. L2\_MEM\_MONITOR\_DATE\_REG (0x03FC)



L2\_MEM\_MONITOR\_DATE   Version control register. (R/W)

19.7.3 Other Registers

Register 19.26. ASSIST\_DEBUG\_CORE\_O\_MONTR\_ENA\_REG (0x0000)



**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_0\_RD\_ENA** Configures whether to monitor read operations in HP CPU0 region 0 by the HP CPU0 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_0\_WR\_ENA** Configures whether to monitor write operations in HP CPU0 region 0 by the HP CPU0 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_RD\_ENA** Configures whether to monitor read operations in HP CPU0 region 1 by the HP CPU0 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_WR\_ENA** Configures whether to monitor write operations in HP CPU0 region 1 by the HP CPU0 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_0\_RD\_ENA** Configures whether to monitor read operations in region 0 by the Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

Continued on the next page...



**Register 19.26. ASSIST\_DEBUG\_CORE\_O\_MONTR\_ENA\_REG (0x0000)**

Continued from the previous page...

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_0\_WR\_ENA** Configures whether to monitor write operations in HP CPU0 region 0 by the HP CPU0 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_RD\_ENA** Configures whether to monitor read operations in HP CPU0 region 1 by the HP CPU0 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_WR\_ENA** Configures whether to monitor write operations in HP CPU0 region 1 by the HP CPU0 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_SP\_SPILL\_MIN\_ENA** Configures whether to monitor HP CPU0 SP going below the lower bound address of HP CPU0 SP monitored region.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_O\_SP\_SPILL\_MAX\_ENA** Configures whether to monitor HP CPU0 SP going beyond the upper bound address of HP CPU0 SP monitored region.

0: Not monitor

1: Monitor

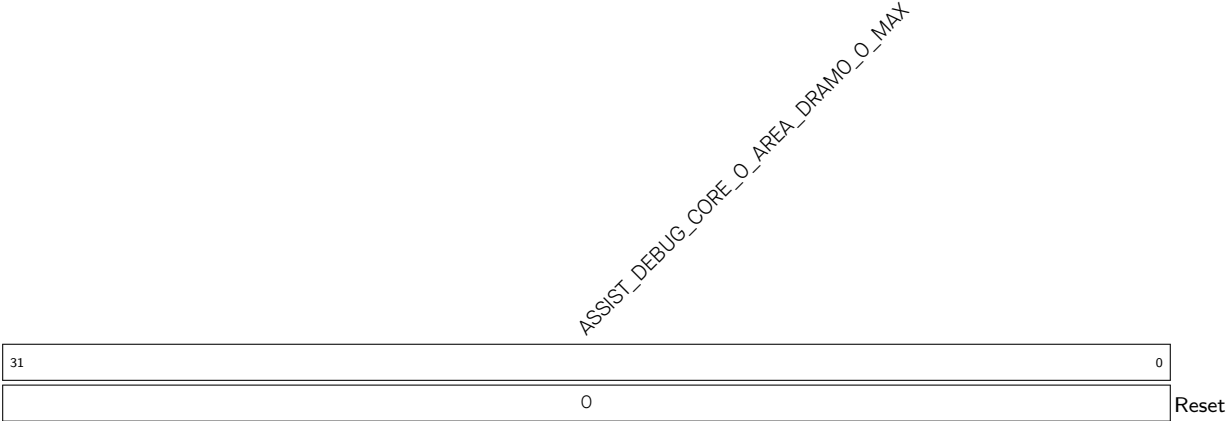
(R/W)

Register 19.27. ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_MIN\_REG (0x0010)



**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_MIN** Configures the lower bound address of HP CPU0 Data bus region 0. (R/W)

Register 19.28. ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_MAX\_REG (0x0014)



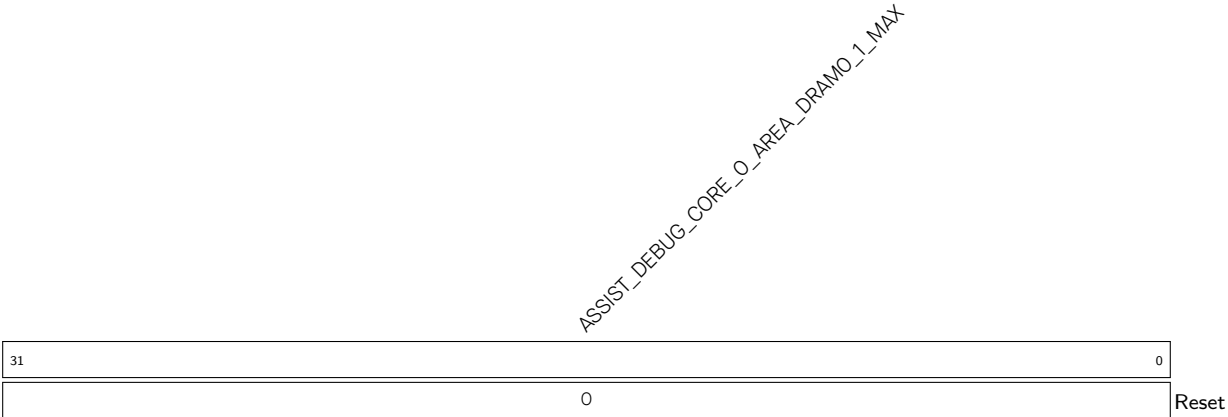
**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_MAX** Configures the upper bound address of HP CPU0 Data bus region 0. (R/W)

Register 19.29. ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_MIN\_REG (0x0018)



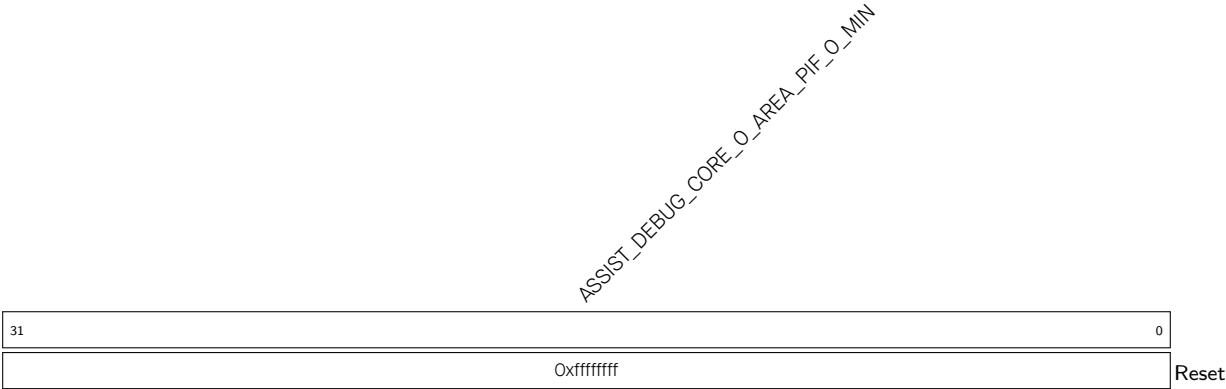
**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_MIN** Configures the lower bound address of HP CPU0 Data bus region 1. (R/W)

Register 19.30. ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_MAX\_REG (0x001C)



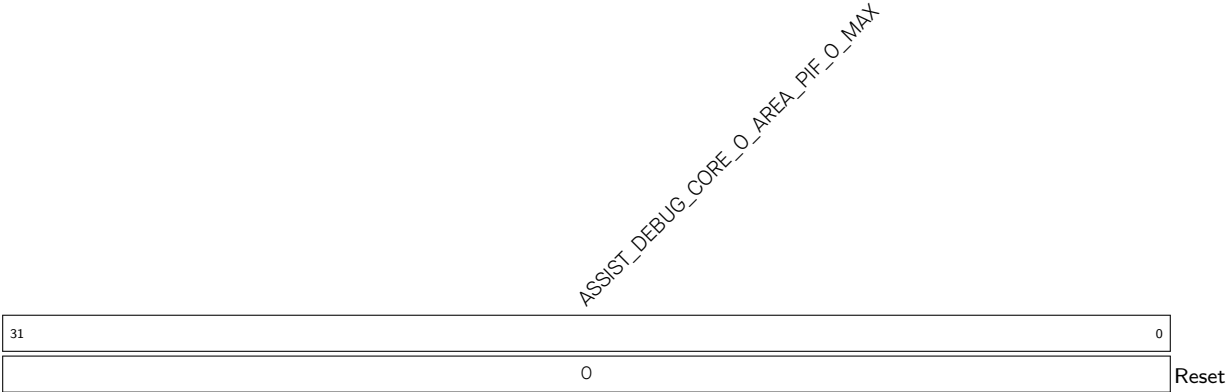
**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_MAX** Configures the upper bound address of HP CPU0 Data bus region 1. (R/W)

Register 19.31. ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_MIN\_REG (0x0020)



**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_MIN** Configures the lower bound address of HP CPU0 Peripheral bus region O. (R/W)

Register 19.32. ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_MAX\_REG (0x0024)



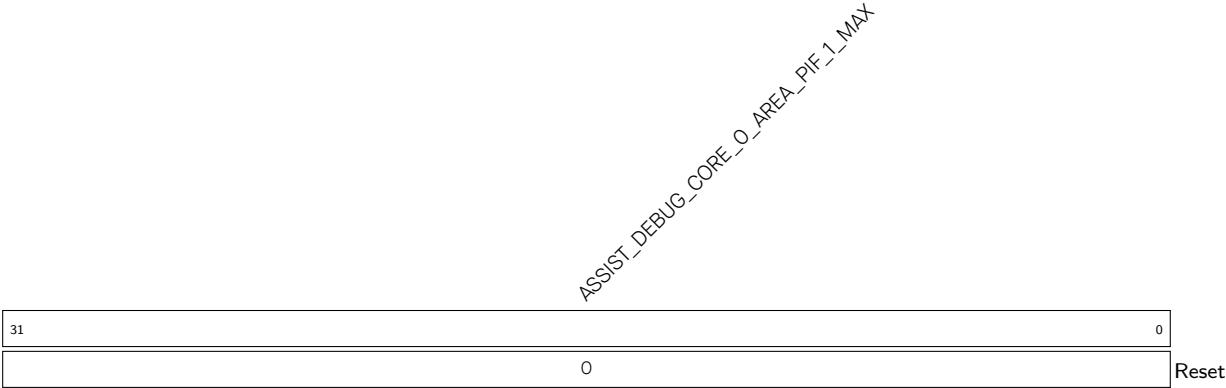
**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_MAX** Configures the upper bound address of HP CPU0 Peripheral bus region O. (R/W)

Register 19.33. ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_MIN\_REG (0x0028)



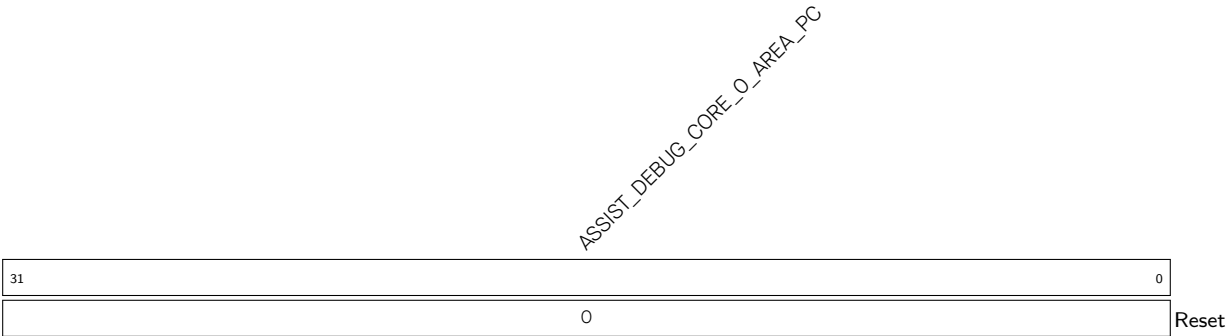
**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_MIN** Configures the lower bound address of HP CPU0 Peripheral bus region 1. (R/W)

Register 19.34. ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_MAX\_REG (0x002C)



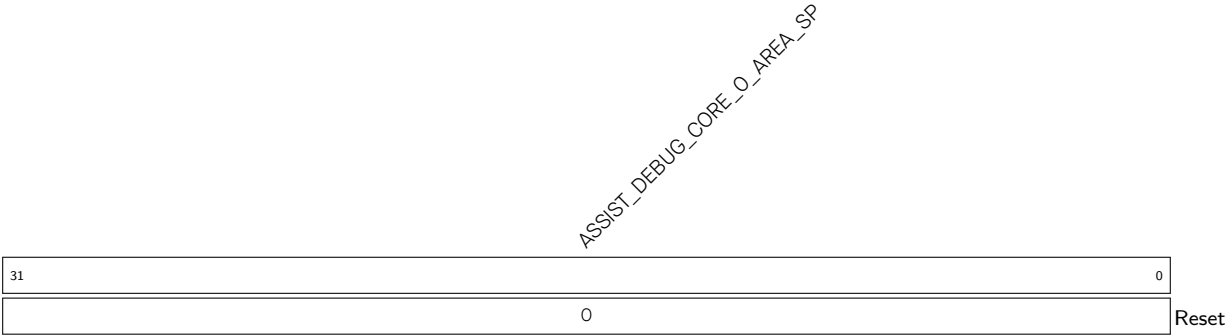
**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_MAX** Configures the upper bound address of HP CPU0 Peripheral bus region 1. (R/W)

Register 19.35. ASSIST\_DEBUG\_CORE\_O\_AREA\_PC\_REG (0x0030)



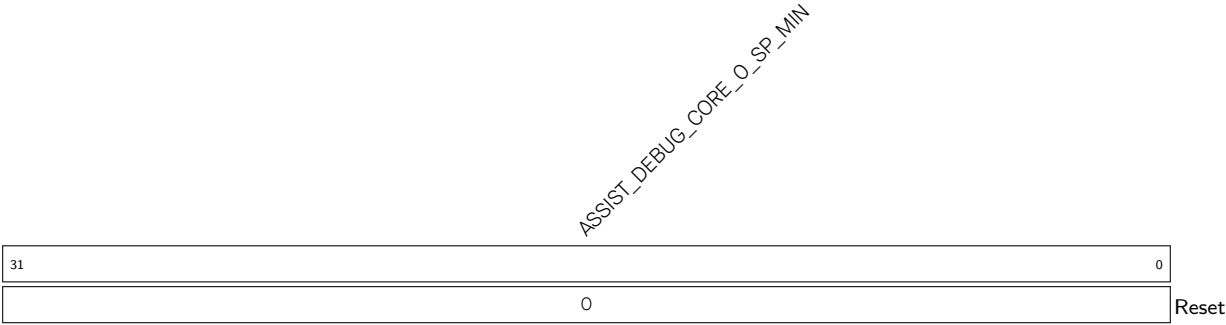
**ASSIST\_DEBUG\_CORE\_O\_AREA\_PC** Represents the HP CPU0 PC value when an interrupt is triggered during region monitoring. (RO)

Register 19.36. ASSIST\_DEBUG\_CORE\_O\_AREA\_SP\_REG (0x0034)



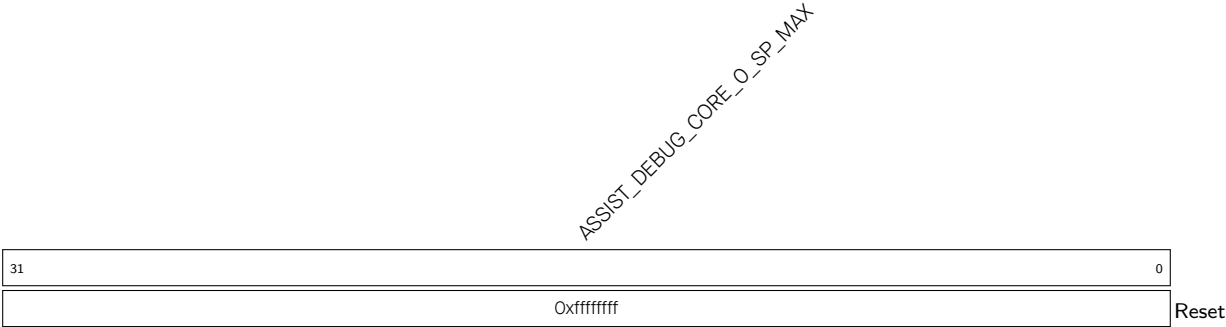
**ASSIST\_DEBUG\_CORE\_O\_AREA\_SP** Represents the HP CPU0 SP value when an interrupt is triggered during region monitoring. (RO)

Register 19.37. ASSIST\_DEBUG\_CORE\_O\_SP\_MIN\_REG (0x0038)



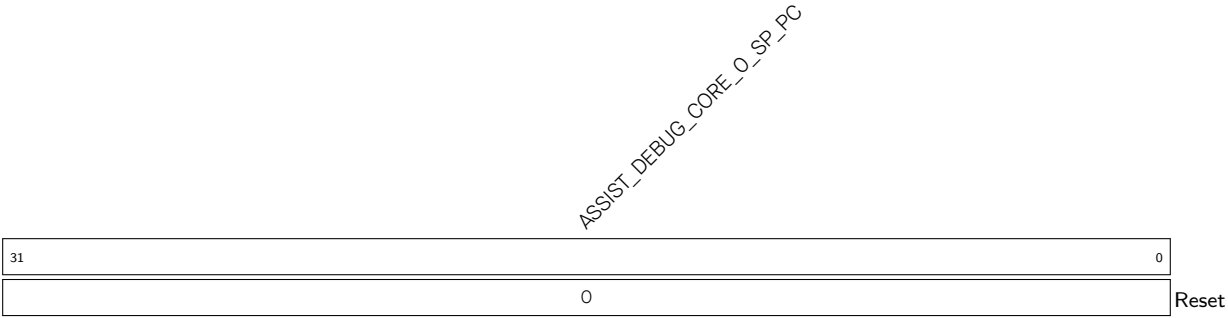
**ASSIST\_DEBUG\_CORE\_O\_SP\_MIN** Configures the lower bound address of the HP CPU0 SP monitored region. (R/W)

Register 19.38. ASSIST\_DEBUG\_CORE\_O\_SP\_MAX\_REG (0x003C)



**ASSIST\_DEBUG\_CORE\_O\_SP\_MAX** Configures the upper bound address of the HP CPU0 SP monitored region. (R/W)

Register 19.39. ASSIST\_DEBUG\_CORE\_0\_SP\_PC\_REG (0x0040)



**ASSIST\_DEBUG\_CORE\_0\_SP\_PC** Represents the HP CPU0 PC value during SP monitoring. (RO)

Register 19.40. ASSIST\_DEBUG\_CORE\_O\_INTR\_RAW\_REG (0x0004)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ASSIST_DEBUG_CORE_O_SP_SPILL_MAX_RAW<br>ASSIST_DEBUG_CORE_O_SP_SPILL_MIN_RAW<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_RD_RAW<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_WR_RAW<br>ASSIST_DEBUG_CORE_O_AREA_PIF_O_RD_RAW<br>ASSIST_DEBUG_CORE_O_AREA_PIF_O_WR_RAW<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_RAW<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_RAW<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_RD_RAW<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_WR_RAW |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |       |

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_RD\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_DRAMO\\_O\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_O\_WR\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_DRAMO\\_O\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_RD\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_DRAMO\\_1\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_DRAMO\_1\_WR\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_DRAMO\\_1\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_RD\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_PIF\\_O\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_O\_WR\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_PIF\\_O\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_RD\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_PIF\\_1\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_AREA\_PIF\_1\_WR\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_AREA\\_PIF\\_1\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_SP\_SPILL\_MIN\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_SP\\_SPILL\\_MIN\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_O\_SP\_SPILL\_MAX\_RAW** The raw interrupt status of [AS-SIST\\_DEBUG\\_CORE\\_O\\_SP\\_SPILL\\_MAX\\_INT](#). (RO)



Register 19.41. ASSIST\_DEBUG\_CORE\_O\_INTR\_ENA\_REG (0x0008)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ASSIST_DEBUG_CORE_O_SP_SPILL_MAX_INTR_ENA<br>ASSIST_DEBUG_CORE_O_SP_SPILL_MIN_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_PIF_1_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_INTR_ENA |   |   |   |   |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |       |

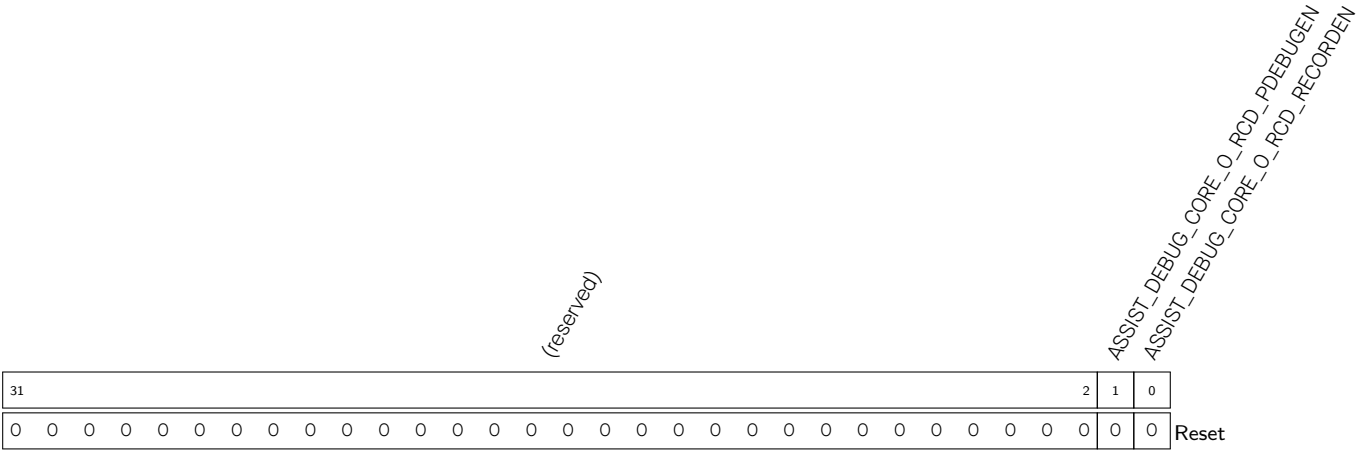
|  |       |   |    |        |                     |
|--|-------|---|----|--------|---------------------|
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_RD_INTR_ENA           | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_DRAMO_O_RD_INT.</a> | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_O_WR_INTR_ENA           | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_DRAMO_O_WR_INT.</a> | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_INTR_ENA           | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_INT.</a> | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_INTR_ENA           | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_INT.</a> | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_O_RD_INTR_ENA             | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_PIF_O_RD_INT.</a>   | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_O_WR_INTR_ENA             | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_PIF_O_WR_INT.</a>   | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_1_RD_INTR_ENA             | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_PIF_1_RD_INT.</a>   | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_1_WR_INTR_ENA             | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_AREA_PIF_1_WR_INT.</a>   | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_SP_SPILL_MIN_INTR_ENA              | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_SP_SPILL_MIN_INT.</a>    | (R/W) |   |    |        |                     |
| ASSIST_DEBUG_CORE_O_SP_SPILL_MAX_INTR_ENA              | Write | 1 | to | enable | <a href="#">AS-</a> |
| <a href="#">SIST_DEBUG_CORE_O_SP_SPILL_MAX_INT.</a>    | (R/W) |   |    |        |                     |

Register 19.42. ASSIST\_DEBUG\_CORE\_O\_INTR\_CLR\_REG (0x000C)

|            |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |   |   |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|---|---|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   | ASSIST_DEBUG_CORE_0_SP_SPILL_MAX_CLR<br>(ASSIST_DEBUG_CORE_0_SP_SPILL_MIN_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_PIF_1_WR_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_PIF_1_RD_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_PIF_0_WR_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_PIF_0_RD_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_DRAMO_1_WR_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_DRAMO_1_RD_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_DRAMO_0_WR_CLR<br>(ASSIST_DEBUG_CORE_0_AREA_DRAMO_0_RD_CLR |   |       |   |   |   |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   | 10 |   |   |   |   |   |   |   |   |   | 9 | 8 | 7   | 6 | 5     | 4 | 3 | 2 | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | Reset |   |   |   |   |   |  |  |

|   |       |   |    |       |     |
|---|-------|---|----|-------|-----|
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_0_RD_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_DRAMO_0_RD_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_0_WR_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_DRAMO_0_WR_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_DRAMO_1_RD_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_DRAMO_1_WR_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_0_RD_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_PIF_0_RD_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_0_WR_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_PIF_0_WR_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_1_RD_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_PIF_1_RD_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_AREA_PIF_1_WR_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_AREA_PIF_1_WR_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_SP_SPILL_MIN_CLR    | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_SP_SPILL_MIN_INT.     | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_O_SP_SPILL_MAX_CLR    | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_O_SP_SPILL_MAX_INT.     | (WT)  |   |    |       |     |

Register 19.43. ASSIST\_DEBUG\_CORE\_O\_RCD\_EN\_REG (0x0044)



**ASSIST\_DEBUG\_CORE\_O\_RCD\_RECORDEN** Configures whether to enable HP CPU0 PC logging.

0: Disable

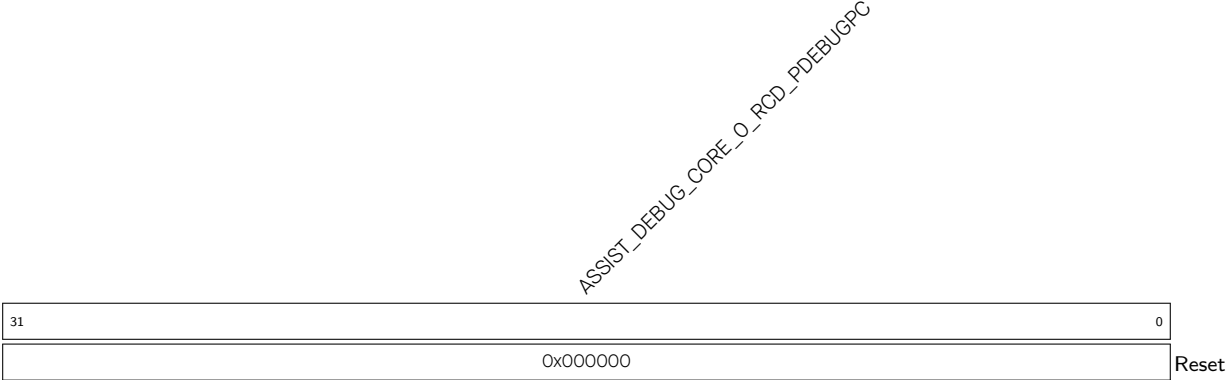
1: [ASSIST\\_DEBUG\\_CORE\\_O\\_RCD\\_PDEBUGPC\\_REG](#) starts to record HP CPU0 PC in real time (R/W)

**ASSIST\_DEBUG\_CORE\_O\_RCD\_PDEBUGEN** Configures whether to enable HP CPU0 debugging.

0: Disable

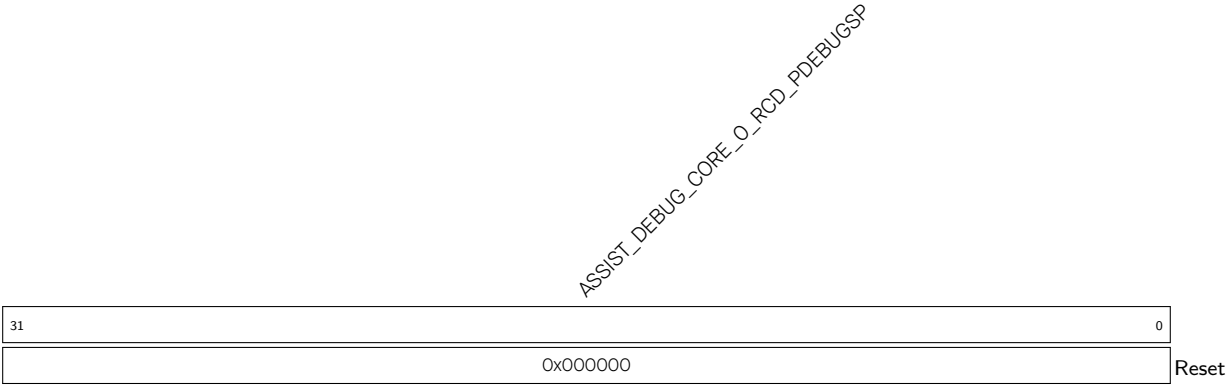
1: HP CPU0 outputs HP CPU0 PC (R/W)

Register 19.44. ASSIST\_DEBUG\_CORE\_O\_RCD\_PDEBUGPC\_REG (0x0048)



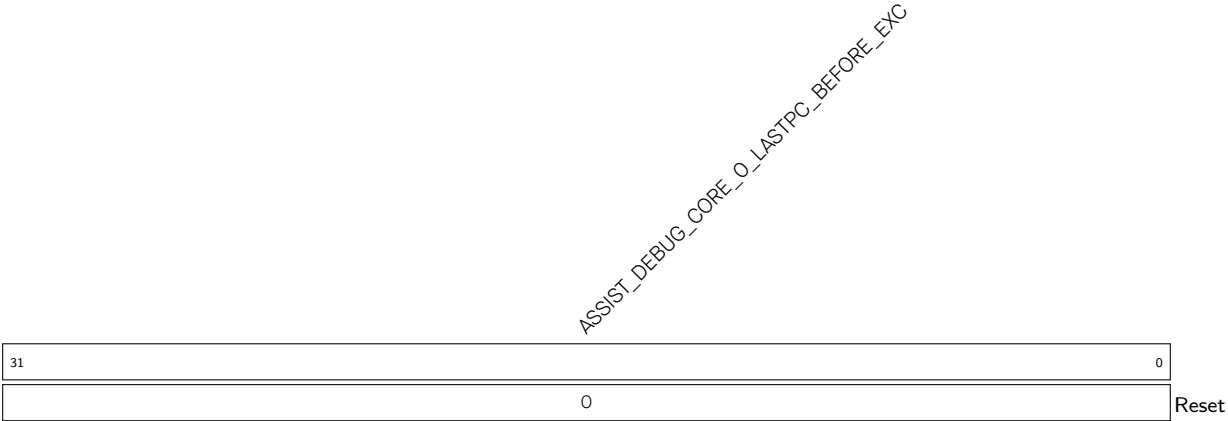
**ASSIST\_DEBUG\_CORE\_O\_RCD\_PDEBUGPC** Represents the PC value at HP CPU0 reset. (RO)

Register 19.45. ASSIST\_DEBUG\_CORE\_O\_RCD\_PDEBUGSP\_REG (0x004C)



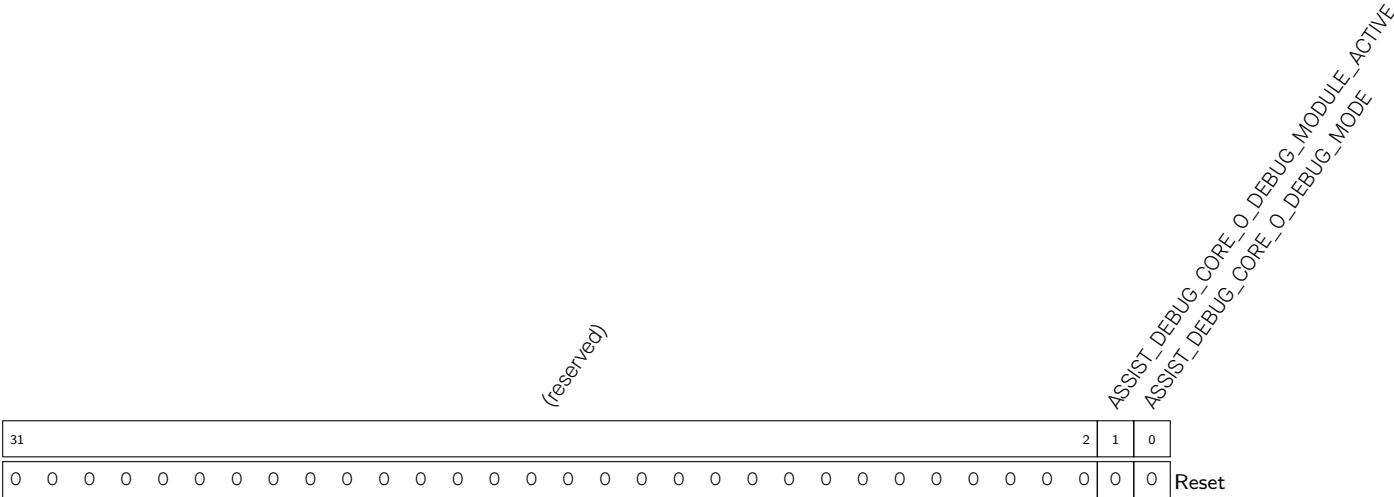
**ASSIST\_DEBUG\_CORE\_O\_RCD\_PDEBUGSP** Represents the HP CPU0 SP. (RO)

Register 19.46. ASSIST\_DEBUG\_CORE\_O\_LASTPC\_BEFORE\_EXCEPTION\_REG (0x0070)



**ASSIST\_DEBUG\_CORE\_O\_LASTPC\_BEFORE\_EXC** Represents the HP CPU0 PC of the last command before the HP CPU0 enters exception. (RO)

Register 19.47. ASSIST\_DEBUG\_CORE\_O\_DEBUG\_MODE\_REG (0x0074)



**ASSIST\_DEBUG\_CORE\_O\_DEBUG\_MODE**   Represents whether HP CPU0 is in debugging mode.

1: In debugging mode

0: Not in debugging mode

(RO)

**ASSIST\_DEBUG\_CORE\_O\_DEBUG\_MODULE\_ACTIVE**   Represents the status of the HP CPU0 debug module.

1: Active status

Other: Inactive status

(RO)

Register 19.48. ASSIST\_DEBUG\_CORE\_1\_MONTR\_ENA\_REG (0x0080)

|            |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |   |   |  |   |   |   |   |   |   |   |   |       |  |
|------------|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|---|---|--|---|---|---|---|---|---|---|---|-------|--|
| (reserved) |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |   |   | ASSIST_DEBUG_CORE_1_SP_SPILL_MAX_ENA<br>ASSIST_DEBUG_CORE_1_SP_SPILL_MIN_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_WR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_RD_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_0_WR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_0_RD_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_ENA<br>ASSIST_DEBUG_CORE_0_WR_ENA<br>ASSIST_DEBUG_CORE_0_RD_ENA |   |   |   |   |   |   |   |   |       |  |
| 31         |  |  |  |  |  |  |  |  |  | 10 |  |  |  |  |  |  |  |  |  | 9 | 8 | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |  |
| 0          |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_RD\_ENA** Configures whether to monitor read operations in HP CPU1 region 0 by the HP CPU1 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_WR\_ENA** Configures whether to monitor write operations in HP CPU1 region 0 by the HP CPU1 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_RD\_ENA** Configures whether to monitor read operations in HP CPU1 region 1 by the HP CPU1 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_WR\_ENA** Configures whether to monitor write operations in HP CPU1 region 1 by the HP CPU1 Data bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_RD\_ENA** Configures whether to monitor read operations in HP CPU1 region 0 by the HP CPU1 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

Continued on the next page...

**Register 19.48. ASSIST\_DEBUG\_CORE\_1\_MONTR\_ENA\_REG (0x0000)**

Continued from the previous page...

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_WR\_ENA** Configures whether to monitor write operations in HP CPU1 region 0 by the HP CPU1 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_RD\_ENA** Configures whether to monitor read operations in HP CPU1 region 1 by the HP CPU1 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_WR\_ENA** Configures whether to monitor write operations in HP CPU1 region 1 by the HP CPU1 Peripheral bus.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MIN\_ENA** Configures whether to monitor HP CPU1 SP going below the lower bound address of HP CPU1 SP monitored region.

0: Not monitor

1: Monitor

(R/W)

**ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MAX\_ENA** Configures whether to monitor HP CPU1 SP going beyond the upper bound address of HP CPU1 SP monitored region.

0: Not monitor

1: Monitor

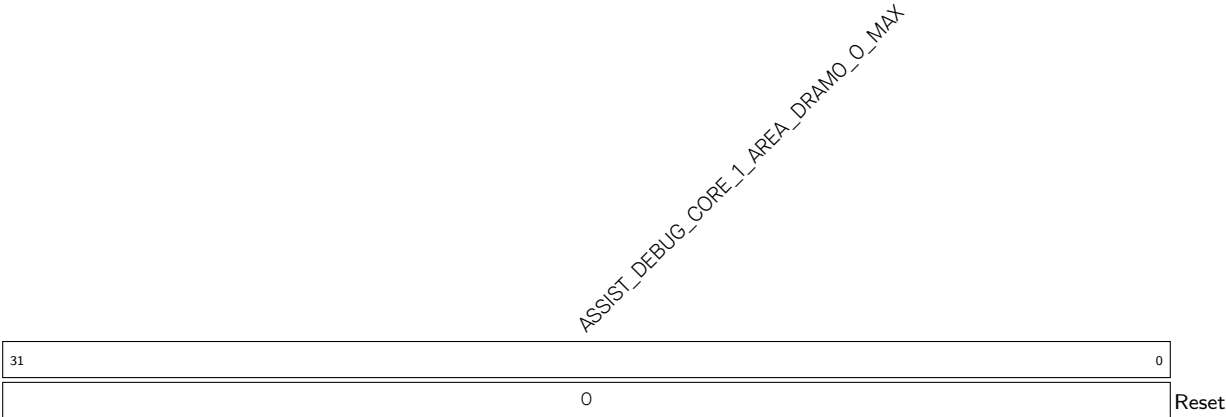
(R/W)

Register 19.49. ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_MIN\_REG (0x0090)



**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_MIN** Configures the lower bound address of HP CPU1 Data bus region 0. (R/W)

Register 19.50. ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_MAX\_REG (0x0094)



**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_MAX** Configures the upper bound address of HP CPU1 Data bus region 0. (R/W)

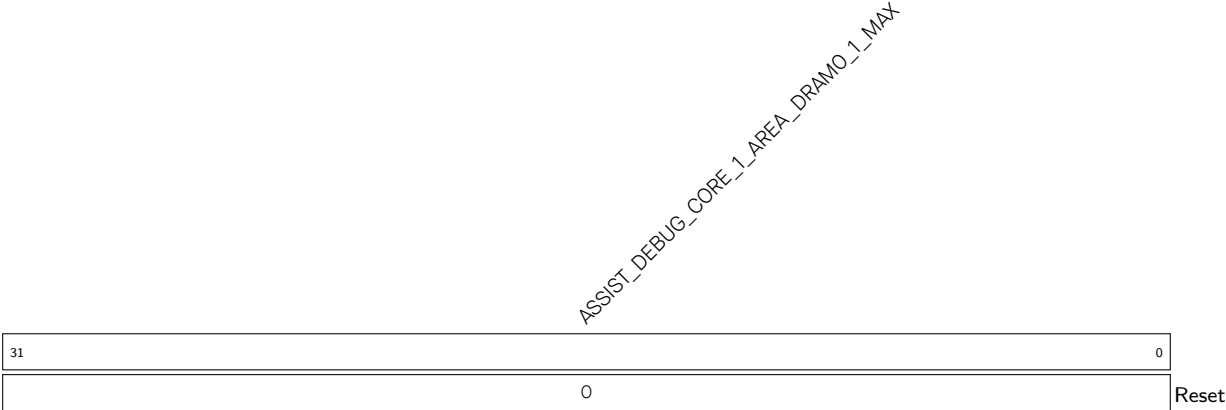


Register 19.51. ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_MIN\_REG (0x0098)



**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_MIN** Configures the lower bound address of HP CPU1 Data bus region 1. (R/W)

Register 19.52. ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_MAX\_REG (0x009C)



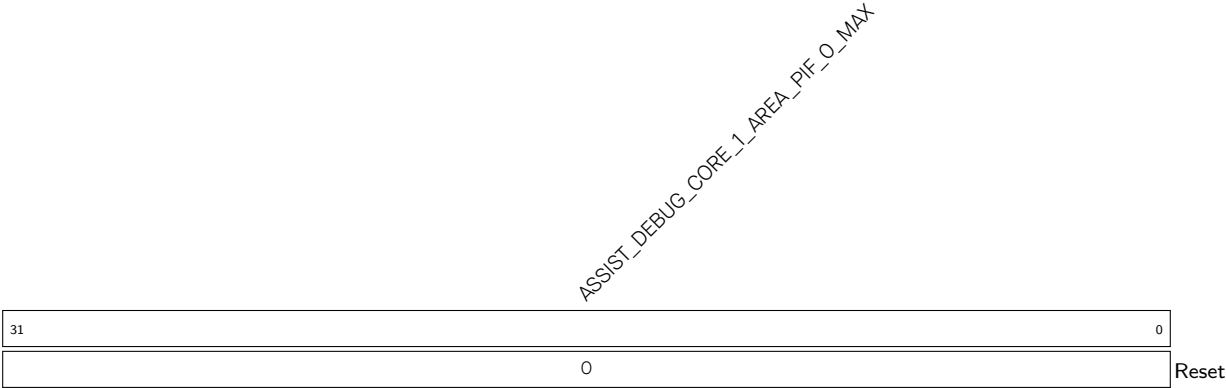
**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_MAX** Configures the upper bound address of HP CPU1 Data bus region 1. (R/W)

Register 19.53. ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_MIN\_REG (0x00A0)



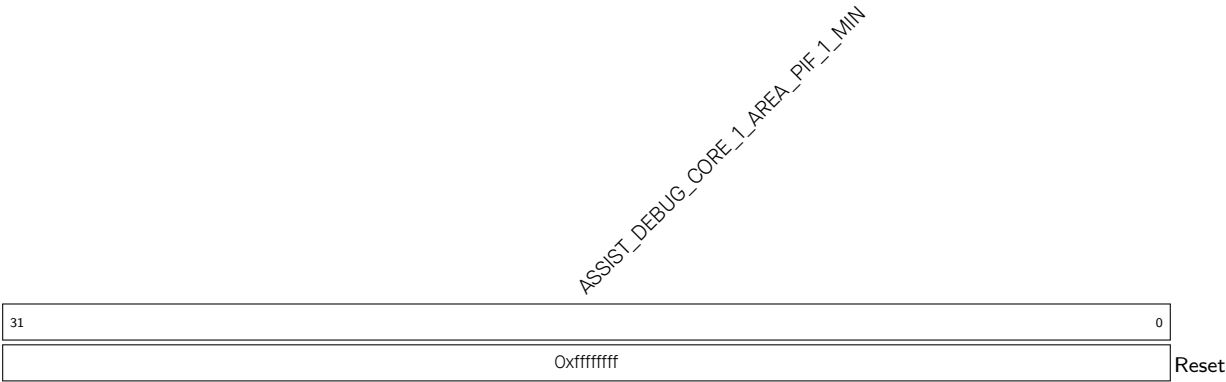
**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_MIN** Configures the lower bound address of HP CPU1 Peripheral bus region 0. (R/W)

Register 19.54. ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_MAX\_REG (0x00A4)



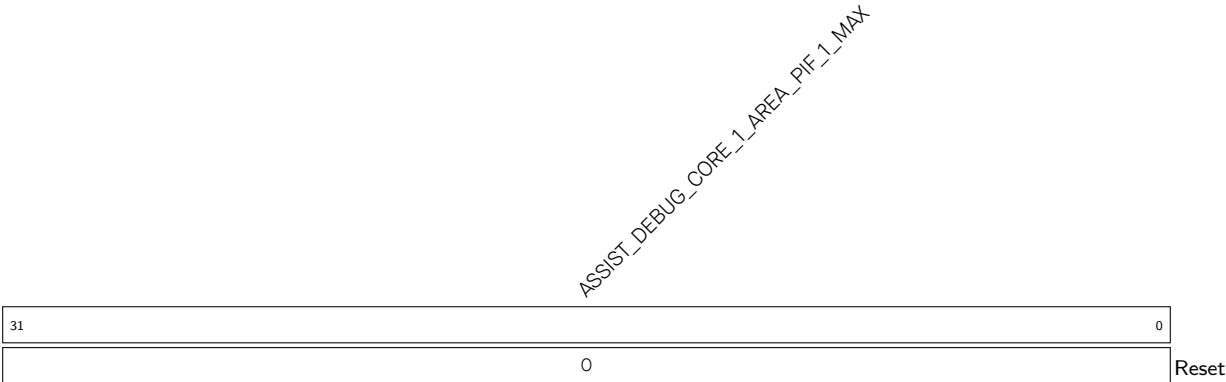
**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_MAX** Configures the upper bound address of HP CPU1 Peripheral bus region 0. (R/W)

Register 19.55. ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_MIN\_REG (0x00A8)



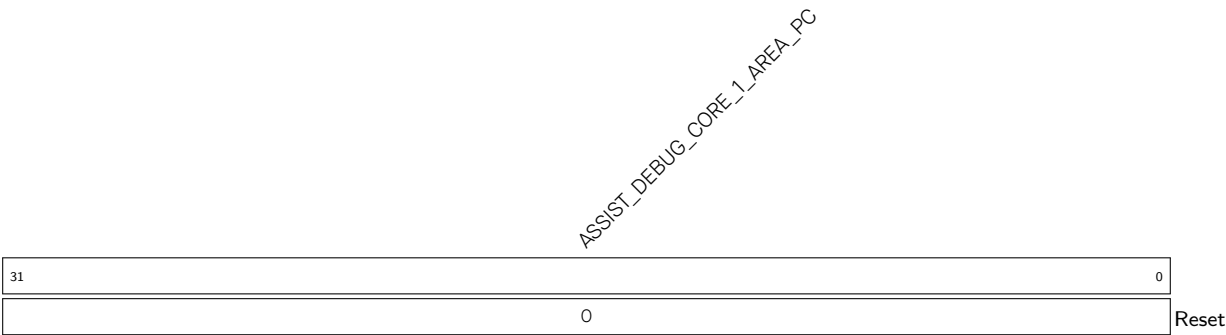
**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_MIN** Configures the lower bound address of HP CPU1 Peripheral bus region 1. (R/W)

Register 19.56. ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_MAX\_REG (0x00AC)



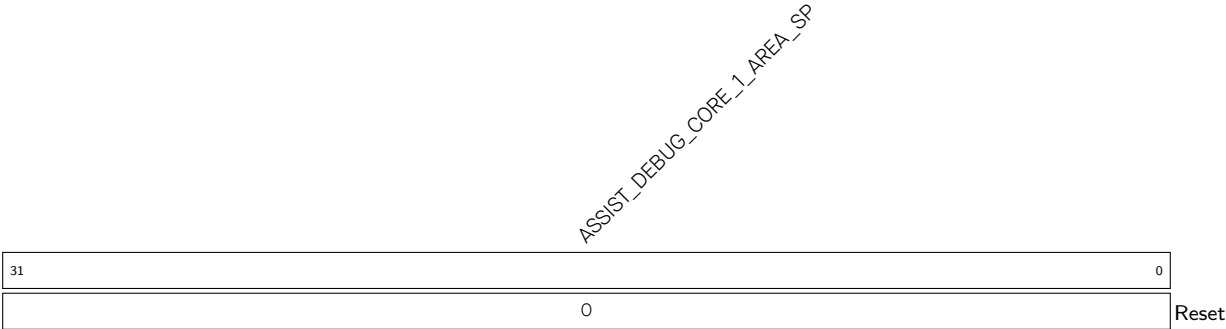
**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_MAX** Configures the upper bound address of HP CPU1 Peripheral bus region 1. (R/W)

Register 19.57. ASSIST\_DEBUG\_CORE\_1\_AREA\_PC\_REG (0x00B0)



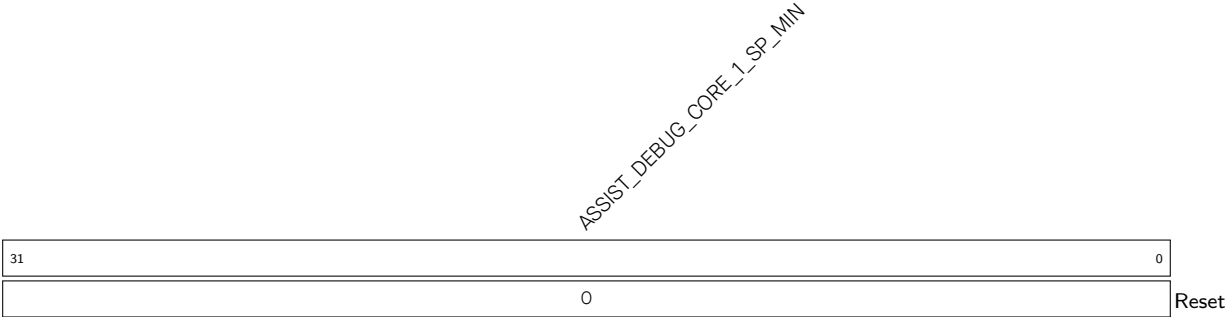
**ASSIST\_DEBUG\_CORE\_1\_AREA\_PC** Represents the HP CPU1 PC value when an interrupt is triggered during region monitoring. (RO)

Register 19.58. ASSIST\_DEBUG\_CORE\_1\_AREA\_SP\_REG (0x00B4)



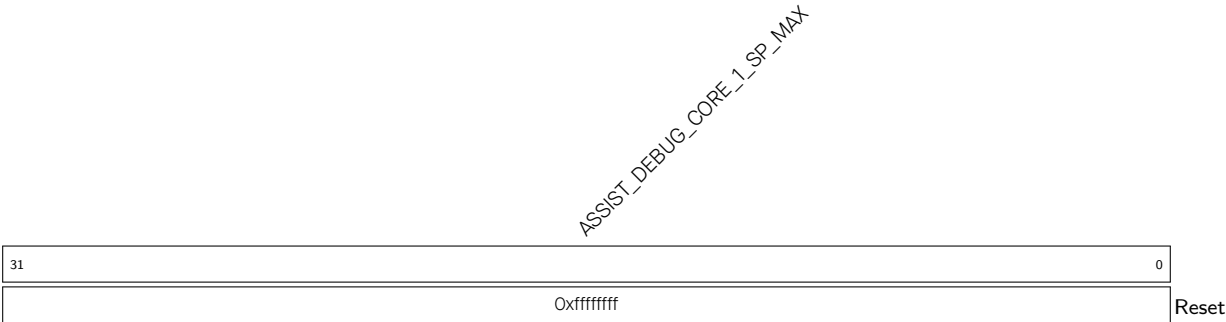
**ASSIST\_DEBUG\_CORE\_1\_AREA\_SP** Represents the HP CPU1 SP value when an interrupt is triggered during region monitoring. (RO)

Register 19.59. ASSIST\_DEBUG\_CORE\_1\_SP\_MIN\_REG (0x00B8)



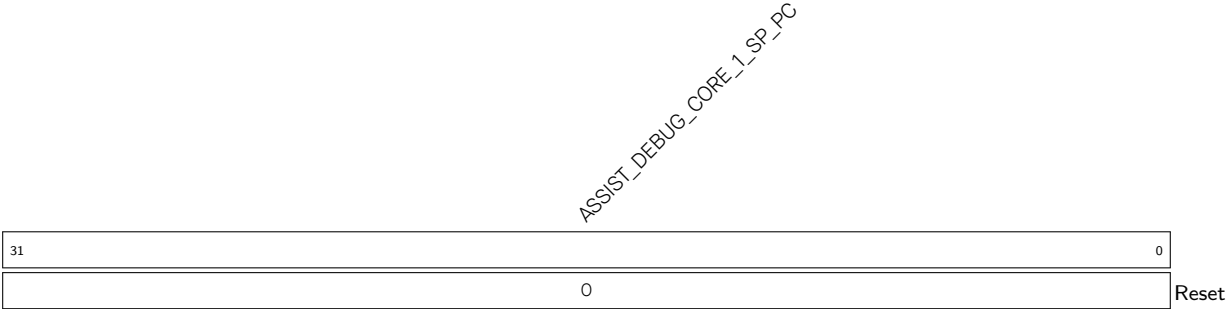
**ASSIST\_DEBUG\_CORE\_1\_SP\_MIN** Configures the lower bound address of the HP CPU1 SP monitored region. (R/W)

Register 19.60. ASSIST\_DEBUG\_CORE\_1\_SP\_MAX\_REG (0x00BC)



**ASSIST\_DEBUG\_CORE\_1\_SP\_MAX** Configures the upper bound address of the HP CPU1 SP monitored region. (R/W)

Register 19.61. ASSIST\_DEBUG\_CORE\_1\_SP\_PC\_REG (0x00C0)



**ASSIST\_DEBUG\_CORE\_1\_SP\_PC** Represents the HP CPU1 PC value during SP monitoring. (RO)

Register 19.62. ASSIST\_DEBUG\_CORE\_1\_INTR\_RAW\_REG (0x0084)

|            |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |       |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|-------|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   | ASSIST_DEBUG_CORE_1_SP_SPILL_MAX_RAW<br>ASSIST_DEBUG_CORE_1_SP_SPILL_MIN_RAW<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_MIN_RAW<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_WR_RAW<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_RD_RAW<br>ASSIST_DEBUG_CORE_1_AREA_PIF_0_WR_RAW<br>ASSIST_DEBUG_CORE_1_AREA_PIF_0_RD_RAW<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_RAW<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_RAW<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_WR_RAW<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_RD_RAW |   |   |   |   |   |   |   |       |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   | 10 |   |   |   |   |   |   |   |   |   | 9 | 8 | 7  | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 |   |   |   |   |   |   |       |  |  |  |

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_RD\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_0\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_0\_WR\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_0\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_RD\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_WR\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_RD\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_0\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_0\_WR\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_0\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_RD\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_RD\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_WR\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_WR\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MIN\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_SP\\_SPILL\\_MIN\\_INT](#). (RO)

**ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MAX\_RAW** The raw interrupt status of [ASSIST\\_DEBUG\\_CORE\\_1\\_SP\\_SPILL\\_MAX\\_INT](#). (RO)

Register 19.63. ASSIST\_DEBUG\_CORE\_1\_INTR\_ENA\_REG (0x0088)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ASSIST_DEBUG_CORE_1_SP_SPILL_MAX_INTR_ENA<br>ASSIST_DEBUG_CORE_1_SP_SPILL_MIN_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_1_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_O_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_PIF_O_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_O_WR_INTR_ENA<br>ASSIST_DEBUG_CORE_1_AREA_DRAMO_O_RD_INTR_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10   |   |   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_RD\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_O\\_RD\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_O\_WR\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_O\\_WR\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_RD\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_RD\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_DRAMO\_1\_WR\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_DRAMO\\_1\\_WR\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_RD\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_O\\_RD\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_O\_WR\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_O\\_WR\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_RD\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_RD\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_AREA\_PIF\_1\_WR\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_AREA\\_PIF\\_1\\_WR\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MIN\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_SP\\_SPILL\\_MIN\\_INT.](#) (R/W)

ASSIST\_DEBUG\_CORE\_1\_SP\_SPILL\_MAX\_INTR\_ENA Write 1 to enable [AS-SIST\\_DEBUG\\_CORE\\_1\\_SP\\_SPILL\\_MAX\\_INT.](#) (R/W)

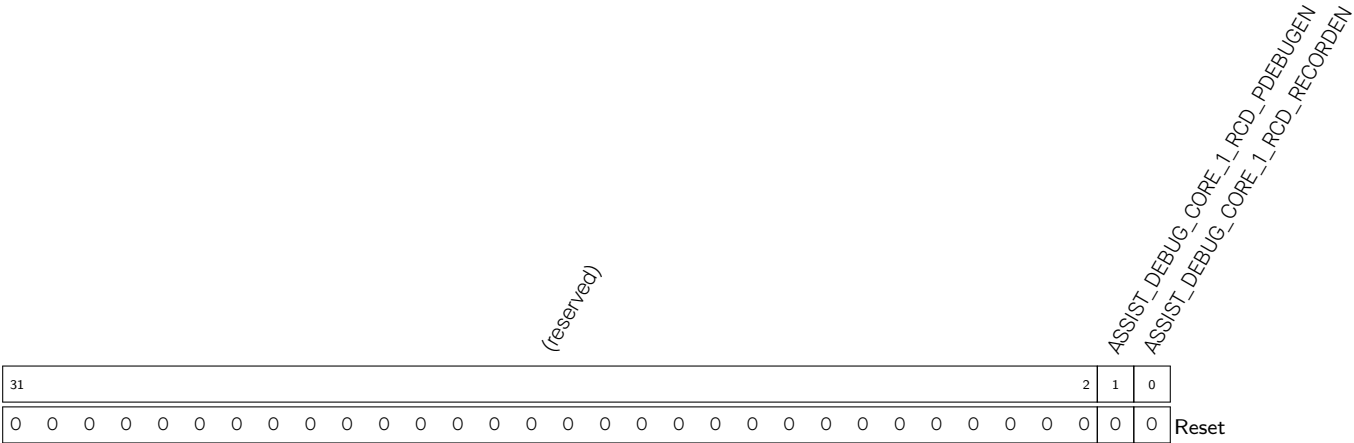
## Register 19.64. ASSIST\_DEBUG\_CORE\_1\_INTR\_CLR\_REG (0x008C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ASSIST_DEBUG_CORE_1_SP_SPILL_MAX_CLR<br>(ASSIST_DEBUG_CORE_1_SP_SPILL_MIN_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_PIF_1_MIN_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_PIF_1_WR_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_PIF_1_RD_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_WR_CLR<br>(ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_RD_CLR |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |   |   |   |   |   |   |   |   |   |   |       |

|   |       |   |    |       |     |
|---|-------|---|----|-------|-----|
| ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_RD_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_DRAMO_0_RD_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_DRAMO_0_WR_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_DRAMO_0_WR_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_DRAMO_1_RD_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_CLR | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_DRAMO_1_WR_INT.  | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_PIF_0_RD_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_PIF_0_RD_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_PIF_0_WR_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_PIF_0_WR_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_PIF_1_RD_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_PIF_1_RD_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_AREA_PIF_1_WR_CLR   | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_AREA_PIF_1_WR_INT.    | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_SP_SPILL_MIN_CLR    | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_SP_SPILL_MIN_INT.     | (WT)  |   |    |       |     |
| ASSIST_DEBUG_CORE_1_SP_SPILL_MAX_CLR    | Write | 1 | to | clear | AS- |
| SIST_DEBUG_CORE_1_SP_SPILL_MAX_INT.     | (WT)  |   |    |       |     |



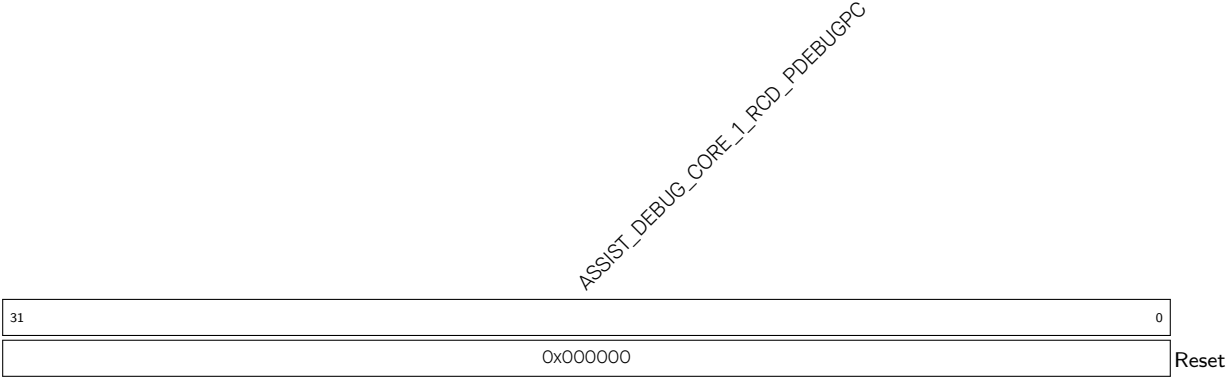
Register 19.65. ASSIST\_DEBUG\_CORE\_1\_RCD\_EN\_REG (0x00C4)



**ASSIST\_DEBUG\_CORE\_1\_RCD\_RECORDEN** Configures whether to enable HP CPU1 PC logging.  
0: Disable  
1: [ASSIST\\_DEBUG\\_CORE\\_1\\_RCD\\_PDEBUGPC\\_REG](#) starts to record HP CPU1 PC in real time (R/W)

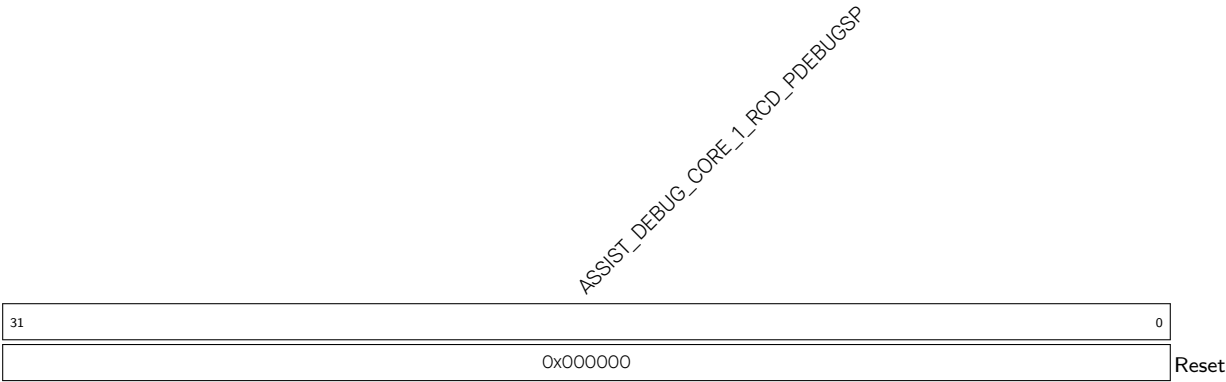
**ASSIST\_DEBUG\_CORE\_1\_RCD\_PDEBUGEN** Configures whether to enable HP CPU1 debugging.  
0: Disable  
1: HP CPU1 outputs HP CPU1 PC (R/W)

Register 19.66. ASSIST\_DEBUG\_CORE\_1\_RCD\_PDEBUGPC\_REG (0x00C8)



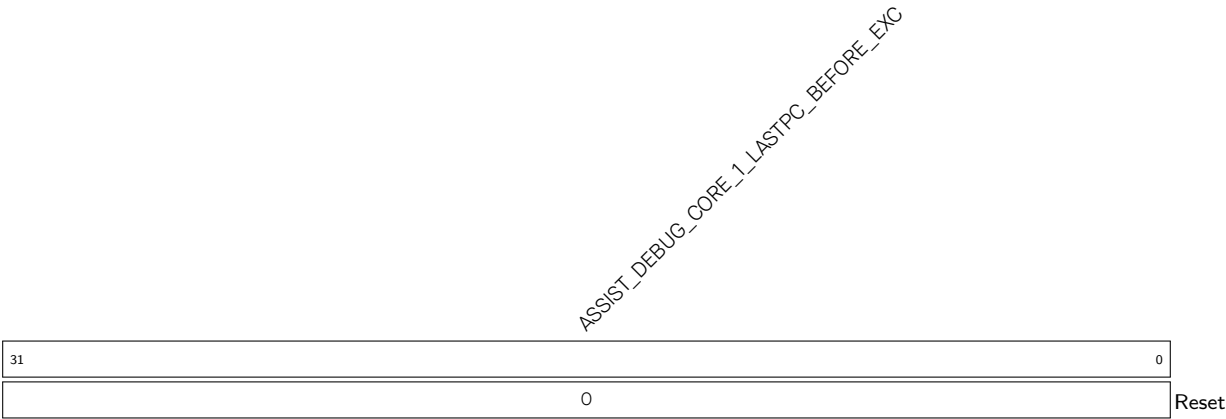
**ASSIST\_DEBUG\_CORE\_1\_RCD\_PDEBUGPC** Represents the PC value at HP CPU1 reset. (RO)

Register 19.67. ASSIST\_DEBUG\_CORE\_1\_RCD\_PDEBUGSP\_REG (0x00CC)



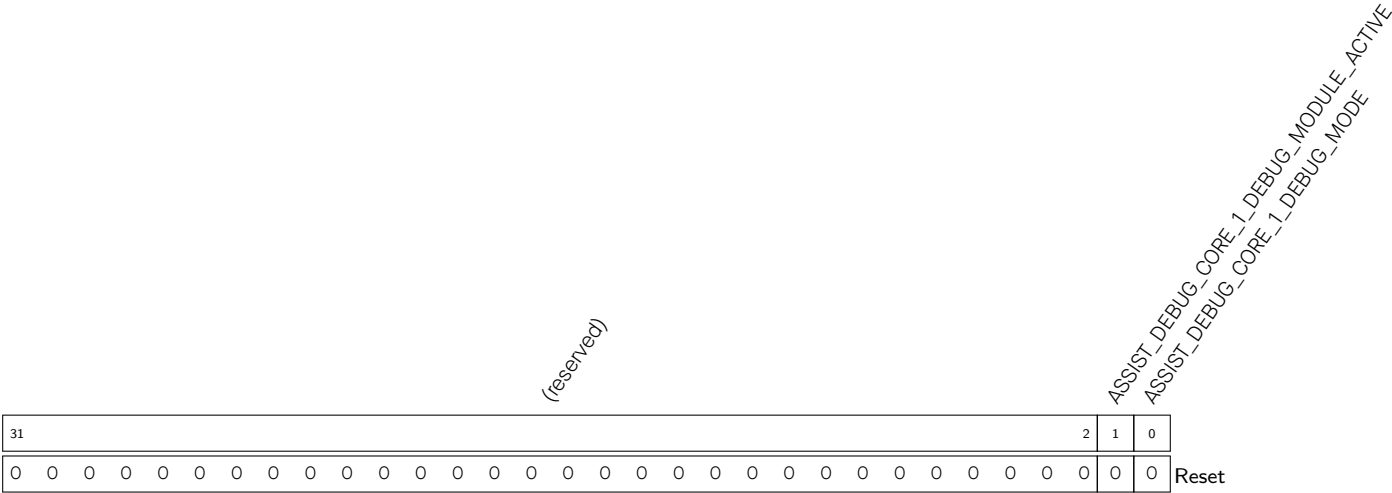
**ASSIST\_DEBUG\_CORE\_1\_RCD\_PDEBUGSP**   Represents the HP CPU1 SP. (RO)

Register 19.68. ASSIST\_DEBUG\_CORE\_1\_LASTPC\_BEFORE\_EXCEPTION\_REG (0x00F0)



**ASSIST\_DEBUG\_CORE\_1\_LASTPC\_BEFORE\_EXC**   Represents the HP CPU1 PC of the last command before the HP CPU1 enters exception. (RO)

Register 19.69. ASSIST\_DEBUG\_CORE\_1\_DEBUG\_MODE\_REG (0x00F4)



**ASSIST\_DEBUG\_CORE\_1\_DEBUG\_MODE** Represents whether HP CPU1 is in debugging mode.

- 1: In debugging mode
- 0: Not in debugging mode

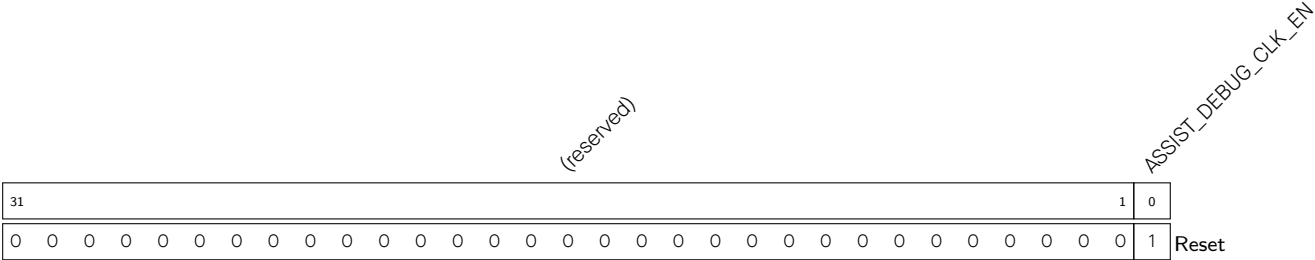
(RO)

**ASSIST\_DEBUG\_CORE\_1\_DEBUG\_MODULE\_ACTIVE** Represents the status of the HP CPU1 debug module.

- 1: Active status
- Other: Inactive status

(RO)

Register 19.70. ASSIST\_DEBUG\_CLOCK\_GATE\_REG (0x0108)



**ASSIST\_DEBUG\_CLK\_EN** Configures whether to enable the register clock gating.

- 0: Disable
- 1: Enable

(R/W)

Register 19.71. ASSIST\_DEBUG\_DATE\_REG (0x03FC)

|            |    |   |   |                   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|---|---|-------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |   |   | ASSIST_DEBUG_DATE |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 |   |   | 27                | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0 | 0 | 0x2109130         |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ASSIST\_DEBUG\_DATE**   Version control register. (R/W)

## Chapter 20

### LP Mailbox

#### 20.1 Overview

ESP32-P4 integrates an LP Mailbox module which provides an efficient inter-core communication mechanism between the LP CPU and HP CPU0/1. The LP Mailbox module comprises of sixteen 32-bit message registers that the LP CPU and HP CPU0/1 can use to store and exchange message. Inter-core communication between LP CPU and HP CPU0/1 is achieved through an interrupt mechanism implemented within the LP Mailbox module.

#### 20.2 Features

ESP32-P4 LP Mailbox has the following features:

- Sixteen 32-bit message registers for inter-core communication
- LP CPU external interrupt signal: [MB\\_LP\\_INTR](#)
- HP CPU<sub>x</sub> (<sub>x</sub>: 0 ~ 1) external interrupt signal: [MB\\_HP\\_INTR](#)

## 20.3 Functional Description

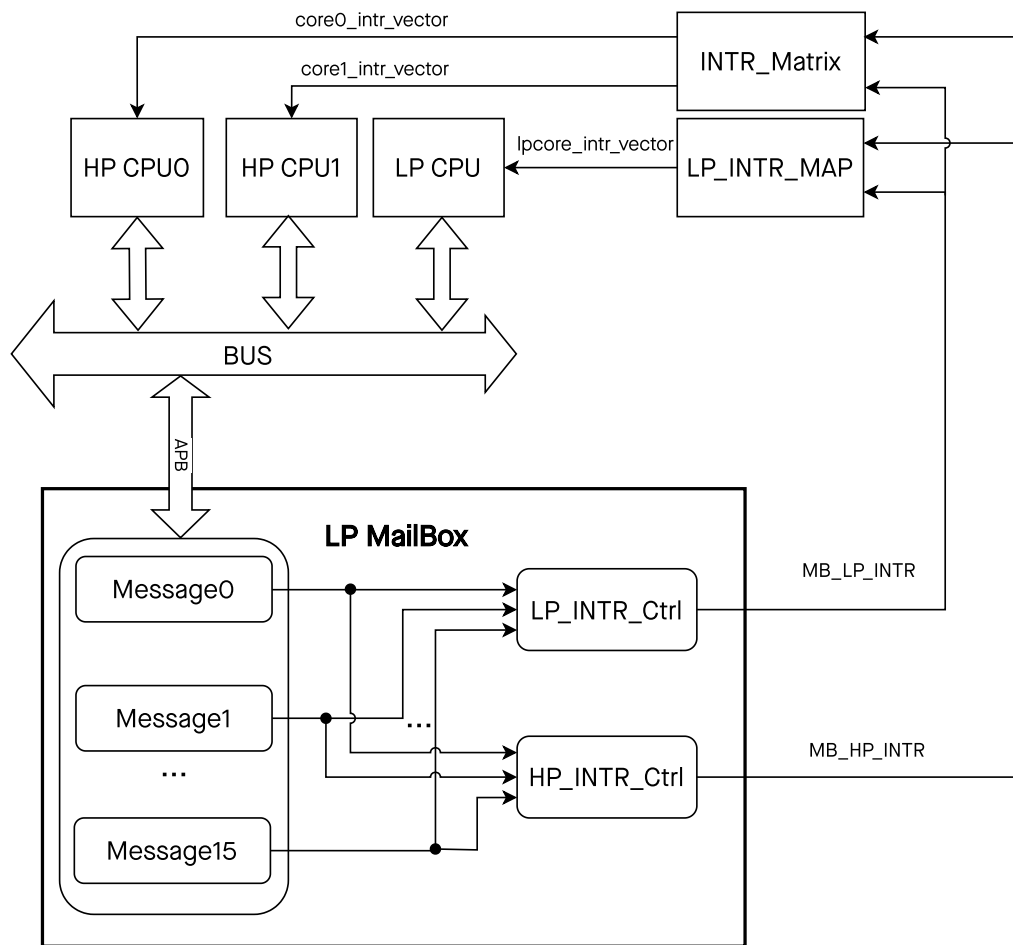


Figure 20.3-1. LP Mailbox Block Diagram

### 20.3.1 Message Registers

The LP Mailbox provides sixteen 32-bit message registers in total, denoted as [MB\\_MESSAGE\\_0\\_REG](#) ~ [MB\\_MESSAGE\\_15\\_REG](#), for caching inter-core communication messages. Both LP CPU and HP CPU0/1 can read and write these message registers to pass or retrieve message.

Read and write message registers is done through the APB bus, using APB\_CLK, which is the only one clock in LP Mailbox. For more information about the clock, please refer to Chapter 9 [Reset and Clock](#).

### 20.3.2 Interrupts

ESP32-P4 LP Mailbox can generate the following external interrupt signals:

- MB\_LP\_INTR
- MB\_HP\_INTR

MB\_LP\_INTR is directly mapped to LP CPU (see [Low-Power CPU](#)), and MB\_HP\_INTR can be mapped to HP CPU0/1 through the [Interrupt Matrix](#). These interrupt signals are generated by internal interrupt sources of the

LP Mailbox module. Table 20.3-1 lists the internal interrupt sources, interrupt trigger conditions, and generated interrupt signals of the LP Mailbox.

**Table 20.3-1. LP Mailbox's Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition                  | Interrupt Signal |
|---------------------------|------------------------------------|------------------|
| MB_HP_ <i>m</i> _INT      | Write to MB_MESSAGE_ <i>m</i> _REG | MB_HP_INTR       |
| MB_LP_ <i>n</i> _INT      | Write to MB_MESSAGE_ <i>n</i> _REG | MB_LP_INTR       |

**Note:**

- *m* and *n* can be 0 ~ 15.
- MB\_HP\_INTR can also serve as an external interrupt source for LP CPU and be mapped to LP CPU by LP\_INTR\_MAP as illustrated in Figure 20.3-1. For more information about LP\_INTR\_MAP, please refer to Chapter 2 *Low-Power CPU*.
- MB\_LP\_INTR can also serve as an external interrupt source for HP CPU<sub>x</sub> and can be mapped to HP CPU<sub>x</sub> through the *Interrupt Matrix*.
- When the LP Mailbox is required to assign different interrupt sources for HP CPU0 and HP CPU1, it can map MB\_HP\_INTR and MB\_LP\_INTR independently to HP CPU0 and HP CPU1 using the *Interrupt Matrix*.

### 20.3.3 Inter-Core Communication

When communication is required between LP CPU and HP CPU<sub>x</sub>, subset of or all message registers in the LP Mailbox can be utilized to share message as needed. The synchronization of message can be achieved through the corresponding interrupts. During communication, software must ensure that only the sender is allowed to write to the message registers to prevent data corruption.

- Example of initiating communication from HP CPU0 to LP CPU using MB\_MESSAGE\_*n*\_REG:
  - Set MB\_LP\_*n*\_INT\_ENA to enable the MB\_LP\_*n*\_INT interrupt.
  - HP CPU0 writes to MB\_MASSEGE\_*n*\_REG, caching shared message.
  - LP CPU checks MB\_LP\_INT\_ST\_REG interrupt status register, finding the MB\_LP\_*n*\_ST status bit set.
  - LP CPU reads MB\_MASSEGE\_*n*\_REG to retrieve shared message.
- Example of initiating communication from LP CPU to HP CPU0:
  - Set MB\_HP\_*m*\_INT\_ENA to enable the MB\_HP\_*m*\_INT interrupt.
  - Configure the *Interrupt Matrix* to map MB\_HP\_INTR to HP CPU0. See Chapter 11 *Interrupt Matrix*.
  - LP CPU writes to MB\_MASSEGE\_*m*\_REG, caching shared messages.
  - HP CPU0 checks the MB\_HP\_INT\_ST\_REG interrupt status register, finding the MB\_HP\_*m*\_ST status bit set.
  - HP CPU0 reads MB\_MASSEGE\_*m*\_REG to retrieve shared messages.

## 20.4 Register Summary

The addresses in this section are relative to LP Mailbox base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                              | Description            | Address | Access |
|-----------------------------------|------------------------|---------|--------|
| <b>Configuration Registers</b>    |                        |         |        |
| <a href="#">MB_MASSEGE_0_REG</a>  | Message register 0     | 0x0000  | R/W    |
| <a href="#">MB_MASSEGE_1_REG</a>  | Message register 1     | 0x0004  | R/W    |
| <a href="#">MB_MASSEGE_2_REG</a>  | Message register 2     | 0x0008  | R/W    |
| <a href="#">MB_MASSEGE_3_REG</a>  | Message register 3     | 0x000C  | R/W    |
| <a href="#">MB_MASSEGE_4_REG</a>  | Message register 4     | 0x0010  | R/W    |
| <a href="#">MB_MASSEGE_5_REG</a>  | Message register 5     | 0x0014  | R/W    |
| <a href="#">MB_MASSEGE_6_REG</a>  | Message register 6     | 0x0018  | R/W    |
| <a href="#">MB_MASSEGE_7_REG</a>  | Message register 7     | 0x001C  | R/W    |
| <a href="#">MB_MASSEGE_8_REG</a>  | Message register 8     | 0x0020  | R/W    |
| <a href="#">MB_MASSEGE_9_REG</a>  | Message register 9     | 0x0024  | R/W    |
| <a href="#">MB_MASSEGE_10_REG</a> | Message register 10    | 0x0028  | R/W    |
| <a href="#">MB_MASSEGE_11_REG</a> | Message register 11    | 0x002C  | R/W    |
| <a href="#">MB_MASSEGE_12_REG</a> | Message register 12    | 0x0030  | R/W    |
| <a href="#">MB_MASSEGE_13_REG</a> | Message register 13    | 0x0034  | R/W    |
| <a href="#">MB_MASSEGE_14_REG</a> | Message register 14    | 0x0038  | R/W    |
| <a href="#">MB_MASSEGE_15_REG</a> | Message register 15    | 0x003C  | R/W    |
| <a href="#">MB_REG_CLK_EN_REG</a> | Clock gate register    | 0x0060  | R/W    |
| <b>Interrupt Registers</b>        |                        |         |        |
| <a href="#">MB_LP_INT_RAW_REG</a> | MB_LP_INTR raw bits    | 0x0040  | RO     |
| <a href="#">MB_LP_INT_ST_REG</a>  | MB_LP_INTR status bits | 0x0044  | RO     |
| <a href="#">MB_LP_INT_ENA_REG</a> | MB_LP_INTR enable bits | 0x0048  | R/W    |
| <a href="#">MB_LP_INT_CLR_REG</a> | MB_LP_INTR clear bits  | 0x004C  | WO     |
| <a href="#">MB_HP_INT_RAW_REG</a> | MB_HP_INTR raw bits    | 0x0050  | RO     |
| <a href="#">MB_HP_INT_ST_REG</a>  | MB_HP_INTR status bits | 0x0054  | RO     |
| <a href="#">MB_HP_INT_ENA_REG</a> | MB_HP_INTR enable bits | 0x0058  | R/W    |
| <a href="#">MB_HP_INT_CLR_REG</a> | MB_HP_INTR clear bits  | 0x005C  | WO     |

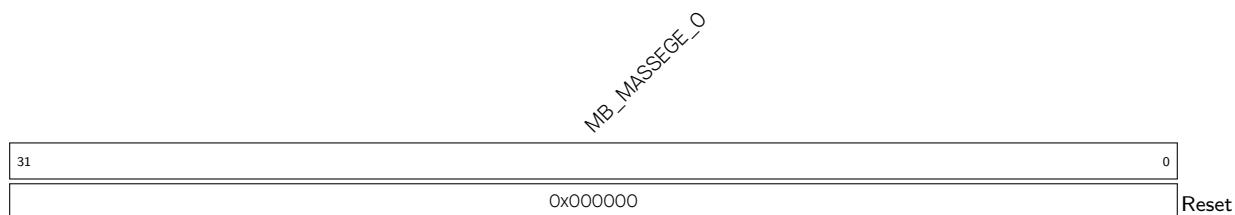
## 20.5 Registers

The addresses in this section are relative to LP Mailbox base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

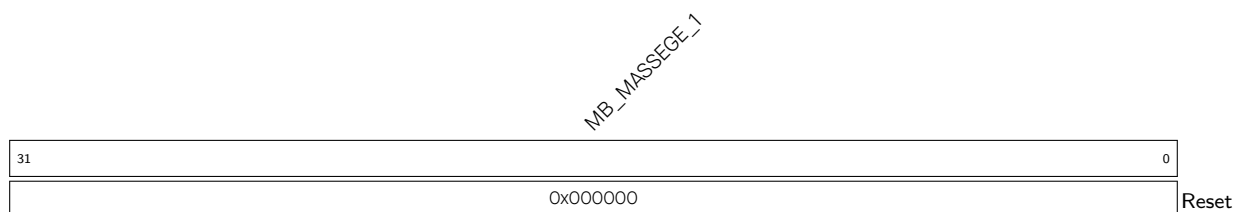


## Register 20.1. MB\_MASSEGE\_O\_REG (0x0000)



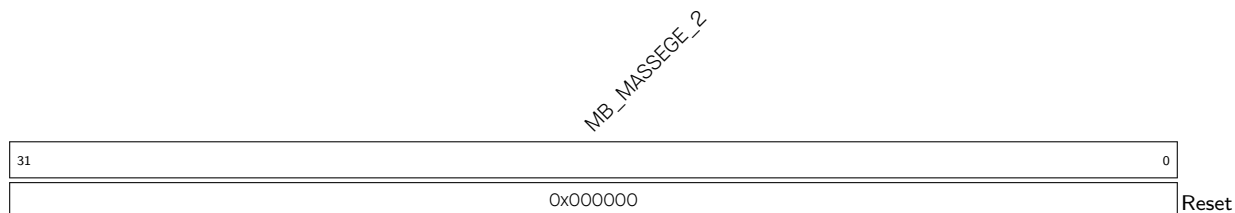
**MB\_MASSEGE\_O** Message register 0. (R/W)

## Register 20.2. MB\_MASSEGE\_1\_REG (0x0004)



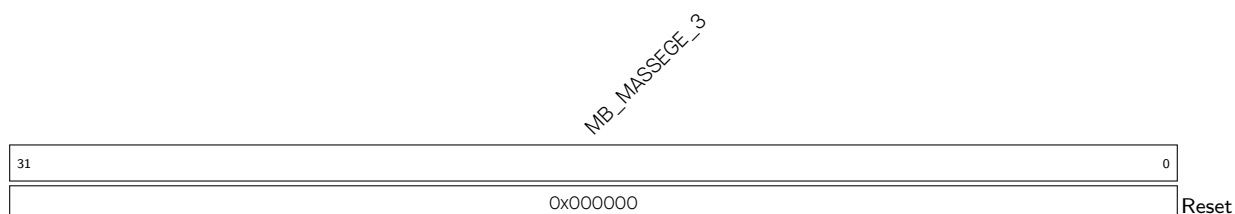
**MB\_MASSEGE\_1** Message register 1. (R/W)

## Register 20.3. MB\_MASSEGE\_2\_REG (0x0008)



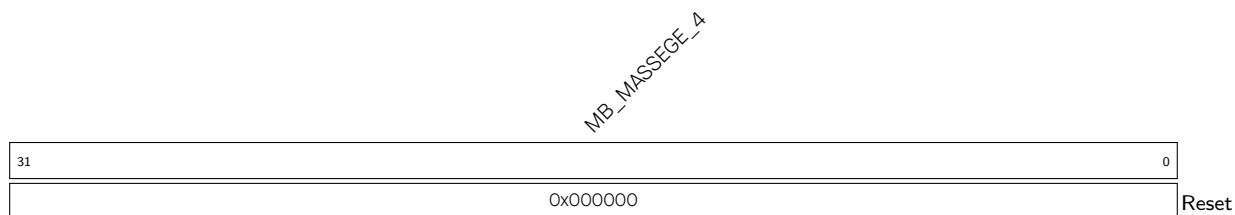
**MB\_MASSEGE\_2** Message register 2. (R/W)

## Register 20.4. MB\_MASSEGE\_3\_REG (0x000C)



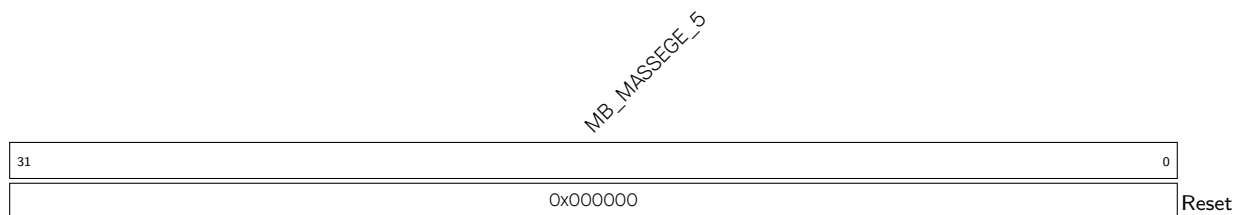
**MB\_MASSEGE\_3** Message register 3. (R/W)

## Register 20.5. MB\_MASSEGE\_4\_REG (0x0010)



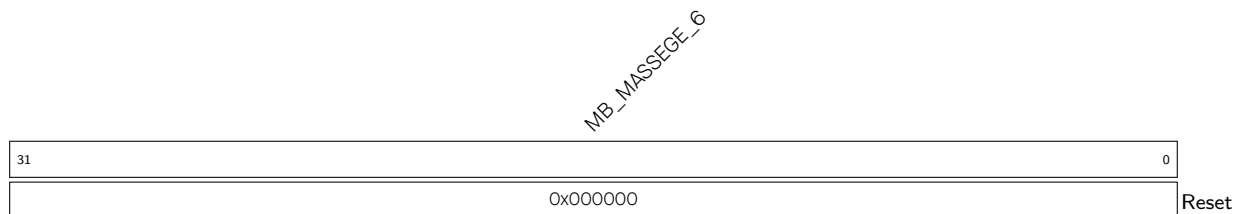
**MB\_MASSEGE\_4** Message register 4. (R/W)

## Register 20.6. MB\_MASSEGE\_5\_REG (0x0014)



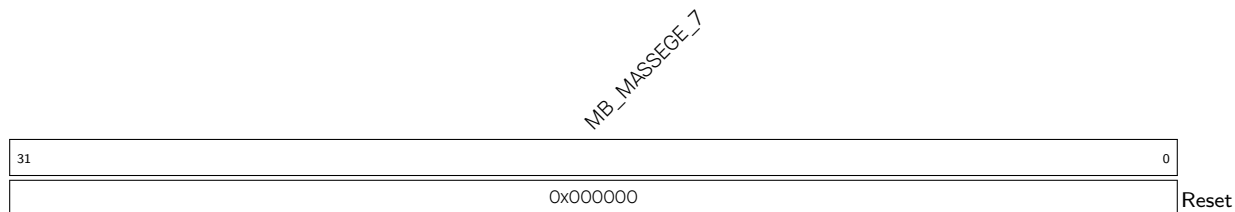
**MB\_MASSEGE\_5** Message register 5. (R/W)

## Register 20.7. MB\_MASSEGE\_6\_REG (0x0018)



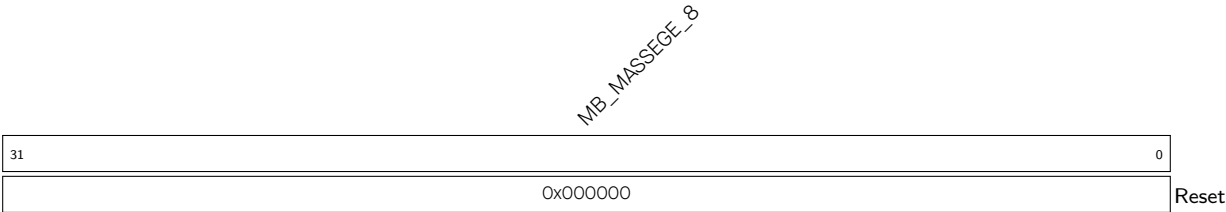
**MB\_MASSEGE\_6** Message register 6. (R/W)

## Register 20.8. MB\_MASSEGE\_7\_REG (0x001C)



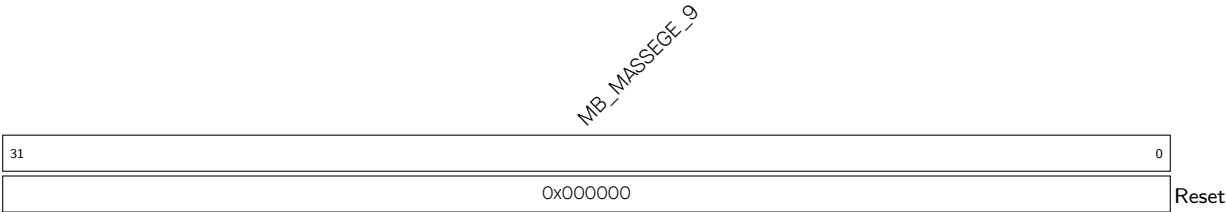
**MB\_MASSEGE\_7** Message register 7. (R/W)

Register 20.9. MB\_MASSEGE\_8\_REG (0x0020)



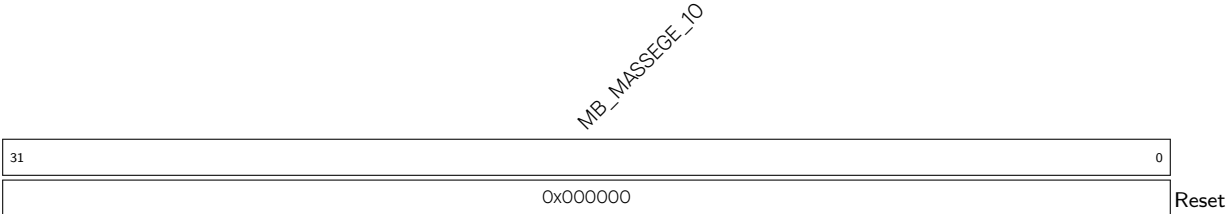
**MB\_MASSEGE\_8** Message register 8. (R/W)

Register 20.10. MB\_MASSEGE\_9\_REG (0x0024)



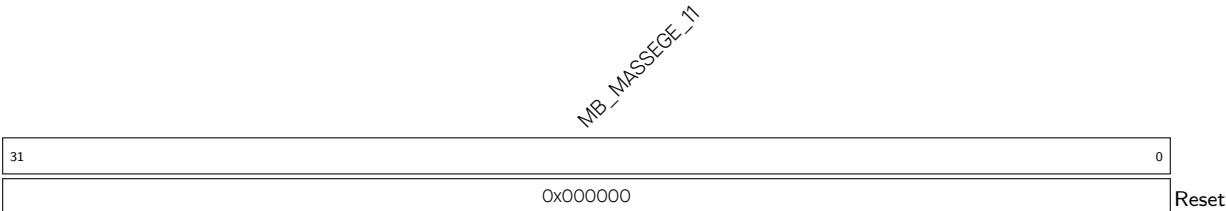
**MB\_MASSEGE\_9** Message register 9. (R/W)

Register 20.11. MB\_MASSEGE\_10\_REG (0x0028)

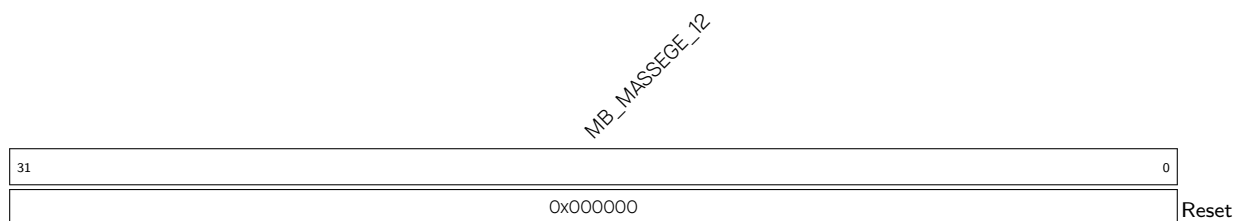
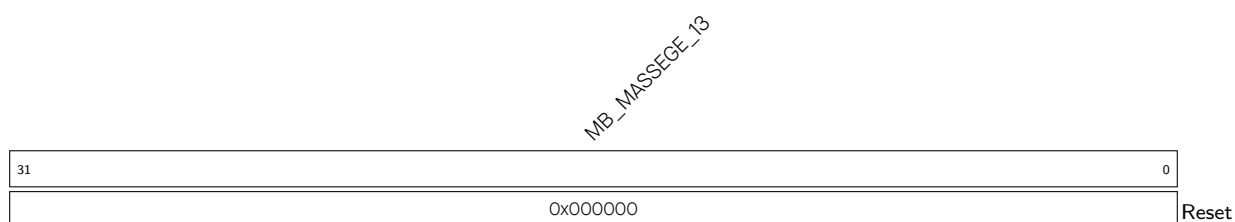
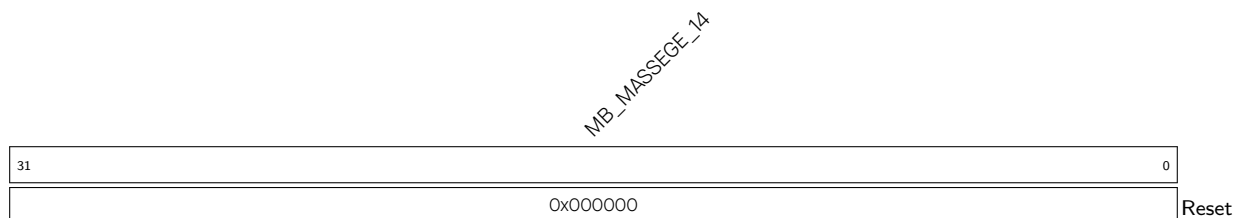
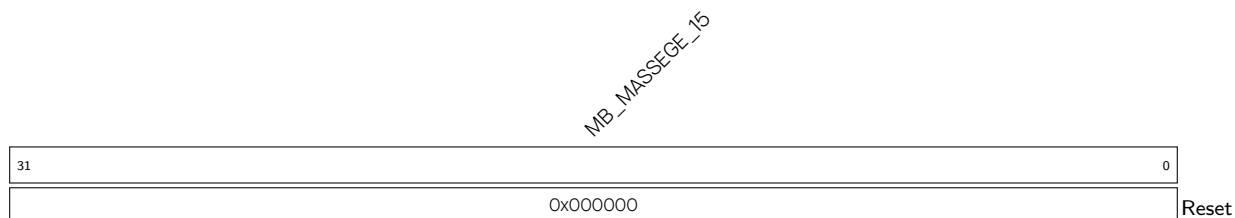


**MB\_MASSEGE\_10** Message register 10. (R/W)

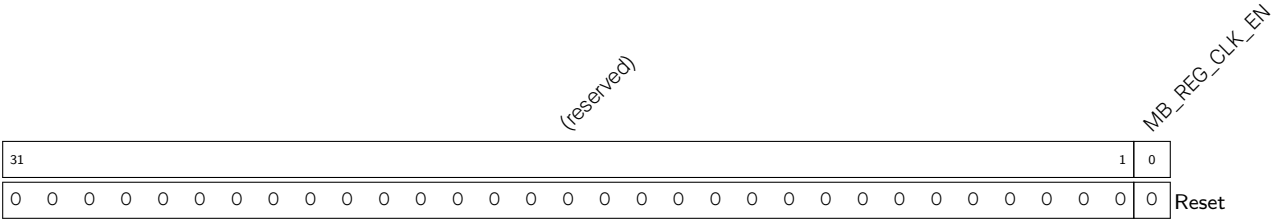
Register 20.12. MB\_MASSEGE\_11\_REG (0x002C)



**MB\_MASSEGE\_11** Message register 11. (R/W)

**Register 20.13. MB\_MASSEGE\_12\_REG (0x0030)****MB\_MASSEGE\_12** Message register 12. (R/W)**Register 20.14. MB\_MASSEGE\_13\_REG (0x0034)****MB\_MASSEGE\_13** Message register 13. (R/W)**Register 20.15. MB\_MASSEGE\_14\_REG (0x0038)****MB\_MASSEGE\_14** Message register 14. (R/W)**Register 20.16. MB\_MASSEGE\_15\_REG (0x003C)****MB\_MASSEGE\_15** Message register 15. (R/W)

Register 20.17. MB\_REG\_CLK\_EN\_REG (0x0060)



**MB\_REG\_CLK\_EN** Configures register clock gating.

- 1: Register clock is always enabled for read and write operations.
- 0: Only enable clock for register read or write operations.

(R/W)

Register 20.18. MB\_LP\_INT\_RAW\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |    |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|----|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_15_INT_RAW<br>MB_LP_14_INT_RAW<br>MB_LP_13_INT_RAW<br>MB_LP_12_INT_RAW<br>MB_LP_11_INT_RAW<br>MB_LP_10_INT_RAW<br>MB_LP_9_INT_RAW<br>MB_LP_8_INT_RAW<br>MB_LP_7_INT_RAW<br>MB_LP_6_INT_RAW<br>MB_LP_5_INT_RAW<br>MB_LP_4_INT_RAW<br>MB_LP_3_INT_RAW<br>MB_LP_2_INT_RAW<br>MB_LP_1_INT_RAW<br>MB_LP_0_INT_RAW |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |    |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 31   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       | 16 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |    |

**MB\_LP\_0\_INT\_RAW** The raw interrupt bit of the MB\_LP\_0\_INT interrupt. (RO)

**MB\_LP\_1\_INT\_RAW** The raw interrupt bit of the MB\_LP\_1\_INT interrupt. (RO)

**MB\_LP\_2\_INT\_RAW** The raw interrupt bit of the MB\_LP\_2\_INT interrupt. (RO)

**MB\_LP\_3\_INT\_RAW** The raw interrupt bit of the MB\_LP\_3\_INT interrupt. (RO)

**MB\_LP\_4\_INT\_RAW** The raw interrupt bit of the MB\_LP\_4\_INT interrupt. (RO)

**MB\_LP\_5\_INT\_RAW** The raw interrupt bit of the MB\_LP\_5\_INT interrupt. (RO)

**MB\_LP\_6\_INT\_RAW** The raw interrupt bit of the MB\_LP\_6\_INT interrupt. (RO)

**MB\_LP\_7\_INT\_RAW** The raw interrupt bit of the MB\_LP\_7\_INT interrupt. (RO)

**MB\_LP\_8\_INT\_RAW** The raw interrupt bit of the MB\_LP\_8\_INT interrupt. (RO)

**MB\_LP\_9\_INT\_RAW** The raw interrupt bit of the MB\_LP\_9\_INT interrupt. (RO)

**MB\_LP\_10\_INT\_RAW** The raw interrupt bit of the MB\_LP\_10\_INT interrupt. (RO)

**MB\_LP\_11\_INT\_RAW** The raw interrupt bit of the MB\_LP\_11\_INT interrupt. (RO)

**MB\_LP\_12\_INT\_RAW** The raw interrupt bit of the MB\_LP\_12\_INT interrupt. (RO)

**MB\_LP\_13\_INT\_RAW** The raw interrupt bit of the MB\_LP\_13\_INT interrupt. (RO)

**MB\_LP\_14\_INT\_RAW** The raw interrupt bit of the MB\_LP\_14\_INT interrupt. (RO)

**MB\_LP\_15\_INT\_RAW** The raw interrupt bit of the MB\_LP\_15\_INT interrupt. (RO)

Register 20.19. MB\_LP\_INT\_ST\_REG (0x0044)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_15_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_14_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_13_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_12_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_11_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_10_INT_ST |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_9_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_8_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_7_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_6_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_5_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_4_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_3_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_2_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_1_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_LP_0_INT_ST  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MB\_LP\_0\_INT\_ST** The masked interrupt status bit of the MB\_LP\_0\_INT interrupt. (RO)

**MB\_LP\_1\_INT\_ST** The masked interrupt status bit of the MB\_LP\_1\_INT interrupt. (RO)

**MB\_LP\_2\_INT\_ST** The masked interrupt status bit of the MB\_LP\_2\_INT interrupt. (RO)

**MB\_LP\_3\_INT\_ST** The masked interrupt status bit of the MB\_LP\_3\_INT interrupt. (RO)

**MB\_LP\_4\_INT\_ST** The masked interrupt status bit of the MB\_LP\_4\_INT interrupt. (RO)

**MB\_LP\_5\_INT\_ST** The masked interrupt status bit of the MB\_LP\_5\_INT interrupt. (RO)

**MB\_LP\_6\_INT\_ST** The masked interrupt status bit of the MB\_LP\_6\_INT interrupt. (RO)

**MB\_LP\_7\_INT\_ST** The masked interrupt status bit of the MB\_LP\_7\_INT interrupt. (RO)

**MB\_LP\_8\_INT\_ST** The masked interrupt status bit of the MB\_LP\_8\_INT interrupt. (RO)

**MB\_LP\_9\_INT\_ST** The masked interrupt status bit of the MB\_LP\_9\_INT interrupt. (RO)

**MB\_LP\_10\_INT\_ST** The masked interrupt status bit of the MB\_LP\_10\_INT interrupt. (RO)

**MB\_LP\_11\_INT\_ST** The masked interrupt status bit of the MB\_LP\_11\_INT interrupt. (RO)

**MB\_LP\_12\_INT\_ST** The masked interrupt status bit of the MB\_LP\_12\_INT interrupt. (RO)

**MB\_LP\_13\_INT\_ST** The masked interrupt status bit of the MB\_LP\_13\_INT interrupt. (RO)

**MB\_LP\_14\_INT\_ST** The masked interrupt status bit of the MB\_LP\_14\_INT interrupt. (RO)

**MB\_LP\_15\_INT\_ST** The masked interrupt status bit of the MB\_LP\_15\_INT interrupt. (RO)

**Register 20.20. MB\_LP\_INT\_ENA\_REG (0x0048)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |       |  |    |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|----|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_15_INT_ENA<br>MB_LP_14_INT_ENA<br>MB_LP_13_INT_ENA<br>MB_LP_12_INT_ENA<br>MB_LP_11_INT_ENA<br>MB_LP_10_INT_ENA<br>MB_LP_9_INT_ENA<br>MB_LP_8_INT_ENA<br>MB_LP_7_INT_ENA<br>MB_LP_6_INT_ENA<br>MB_LP_5_INT_ENA<br>MB_LP_4_INT_ENA<br>MB_LP_3_INT_ENA<br>MB_LP_2_INT_ENA<br>MB_LP_1_INT_ENA<br>MB_LP_0_INT_ENA |   |   |   |   |   |   |   |   |   |   |   |   |       |  |    |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 31   |   |   |   |   |   |   |   |   |   |   |   |   |       |  | 16 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |  |    |

**MB\_LP\_0\_INT\_ENA** Write 1 to enable the MB\_LP\_0\_INT interrupt. (R/W)

**MB\_LP\_1\_INT\_ENA** Write 1 to enable the MB\_LP\_1\_INT interrupt. (R/W)

**MB\_LP\_2\_INT\_ENA** Write 1 to enable the MB\_LP\_2\_INT interrupt. (R/W)

**MB\_LP\_3\_INT\_ENA** Write 1 to enable the MB\_LP\_3\_INT interrupt. (R/W)

**MB\_LP\_4\_INT\_ENA** Write 1 to enable the MB\_LP\_4\_INT interrupt. (R/W)

**MB\_LP\_5\_INT\_ENA** Write 1 to enable the MB\_LP\_5\_INT interrupt. (R/W)

**MB\_LP\_6\_INT\_ENA** Write 1 to enable the MB\_LP\_6\_INT interrupt. (R/W)

**MB\_LP\_7\_INT\_ENA** Write 1 to enable the MB\_LP\_7\_INT interrupt. (R/W)

**MB\_LP\_8\_INT\_ENA** Write 1 to enable the MB\_LP\_8\_INT interrupt. (R/W)

**MB\_LP\_9\_INT\_ENA** Write 1 to enable the MB\_LP\_9\_INT interrupt. (R/W)

**MB\_LP\_10\_INT\_ENA** Write 1 to enable the MB\_LP\_10\_INT interrupt. (R/W)

**MB\_LP\_11\_INT\_ENA** Write 1 to enable the MB\_LP\_11\_INT interrupt. (R/W)

**MB\_LP\_12\_INT\_ENA** Write 1 to enable the MB\_LP\_12\_INT interrupt. (R/W)

**MB\_LP\_13\_INT\_ENA** Write 1 to enable the MB\_LP\_13\_INT interrupt. (R/W)

**MB\_LP\_14\_INT\_ENA** Write 1 to enable the MB\_LP\_14\_INT interrupt. (R/W)

**MB\_LP\_15\_INT\_ENA** Write 1 to enable the MB\_LP\_15\_INT interrupt. (R/W)



**Register 20.21. MB\_LP\_INT\_CLR\_REG (0x004C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_15_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_14_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_13_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_12_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_11_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_10_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_9_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_8_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_7_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_6_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_5_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_4_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_3_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_2_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_1_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_LP_0_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16               | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |       |

**MB\_LP\_0\_INT\_CLR** Write 1 to clear the MB\_LP\_0\_INT interrupt. (WO)

**MB\_LP\_1\_INT\_CLR** Write 1 to clear the MB\_LP\_1\_INT interrupt. (WO)

**MB\_LP\_2\_INT\_CLR** Write 1 to clear the MB\_LP\_2\_INT interrupt. (WO)

**MB\_LP\_3\_INT\_CLR** Write 1 to clear the MB\_LP\_3\_INT interrupt. (WO)

**MB\_LP\_4\_INT\_CLR** Write 1 to clear the MB\_LP\_4\_INT interrupt. (WO)

**MB\_LP\_5\_INT\_CLR** Write 1 to clear the MB\_LP\_5\_INT interrupt. (WO)

**MB\_LP\_6\_INT\_CLR** Write 1 to clear the MB\_LP\_6\_INT interrupt. (WO)

**MB\_LP\_7\_INT\_CLR** Write 1 to clear the MB\_LP\_7\_INT interrupt. (WO)

**MB\_LP\_8\_INT\_CLR** Write 1 to clear the MB\_LP\_8\_INT interrupt. (WO)

**MB\_LP\_9\_INT\_CLR** Write 1 to clear the MB\_LP\_9\_INT interrupt. (WO)

**MB\_LP\_10\_INT\_CLR** Write 1 to clear the MB\_LP\_10\_INT interrupt. (WO)

**MB\_LP\_11\_INT\_CLR** Write 1 to clear the MB\_LP\_11\_INT interrupt. (WO)

**MB\_LP\_12\_INT\_CLR** Write 1 to clear the MB\_LP\_12\_INT interrupt. (WO)

**MB\_LP\_13\_INT\_CLR** Write 1 to clear the MB\_LP\_13\_INT interrupt. (WO)

**MB\_LP\_14\_INT\_CLR** Write 1 to clear the MB\_LP\_14\_INT interrupt. (WO)

**MB\_LP\_15\_INT\_CLR** Write 1 to clear the MB\_LP\_15\_INT interrupt. (WO)

Register 20.22. MB\_HP\_INT\_RAW\_REG (0x0050)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_15_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_14_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_13_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_12_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_11_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_10_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_9_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_8_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_7_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_6_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_5_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_4_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_3_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_2_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_1_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MB_HP_0_INT_RAW  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MB\_HP\_0\_INT\_RAW** The raw interrupt bit of the MB\_HP\_0\_INT interrupt. (RO)

**MB\_HP\_1\_INT\_RAW** The raw interrupt bit of the MB\_HP\_1\_INT interrupt. (RO)

**MB\_HP\_2\_INT\_RAW** The raw interrupt bit of the MB\_HP\_2\_INT interrupt. (RO)

**MB\_HP\_3\_INT\_RAW** The raw interrupt bit of the MB\_HP\_3\_INT interrupt. (RO)

**MB\_HP\_4\_INT\_RAW** The raw interrupt bit of the MB\_HP\_4\_INT interrupt. (RO)

**MB\_HP\_5\_INT\_RAW** The raw interrupt bit of the MB\_HP\_5\_INT interrupt. (RO)

**MB\_HP\_6\_INT\_RAW** The raw interrupt bit of the MB\_HP\_6\_INT interrupt. (RO)

**MB\_HP\_7\_INT\_RAW** The raw interrupt bit of the MB\_HP\_7\_INT interrupt. (RO)

**MB\_HP\_8\_INT\_RAW** The raw interrupt bit of the MB\_HP\_8\_INT interrupt. (RO)

**MB\_HP\_9\_INT\_RAW** The raw interrupt bit of the MB\_HP\_9\_INT interrupt. (RO)

**MB\_HP\_10\_INT\_RAW** The raw interrupt bit of the MB\_HP\_10\_INT interrupt. (RO)

**MB\_HP\_11\_INT\_RAW** The raw interrupt bit of the MB\_HP\_11\_INT interrupt. (RO)

**MB\_HP\_12\_INT\_RAW** The raw interrupt bit of the MB\_HP\_12\_INT interrupt. (RO)

**MB\_HP\_13\_INT\_RAW** The raw interrupt bit of the MB\_HP\_13\_INT interrupt. (RO)

**MB\_HP\_14\_INT\_RAW** The raw interrupt bit of the MB\_HP\_14\_INT interrupt. (RO)

**MB\_HP\_15\_INT\_RAW** The raw interrupt bit of the MB\_HP\_15\_INT interrupt. (RO)

**Register 20.23. MB\_HP\_INT\_ST\_REG (0x0054)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_15_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_14_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_13_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_12_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_11_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_10_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_9_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_8_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_7_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_6_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_5_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_4_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_3_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_2_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_1_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_0_INT_ST  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16              | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 |   |   |   |   |   |   |       |

**MB\_HP\_0\_INT\_ST** The masked interrupt status bit of the MB\_HP\_0\_INT interrupt. (RO)

**MB\_HP\_1\_INT\_ST** The masked interrupt status bit of the MB\_HP\_1\_INT interrupt. (RO)

**MB\_HP\_2\_INT\_ST** The masked interrupt status bit of the MB\_HP\_2\_INT interrupt. (RO)

**MB\_HP\_3\_INT\_ST** The masked interrupt status bit of the MB\_HP\_3\_INT interrupt. (RO)

**MB\_HP\_4\_INT\_ST** The masked interrupt status bit of the MB\_HP\_4\_INT interrupt. (RO)

**MB\_HP\_5\_INT\_ST** The masked interrupt status bit of the MB\_HP\_5\_INT interrupt. (RO)

**MB\_HP\_6\_INT\_ST** The masked interrupt status bit of the MB\_HP\_6\_INT interrupt. (RO)

**MB\_HP\_7\_INT\_ST** The masked interrupt status bit of the MB\_HP\_7\_INT interrupt. (RO)

**MB\_HP\_8\_INT\_ST** The masked interrupt status bit of the MB\_HP\_8\_INT interrupt. (RO)

**MB\_HP\_9\_INT\_ST** The masked interrupt status bit of the MB\_HP\_9\_INT interrupt. (RO)

**MB\_HP\_10\_INT\_ST** The masked interrupt status bit of the MB\_HP\_10\_INT interrupt. (RO)

**MB\_HP\_11\_INT\_ST** The masked interrupt status bit of the MB\_HP\_11\_INT interrupt. (RO)

**MB\_HP\_12\_INT\_ST** The masked interrupt status bit of the MB\_HP\_12\_INT interrupt. (RO)

**MB\_HP\_13\_INT\_ST** The masked interrupt status bit of the MB\_HP\_13\_INT interrupt. (RO)

**MB\_HP\_14\_INT\_ST** The masked interrupt status bit of the MB\_HP\_14\_INT interrupt. (RO)

**MB\_HP\_15\_INT\_ST** The masked interrupt status bit of the MB\_HP\_15\_INT interrupt. (RO)

**Register 20.24. MB\_HP\_INT\_ENA\_REG (0x0058)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |    |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|----|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_15_INT_ENA<br>MB_HP_14_INT_ENA<br>MB_HP_13_INT_ENA<br>MB_HP_12_INT_ENA<br>MB_HP_11_INT_ENA<br>MB_HP_10_INT_ENA<br>MB_HP_9_INT_ENA<br>MB_HP_8_INT_ENA<br>MB_HP_7_INT_ENA<br>MB_HP_6_INT_ENA<br>MB_HP_5_INT_ENA<br>MB_HP_4_INT_ENA<br>MB_HP_3_INT_ENA<br>MB_HP_2_INT_ENA<br>MB_HP_1_INT_ENA<br>MB_HP_0_INT_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |    |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 31   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  | 16 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | Reset |  |    |

**MB\_HP\_0\_INT\_ENA** Write 1 to enable the MB\_HP\_0\_INT interrupt. (R/W)

**MB\_HP\_1\_INT\_ENA** Write 1 to enable the MB\_HP\_1\_INT interrupt. (R/W)

**MB\_HP\_2\_INT\_ENA** Write 1 to enable the MB\_HP\_2\_INT interrupt. (R/W)

**MB\_HP\_3\_INT\_ENA** Write 1 to enable the MB\_HP\_3\_INT interrupt. (R/W)

**MB\_HP\_4\_INT\_ENA** Write 1 to enable the MB\_HP\_4\_INT interrupt. (R/W)

**MB\_HP\_5\_INT\_ENA** Write 1 to enable the MB\_HP\_5\_INT interrupt. (R/W)

**MB\_HP\_6\_INT\_ENA** Write 1 to enable the MB\_HP\_6\_INT interrupt. (R/W)

**MB\_HP\_7\_INT\_ENA** Write 1 to enable the MB\_HP\_7\_INT interrupt. (R/W)

**MB\_HP\_8\_INT\_ENA** Write 1 to enable the MB\_HP\_8\_INT interrupt. (R/W)

**MB\_HP\_9\_INT\_ENA** Write 1 to enable the MB\_HP\_9\_INT interrupt. (R/W)

**MB\_HP\_10\_INT\_ENA** Write 1 to enable the MB\_HP\_10\_INT interrupt. (R/W)

**MB\_HP\_11\_INT\_ENA** Write 1 to enable the MB\_HP\_11\_INT interrupt. (R/W)

**MB\_HP\_12\_INT\_ENA** Write 1 to enable the MB\_HP\_12\_INT interrupt. (R/W)

**MB\_HP\_13\_INT\_ENA** Write 1 to enable the MB\_HP\_13\_INT interrupt. (R/W)

**MB\_HP\_14\_INT\_ENA** Write 1 to enable the MB\_HP\_14\_INT interrupt. (R/W)

**MB\_HP\_15\_INT\_ENA** Write 1 to enable the MB\_HP\_15\_INT interrupt. (R/W)

**Register 20.25. MB\_HP\_INT\_CLR\_REG (0x005C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_15_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_14_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_13_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_12_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_11_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_10_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_9_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_8_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_7_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_6_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_5_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_4_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_3_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_2_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_1_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MB_HP_0_INT_CLR  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16               | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |       |

**MB\_HP\_0\_INT\_CLR** Write 1 to clear the MB\_HP\_0\_INT interrups. (WO)

**MB\_HP\_1\_INT\_CLR** Write 1 to clear the MB\_HP\_1\_INT interrups. (WO)

**MB\_HP\_2\_INT\_CLR** Write 1 to clear the MB\_HP\_2\_INT interrups. (WO)

**MB\_HP\_3\_INT\_CLR** Write 1 to clear the MB\_HP\_3\_INT interrups. (WO)

**MB\_HP\_4\_INT\_CLR** Write 1 to clear the MB\_HP\_4\_INT interrups. (WO)

**MB\_HP\_5\_INT\_CLR** Write 1 to clear the MB\_HP\_5\_INT interrups. (WO)

**MB\_HP\_6\_INT\_CLR** Write 1 to clear the MB\_HP\_6\_INT interrups. (WO)

**MB\_HP\_7\_INT\_CLR** Write 1 to clear the MB\_HP\_7\_INT interrups. (WO)

**MB\_HP\_8\_INT\_CLR** Write 1 to clear the MB\_HP\_8\_INT interrups. (WO)

**MB\_HP\_9\_INT\_CLR** Write 1 to clear the MB\_HP\_9\_INT interrups. (WO)

**MB\_HP\_10\_INT\_CLR** Write 1 to clear the MB\_HP\_10\_INT interrups. (WO)

**MB\_HP\_11\_INT\_CLR** Write 1 to clear the MB\_HP\_11\_INT interrups. (WO)

**MB\_HP\_12\_INT\_CLR** Write 1 to clear the MB\_HP\_12\_INT interrups. (WO)

**MB\_HP\_13\_INT\_CLR** Write 1 to clear the MB\_HP\_13\_INT interrups. (WO)

**MB\_HP\_14\_INT\_CLR** Write 1 to clear the MB\_HP\_14\_INT interrups. (WO)

**MB\_HP\_15\_INT\_CLR** Write 1 to clear the MB\_HP\_15\_INT interrups. (WO)

## Chapter 21

### Brown-out Detector

#### 21.1 Introduction

The brown-out detector of ESP32-P4 monitors the voltage levels of pins VDD\_ANA and VDD\_BAT. If the voltage on these pins drops below the predefined threshold (defaulting to 2.7 V), the detector triggers signals to shut down certain power-consuming blocks (e.g., flash), ensuring that the digital module has sufficient time to save and transfer important data.

#### 21.2 Feature List

- Two monitored sources
  - Monitors the voltage level of pin VDD\_ANA, which supplies power to the analog circuit.
  - Monitors the voltage level of pin VDD\_BAT, which connects the external battery to the chip.
- Two configurable monitoring modes
  - Mode 0: The brown-out detector triggers interrupts when the brown-out counter reaches the predefined threshold and selects the reset mode according to the configuration.
  - Mode 1: The brown-out detector triggers a system reset when the voltage falls below the threshold.
- Configurable voltage-monitoring thresholds and noise tolerance
- Configurable handling modes for under-voltage events

## 21.3 Architectural Overview

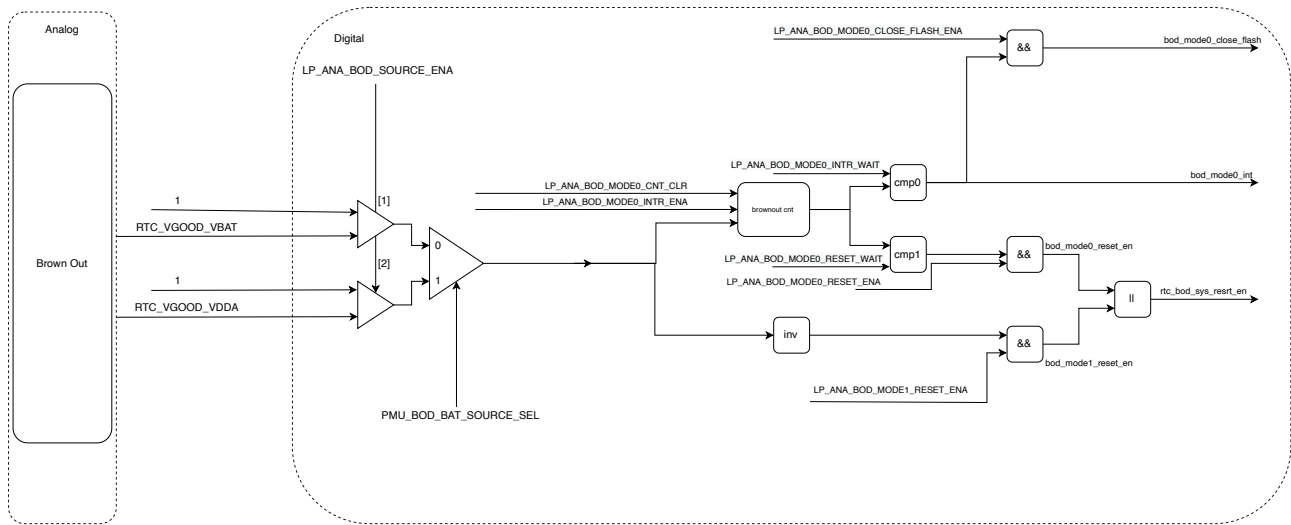


Figure 21.3-1. Brown-out Detector Overview

- Source selection for detection: The brown-out detector can select which power source to monitor by configuring `LP_ANA_BOD_SOURCE_ENA`. `RTC_VGOOD_VBAT` indicates the detection result of `VDD_BAT`, and `RTC_VGOOD_VDDA` indicates the detection result of `VDD_ANA`.
- Brown-out detector (Brown Out): An analog circuit designed to monitor the voltage of power pins and generate brown-out signals. It compares the voltage with the predefined threshold. When the voltage falls below this threshold, the detector outputs brown-out signals.
- Brown-out counter (brownout cnt): A counter used for filtering voltage noise on the detected power pins. When the brown-out signal is received, the counter starts counting based on the clock source `LP_DYN_FAST_CLK`. If the brown-out signal ceases during the counting process, the counter resets to 0. This counter can be cleared by configuring `LP_ANA_BOD_MODE0_CNT_CLR`.
- Interrupt comparator (cmp0): The comparator generates interrupts by comparing the counter value with the threshold. When the counter value exceeds the threshold, the comparator generates the interrupt signal `bod_mode0_int`. If `LP_ANA_BOD_MODE0_CLOSE_FLASH_ENA` is enabled, `bod_mode0_close_flash` will be triggered, causing flash to enter the SUSPEND state.
- Reset comparator (cmp1): The comparator triggers reset signals by comparing the counter value with the threshold. When the counter value exceeds the threshold, the comparator triggers reset signals.

## 21.4 Functional Description

- Monitored sources
  - `VDD_ANA`: Power pin for the analog circuit, supporting both Mode 0 and Mode 1.
  - `VDD_BAT`: Power pin connected to the battery, supporting both Mode 0 and Mode 1. In addition, it supports two configurable voltage thresholds:
    - \* `VBAT_BOD`: Used for brown-out detection of `VDD_BAT`

\* VBAT\_CHARGER: Indicates whether the battery connected to VDD\_BAT needs charging.

These thresholds trigger different interrupts.

- Monitoring modes

There are two monitoring modes based on the way the brown-out detector handles the brown-out signal:

- Mode 0: When Mode 0 is enabled, the brown-out counter starts counting after detecting a brown-out signal. Interrupt and reset signals are generated when the counter reaches the thresholds defined by [LP\\_ANA\\_BOD\\_MODE0\\_RESET\\_WAIT](#) and [LP\\_ANA\\_BOD\\_MODE0\\_INTR\\_WAIT](#), respectively. This helps filter out noise on the monitored pins. Configure [LP\\_ANA\\_BOD\\_MODE0\\_RESET\\_SEL](#) to select the reset options:

- \* 0: Reset the chip.

- \* 1: Reset the system.

- Mode 1: Mode 1 is the default mode, which resets the system immediately upon detecting under-voltage.

- Voltage-monitoring thresholds

The voltage-monitoring threshold is configured in the analog circuit by the analog I2C master. The threshold configuration registers are as follows. BIAS is the slave of the analog I2C master. The address of BIAS is 0x6a. REGXX indicates the register address of BIAS, and [x:x] indicates the bits of this register.

- BIAS\_OR\_DREFL\_VBAT (REG08[7:5]): threshold for releasing the under-voltage state of VDD\_BAT
- BIAS\_OR\_DREFH\_VBAT (REG08[4:2]): under-voltage threshold of VDD\_BAT
- BIAS\_OR\_DREFL\_VDDA (REG09[7:5]): threshold for releasing the under-voltage state of VDD\_ANA
- BIAS\_OR\_DREFH\_VDDA (REG09[4:2]): under-voltage threshold of VDD\_ANA
- BIAS\_OR\_DREFL\_VBAT\_CHARGER (REG10[7:5]): threshold for releasing the under-voltage state of battery connected to VDD\_BAT
- BIAS\_OR\_DREFH\_VBAT\_CHARGER (REG10[4:2]): under-voltage threshold of battery connected to VDD\_BAT

The relationship between the threshold configuration and voltage is:

- 0: 2.52 V
- 1: 2.57 V
- 2: 2.63 V
- 3: 2.68 V
- 4: 2.74 V
- 5: 2.78 V
- 6: 2.83 V
- 7: 2.89 V

- Voltage-monitoring filter

A dedicated glitch filter is used to process the detection results of VDD\_BAT, as shown in the figure below.



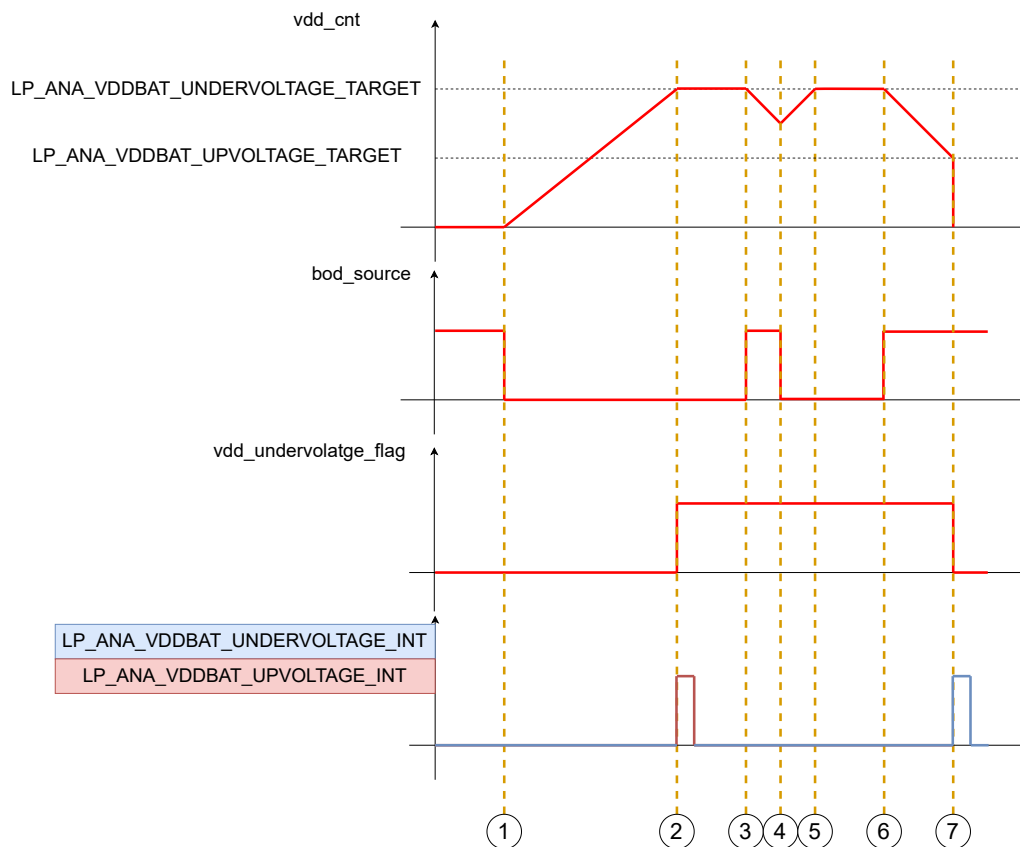


Figure 21.4-1. Structure of Brown-out Detector

- vdd\_cnt: the value of the brown-out counter.
- bod\_source: the monitored source, which is VDD\_BAT in the figure.
- vdd\_undervoltage\_flag: the under-voltage flag.
- Stage 0 ~ 1: When bod\_source is 1, it indicates the voltage is normal, and the brown-out counter (vdd\_cnt) remains 0.
- Stage 1 ~ 2: When bod\_source is 0, it indicates under-voltage happens, and the brown-out counter will start to count. When the counter value reaches the corresponding threshold, vdd\_undervoltage\_flag will be set to 1, and the interrupt is generated.
- Stage 2 ~ 3: When vdd\_undervoltage\_flag is 1, the brown-out counter will stop counting, and stabilize at LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_TARGET.
- Stage 3 ~ 4 ~ 5: When bod\_source changes back to 0 for a short period, the value in the brown-out counter will decrease. However, as the value does not reach to LP\_ANA\_VDDBAT\_UPVOLTAGE\_TARGET, vdd\_undervoltage\_flag will not be toggled.
- Stage 6 ~ 7: After bod\_source remains 0 for a certain period, i.e., the counter value decreases to LP\_ANA\_VDDBAT\_UPVOLTAGE\_TARGET, vdd\_undervoltage\_flag is reset to 0. Then the counter is cleared to 0.

## 21.5 Interrupts

ESP32-P4's brown-out detector can generate the following interrupt and send it to [Interrupt Matrix](#).

- LP\_ANAPERI\_INT

The interrupt is generated by the internal interrupt sources of the brown-out detector.

- LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT: Triggered when the voltage of VDD\_BAT increases to the predefined charging threshold.
- LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT: Triggered when the voltage of VDD\_BAT decreases to the predefined charging threshold.
- LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT: Triggered when the voltage of VDD\_BAT increases to the predefined brown-out threshold.
- LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT: Triggered when the voltage of VDD\_BAT reduces to the predefined brown-out threshold.
- LP\_ANA\_BOD\_MODE0\_INT: Triggered when the value of the brown-out counter reaches the predefined threshold in Mode 0.

Each interrupt source can be configured by a common set of registers that are described in Chapter [Interrupt Configuration Registers](#). The specific registers can be found in Section [21.7 Register Summary](#).

## 21.6 Programming Procedures

- Mode 0
  - Configure [LP\\_ANA\\_BOD\\_MODE0\\_RESET\\_WAIT](#) to set the counter threshold for triggering the reset signal.
  - Configure [LP\\_ANA\\_BOD\\_MODE0\\_INTR\\_WAIT](#) to set the counter threshold for triggering interrupts.
  - Set [LP\\_ANA\\_BOD\\_MODE0\\_RESET\\_SEL](#) to select the reset way in Mode 0.
  - Configure [LP\\_ANA\\_BOD\\_SOURCE\\_ENA](#) to enable the power pin to be detected.
  - Set [LP\\_ANA\\_BOD\\_MODE0\\_RESET\\_ENA](#) to enable the brown-out reset functionality.
  - Set [LP\\_ANA\\_BOD\\_MODE0\\_INTR\\_ENA](#) to enable the noise-filtering counter and interrupts.
- Mode 1
  - Configure [LP\\_ANA\\_BOD\\_SOURCE\\_ENA](#) to enable the power pin to be detected.

## 21.7 Register Summary

The addresses in this section are relative to Brown-out Detector base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">LP_ANA_BOD_MODE0_CNTL_REG</a>     | Control register of Mode 0                               | 0x0000  | R/W    |
| <a href="#">LP_ANA_VDD_SOURCE_CNTL_REG</a>    | Control register of monitoring sources                   | 0x0008  | varies |
| <a href="#">LP_ANA_VDDBAT_BOD_CNTL_REG</a>    | Control register of brown-out detecting for VDD_BAT      | 0x000C  | varies |
| <a href="#">LP_ANA_VDDBAT_CHARGE_CNTL_REG</a> | Pre-charge control register for under-voltage of VDD_BAT | 0x0010  | varies |
| <a href="#">LP_ANA_INT_RAW_REG</a>            | Raw interrupt status                                     | 0x0020  | RO     |
| <a href="#">LP_ANA_INT_ST_REG</a>             | Interrupt state register                                 | 0x0024  | RO     |
| <a href="#">LP_ANA_INT_ENA_REG</a>            | Interrupt enable register                                | 0x0028  | R/W    |
| <a href="#">LP_ANA_INT_CLR_REG</a>            | Interrupt clear register                                 | 0x002C  | WT     |

## 21.8 Registers

The addresses in this section are relative to Brown-out Detector base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 21.1. LP\_ANA\_BOD\_MODE0\_CNTL\_REG (0x0000)**

|                            |    |    |    |    |       |  |  |  |  |  |  |  |  |  |  |                             |    |    |  |  |  |  |  |  |  |  |  |  |  |  |   |                            |   |   |   |   |   |   |   |   |   |       |  |  |  |  |   |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------------------------|----|----|----|----|-------|--|--|--|--|--|--|--|--|--|--|-----------------------------|----|----|--|--|--|--|--|--|--|--|--|--|--|--|---|----------------------------|---|---|---|---|---|---|---|---|---|-------|--|--|--|--|---|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LP_ANA_BOD_MODE0_RESET_ENA |    |    |    |    |       |  |  |  |  |  |  |  |  |  |  | LP_ANA_BOD_MODE0_RESET_WAIT |    |    |  |  |  |  |  |  |  |  |  |  |  |  |   | LP_ANA_BOD_MODE0_INTR_WAIT |   |   |   |   |   |   |   |   |   |       |  |  |  |  |   | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_ANA_BOD_MODE0_CLOSE_FLASH_ENA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LP_ANA_BOD_MODE0_RESET_SEL |    |    |    |    |       |  |  |  |  |  |  |  |  |  |  | LP_ANA_BOD_MODE0_INTR_ENA   |    |    |  |  |  |  |  |  |  |  |  |  |  |  |   | (reserved)                 |   |   |   |   |   |   |   |   |   |       |  |  |  |  |   | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LP_ANA_BOD_MODE0_CNTL_CLR  |    |    |    |    |       |  |  |  |  |  |  |  |  |  |  |                             |    |    |  |  |  |  |  |  |  |  |  |  |  |  |   |                            |   |   |   |   |   |   |   |   |   |       |  |  |  |  |   |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                         | 30 | 29 | 28 | 27 |       |  |  |  |  |  |  |  |  |  |  |                             | 18 | 17 |  |  |  |  |  |  |  |  |  |  |  |  | 8 | 7                          | 6 | 5 |   |   |   |   |   |   |   |       |  |  |  |  | 0 |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                          | 0  | 0  | 0  |    | 0x3ff |  |  |  |  |  |  |  |  |  |  |                             |    | 1  |  |  |  |  |  |  |  |  |  |  |  |  |   | 0                          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |  |  |  |   |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_ANA\_BOD\_MODE0\_CLOSE\_FLASH\_ENA** Configure to close the flash functionality when under-voltage happens in Mode 0.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_BOD\_MODE0\_INTR\_WAIT** Configure the counter threshold that triggers interrupts in Mode 0. (R/W)

**LP\_ANA\_BOD\_MODE0\_RESET\_WAIT** Configure the counter threshold that triggers reset in Mode 0. (R/W)

**LP\_ANA\_BOD\_MODE0\_CNTL\_CLR** Clear counter value in Mode 0. (R/W)

**LP\_ANA\_BOD\_MODE0\_INTR\_ENA** Configure to enable the counter and interrupts in Mode 0.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_BOD\_MODE0\_RESET\_SEL** Configure the reset way when under-voltage happens in Mode 0.

0: Reset the chip

1: Reset the system

(R/W)

**LP\_ANA\_BOD\_MODE0\_RESET\_ENA** Configure to enable reset in Mode 0.

0: Disable

1: Enable

(R/W)

Register 21.2. LP\_ANA\_VDD\_SOURCE\_CNTL\_REG (0x0008)

|            |    |    |    |    |                       |    |    |    |    |            |   |   |   |   |                              |   |   |   |   |            |   |   |   |   |                           |   |   |   |   |            |   |       |  |  |
|------------|----|----|----|----|-----------------------|----|----|----|----|------------|---|---|---|---|------------------------------|---|---|---|---|------------|---|---|---|---|---------------------------|---|---|---|---|------------|---|-------|--|--|
| (reserved) |    |    |    |    | LP_ANA_BOD_SOURCE_ENA |    |    |    |    | (reserved) |   |   |   |   | LP_ANA_VBAT_EVENT_RECORD_CLR |   |   |   |   | (reserved) |   |   |   |   | LP_ANA_VGOOD_EVENT_RECORD |   |   |   |   | (reserved) |   |       |  |  |
| 31         | 27 | 26 | 25 | 24 | 19                    | 18 | 17 | 16 | 11 | 10         | 9 | 8 | 0 |   |                              |   |   |   |   |            |   |   |   |   |                           |   |   |   |   |            |   |       |  |  |
| 0          | 0  | 0  | 0  | 0  | 2                     | 0  | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0                         | 0 | 0 | 0 | 0 | 0          | 0 | Reset |  |  |

**LP\_ANA\_VGOOD\_EVENT\_RECORD** Flags for indicating pins whose voltage is lower than the threshold.

0: Under-voltage does not happen on either VDD\_BAT or VDD\_ANA;

1: Under-voltage happens on VDD\_BAT;

2: Under-voltage happens on VDD\_ANA;

3: Under-voltage happens on both VDD\_BAT and VDD\_ANA.

(RO)

**LP\_ANA\_VBAT\_EVENT\_RECORD\_CLR** Clear the flags.

0: Not clear

1: Clear the brown-out flag of VDD\_BAT

2: Clear the brown-out flag of VDD\_ANA

3: No effect

(WT)

**LP\_ANA\_BOD\_SOURCE\_ENA** Configure to detect monitoring sources.

0: Not detecting any pins;

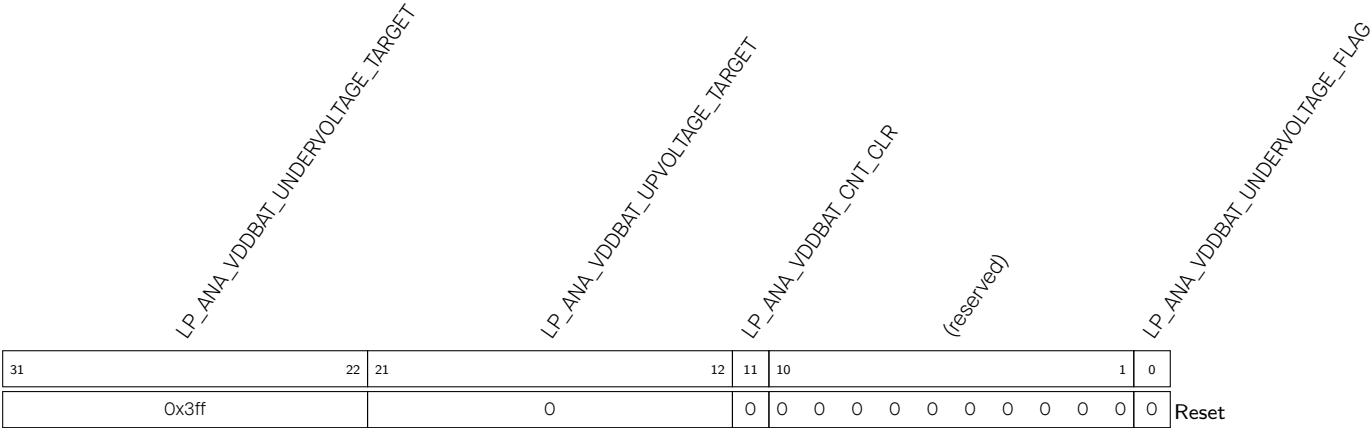
1: Only detect VDD\_BAT;

2: Only detect VDD\_ANA;

3: Detect both VDD\_BAT and VDD\_ANA.

(R/W)

Register 21.3. LP\_ANA\_VDDBAT\_BOD\_CNTL\_REG (0x000C)



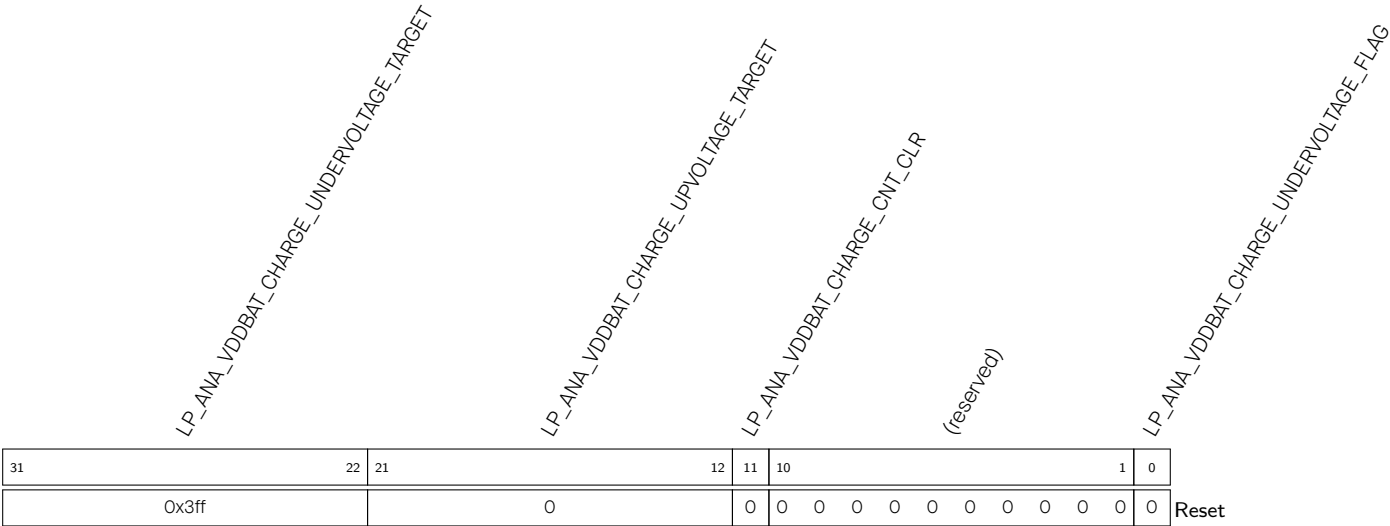
**LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_FLAG** Flag indicating that under-voltage occurs on VDD\_BAT. (RO)

**LP\_ANA\_VDDBAT\_CNT\_CLR** Clear the brown-out counter of VDD\_BAT. (WT)

**LP\_ANA\_VDDBAT\_UPVOLTAGE\_TARGET** Configure the voltage-recovery threshold for the brown-out counter of VDD\_BAT. When the counter decreases to this threshold, [LP\\_ANA\\_VDDBAT\\_UNDERVOLTAGE\\_FLAG](#) is cleared to 0. (R/W)

**LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_TARGET** Configure the brown-out threshold for the brown-out counter of VDD\_BAT. When the counter increases to this threshold, [LP\\_ANA\\_VDDBAT\\_UNDERVOLTAGE\\_FLAG](#) is set to 1. (R/W)

Register 21.4. LP\_ANA\_VDDBAT\_CHARGE\_CNTL\_REG (0x0010)



**LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_FLAG** Flag indicating that VDD\_BAT is charging. (RO)

**LP\_ANA\_VDDBAT\_CHARGE\_CNT\_CLR** Clear the brown-out counter of VDD\_BAT. (WT)

**LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_TARGET** Configure the voltage-recovery threshold for the brown-out counter of VDD\_BAT. When the counter decreases to this threshold, [LP\\_ANA\\_VDDBAT\\_CHARGE\\_UNDERVOLTAGE\\_FLAG](#) is cleared to 0. (R/W)

**LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_TARGET** Configure the brown-out threshold for the brown-out counter of VDD\_BAT. When the counter increases to this threshold, [LP\\_ANA\\_VDDBAT\\_CHARGE\\_UNDERVOLTAGE\\_FLAG](#) is set to 1. (R/W)

Register 21.5. LP\_ANA\_INT\_RAW\_REG (0x0020)

|   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |
|---|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|
| <div>LP_ANA_BOD_MODE0_INT_RAW</div> <div>LP_ANA_VDDBAT_UNDERVOLTAGE_INT_RAW</div> <div>LP_ANA_VDDBAT_UPVOLTAGE_INT_RAW</div> <div>LP_ANA_VDDBAT_CHARGE_UNDERVOLTAGE_INT_RAW</div> <div>LP_ANA_VDDBAT_CHARGE_UPVOLTAGE_INT_RAW</div> <div>(reserved)</div> |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |
| 31  | 30 | 29 | 28 | 27 | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |  |
| 0   | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |

- LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT\_RAW The interrupt is triggered when the voltage of VDD\_BAT increases to the charging threshold. (RO)
- LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT\_RAW The interrupt is triggered when the voltage of VDD\_BAT decreases to the charging threshold. (RO)
- LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT\_RAW The interrupt is triggered when the voltage of VDD\_BAT increases to the brown-out threshold. (RO)
- LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT\_RAW The interrupt is triggered when the voltage of VDD\_BAT decreases to the brown-out threshold. (RO)
- LP\_ANA\_BOD\_MODE0\_INT\_RAW Brown-out interrupt in Mode 0. (RO)



### Register 21.6. LP\_ANA\_INT\_ST\_REG (0x0024)

Diagram illustrating the Reset Vector field (bits 31:0) in the Reset Register:

- Bits 31:27: Reset Vector Address (5 bits)
- Bits 26:0: Reset Vector (27 bits, reserved)

Reset Vectors (bits 31:27):

- LP\_ANA\_BOD\_MODE0\_INT\_ST
- LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT\_ST
- LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT\_ST
- LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT\_ST
- LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT\_ST

**LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT\_ST** The interrupt is triggered and sent to CPU when the voltage of VDD\_BAT increases to the charging threshold. (RO)

**LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT\_ST** The interrupt is triggered and sent to CPU when the voltage of VDD\_BAT decreases to the charging threshold. (RO)

**LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT\_ST** The interrupt is triggered and sent to CPU when the voltage of VDD\_BAT increases to the brown-out threshold. (RO)

**LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT\_ST** The interrupt is triggered and sent to CPU when the voltage of VDD\_BAT decreases to the brown-out threshold. (RO)

**LP\_ANA\_BOD\_MODE0\_INT\_ST** The brown-out interrupt in Mode 0 is triggered and sent to CPU.  
(RO)

## Register 21.7. LP\_ANA\_INT\_ENA\_REG (0x0028)

|  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div> <div>LP_ANA_BOD_MODE0_INT_ENA</div> <div>LP_ANA_VDDBAT_UNDERVOLTAGE_INT_ENA</div> <div>LP_ANA_VDDBAT_UPVOLTAGE_INT_ENA</div> <div>LP_ANA_VDDBAT_CHARGE_UPVOLTAGE_INT_ENA</div> <div>LP_ANA_VDDBAT_CHARGE_UNDERVOLTAGE_INT_ENA</div> <div>(reserved)</div> </div> |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT\_ENA** Configure whether to enable the interrupt which is triggered when the voltage of VDD\_BAT increases to the charging threshold.

0: No

1: Yes

(R/W)

**LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT\_ENA** Configures whether to enable the interrupt which is triggered when the voltage of VDD\_BAT reduces to the charging threshold.

0: Yes

1: No

(R/W)

**LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT\_ENA** Configures whether to enable the interrupt which is triggered when the voltage of VDD\_BAT increases to the brown-out threshold.

0: Yes

1: No

(R/W)

**LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT\_ENA** Configures whether to enable the interrupt which is triggered when the voltage of VDD\_BAT reduces to the brown-out threshold.

0: No

1: Yes

(R/W)

**LP\_ANA\_BOD\_MODE0\_INT\_ENA** Configures whether to enable the brown-out interrupt in Mode 0.

0: No

1: Yes

(R/W)

### Register 21.8. LP\_ANA\_INT\_CLR\_REG (0x002C)

Diagram illustrating the Reset signal (32 bits). The signal is shown as a horizontal bar divided into 32 segments, labeled 31 down to 0. The signal is labeled "Reset" at the right end.

**LP\_ANA\_VDDBAT\_CHARGE\_UPVOLTAGE\_INT\_CLR** Configures whether to clear the interrupt triggered by the VDD\_BAT voltage increasing to the charging threshold. (WT)

**LP\_ANA\_VDDBAT\_CHARGE\_UNDERVOLTAGE\_INT\_CLR** Configures whether to clear the interrupt triggered by the VDD\_BAT voltage reducing to the charging threshold. (WT)

**LP\_ANA\_VDDBAT\_UPVOLTAGE\_INT\_CLR** Configures whether to clear the interrupt triggered by the VDD\_BAT voltage increasing to the brown-out threshold. (WT)

**LP\_ANA\_VDDBAT\_UNDERVOLTAGE\_INT\_CLR** Configures whether to clear the interrupt triggered by the VDD\_BAT voltage reducing to the brown-out threshold. (WT)

LP\_ANA\_BOD\_MODE0\_INT\_ST Configures whether to clear the brown-out interrupt in Mode 0.  
(WT)

## Part V

# Cryptography/Security Component

Dedicated to security features, this part explores cryptographic accelerators like AES and ECC. It also covers digital signatures, random number generation, and encryption/decryption algorithms, showcasing the SoC's capabilities in cryptography and secure data processing.

## Chapter 22

## AES Accelerator (AES)

### 22.1 Introduction

ESP32-P4 integrates an Advanced Encryption Standard (AES) accelerator, which is a hardware device that speeds up computation using AES algorithm significantly, compared to AES algorithms implemented solely in software. The AES accelerator integrated in ESP32-P4 has two working modes, which are [Typical AES](#) and [DMA-AES](#).

### 22.2 Features

The following functionality is supported:

- Typical AES working mode
  - AES-128/AES-256 encryption and decryption
- DMA-AES working mode
  - AES-128/AES-256 encryption and decryption
  - Block cipher mode
    - \* ECB (Electronic Codebook)
    - \* CBC (Cipher Block Chaining)
    - \* OFB (Output Feedback)
    - \* CTR (Counter)
    - \* CFB8 (8-bit Cipher Feedback)
    - \* CFB128 (128-bit Cipher Feedback)
  - GCM (Galois/Counter Mode)
  - Interrupt on completion of computation

### 22.3 Clock and Reset

The AES accelerator is activated by setting the [HP\\_SYS\\_CLKRST\\_CRYPT\\_AES\\_CLK\\_EN](#) bit in the [HP\\_SYS\\_CLKRST\\_PERI\\_CLK\\_CTRL25\\_REG](#) register and clearing the [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_AES](#) bit in the [HP\\_SYS\\_CLKRST\\_HP\\_RST\\_EN2\\_REG](#) register. Besides, due to resource reuse between cryptography accelerator modules, users also need to additionally clear the [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_DS](#) bit and the [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_KM](#) bit in the [HP\\_SYS\\_CLKRST\\_HP\\_RST\\_EN2\\_REG](#) register.

## 22.4 AES Working Modes

The AES accelerator integrated in ESP32-P4 has two working modes, which are [Typical AES](#) and [DMA-AES](#).

- Typical AES Working Mode:
  - Supports encryption and decryption using cryptographic keys of 128 and 256 bits, specified in [NIST FIPS 197](#).

In this working mode, the plaintext and ciphertext is written and read via CPU directly.

- DMA-AES Working Mode:
  - Supports encryption and decryption using cryptographic keys of 128 and 256 bits, specified in [NIST FIPS 197](#);
  - Supports block cipher modes ECB, CBC, OFB, CTR, CFB8, and CFB128 under [NIST SP 800-38A](#).
  - Supports GCM under [NIST SP 800-38D](#).

In this working mode, the plaintext and ciphertext are written and read via DMA. An interrupt will be generated when operation completes.

Users can choose the working mode for AES accelerator by configuring the [AES\\_DMA\\_ENABLE\\_REG](#) register according to Table 22.4-1 below.

**Table 22.4-1. AES Accelerator Working Mode**

| <a href="#">AES_DMA_ENABLE_REG</a> | Working Mode |
|------------------------------------|--------------|
| 0                                  | Typical AES  |
| 1                                  | DMA-AES      |

Users can choose the length of cryptographic keys and encryption/decryption by configuring the [AES\\_MODE\\_REG](#) register according to Table 22.4-2 below.

**Table 22.4-2. Key Length and Encryption/Decryption**

| <a href="#">AES_MODE_REG</a> [2:0] | Key Length and Encryption/Decryption |
|------------------------------------|--------------------------------------|
| 0                                  | AES-128 encryption                   |
| 1                                  | reserved                             |
| 2                                  | AES-256 encryption                   |
| 3                                  | reserved                             |
| 4                                  | AES-128 decryption                   |
| 5                                  | reserved                             |
| 6                                  | AES-256 decryption                   |
| 7                                  | reserved                             |

For a detailed introduction to these two working modes, please refer to Section 22.5 and Section 22.6 below.

**Notice:**

ESP32-P4's [Digital Signature Algorithm \(DSA\)](#) module will call the AES accelerator. Therefore, users cannot access the AES accelerator when [Digital Signature Algorithm \(DSA\)](#) module is working.

## 22.5 Typical AES Working Mode

In the Typical AES working mode, users can check the working status of the AES accelerator by inquiring the [AES\\_STATE\\_REG](#) register and comparing the return value against the Table 22.5-1 below.

Table 22.5-1. Working Status under Typical AES Working Mode

| <a href="#">AES_STATE_REG</a> | Status | Description   |
|-------------------------------|--------|---|
| 0                             | IDLE   | The AES accelerator is idle or completed operation.   |
| 1                             | WORK   | The AES accelerator is in the middle of an operation. |

### 22.5.1 Key, Plaintext, and Ciphertext

The encryption or decryption key is stored in [AES\\_KEY\\_n\\_REG](#), which is a set of eight 32-bit registers.

- For AES-128 encryption or decryption, the 128-bit key is stored in [AES\\_KEY\\_0\\_REG](#) ~ [AES\\_KEY\\_3\\_REG](#).
- For AES-256 encryption or decryption, the 256-bit key is stored in [AES\\_KEY\\_0\\_REG](#) ~ [AES\\_KEY\\_7\\_REG](#).

The plaintext and ciphertext are stored in [AES\\_TEXT\\_IN\\_m\\_REG](#) and [AES\\_TEXT\\_OUT\\_m\\_REG](#), which are two sets of four 32-bit registers.

- For AES-128 or AES-256 encryption, the [AES\\_TEXT\\_IN\\_m\\_REG](#) registers are initialized with plaintext. Then, the AES accelerator stores the ciphertext into [AES\\_TEXT\\_OUT\\_m\\_REG](#) after operation.
- For AES-128 or AES-256 decryption, the [AES\\_TEXT\\_IN\\_m\\_REG](#) registers are initialized with ciphertext. Then, the AES accelerator stores the plaintext into [AES\\_TEXT\\_OUT\\_m\\_REG](#) after operation.

### 22.5.2 Endianness

#### Text Endianness

In Typical AES working mode, the AES accelerator uses cryptographic keys to encrypt and decrypt data in blocks of 128 bits. When filling data into [AES\\_TEXT\\_IN\\_m\\_REG](#) register or reading result from [AES\\_TEXT\\_OUT\\_m\\_REG](#) registers, users should follow the text endianness type specified in Table 22.5-2.

Table 22.5-2. Text Endianness Type for Typical AES

| Plaintext/Ciphertext |                |   |   |   |
|----------------------|----------------|---|---|---|
| State <sup>1</sup>   | c <sup>2</sup> |   |   |   |
|                      | 0              | 1                                       | 2                                       | 3                                       |
| r                    | 0              | <a href="#">AES_TEXT_x_0_REG[7:0]</a>   | <a href="#">AES_TEXT_x_1_REG[7:0]</a>   | <a href="#">AES_TEXT_x_2_REG[7:0]</a>   |
|                      | 1              | <a href="#">AES_TEXT_x_0_REG[15:8]</a>  | <a href="#">AES_TEXT_x_1_REG[15:8]</a>  | <a href="#">AES_TEXT_x_2_REG[15:8]</a>  |
|                      | 2              | <a href="#">AES_TEXT_x_0_REG[23:16]</a> | <a href="#">AES_TEXT_x_1_REG[23:16]</a> | <a href="#">AES_TEXT_x_2_REG[23:16]</a> |

Table 22.5-2. Text Endianness Type for Typical AES

| Plaintext/Ciphertext |   |                         |                         |                         |                         |
|----------------------|---|-------------------------|-------------------------|-------------------------|-------------------------|
|                      | 3 | AES_TEXT_x_0_REG[31:24] | AES_TEXT_x_1_REG[31:24] | AES_TEXT_x_2_REG[31:24] | AES_TEXT_x_3_REG[31:24] |

<sup>1</sup> The definition of “State (including c and r)” is described in Section 3.4 *The State* in [NIST FIPS 197](#).  
<sup>2</sup> Where **x** = IN or OUT.



## Key Endianness

In Typical AES working mode, when filling keys into [AES\\_KEY\\_m\\_REG](#) registers, users should follow the key endianness type specified in Table 22.5-3 and Table 22.5-4.

**Table 22.5-3. Key Endianness Type for AES-128 Encryption and Decryption**

| Bit <sup>1</sup> | w[0]                                 | w[1]                                 | w[2]                                 | w[3] <sup>2</sup>                    |
|------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| [31:24]          | <a href="#">AES_KEY_O_REG[7:0]</a>   | <a href="#">AES_KEY_1_REG[7:0]</a>   | <a href="#">AES_KEY_2_REG[7:0]</a>   | <a href="#">AES_KEY_3_REG[7:0]</a>   |
| [23:16]          | <a href="#">AES_KEY_O_REG[15:8]</a>  | <a href="#">AES_KEY_1_REG[15:8]</a>  | <a href="#">AES_KEY_2_REG[15:8]</a>  | <a href="#">AES_KEY_3_REG[15:8]</a>  |
| [15:8]           | <a href="#">AES_KEY_O_REG[23:16]</a> | <a href="#">AES_KEY_1_REG[23:16]</a> | <a href="#">AES_KEY_2_REG[23:16]</a> | <a href="#">AES_KEY_3_REG[23:16]</a> |
| [7:0]            | <a href="#">AES_KEY_O_REG[31:24]</a> | <a href="#">AES_KEY_1_REG[31:24]</a> | <a href="#">AES_KEY_2_REG[31:24]</a> | <a href="#">AES_KEY_3_REG[31:24]</a> |

<sup>1</sup> Column “Bit” specifies the bytes of each word stored in w[0] ~ w[3].

<sup>2</sup> w[0] ~ w[3] are “the first Nk words of the expanded key” as specified in Section 5.2 *Key Expansion* in [NIST FIPS 197](#).

**Table 22.5-4. Key Endianness Type for AES-256 Encryption and Decryption**

| Bit <sup>1</sup> | w[0]                                 | w[1]                                 | w[2]                                 | w[3]                                 | w[4]                                 | w[5]                                 | w[6]                                 | w[7] <sup>2</sup>                    |
|------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|--------------------------------------|
| [31:24]          | <a href="#">AES_KEY_O_REG[7:0]</a>   | <a href="#">AES_KEY_1_REG[7:0]</a>   | <a href="#">AES_KEY_2_REG[7:0]</a>   | <a href="#">AES_KEY_3_REG[7:0]</a>   | <a href="#">AES_KEY_4_REG[7:0]</a>   | <a href="#">AES_KEY_5_REG[7:0]</a>   | <a href="#">AES_KEY_6_REG[7:0]</a>   | <a href="#">AES_KEY_7_REG[7:0]</a>   |
| [23:16]          | <a href="#">AES_KEY_O_REG[15:8]</a>  | <a href="#">AES_KEY_1_REG[15:8]</a>  | <a href="#">AES_KEY_2_REG[15:8]</a>  | <a href="#">AES_KEY_3_REG[15:8]</a>  | <a href="#">AES_KEY_4_REG[15:8]</a>  | <a href="#">AES_KEY_5_REG[15:8]</a>  | <a href="#">AES_KEY_6_REG[15:8]</a>  | <a href="#">AES_KEY_7_REG[15:8]</a>  |
| [15:8]           | <a href="#">AES_KEY_O_REG[23:16]</a> | <a href="#">AES_KEY_1_REG[23:16]</a> | <a href="#">AES_KEY_2_REG[23:16]</a> | <a href="#">AES_KEY_3_REG[23:16]</a> | <a href="#">AES_KEY_4_REG[23:16]</a> | <a href="#">AES_KEY_5_REG[23:16]</a> | <a href="#">AES_KEY_6_REG[23:16]</a> | <a href="#">AES_KEY_7_REG[23:16]</a> |
| [7:0]            | <a href="#">AES_KEY_O_REG[31:24]</a> | <a href="#">AES_KEY_1_REG[31:24]</a> | <a href="#">AES_KEY_2_REG[31:24]</a> | <a href="#">AES_KEY_3_REG[31:24]</a> | <a href="#">AES_KEY_4_REG[31:24]</a> | <a href="#">AES_KEY_5_REG[31:24]</a> | <a href="#">AES_KEY_6_REG[31:24]</a> | <a href="#">AES_KEY_7_REG[31:24]</a> |

<sup>1</sup> Column “Bit” specifies the bytes of each word stored in w[0] ~ w[7].

<sup>2</sup> w[0] ~ w[7] are “the first Nk words of the expanded key” as specified in Chapter 5.2 *Key Expansion* in [NIST FIPS 197](#).

## 22.5.3 Operation Process

### Single Operation

1. Write 0 to the [AES\\_DMA\\_ENABLE\\_REG](#) register.
2. Initialize registers [AES\\_MODE\\_REG](#), [AES\\_KEY\\_n\\_REG](#), and [AES\\_TEXT\\_IN\\_m\\_REG](#).
3. Start operation by writing 1 to the [AES\\_TRIGGER\\_REG](#) register.
4. Wait till the content of the [AES\\_STATE\\_REG](#) register becomes 0, which indicates the operation is completed.
5. Read results from the [AES\\_TEXT\\_OUT\\_m\\_REG](#) register.

### Consecutive Operations

In consecutive operations, primarily the input [AES\\_TEXT\\_IN\\_m\\_REG](#) and output [AES\\_TEXT\\_OUT\\_m\\_REG](#) registers (*m*: 0-3) are being written and read, while the content of [AES\\_DMA\\_ENABLE\\_REG](#), [AES\\_MODE\\_REG](#), and [AES\\_KEY\\_n\\_REG](#) is kept unchanged. Therefore, the initialization can be simplified during the consecutive operation.

1. Write 0 to the [AES\\_DMA\\_ENABLE\\_REG](#) register before starting the first operation.
2. Initialize registers [AES\\_MODE\\_REG](#) and [AES\\_KEY\\_n\\_REG](#) before starting the first operation.
3. Update the content of [AES\\_TEXT\\_IN\\_m\\_REG](#).
4. Start operation by writing 1 to the [AES\\_TRIGGER\\_REG](#) register.
5. Wait till the content of the [AES\\_STATE\\_REG](#) register becomes 0, which indicates the operation completes.
6. Read results from the [AES\\_TEXT\\_OUT\\_m\\_REG](#) register, and return to Step 3 to continue the next operation.

## 22.6 DMA-AES Working Mode

In the DMA-AES working mode, the AES accelerator supports six block cipher modes: ECB, CBC, OFB, CTR, CFB8, and CFB128. Users can choose the block cipher mode by configuring the [AES\\_BLOCK\\_MODE\\_REG](#) register according to Table 22.6-1 below.

Table 22.6-1. Block Cipher Mode

| <a href="#">AES_BLOCK_MODE_REG</a> [2:0] | Block Cipher Mode                |
|--|----------------------------------|
| 0  | ECB (Electronic Codebook)        |
| 1  | CBC (Cipher Block Chaining)      |
| 2  | OFB (Output Feedback)            |
| 3  | CTR (Counter)                    |
| 4  | CFB8 (8-bit Cipher Feedback)     |
| 5  | CFB128 (128-bit Cipher Feedback) |
| 6  | GCM (Galois/Counter Mode)        |
| 7  | reserved                         |

Users can check the working status of the AES accelerator by inquiring the [AES\\_STATE\\_REG](#) register and comparing the return value against the Table 22.6-2 below.

Table 22.6-2. Working Status under DMA-AES Working mode

| <a href="#">AES_STATE_REG</a> [1:0] | Status | Description   |
|-------------------------------------|--------|---|
| 0                                   | IDLE   | The AES accelerator is idle.                          |
| 1                                   | WORK   | The AES accelerator is in the middle of an operation. |
| 2                                   | DONE   | The AES accelerator completed operations.             |

When working in the DMA-AES working mode, the AES accelerator supports interrupt on the completion of computation. To enable this function, write 1 to the [AES\\_INT\\_ENA\\_REG](#) register. By default, the interrupt function is disabled. Also, note that the interrupt should be cleared by software after use.

### 22.6.1 Key, Plaintext, and Ciphertext

#### Block Operation

During the block operations, the AES accelerator reads source data from DMA, and writes result data to DMA after the computation.

- For encryption, DMA reads plaintext from memory, then passes it to AES as source data. After computation, AES passes ciphertext as result data back to DMA to write into memory.
- For decryption, DMA reads ciphertext from memory, then passes it to AES as source data. After computation, AES passes plaintext as result data back to DMA to write into memory.

During block operations, the lengths of the source data and result data are the same. The total computation time is reduced because the DMA data operation and AES computation can happen concurrently.

The length of source data for AES accelerator under DMA-AES working mode must be 128 bits or the integral multiples of 128 bits. Otherwise, trailing zeros will be added to the original source data, so the length of source data equals to the nearest integral multiples of 128 bits. Please see details in Table 22.6-3 below.

Table 22.6-3. TEXT-PADDING

| Function : TEXT-PADDING( )  |  |
|---|--|
| <b>Input</b>  | : $X$ , bit string.  |
| <b>Output</b>   | : $Y = \text{TEXT-PADDING}(X)$ , whose length is the nearest integral multiples of 128 bits. |
| <b>Steps</b><br><p>Let us assume that <math>X</math> is a data-stream that can be split into <math>n</math> parts as following:</p> $X = X_1    X_2    \cdots    X_{n-1}    X_n$ <p>Here, the lengths of <math>X_1, X_2, \cdots, X_{n-1}</math> all equal to 128 bits, and the length of <math>X_n</math> is <math>t</math> (<math>0 \leq t \leq 127</math>).</p> <p>If <math>t = 0</math>, then</p> $\text{TEXT-PADDING}(X) = X;$ <p>If <math>0 &lt; t \leq 127</math>, define a 128-bit block, <math>X_n^*</math>, and let <math>X_n^* = X_n    0^{128-t}</math>, then</p> $\text{TEXT-PADDING}(X) = X_1    X_2    \cdots    X_{n-1}    X_n^* = X    0^{128-t}$ |  |

## 22.6.2 Endianness

Under the DMA-AES working mode, the transmission of source data and result data for AES accelerator is solely controlled by DMA. Therefore, the AES accelerator cannot control the Endianness of the source data and result data, but does have requirement on how these data should be stored in memory and on the length of the data.

For example, let us assume DMA needs to write the following data into memory at address 0x0280.

- Data represented in hexadecimal:
  - 0102030405060708090A0B0C0D0E0F101112131415161718191A1B1C1D1E1F20
- Data Length:
  - Equals to 2 blocks.

Then, this data will be stored in memory as shown in Table 22.6-4 below.

Table 22.6-4. Text Endianness for DMA-AES

| Address | Byte | Address | Byte | Address | Byte | Address | Byte |
|---------|------|---------|------|---------|------|---------|------|
| 0x0280  | 0x01 | 0x0281  | 0x02 | 0x0282  | 0x03 | 0x0283  | 0x04 |
| 0x0284  | 0x05 | 0x0285  | 0x06 | 0x0286  | 0x07 | 0x0287  | 0x08 |
| 0x0288  | 0x09 | 0x0289  | 0x0A | 0x028A  | 0x0B | 0x028B  | 0x0C |
| 0x028C  | 0x0D | 0x028D  | 0x0E | 0x028E  | 0x0F | 0x028F  | 0x10 |
| 0x0290  | 0x11 | 0x0291  | 0x12 | 0x0292  | 0x13 | 0x0293  | 0x14 |
| 0x0294  | 0x15 | 0x0295  | 0x16 | 0x0296  | 0x17 | 0x0297  | 0x18 |
| 0x0298  | 0x19 | 0x0299  | 0x1A | 0x029A  | 0x1B | 0x029B  | 0x1C |
| 0x029C  | 0x1D | 0x029D  | 0x1E | 0x029E  | 0x1F | 0x029F  | 0x20 |

### 22.6.3 Standard Incrementing Function

AES accelerator provides two Standard Incrementing Functions for the CTR block operation, which are INC<sub>32</sub> and INC<sub>128</sub> Standard Incrementing Functions. By setting the [AES\\_INC\\_SEL\\_REG](#) register to 0 or 1, users can choose the INC<sub>32</sub> or INC<sub>128</sub> functions respectively. For details on the Standard Incrementing Function, please see Chapter B.1 *The Standard Incrementing Function* in [NIST SP 800-38A](#).

### 22.6.4 Block Number

Register [AES\\_BLOCK\\_NUM\\_REG](#) stores the Block Number of plaintext  $P$  or ciphertext  $C$ . The length of this register equals to  $\text{length}(\text{TEXT-PADDING}(P))/128$  or  $\text{length}(\text{TEXT-PADDING}(C))/128$ . The AES accelerator only uses this register when working in the DMA-AES mode.

### 22.6.5 Initialization Vector

[AES\\_IV\\_MEM](#) is a 16-byte memory, which is only available for AES accelerator working in block operations. For CBC/OFB/CFB8/CFB128 operations, the [AES\\_IV\\_MEM](#) memory stores the Initialization Vector (IV). For the CTR operation, the [AES\\_IV\\_MEM](#) memory stores the Initial Counter Block (ICB).

Both IV and ICB are 128-bit strings, which can be divided into Byte0, Byte1, Byte2  $\dots$  Byte15 (from left to right). [AES\\_IV\\_MEM](#) stores data following the Endianness pattern presented in Table 22.6-4, i.e., the most significant (i.e., left-most) byte Byte0 is stored at the lowest address while the least significant (i.e., right-most) byte Byte15 at the highest address.

For more details on IV and ICB, please refer to [NIST SP 800-38A](#).

### 22.6.6 Block Operation Process

1. Select one of DMA channels to connect with AES, configure the DMA linked list, and then start DMA. For details, please refer to Chapter 3 *GDMA Controller (GDMA-AHB, GDMA-AXI)*.
2. Initialize the AES accelerator-related registers:
  - Write 1 to the [AES\\_DMA\\_ENABLE\\_REG](#) register.
  - Configure the [AES\\_INT\\_ENA\\_REG](#) register to enable or disable the interrupt function.
  - Initialize registers [AES\\_MODE\\_REG](#) and [AES\\_KEY\\_n\\_REG](#).
  - Select block cipher mode by configuring the [AES\\_BLOCK\\_MODE\\_REG](#) register. For details, see Table 22.6-1.
  - Initialize the [AES\\_BLOCK\\_NUM\\_REG](#) register. For details, see Section 22.6.4.
  - Initialize the [AES\\_INC\\_SEL\\_REG](#) register (only needed when AES accelerator is working under CTR block operation).
  - Initialize the [AES\\_IV\\_MEM](#) memory (This is always needed except for ECB block operation).
3. Start operation by writing 1 to the [AES\\_TRIGGER\\_REG](#) register.
4. Wait for the completion of computation, which happens when the content of [AES\\_STATE\\_REG](#) becomes 2 or the AES interrupt occurs.

5. Check if DMA completes data transmission from AES to memory. At this time, DMA had already written the result data in memory, which can be accessed directly. For details on DMA, please refer to Chapter 3 [GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).
6. Clear interrupt by writing 1 to the [AES\\_INT\\_CLR\\_REG](#) register, if any AES interrupt occurred during the computation.
7. Release the AES accelerator by writing 1 to the [AES\\_DMA\\_EXIT\\_REG](#) register. After this, the content of the [AES\\_STATE\\_REG](#) register becomes 0. Note that, you can release DMA earlier, but only after Step 4 is completed.

### 22.6.7 GCM Operation Process

1. Configure DMA chain and start DMA. For details on DMA, please refer to Chapter 3 [GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).
2. Initialize the AES accelerator-related registers:
  - Write 1 to the [AES\\_DMA\\_ENABLE\\_REG](#) register.
  - Configure the [AES\\_INT\\_ENA\\_REG](#) register to enable or disable the interrupt function.
  - Initialize registers [AES\\_MODE\\_REG](#) and [AES\\_KEY\\_n\\_REG](#).
  - Write 6 to the [AES\\_BLOCK\\_MODE\\_REG](#) register.
  - Initialize the [AES\\_BLOCK\\_NUM\\_REG](#) register. Details about this register are described in Section [22.6.4 Block Number](#).
  - Initialize the [AES\\_AAD\\_BLOCK\\_NUM\\_REG](#) register. Details about this register are described in Section [22.7.4 AAD Block Number](#).
  - Initialize the [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#) register. Details about this register is described in Section [22.7.5 Number of Effective Bits of Incomplete Blocks](#).
3. Start operation by writing 1 to the [AES\\_TRIGGER\\_REG](#) register.
4. Wait for the completion of computation, which happens when the content of [AES\\_STATE\\_REG](#) becomes 2. For details on the working status of AES Accelerator, please refer to Table [22.6-2 Working Status under DMA-AES Working mode](#). At this step, no interrupt occurs.
5. Obtain the  $H$  value from the [AES\\_H\\_MEM](#) memory.
6. Generate  $J_0$  and write it to the [AES\\_JO\\_MEM](#) memory.
7. Continue operating by writing 1 to the [AES\\_CONTINUE\\_OP\\_REG](#) register.
8. Wait for the completion of computation, which happens when the content of [AES\\_STATE\\_REG](#) becomes 2 or the AES interrupt occurs. For details on the working status of AES Accelerator, please refer to Table [22.6-2 Working Status under DMA-AES Working mode](#).
9. Obtain  $T_0$  by reading [AES\\_TO\\_MEM](#).
10. Check if DMA completes data transmission from AES to memory. At this time, DMA had already written the result data in memory, which can be accessed directly. For details on DMA, please refer to Chapter 3 [GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).

11. Clear interrupt by writing 1 to the [AES\\_INT\\_CLR\\_REG](#) register, if any AES interrupt occurred during the computation.
12. Exit DMA by writing 1 to the [AES\\_DMA\\_EXIT\\_REG](#) register. After this, the content of the [AES\\_STATE\\_REG](#) becomes 0. Note that, you can exit DMA earlier, but only after Step 8 is completed.

## 22.7 GCM Algorithm

ESP32-P4's AES accelerator fully supports GCM Algorithm. In reality, the  $AAD$ ,  $C$  and  $P$  that are longer than  $2^{32}-1$  bits are seldom used. Therefore, we specify that the length of  $AAD$ ,  $C$  and  $P$  should be no longer than  $2^{32}-1$  here. Figure 22.7-1 below demonstrates how GCM encryption is implemented in the AES Accelerator of ESP32-P4.

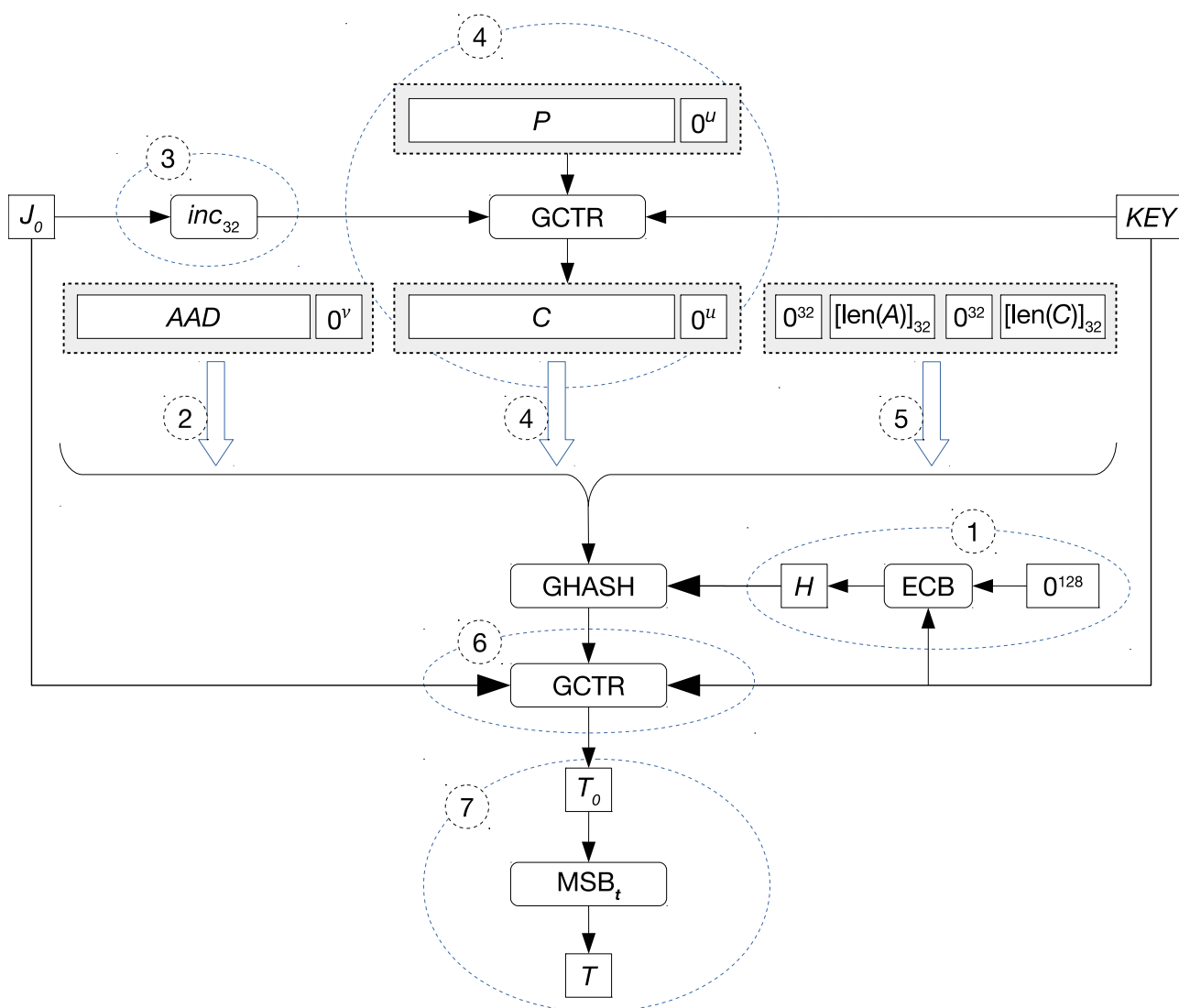


Figure 22.7-1. GCM Encryption Process

GCM encryption is implemented as follows:

1. Hardware executes the ECB Algorithm to obtain the Hash subkey  $H$ , which is needed in the Hash computation.
2. Hardware executes the GHASH Algorithm to perform Hash computation with the [padded](#)  $AAD$ .

3. Hardware gets ready for CTR encryption by obtaining the result of applying Standard Incrementing Function  $\text{INC}_{32}$  to  $J_0$ .
4. Hardware executes the GCTR Algorithm to encrypt the padded plaintext  $P$ , then executes the GHASH Algorithm to perform Hash computation on the padded ciphertext  $C$ .
5. Hardware executes the GHASH Algorithm to perform Hash computation on AAD Blocks, obtaining a 128-bit Hash result.
6. Hardware executes the GCTR Algorithm to encrypt  $J_0$ , obtaining  $T_0$ .
7. Software obtains the result  $T_0$  from hardware, and executes  $\text{MSB}_t$  Algorithm to obtain the final authentication tag  $T$ .

The only difference between GCM decryption and GCM encryption lies in Step 4 in Figure 22.7-1. To be more specific, instead of executing GCTR Algorithm to encrypt the padded plaintext, the AES Accelerator executes the same algorithm to decrypt the padded ciphertext in GCM decryption. For details, please see [NIST SP 800-38D](#).

## 22.7.1 Hash Subkey

During GCM operation, the Hash subkey  $H$  is a 128-bit value computed by hardware, which is demonstrated in Step 1 in Figure 22.7-1. Also you can find more information about Hash subkey at “Step 1. Let  $H = \text{CIPH}_K(0^{128})$ ” in Chapter 7 GCM Specification of [NIST SP 800-38D](#).

The Hash subkey  $H$  is stored in the `AES_H_MEM` memory. Just like other endianness, its most significant (i.e., left-most) byte Byte0 is stored at the lowest address in the memory while least significant (i.e., right-most) byte Byte15 at the highest address. For details, see Table 22.5-2.

## 22.7.2 $J_0$

$J_0$  is a 128-bit value computed by hardware, which is required during Step 3 and Step 6 in Figure 22.7-1. For details on the generation of  $J_0$ , please see Chapter 7 GCM Specification in [NIST SP 800-38D](#).

$J_0$  is stored in the `AES_JO_MEM` memory. Just like other endianness, its most significant (i.e., left-most) byte Byte0 is stored at the lowest address in the memory while least significant (i.e., right-most) byte Byte15 at the highest address. For details, see Table 22.5-2.

## 22.7.3 Authentication Tag

Authentication Tag (Tag for short) is one of the key results of GCM computation, which is demonstrated in Step 7 of Figure 22.7-1. The value of the Tag is determined by its length  $t$  ( $1 \leq t \leq 128$ ):

- When  $t = 128$ , the value of Tag equals to  $T_0$ , a 128-bit string that is stored in the `AES_TO_MEM`. Just like other endianness, its most significant (i.e., left-most) byte Byte0 is stored at the lowest address in the memory while least significant (i.e., right-most) byte Byte15 at the highest address. For details, see Table 22.5-2.
- When  $1 \leq t < 128$ , the value of Tag equals to the  $t$  most significant (i.e., left-most) bits of  $T_0$ . In this case, Tag is represented as  $\text{MSB}_t(T_0)$ , which returns the  $t$  most significant bits of  $T_0$ . For example,  $\text{MSB}_4(111011010) = 1110$  and  $\text{MSB}_5(11010011010) = 11010$ . For details on the  $\text{MSB}_t()$  function, please refer to Chapter 6 Mathematical Components of GCM in [NIST SP 800-38D](#).



## 22.7.4 AAD Block Number

Register [AES\\_AAD\\_BLOCK\\_NUM\\_REG](#) stores the Block Number of Additional Authenticated Data (AAD). The length of this register equals to  $(\text{TEXT-PADDING}(\text{AAD}) \text{ length})/128$ . AES Accelerator only uses this register when working in the DMA-AES mode.

## 22.7.5 Number of Effective Bits of Incomplete Blocks

Register [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#) stores the Remainder Bit Number, which indicates the number of effective bits of incomplete blocks in plaintext/ciphertext. The value stored in this register equals to  $\text{length}(P)/128$  or  $\text{length}(C)/128$ . AES Accelerator only uses this register when working in the DMA-AES mode.

Register [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#) does not affect the results of plaintext or ciphertext, but does impact the value of  $T_0$ , therefore the Tag value too.

The GCM Algorithm can be viewed as the combination of GCTR operation and GHASH operation, among which, the GCTR performs the encryption and decryption, while the GHASH solves the Tag.

Note that the [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#) register is only effective for GCM encryption. To be more specific:

- For GCM encryption, the Hardware firstly computes  $C$ , then passes it in the form of  $\text{TEXT-PADDING}(C)$  as the input of GHASH operation. In this case, hardware determines how many trailing “0” should be added based on the content of [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#).
- For GCM decryption, the padding is completed with the  $\text{TEXT-PADDING}(C)$  function. In this case, the [AES\\_REMAINDER\\_BIT\\_NUM\\_REG](#) register is not effective.

## 22.8 Interrupts

ESP32-P4's AES can generate the following interrupt signal(s) that will be sent to the [Interrupt Matrix](#).

- AES\_INTR

There is one internal interrupt source from AES that can generate the above interrupt signal(s). The interrupt source from AES are listed with its trigger condition and the resulted interrupt signal(s) in Table [22.8-1](#).

Table 22.8-1. AES's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition                  | Interrupt Signal |
|---------------------------|------------------------------------|------------------|
| AES_DMA_DONE_INT          | Completion of an AES DMA operation | AES_INTR         |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

## 22.9 Memory Summary

The addresses in this section are relative to the AES accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                       | Description | Size (byte) | Starting Address | Ending Address | Access |
|----------------------------|-------------|-------------|------------------|----------------|--------|
| <a href="#">AES_IV_MEM</a> | Memory IV   | 16 bytes    | 0x0050           | 0x005F         | R/W    |
| <a href="#">AES_H_MEM</a>  | Memory H    | 16 bytes    | 0x0060           | 0x006F         | RO     |
| <a href="#">AES_JO_MEM</a> | Memory JO   | 16 bytes    | 0x0070           | 0x007F         | R/W    |
| <a href="#">AES_TO_MEM</a> | Memory TO   | 16 bytes    | 0x0080           | 0x008F         | RO     |

## 22.10 Register Summary

The addresses in this section are relative to the AES accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

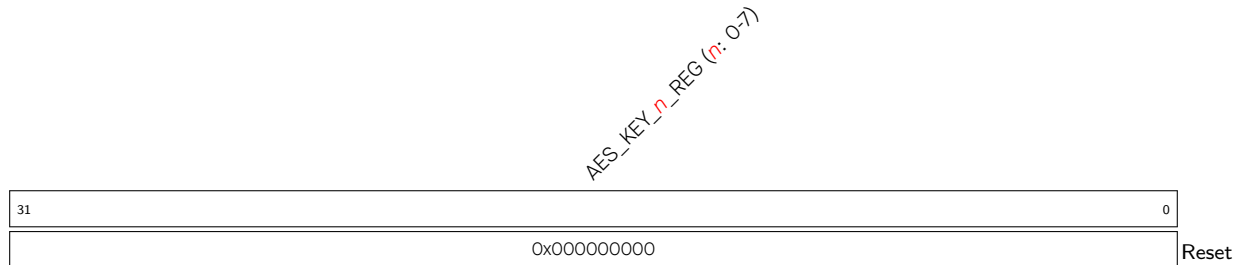
| Name                                      | Description                                     | Address | Access |
|---|---|---------|--------|
| <b>Key Registers</b>                      |   |         |        |
| <a href="#">AES_KEY_0_REG</a>             | AES key data register 0                         | 0x0000  | R/W    |
| <a href="#">AES_KEY_1_REG</a>             | AES key data register 1                         | 0x0004  | R/W    |
| <a href="#">AES_KEY_2_REG</a>             | AES key data register 2                         | 0x0008  | R/W    |
| <a href="#">AES_KEY_3_REG</a>             | AES key data register 3                         | 0x000C  | R/W    |
| <a href="#">AES_KEY_4_REG</a>             | AES key data register 4                         | 0x0010  | R/W    |
| <a href="#">AES_KEY_5_REG</a>             | AES key data register 5                         | 0x0014  | R/W    |
| <a href="#">AES_KEY_6_REG</a>             | AES key data register 6                         | 0x0018  | R/W    |
| <a href="#">AES_KEY_7_REG</a>             | AES key data register 7                         | 0x001C  | R/W    |
| <b>TEXT_IN Registers</b>                  |   |         |        |
| <a href="#">AES_TEXT_IN_0_REG</a>         | Source text data register 0                     | 0x0020  | R/W    |
| <a href="#">AES_TEXT_IN_1_REG</a>         | Source text data register 1                     | 0x0024  | R/W    |
| <a href="#">AES_TEXT_IN_2_REG</a>         | Source text data register 2                     | 0x0028  | R/W    |
| <a href="#">AES_TEXT_IN_3_REG</a>         | Source text data register 3                     | 0x002C  | R/W    |
| <b>TEXT_OUT Registers</b>                 |   |         |        |
| <a href="#">AES_TEXT_OUT_0_REG</a>        | Result text data register 0                     | 0x0030  | RO     |
| <a href="#">AES_TEXT_OUT_1_REG</a>        | Result text data register 1                     | 0x0034  | RO     |
| <a href="#">AES_TEXT_OUT_2_REG</a>        | Result text data register 2                     | 0x0038  | RO     |
| <a href="#">AES_TEXT_OUT_3_REG</a>        | Result text data register 3                     | 0x003C  | RO     |
| <b>Control or Configuration Registers</b> |   |         |        |
| <a href="#">AES_MODE_REG</a>              | Defines key length and encryption/decryption    | 0x0040  | R/W    |
| <a href="#">AES_DMA_ENABLE_REG</a>        | Selects the working mode of the AES accelerator | 0x0090  | R/W    |
| <a href="#">AES_BLOCK_MODE_REG</a>        | Defines the block cipher mode                   | 0x0094  | R/W    |
| <a href="#">AES_BLOCK_NUM_REG</a>         | Block number configuration register             | 0x0098  | R/W    |
| <a href="#">AES_INC_SEL_REG</a>           | Standard incrementing function register         | 0x009C  | R/W    |
| <a href="#">AES_AAD_BLOCK_NUM_REG</a>     | AAD block number configuration register         | 0x00A0  | R/W    |
| <a href="#">AES_REMAINDER_BIT_NUM_REG</a> | Remainder bit number of plaintext/ciphertext    | 0x00A4  | R/W    |
| <a href="#">AES_TRIGGER_REG</a>           | Operation start controlling register            | 0x0048  | WT     |
| <a href="#">AES_CONTINUE_OP_REG</a>       | Operation continue controlling register         | 0x00A8  | WO     |
| <a href="#">AES_DMA_EXIT_REG</a>          | Operation exit controlling register             | 0x00B8  | WO     |
| <b>Status Register</b>                    |   |         |        |
| <a href="#">AES_STATE_REG</a>             | Operation status register                       | 0x004C  | RO     |
| <b>Interrupt Registers</b>                |   |         |        |
| <a href="#">AES_INT_CLR_REG</a>           | DMA-AES interrupt clear register                | 0x00AC  | WT     |
| <a href="#">AES_INT_ENA_REG</a>           | DMA-AES interrupt enable register               | 0x00B0  | R/W    |

## 22.11 Registers

The addresses in this section are relative to the AES accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

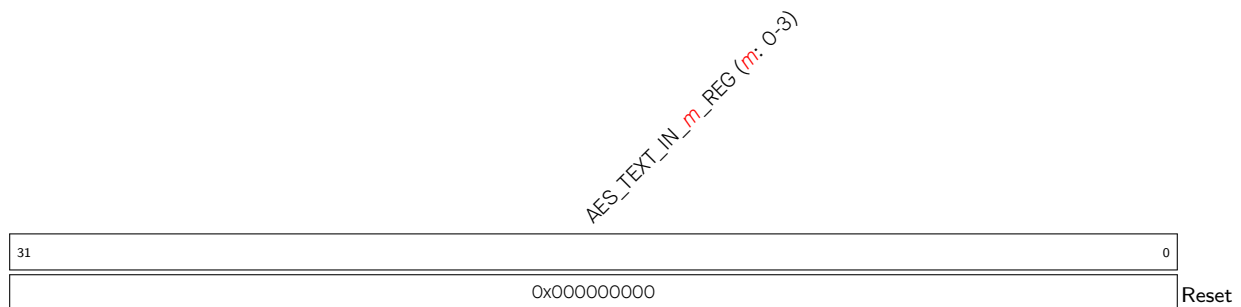
For how to program reserved fields, please refer to Section IX.

**Register 22.1. AES\_KEY\_ *n*\_REG (*n*: 0-7) (0x0000+4\**n*)**



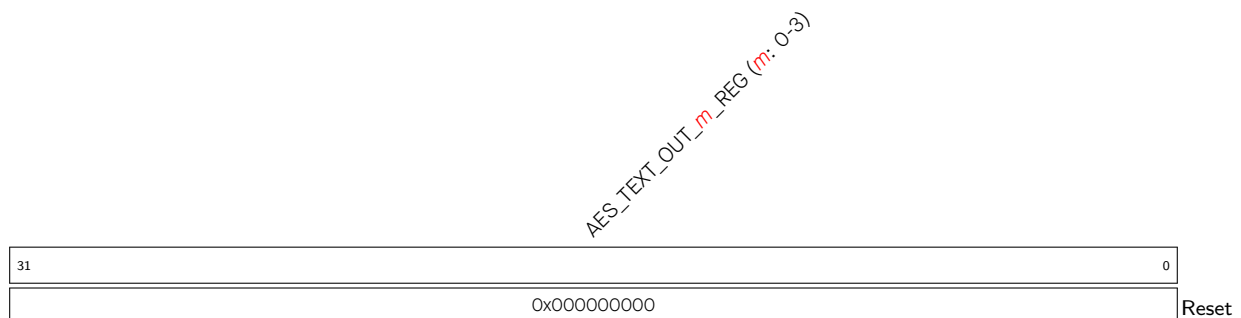
**AES\_KEY\_ *n*\_REG (*n*: 0-7)** Represents AES key data. (R/W)

**Register 22.2. AES\_TEXT\_IN\_ *m*\_REG (*m*: 0-3) (0x0020+4\**m*)**



**AES\_TEXT\_IN\_ *m*\_REG (*m*: 0-3)** Represents the source text data when the AES accelerator operates in the Typical AES working mode. (R/W)

**Register 22.3. AES\_TEXT\_OUT\_ *m*\_REG (*m*: 0-3) (0x0030+4\**m*)**



**AES\_TEXT\_OUT\_ *m*\_REG (*m*: 0-3)** Represents the result text data when the AES accelerator operates in the Typical AES working mode. (RO)

**Register 22.4. AES\_MODE\_REG (0x0040)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |          |       |   |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------|-------|---|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_MODE |       |   |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 3        | 2     | 0 |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0        | Reset |   |

**AES\_MODE** Configures the key length and encryption/decryption of the AES accelerator.

- 0: AES-128 encryption
  - 1: Reserved
  - 2: AES-256 encryption
  - 3: Reserved
  - 4: AES-128 decryption
  - 5: Reserved
  - 6: AES-256 decryption
  - 7: Reserved
- (R/W)

**Register 22.5. AES\_DMA\_ENABLE\_REG (0x0090)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |                |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | AES_DMA_ENABLE |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | 0              |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | 0              | Reset |

**AES\_DMA\_ENABLE** Configures the working mode of the AES accelerator.

- 0: Typical AES
  - 1: DMA-AES
- (R/W)

**Register 22.6. AES\_BLOCK\_MODE\_REG (0x0094)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |       |   |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|-------|---|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_BLOCK_MODE |       |   |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 3              | 2     | 0 |  |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              | Reset |   |  |

**AES\_BLOCK\_MODE** Configures the block cipher mode of the AES accelerator operating under the DMA-AES working mode.

- 0: ECB (Electronic Code Block)
- 1: CBC (Cipher Block Chaining)
- 2: OFB (Output FeedBack)
- 3: CTR (Counter)
- 4: CFB8 (8-bit Cipher FeedBack)
- 5: CFB128 (128-bit Cipher FeedBack)
- 6: GCM (Galois/Counter Mode)
- 7: Reserved

(R/W)

**Register 22.7. AES\_BLOCK\_NUM\_REG (0x0098)**

|               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| AES_BLOCK_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x00000000    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**AES\_BLOCK\_NUM** Represents the Block Number of plaintext or ciphertext when the AES accelerator operates under the DMA-AES working mode. For details, see Section 22.6.4. (R/W)

**Register 22.8. AES\_INC\_SEL\_REG (0x009C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |       |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|-------|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_INC_SEL |       |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1           | 0     |  |  |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0           | Reset |  |  |

**AES\_INC\_SEL** Configures the Standard Incrementing Function for CTR block operation.

- 0: INC<sub>32</sub>
  - 1: INC<sub>128</sub>
- (R/W)

Register 22.9. AES\_AAD\_BLOCK\_NUM\_REG (0x00A0)

|            |   |
|------------|---|
| 31         | 0 |
| 0x00000000 |   |
| Reset      |   |

**AES\_AAD\_BLOCK\_NUM** Stores the ADD block number for the GCM operation. For details, see Section 22.7.4. (R/W)

Register 22.10. AES\_REMAINDER\_BIT\_NUM\_REG (0x00A4)

|            |   |   |   |  |  |  |                       |       |
|------------|---|---|---|--|--|--|-----------------------|-------|
| (reserved) |   |   |   |  |  |  | AES_REMAINDER_BIT_NUM |       |
| 31         | 7 | 6 | 0 |  |  |  |                       |       |
| 0x00000000 |   |   |   |  |  |  | 0                     | Reset |

**AES\_REMAINDER\_BIT\_NUM** Stores the Remainder Bit Number for the GCM operation. For details, see Section 22.7.5. (R/W)

Register 22.11. AES\_TRIGGER\_REG (0x0048)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |   |             |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |   | AES_TRIGGER |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | 0           |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |   | x           | Reset |

**AES\_TRIGGER** Configures whether to start AES operation.

- 0: No effect
- 1: Start

(WT)

## Register 22.12. AES\_STATE\_REG (0x004C)

|            |   |           |       |
|------------|---|-----------|-------|
| (reserved) |   | AES_STATE |       |
| 31         | 2 | 1         | 0     |
| 0x00000000 |   | 0x0       | Reset |

**AES\_STATE** Represents the working status of the AES accelerator.

In Typical AES working mode:

- 0: IDLE
- 1: WORK
- 2: No effect
- 3: No effect

In DMA-AES working mode:

- 0: IDLE
- 1: WORK
- 2: DONE
- 3: No effect

(RO)

## Register 22.13. AES\_CONTINUE\_OP\_REG (0x00A8)

|            |   |              |       |
|------------|---|--------------|-------|
| (reserved) |   | AES_CONTINUE |       |
| 31         | 1 | 0            |       |
| 0x00000000 |   | x            | Reset |

**AES\_CONTINUE\_OP** Configures whether to continue AES operation.

- 0: No effect
  - 1: Continue
- (WO)



**Register 22.14. AES\_DMA\_EXIT\_REG (0x00B8)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_DMA_EXIT |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1            | 0     |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | x            | Reset |

**AES\_DMA\_EXIT** Configures whether to exit AES operation.

0: No effect

1: Exit

Only valid for DMA-AES operation. (WO)

**Register 22.15. AES\_INT\_CLR\_REG (0x00AC)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_INT_CLR |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1           | 0     |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | x           | Reset |

**AES\_INT\_CLR** Configures whether to clear AES interrupt.

0: No effect

1: Clear

(WT)

**Register 22.16. AES\_INT\_ENA\_REG (0x00B0)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | AES_INT_ENA |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1           | 0     |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0           | Reset |

**AES\_INT\_ENA** Configures whether to enable AES interrupt.

0: Disable

1: Enable

(R/W)

## Chapter 23

### ECC Accelerator (ECC)

#### 23.1 Introduction

Elliptic Curve Cryptography (ECC) is an approach to public-key cryptography based on the algebraic structure of elliptic curves. ECC uses smaller keys compared to RSA cryptography while providing equivalent security.

ESP32-P4's ECC accelerator can complete various calculations based on different elliptic curves, thus accelerating the ECC algorithm and ECC-derived algorithms (such as ECDSA).

#### 23.2 Features

ESP32-P4's ECC accelerator has the following features:

- 2 different elliptic curves, namely P-192 and P-256 defined in [FIPS 186-3](#)
- 11 working modes
- Interrupt upon completion of calculation

#### 23.3 ECC Basics

To better illustrate the functionality of the ECC accelerator, the basic knowledge and terminology used in this chapter are introduced in this section.

##### 23.3.1 Elliptic Curve and Points on the Curves

The ECC algorithm is based on elliptic curves over prime fields, which can be represented as:

$$y^2 = x^3 + ax + b \bmod p$$

where,

- $p$  is a prime number,
- $a$  and  $b$  are two non-negative integers smaller than  $p$ ,
- and  $(x, y)$  is a point on the curve satisfying the representation.

##### 23.3.2 Affine Coordinates and Jacobian Coordinates

An elliptic curve can be represented as below:

- In affine coordinates:

$$y^2 = x^3 + ax + b \bmod p$$

- In Jacobian coordinates:

$$Y^2 = X^3 + aXZ^4 + bZ^6 \bmod p$$

To convert affine coordinates  $(x, y)$  to/from Jacobian coordinates  $(X, Y, Z)$ :

- From Jacobian to Affine coordinates:

$$x = X/Z^2 \bmod p$$

$$y = Y/Z^3 \bmod p$$

- From Affine to Jacobian coordinates:

$$X = x$$

$$Y = y$$

$$Z = 1$$

### 23.3.3 Memory Blocks

ECC's memory blocks store the input and output data of the ECC operation.

Table 23.3-1. ECC Accelerator Memory Blocks

| Memory Block    | Size (byte) | Starting Address <sup>*</sup> | Ending Address <sup>*</sup> | Access |
|-----------------|-------------|-------------------------------|-----------------------------|--------|
| ECC_MULT_Mem_k  | 32          | 0x100                         | 0x11F                       | R/W    |
| ECC_MULT_Mem_Px | 32          | 0x120                         | 0x13F                       | R/W    |
| ECC_MULT_Mem_Py | 32          | 0x140                         | 0x15F                       | R/W    |
| ECC_MULT_Mem_Qx | 32          | 0x160                         | 0x17F                       | R/W    |
| ECC_MULT_Mem_Qy | 32          | 0x180                         | 0x19F                       | R/W    |
| ECC_MULT_Mem_Qz | 32          | 0x1A0                         | 0x1BF                       | R/W    |

<sup>\*</sup> Address offset related to the ECC accelerator base address is provided in Table 6.3-2 in Chapter 6 *System and Memory*.

### 23.3.4 Data and Data Block

ESP32-P4's ECC operates on 256-bit data. The data ( $D[255 : 0]$ ) can be divided into eight 32-bit data blocks  $D[n][31 : 0]$  ( $n = 0, 1, \dots, 7$ ). Data blocks with smaller indexes correspond to lower binary bits. To be specific:

$$D[255 : 0] = D[7][31 : 0], D[6][31 : 0], D[5][31 : 0], D[4][31 : 0], D[3][31 : 0], D[2][31 : 0], D[1][31 : 0], D[0][31 : 0]$$

### 23.3.5 Writing Data

Write data means writing data to an ECC memory block and using this data as the input to the ECC algorithm. To be specific, write data to an ECC memory block means writing  $D[n][31 : 0]$  ( $n = 0, 1, \dots, 7$ ) to the "starting address of this ECC memory block +  $4 \times n$ " successively:

- write  $D[0]$  to "starting address"

- write  $D[1]$  to “starting address + 4”
- ...
- write  $D[7]$  to “starting address + 28”

**Note:**

When the key size of 192 bits is used, append 0 before 192 bits of data to ensure 256-bit data is written.

### 23.3.6 Reading Data

Read data means reading data from the starting address of an ECC memory block and using this data as the output from the ECC algorithm. To be specific, read data from an ECC memory block means reading  $D[n][31:0](n = 0, 1, \dots, 7)$  from the “starting address of this ECC memory block +  $4 \times n$ ” successively:

- read  $D[0]$  from “starting address”
- read  $D[1]$  from “starting address + 4”
- ...
- read  $D[7]$  from “starting address + 28”

**Note:**

When the key size of 192 bits is used, only read the low 192 bits (6 blocks) of data.

### 23.3.7 Standard Calculation and Jacobian Calculation

ESP32-P4's ECC performs Affine Point Calculation (including Affine Point Verification, Affine Point Add, and Affine Point Multiplication) using the affine coordinates and Jacobian Calculation (including Jacobian Point Verification, Jacobian Point Add, and Jacobian Point Multiplication) using the Jacobian coordinates.

## 23.4 Function Description

### 23.4.1 Key Size

ESP32-P4's ECC supports acceleration based on two key sizes, each corresponding to an elliptic curve. By configuring the `ECC_MULT_KEY_LENGTH` field, users can select the desired key size. For details, see Table 23.4-1 below.

Table 23.4-1. ECC Accelerator Key Size Selection

| <code>ECC_MULT_KEY_LENGTH</code> | Elliptic Curves <sup>*</sup> |
|----------------------------------|------------------------------|
| 0                                | FIPS P-192                   |
| 1                                | FIPS P-256                   |

<sup>\*</sup> See definition of FIPS P-192 and P-256 in [FIPS 186-3](#).

## 23.4.2 Working Modes

ESP32-P4's ECC accelerator supports 11 working modes based on two elliptic curves described in the above section. By configuring the [ECC\\_MULT\\_WORK\\_MODE](#) field, users can select the desired working mode. For details, see Table 23.4-2.

Table 23.4-2. Working Modes of ECC Accelerator

| <a href="#">ECC_MULT_WORK_MODE</a> | Working Modes                             |
|------------------------------------|---|
| 0                                  | Affine Point Multi                        |
| 1                                  | <b>Reserved</b>                           |
| 2                                  | Affine Point Verif                        |
| 3                                  | Affine Point Verif + Multi                |
| 4                                  | Jacobian Point Multi                      |
| 5                                  | Point Add                                 |
| 6                                  | Jacobian Point Verif                      |
| 7                                  | Affine Point Verif + Jacobian Point Multi |
| 8                                  | Mod Add                                   |
| 9                                  | Mod Sub                                   |
| 10                                 | Mod Multi                                 |
| 11                                 | Mod Div                                   |

**Note:**

Note that the calculation of Jacobian Point Multi mode is about 10% faster than that of the Affine Point Multi mode.

Detailed descriptions about different working modes are provided in the following sections.

### 23.4.2.1 Affine Point Multiplication (Affine Point Multi)

Affine Point Multiplication can be represented as:

$$Q = (Q_x, Q_y) = (J_x, J_y, J_z) = k \cdot (P_x, P_y)$$

where,

- $(Q_x, Q_y)$  is the affine expression of point Q.
- $(J_x, J_y, J_z)$  is the Jacobian expression of point Q.
- Input:  $P_x$ ,  $P_y$ , and  $k$  are stored in [ECC\\_MULT\\_Mem\\_Px](#), [ECC\\_MULT\\_Mem\\_Py](#), and [ECC\\_MULT\\_Mem\\_k](#) respectively.
- Output:  $Q_x$  and  $Q_y$  are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#) respectively.

### 23.4.2.2 Affine Point Verification (Affine Point Verif)

Affine Point Verification can be used to verify if a point  $(P_x, P_y)$  is on a selected elliptic curve.

- Input:  $P_x$  and  $P_y$  are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#) respectively.
- Output: The verification result is stored in the [ECC\\_MULT\\_VERIFICATION\\_RESULT](#) bit.

### 23.4.2.3 Affine Point Verification + Affine Point Multiplication (Affine Point Verif + Multi)

In this mode, ECC first verifies if point  $(P_x, P_y)$  is on the selected elliptic curve. If so, the following multiplication is performed:

$$Q = (Q_x, Q_y) = (J_x, J_y, J_z) = k \cdot (P_x, P_y)$$

where,

- $(Q_x, Q_y)$  is the affine expression of point Q.
- $(J_x, J_y, J_z)$  is the Jacobian expression of point Q.
- Input:  $P_x$ ,  $P_y$ , and  $k$  are stored in [ECC\\_MULT\\_Mem\\_Px](#), [ECC\\_MULT\\_Mem\\_Py](#), and [ECC\\_MULT\\_Mem\\_k](#) respectively.
- Output:
  - The verification result is stored in the [ECC\\_MULT\\_VERIFICATION\\_RESULT](#) bit.
  - $Q_x$  and  $Q_y$  are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#) respectively.
  - $J_x$ ,  $J_y$ , and  $J_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#).

### 23.4.2.4 Jacobian Point Multiplication (Jacobian Point Multi)

Jacobian Point Multiplication can be represented as:

$$Q = (Q_x, Q_y, Q_z) = k \cdot (P_x, P_y, 1)$$

where,

- $(Q_x, Q_y, Q_z)$  is the Jacobian expression of point Q.
- 1 in the point's Jacobian coordinates is automatically completed by hardware.
- Input:  $P_x$ ,  $P_y$ , and  $k$  are stored in [ECC\\_MULT\\_Mem\\_Px](#), [ECC\\_MULT\\_Mem\\_Py](#), and [ECC\\_MULT\\_Mem\\_k](#) respectively.
- Output:  $Q_x$ ,  $Q_y$ , and  $Q_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#) respectively.

### 23.4.2.5 Point Addition (Point Add)

Point Addition can be represented as:

$$R = (R_x, R_y) = (J_x, J_y, J_z) = (P_x, P_y, 1) + (Q_x, Q_y, Q_z)$$

where,

- $(R_x, R_y)$  is the affine expression of point R.
- $(J_x, J_y, J_z)$  is the Jacobian expression of point R.
- 1 in the point's Jacobian coordinates is automatically completed by hardware.
- Input:
  - $P_x$  and  $P_y$  are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - $Q_x$ ,  $Q_y$ , and  $Q_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#).

- Output:
  - $R_x$  and  $R_y$  are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - $J_x$ ,  $J_y$  and  $J_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#).

#### 23.4.2.6 Jacobian Point Verification (Jacobian Point Verif)

Jacobian Point Verification can be used to verify if point  $(Q_x, Q_y, Q_z)$  is on a selected elliptic curve.

- $(Q_x, Q_y, Q_z)$  is the Jacobian expression of point Q.
- Input:  $Q_x$ ,  $Q_y$ , and  $Q_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#) respectively.
- Output: The verification result is stored in the [ECC\\_MULT\\_VERIFICATION\\_RESULT](#) bit.

#### 23.4.2.7 Affine Point Verification + Jacobian Point Multiplication (Affine Point Verif + Jacobian Point Multi)

In this mode, ECC first verifies if point  $(P_x, P_y)$  is on the selected elliptic curve. If so, the following multiplication is performed:

$$Q = (Q_x, Q_y, Q_z) = k \cdot (P_x, P_y, 1)$$

where,

- $(Q_x, Q_y, Q_z)$  is the Jacobian expression of point Q.
- 1 in the point's Jacobian coordinates is automatically completed by hardware.
- Input:  $P_x$ ,  $P_y$ , and  $k$  are stored in [ECC\\_MULT\\_Mem\\_Px](#), [ECC\\_MULT\\_Mem\\_Py](#), and [ECC\\_MULT\\_Mem\\_k](#).
- Output:
  - The verification result is stored in the [ECC\\_MULT\\_VERIFICATION\\_RESULT](#) bit.
  - $Q_x$ ,  $Q_y$ , and  $Q_z$  are stored in [ECC\\_MULT\\_Mem\\_Qx](#), [ECC\\_MULT\\_Mem\\_Qy](#), and [ECC\\_MULT\\_Mem\\_Qz](#).

#### 23.4.2.8 Mod Addition (Mod Add)

Mod Addition can be represented as:

$$R = A + B \bmod N$$

where,

- Input:
  - A and B are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - The value of N is related to the register fields below:
    - \* [ECC\\_MULT\\_KEY\\_LENGTH](#) to select the related curve.
    - \* [ECC\\_MULT\\_MOD\\_BASE](#) to choose using mod base or order of the base point.
- Output: R is stored in [ECC\\_MULT\\_Mem\\_Px](#).

### 23.4.2.9 Mod Subtraction (Mod Sub)

Mod Subtraction can be represented as:

$$R = A - B \bmod N$$

where,

- Input:
  - A and B are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - The value of N is related to the register fields below:
    - \* [ECC\\_MULT\\_KEY\\_LENGTH](#) to select the related curve.
    - \* [ECC\\_MULT\\_MOD\\_BASE](#) to choose using mod base or order of the base point.
- Output: R is stored in [ECC\\_MULT\\_Mem\\_Px](#).

### 23.4.2.10 Mod Multiplication (Mod Multi)

Mod Multiplication can be represented as:

$$R = A \cdot B \bmod N$$

where,

- Input:
  - A and B are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - The value of N is related to the register fields below:
    - \* [ECC\\_MULT\\_KEY\\_LENGTH](#) to select the related curve.
    - \* [ECC\\_MULT\\_MOD\\_BASE](#) to choose using mod base or order of the base point.
- Output: R is stored in [ECC\\_MULT\\_Mem\\_Py](#).

### 23.4.2.11 Mod Division (Mod Div)

Mod Division can be represented as:

$$R = A \cdot B^{-1} \bmod N$$

where,

- Input:
  - A and B are stored in [ECC\\_MULT\\_Mem\\_Px](#) and [ECC\\_MULT\\_Mem\\_Py](#).
  - The value of N is related to the register fields below:
    - \* [ECC\\_MULT\\_KEY\\_LENGTH](#) to select the related curve.
    - \* [ECC\\_MULT\\_MOD\\_BASE](#) to choose using mod base or order of the base point.
- Output: R is stored in [ECC\\_MULT\\_Mem\\_Py](#).



## 23.5 Clock and Reset

ESP32-P4's ECC only has one clock module (CRYPTO\_ECC\_CLK) and one reset module (CRYPTO\_ECC\_RST).

ECC's clock and reset is handled by the the Power/Clock/Reset (PCR) module (see Chapter 9 [Reset and Clock](#) for more information). Users should enable the ECC clock by setting [HP\\_SYS\\_CLKRST\\_CRYPT0\\_ECC\\_CLK\\_EN](#) and release the ECC reset by clearing [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_ECC](#) before starting the ECC accelerator. Besides, due to resource reuse between cryptography accelerator modules, users also need to additionally clear the [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_ECDSA](#) bit.

## 23.6 Interrupts

ESP32-P4's ECC accelerator can generate the ECC\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#).

ECC\_INTR has only one interrupt source to generate the ECC\_INTR interrupt signal, i.e., ECC\_MULT\_CALC\_DONE\_INT, which is triggered on the completion of an ECC calculation.

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The ECC\_MULT\_CALC\_DONE\_INT interrupt source is configured by the following registers (refer to Section [23.8 Register Summary](#) for more information):

- [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_RAW](#): Stores the raw interrupt status of ECC\_MULT\_CALC\_DONE\_INT.
- [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_ST](#): Indicates the status of the ECC\_MULT\_CALC\_DONE\_INT interrupt. This bit is generated by enabling or disabling the [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_RAW](#) bit via [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_ENA](#).
- [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_ENA](#): Enables or disables the ECC\_MULT\_CALC\_DONE\_INT interrupt.
- [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_CLR](#): Set this bit to clear the ECC\_MULT\_CALC\_DONE\_INT interrupt status. By setting this bit to 1, the [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_RAW](#) and [ECC\\_MULT\\_CALC\\_DONE\\_INT\\_ST](#) bits will be cleared.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

## 23.7 Programming Procedures

The programming procedure for configuring ECC is described below:

1. Configure the ECC clock and reset. Refer to Section [23.5](#) for detailed information.
2. Select the key size and working mode as described in Section [23.4](#).
3. Enable the [ECC\\_MULT\\_CALC\\_DONE\\_INT](#) interrupt as described in Section [23.6](#).
4. Set the [ECC\\_MULT\\_START](#) field to start ECC calculation.

5. Wait for the [ECC\\_MULT\\_CALC\\_DONE\\_INT](#) interrupt, which indicates the completion of the ECC calculation.
6. Check the result as described in Section [23.4](#).

## 23.8 Register Summary

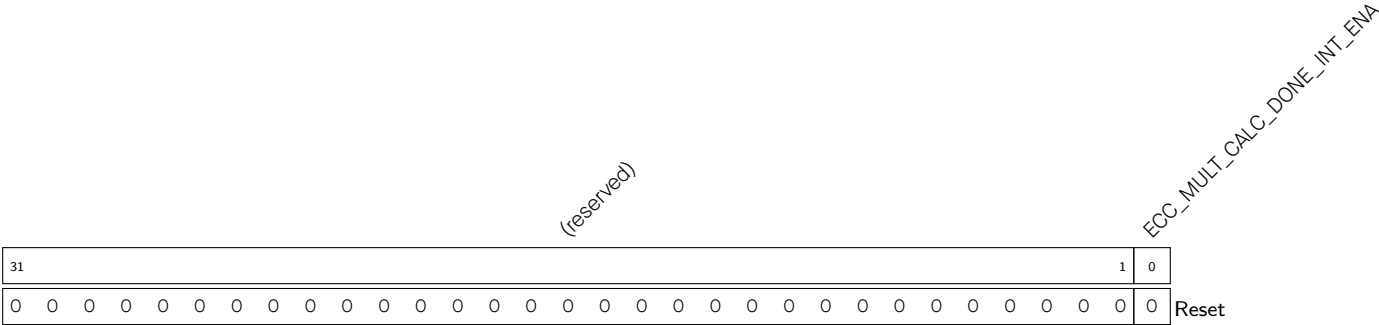
The addresses in this section are relative to ECC Accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                 | Description                          | Address | Access   |
|--------------------------------------|--------------------------------------|---------|----------|
| <b>Interrupt Registers</b>           |                                      |         |          |
| <a href="#">ECC_MULT_INT_RAW_REG</a> | ECC raw interrupt status register    | 0x000C  | R/SS/WTC |
| <a href="#">ECC_MULT_INT_ST_REG</a>  | ECC masked interrupt status register | 0x0010  | RO       |
| <a href="#">ECC_MULT_INT_ENA_REG</a> | ECC interrupt enable register        | 0x0014  | R/W      |
| <a href="#">ECC_MULT_INT_CLR_REG</a> | ECC interrupt clear register         | 0x0018  | WT       |
| <b>Configuration Register</b>        |                                      |         |          |
| <a href="#">ECC_MULT_CONF_REG</a>    | ECC configuration register           | 0x001C  | varies   |
| <b>Version Register</b>              |                                      |         |          |
| <a href="#">ECC_MULT_DATE_REG</a>    | Version control register             | 0x00FC  | R/W      |

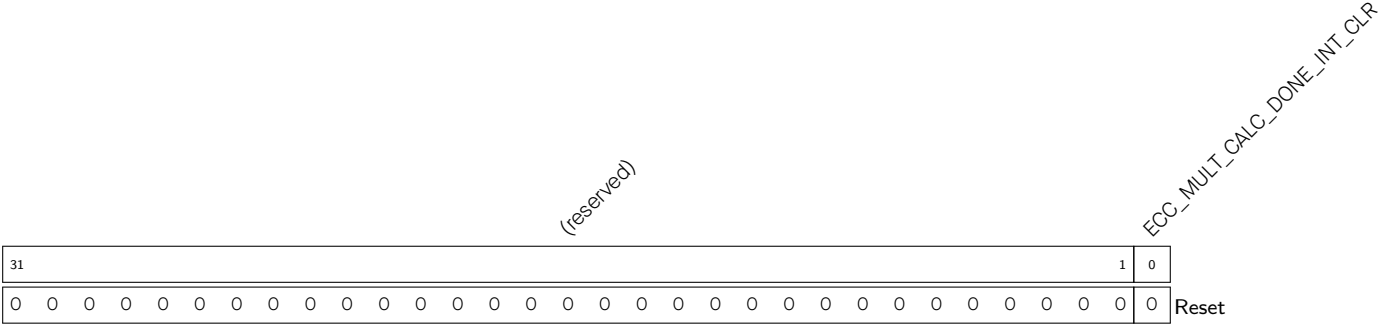


Register 23.3. ECC\_MULT\_INT\_ENA\_REG (0x0014)



ECC\_MULT\_CALC\_DONE\_INT\_ENA Write 1 to enable the ECC\_MULT\_CALC\_DONE\_INT interrupt.  
(R/W)

Register 23.4. ECC\_MULT\_INT\_CLR\_REG (0x0018)



ECC\_MULT\_CALC\_DONE\_INT\_CLR Write 1 to clear the ECC\_MULT\_CALC\_DONE\_INT interrupt. (WT)

Register 23.5. ECC\_MULT\_CONF\_REG (0x001C)

|                                  |  |    |  |    |  |    |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |       |  |   |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |
|----------------------------------|--|----|--|----|--|----|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|-------|--|---|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|
| ECC_MULT_MEM_CLOCK_GATE_FORCE_ON |  |    |  |    |  |    |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |       |  |   |  |  |  |  |  |  |  |  |  |  |  | ECC_MULT_WORK_MODE |  |  |  |  |  |  |  |  |  |  |  | ECC_MULT_MOD_BASE |  |  |  |  |  |  |  |  |  |  |  | ECC_MULT_KEY_LENGTH |  |  |  |  |  |  |  |  |  |  |  | ECC_MULT_RESET |  |  |  |  |  |  |  |  |  |  |  | ECC_MULT_START |  |  |  |  |  |  |  |  |  |  |  |
| 31                               |  | 30 |  | 29 |  | 28 |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  | 9 |  | 7 |  |   |  | 4 |  | 3 |  | 2 |  | 1     |  | 0 |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |
| 0                                |  | 0  |  | 0  |  | 0  |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | Reset |  |   |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |

**ECC\_MULT\_START** Configures whether to start the calculation of the ECC accelerator. This bit will be self-cleared when the calculation is done.

0: No effect

1: Start the calculation of the ECC accelerator

(R/W/SC)

**ECC\_MULT\_RESET** Configures whether to reset the ECC accelerator.

0: No effect

1: Reset

(WT)

**ECC\_MULT\_KEY\_LENGTH** Configures the key length of the ECC accelerator.

0: P-192

1: P-256

(R/W)

**ECC\_MULT\_MOD\_BASE** Configures whether to choose using the mod base or order of base point in the mod operation. Only valid in working modes 8-11.

0: n (order of base point)

1: p (mod base of curve)

(R/W)

**ECC\_MULT\_WORK\_MODE** Configures the working mode of the ECC accelerator.

0: Affine Point Multi mode

1: Reserved

2: Affine Point Verif mode

3: Affine Point Verif + Multi mode

4: Jacobian Point Multi mode

5: Point Add mode

6: Jacobian Point Verif mode

7: Affine Point Verif + Jacobian Point Multi mode

8: Mod Add mode

9: Mod Sub mode

10: Mod Multi mode

11: Mod Div mode

(R/W)

Continued on the next page...

Register 23.5. ECC\_MULT\_CONF\_REG (0x001C)

Continued from the previous page...

**ECC\_MULT\_VERIFICATION\_RESULT** Represents the verification result of the ECC accelerator, valid only when the calculation is done.  
0: Verification failed  
1: Verification passed  
(R/SS)

**ECC\_MULT\_CLK\_EN** Configures whether to force on register clock gate.  
0: No effect  
1: Force on  
(R/W)

**ECC\_MULT\_MEM\_CLOCK\_GATE\_FORCE\_ON** Configures whether to force on ECC memory clock gate.  
0: No effect  
1: Force on  
(R/W)

Register 23.6. ECC\_MULT\_DATE\_REG (0x00FC)

|            |    |    |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | ECC_MULT_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0  | 0  | 0 | 0x2207180     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ECC\_MULT\_DATE** Version control register. (R/W)

## Chapter 24

### HMAC Accelerator (HMAC)

The Hash-based Message Authentication Code (HMAC) module computes Message Authentication Codes (MACs) using hash algorithm SHA-256 and keys as described in RFC 2104. The 256-bit HMAC key is stored in an eFuse key block and can be set as read-protected, i.e., the key is not accessible from outside the HMAC accelerator.

#### 24.1 Main Features

- Standard HMAC-SHA-256 algorithm
- HMAC-SHA-256 calculation based on key in eFuse,
  - whose result cannot be accessed by software in downstream mode for high security
  - whose result can be accessed by software in upstream mode
- Generates required keys for the Digital Signature Algorithm (DSA) peripheral in downstream mode
- Re-enables soft-disabled JTAG in downstream mode

#### 24.2 Functional Description

The HMAC module operates in two modes: upstream mode and downstream mode. In upstream mode, users provide the HMAC message and read back the calculation result. In downstream mode, the HMAC module provides input to two possible other internal hardware modules: On the one hand, an HMAC can be used to enable JTAG after JTAG has been temporarily disabled before. On the other hand, an HMAC can be used as decryption key for Digital Signature parameters stored in flash memory for the DSA peripheral. Furthermore, the calculations happen internally and automatically in downstream mode, so that confidentiality of any key and derived key material is ensured, given correct configuration.

**Note:**

After the reset signal being released, the HMAC module will check whether the DSA key exists in the eFuse. If the key exists, the HMAC module will enter downstream digital signature algorithm mode and finish the DSA key calculation automatically. This process is automatically completed by hardware and does not require software participation. When the downstream operation after reset is completed, the HMAC will automatically return to the idle state.

##### 24.2.1 Upstream Mode

To calculate the HMAC value in upstream mode, users should perform the following steps:

1. Initialize the HMAC module and enter upstream mode.



2. Write the correctly padded message to the HMAC, one block at a time.
3. Read back the result from HMAC.

For details of this process, please see Section [24.2.5](#).

**Note:**

Common use cases for the upstream mode are challenge-response protocols supporting HMAC-SHA-256. Assume the two entities in the challenge-response protocol are A and B respectively, and the data message they expect to exchange is M. The general authentication process of this protocol is as follows:

- A calculates a unique random number M.
- A sends M to B.
- B calculates the HMAC (through M and KEY) and sends the result to A.
- A calculates the HMAC (through M and KEY) internally.
- A compares the two results. If the results are the same, then the identity of B is authenticated.

## 24.2.2 Downstream Mode - JTAG Enable Feature

JTAG debugging can be disabled by eFuse in a way which allows later re-enabling using the HMAC module. (For more details, please see Chapter [7 eFuse Controller](#).) The HMAC module will expect the user to supply the HMAC result for one of the eFuse keys. The HMAC module will check whether the supplied HMAC matches the one calculated from the chosen key. If both HMACs are the same, JTAG will be enabled until the user calls the HMAC module to clear the results and consequently disable JTAG again.

To re-enable JTAG, users should perform the following steps:

1. Enable the HMAC module by initializing clock and reset signals of HMAC, and enter downstream JTAG enable mode by configuring [HMAC\\_SET\\_PARA\\_PURPOSE\\_REG](#). Then, wait for the calculation to complete. Please see Section [24.2.5](#) for more details.
2. Write 1 to the [HMAC\\_SOFT\\_JTAG\\_CTRL\\_REG](#) register to enter JTAG re-enable mode.
3. Write the 256-bit HMAC value to register [HMAC\\_WR\\_JTAG\\_REG](#). This value is obtained by performing a local HMAC calculation from the 32-byte 0x00 using SHA-256 and the key that has been written to the eFuse. It needs to be written 8 times and 32-bit each time in big-endian word order.
4. If the HMAC result calculated from the key in the eFuse matches the value that users wrote in step 3, then JTAG is re-enabled. Otherwise, JTAG remains disabled.
5. After writing 1 to [HMAC\\_SET\\_INVALIDATE\\_JTAG\\_REG](#) or resetting the chip, JTAG will be disabled. If users want to re-enable JTAG again, they need to repeat the above steps again.

## 24.2.3 Downstream Mode - Digital Signature Algorithm and Key Derivation Feature

The Digital Signature Algorithm (DSA) module encrypts its parameters using the AES-CBC algorithm. The HMAC module is used as a Key Derivation Function (KDF) to derive the AES key to decrypt these parameters (parameter decryption key).

Before starting the DSA module, users need to obtain the parameter decryption key for the DSA module through HMAC calculation. For more information, please see Chapter [27 Digital Signature Algorithm \(DSA\)](#). After the chip is powered on, the HMAC module will check whether the key required to calculate the parameter decryption key has been burned in the eFuse block. If the key has been burned, HMAC module will automatically enter the downstream digital signature algorithm mode and complete the HMAC calculation based on the chosen key.

### 24.2.4 HMAC eFuse Configuration

Each HMAC key burned into an eFuse block has a key purpose, specifying for which functionality the key can be used. The HMAC module will not accept a key with a non-matching purpose for any functionality. The HMAC module provides three different functionalities: re-enabling JTAG, DSA KDF in downstream mode, and pure HMAC calculation in upstream mode. For each functionality, there exists a corresponding key purpose, listed in Table [24.2-1](#). Additionally, another purpose specifies a key which may be used for re-enabling JTAG as well as for serving as DSA KDF.

Before enabling HMAC to do calculations, user should make sure the key to be used has been burned in eFuse by reading the registers EFUSE\_KEY\_PURPOSE\_x (We have a total of 6 keys in eFuse, so the value of x is 0 ~ 5. Among which, [EFUSE\\_KEY\\_PURPOSE\\_0 ~ EFUSE\\_KEY\\_PURPOSE\\_1](#) belong to the register [EFUSE\\_RD\\_REPEAT\\_DATA1\\_REG](#), and [EFUSE\\_KEY\\_PURPOSE\\_2 ~ EFUSE\\_KEY\\_PURPOSE\\_5](#) belong to the register [EFUSE\\_RD\\_REPEAT\\_DATA2\\_REG](#)) from [7 eFuse Controller](#). Take upstream mode as an example, if there is no EFUSE\_KEY\_PURPOSE\_HMAC\_UP in EFUSE\_KEY\_PURPOSE\_0 ~ 5, it means there is no key in eFuse that can be used for the HMAC upstream mode. Users can burn a key to eFuse as follows:

1. Prepare a secret 256-bit HMAC key and burn the key to an empty eFuse block  $y$ . As there are 6 blocks for storing a key in eFuse and the numbers of those blocks range from 4 to 9, the value of  $y$  is 4 ~ 9. Hence, when talking about key0, it means eFuse block4. Then, program the purpose to EFUSE\_KEY\_PURPOSE\_ $(y - 4)$ . Take upstream mode as an example: after programming the key, the user should program EFUSE\_KEY\_PURPOSE\_HMAC\_UP (corresponding value is 8) to EFUSE\_KEY\_PURPOSE\_ $(y - 4)$ . Please see Chapter [7 eFuse Controller](#) on how to program eFuse keys.
2. If needed, configure this eFuse key block to be read protected, so that users cannot read its value. A copy of this key should be kept by any party who needs to verify this device.

Please note that the key whose purpose is EFUSE\_KEY\_PURPOSE\_HMAC\_DOWN\_ALL can be used for both re-enabling JTAG or DSA.

**Table 24.2-1. HMAC Purposes and Configuration Value**

| Purpose                         | Mode       | Value | Description                                   |
|---------------------------------|------------|-------|---|
| JTAG Re-enable                  | Downstream | 6     | EFUSE_KEY_PURPOSE_HMAC_DOWN_JTAG              |
| DSA KDF                         | Downstream | 7     | EFUSE_KEY_PURPOSE_HMAC_DOWN_DIGITAL_SIGNATURE |
| HMAC Calculation                | Upstream   | 8     | EFUSE_KEY_PURPOSE_HMAC_UP                     |
| Both JTAG Re-enable and DSA KDF | Downstream | 5     | EFUSE_KEY_PURPOSE_HMAC_DOWN_ALL               |

#### Select eFuse Key Blocks and HMAC Purposes

The eFuse controller provides six key blocks, i.e., KEY0 ~ 5. To select a particular KEY $n$  for an HMAC calculation, write the key number  $n$  to register [HMAC\\_SET\\_PARA\\_KEY\\_REG](#).

Write a correct purpose to register [HMAC\\_SET\\_PARA\\_PURPOSE\\_REG](#) (see Section 24.2.5). Note that the purpose of the key has also been programmed to eFuse memory. Only when the configured HMAC purpose matches the defined purpose of KEY $n$ , the HMAC module will execute the configured calculation. Otherwise, it will return a matching error and stop the current calculation.

For example, suppose a user selects KEY3 for HMAC calculation, and the value programmed to [EFUSE\\_KEY\\_PURPOSE\\_3](#) is 6 (EFUSE\_KEY\_PURPOSE\_HMAC\_DOWN\_JTAG). Based on Table 24.2-1, KEY3 can be used to re-enable JTAG. If the value written to register [HMAC\\_SET\\_PARA\\_PURPOSE\\_REG](#) is also 6, then the HMAC module will start the process to re-enable JTAG.

## 24.2.5 HMAC Process (Detailed)

The process for users to call HMAC in ESP32-P4 is as follows:

### 24.2.5.1 Enable HMAC Module

1. Set the peripheral clock bits for HMAC and SHA peripherals in register [HP\\_SYS\\_CLKRST\\_REG\\_CRYPTO\\_HMAC\\_CLK\\_EN](#), and clear the corresponding peripheral reset bits in register [HP\\_SYS\\_CLKRST\\_REG\\_RST\\_EN\\_HMAC](#). For information on those registers, please see Chapter 9 [Reset and Clock](#).
2. Write 1 to register [HMAC\\_SET\\_START\\_REG](#).

### 24.2.5.2 Configure HMAC Keys and Key Purposes

1. Write the key purpose  $m$  to register [HMAC\\_SET\\_PARA\\_PURPOSE\\_REG](#). The possible key purpose values are shown in Table 24.2-1. For more information, please refer to Section 24.2.4.
2. Select KEY $n$  in eFuse memory as the key by writing  $n$  (ranges from 0 to 5) to register [HMAC\\_SET\\_PARA\\_KEY\\_REG](#). For more information, please refer to Section 24.2.4.
3. Write 1 to register [HMAC\\_SET\\_PARA\\_FINISH\\_REG](#) to complete the configuration.
4. Read register [HMAC\\_QUERY\\_ERROR\\_REG](#). If its value is 1, it means the purpose of the selected block does not match the configured key purpose and the calculation will not proceed. If its value is 0, it means the purpose of the selected block matches the configured key purpose, and then the calculation can proceed.
5. When the value of [HMAC\\_SET\\_PARA\\_PURPOSE\\_REG](#) is not 8, it means the HMAC module is in downstream mode, proceed with 24.2.5.3. When the value is 8, it means the HMAC module is in upstream mode, proceed with 24.2.5.4.

### 24.2.5.3 Downstream Mode Process

1. Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
2. To clear the result and make further usage of the dependent hardware (JTAG or DSA) impossible, write 1 to either register [HMAC\\_SET\\_INVALIDATE\\_JTAG\\_REG](#) to clear the result generated by the JTAG key; or to register [HMAC\\_SET\\_INVALIDATE\\_DS\\_REG](#) to clear the result generated by DSA key. Afterwards, the HMAC process needs to be restarted to re-enable any of the dependent peripherals.

#### 24.2.5.4 Upstream Mode Process

1. Write message in upstream mode:

- (a) Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
- (b) Apply SHA padding to message as described in Section 24.3.1, and get message block: Block\_*n* (*n* ≥ 0)
- (c) Perform one of the following operations according to the block number *n*:
  - If there is only one message block in total which has included all padding bits:
    - i. Write the 512-bit Block\_*n* to register [HMAC\\_WR\\_MESSAGE\\_n\\_REG](#) (*n*: 0-15). Write 1 to register [HMAC\\_SET\\_MESSAGE\\_ONE\\_REG](#), to trigger the processing of this message block.
    - ii. Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
    - iii. Write 1 to register [HMAC\\_ONE\\_BLOCK\\_REG](#), and finish message transmission.
  - If Block\_*n* is the last padded block:
    - i. Write the 512-bit Block\_0 to register [HMAC\\_WR\\_MESSAGE\\_n\\_REG](#) (*n*: 0-15). Write 1 to register [HMAC\\_SET\\_MESSAGE\\_ONE\\_REG](#), to trigger the processing of this message block.
    - ii. Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
    - iii. Message transmission finished automatically.
  - If Block\_*n* is the second last padded block:
    - i. Write the 512-bit Block\_*n* to register [HMAC\\_WR\\_MESSAGE\\_n\\_REG](#) (*n*: 0-15). Write 1 to register [HMAC\\_SET\\_MESSAGE\\_ONE\\_REG](#), to trigger the processing of this message block.
    - ii. Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
    - iii. Write 1 to register [HMAC\\_SET\\_MESSAGE\\_PAD\\_REG](#), and continue message transmission (jump back to step (c)).
  - If Block\_*n* is neither the last nor the second last message block:
    - i. Write the 512-bit Block\_*n* to register [HMAC\\_WR\\_MESSAGE\\_n\\_REG](#) (*n*: 0-15). Write 1 to register [HMAC\\_SET\\_MESSAGE\\_ONE\\_REG](#), to trigger the processing of this message block.
    - ii. Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
    - iii. Write 1 to register [HMAC\\_SET\\_MESSAGE\\_ING\\_REG](#), and continue message transmission (jump back to step (c)).

2. Read hash result in upstream mode:

- (a) Poll Status register [HMAC\\_QUERY\\_BUSY\\_REG](#) until it reads 0.
- (b) Read hash result from register [HMAC\\_RD\\_RESULT\\_n\\_REG](#) (*n*: 0-7).
- (c) Write 1 to register [HMAC\\_SET\\_RESULT\\_FINISH\\_REG](#) to finish calculation. The result will be cleared at the same time.
- (d) Upstream mode operation is completed.

**Note:**

The SHA accelerator can be called directly, or used internally by the DSA module and the HMAC module. However, they can not share the hardware resources simultaneously. Therefore, the SHA module must not be called neither by the CPU nor by the DSA module when the HMAC module is in use.

## 24.3 HMAC Algorithm Details

### 24.3.1 Padding Bits

The HMAC module uses SHA-256 as hash algorithm. If the input message is not a multiple of 512 bits, the user must apply a SHA-256 padding algorithm in software. The SHA-256 padding algorithm is the same as described in Section *Padding the Message* of [FIPS PUB 180-4](#). In downstream mode, users do not need to input any message or apply padding. The HMAC module uses a default 32-byte pattern of 0x00 for re-enabling JTAG and a 32-byte pattern of 0xff for deriving the AES key for the DSA module.

For the convenience of reading, here we will briefly describe the process of message padding. As shown in Figure 24.3-1, suppose the length of the unpadded message is  $m$  bits. Padding steps are as follows:

1. Append one bit of value "1" to the end of the unpadded message.
2. Append  $k$  bits of value "0", where  $k$  is the smallest non-negative number which satisfies  $m + 1 + k \equiv 448 \pmod{512}$ .
3. Append a 64-bit integer value as a binary block. This block consists of the length of the unpadded message as a big-endian binary integer value  $m$ .

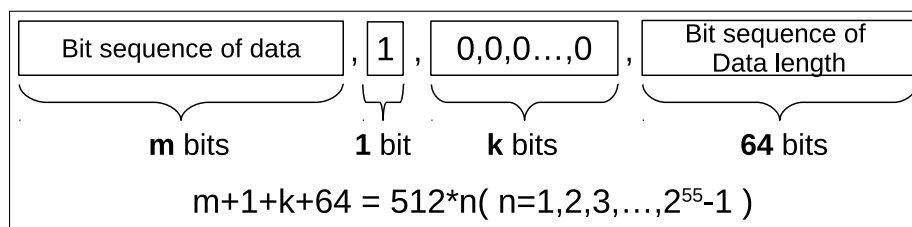


Figure 24.3-1. HMAC SHA-256 Padding Diagram

In upstream mode, if the length of the unpadded message is a multiple of 512 bits, users can configure hardware to apply SHA padding by writing 1 to [HMAC\\_SET\\_MESSAGE\\_END\\_REG](#) or do padding work themselves by writing 1 to [HMAC\\_SET\\_MESSAGE\\_PAD\\_REG](#). If the length is not a multiple of 512 bits, SHA padding must be manually applied by the user. After the user prepared the padding data, they should complete the subsequent configuration according to the Section 24.2.5.

### 24.3.2 HMAC Algorithm Structure

The structure of the implemented algorithm in the HMAC module is shown in Figure 24.3-2. This is the standard HMAC algorithm as described in RFC 2104.

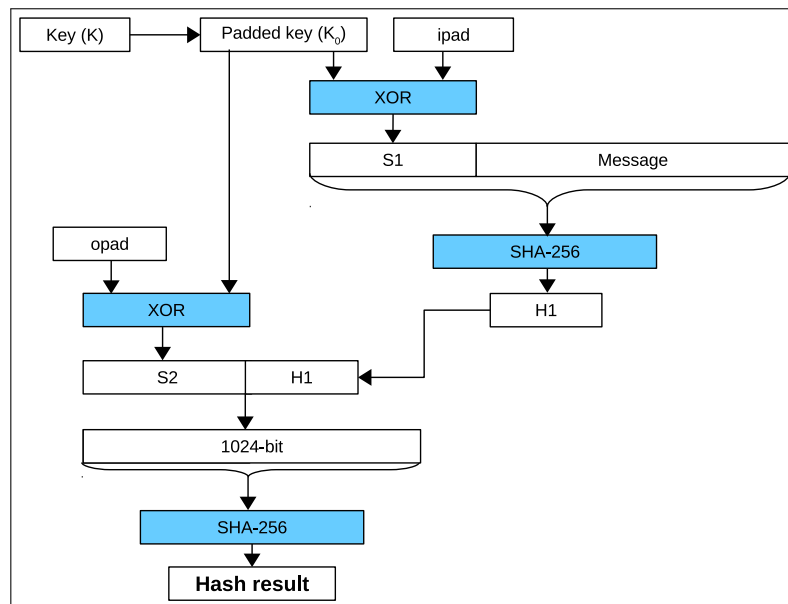


Figure 24.3-2. HMAC Structure Schematic Diagram

In Figure 24.3-2:

1. ipad is a 512-bit message block composed of 64 bytes of 0x36.
2. opad is a 512-bit message block composed of 64 bytes of 0x5c.

The HMAC module appends a 256-bit 0 sequence after the bit sequence of the 256-bit key K in order to get a 512-bit  $K_0$ . Then, the HMAC module XORs  $K_0$  with ipad to get the 512-bit S1. Afterwards, the HMAC module appends the input message (multiple of 512 bits) after the 512-bit S1, and exercises the SHA-256 algorithm to get the 256-bit H1.

The HMAC module appends the 256-bit SHA-256 hash result H1 to the 512-bit S2 value, which is calculated using the XOR operation of  $K_0$  and opad. A 768-bit sequence will be generated. Then, the HMAC module uses the SHA padding algorithm described in Section 24.3.1 to pad the 768-bit sequence to a 1024-bit sequence, and applies the SHA-256 algorithm to get the final hash result (256-bit).

## 24.4 Register Summary

The addresses in this section are relative to HMAC Accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Control/Status Registers</b>              |  |         |        |
| <a href="#">HMAC_SET_START_REG</a>           | HMAC start control register  | 0x0040  | WO     |
| <a href="#">HMAC_SET_PARA_FINISH_REG</a>     | HMAC configuration completion register   | 0x004C  | WO     |
| <a href="#">HMAC_SET_MESSAGE_ONE_REG</a>     | HMAC message control register  | 0x0050  | WO     |
| <a href="#">HMAC_SET_MESSAGE_ING_REG</a>     | HMAC message continue register   | 0x0054  | WO     |
| <a href="#">HMAC_SET_MESSAGE_END_REG</a>     | HMAC message end register  | 0x0058  | WO     |
| <a href="#">HMAC_SET_RESULT_FINISH_REG</a>   | HMAC result reading finish register  | 0x005C  | WO     |
| <a href="#">HMAC_SET_INVALIDATE_JTAG_REG</a> | Invalidate JTAG result register  | 0x0060  | WO     |
| <a href="#">HMAC_SET_INVALIDATE_DS_REG</a>   | Invalidate digital signature result register                                       | 0x0064  | WO     |
| <a href="#">HMAC_QUERY_ERROR_REG</a>         | Stores matching results between keys generated by users and corresponding purposes | 0x0068  | RO     |
| <a href="#">HMAC_QUERY_BUSY_REG</a>          | Busy state of HMAC module  | 0x006C  | RO     |
| <a href="#">HMAC_SET_MESSAGE_PAD_REG</a>     | Software padding register  | 0x00F0  | WO     |
| <a href="#">HMAC_ONE_BLOCK_REG</a>           | One block message register   | 0x00F4  | WO     |
| <b>Configuration Registers</b>               |  |         |        |
| <a href="#">HMAC_SET_PARA_PURPOSE_REG</a>    | HMAC parameter configuration register  | 0x0044  | WO     |
| <a href="#">HMAC_SET_PARA_KEY_REG</a>        | HMAC parameters configuration register   | 0x0048  | WO     |
| <a href="#">HMAC_SOFT_JTAG_CTRL_REG</a>      | Re-enable JTAG register 0  | 0x00F8  | WO     |
| <a href="#">HMAC_WR_JTAG_REG</a>             | Re-enable JTAG register 1  | 0x00FC  | WO     |
| <b>HMAC Message Block</b>                    |  |         |        |
| <a href="#">HMAC_WR_MESSAGE_0_REG</a>        | Message register 0   | 0x0080  | WO     |
| <a href="#">HMAC_WR_MESSAGE_1_REG</a>        | Message register 1   | 0x0084  | WO     |
| <a href="#">HMAC_WR_MESSAGE_2_REG</a>        | Message register 2   | 0x0088  | WO     |
| <a href="#">HMAC_WR_MESSAGE_3_REG</a>        | Message register 3   | 0x008C  | WO     |
| <a href="#">HMAC_WR_MESSAGE_4_REG</a>        | Message register 4   | 0x0090  | WO     |
| <a href="#">HMAC_WR_MESSAGE_5_REG</a>        | Message register 5   | 0x0094  | WO     |
| <a href="#">HMAC_WR_MESSAGE_6_REG</a>        | Message register 6   | 0x0098  | WO     |
| <a href="#">HMAC_WR_MESSAGE_7_REG</a>        | Message register 7   | 0x009C  | WO     |
| <a href="#">HMAC_WR_MESSAGE_8_REG</a>        | Message register 8   | 0x00A0  | WO     |
| <a href="#">HMAC_WR_MESSAGE_9_REG</a>        | Message register 9   | 0x00A4  | WO     |
| <a href="#">HMAC_WR_MESSAGE_10_REG</a>       | Message register 10  | 0x00A8  | WO     |
| <a href="#">HMAC_WR_MESSAGE_11_REG</a>       | Message register 11  | 0x00AC  | WO     |
| <a href="#">HMAC_WR_MESSAGE_12_REG</a>       | Message register 12  | 0x00B0  | WO     |
| <a href="#">HMAC_WR_MESSAGE_13_REG</a>       | Message register 13  | 0x00B4  | WO     |
| <a href="#">HMAC_WR_MESSAGE_14_REG</a>       | Message register 14  | 0x00B8  | WO     |
| <a href="#">HMAC_WR_MESSAGE_15_REG</a>       | Message register 15  | 0x00BC  | WO     |
| <b>HMAC Upstream Result</b>                  |  |         |        |

| Name                                 | Description              | Address | Access |
|--------------------------------------|--------------------------|---------|--------|
| <a href="#">HMAC_RD_RESULT_0_REG</a> | Hash result register 0   | 0x00C0  | RO     |
| <a href="#">HMAC_RD_RESULT_1_REG</a> | Hash result register 1   | 0x00C4  | RO     |
| <a href="#">HMAC_RD_RESULT_2_REG</a> | Hash result register 2   | 0x00C8  | RO     |
| <a href="#">HMAC_RD_RESULT_3_REG</a> | Hash result register 3   | 0x00CC  | RO     |
| <a href="#">HMAC_RD_RESULT_4_REG</a> | Hash result register 4   | 0x00D0  | RO     |
| <a href="#">HMAC_RD_RESULT_5_REG</a> | Hash result register 5   | 0x00D4  | RO     |
| <a href="#">HMAC_RD_RESULT_6_REG</a> | Hash result register 6   | 0x00D8  | RO     |
| <a href="#">HMAC_RD_RESULT_7_REG</a> | Hash result register 7   | 0x00DC  | RO     |
| <b>Version Register</b>              |                          |         |        |
| <a href="#">HMAC_DATE_REG</a>        | Version control register | 0x01FC  | R/W    |

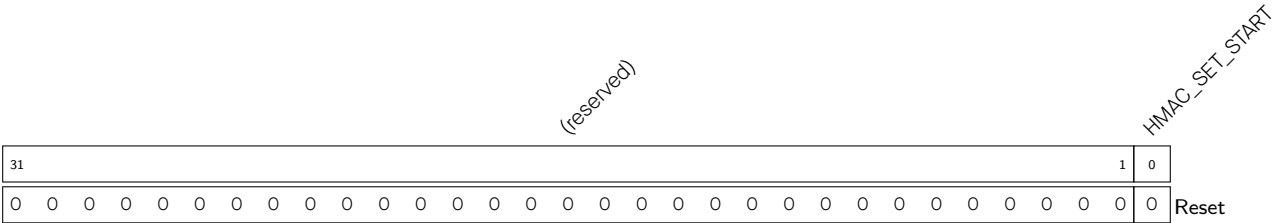


## 24.5 Registers

The addresses in this section are relative to HMAC Accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 24.1. HMAC\_SET\_START\_REG (0x0040)

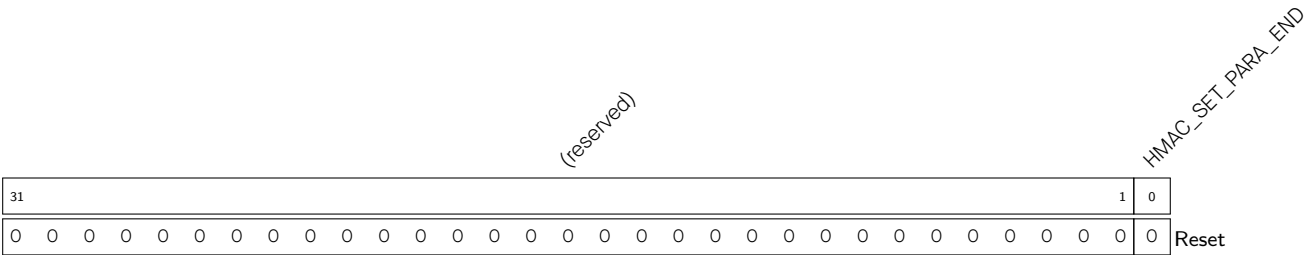


**HMAC\_SET\_START** Configures whether or not to enable HMAC.

- 0: Disable HMAC
- 1: Enable HMAC

(WO)

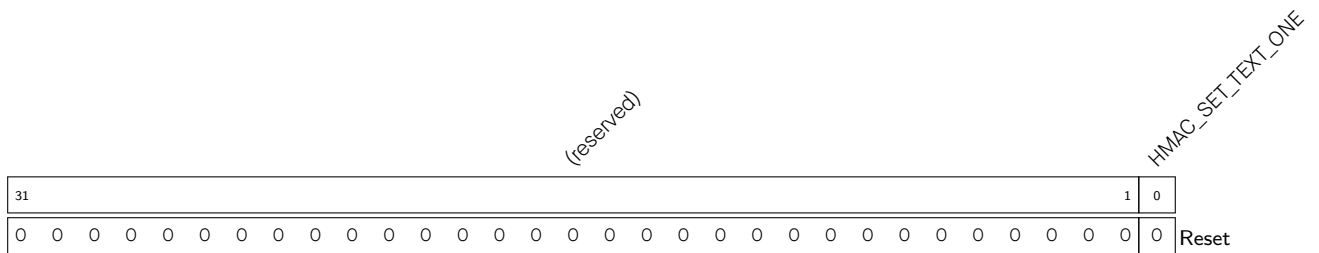
Register 24.2. HMAC\_SET\_PARA\_FINISH\_REG (0x004C)



**HMAC\_SET\_PARA\_FINISH** Configures whether to finish HMAC configuration.

- 0: No effect
- 1: Finish configuration

(WO)

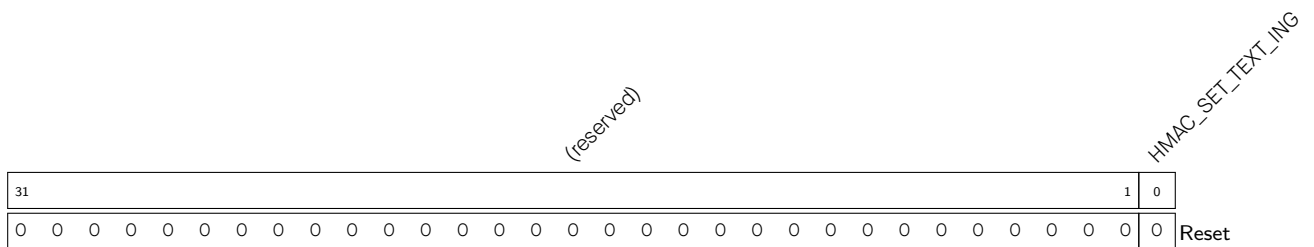
**Register 24.3. HMAC\_SET\_MESSAGE\_ONE\_REG (0x0050)**

**HMAC\_SET\_TEXT\_ONE** Calls SHA to calculate one message block.

0: No effect

1: Calls SHA to calculate one message block.

(WO)

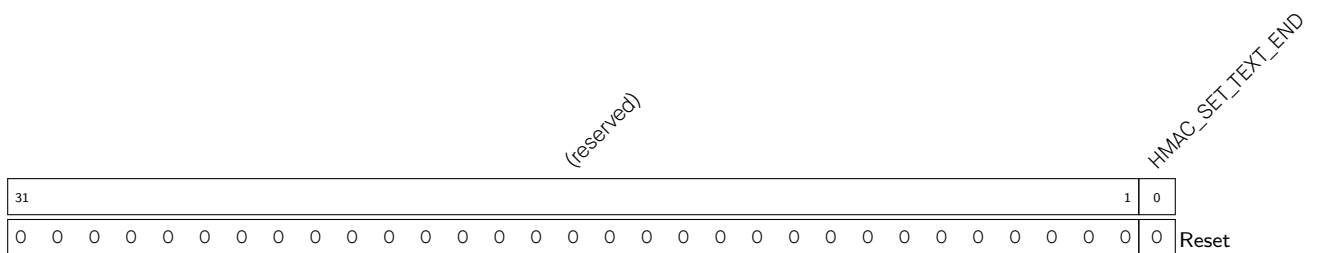
**Register 24.4. HMAC\_SET\_MESSAGE\_ING\_REG (0x0054)**

**HMAC\_SET\_TEXT\_ING** Configures whether or not there are unprocessed message blocks.

0: No unprocessed message block

1: There are still some message blocks to be processed.

(WO)

**Register 24.5. HMAC\_SET\_MESSAGE\_END\_REG (0x0058)**

**HMAC\_SET\_TEXT\_END** Configures whether to start hardware padding.

0: No effect

1: Start hardware padding

(WO)

### Register 24.6. HMAC\_SET\_RESULT\_FINISH\_REG (0x005C)

[illegible]

**HMAC\_SET\_RESULT\_END** Configures whether to exit upstream mode and clear calculation results.

0: Not exit

1: Exit upstream mode and clear calculation results.

(WO)

### Register 24.7. HMAC\_SET\_INVALIDATE\_JTAG\_REG (0x0060)

[illegible]

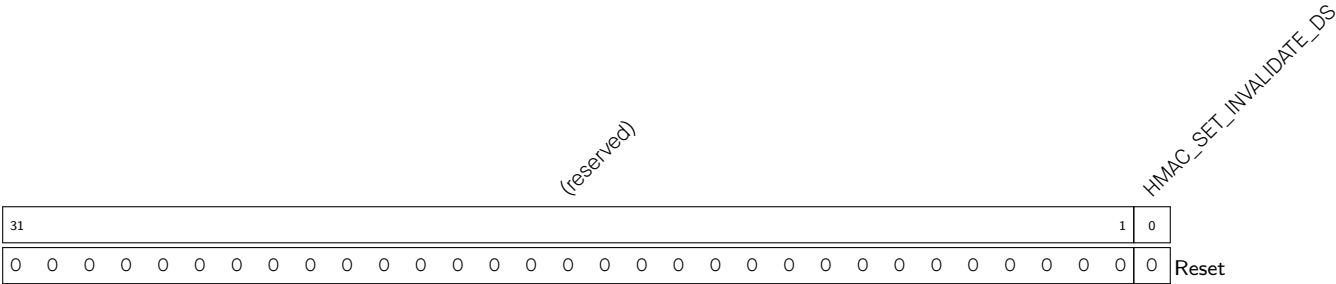
**HMAC\_SET\_INVALIDATE\_JTAG** Configures whether or not to clear calculation results when re-enabling JTAG in downstream mode.

0: Not clear

### 1: Clear calculation results

(WO)

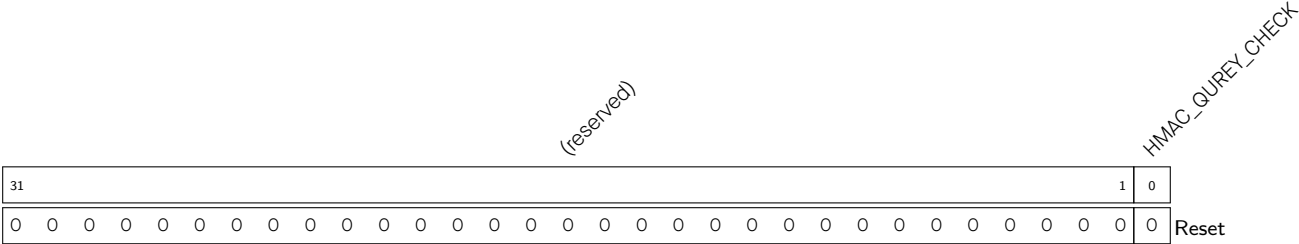
Register 24.8. HMAC\_SET\_INVALIDATE\_DS\_REG (0x0064)



**HMAC\_SET\_INVALIDATE\_DS** Configures whether or not to clear calculation results of the DS module in downstream mode.

- 0: Not clear
- 1: Clear calculation results (WO)

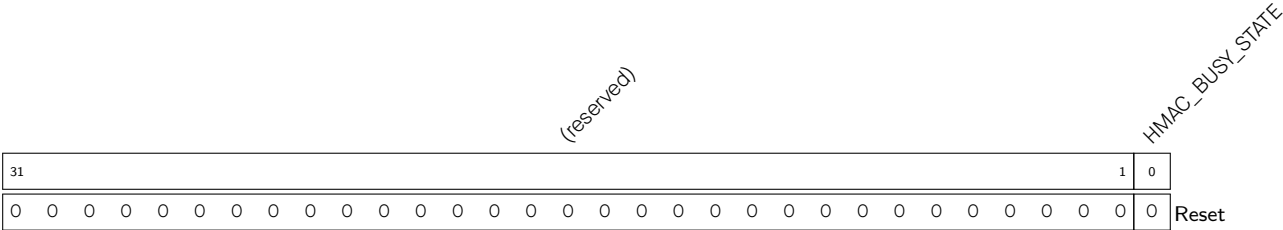
Register 24.9. HMAC\_QUERY\_ERROR\_REG (0x0068)



**HMAC\_QUEY\_CHECK** Represents whether or not an HMAC key matches the purpose.

- 0: Match
- 1: Error (RO)

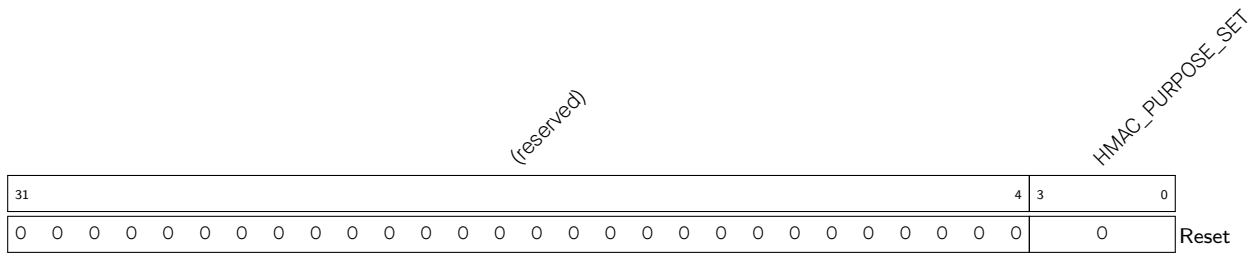
Register 24.10. HMAC\_QUERY\_BUSY\_REG (0x006C)



**HMAC\_BUSY\_STATE** Represents whether or not HMAC is in a busy state. Before configuring HMAC, please make sure HMAC is in an IDLE state.

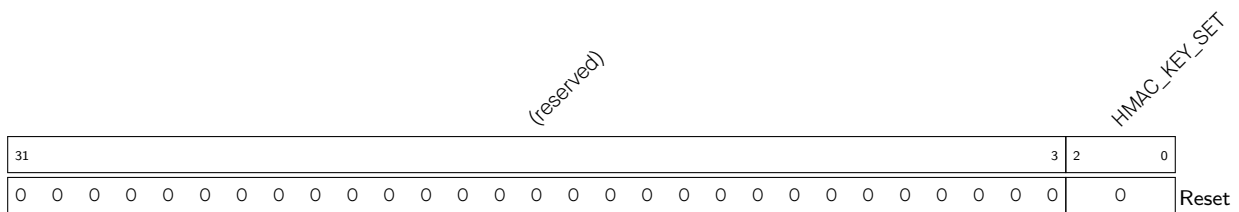
- 0: Idle
- 1: HMAC is still working on the calculation (RO)

Register 24.11. HMAC\_SET\_PARA\_PURPOSE\_REG (0x0044)

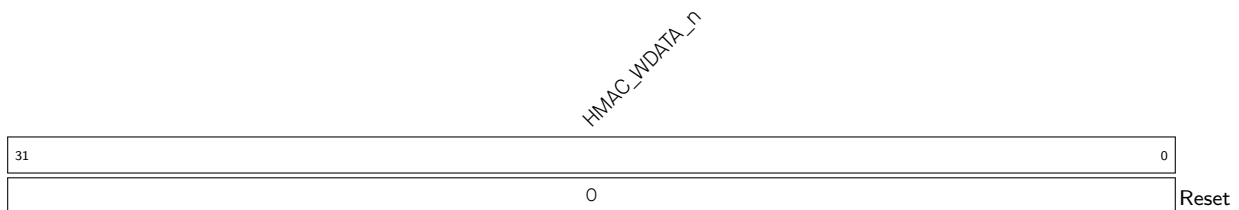


**HMAC\_PURPOSE\_SET** Configures the HMAC purpose, refer to the Table 24.2-1. (WO)

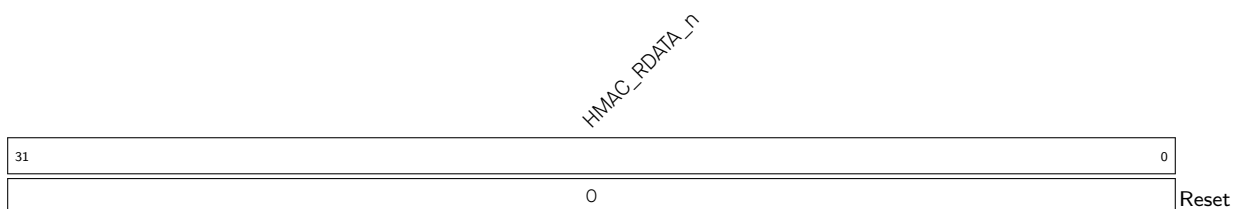
Register 24.12. HMAC\_SET\_PARA\_KEY\_REG (0x0048)



**HMAC\_KEY\_SET** Configures HMAC key. There are six keys with index 0~5. Write the index of the selected key to this field. (WO)

Register 24.13. HMAC\_WR\_MESSAGE\_ *n* \_REG (*n*: 0-15) (0x0080+4\**n*)

**HMAC\_WDATA\_ *n*** Represents the *n*th 32-bit of message. (WO)

Register 24.14. HMAC\_RD\_RESULT\_ *n* \_REG (*n*: 0-7) (0x00C0+4\**n*)

**HMAC\_RDATA\_ *n*** Represents the *n*th 32-bit of hash result. (RO)

**Register 24.15. HMAC\_SET\_MESSAGE\_PAD\_REG (0x00F0)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HMAC_SET_TEXT_PAD |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**HMAC\_SET\_TEXT\_PAD** Configures whether or not the padding is applied by software.

0: Not applied by software

1: Applied by software

(WO)

**Register 24.16. HMAC\_ONE\_BLOCK\_REG (0x00F4)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                    |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HMAC_SET_ONE_BLOCK |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                  |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                  | 0 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |

**HMAC\_SET\_ONE\_BLOCK** Write 1 to indicate there is only one block which already contains padding bits and there is no need for padding. (WO)

**Register 24.17. HMAC\_SOFT\_JTAG\_CTRL\_REG (0x00F8)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | HMAC_SOFT_JTAG_CTRL |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | Reset |

**HMAC\_SOFT\_JTAG\_CTRL** Configures whether or not to enable JTAG authentication mode.

0: Disable

1: Enable

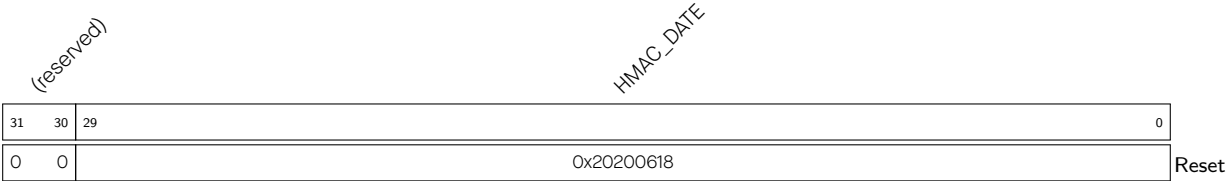
(WO)

Register 24.18. HMAC\_WR\_JTAG\_REG (0x00FC)



**HMAC\_WR\_JTAG** Writes the comparing input used for re-enabling JTAG. (WO)

Register 24.19. HMAC\_DATE\_REG (0x01FC)



**HMAC\_DATE** Version control register. (R/W)

## Chapter 25

### RSA Accelerator (RSA)

#### 25.1 Introduction

The RSA accelerator provides hardware support for high-precision computation used in various RSA asymmetric cipher algorithms, significantly improving their run time and reducing their software complexity compared with RSA algorithms implemented solely in software. The RSA accelerator also supports operands of different lengths, which provides more flexibility during the computation.

#### 25.2 Features

The following functionality is supported:

- Large-number modular exponentiation with two additional acceleration options to further increase the calculation speed
- Large-number modular multiplication
- Large-number multiplication
- Operands of different lengths
- Interrupt on completion of computation

#### 25.3 Functional Description

The RSA accelerator is activated by setting the HP\_SYS\_CLKRST\_REG\_CRYPT0\_RSA\_CLK\_EN bit in the [HP\\_SYS\\_CLKRST\\_PERI\\_CLK\\_CTRL25\\_REG](#) register and clearing the HP\_SYS\_CLKRST\_REG\_RST\_EN\_RSA bit in the [HP\\_SYS\\_CLKRST\\_HP\\_RST\\_EN2\\_REG](#) register. Additionally, users also need to clear HP\_SYS\_CLKRST\_REG\_RST\_EN\_DS and HP\_SYS\_CLKRST\_REG\_RST\_EN\_ECDSA bits to reset the [Digital Signature Algorithm \(DSA\)](#) and the [Elliptic Curve Digital Signature Algorithm \(ECDSA\)](#) accelerators.

The RSA accelerator is only available after the [RSA-related memories](#) are initialized. The content of the [RSA\\_QUERY\\_CLEAN\\_REG](#) register is 0 during initialization and will become 1 after the initialization is done. Therefore, wait until [RSA\\_QUERY\\_CLEAN\\_REG](#) becomes 1 before using the RSA accelerator.

The [RSA\\_INT\\_ENA\\_REG](#) register is used to control the interrupt triggered on completion of computation. Write 1 or 0 to this field to enable or disable the interrupt. By default, the interrupt function of the RSA accelerator is enabled.

**Notice:**

ESP32-P4's [Digital Signature Algorithm \(DSA\)](#) and [Elliptic Curve Digital Signature Algorithm \(ECDSA\)](#) modules also call



the RSA accelerator when working. Therefore, users cannot access the RSA accelerator when the [Digital Signature Algorithm \(DSA\)](#) or the [Elliptic Curve Digital Signature Algorithm \(ECDSA\)](#) module is working.

### 25.3.1 Definitions and Representations

ESP32-P4's RSA accelerator supports operands of different lengths  $N = 32 \times n$ .

To represent the numbers used as operands, let us define a base- $b$  positional notation, as follows:

$$b = 2^{32}$$

Using this notation, each number is represented by a sequence of base- $b$  digits:

$$n = \frac{N}{32}$$

$$Z = (Z_{n-1}Z_{n-2} \cdots Z_0)_b$$

$$X = (X_{n-1}X_{n-2} \cdots X_0)_b$$

$$Y = (Y_{n-1}Y_{n-2} \cdots Y_0)_b$$

$$M = (M_{n-1}M_{n-2} \cdots M_0)_b$$

$$\bar{r} = (\bar{r}_{n-1}\bar{r}_{n-2} \cdots \bar{r}_0)_b$$

Each of the values in  $Z_{n-1} \cdots Z_0$ ,  $X_{n-1} \cdots X_0$ ,  $Y_{n-1} \cdots Y_0$ ,  $M_{n-1} \cdots M_0$ ,  $\bar{r}_{n-1} \cdots \bar{r}_0$  represents one base- $b$  digit (a 32-bit word).

$Z_{n-1}$ ,  $X_{n-1}$ ,  $Y_{n-1}$ ,  $M_{n-1}$  and  $\bar{r}_{n-1}$  are the most significant bits of  $Z$ ,  $X$ ,  $Y$ ,  $M$ , while  $Z_0$ ,  $X_0$ ,  $Y_0$ ,  $M_0$  and  $\bar{r}_0$  are the least significant bits.

If we define  $R = b^n$ , the additional argument  $\bar{r}$  can be calculated as  $\bar{r} = R^2 \bmod M$ .

Also, argument  $M'$  can be calculated using the formula below:

$$M' = -M^{-1} \bmod b$$

where,  $M^{-1}$  is the [modular multiplicative inverse](#) of  $M$ , and it can be calculated with the extended binary GCD algorithm.

### 25.3.2 Large-Number Modular Exponentiation

Large-number modular exponentiation performs  $Z = X^Y \bmod M$ . The computation is based on Montgomery multiplication. Therefore, aside from the  $X$ ,  $Y$ , and  $M$  arguments, two additional ones are needed —  $\bar{r}$  and  $M'$ , which need to be calculated in advance by software.

The RSA accelerator supports operands of length  $N = 32 \times n$ , where  $n \in \{1, 2, 3, \dots, 128\}$ . The bit lengths of arguments  $Z$ ,  $X$ ,  $Y$ ,  $M$ , and  $\bar{r}$  can be arbitrary  $N$ , but all numbers in a calculation must be of the same length. The bit length of  $M'$  must be 32.

Large-number modular exponentiation on the ESP32-P4 can be implemented as follows:

1. Write 1 or 0 to the [RSA\\_INT\\_ENA](#) field to enable or disable the interrupt function.
2. Configure relevant registers:

- (a) Write  $(\frac{N}{32} - 1)$  to the [RSA\\_MODE\\_REG](#) register.

- (b) Write  $M'$  to the [RSA\\_M\\_PRIME\\_REG](#) register.
- (c) Configure registers related to the acceleration options, which are described later in Section 25.3.5.
- 3. Write  $X_i$ ,  $Y_i$ ,  $M_i$  and  $\bar{r}_i$  for  $i \in \{0, 1, \dots, n-1\}$  to memory blocks [RSA\\_X\\_MEM](#), [RSA\\_Y\\_MEM](#), [RSA\\_M\\_MEM](#) and [RSA\\_Z\\_MEM](#). The capacity of each memory block is 128 words. Each word of each memory block can store one base- $b$  digit. The memory blocks use the little endian format for storage, i.e., the least significant digit of each number is in the lowest address.  
  
Users need to write data to each memory block only according to the length of the number; data beyond this length is ignored.
- 4. Write 1 to the [RSA\\_SET\\_START\\_MODEXP](#) field of the [RSA\\_SET\\_START\\_MODEXP\\_REG](#) register to start computation.
- 5. Wait for the completion of computation, which happens when the content of [RSA\\_QUERY\\_IDLE](#) becomes 1 or the RSA interrupt occurs, if enabled.
- 6. Read the result  $Z_i$  for  $i \in \{0, 1, \dots, n-1\}$  from [RSA\\_Z\\_MEM](#).
- 7. If you have the interrupt enabled, write 1 to [RSA\\_CLEAR\\_INTERRUPT](#) to clear the interrupt.

After the computation, the [RSA\\_MODE\\_REG](#) register, memory blocks [RSA\\_Y\\_MEM](#) and [RSA\\_M\\_MEM](#), as well as the [RSA\\_M\\_PRIME\\_REG](#) remain unchanged. However,  $X_i$  in [RSA\\_X\\_MEM](#) and  $\bar{r}_i$  in [RSA\\_Z\\_MEM](#) computation are overwritten, and only these overwritten memory blocks need to be re-initialized before starting another computation.

### 25.3.3 Large-Number Modular Multiplication

Large-number modular multiplication performs  $Z = X \times Y \bmod M$ . This computation is based on Montgomery multiplication. Therefore, similar to the large-number modular exponentiation, two additional arguments are needed –  $\bar{r}$  and  $M'$ , which need to be calculated in advance by software.

The RSA accelerator supports large-number modular multiplication with operands of length  $N = 32 \times n$ , where  $n \in \{1, 2, 3, \dots, 128\}$ .

The computation can be executed as follows:

- 1. Write 1 or 0 to the [RSA\\_INT\\_ENA\\_REG](#) register to enable or disable the interrupt function.
- 2. Configure relevant configuration registers:
  - (a) Write  $(\frac{N}{32} - 1)$  to the [RSA\\_MODE\\_REG](#) register.
  - (b) Write  $M'$  to the [RSA\\_M\\_PRIME\\_REG](#) register.
- 3. Write  $X_i$ ,  $Y_i$ ,  $M_i$ , and  $\bar{r}_i$  for  $i \in \{0, 1, \dots, n-1\}$  to memory blocks [RSA\\_X\\_MEM](#), [RSA\\_Y\\_MEM](#), [RSA\\_M\\_MEM](#), and [RSA\\_Z\\_MEM](#), respectively. The capacity of each memory block is 128 words. Each word of each memory block can store one base- $b$  digit. The memory blocks use the little endian format for storage, i.e., the least significant digit of each number is in the lowest address.  
  
Users need to write data to each memory block only according to the length of the number; data beyond this length are ignored.
- 4. Write 1 to the [RSA\\_SET\\_START\\_MODMULT](#) field.

5. Wait for the completion of computation, which happens when the content of [RSA\\_QUERY\\_IDLE](#) becomes 1 or the RSA interrupt occurs, if enabled.
6. Read the result  $Z_i$  for  $i \in \{0, 1, \dots, n-1\}$  from [RSA\\_Z\\_MEM](#).
7. If you have the interrupt enabled, write 1 to [RSA\\_CLEAR\\_INTERRUPT](#) to clear the interrupt, .

After the computation, the length of operands in [RSA\\_MODE\\_REG](#), the  $X_i$  in memory [RSA\\_X\\_MEM](#), the  $Y_i$  in memory [RSA\\_Y\\_MEM](#), the  $M_i$  in memory [RSA\\_M\\_MEM](#), and the  $M'$  in memory [RSA\\_M\\_PRIME\\_REG](#) remain unchanged. However, the  $\bar{r}_i$  in memory [RSA\\_Z\\_MEM](#) has already been overwritten, and only this overwritten memory block needs to be re-initialized before starting another computation.

### 25.3.4 Large-Number Multiplication

Large-number multiplication performs  $Z = X \times Y$ . The length of result  $Z$  is twice that of operand  $X$  and operand  $Y$ . Therefore, the RSA accelerator only supports large-number multiplication with operand length  $N = 32 \times n$ , where  $n \in \{1, 2, 3, \dots, 64\}$ . The length  $\hat{N}$  of result  $Z$  is  $2 \times N$ .

The computation can be executed as follows:

1. Write 1 or 0 to the [RSA\\_INT\\_ENA\\_REG](#) register to enable or disable the interrupt function.
2. Write  $(\frac{\hat{N}}{32} - 1)$ , i.e.,  $(\frac{N}{16} - 1)$  to the [RSA\\_MODE\\_REG](#) register.
3. Write  $X_i$  and  $Y_i$  for  $i \in \{0, 1, \dots, n-1\}$  to memory blocks [RSA\\_X\\_MEM](#) and [RSA\\_Z\\_MEM](#). Each word of each memory block can store one base- $b$  digit. The memory blocks use the little endian format for storage, i.e., the least significant digit of each number is in the lowest address.  $n$  is  $\frac{N}{32}$ .

Write  $X_i$  for  $i \in \{0, 1, \dots, n-1\}$  to the address of the  $i$  words of the [RSA\\_X\\_MEM](#) memory block. Note that  $Y_i$  for  $i \in \{0, 1, \dots, n-1\}$  will not be written to the address of the  $i$  words of the [RSA\\_Z\\_MEM](#) register, but the address of the  $n + i$  words, i.e., the base address of the [RSA\\_Z\\_MEM](#) memory plus the address offset  $4 \times (n + i)$ .

Users need to write data to each memory block only according to the length of the number; data beyond this length is ignored.

4. Write 1 to the [RSA\\_SET\\_START\\_MULT](#) register.
5. Wait for the completion of computation, which happens when the content of [RSA\\_QUERY\\_IDLE](#) becomes 1 or the RSA interrupt occurs, if enabled.
6. Read the result  $Z_i$  for  $i \in \{0, 1, \dots, \hat{n}-1\}$  from the [RSA\\_Z\\_MEM](#) register.  $\hat{n}$  is  $2 \times n$ .
7. If you have the interrupt enabled, write 1 to [RSA\\_CLEAR\\_INTERRUPT](#) to clear the interrupt.

After the computation, the length of operands in [RSA\\_MODE\\_REG](#) and the  $X_i$  in memory [RSA\\_X\\_MEM](#) remain unchanged. However, the  $Y_i$  in memory [RSA\\_Z\\_MEM](#) has already been overwritten, and only this overwritten memory block needs to be re-initialized before starting another computation.

### 25.3.5 Options for Additional Acceleration

The ESP32-P4 RSA accelerator also provides [SEARCH](#) and [CONSTANT\\_TIME](#) options that can be configured to further accelerate the large-number modular exponentiation. By default, both options are configured as no additional acceleration.

Users can choose to use one or two of these options to further accelerate the computation. Note that, even when none of these two options is configured, using the hardware RSA accelerator is still much faster than implementing the RSA algorithm in software.

To be more specific, when neither of these two options are configured for additional acceleration, the time required to calculate  $Z = X^Y \bmod M$  is solely determined by the lengths of operands. When either or both of these two options are configured for additional acceleration, the time required is also correlated with the 0 and 1 bit distribution in  $Y$ .

To better illustrate how these two options work, first assume  $Y$  is represented in binaries as

$$Y = (\tilde{Y}_{N-1}\tilde{Y}_{N-2}\cdots\tilde{Y}_{t+1}\tilde{Y}_t\tilde{Y}_{t-1}\cdots\tilde{Y}_0)_2$$

where,

- $N$  is the length of  $Y$ ,
- $\tilde{Y}_t$  is 1,
- $\tilde{Y}_{N-1}, \tilde{Y}_{N-2}, \dots, \tilde{Y}_{t+1}$  are all equal to 0,
- and  $\tilde{Y}_{t-1}, \tilde{Y}_{t-2}, \dots, \tilde{Y}_0$  are either 0 or 1 but exactly  $m$  bits should be equal to 0 and  $t-m$  bits 1, i.e., the Hamming weight of  $\tilde{Y}_{t-1}\tilde{Y}_{t-2}, \dots, \tilde{Y}_0$  is  $t-m$ .

When either of these two options is configured for additional acceleration:

- SEARCH Option (Configuring [RSA\\_SEARCH\\_ENABLE](#) to 1 for additional acceleration)
  - The accelerator ignores the bit positions of  $\tilde{Y}_i$ , where  $i > \alpha$ . Search position  $\alpha$  is set by configuring the [RSA\\_SEARCH\\_POS\\_REG](#) register. Set  $\alpha$  to a number smaller than  $N-1$ , which otherwise leads to the same result as if this option is not used for additional acceleration. The best acceleration performance can be achieved by setting  $\alpha$  to  $t$ , in which case all the  $\tilde{Y}_{N-1}, \tilde{Y}_{N-2}, \dots, \tilde{Y}_{t+1}$  of 0 s are ignored during the calculation. Note that if you set  $\alpha$  to be less than  $t$ , then the result of the modular exponentiation  $Z = X^Y \bmod M$  will be incorrect.
  - Note that this option compromises the security because it ignores some bits, which essentially shortens the key length, thus should not be enabled for applications with high security requirement.
- CONSTANT\_TIME Option (Configuring [RSA\\_CONSTANT\\_TIME\\_REG](#) to 0 for additional acceleration)
  - The accelerator speeds up the calculation by simplifying the calculation concerning the 0 bits of  $Y$ . Therefore, the higher the proportion of bits 0 against bits 1, the better is the acceleration performance.
  - Note that this option also compromises the security because its time cost correlates with the 0/1 distribution of the key, which can be used in a Side Channel Attack (SCA), thus should not be enabled for applications with high security requirement.

Below is an example to demonstrate the performance of the RSA accelerator under different combinations of [SEARCH](#) and [CONSTANT\\_TIME](#) configuration. In this example:

- We perform  $Z = X^Y \bmod M$
- $N = 3072$

- $Y = 65537$
- $X$  and  $M$  are taken at random
- When the SEARCH option is enabled,  $\alpha$ , i.e., the position register [RSA\\_SEARCH\\_POS\\_REG](#), is set to 16.

Table 25.3-1 below demonstrates the time cost in clock cycles under different combinations of [SEARCH](#) and [CONSTANT\\_TIME](#) configuration when performing  $Z = X^Y \bmod M$  as described above.

**Table 25.3-1. Acceleration Performance**

| SEARCH Option   | CONSTANT_TIME Option | Time Cost (clock cycle) |
|-----------------|----------------------|-------------------------|
| No acceleration | No acceleration      | $174.7 \times 10^6$     |
| Accelerated     | No acceleration      | $1.023 \times 10^6$     |
| No acceleration | Acceleration         | $0.546 \times 10^6$     |
| Acceleration    | Acceleration         | $0.540 \times 10^6$     |

As shown in Table 25.3-1:

- The time cost is biggest when none of these two options is configured for additional acceleration.
- The time cost is smallest when both of these two options are configured for additional acceleration.
- The time cost can be dramatically reduced when either or both option(s) are configured for additional acceleration.

## 25.4 Interrupts

ESP32-P4's RSA accelerator can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- RSA\_INTR

There is one internal interrupt source from the RSA accelerator that can generate the above interrupt signal. The interrupt source from the RSA accelerator is listed with its trigger condition and the resulting interrupt signal in Table 25.4-1.

**Table 25.4-1. RSA's Internal Interrupt Source**

| Internal Interrupt Source | Trigger Condition                | Interrupt Signal |
|---------------------------|----------------------------------|------------------|
| RSA_CALC_DONE_INT         | Completion of an RSA calculation | RSA_INTR         |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

## 25.5 Memory Summary

The addresses in this section are relative to the RSA accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

Table 25.5-1. RSA Accelerator Memory Blocks

| Name                      | Description | Size (byte) | Starting Address | Ending Address | Access |
|---------------------------|-------------|-------------|------------------|----------------|--------|
| <a href="#">RSA_M_MEM</a> | Memory M    | 512         | 0x0000           | 0x01FF         | R/W    |
| <a href="#">RSA_Z_MEM</a> | Memory Z    | 512         | 0x0200           | 0x03FF         | R/W    |
| <a href="#">RSA_Y_MEM</a> | Memory Y    | 512         | 0x0400           | 0x05FF         | R/W    |
| <a href="#">RSA_X_MEM</a> | Memory X    | 512         | 0x0600           | 0x07FF         | R/W    |

## 25.6 Register Summary

The addresses in this section are relative to the RSA accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

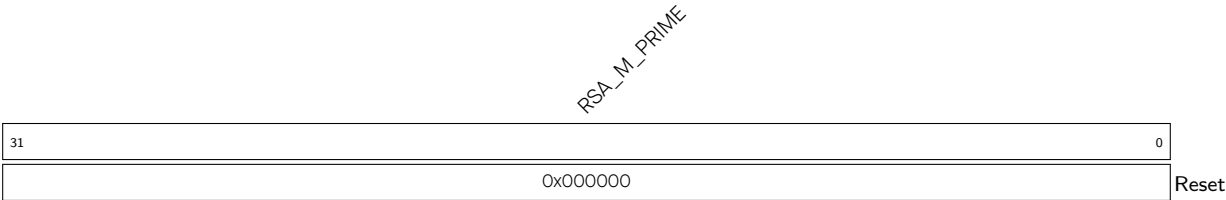
| Name                                      | Description                         | Address | Access |
|---|-------------------------------------|---------|--------|
| <b>Control or Configuration Registers</b> |                                     |         |        |
| <a href="#">RSA_M_PRIME_REG</a>           | Represents M'                       | 0x0800  | R/W    |
| <a href="#">RSA_MODE_REG</a>              | Configures RSA length               | 0x0804  | R/W    |
| <a href="#">RSA_SET_START_MODEXP_REG</a>  | Starts modular exponentiation       | 0x080C  | WT     |
| <a href="#">RSA_SET_START_MODMULT_REG</a> | Starts modular multiplication       | 0x0810  | WT     |
| <a href="#">RSA_SET_START_MULT_REG</a>    | Starts multiplication               | 0x0814  | WT     |
| <a href="#">RSA_QUERY_IDLE_REG</a>        | Represents the RSA status           | 0x0818  | RO     |
| <a href="#">RSA_CONSTANT_TIME_REG</a>     | Configures the constant_time option | 0x0820  | R/W    |
| <a href="#">RSA_SEARCH_ENABLE_REG</a>     | Configures the search option        | 0x0824  | R/W    |
| <a href="#">RSA_SEARCH_POS_REG</a>        | Configures the search position      | 0x0828  | R/W    |
| <b>Status Register</b>                    |                                     |         |        |
| <a href="#">RSA_QUERY_CLEAN_REG</a>       | RSA initialization status           | 0x0808  | RO     |
| <b>Interrupt Registers</b>                |                                     |         |        |
| <a href="#">RSA_INT_CLR_REG</a>           | Clears RSA interrupt                | 0x081C  | WT     |
| <a href="#">RSA_INT_ENA_REG</a>           | Enables the RSA interrupt           | 0x082C  | R/W    |
| <b>Version Control Register</b>           |                                     |         |        |
| <a href="#">RSA_DATE_REG</a>              | Version control register            | 0x0830  | R/W    |

## 25.7 Registers

The addresses in this section are relative to the RSA accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

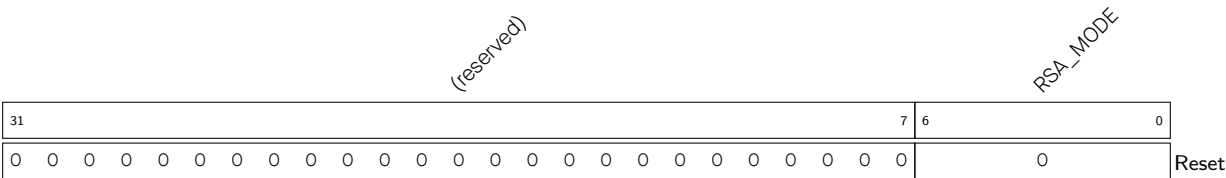
For how to program reserved fields, please refer to Section IX .

Register 25.1. RSA\_M\_PRIME\_REG (0x0800)



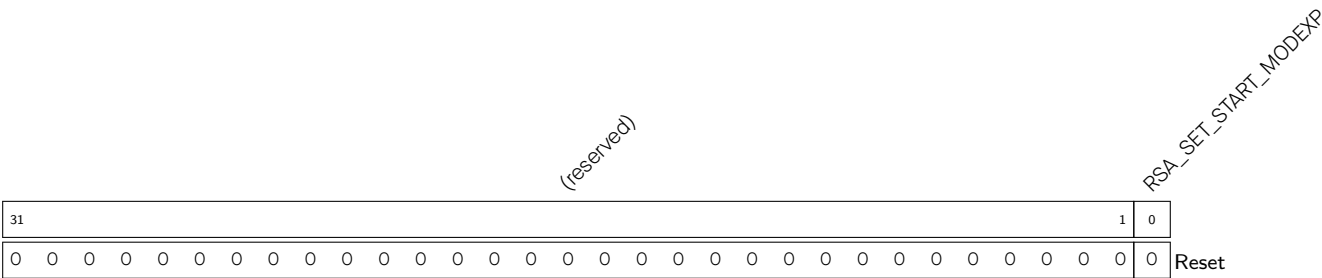
**RSA\_M\_PRIME** Represents  $M'$ . (R/W)

Register 25.2. RSA\_MODE\_REG (0x0804)



**RSA\_MODE** Configures the RSA length. (R/W)

Register 25.3. RSA\_SET\_START\_MODEXP\_REG (0x080C)



**RSA\_SET\_START\_MODEXP** Configures whether or not to starts the modular exponentiation.

- 0: No effect
  - 1: Start
- (WT)

#### Register 25.4. RSA\_SET\_START\_MODMULT\_REG (0x0810)

Diagram of the RSA\_SET\_START\_MODMULT register structure:

- Bit 31: reserved
- Bits 0-30: RSA\_SET\_START\_MODMULT
- Bit 0: Reset

**RSA\_SET\_START\_MODMULT** Configures whether or not to start the modular multiplication.

0: No effect

1: Start

(WT)

### Register 25.5. RSA\_SET\_START\_MULT\_REG (0x0814)

Diagram illustrating the structure of the **RSA\_SET\_START\_MULT** register:

- The register is 32 bits wide, with bit positions 31 down to 0.
- Bit 31 is the most significant bit.
- Bits 31 down to 1 are labeled **(reserved)**.
- Bit 0 is labeled **0**.
- The register is divided into two main sections:
  - RSA\_SET\_START\_MULT** (bits 31 down to 1): This section contains the reserved bits.
  - Reset** (bit 0): This section contains the reset bit.

**RSA\_SET\_START\_MULT** Configures whether or not to start the multiplication.

0: No effect

1: Start

(WT)

### Register 25.6. RSA\_QUERY\_IDLE\_REG (0x0818)

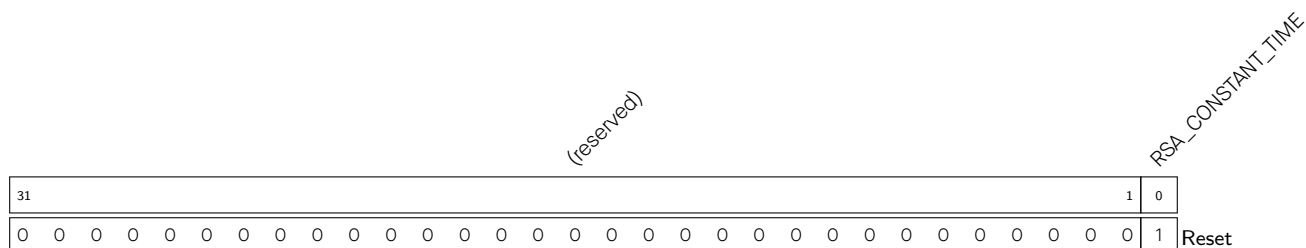
**RSA\_QUERY\_IDLE** Represents the RSA status.

0: Busy

1: Idle

(RO)



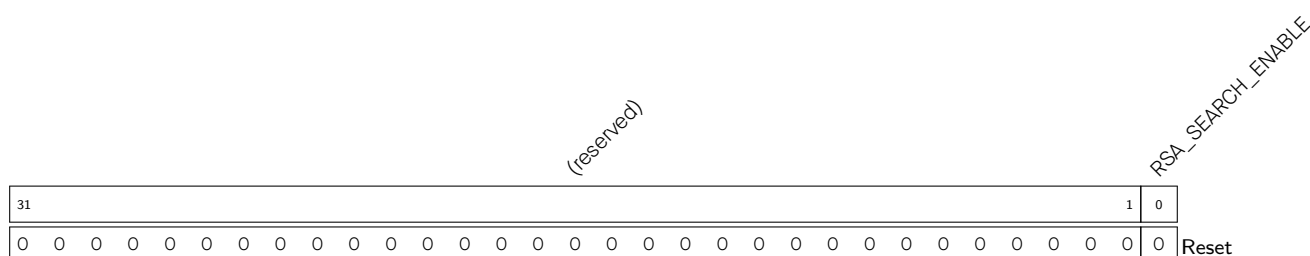
**Register 25.7. RSA\_CONSTANT\_TIME\_REG (0x0820)**

**RSA\_CONSTANT\_TIME** Configures the constant\_time option.

0: Acceleration

1: No acceleration (default)

(R/W)

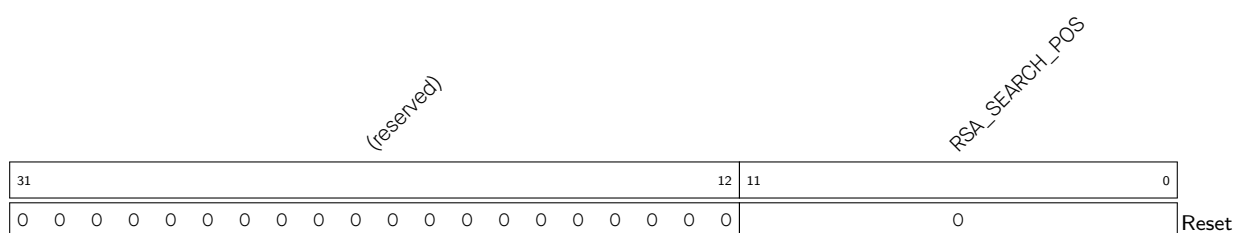
**Register 25.8. RSA\_SEARCH\_ENABLE\_REG (0x0824)**

**RSA\_SEARCH\_ENABLE** Configures the search option.

0: No acceleration (default)

1: Acceleration

This option should be used together with [RSA\\_SEARCH\\_POS\\_REG](#). (R/W)

**Register 25.9. RSA\_SEARCH\_POS\_REG (0x0828)**

**RSA\_SEARCH\_POS** Configures the starting address to start search. This field should be used together with [RSA\\_SEARCH\\_ENABLE\\_REG](#). The field is only valid when [RSA\\_SEARCH\\_ENABLE](#) is high. (R/W)

**Register 25.10. RSA\_QUERY\_CLEAN\_REG (0x0808)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RSA_QUERY_CLEAN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1               | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**RSA\_QUERY\_CLEAN** Represents whether or not the RSA memory completes initialization.

0: Not complete

1: Completed

(RO)

**Register 25.11. RSA\_INT\_CLR\_REG (0x081C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RSA_CLEAR_INTERRUPT |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                   | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | Reset |

**RSA\_CLEAR\_INTERRUPT** Write 1 to clear the RSA interrupt. (WT)

**Register 25.12. RSA\_INT\_ENA\_REG (0x082C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RSA_INT_ENA |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1           | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0           | Reset |

**RSA\_INT\_ENA** Write 1 to enable the RSA interrupt. (R/W)

**Register 25.13. RSA\_DATE\_REG (0x0830)**

|            |    |            |          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|------------|----------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |            | RSA_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 30 | 29         |          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0x20200618 |          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**RSA\_DATE** Version control register. (R/W)

## Chapter 26

### SHA Accelerator (SHA)

#### 26.1 Introduction

ESP32-P4 integrates an SHA accelerator, which is a hardware device that speeds up the SHA algorithm significantly, compared to an SHA algorithm implemented solely in software. The SHA accelerator integrated in ESP32-P4 has two working modes, which are [Typical SHA](#) and [DMA-SHA](#).

#### 26.2 Features

The following functionality is supported:

- The following hash algorithms introduced in [FIPS PUB 180-4 Spec](#).
  - SHA-1
  - SHA-224
  - SHA-256
  - SHA-384
  - SHA-512
  - SHA-512/224
  - SHA-512/256
  - SHA-512/t
- Two working modes
  - Typical SHA
  - DMA-SHA
- Interleaved function when working in Typical SHA working mode
- Interrupt function when working in DMA-SHA working mode

#### 26.3 Working Modes

The SHA accelerator integrated in ESP32-P4 has two working modes.

- [Typical SHA Working Mode](#): all the data is written and read via CPU directly.
- [DMA-SHA Working Mode](#): all the data is read via DMA. That is, users can configure the GDMA-AXI controller to read all the data needed for hash operation, thus releasing CPU for completing other tasks.

The SHA accelerator is activated by setting the [HP\\_SYS\\_CLKRST\\_CRYPT\\_SHA\\_CLK\\_EN](#) register field and clearing the [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_SHA](#) register field. Additionally, due to the hardware reuse relationship between cryptography modules, set the related reset register field of [Digital Signature Algorithm \(DSA\)](#), [HMAC Accelerator \(HMAC\)](#), and [Elliptic Curve Digital Signature Algorithm \(ECDSA\)](#) to 1 can reset the SHA module. Therefore, users also need to clear [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_DS](#), [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_HMAC](#), and [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_ECDSA](#) fields.

Users can start the SHA accelerator with different working modes by configuring registers [SHA\\_START\\_REG](#) and [SHA\\_DMA\\_START\\_REG](#). For details, please see Table 26.3-1.

Table 26.3-1. SHA Accelerator Working Mode

| Working Mode | Configuration Method                       |
|--------------|--|
| Typical SHA  | Set <a href="#">SHA_START_REG</a> to 1     |
| DMA-SHA      | Set <a href="#">SHA_DMA_START_REG</a> to 1 |

Users can choose hash algorithms by configuring the [SHA\\_MODE\\_REG](#) register. For details, please see Table 26.3-2.

Table 26.3-2. SHA Hash Algorithm Selection

| Hash Algorithm | <a href="#">SHA_MODE_REG</a> Configuration |
|----------------|--|
| SHA-1          | 0  |
| SHA-224        | 1  |
| SHA-256        | 2  |
| SHA-384        | 3  |
| SHA-512        | 4  |
| SHA-512/224    | 5  |
| SHA-512/256    | 6  |
| SHA-512/t      | 7  |

**Notice:**

ESP32-P4's [Digital Signature Algorithm \(DSA\)](#) and [HMAC Accelerator \(HMAC\)](#) modules also call the SHA accelerator when working. Therefore, users cannot access the SHA accelerator when these modules are working.

## 26.4 Function Description

The SHA accelerator generates the message digest via two steps: [Preprocessing](#) and [Hash operation](#).

### 26.4.1 Preprocessing

Preprocessing consists of three steps: [padding the message](#), [parsing the message into message blocks](#) and [setting the initial hash value](#).

### 26.4.1.1 Padding the Message

The SHA accelerator can only process message blocks of 512 or 1024 bits, depending on the algorithm. Thus, all the messages should be padded to a multiple of 512 bits or 1024 bits before the hash operation.

Suppose that the length of the message  $M$  is  $m$  bits. Then  $M$  shall be padded as introduced below:

- **SHA-1, SHA-224 and SHA-256**

1. First, append the bit “1” to the end of the message;
2. Second, append  $k$  bits of zeros, where  $k$  is the smallest, non-negative solution to the equation  $m + 1 + k \equiv 448 \bmod 512$ ;
3. Last, append the 64-bit block of value equal to the number  $m$  expressed using a binary representation.

- **SHA-384, SHA-512, SHA-512/224, SHA-512/256 and SHA-512/t**

1. First, append the bit “1” to the end of the message;
2. Second, append  $k$  zero bits, where  $k$  is the smallest, non-negative solution to the equation  $m + 1 + k \equiv 896 \bmod 1024$ ;
3. Last, append the 128-bit block of value equal to the number  $m$  expressed using a binary representation.

For more details, please refer to [FIPS PUB 180-4 Spec](#) > Section “Padding the Message”.

### 26.4.1.2 Parsing the Message

The message and its padding must be parsed into  $N$  512-bit or 1024-bit blocks. During the task, all the message blocks should be written into the [SHA\\_M\\_n\\_REG](#).

- For **SHA-1, SHA-224 and SHA-256**:

The message and its padding are parsed into  $N$  512-bit blocks,  $M^{(1)}, M^{(2)}, \dots, M^{(N)}$ . Since the 512 bits of the input block may be expressed as sixteen 32-bit words, the first 32 bits of message block  $i$  are denoted  $M_0^{(i)}$ , the next 32 bits are  $M_1^{(i)}$ , and so on up to  $M_{15}^{(i)}$ .

During the task,  $M_0^{(i)}$  should be stored in [SHA\\_M\\_0\\_REG](#),  $M_1^{(i)}$  stored in [SHA\\_M\\_1\\_REG](#), ..., and  $M_{15}^{(i)}$  stored in [SHA\\_M\\_15\\_REG](#).

- For **SHA-384, SHA-512, SHA-512/224, SHA-512/256 and SHA-512/t**:

The message and its padding are parsed into  $N$  1024-bit blocks. Since the 1024 bits of the input block may be expressed as sixteen 64-bit words, the first 64 bits of message block  $i$  are denoted  $M_0^{(i)}$ , the next 64 bits are  $M_1^{(i)}$ , and so on up to  $M_{15}^{(i)}$ .

During the task, the most significant 32 bits and the least significant 32 bits of  $M_0^{(i)}$  should be stored in [SHA\\_M\\_0\\_REG](#) and [SHA\\_M\\_1\\_REG](#), respectively, ..., the most significant 32 bits and the least significant 32 bits of  $M_{15}^{(i)}$  should be stored in [SHA\\_M\\_30\\_REG](#) and [SHA\\_M\\_31\\_REG](#), respectively.

**Note:**

For more information about “message block”, please refer to [FIPS PUB 180-4 Spec](#) > Section “Glossary of Terms and Acronyms”.

### 26.4.1.3 Setting the Initial Hash Value

Before hash task begins for each of the secure hash algorithms, the initial Hash value  $H^{(0)}$  must be set based on different algorithms, among which the SHA-1, SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/224, and SHA-512/256 algorithms use the initial Hash values (constant C) stored in the hardware.

However, SHA-512/ $t$  requires a distinct initial hash value for each operation for a given value of  $t$ . Simply put, SHA-512/ $t$  is the generic name for a  $t$ -bit hash function based on SHA-512 whose output is truncated to  $t$  bits.  $t$  is any positive integer without a leading zero such that  $t < 512$ , and  $t$  is not 384. The initial hash value for SHA-512/ $t$  for a given value of  $t$  can be calculated by performing SHA-512 from hexadecimal representation of the string "SHA-512/ $t$ ". It's not hard to observe that when determining the initial hash values for SHA-512/ $t$  algorithms with different  $t$ , the only difference lies in the value of  $t$ .

Therefore, we have specially developed the following simplified method to calculate the initial hash value for SHA-512/ $t$ :

1. **Generate  $t\_string$  and  $t\_length$ :**  $t\_string$  is a 32-bit data that stores the input message of  $t$ .  $t\_length$  is a 7-bit data that stores the length of the input message. The  $t\_string$  and  $t\_length$  are generated in methods described below, depending on the value of  $t$ :

- If  $1 \leq t \leq 9$ , then  $t\_length = 7'h48$  and  $t\_string$  is padded in the following format:

|                  |        |         |
|------------------|--------|---------|
| $8'h30 + 8'ht_0$ | $1'b1$ | $23'b0$ |
|------------------|--------|---------|

where  $t_0 = t$ .

For example, if  $t = 8$ , then  $t_0 = 8$  and  $t\_string = 32'h38800000$ .

- If  $10 \leq t \leq 99$ , then  $t\_length = 7'h50$  and  $t\_string$  is padded in the following format:

|                  |                  |        |         |
|------------------|------------------|--------|---------|
| $8'h30 + 8'ht_1$ | $8'h30 + 8'ht_0$ | $1'b1$ | $15'b0$ |
|------------------|------------------|--------|---------|

where,  $t_0 = t \% 10$  and  $t_1 = t / 10$ .

For example, if  $t = 56$ , then  $t_0 = 6$ ,  $t_1 = 5$ , and  $t\_string = 32'h35368000$ .

- If  $100 \leq t < 512$ , then  $t\_length = 7'h58$  and  $t\_string$  is padded in the following format:

|                  |                  |                  |        |        |
|------------------|------------------|------------------|--------|--------|
| $8'h30 + 8'ht_2$ | $8'h30 + 8'ht_1$ | $8'h30 + 8'ht_0$ | $1'b1$ | $7'b0$ |
|------------------|------------------|------------------|--------|--------|

where,  $t_0 = t \% 10$ ,  $t_1 = (t / 10) \% 10$ , and  $t_2 = t / 100$ .

For example, if  $t = 231$ , then  $t_0 = 1$ ,  $t_1 = 3$ ,  $t_2 = 2$ , and  $t\_string = 32'h32333180$ .

2. **Initialize relevant registers:** Initialize [SHA\\_T\\_STRING\\_REG](#) and [SHA\\_T\\_LENGTH\\_REG](#) with the generated  $t\_string$  and  $t\_length$  in the previous step.
3. **Obtain initial hash value:** Set the [SHA\\_MODE\\_REG](#) register to 7. Set the [SHA\\_START\\_REG](#) register to 1 to start the SHA accelerator. Then poll register [SHA\\_BUSY\\_REG](#) until the content of this register becomes 0, indicating the calculation of initial hash value is completed.

Please note that the initial value for SHA-512/ $t$  can be also calculated according to the Section "5.3.6 SHA-512/ $t$ " in [FIPS PUB 180-4 Spec](#), which is performing SHA-512 operation (with its initial hash value set to the result of 8-bitwise XOR operation of C and 0xa5) from the hexadecimal representation of the string "SHA-512/ $t$ ".

## 26.4.2 Hash Operation

After the preprocessing, the ESP32-P4 SHA accelerator starts to hash a message  $M$  and generates message digest of different lengths, depending on different hash algorithms. As described above, the ESP32-P4 SHA accelerator supports two working modes, which are [Typical SHA](#) and [DMA-SHA](#). The operation process for the SHA accelerator under two working modes is described in the following subsections.

### 26.4.2.1 Typical SHA Mode Process

Usually, the SHA accelerator will process all blocks of a message and produce a message digest before starting the computation of the next message digest.

However, ESP32-P4 SHA also supports optional “interleaved” message digest calculation in Typical SHA mode, which means before SHA completes all blocks of the current message, users are given a chance to insert new computation of another message digest upon the completion of each individual block of the current message.

Specifically, users can read out the message digest from registers [SHA\\_H\\_n\\_REG](#) after completing part of a message digest calculation, and use the SHA accelerator for a different calculation. After the different calculation completes, users can restore the previous message digest to registers [SHA\\_H\\_n\\_REG](#), and resume the accelerator with the previously paused calculation.

#### Typical SHA Process (except for SHA-512/t)

1. Select a hash algorithm.
  - Configure the [SHA\\_MODE\\_REG](#) register based on Table [26.3-2](#).
2. Process the current message block.
  - Write the message block in registers [SHA\\_M\\_n\\_REG](#).
3. Start the SHA accelerator<sup>1</sup>.
  - If this is the first time to execute this step, set the [SHA\\_START\\_REG](#) register to 1 to start the SHA accelerator. In this case, the accelerator uses the initial hash value stored in hardware for a given algorithm configured in Step 1 to start the calculation;
  - If this is not the first time to execute this step<sup>2</sup>, set the [SHA\\_CONTINUE\\_REG](#) register to 1 to start the SHA accelerator. In this case, the accelerator uses the hash value stored in the [SHA\\_H\\_n\\_REG](#) register to start calculation.
4. Check the progress of the current message block.
  - Poll register [SHA\\_BUSY\\_REG](#) until the content of this register becomes 0, indicating the accelerator has completed the calculation for the current message block and now is in the “idle” status<sup>3</sup>.
5. Decide if you have more message blocks to process:
  - If yes, please go back to Step 2.
  - Otherwise, please continue.
6. Obtain the message digest.
  - Read the message digest from registers [SHA\\_H\\_n\\_REG](#).

### Typical SHA Process (SHA-512/t)

1. Select a hash algorithm.
  - Configure the [SHA\\_MODE\\_REG](#) register to 7 for SHA-512/t.
2. Calculate the initial hash value.
  - (a) Calculate `t_string` and `t_length` and initialize [SHA\\_T\\_STRING\\_REG](#) and [SHA\\_T\\_LENGTH\\_REG](#) with the generated `t_string` and `t_length`. For details, please refer to Section 26.4.1.3.
  - (b) Set the [SHA\\_START\\_REG](#) register to 1 to start the SHA accelerator.
  - (c) Poll register [SHA\\_BUSY\\_REG](#) until the content of this register becomes 0, indicating the calculation of initial hash value is completed.
3. Process the current message block<sup>1</sup>.
  - Write the message block in registers [SHA\\_M\\_n\\_REG](#).
4. Start the SHA accelerator
  - Set the [SHA\\_CONTINUE\\_REG](#) register to 1. In this case, the accelerator uses the hash value stored in the [SHA\\_H\\_n\\_REG](#) register to start calculation.
5. Check the progress of the calculation.
  - Poll register [SHA\\_BUSY\\_REG](#) until the content of this register becomes 0, indicating the accelerator has completed the calculation for the current message block and now is in the “idle” status<sup>3</sup>.
6. Decide if you have more message blocks to process:
  - If yes, please go back to Step 3.
  - Otherwise, please continue.
7. Obtain the message digest.
  - Read the message digest from registers [SHA\\_H\\_n\\_REG](#).

**Note:**

1. In this step, the software can also write the next message block (to be processed) in registers [SHA\\_M\\_n\\_REG](#), if any, while the hardware starts SHA calculation, to save time.
2. You are resuming the SHA accelerator with the previously paused calculation.
3. Here you can decide if you want to insert other calculations. If yes, please go to the [process for interleaved calculations](#) for details.

As mentioned above, ESP32-P4 SHA accelerator supports “interleaving” calculation under the Typical SHA working mode.

The process to implement interleaved calculation is described below.

1. Prepare to hand the SHA accelerator over for an interleaved calculation by storing the following data of the previous calculation.
  - The selected hash algorithm configured in the [SHA\\_MODE\\_REG](#) register.
  - The message digest stored in registers [SHA\\_H\\_n\\_REG](#).



2. Perform the interleaved calculation. For the detailed process of the interleaved calculation, please refer to [Typical SHA process](#) or [DMA-SHA process](#), depending on the working mode of your interleaved calculation.
3. Prepare to hand the SHA accelerator back to the previously paused calculation by restoring the following data of the previous calculation.
  - Write the previously stored hash algorithm back to register [SHA\\_MODE\\_REG](#).
  - Write the previously stored message digest back to registers [SHA\\_H\\_n\\_REG](#).
4. Write the next message block from the previous paused calculation in registers [SHA\\_M\\_n\\_REG](#), and set the [SHA\\_CONTINUE\\_REG](#) register to 1 to restart the SHA accelerator with the previously paused calculation.

### 26.4.2.2 DMA-SHA Mode Process

ESP32-P4 SHA accelerator does not support “interleaving” message digest calculation at the level of individual message blocks when using DMA, which means you cannot insert new calculation before a complete DMA-SHA process (of one or more message blocks) completes. In this case, users who need interleaved operation are recommended to divide the message blocks and perform several DMA-SHA calculations, instead of trying to compute all the messages in one go.

Single DMA-SHA calculation supports up to 63 message blocks.

In contrast to the Typical SHA working mode, when the SHA accelerator is working under the DMA-SHA mode, all data read are completed via GDMA-AXI. Therefore, users are required to configure the GDMA-AXI controller following the description in Chapter 3 [GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).

#### DMA-SHA process (except SHA-512/t)

1. Select a hash algorithm.
  - Select a hash algorithm by configuring the [SHA\\_MODE\\_REG](#) register. For details, please refer to Table 26.3-2.
2. Configure the [SHA\\_INT\\_ENA\\_REG](#) register to enable or disable interrupt (Set 1 to enable).
3. Configure the number of message blocks.
  - Write the number of message blocks  $M$  to the [SHA\\_DMA\\_BLOCK\\_NUM\\_REG](#) register.
4. Start the DMA-SHA calculation.
  - If the current DMA-SHA calculation follows a previous calculation, firstly write the message digest from the previous calculation to registers [SHA\\_H\\_n\\_REG](#), then write 1 to register [SHA\\_DMA\\_CONTINUE\\_REG](#) to start SHA accelerator;
  - Otherwise, write 1 to register [SHA\\_DMA\\_START\\_REG](#) to start the accelerator.
5. Wait till the completion of the DMA-SHA calculation, which happens when:
  - The content of [SHA\\_BUSY\\_REG](#) register becomes 0, or
  - An SHA interrupt occurs. In this case, please clear interrupt by writing 1 to the [SHA\\_INT\\_CLEAR\\_REG](#) register.

6. Obtain the message digest:

- Read the message digest from registers [SHA\\_H\\_n\\_REG](#).

#### DMA-SHA process for SHA-512/t

1. Select a hash algorithm.

- Select SHA-512/t algorithm by configuring the [SHA\\_MODE\\_REG](#) register to 7.

2. Configure the [SHA\\_INT\\_ENA\\_REG](#) register to enable or disable interrupt (Set 1 to enable).

3. Calculate the initial hash value.

- (a) Calculate t\_string and t\_length and initialize [SHA\\_T\\_STRING\\_REG](#) and [SHA\\_T\\_LENGTH\\_REG](#) with the generated t\_string and t\_length. For details, please refer to Section [26.4.1.3](#).
- (b) Set the [SHA\\_START\\_REG](#) register to 1 to start the SHA accelerator.
- (c) Poll register [SHA\\_BUSY\\_REG](#) until the content of this register becomes 0, indicating the calculation of initial hash value is completed.

4. Configure the number of message blocks.

- Write the number of message blocks  $M$  to the [SHA\\_DMA\\_BLOCK\\_NUM\\_REG](#) register.

5. Start the DMA-SHA calculation.

- Write 1 to register [SHA\\_DMA\\_CONTINUE\\_REG](#) to start the accelerator.

6. Wait till the completion of the DMA-SHA calculation, which happens when:

- The content of [SHA\\_BUSY\\_REG](#) register becomes 0, or
- An SHA interrupt occurs. In this case, please clear interrupt by writing 1 to the [SHA\\_INT\\_CLEAR\\_REG](#) register.

7. Obtain the message digest:

- Read the message digest from registers [SHA\\_H\\_n\\_REG](#).

### 26.4.3 Message Digest

After the hash task completes, the SHA accelerator writes the message digest from the task to registers [SHA\\_H\\_n\\_REG](#) ( $n$ : 0 ~ 15). The lengths of the generated message digest are different depending on different hash algorithms. For details, see Table [26.4-4](#) below:

Table 26.4-4. The Storage and Length of Message Digest from Different Algorithms

| Hash Algorithm | Length of Message Digest (in bits) | Storage <sup>1</sup>       |
|----------------|------------------------------------|----------------------------|
| SHA-1          | 160                                | SHA_H_O_REG ~ SHA_H_4_REG  |
| SHA-224        | 224                                | SHA_H_O_REG ~ SHA_H_6_REG  |
| SHA-256        | 256                                | SHA_H_O_REG ~ SHA_H_7_REG  |
| SHA-384        | 384                                | SHA_H_O_REG ~ SHA_H_11_REG |
| SHA-512        | 512                                | SHA_H_O_REG ~ SHA_H_15_REG |
| SHA-512/224    | 224                                | SHA_H_O_REG ~ SHA_H_6_REG  |
| SHA-512/256    | 256                                | SHA_H_O_REG ~ SHA_H_7_REG  |
| SHA-512/ $t^2$ | $t$                                | SHA_H_O_REG ~ SHA_H_x_REG  |

<sup>1</sup> The message digest is stored in registers from most significant bits to the least significant bits, with the first word stored in register [SHA\\_H\\_O\\_REG](#) and the second word stored in register [SHA\\_H\\_1\\_REG](#)... For details, please see subsection [26.4.1.2](#).

<sup>2</sup> The registers used for SHA-512/ $t$  algorithm depend on the value of  $t$ .  $x+1$  indicates the number of 32-bit registers used to store  $t$  bits of message digest, so that  $x = \text{roundup}(t/32)-1$ .

1. For example:

- When  $t = 8$ , then  $x = 0$ , indicating that the 8-bit long message digest is stored in the most significant 8 bits of register [SHA\\_H\\_O\\_REG](#);
- When  $t = 32$ , then  $x = 0$ , indicating that the 32-bit long message digest is stored in register [SHA\\_H\\_O\\_REG](#);
- When  $t = 132$ , then  $x = 4$ , indicating that the 132-bit long message digest is stored in registers [SHA\\_H\\_O\\_REG](#), [SHA\\_H\\_1\\_REG](#), [SHA\\_H\\_2\\_REG](#), [SHA\\_H\\_3\\_REG](#), and [SHA\\_H\\_4\\_REG](#).

## 26.5 Interrupt

ESP32-P4's SHA accelerator can generate the following interrupt signal(s) that will be sent to the [Interrupt Matrix](#).

- SHA\_INTR

There are several internal interrupt sources from SHA that can generate the above interrupt signal(s). The interrupt sources from SHA are listed with their trigger conditions and the resulted interrupt signal(s) in [Table 26.5-1](#).

Table 26.5-1. SHA's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition   | Interrupt Signal |
|---------------------------|---|------------------|
| SHA_CALC_DONE_INT         | Completion of an message digest calculation in DMA-SHA mode | SHA_INTR         |

### Note:

- For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to [Chapter 11](#)

*Interrupt Matrix* > Section 11.2 *Interrupt Terminology in ESP32-P4*.

- Different from the standard interrupt register group, the interrupt register group of SHA only contains the INT\_ENA ([SHA\\_INT\\_ENA\\_REG](#)) and INT\_CLR ([SHA\\_INT\\_CLEAR\\_REG](#)) fields, and does not support users to read the INT\_RAW and INT\_ST fields.

## 26.6 Register Summary

The addresses in this section are relative to SHA accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Control/Configuration Registers</b> |  |         |        |
| <a href="#">SHA_MODE_REG</a>           | Configures SHA algorithm                                       | 0x0000  | R/W    |
| <a href="#">SHA_T_STRING_REG</a>       | Initial Hash Value calculation factor t_string (for SHA-512/t) | 0x0004  | R/W    |
| <a href="#">SHA_T_LENGTH_REG</a>       | Initial Hash Value calculation factor t_length (for SHA-512/t) | 0x0008  | R/W    |
| <a href="#">SHA_CONTINUE_REG</a>       | Continues SHA operation (only effective in Typical SHA mode)   | 0x0014  | WO     |
| <a href="#">SHA_DMA_START_REG</a>      | Starts the SHA accelerator for DMA-SHA operation               | 0x001C  | WO     |
| <a href="#">SHA_START_REG</a>          | Starts the SHA accelerator for Typical SHA operation           | 0x0010  | WO     |
| <a href="#">SHA_DMA_CONTINUE_REG</a>   | Continues SHA operation (only effective in DMA-SHA mode)       | 0x0020  | WO     |
| <a href="#">SHA_DMA_BLOCK_NUM_REG</a>  | Block number register (only effective in DMA-SHA mode)         | 0x000C  | R/W    |
| <b>Status Registers</b>                |  |         |        |
| <a href="#">SHA_BUSY_REG</a>           | Represents if SHA Accelerator is busy or not                   | 0x0018  | RO     |
| <b>Interrupt Registers</b>             |  |         |        |
| <a href="#">SHA_INT_CLEAR_REG</a>      | DMA-SHA interrupt clear register                               | 0x0024  | WO     |
| <a href="#">SHA_INT_ENA_REG</a>        | DMA-SHA interrupt enable register                              | 0x0028  | R/W    |
| <b>Data Registers</b>                  |  |         |        |
| <a href="#">SHA_H_0_REG</a>            | Hash value   | 0x0040  | R/W    |
| <a href="#">SHA_H_1_REG</a>            | Hash value   | 0x0044  | R/W    |
| <a href="#">SHA_H_2_REG</a>            | Hash value   | 0x0048  | R/W    |
| <a href="#">SHA_H_3_REG</a>            | Hash value   | 0x004C  | R/W    |
| <a href="#">SHA_H_4_REG</a>            | Hash value   | 0x0050  | R/W    |
| <a href="#">SHA_H_5_REG</a>            | Hash value   | 0x0054  | R/W    |
| <a href="#">SHA_H_6_REG</a>            | Hash value   | 0x0058  | R/W    |
| <a href="#">SHA_H_7_REG</a>            | Hash value   | 0x005C  | R/W    |
| <a href="#">SHA_H_8_REG</a>            | Hash value   | 0x0060  | R/W    |
| <a href="#">SHA_H_9_REG</a>            | Hash value   | 0x0064  | R/W    |
| <a href="#">SHA_H_10_REG</a>           | Hash value   | 0x0068  | R/W    |
| <a href="#">SHA_H_11_REG</a>           | Hash value   | 0x006C  | R/W    |
| <a href="#">SHA_H_12_REG</a>           | Hash value   | 0x0070  | R/W    |
| <a href="#">SHA_H_13_REG</a>           | Hash value   | 0x0074  | R/W    |
| <a href="#">SHA_H_14_REG</a>           | Hash value   | 0x0078  | R/W    |
| <a href="#">SHA_H_15_REG</a>           | Hash value   | 0x007C  | R/W    |
| <a href="#">SHA_M_0_REG</a>            | Message  | 0x0080  | R/W    |
| <a href="#">SHA_M_1_REG</a>            | Message  | 0x0084  | R/W    |
| <a href="#">SHA_M_2_REG</a>            | Message  | 0x0088  | R/W    |
| <a href="#">SHA_M_3_REG</a>            | Message  | 0x008C  | R/W    |
| <a href="#">SHA_M_4_REG</a>            | Message  | 0x0090  | R/W    |
| <a href="#">SHA_M_5_REG</a>            | Message  | 0x0094  | R/W    |

| Name                         | Description              | Address | Access |
|------------------------------|--------------------------|---------|--------|
| <a href="#">SHA_M_6_REG</a>  | Message                  | 0x0098  | R/W    |
| <a href="#">SHA_M_7_REG</a>  | Message                  | 0x009C  | R/W    |
| <a href="#">SHA_M_8_REG</a>  | Message                  | 0x00A0  | R/W    |
| <a href="#">SHA_M_9_REG</a>  | Message                  | 0x00A4  | R/W    |
| <a href="#">SHA_M_10_REG</a> | Message                  | 0x00A8  | R/W    |
| <a href="#">SHA_M_11_REG</a> | Message                  | 0x00AC  | R/W    |
| <a href="#">SHA_M_12_REG</a> | Message                  | 0x00B0  | R/W    |
| <a href="#">SHA_M_13_REG</a> | Message                  | 0x00B4  | R/W    |
| <a href="#">SHA_M_14_REG</a> | Message                  | 0x00B8  | R/W    |
| <a href="#">SHA_M_15_REG</a> | Message                  | 0x00BC  | R/W    |
| <a href="#">SHA_M_16_REG</a> | Message                  | 0x00C0  | R/W    |
| <a href="#">SHA_M_17_REG</a> | Message                  | 0x00C4  | R/W    |
| <a href="#">SHA_M_18_REG</a> | Message                  | 0x00C8  | R/W    |
| <a href="#">SHA_M_19_REG</a> | Message                  | 0x00CC  | R/W    |
| <a href="#">SHA_M_20_REG</a> | Message                  | 0x00D0  | R/W    |
| <a href="#">SHA_M_21_REG</a> | Message                  | 0x00D4  | R/W    |
| <a href="#">SHA_M_22_REG</a> | Message                  | 0x00D8  | R/W    |
| <a href="#">SHA_M_23_REG</a> | Message                  | 0x00DC  | R/W    |
| <a href="#">SHA_M_24_REG</a> | Message                  | 0x00E0  | R/W    |
| <a href="#">SHA_M_25_REG</a> | Message                  | 0x00E4  | R/W    |
| <a href="#">SHA_M_26_REG</a> | Message                  | 0x00E8  | R/W    |
| <a href="#">SHA_M_27_REG</a> | Message                  | 0x00EC  | R/W    |
| <a href="#">SHA_M_28_REG</a> | Message                  | 0x00F0  | R/W    |
| <a href="#">SHA_M_29_REG</a> | Message                  | 0x00F4  | R/W    |
| <a href="#">SHA_M_30_REG</a> | Message                  | 0x00F8  | R/W    |
| <a href="#">SHA_M_31_REG</a> | Message                  | 0x00FC  | R/W    |
| <b>Version Register</b>      |                          |         |        |
| <a href="#">SHA_DATE_REG</a> | Version control register | 0x002C  | R/W    |

## 26.7 Registers

The addresses in this section are relative to SHA accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 26.1. SHA\_MODE\_REG (0x0000)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |          |   |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------|---|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SHA_MODE |   |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 3        | 2 | 0     |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0      |   | Reset |  |

**SHA\_MODE** Configures the SHA algorithm.

- 0: SHA-1
  - 1: SHA-224
  - 2: SHA-256
  - 3: SHA-384
  - 4: SHA-512
  - 5: SHA-512/224
  - 6: SHA-512/256
  - 7: SHA-512/t
- (R/W)

**Register 26.2. SHA\_T\_STRING\_REG (0x0004)**

|              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|--------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| SHA_T_STRING |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x000000     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**SHA\_T\_STRING** Configures t\_string for calculating the initial Hash value for SHA-512/t. (R/W)

**Register 26.3. SHA\_T\_LENGTH\_REG (0x0008)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |   |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|---|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SHA_T_LENGTH |   |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7            | 6 | 0     |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0          |   | Reset |  |

**SHA\_T\_LENGTH** Configures t\_length for calculating the initial Hash value for SHA-512/t. (R/W)

Register 26.4. SHA\_DMA\_BLOCK\_NUM\_REG (0x000C)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |   |   |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|---|---|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SHA_DMA_BLOCK_NUM |   |   |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6                 | 5 | 0 |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0               |   |   |  |  |  | Reset |  |

**SHA\_DMA\_BLOCK\_NUM** Configures the DMA-SHA block number. (R/W)

Register 26.5. SHA\_START\_REG (0x0010)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_START |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**SHA\_START** Write 1 to start Typical SHA calculation. (WO)

Register 26.6. SHA\_CONTINUE\_REG (0x0014)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_CONTINUE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

**SHA\_CONTINUE** Write 1 to continue Typical SHA calculation. (WO)

Register 26.7. SHA\_BUSY\_REG (0x0018)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_BUSY_STATE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1              | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**SHA\_BUSY\_STATE** Represents the states of SHA accelerator.

0: idle

1: busy

(RO)



**Register 26.8. SHA\_DMA\_START\_REG (0x001C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_DMA_START |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1             | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 |

Reset

**SHA\_DMA\_START** Write 1 to start DMA-SHA calculation. (WO)**Register 26.9. SHA\_DMA\_CONTINUE\_REG (0x0020)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_DMA_CONTINUE |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0 |

Reset

**SHA\_DMA\_CONTINUE** Write 1 to continue DMA-SHA calculation. (WO)**Register 26.10. SHA\_INT\_CLEAR\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_CLEAR_INTERRUPT |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                   | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 |

Reset

**SHA\_CLEAR\_INTERRUPT** Write 1 to clear DMA-SHA interrupt. (WO)**Register 26.11. SHA\_INT\_ENA\_REG (0x0028)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SHA_INTERRUPT_ENA |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                 | 0 |

Reset

**SHA\_INTERRUPT\_ENA** Write 1 to enable DMA-SHA interrupt. (R/W)

(reserved)

SHA\_DATE

**SHA\_DATE** Version control register. (R/W)

## SHA\_H\_n

31

**SHA\_H\_***n* Represents the *n*th 32-bit piece of the Hash value. (R/W)

## SHA\_M\_n

31

**SHA\_M\_n** Represents the *n*th 32-bit piece of the message. (R/W)

## Chapter 27

# Digital Signature Algorithm (DSA)

## 27.1 Overview

The Digital Signature Algorithm (DSA) is used to verify the authenticity and integrity of a message using a cryptographic algorithm. This can be used to validate a device's identity to a server or to check the integrity of a message.

ESP32-P4 includes a Digital Signature Algorithm (DSA) module providing hardware acceleration of messages' signatures based on RSA. HMAC is used as the key derivation function (KDF) to output the DSA\_KEY key using a key stored in eFuse as the input key. Subsequently, the DSA module uses DSA\_KEY to decrypt the pre-encrypted parameters and calculate the signature. The whole process happens in hardware so that all the keys involved during the calculating process cannot be seen by users, guaranteeing the security of the operation.

## 27.2 Features

- RSA digital signatures with key length up to 4096 bits
- Encrypted private key data, only decryptable by the DSA module
- SHA-256 digest to protect private key data against tampering by an attacker

## 27.3 Functional Description

### 27.3.1 Overview

The DSA peripheral calculates RSA signatures as  $Z = X^Y \bmod M$ , where  $Z$  is the signature,  $X$  is the input message, and  $Y$  and  $M$  are the RSA private key parameters.

Private key parameters are stored in flash as ciphertext. They are decrypted using a key (*DSA\_KEY*) which can only be calculated by the DSA peripheral via the HMAC peripheral. The required inputs (*HMAC\_KEY*) to generate the key are only stored in eFuse and can only be accessed by the HMAC peripheral. That is to say, the DSA peripheral hardware can decrypt the private key, and the private key in plaintext is never accessed by the software. For more detailed information about eFuse and HMAC peripherals, please refer to [Chapter 7 eFuse Controller](#) and [Chapter 24 HMAC Accelerator \(HMAC\)](#).

The input message  $X$  will be sent directly to the DSA peripheral by the software each time a signature is needed. After the RSA signature operation, the signature  $Z$  is read back by the software.

For better understanding, we define some symbols and functions here, which are only applicable to this chapter:

- $1^s$ : A bit string consisting of  $s$  bits with the value of “1”.
- $[x]_s$ : A bit string of  $s$  bits, in which  $s$  is an integer multiple of 8 bits. If  $x$  is a number ( $x < 2^s$ ), it is represented in little-endian byte order in the bit string.  $x$  may be a variable such as  $[Y]_{4096}$  or a hexadecimal constant such as  $[0x0C]_8$ . If necessary, the value  $[x]_t$  can be right-padded with  $(s - t)$  number of zeros to reach  $s$  bits in length, and finally get  $[x]_s$ . For example,  $[0x05]_8 = 00000101$ ,  $[0x05]_{16} = 0000010100000000$ ,  $[0x0005]_{16} = 0000000000000101$ ,  $[0x13]_8 = 00010011$ ,  $[0x13]_{16} = 0001001100000000$ ,  $[0x0013]_{16} = 0000000000010011$ .
- $||$ : A bit string concatenation operator for joining multiple-bit strings into a longer bit string.

## 27.3.2 Private Key Operands

Private key operands  $Y$  (private key exponent) and  $M$  (key modulus) are generated by the user. They have a particular RSA key length (up to 4096 bits). Two additional private key operands are needed:  $\bar{r}$  and  $M'$ . These two operands are derived from  $Y$  and  $M$ .

Operands  $Y$ ,  $M$ ,  $\bar{r}$ , and  $M'$  are encrypted by the user along with an authentication digest and stored as a single ciphertext  $C$ .  $C$  is input to the DSA peripheral in this encrypted format, decrypted by the hardware, and then used for RSA signature calculation. A detailed description of how to generate  $C$  is provided in Section [27.3.3](#).

The DSA peripheral supports RSA signature calculation  $Z = X^Y \bmod M$ , in which the length of operands should be  $N = 32 \times x$  where  $x \in \{1, 2, 3, \dots, 128\}$ . The bit lengths of arguments  $Z$ ,  $X$ ,  $Y$ ,  $M$ , and  $\bar{r}$  should be an arbitrary value in  $N$ , and all of them in a calculation must be of the same length, while the bit length of  $M'$  should always be 32. For more detailed information about RSA calculation, please refer to Section [25.3.2 Large-Number Modular Exponentiation](#) in Chapter [25 RSA Accelerator \(RSA\)](#).

## 27.3.3 Software Prerequisites

If you want to use the DSA module, the software needs a series of preparations, as shown in Figure [27.3-1](#). The left side lists preparations required by the software before the hardware starts the RSA signature calculation, while the right side lists the hardware workflow during the entire calculation procedure.

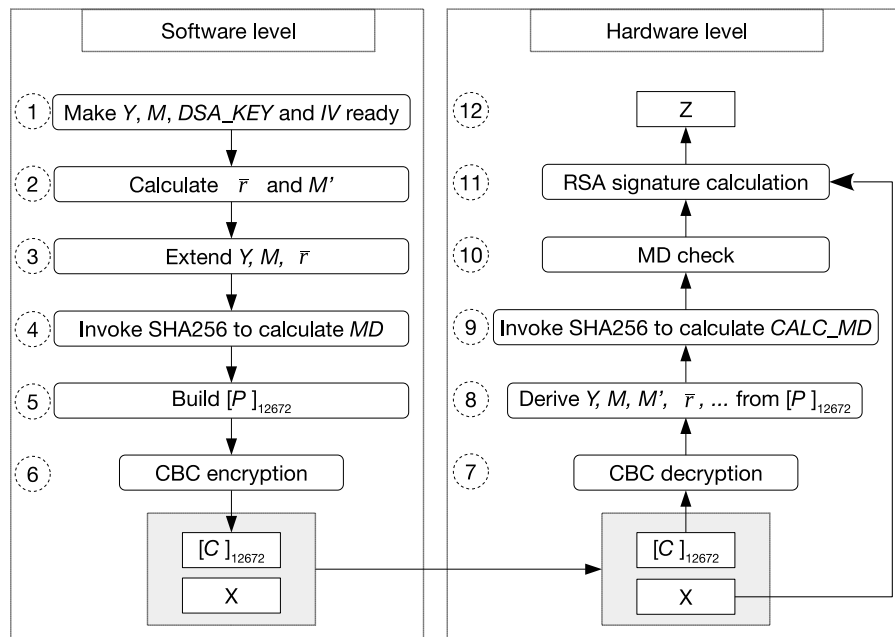


Figure 27.3-1. Software Preparations and Hardware Working Process

**Note:**

1. The software preparation (left side in Figure 27.3-1) is a one-time operation before any signature is calculated, while the hardware calculation (right side in Figure 27.3-1) repeats for every signature calculation.
2. Software preparation requires configuring the clock reset. For more information, please refer to Chapter 9 [Reset and Clock](#).

Users need to follow the steps shown in the left part of Figure 27.3-1 to calculate  $C$ . Detailed instructions are as follows:

- **Step 1:** Prepare operands  $Y$  and  $M$  whose lengths should meet the requirements in Section 27.3.2. Define  $[L]_{32} = \frac{N}{32} - 1$  (i.e., for RSA 4096,  $[L]_{32} = [0x80-1]_{32}$ ). Prepare  $[HMAC\_KEY]_{256}$  and calculate  $[DSA\_KEY]_{256}$  based on  $DSA\_KEY = \text{HMAC-SHA256}([HMAC\_KEY]_{256}, 1^{256})$ . Generate a random  $[IV]_{128}$  which should meet the requirements of the AES-CBC block encryption algorithm. For more information on AES, please refer to Chapter 22 [AES Accelerator \(AES\)](#).
- **Step 2:** Calculate  $\bar{r}$  and  $M'$  based on  $M$ .
- **Step 3:** Extend  $Y$ ,  $M$ , and  $\bar{r}$  in order to get  $[Y]_{4096}$ ,  $[M]_{4096}$ , and  $[\bar{r}]_{4096}$ , respectively. This step is only required for  $Y$ ,  $M$ , and  $\bar{r}$  whose length are less than 4096 bits, since their largest length are 4096 bits.
- **Step 4:** Calculate MD authentication code using the SHA-256:  
 $[MD]_{256} = \text{SHA256}([Y]_{4096} || [M]_{4096} || [\bar{r}]_{4096} || [M']_{32} || [L]_{32} || [IV]_{128})$
- **Step 5:** Build  $[P]_{12672} = ([Y]_{4096} || [M]_{4096} || [\bar{r}]_{4096} || [Box]_{384})$ , where  $[Box]_{384} = ([MD]_{256} || [M']_{32} || [L]_{32} || [\beta]_{64})$  and  $[\beta]_{64}$  is a PKCS#7 padding value, i.e., a  $[0x0808080808080808]_{64}$  string composed of 8 bytes (0x80). The purpose of  $[\beta]_{64}$  is to make the bit length of  $P$  a multiple of 128.
- **Step 6:** Calculate  $C = [C]_{12672} = \text{AES-CBC-ENC}([P]_{12672}, [DSA\_KEY]_{256}, [IV]_{128})$ , where  $C$  is the ciphertext with a length of 1200 bytes.  $C$  can also be calculated as  $C = [C]_{12672} = ([\hat{Y}]_{4096} || [\hat{M}]_{4096} || [\hat{\bar{r}}]_{4096} || [\hat{Box}]_{384})$ , where  $[\hat{Y}]_{4096}$ ,  $[\hat{M}]_{4096}$ ,  $[\hat{\bar{r}}]_{4096}$ ,  $[\hat{Box}]_{384}$  are the four sub-parameters

of  $C$ , and correspond to the ciphertext of  $[Y]_{4096}$ ,  $[M]_{4096}$ ,  $[\bar{r}]_{4096}$ ,  $[Box]_{384}$  respectively.

### 27.3.4 DSA Operation at the Hardware Level

The hardware operation is triggered each time a digital signature needs to be calculated. The inputs are the pre-generated private key ciphertext  $C$ , a unique message  $X$ , and  $IV$ .

The DSA operation at the hardware level can be divided into the following three stages:

#### 1. Decryption: Step 7 and 8 in Figure 27.3-1

The decryption process is the inverse of Step 6 in Figure 27.3-1. The DSA module will call the AES accelerator to decrypt  $C$  in CBC block mode and get the resulting plaintext. The decryption process can be represented by  $P = \text{AES-CBC-DEC}(C, DSA\_KEY, IV)$ , where  $IV$  (i.e.,  $[IV]_{128}$ ) is defined by the user.  $[DSA\_KEY]_{256}$  is provided by the HMAC module, derived from  $HMAC\_KEY$  stored in eFuse.  $[DSA\_KEY]_{256}$ , as well as  $[HMAC\_KEY]_{256}$  are not readable by users. For more information, please refer to Chapter 24 [HMAC Accelerator \(HMAC\)](#).

With  $P$ , the DSA module can derive  $[Y]_{4096}$ ,  $[M]_{4096}$ ,  $[\bar{r}]_{4096}$ ,  $[M']_{32}$ ,  $[L]_{32}$ , MD authentication code, and the padding value  $[\beta]_{64}$ . This process is the inverse of Step 5.

#### 2. Check: Step 9 and 10 in Figure 27.3-1

The DSA module will perform two checks: MD check and padding check. The padding check is not shown in Figure 27.3-1, as it happens at the same time as the MD check.

- MD check: The DSA module calls SHA-256 to calculate the hash value  $[CALC\_MD]_{256}$  ( $[CALC\_MD]_{256}$  is calculated the same way and with same parameters as  $[MD]_{256}$ , see step 4). Then,  $[CALC\_MD]_{256}$  is compared against the MD authentication code  $[MD]_{256}$  from step 4. Only when the two match does the MD check pass.
- Padding check: The DSA module checks if  $[\beta]_{64}$  complies with the aforementioned PKCS#7 format. Only when  $[\beta]_{64}$  complies with the format does the padding check pass.

The DSA module will only perform subsequent operations if MD check passes. If the padding check fails, a warning is generated, but it does not affect the subsequent operations.

#### 3. Calculation: Step 11 and 12 in Figure 27.3-1

The DSA module treats  $X$  (input by the user) and  $Y$ ,  $M$ ,  $\bar{r}$  (decrypted in step 8) as big numbers. With  $M'$ , all operands to perform  $X^Y \bmod M$  are in place. The operand length is defined by  $L$  only. The DSA module will calculate the signed result  $Z$  by calling RSA to perform  $Z = X^Y \bmod M$ .

### 27.3.5 DSA Operation at the Software Level

The software steps below should be followed each time a digital signature needs to be calculated. The inputs are the pre-generated private key ciphertext  $C$ , a unique message  $X$ , and  $IV$ . These software steps trigger the hardware steps described in Section 27.3.4.

We assume that the software has called the HMAC peripheral and the HMAC peripheral has calculated  $DSA\_KEY$  based on  $HMAC\_KEY$ .

1. **Prerequisites:** Prepare operands  $C$ ,  $X$ ,  $IV$  according to Section 27.3.3.
2. **Activate the DSA peripheral:** Write 1 to [DSA\\_SET\\_START\\_REG](#).

3. **Check if  $DSA\_KEY$  is ready:** Poll [DSA\\_QUERY\\_BUSY\\_REG](#) until the software reads 0.

If the software does not read 0 in [DSA\\_QUERY\\_BUSY\\_REG](#) after approximately 1 ms, it indicates a problem with HMAC initialization. In such a case, the software can read register [DSA\\_QUERY\\_KEY\\_WRONG\\_REG](#) to get more information:

- If the software reads 0 in [DSA\\_QUERY\\_KEY\\_WRONG\\_REG](#), it indicates that the HMAC peripheral has not been called.
- If the software reads any value from 1 to 15 in [DSA\\_QUERY\\_KEY\\_WRONG\\_REG](#), it indicates that HMAC was called, but the DSA module did not successfully get the  $DSA\_KEY$  value from the HMAC peripheral. This may indicate that the HMAC operation has been interrupted due to a software concurrency problem.

4. **Configure register:** Write the content in the  $IV$  block to register [DSA\\_IV\\_m\\_REG](#) ( $m$ : 0 ~ 3). For more information on the  $IV$  block, please refer to Chapter [22 AES Accelerator \(AES\)](#).
5. **Write  $X$  to memory block [DSA\\_X\\_MEM](#):** Write  $X_i$  ( $i \in \{0, 1, \dots, n-1\}$ ), where  $n = \frac{N}{32}$ , to memory block [DSA\\_X\\_MEM](#) whose capacity is 96 words. Each word can store one base- $b$  digit. The memory block uses the little endian format for storage, i.e., the least significant digit of the operand is in the lowest address. Words in [DSA\\_X\\_MEM](#) block after the configured length of  $X$  ( $N$  bits, as described in Section [27.3.2](#)), are ignored.
6. **Write  $C$  to corresponding memory blocks:** Write the four sub-parameters of  $C$  to corresponding memory blocks:

- Write  $\widehat{Y}_i$  ( $i \in \{0, 1, \dots, 127\}$ ) to [DSA\\_Y\\_MEM](#).
- Write  $\widehat{M}_i$  ( $i \in \{0, 1, \dots, 127\}$ ) to [DSA\\_M\\_MEM](#).
- Write  $\widehat{r}_i$  ( $i \in \{0, 1, \dots, 127\}$ ) to [DSA\\_RB\\_MEM](#).
- write  $\widehat{Box}_i$  ( $i \in \{0, 1, \dots, 11\}$ ) to [DSA\\_BOX\\_MEM](#).

The capacity of [DSA\\_Y\\_MEM](#), [DSA\\_M\\_MEM](#), and [DSA\\_RB\\_MEM](#) is 128 words, whereas the capacity of [DSA\\_BOX\\_MEM](#) is only 12 words. Each word can store one base- $b$  digit. The memory blocks use the little endian format for storage, i.e., the least significant digit of the operand is in the lowest address.

7. **Start DSA operation:** Write 1 to register [DSA\\_SET\\_ME\\_REG](#).
8. **Wait for the operation to be completed:** Poll register [DSA\\_QUERY\\_BUSY\\_REG](#) until the software reads 0.
9. **Query check result:** Read register [DSA\\_QUERY\\_CHECK\\_REG](#) and conduct subsequent operations as illustrated below based on the return value:
- If the value is 0, it indicates that both the padding check and MD check pass. Users can continue to get the signed result  $Z$ .
  - If the value is 1, it indicates that the padding check passes but MD check fails. The signed result  $Z$  is invalid. The operation will resume directly from Step 11.
  - If the value is 2, it indicates that the padding check fails but the MD check passes. Users can continue to get the signed result  $Z$ . But please note that the data does not comply with the aforementioned PKCS#7 padding format, which may not be what you want.

- If the value is 3, it indicates that both the padding check and MD check fail. In this case, some fatal errors have occurred and the signed result  $Z$  is invalid. The operation will resume directly from Step 11.
10. **Read the signed result:** Read the signed result  $Z_i$  ( $i \in \{0, 1, \dots, n - 1\}$ ), where  $n = \frac{N}{32}$ , from memory block [DSA\\_Z\\_MEM](#). The memory block stores  $Z$  in little-endian byte order.
  11. **Exit the operation:** Write 1 to [DSA\\_SET\\_FINISH\\_REG](#), and then poll [DSA\\_QUERY\\_BUSY\\_REG](#) until the software reads 0.

After the operation, all the input/output registers and memory blocks are cleared.



## 27.4 Memory Summary

The addresses in this section are relative to the Digital Signature Algorithm base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

| Name        | Description            | Size (byte) | Starting Address | Ending Address | Access |
|-------------|------------------------|-------------|------------------|----------------|--------|
| DSA_Y_MEM   | Memory block Y         | 512         | 0x0000           | 0x01FF         | WO     |
| DSA_M_MEM   | Memory block M         | 512         | 0x0200           | 0x03FF         | WO     |
| DSA_RB_MEM  | Memory block $\bar{r}$ | 512         | 0x0400           | 0x05FF         | WO     |
| DSA_BOX_MEM | Memory block Box       | 48          | 0x0600           | 0x062F         | WO     |
| DSA_X_MEM   | Memory block X         | 512         | 0x0800           | 0x09FF         | WO     |
| DSA_Z_MEM   | Memory block Z         | 512         | 0x0A00           | 0x0BFF         | RO     |

## 27.5 Register Summary

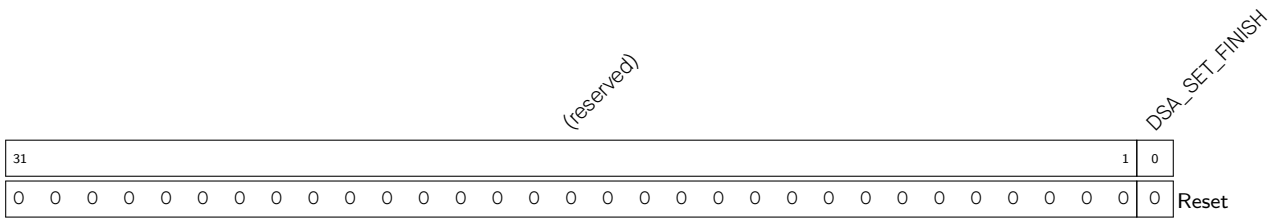
The addresses in this section are relative to Digital Signature Algorithm base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                    | Description                                       | Address | Access |
|---|---|---------|--------|
| <b>Configuration Registers</b>          |   |         |        |
| <a href="#">DSA_IV_0_REG</a>            | IV block data                                     | 0x0630  | WO     |
| <a href="#">DSA_IV_1_REG</a>            | IV block data                                     | 0x0634  | WO     |
| <a href="#">DSA_IV_2_REG</a>            | IV block data                                     | 0x0638  | WO     |
| <a href="#">DSA_IV_3_REG</a>            | IV block data                                     | 0x063C  | WO     |
| <b>Status/Control Registers</b>         |   |         |        |
| <a href="#">DSA_SET_START_REG</a>       | Activates the DSA module                          | 0x0E00  | WO     |
| <a href="#">DSA_SET_ME_REG</a>          | Starts DSA operation                              | 0x0E04  | WO     |
| <a href="#">DSA_SET_FINISH_REG</a>      | Ends DSA operation                                | 0x0E08  | WO     |
| <a href="#">DSA_QUERY_BUSY_REG</a>      | Status of the DSA module                          | 0x0E0C  | RO     |
| <a href="#">DSA_QUERY_KEY_WRONG_REG</a> | Checks the reason why <i>DSA_KEY</i> is not ready | 0x0E10  | RO     |
| <a href="#">DSA_QUERY_CHECK_REG</a>     | Queries DSA check result                          | 0x0E14  | RO     |
| <b>Version control register</b>         |   |         |        |
| <a href="#">DSA_DATE_REG</a>            | Version control register                          | 0x0E20  | W/R    |



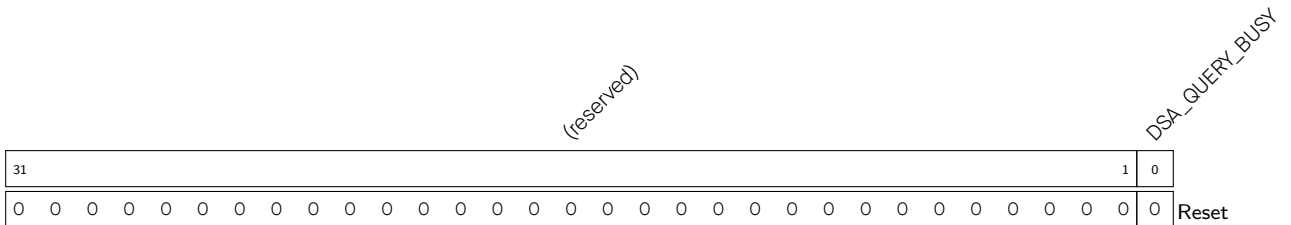
### Register 27.4. DSA\_SET\_FINISH\_REG (0x0E08)



**DSA\_SET\_FINISH** Configures whether to end the DSA operation.

- 0: No effect  
1: End the DSA operation  
(WO)

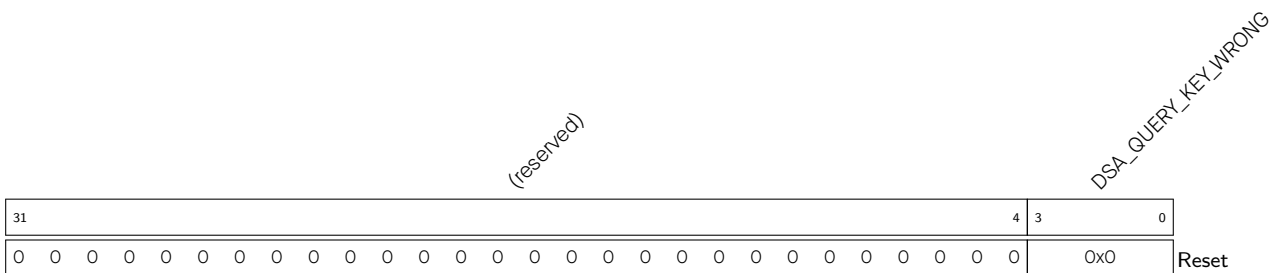
### Register 27.5. DSA\_QUERY\_BUSY\_REG (0x0E0C)



**DSA\_QUERY\_BUSY** Represents whether the DSA module is idle.

- 0: The DSA module is idle.  
1: The DSA module is busy.  
(RO)

### Register 27.6. DSA\_QUERY\_KEY\_WRONG\_REG (0x0E10)



**DSA\_QUERY\_KEY\_WRONG** Represents the specific problem with HMAC initialization.

- 0: HMAC is not called.  
1-15: HMAC was activated, but the DSA peripheral did not successfully receive the *DSA\_KEY* from the HMAC peripheral.  
(RO)

(reserved)

DSA\_PADDING\_BAD  
DSA\_MD\_ERROR

(RO)

(RO)

(reserved)

DSA\_DATE

Reset

## Chapter 28

# Elliptic Curve Digital Signature Algorithm (ECDSA)

## 28.1 Introduction

In cryptography, the Elliptic Curve Digital Signature Algorithm (ECDSA) offers a variant of the Digital Signature Algorithm (DSA) which uses elliptic-curve cryptography.

ESP32-P4's ECDSA accelerator provides a secure and efficient environment for computing ECDSA signatures. It offers fast computations while ensuring the confidentiality of the signing process to prevent information leakage. This makes it a valuable tool for applications that require high-speed cryptographic operations with strong security guarantees. By using the ECDSA accelerator, users can be confident that their data is being protected without sacrificing performance.

## 28.2 Features

ESP32-P4's ECDSA accelerator supports:

- Digital signature verification
- Two different elliptic curves, namely P-192 and P-256, defined in [FIPS 186-3 Spec](#)
- Two hash algorithms for message hash in the ECDSA operation, namely SHA-224 and SHA-256, defined in [FIPS PUB 180-4 Spec](#)
- Dynamic access permission in different operation statuses to ensure information security

## 28.3 ECDSA Basics

### 28.3.1 Domain Parameters

ECDSA uses parameters that define the elliptic curve over a finite field, as well as the generator point and the order of the base point. These parameters are usually referred to as domain parameters, and they are required for key generation, signature generation, and signature verification.

The domain parameters used in ECDSA consist of the followings:

- The elliptic curve domain parameters, which include:
  - The prime modulus  $p$ , which specifies the size of the finite field over which the elliptic curve is defined.
  - The base point  $G$  on the curve, which can be used to generate public keys.

- The order  $n$  of the base point, which is the number of points on the curve that can be generated by repeatedly adding  $G$  to itself.
- The parameters for the hash function, which include:
  - The hash algorithm used to generate a fixed-length hash value from the message being signed.
  - The length of the hash value, which determines the size of the signature.

Together, these parameters define the ECDSA domain.

### 28.3.2 Key Generation

The process of key generation in ECDSA is described below:

1. Select an elliptic curve domain by defining:
  - the prime modulus  $p$
  - the coefficients  $a$  and  $b$
  - the base point  $G$  and its order  $n$
2. Generate a private key:
  - A private key  $d$  is a randomly chosen integer between 1 and  $n-1$ . It is essential to use a secure [Random Number Generator \(RNG\)](#) to ensure that the private key is truly random and cannot be predicted or reproduced.
  - The private key is used for signature generation. This key must be kept secret and secure.
3. Compute the public key:
  - The public key  $Q$  is calculated as  $Q = dG$ .
4. Export the public key:
  - The public key  $Q$  is typically represented as a pair of coordinates  $(Qx, Qy)$  that can be shared with others.

### 28.3.3 Signature Generation

The ECDSA signature generation process is described below:

1. Select a message  $m$  to be signed.
2. Calculate the hash of the message  $e$ :  $e$  is equal to HASH ( $m$ ), where HASH is a cryptographic hash function, such as SHA-256.
3. Compute the digest of the message hash  $z$ : Let  $z$  be the  $L_n$  leftmost bits of  $e$ , where  $L_n$  is the bit length of the base point order  $n$ .
4. Select a random number  $k$ , which is chosen between 1 and  $n-1$ , where  $n$  is the order of the base point on the elliptic curve.
5. Compute the signature: The signature is calculated as follows:
  - (a) Compute the point  $(x, y) = kG$

- (b) Calculate  $r = x \bmod n$ . If  $r$  is equal to zero, return to the previous step and select a new random value of  $k$ .
  - (c) Calculate  $s = k^{-1} * (z + d * r) \bmod n$ . If  $s$  is equal to zero, return to step 4 and select a new random value of  $k$ .
  - (d) The signature is the pair  $(r, s)$ .
6. Send the message  $m$  and signature  $(r, s)$  to the recipient.

### 28.3.4 Signature Verification

The recipient can then use the public key associated with the private key used for signature generation to verify the signature. The verification process involves checking that the signature was generated using the correct private key and that the signature is valid for the given message.

The ECDSA signature verification process is described below:

1. Obtain public key  $Q$  and receive the message  $m$  and signature  $(r, s)$ .
2. Calculate the hash of the message  $e$ :  $e$  is equal to HASH ( $m$ ), where HASH is a cryptographic hash function, such as SHA-256.
3. Compute the digest of the message  $z$ : Let  $z$  be the  $L_n$  leftmost bits of  $e$ , where  $L_n$  is the bit length of the base point order  $n$ .
4. Verify the signature: The signature is verified as follows:
  - (a) Verify that  $r$  and  $s$  are integers between 1 and  $n-1$ , where  $n$  is the order of the base point on the elliptic curve. If either  $r$  or  $s$  is outside of this range, the signature is invalid.
  - (b) Calculate  $u_1 = z * s^{-1} \bmod n$  and  $u_2 = r * s^{-1} \bmod n$ .
  - (c) Calculate the point  $(x_1, y_1) = u_1 * G + u_2 * Q$ , where  $G$  is the base point on the elliptic curve, and  $Q$  is the public key associated with the private key used for signature generation.
  - (d) Verify that  $r = x_1 \bmod n$ . If  $r$  is not equal to  $x_1 \bmod n$ , the signature is invalid.
5. Accept or reject the signature: If the signature is valid, the recipient can be confident that the message was not tampered with and that it came from the expected sender, thus can accept the message as authentic. Otherwise, the recipient rejects the message as invalid.

## 28.4 Functional Description

This section describes the details of ESP32-P4's ECDSA accelerator.

### 28.4.1 ECDSA Working Modes

The ECDSA accelerator integrated in the ESP32-P4 supports Signature Verification mode.

Users can select the elliptic curves used by configuring the [ECDSA\\_ECC\\_CURVE](#) according to Table [28.4-1](#).



Table 28.4-1. ECDSA Elliptic Curves Selection

| ECDSA_ECC_CURVE | Elliptic Curve |
|-----------------|----------------|
| 0               | P-192          |
| 1               | P-256          |

Users can select the SHA algorithms for message hash by configuring the [ECDSA\\_SHA\\_MODE](#) according to Table 28.4-2.

Table 28.4-2. ECDSA SHA Algorithm

| ECDSA_SHA_MODE | SHA Algorithm |
|----------------|---------------|
| 1              | SHA-224       |
| 2              | SHA-256       |
| Others         | Invalid       |

Additionally, users can check the working status of the ECDSA accelerator by inquiring the [ECDSA\\_STATE\\_REG](#) register and comparing the return value against the Table 28.4-3 below.

Table 28.4-3. ECDSA Working Status

| ECDSA_STATE_REG | Status   | Description  |
|-----------------|----------|--|
| 0               | IDLE     | Idle or completed operation. Corresponding to IDLE Stage.                        |
| 1               | LOAD     | Waiting for users to load information into ECDSA. Corresponding to LOAD Stage.   |
| 2               | Reserved | –  |
| 3               | BUSY     | In the middle of a hardware operation. Corresponding to PREP, PROC & POST Stage. |

## 28.4.2 Data and Data Block

ESP32-P4's ECDSA accelerator operates on data of 256 or 512 bits. This data ( $D[255 : 0]$ ) can be divided into 32-bit data blocks.

Take 256-bit long data as an example,  $D[n][31 : 0]$  ( $n = 0, 1, \dots, 7$ ). Data blocks with the smaller serial number correspond to the lower binary bits. To be specific:

$$D[255 : 0] = D[7][31 : 0], D[6][31 : 0], D[5][31 : 0], D[4][31 : 0], D[3][31 : 0], D[2][31 : 0], D[1][31 : 0], D[0][31 : 0]$$

### 28.4.2.1 Writing Data

Writing data means writing data to an ECDSA memory block and using this data as the input to the ECDSA algorithm. To be specific, writing data to an ECDSA memory block means writing  $D[n][31 : 0]$  to the “starting address of this ECDSA memory block +  $4 \times n$ ” For a 256-bit long data example:

- write  $D[0]$  to “starting address”
- write  $D[1]$  to “starting address + 4”

- ...
- write  $D[7]$  to “starting address + 28”

**Note:**

When the data size of 192 bits is used, you need to append 0 after 192 bits of data and write 256 bits of data.

### 28.4.2.2 Reading Data

Reading data means reading data from the starting address of an ECDSA memory block and using this data as the output from the ECDSA algorithm. To be specific, reading data from an ECDSA memory block means reading  $D[n][31 : 0]$  from the “starting address of this ECDSA memory block +  $4 \times n$ ”. For a 256-bit long data example:

- read  $D[0]$  from “starting address”
- read  $D[1]$  from “starting address + 4”
- ...
- read  $D[7]$  from “starting address + 28”

**Note:**

When the data size of 192 bits is used, only use the low 192 bits (6 blocks) of data.

### 28.4.2.3 Padding the Message

The SHA accelerator can only process message blocks of 512 bits. Thus, all the messages should be padded to a multiple of 512 bits before the hash operation.

Suppose that the length of the message  $M$  is  $L_M$  bits. Then  $M$  shall be padded as introduced below:

1. First, append the bit “1” to the end of the message;
2. Second, append  $L_A$  bits of zeros, where  $L_A$  is the smallest, non-negative solution to the equation  $L_M + 1 + L_A \equiv 448 \pmod{512}$ ;
3. Last, append the 64-bit block of value equal to the number  $L_M$  expressed using a binary representation.

For more details, please refer to [FIPS PUB 180-4 Spec](#) > Section “Padding the Message”.

### 28.4.2.4 Parsing the Message

The message and its padding must be parsed into  $N$  512-bit message blocks:  $M^{(1)}, M^{(2)}, \dots, M^{(N)}$ .

**Note:**

1. For more details about “parsing the message”, please refer to [FIPS PUB 180-4 Spec](#) > Section “Parsing the Message”.
2. For more information on “message block”, please refer to [FIPS PUB 180-4 Spec](#) > Section “Glossary of Terms and Acronyms”.

### 28.4.3 Security Features

To ensure the security of the ECDSA operation process, the ECDSA accelerator implements a variety of security functions.

#### 28.4.3.1 Dynamic Access Permission

ESP32-P4's ECDSA accelerator has implemented a dynamic access permission mechanism to prevent any possibility of key theft by tampering with the configuration or accessing the data during the operation.

By implementing this dynamic access permission mechanism, the accesses for ECDSA registers are designed to vary in different statuses. For example, [ECDSA\\_CONF\\_REG](#) is only available for reading and writing when the accelerator is in the IDLE status. In this way, the configuration information is protected from reading or writing when the accelerator is in other statuses, such as LOAD and BUSY. For details about all ECDSA working statuses, please refer to Table [28.4-3](#).

For detailed information on the dynamic access permission of each ECDSA register, please refer to Section [Register Summary](#).

#### 28.4.3.2 Hardware Occupation

During the ECDSA operation, the following hardware modules will be occupied by ESP32-P4's ECDSA accelerator:

- SHA Accelerator
- RSA Accelerator
- ECC Accelerator

Among them, the SHA accelerator will be released when the [ECDSA\\_SHA\\_RELEASE\\_INT](#) is triggered. While, the RSA accelerator and the ECC accelerator will be occupied during the whole ECDSA operation.

**Note:**

Hardware occupation is a mechanism to protect multiplexed modules and storage space. When a module is hardware occupied, the user will fail to:

- read or write data to the module's registers or memories.
- disable the module clock.
- reset the module.

At the end of the hardware occupation, the occupied module will be automatically reset. In addition, when the user performs a software reset to the master module, all the occupied modules will be reset at the same time.

## 28.5 Programming Procedures

### 28.5.1 ECDSA Process

The overall ECDSA process consists of the following five stages.

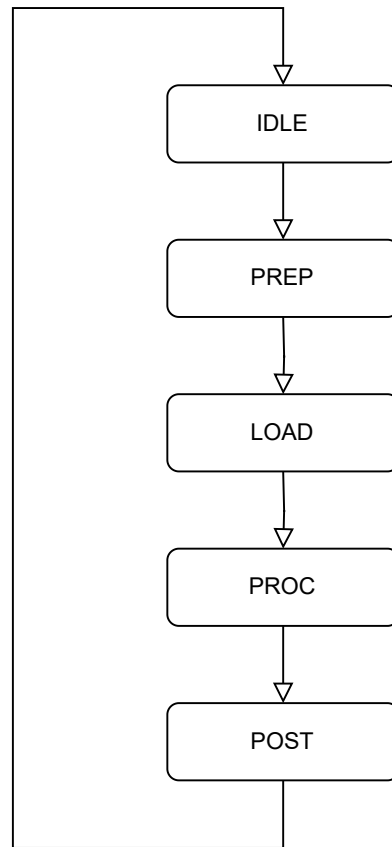


Figure 28.5-1. ECDSA Process

The detailed programming procedures of each stage are described in the following sections.

### 28.5.1.1 IDLE Stage

In the IDLE stage:

1. Configure the static parameters including eFuse bits ECDSA\_KEY, i.e., the value of private key  $d$  in ECDSA. To correctly configure the key value in eFuse, user need to write the key value in KEY $n$  ( $n = 0 \sim 5$ ), and set the corresponding EFUSE\_KEY\_PURPOSE\_ $n$  as ECDSA\_KEY. Please refer to Chapter 7 [eFuse Controller](#) for more detailed configuration steps.
2. Configure the configuration register, including the following fields:
  - (a) [ECDSA\\_ECC\\_CURVE](#): Choose the elliptic curve of the ECDSA accelerator.
  - (b) [ECDSA\\_SOFTWARE\\_SET\\_Z](#): Choose to use direct input  $z$ .
3. Configure the register field [ECDSA\\_START](#) to enter the PREP stage.

### 28.5.1.2 PREP Stage

In the PREP stage, the [ECDSA\\_STATE\\_REG](#) is BUSY, and the ECDSA accelerator performs preparation.

Wait till the PREP stage to end by polling [ECDSA\\_BUSY](#) until it is not BUSY. Then the ECDSA accelerator will automatically enter the LOAD stage.

### 28.5.1.3 LOAD Stage

In the LOAD stage:

1. Provide input  $z$  into the ECDSA accelerator using one of the following options:
  - Direct input  $z$ : write  $z$  to [ECDSA\\_Z\\_MEM](#).
  - ECDSA-SHA interface: generate  $z$  from the message. For details, please refer to Section [28.5.1.6](#).
2. Provide signature and public key required by signature verification:
  - (a) write signature  $(r, s)$  to [ECDSA\\_R\\_MEM](#) and [ECDSA\\_S\\_MEM](#).
  - (b) write public key  $(Qx, Qy)$  to [ECDSA\\_QX\\_MEM](#) and [ECDSA\\_QY\\_MEM](#).
3. Write 1 to [ECDSA\\_LOAD\\_DONE](#), indicating the configuration is done. Then the accelerator will automatically enter the PROC stage.

### 28.5.1.4 PROC Stage

In the PROC stage, the [ECDSA\\_STATE\\_REG](#) is BUSY, and the ECDSA accelerator performs ECDSA signature verification.

Wait till the PROC stage to end by polling [ECDSA\\_BUSY](#) until it is not BUSY. Then the ECDSA accelerator will automatically enter the POST stage.

### 28.5.1.5 POST Stage

In the POST stage, the [ECDSA\\_STATE\\_REG](#) is BUSY, and the ECDSA accelerator performs some wrap-up work of ECDSA operation.

Wait till the POST stage to end by polling [ECDSA\\_BUSY](#) until it is not BUSY. Then the ECDSA accelerator will automatically return to the IDLE stage.

### 28.5.1.6 ECDSA SHA Interface

ESP32-P4's ECDSA accelerator can automatically executes hash operation and generates  $z$  based on a direct input message.

For message hash, ECDSA accelerator supports SHA algorithms SHA-224 (only valid when P-192 is selected as the elliptic curve) and SHA-256.

To use the ECDSA SHA interface, complete the following steps:

1. Pad the message by following the steps described in Section [28.4.2.3](#).
2. Parse the message and its padding into message blocks. See details in Section [28.4.2.4](#).
3. Process the current message block.
  - Write the current message block into [ECDSA\\_MEM\\_M](#).
4. Start the ECDSA SHA interface<sup>1</sup>.
  - If this is the first time to execute this step, write 1 to [ECDSA\\_SHA\\_START](#) to start the ECDSA SHA interface;

- If this is not the first time to execute this step<sup>2</sup>, write 1 to [ECDSA\\_SHA\\_CONTINUE](#) to continue the operation.
5. Check the progress of the current message block processing by polling.
    - Poll register [ECDSA\\_SHA\\_BUSY](#) until it's IDLE, indicating the interface has completed the operation for the current message block.
  6. Process the next message block:
    - If yes, go back to Step 3.
    - If no more message block, exit.

**Note:**

1. In this step, the software can also write the next message block (to be processed) in register [ECDSA\\_MEM\\_M](#), if any, while the interface starts SHA operation, to save time.
2. You are resuming the ECDSA SHA interface with the previously paused operation.

## 28.5.2 Clocks and Resets

ESP32-P4's ECDSA accelerator has one clock module and one reset module. It is activated by setting the [HP\\_SYS\\_CLKRST\\_REG\\_CRYPT0\\_ECDSA\\_CLK\\_EN](#) bit in the [HP\\_SYS\\_CLKRST\\_PERI\\_CLK\\_CTRL25\\_REG](#) register and clearing the [HP\\_SYS\\_CLKRST\\_REG\\_RST\\_EN\\_ECDSA](#) bit in the [HP\\_SYS\\_CLKRST\\_HP\\_RST\\_EN2\\_REG](#) register. For details on how to configure the ECDSA clock and reset, please refer to Chapter 9 [Reset and Clock](#).

## 28.5.3 Interrupts

ESP32-P4's ECDSA accelerator can generate one interrupt signal [ECDSA\\_INTR](#) and send it to [Interrupt Matrix](#).

The ECDSA accelerator has two interrupt sources that can generate the [ECDSA\\_INTR](#) interrupt signal:

- [ECDSA\\_CALC\\_DONE\\_INT](#): triggered on the completion of an ECC operation. This interrupt source is configured by the following registers:
  - [ECDSA\\_CALC\\_DONE\\_INT\\_RAW](#): stores the raw interrupt status of [ECDSA\\_CALC\\_DONE\\_INT](#).
  - [ECDSA\\_CALC\\_DONE\\_INT\\_ST](#): indicates the status of the [ECDSA\\_CALC\\_DONE\\_INT](#) interrupt. This field is generated by enabling/disabling the [ECDSA\\_CALC\\_DONE\\_INT\\_RAW](#) field.
  - [ECDSA\\_CALC\\_DONE\\_INT\\_ENA](#): enables/disables the [ECDSA\\_CALC\\_DONE\\_INT](#) interrupt.
  - [ECDSA\\_CALC\\_DONE\\_INT\\_CLR](#): set this bit to clear the [ECDSA\\_CALC\\_DONE\\_INT](#) interrupt status. By setting this bit to 1, fields [ECDSA\\_CALC\\_DONE\\_INT\\_RAW](#) and [ECDSA\\_CALC\\_DONE\\_INT\\_ST](#) will be cleared.
- [ECDSA\\_SHA\\_RELEASE\\_INT](#): triggered when SHA is released. This interrupt source is configured by the following registers:
  - [ECDSA\\_SHA\\_RELEASE\\_INT\\_RAW](#): stores the raw interrupt status of [ECDSA\\_SHA\\_RELEASE\\_INT](#).

- [ECDSA\\_SHA\\_RELEASE\\_INT\\_ST](#): indicates the status of the ECDSA\_SHA\_RELEASE\_INT interrupt. This field is generated by enabling/disabling the [ECDSA\\_SHA\\_RELEASE\\_INT\\_RAW](#) field via [ECDSA\\_SHA\\_RELEASE\\_INT\\_ENA](#).
- [ECDSA\\_SHA\\_RELEASE\\_INT\\_ENA](#): enables/disables the ECDSA\_SHA\_RELEASE\_INT interrupt.
- [ECDSA\\_SHA\\_RELEASE\\_INT\\_CLR](#): set this bit to clear the ECDSA\_SHA\_RELEASE\_INT interrupt status. By setting this bit to 1, fields [ECDSA\\_SHA\\_RELEASE\\_INT\\_RAW](#) and [ECDSA\\_SHA\\_RELEASE\\_INT\\_ST](#) will be cleared.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

## 28.6 Memory Blocks

ECDSA's memory blocks store input data and output data of the ECDSA operation.

Table 28.6-1. ECDSA Memory Blocks

| Memory       | Size (byte) | Starting Address <sup>*</sup> | Ending Address <sup>*</sup> | Access |
|--------------|-------------|-------------------------------|-----------------------------|--------|
| ECDSA_MEM_M  | 64          | 0x280                         | 0x2BF                       | R/W    |
| ECDSA_MEM_R  | 32          | 0xA00                         | 0xA1F                       | R/W    |
| ECDSA_MEM_S  | 32          | 0xA20                         | 0xA3F                       | R/W    |
| ECDSA_MEM_Z  | 32          | 0xA40                         | 0xA5F                       | R/W    |
| ECDSA_MEM_Qx | 32          | 0xA60                         | 0xA7F                       | R/W    |
| ECDSA_MEM_Qy | 32          | 0xA80                         | 0xA9F                       | R/W    |

<sup>\*</sup> Address offset related to the ECDSA accelerator base address is provided in Table 6.3-2 in Chapter 6 *System and Memory*.



## 28.7 Register Summary

The addresses in this section are relative to the ECDSA base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

To enhance security, ECDSA registers have different read and write permissions in different operating statuses. The following is the abbreviation and corresponding relationship of each state:

- PI: IDLE status, corresponding to IDLE Stage.
- PL: LOAD status, corresponding to LOAD Stage.
- PB: BUSY status, corresponding to PREP, PROC and POST Stage.

Other abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

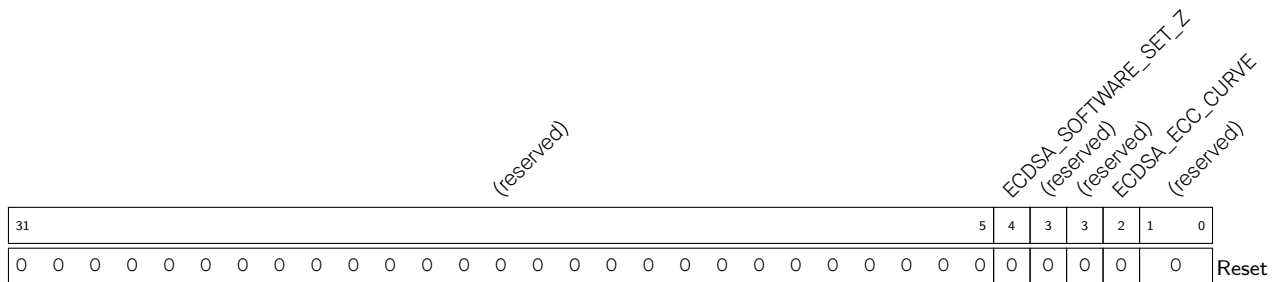
| Name                                   | Description                                     | Address | Access    |     |     |     |
|--|---|---------|-----------|-----|-----|-----|
|  |   |         | PI        | PL  | PG  | PB  |
| Data Memory                            | See Table 28.6-1.                               |         |           |     |     |     |
| Configuration Registers                |   |         |           |     |     |     |
| <a href="#">ECDSA_CONF_REG</a>         | ECDSA configuration register                    | 0x0004  | R/W       | N/A |     |     |
| <a href="#">ECDSA_START_REG</a>        | ECDSA start register                            | 0x001C  | WT        |     |     | N/A |
| Clock and Reset Register               |   |         |           |     |     |     |
| <a href="#">ECDSA_CLK_REG</a>          | ECDSA clock gate register                       | 0x0008  | R/W       | N/A |     |     |
| Interrupt Registers                    |   |         |           |     |     |     |
| <a href="#">ECDSA_INT_RAW_REG</a>      | ECDSA interrupt raw register                    | 0x000C  | RO/WTC/SS |     |     |     |
| <a href="#">ECDSA_INT_ST_REG</a>       | ECDSA interrupt status register                 | 0x0010  | RO        |     |     |     |
| <a href="#">ECDSA_INT_ENA_REG</a>      | ECDSA interrupt enable register                 | 0x0014  | R/W       |     |     |     |
| <a href="#">ECDSA_INT_CLR_REG</a>      | ECDSA interrupt clear register                  | 0x0018  | WT        |     |     |     |
| Status Registers                       |   |         |           |     |     |     |
| <a href="#">ECDSA_STATE_REG</a>        | ECDSA status register                           | 0x0020  | RO        |     |     |     |
| Result Register                        |   |         |           |     |     |     |
| <a href="#">ECDSA_RESULT_REG</a>       | ECDSA result register                           | 0x0024  | RO/SS     |     |     | N/A |
| SHA Registers                          |   |         |           |     |     |     |
| <a href="#">ECDSA_SHA_MODE_REG</a>     | ECDSA controlling SHA register (Hash algorithm) | 0x0200  | N/A       | R/W | N/A |     |
| <a href="#">ECDSA_SHA_START_REG</a>    | ECDSA controlling SHA register (operation)      | 0x0210  | N/A       | WT  | N/A |     |
| <a href="#">ECDSA_SHA_CONTINUE_REG</a> | ECDSA controlling SHA register (operation)      | 0x0214  | N/A       | WT  | N/A |     |
| <a href="#">ECDSA_SHA_BUSY_REG</a>     | ECDSA controlling SHA status register           | 0x0218  | N/A       | RO  | N/A |     |
| Version Register                       |   |         |           |     |     |     |
| <a href="#">ECDSA_DATE_REG</a>         | Version control register                        | 0x00FC  | R/W       | N/A |     |     |

## 28.8 Registers

The addresses in this section are relative to the ECDSA base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 28.1. ECDSA\_CONF\_REG (0x0004)**



**ECDSA\_ECC\_CURVE** Configures the elliptic curve used.

0: P-192

1: P-256

(R/W)

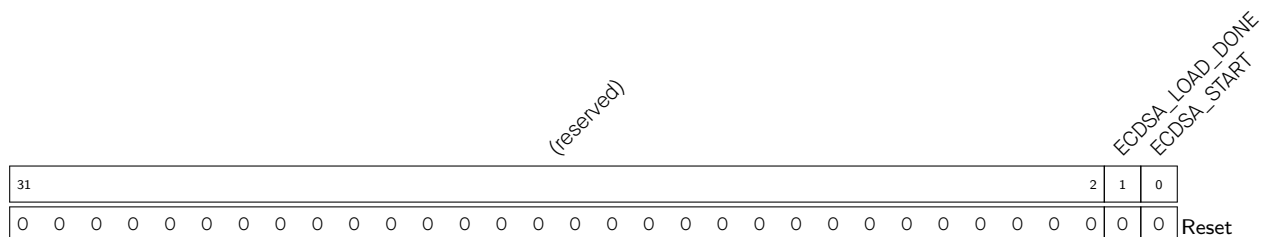
**ECDSA\_SOFTWARE\_SET\_Z** Configures how the parameter  $z$  is set.

0: generated from SHA result

1: written by software

(R/W)

**Register 28.2. ECDSA\_START\_REG (0x001C)**



**ECDSA\_START** Configures whether to start the ECDSA operation. This bit will be self-cleared after configuration.

0: no effect

1: start the ECDSA operation

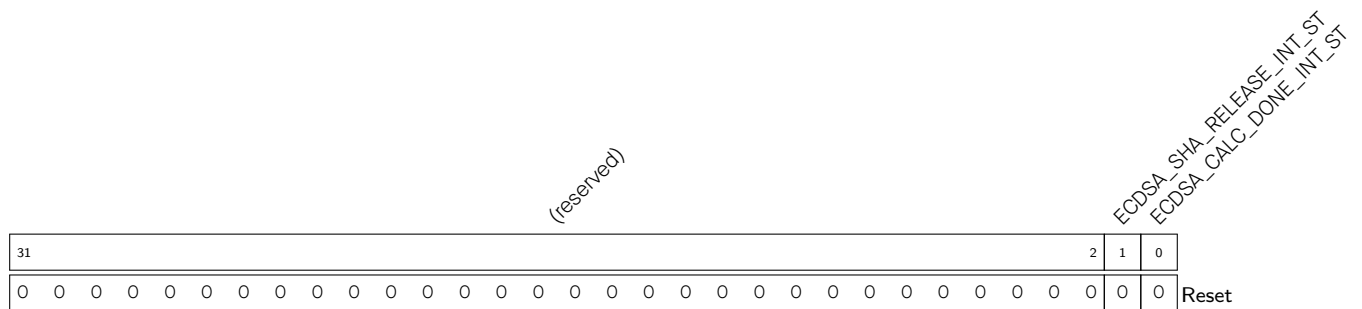
(WT)

**ECDSA\_LOAD\_DONE** Write 1 to generate a signal indicating the ECDSA accelerator's LOAD operation is done. This bit will be self-cleared after configuration. (WT)

ECDSA\_CLK\_GATE\_FORCE\_ON

ECDSA\_SHA\_RELEASE\_INT\_RAW  
ECDSA\_CALC\_DONE\_INT\_RAW

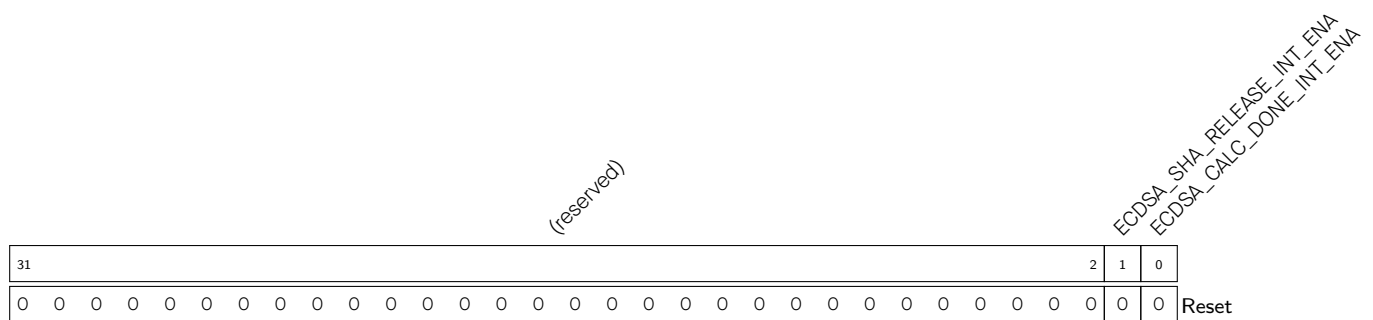
### Register 28.5. ECDSA\_INT\_ST\_REG (0x0010)



**ECDSA\_CALC\_DONE\_INT\_ST** The masked interrupt status of the **ECDSA\_CALC\_DONE\_INT** interrupt. (RO)

**ECDISA\_SHA\_RELEASE\_INT\_ST** The masked interrupt status of the [ECDISA\\_SHA\\_RELEASE\\_INT](#) interrupt. (RO)

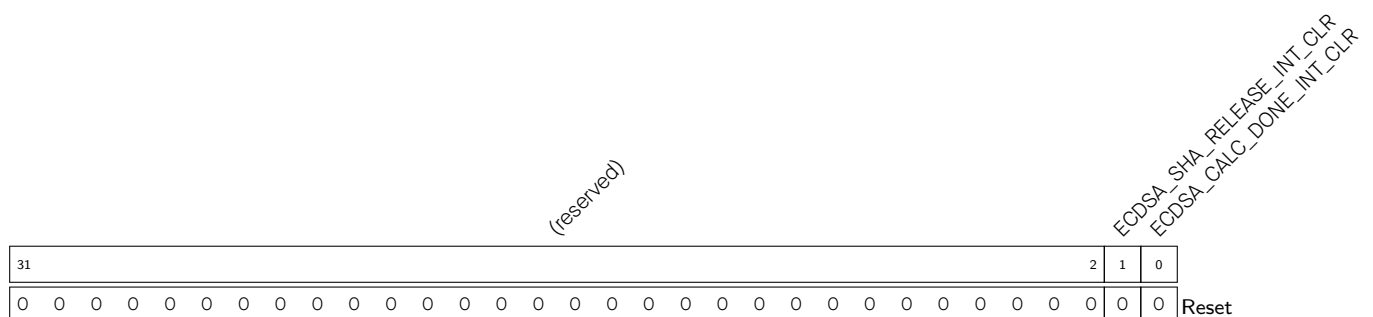
### Register 28.6. ECDSA\_INT\_ENA\_REG (0x0014)



**ECDSA\_CALC\_DONE\_INT\_ENA** Write 1 to enable the [ECDSA\\_CALC\\_DONE\\_INT](#) interrupt. (R/W)

**ECDSA\_SHA\_RELEASE\_INT\_ENA** Write 1 to enable the [ECDSA\\_SHA\\_RELEASE\\_INT](#) interrupt. (R/W)

### Register 28.7. ECDSA\_INT\_CLR\_REG (0x0018)



**ECDSA\_CALC\_DONE\_INT\_CLR** Write 1 to clear the [ECDSA\\_CALC\\_DONE\\_INT](#) interrupt. (WT)

**ECDSA\_SHA\_RELEASE\_INT\_CLR** Write 1 to clear the **ECDSA\_SHA\_RELEASE\_INT** interrupt. (WT)

Register 28.8. ECDSA\_STATE\_REG (0x0020)

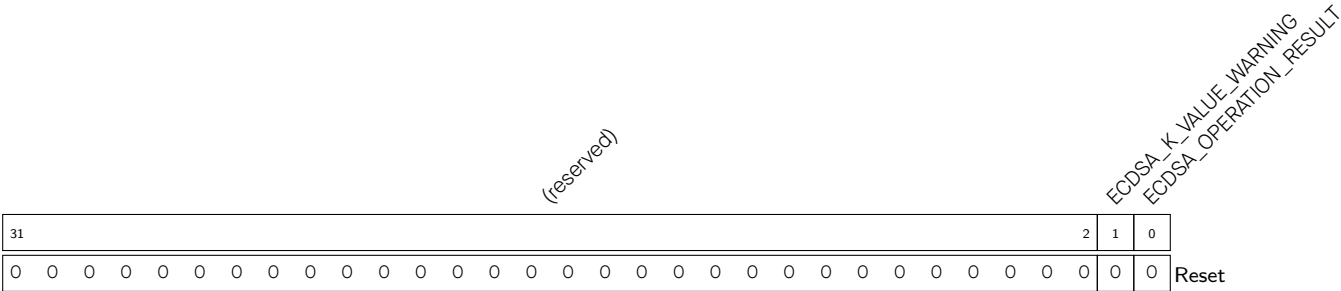


**ECDSA\_BUSY** Represents the working status of the ECDSA accelerator.

- 0: IDLE
- 1: LOAD
- 2: Reserved
- 3: BUSY

(RO)

Register 28.9. ECDSA\_RESULT\_REG (0x0024)



**ECDSA\_OPERATION\_RESULT** Indicates if the ECDSA operation is successful.

- 0: not successful
- 1: successful

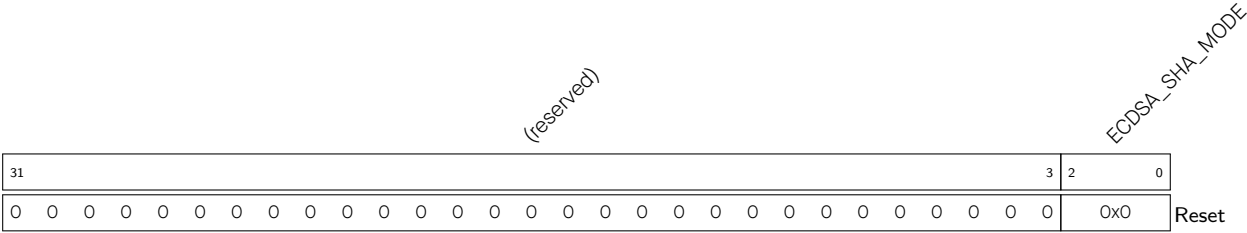
Only valid when the ECDSA operation is done. (RO/SS)

**ECDSA\_K\_VALUE\_WARNING** Indicates if the  $k$  value is greater than the base point order.

- 0:  $k$  value is not greater than the base point order. In this case, the  $k$  value is the set  $k$  value.
- 1:  $k$  value is greater than than the base point order. In this case, the  $k$  value is the set  $k \bmod n$ .

Only valid when the ECDSA operation is done. (RO/SS)

Register 28.10. ECDSA\_SHA\_MODE\_REG (0x0200)

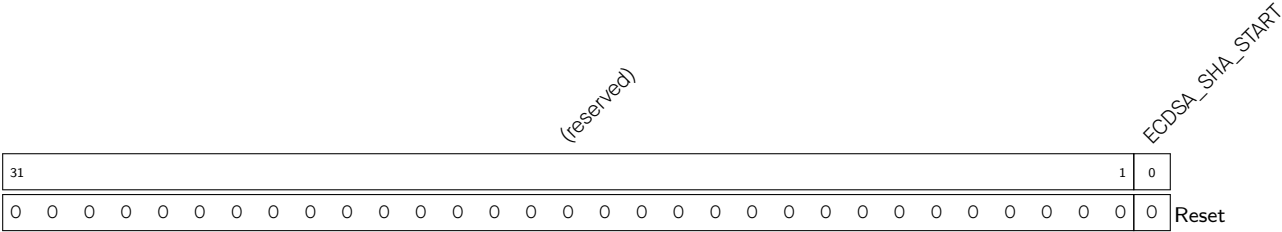


**ECDSA\_SHA\_MODE** Configures SHA algorithms for message hash.

- 1: SHA-224
- 2: SHA-256
- Others: invalid

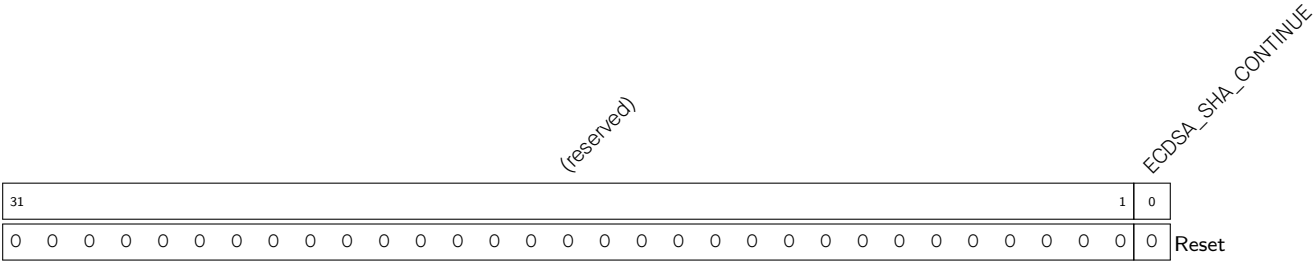
(R/W)

Register 28.11. ECDSA\_SHA\_START\_REG (0x0210)



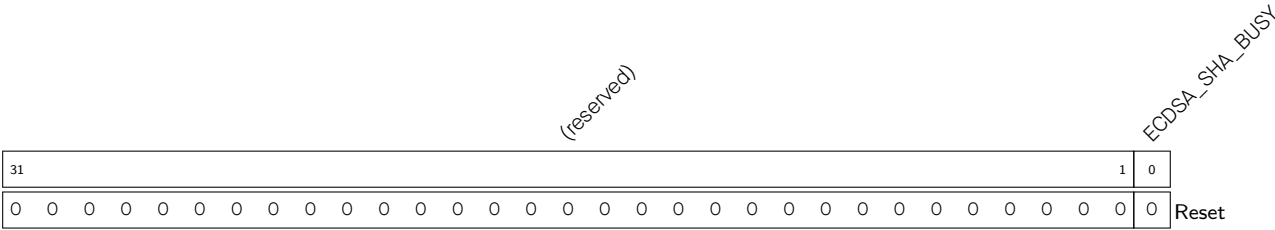
**ECDSA\_SHA\_START** Write 1 to start the first SHA operation in the ECDSA process. This bit will be self-cleared after configuration. (WT)

Register 28.12. ECDSA\_SHA\_CONTINUE\_REG (0x0214)



**ECDSA\_SHA\_CONTINUE** Write 1 to start the latter SHA operation in the ECDSA process. This bit will be self-cleared after configuration. (WT)

Register 28.13. ECDSA\_SHA\_BUSY\_REG (0x0218)

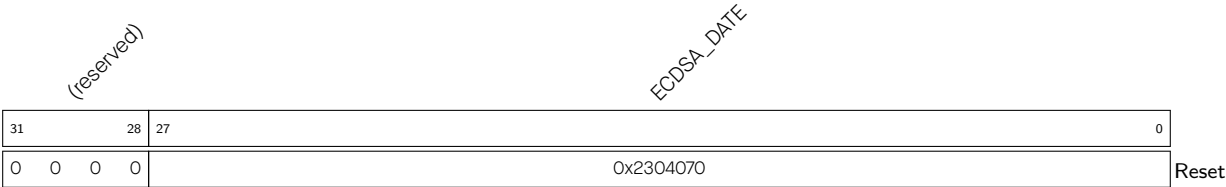


**ECDSA\_SHA\_BUSY** Represents the working status of the SHA accelerator in the ECDSA process.

- 0: IDLE
- 1: BUSY

(RO)

Register 28.14. ECDSA\_DATE\_REG (0x00FC)



**ECDSA\_DATE** The ECDSA version control register. (R/W)

## Chapter 29

# External Memory Encryption and Decryption (XTS\_AES)

## 29.1 Overview

The ESP32-P4 integrates an External Memory Encryption and Decryption module that complies with the XTS-AES standard algorithm specified in [IEEE Std 1619-2007](#), providing security for users' application code and data stored in the external memory (flash and RAM). Users can store proprietary firmware and sensitive data (e.g., credentials for gaining access to a private network) in the external flash, or store general data in the external RAM.

## 29.2 Features

- General XTS-AES algorithm, compliant with IEEE Std 1619-2007
- Software-based manual encryption
- High-speed auto encryption and decryption without software's participation
- Encryption and decryption functions jointly enabled/disabled by registers configuration, eFuse parameters, and boot mode
- Configurable Anti-DPA

## 29.3 Module Structure

The External Memory Encryption and Decryption module consists of three blocks, namely the Manual Encryption block, Auto Encryption block, and Auto Decryption block. The module architecture is shown in Figure [29.3-1](#).



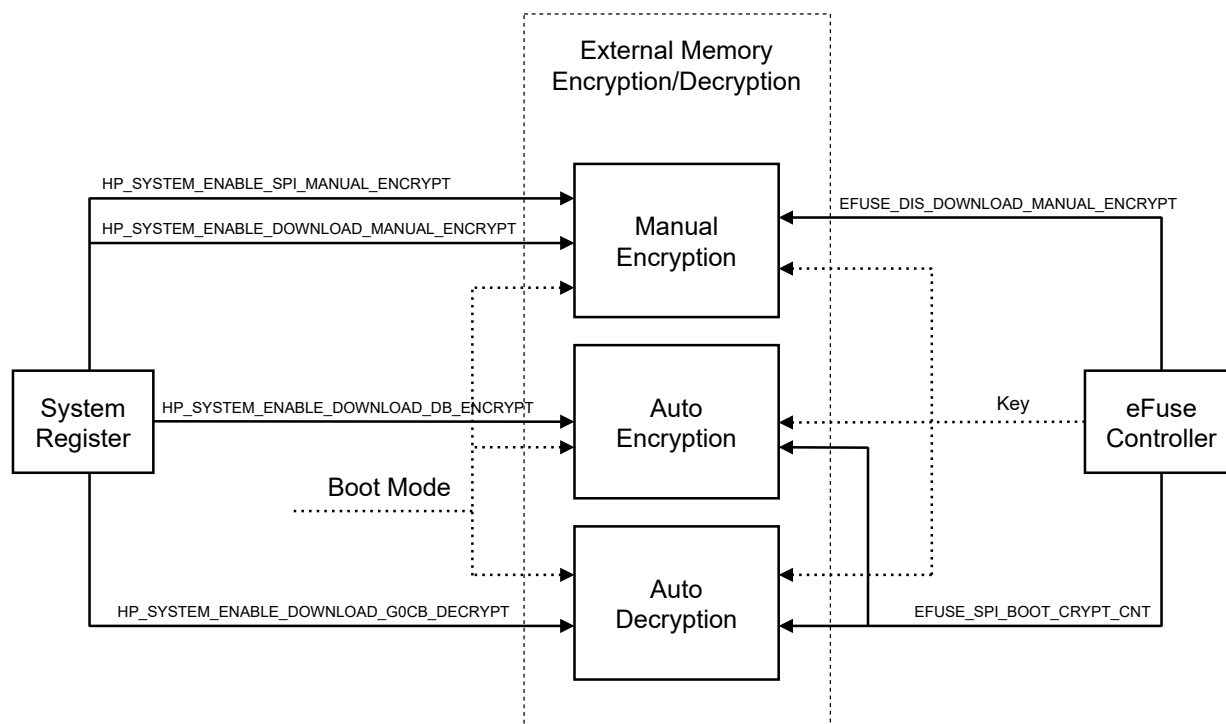


Figure 29.3-1. Architecture of the External Memory Encryption and Decryption

The Manual Encryption block can encrypt instructions and data, which will then be written to the external flash as ciphertext via SPI1.

When the CPU writes data to the external RAM through cache, the Auto Encryption block will automatically encrypt the data first, then the data will be written to the external RAM as ciphertext.

When the CPU reads from the external flash or external RAM through cache, the Auto Decryption block will automatically decrypt the ciphertext to retrieve instructions and data.

In the System Registers peripheral (see [3 System Registers \[to be added later\]](#)), the following four bits in register [HP\\_SYSTEM\\_EXTERNAL\\_DEVICE\\_ENCRYPT\\_DECRYPT\\_CONTROL\\_REG](#) are relevant to the external memory encryption and decryption:

- [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_MANUAL\\_ENCRYPT](#)
- [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_GOCB\\_DECRYPT](#)
- [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_DB\\_ENCRYPT](#)
- [HP\\_SYSTEM\\_ENABLE\\_SPI\\_MANUAL\\_ENCRYPT](#)

The XTS\_AES module also fetches two parameters from the peripheral eFuse Controller, which are: [EFUSE\\_DIS\\_DOWNLOAD\\_MANUAL\\_ENCRYPT](#) and [EFUSE\\_SPI\\_BOOT\\_CRYPT\\_CNT](#). For detailed information, please see Chapter [7 eFuse Controller](#).

## 29.4 Functional Description

## 29.4.1 XTS Algorithm

The manual encryption and auto encryption/decryption all use the same algorithm. During implementation, the XTS algorithm is characterized by a "data unit" of 1024 bits, defined in the Section *XTS-AES encryption procedure* of

[XTS-AES Tweakable Block Cipher](#) Standard. For more information about the XTS-AES algorithm, please refer to [IEEE Std 1619-2007](#).

## 29.4.2 Key

The Manual Encryption block, Auto Encryption block, and Auto Decryption block share the same *Key* when implementing the XTS algorithm. The *Key* is provided by the eFuse hardware and cannot be accessed by users.

The *Key* can be either 256-bit or 512-bit long. The value and length of the *Key* are determined by the content in the eFuse blocks from Block4 ~ Block9 and corresponding eFuse parameters. For easier description, we define:

- Block<sub>A</sub>: the block whose key purpose is EFUSE\_KEY\_PURPOSE\_XTS\_AES\_256\_KEY\_1 (please refer to Table 7.3-2 *Secure Key Purpose Values*). If Block<sub>A</sub> exists, a 256-bit *Key<sub>A</sub>* is stored in it.
- Block<sub>B</sub>: the block whose key purpose is EFUSE\_KEY\_PURPOSE\_XTS\_AES\_256\_KEY\_2 (please refer to Table 7.3-2 *Secure Key Purpose Values*). If Block<sub>B</sub> exists, a 256-bit *Key<sub>B</sub>* is stored in it.
- Block<sub>C</sub>: the block whose key purpose is EFUSE\_KEY\_PURPOSE\_XTS\_AES\_128\_KEY (please refer to Table 7.3-2 *Secure Key Purpose Values*). If Block<sub>C</sub> exists, a 256-bit *Key<sub>C</sub>* is stored in it.

There are five possibilities of how the *Key* is generated depending on whether Block<sub>A</sub>, Block<sub>B</sub>, and Block<sub>C</sub> exist or not, as shown in Table 29.4-1. In each case, the *Key* can be uniquely determined by Block<sub>A</sub>, Block<sub>B</sub> or Block<sub>C</sub>.

**Table 29.4-1. *Key* generated based on *Key<sub>A</sub>*, *Key<sub>B</sub>*, and *Key<sub>C</sub>***

| Block <sub>A</sub> | Block <sub>B</sub> | Block <sub>C</sub> | <i>Key</i>                                       | <i>Key</i> Length (bit) |
|--------------------|--------------------|--------------------|--|-------------------------|
| Yes                | Yes                | Don't care         | <i>Key<sub>A</sub></i>    <i>Key<sub>B</sub></i> | 512                     |
| Yes                | No                 | Don't care         | <i>Key<sub>A</sub></i>   0 <sup>256</sup>        | 512                     |
| No                 | Yes                | Don't care         | 0 <sup>256</sup>    <i>Key<sub>B</sub></i>       | 512                     |
| No                 | No                 | Yes                | <i>Key<sub>C</sub></i>                           | 256                     |
| No                 | No                 | No                 | 0 <sup>256</sup>                                 | 256                     |

### Notes:

- "YES" indicates that the block exists
- "NO" indicates that the block does not exist
- "0<sup>256</sup>" indicates a bit string that consists of 256-bit zeros
- "||" is a bonding operator for joining one-bit string to another

For more information on key purposes, please refer to Table 7.3-2 *Secure Key Purpose Values* in Chapter 7 *eFuse Controller*.

### 29.4.3 Target Memory Space

The target memory space refers to a continuous address space in the external memory where the first encrypted ciphertext is stored. The target memory space can be uniquely determined by three relevant parameters: type, size, and base address, whose definitions are listed below.

- Type: the *type* of the target memory space, either external flash or external RAM. Value 0 indicates external flash, while 1 indicates external RAM.
- Size: the *size* of the target memory space, indicating the number of bytes encrypted in one encryption operation, which supports 16, 32, or 64 bytes.
- Base address: the *base\_addr* of the target memory space. It is a 30-bit physical address, with a range of 0x0000\_0000 ~ 0x3FFF\_FFFF. It should be aligned to *size*, i.e.,  $base\_addr \% size == 0$ .

For example, if there are 16 bytes of instruction data that need to be encrypted and written to address 0x130 ~ 0x13F in the external flash, then the target space is 0x130 ~ 0x13F, type is 0 (external flash), size is 16 (bytes), and the base address is 0x130.

The encryption of any length (must be multiples of 16 bytes) of plaintext instruction/data can be completed separately in multiple operations, and each operation has individual target memory space and relevant parameters.

For Auto Encryption/Decryption blocks, these parameters are automatically defined by hardware. For the Manual Encryption block, these parameters should be configured manually by users.

**Note:**

The “tweak” defined in Chapter 5.1 *Data units and tweaks* of [IEEE Std 1619-2007](#) is a 128-bit non-negative integer (*tweak*), which can be generated according to  $tweak = type * 2^{30} + (base\_addr \& 0x3FFFFFF80)$ . The lowest 7 bits and the highest 97 bits in *tweak* are always zero.

### 29.4.4 Data Writing

For Auto Encryption/Decryption blocks, data writing is automatically applied in hardware. For Manual Encryption blocks, data writing should be applied by users. The Manual Encryption block has a register block which consists of 16 registers, i.e., `XTS_AES_PLAIN_n_REG` ( $n$ : 0 ~ 15), that are dedicated to data writing and can store up to 512 bits of plaintext at a time.

Actually, the Manual Encryption block does not care where the plaintext comes from, but only where the ciphertext will be stored. Because of the strict correspondence between plaintext and ciphertext, in order to better describe how the plaintext is stored in the register block, we assume that the plaintext is stored in the target memory space in the first place and replaced by ciphertext after encryption. Therefore, the following description in this section no longer has the concept of “plaintext”, but uses “target memory space” instead.

**How mapping between target memory space and registers works:**

Assume a word in the target memory space is stored in *address*, define  $offset = address \% 64$ ,  $n = offset / 4$ , then the word will be stored in register `XTS_AES_PLAIN_n_REG`.

For example, when the *size* is 64, all registers in the register block will be used. The mapping between *offset* and registers now is shown in Table 29.4-2.

Table 29.4-2. Mapping Between Offsets and Registers

| <i>offset</i> | Register                            | <i>offset</i> | Register                             |
|---------------|-------------------------------------|---------------|--------------------------------------|
| 0x00          | <a href="#">XTS_AES_PLAIN_0_REG</a> | 0x20          | <a href="#">XTS_AES_PLAIN_8_REG</a>  |
| 0x04          | <a href="#">XTS_AES_PLAIN_1_REG</a> | 0x24          | <a href="#">XTS_AES_PLAIN_9_REG</a>  |
| 0x08          | <a href="#">XTS_AES_PLAIN_2_REG</a> | 0x28          | <a href="#">XTS_AES_PLAIN_10_REG</a> |
| 0x0C          | <a href="#">XTS_AES_PLAIN_3_REG</a> | 0x2C          | <a href="#">XTS_AES_PLAIN_11_REG</a> |
| 0x10          | <a href="#">XTS_AES_PLAIN_4_REG</a> | 0x30          | <a href="#">XTS_AES_PLAIN_12_REG</a> |
| 0x14          | <a href="#">XTS_AES_PLAIN_5_REG</a> | 0x34          | <a href="#">XTS_AES_PLAIN_13_REG</a> |
| 0x18          | <a href="#">XTS_AES_PLAIN_6_REG</a> | 0x38          | <a href="#">XTS_AES_PLAIN_14_REG</a> |
| 0x1C          | <a href="#">XTS_AES_PLAIN_7_REG</a> | 0x3C          | <a href="#">XTS_AES_PLAIN_15_REG</a> |

### 29.4.5 Manual Encryption Block

The Manual Encryption block is a peripheral module. It is equipped with registers and can be accessed by the CPU directly. Registers embedded in this block, the System Registers peripheral, eFuse parameters, and boot mode jointly configure and use this module. Please note that the Manual Encryption block can only encrypt for storage in the external flash.

**The Manual Encryption block is operational only under certain conditions:**

- In SPI Boot mode:

If bit [HP\\_SYSTEM\\_ENABLE\\_SPI\\_MANUAL\\_ENCRYPT](#) in register

[HP\\_SYSTEM\\_EXTERNAL\\_DEVICE\\_ENCRYPT\\_DECRYPT\\_CONTROL\\_REG](#) is 1, the Manual Encryption block can be enabled. Otherwise, it is not operational.

- In Joint Download Boot mode:

If bit [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_MANUAL\\_ENCRYPT](#) in register

[HP\\_SYSTEM\\_EXTERNAL\\_DEVICE\\_ENCRYPT\\_DECRYPT\\_CONTROL\\_REG](#) is 1 and the eFuse parameter [EFUSE\\_DIS\\_DOWNLOAD\\_MANUAL\\_ENCRYPT](#) is 0, the Manual Encryption block can be enabled.

Otherwise, it is not operational.

**Note:**

Even though the CPU can skip cache and get the encrypted instruction/data directly by reading the external memory, users can by no means access *Key*.

### 29.4.6 Auto Encryption Block

The Auto Encryption block is not a conventional peripheral, so it does not have any registers and cannot be accessed by the CPU directly. The System Registers peripheral, eFuse parameters, and boot mode jointly configure and use this block.

**The Auto Encryption block is operational only under certain conditions:**

- In SPI Boot mode:

when [EFUSE\\_SPI\\_BOOT\\_CRYPT\\_CNT](#) (3 bits) is set to 1, 2, 4 or 7 (i.e., there is an odd number of 1s in its binary representation), then the Auto Encryption block can be enabled. Otherwise, it is not operational.

- In Joint Download Boot mode:

when bit [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_DB\\_ENCRYPT](#) in register

[HP\\_SYSTEM\\_EXTERNAL\\_DEVICE\\_ENCRYPT\\_DECRYPT\\_CONTROL\\_REG](#) is 1, the Auto Encryption block can be enabled. Otherwise, it is not operational.

**Note:**

- When the Auto Encryption block is enabled, it will automatically encrypt data if the CPU writes data to the external RAM, and then the encrypted ciphertext will be written to the external RAM. The entire encryption process does not need software participation and is transparent to the cache. Users can by no means obtain the encryption *Key* during the process.
- When the Auto Encryption block is disabled, it will ignore the CPU's access request to the cache and not process the data. Therefore, the data will be written to the external RAM as plaintext directly.

## 29.4.7 Auto Decryption Block

The Auto Decryption block is not a conventional peripheral, so it does not have any registers and cannot be accessed by the CPU directly. The System Registers peripheral, eFuse parameters, and boot mode jointly configure and use this block.

**The Auto Decryption block is operational only under certain conditions:**

- In SPI Boot mode:

when [EFUSE\\_SPI\\_BOOT\\_CRYPT\\_CNT](#) (3 bits in total) is set to 1, 2, 4 or 7 (i.e., there is an odd number of 1s in its binary representation), then the Auto Decryption block can be enabled. Otherwise, it is not operational.

- In Joint Download Boot mode:

when bit [HP\\_SYSTEM\\_ENABLE\\_DOWNLOAD\\_GOCB\\_DECRYPT](#) in register

[HP\\_SYSTEM\\_EXTERNAL\\_DEVICE\\_ENCRYPT\\_DECRYPT\\_CONTROL\\_REG](#) is 1, the Auto Decryption block can be enabled. Otherwise, it is not operational.

**Note:**

- When the Auto Decryption block is enabled, it will automatically decrypt the ciphertext if the CPU reads instructions/data from the external memory via cache to retrieve the instructions/data. The entire decryption process does not need software participation and is transparent to the cache. The software can by no means obtain the decryption *Key* during the process.
- When the Auto Decryption block is disabled, it does not have any effect on the contents stored in the external memory, no matter if they are encrypted or not. Therefore, what the CPU reads via cache is the original information stored in the external memory.

## 29.5 Software Process

When the Manual Encryption block operates, software needs to be involved in the process. The steps are as follows:

## 1. Configure XTS\_AES:

- Set register [XTS\\_AES\\_DESTINATION\\_REG](#) to *type* = 0.
- Set register [XTS\\_AES\\_PHYSICAL\\_ADDRESS\\_REG](#) to *base\_addr*.
- Set register [XTS\\_AES\\_LINESIZE\\_REG](#) to  $\frac{size}{32}$ .

For definitions of *base\_addr* and *size*, please refer to Section [29.4.3](#).

2. Write plaintext instructions/data to the registers block XTS\_AES\_PLAIN\_*n*\_REG (*n*: 0-15). For detailed information, please refer to Section [29.4.4](#).

Please write data to registers according to your actual needs, and the unused ones could be set to arbitrary values.

3. Wait for Manual Encryption block to be idle. Poll register [XTS\\_AES\\_STATE\\_REG](#) until it reads 0 which indicates the Manual Encryption block is idle.4. Trigger manual encryption by writing 1 to register [XTS\\_AES\\_TRIGGER\\_REG](#).5. Wait for the encryption process completion. Poll register [XTS\\_AES\\_STATE\\_REG](#) until it reads 2.

*Step 1 to 5 are the steps of encrypting plaintext instructions/data with the Manual Encryption block using the Key.*

6. Write 1 to register [XTS\\_AES\\_RELEASE\\_REG](#) to grant SPI1 the access to the encrypted ciphertext. After this, the value of register [XTS\\_AES\\_STATE\\_REG](#) will become 3.7. Call SPI1 to write the ciphertext in the external flash (see Section [API Reference - Flash Encrypt](#) in [ESP-IDF Programming Guide](#)).8. Write 1 to register [XTS\\_AES\\_DESTROY\\_REG](#) to destroy the ciphertext. After this, the value of register [XTS\\_AES\\_STATE\\_REG](#) will become 0.

Repeat the above steps according to the amount of plaintext instructions/data that need to be encrypted.

## 29.6 Anti-DPA

DPA (Differential Power Analysis) is a side-channel attack method in cryptography, through which an attacker can statistically analyze data collected from multiple encryption operations to calculate intermediate values in the encryption computation. ESP32-P4 XTS\_AES supports Anti-DPA to defend against external DPA attacks.

The XTS-AES algorithm can be divided into two steps, according to [IEEE Std 1619-2007](#):

- Step 1: Calculating T value. In this section, we define this step as "calculating T".
- Step 2: Calculating Cipher/Plain text. In this section, we define this step as "calculating D".

Different security levels can be configured through registers:

- First we define the below parameters for a better description:
  - *select\_reg* = [XTS\\_AES\\_CRYPT\\_DPA\\_SELECT\\_REGISTER](#)
  - *reg\_d\_dpa\_en* = [XTS\\_AES\\_CRYPT\\_CALC\\_D\\_DPA\\_EN](#)
  - *efuse\_dpa\_en* = [EFUSE\\_CRYPT\\_DPA\\_ENABLE](#)

- $reg\_anti\_dpa\_level = XTS\_AES\_CRYPT\_SECURITY\_LEVEL$
- $efuse\_anti\_dpa\_level = 3$

- Configure the security level of Anti-DPA for the XTS\_AES module:

$$Anti\_DPA\_level = select\_reg ? (reg\_anti\_dpa\_level) : (efuse\_dpa\_en * efuse\_anti\_dpa\_level)$$

When  $Anti\_DPA\_level$  equals 0, Anti-DPA is disabled. The higher the value of  $Anti\_DPA\_level$  is, the stronger the Anti-DPA ability is.

- Configure whether to enable Anti-DPA when the XTS-AES algorithm is calculating D:

$$Anti\_DPA\_enabled\_in\_calc\_D = select\_reg ? reg\_d\_dpa\_en : efuse\_dpa\_en$$

If  $Anti\_DPA\_level$  is not 0, when  $Anti\_DPA\_enabled\_in\_calc\_D$  equals to 1, Anti-DPA is enabled when XTS-AES algorithm is calculating D.

If  $Anti\_DPA\_level$  is not 0, Anti-DPA is always enabled when the XTS-AES algorithm is calculating T.

**Note:**

- Even if  $efuse\_dpa\_en$  is set to 1, you can still disable anti-DPA by configuring  $select\_reg = 1$  and  $reg\_anti\_dpa\_level = 0$ .
- Configuring whether or not to enable Anti-DPA will have an impact on the external storage access bandwidth:
  - When Anti-DPA is enabled during the calculation of D, the read and write bandwidth will be reduced by more than 50% when the Anti-DPA level  $\geq 4$ .
  - When Anti-DPA is disabled during the calculation of D, the read and write bandwidth will be reduced by more than 50% when the Anti-DPA level  $\geq 6$ .

## 29.7 Register Summary

The addresses in this section are relative to the External Memory Encryption and Decryption base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description                                | Address | Access |
|--|--|---------|--------|
| <b>Plaintext Register Heap</b>               |  |         |        |
| <a href="#">XTS_AES_PLAIN_0_REG</a>          | Plaintext register 0                       | 0x0300  | R/W    |
| <a href="#">XTS_AES_PLAIN_1_REG</a>          | Plaintext register 1                       | 0x0304  | R/W    |
| <a href="#">XTS_AES_PLAIN_2_REG</a>          | Plaintext register 2                       | 0x0308  | R/W    |
| <a href="#">XTS_AES_PLAIN_3_REG</a>          | Plaintext register 3                       | 0x030C  | R/W    |
| <a href="#">XTS_AES_PLAIN_4_REG</a>          | Plaintext register 4                       | 0x0310  | R/W    |
| <a href="#">XTS_AES_PLAIN_5_REG</a>          | Plaintext register 5                       | 0x0314  | R/W    |
| <a href="#">XTS_AES_PLAIN_6_REG</a>          | Plaintext register 6                       | 0x0318  | R/W    |
| <a href="#">XTS_AES_PLAIN_7_REG</a>          | Plaintext register 7                       | 0x031C  | R/W    |
| <a href="#">XTS_AES_PLAIN_8_REG</a>          | Plaintext register 8                       | 0x0320  | R/W    |
| <a href="#">XTS_AES_PLAIN_9_REG</a>          | Plaintext register 9                       | 0x0324  | R/W    |
| <a href="#">XTS_AES_PLAIN_10_REG</a>         | Plaintext register 10                      | 0x0328  | R/W    |
| <a href="#">XTS_AES_PLAIN_11_REG</a>         | Plaintext register 11                      | 0x032C  | R/W    |
| <a href="#">XTS_AES_PLAIN_12_REG</a>         | Plaintext register 12                      | 0x0330  | R/W    |
| <a href="#">XTS_AES_PLAIN_13_REG</a>         | Plaintext register 13                      | 0x0334  | R/W    |
| <a href="#">XTS_AES_PLAIN_14_REG</a>         | Plaintext register 14                      | 0x0338  | R/W    |
| <a href="#">XTS_AES_PLAIN_15_REG</a>         | Plaintext register 15                      | 0x033C  | R/W    |
| <b>Configuration Registers</b>               |  |         |        |
| <a href="#">XTS_AES_LINESIZE_REG</a>         | Configures the size of target memory space | 0x0340  | R/W    |
| <a href="#">XTS_AES_DESTINATION_REG</a>      | Configures the type of the external memory | 0x0344  | R/W    |
| <a href="#">XTS_AES_PHYSICAL_ADDRESS_REG</a> | Physical address                           | 0x0348  | R/W    |
| <a href="#">XTS_AES_DPA_CTRL_REG</a>         | Configures the Anti-DPA function           | 0x0388  | R/W    |
| <b>Control/Status Registers</b>              |  |         |        |
| <a href="#">XTS_AES_TRIGGER_REG</a>          | Activates AES algorithm                    | 0x034C  | WO     |
| <a href="#">XTS_AES_RELEASE_REG</a>          | Release control                            | 0x0350  | WO     |
| <a href="#">XTS_AES_DESTROY_REG</a>          | Destroy control                            | 0x0354  | WO     |
| <a href="#">XTS_AES_STATE_REG</a>            | Status register                            | 0x0358  | RO     |
| <b>Version Register</b>                      |  |         |        |
| <a href="#">XTS_AES_DATE_REG</a>             | Version control register                   | 0x035C  | R/W    |

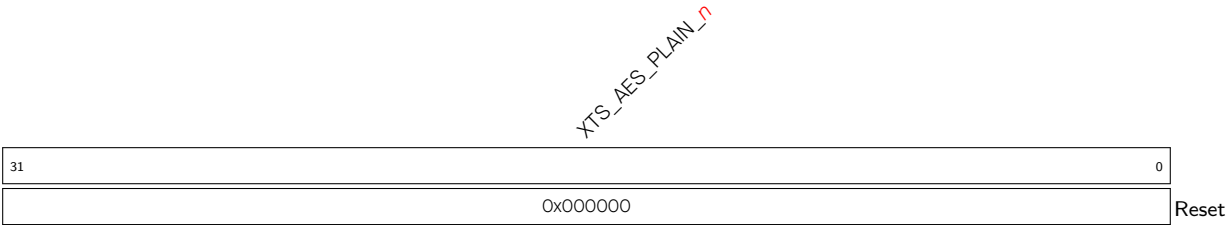


## 29.8 Registers

The addresses in this section are relative to the External Memory Encryption and Decryption base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

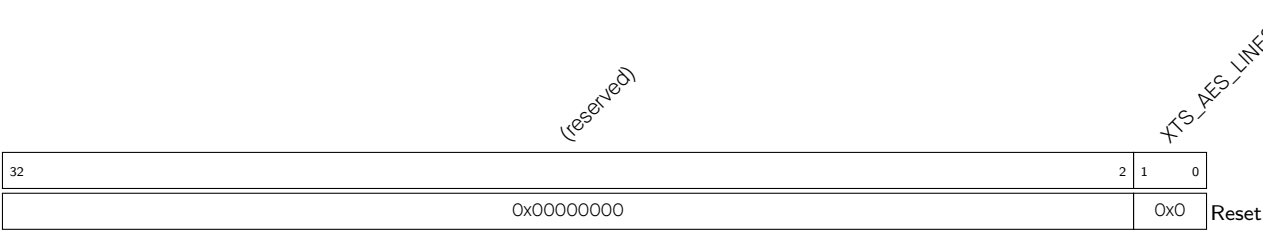
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 29.1. XTS\_AES\_PLAIN\_ *n* \_REG (*n*: 0-15) (0x0300+4\**n*)



XTS\_AES\_PLAIN\_ *n* Configures the *n*th 32-bit piece of plain text. (R/W)

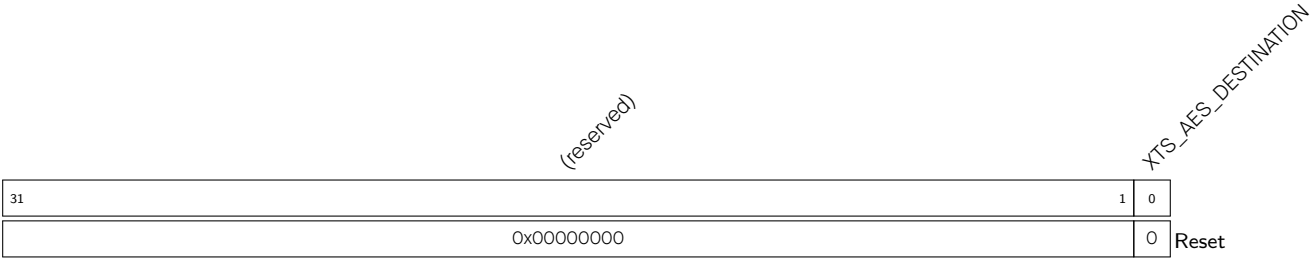
Register 29.2. XTS\_AES\_LINESIZE\_REG (0x0340)



XTS\_AES\_LINESIZE Configures the data size of one encryption operation.

- 0: 16 bytes
  - 1: 32 bytes
  - 2: 64 bytes
  - 3: Invalid
- (R/W)

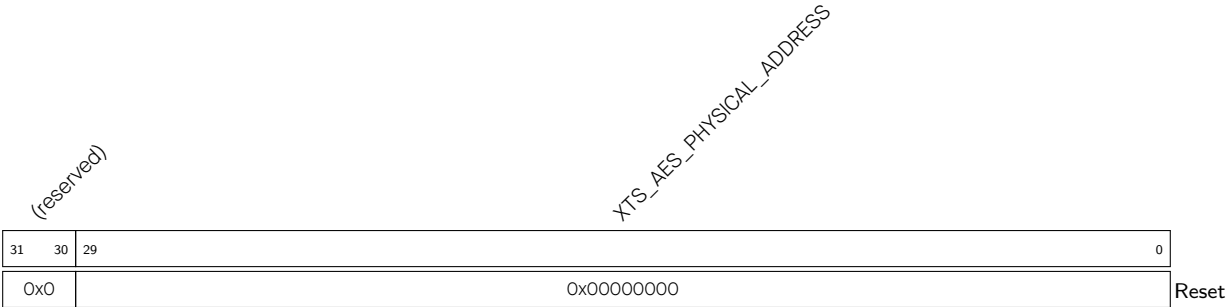
Register 29.3. XTS\_AES\_DESTINATION\_REG (0x0344)



**XTS\_AES\_DESTINATION** Configures the type of external memory for Manual Encryption. Currently, it must be set to 0, as the Manual Encryption block only supports flash encryption. Set this bit to 1 may cause an error.

0: flash  
1: external RAM  
(R/W)

Register 29.4. XTS\_AES\_PHYSICAL\_ADDRESS\_REG (0x0348)



**XTS\_AES\_PHYSICAL\_ADDRESS** Configures physical address. Note that its value should be within the range between 0x0000\_0000 and 0x00FF\_FFFF. (R/W)

**Register 29.5. XTS\_AES\_DPA\_CTRL\_REG (0x0388)**

|            |  |  |  |  |  |  |  |  |  |  |     |   |     |   |     |                                   |       |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|-----|---|-----|---|-----|-----------------------------------|-------|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |     |   |     |   |     | XTS_AES_CRYPT_DPA_SELECT_REGISTER |       |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |     |   |     |   |     | XTS_AES_CRYPT_CALC_D_DPA_EN       |       |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |     |   |     |   |     | XTS_AES_CRYPT_SECURITY_LEVEL      |       |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  | 5   | 4 | 3   | 2 | 0   |                                   |       |  |  |  |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  | 0x0 |   | 0x1 |   | 0x7 |                                   | Reset |  |  |  |

**XTS\_AES\_CRYPT\_DPA\_SELECT\_REGISTER** Configures whether the Anti-DPA function is controlled by eFuse or register.

0: The Anti-DPA function is configured by register.

1: The Anti-DPA function is configured by eFuse.

(R/W)

**XTS\_AES\_CRYPT\_CALC\_D\_DPA\_EN** Configures whether to enable Anti-DPA in the XTS\_AES algorithm.

0: Enable Anti-DPA only when calculating T

1: Enable Anti-DPA both when calculating T and D

Note that this field is only effective when [XTS\\_AES\\_CRYPT\\_SECURITY\\_LEVEL](#) is not 0.

(R/W)

**XTS\_AES\_CRYPT\_SECURITY\_LEVEL** Configures the security level of external memory encryption and decryption.

0: Disable the Anti-DPA function

1-7: The bigger the number is, the more secure the encryption and decryption are

(R/W)

**Register 29.6. XTS\_AES\_TRIGGER\_REG (0x034C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |       |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|-------|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | XTS_AES_TRIGGER |  |       |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1               |  | 0     |  |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | x               |  | Reset |  |

**XTS\_AES\_TRIGGER** Configures whether or not to enable manual encryption.

0: Disable manual encryption

1: Enable manual encryption

(WO)

**Register 29.7. XTS\_AES\_RELEASE\_REG (0x0350)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |                 |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-----------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | XTS_AES_RELEASE |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | 0               | Reset |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | x               |       |

**XTS\_AES\_RELEASE** Configures whether to grant SPI1 access to the encrypted result.

0: No effect

1: Grant SPI1 access

(WO)

**Register 29.8. XTS\_AES\_DESTROY\_REG (0x0354)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |                 |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-----------------|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | XTS_AES_DESTROY |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | 0               | Reset |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | x               |       |

**XTS\_AES\_DESTROY** Configures whether to destroy the encrypted result.

0: No effect

1: Destroy encrypted result

(WO)

**Register 29.9. XTS\_AES\_STATE\_REG (0x0358)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |               |   |  |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---------------|---|--|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | XTS_AES_STATE |   |  |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2 | 1             | 0 |  |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | 0x0           |   |  | Reset |

**XTS\_AES\_STATE** Represents the status of the Manual Encryption block. 0 (XTS\_AES\_IDLE): Idle

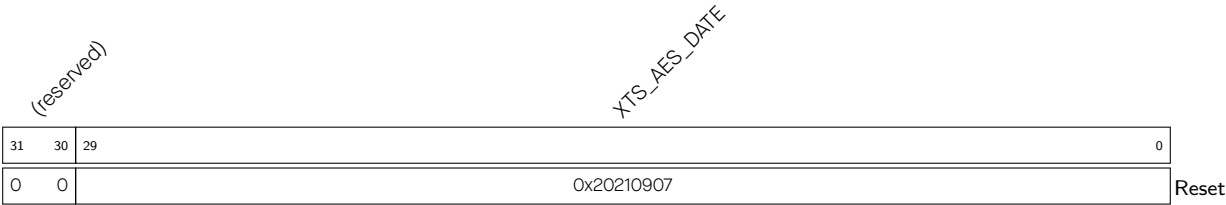
1 (XTS\_AES\_BUSY): Busy with encryption

2 (XTS\_AES\_DONE): Encryption completed, but the encrypted result is not accessible to SPI

3 (XTS\_AES\_RELEASE): Encrypted result is accessible to SPI

(RO)

Register 29.10. XTS\_AES\_DATE\_REG (0x035C)



**XTS\_AES\_DATE** Version control register. (R/W)

## Chapter 30

# Random Number Generator (RNG)

## 30.1 Introduction

The ESP32-P4 contains a true random number generator, which generates 32-bit random numbers that can be used for cryptographical operations, among other things.

## 30.2 Feature List

The random number generator in ESP32-P4 generates true random numbers, which means random numbers generated from a physical process, rather than by means of an algorithm. No number generated within the specified range is more or less likely to appear than any other number.

## 30.3 Functional Description

Every 32-bit value that the system reads from the [LPSYSREG\\_RNG\\_DATA\\_REG](#) register of the random number generator is a true random number. These true random numbers are generated based on the **thermal noise** in the system and the **asynchronous clock mismatch**.

- **Thermal noise** comes from the SAR ADC. Whenever the SAR ADC is enabled, bit streams will be generated and fed into the random number generator through an XOR logic gate as random seeds.
- RC\_FAST\_CLK is an **asynchronous clock** source and it increases the RNG entropy by introducing circuit metastability. Please refer to the [Note](#) about the RC\_FAST\_CLK.

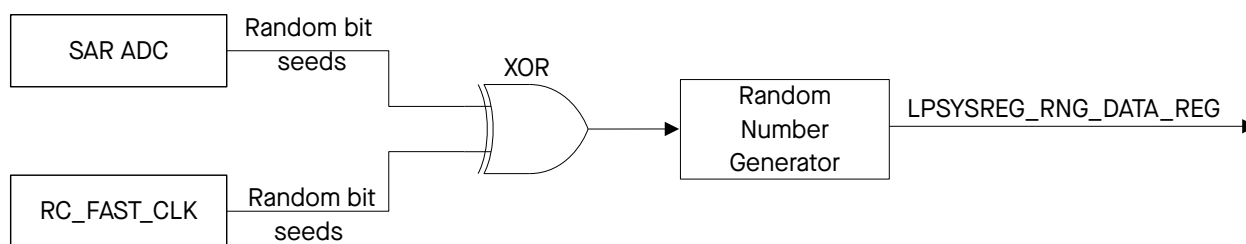


Figure 30.3-1. Noise Source

When there is noise coming from the SAR ADC, the random number generator is fed with a 1-bit entropy in one clock cycle of RC\_FAST\_CLK, which is generated from an internal RC oscillator (see Chapter 9 [Reset and Clock](#) for details). Thus, it is advisable to read the [LPSYSREG\\_RNG\\_DATA\\_REG](#) register at a maximum rate of 1 MHz to obtain the maximum entropy.

## 30.4 Programming Procedure

When using the random number generator, make sure at least either the SAR ADC or RC\_FAST\_CLK is enabled. Otherwise, pseudo-random numbers will be returned.

- For SAR ADC, please refer to Chapter [57 ADC Controller \(ADC\)](#).
- RC\_FAST\_CLK is enabled by setting the PMU\_HP\_SLEEP\_XPD\_FOSC\_CLK bit in the [PMU\\_HP\\_SLEEP\\_LP\\_CK\\_POWER\\_REG](#) register. Please refer to the [Note](#) about the RC\_FAST\_CLK.
- RC\_FAST\_CLK is gated by setting the [LPPERI\\_CK\\_EN\\_RNG](#) bit in the [LPPERI\\_CLK\\_EN\\_REG](#) register.

**Note:**

Enabling RC\_FAST\_CLK increases the RNG entropy. However, to ensure maximum entropy, it's recommended to always enable an ADC source as well.

When using the random number generator, read the [LPSYSREG\\_RNG\\_DATA\\_REG](#) register multiple times until sufficient random numbers have been generated. Ensure the rate at which the register is read does not exceed the frequencies described in section [30.3](#) above.

## 30.5 Register Summary

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

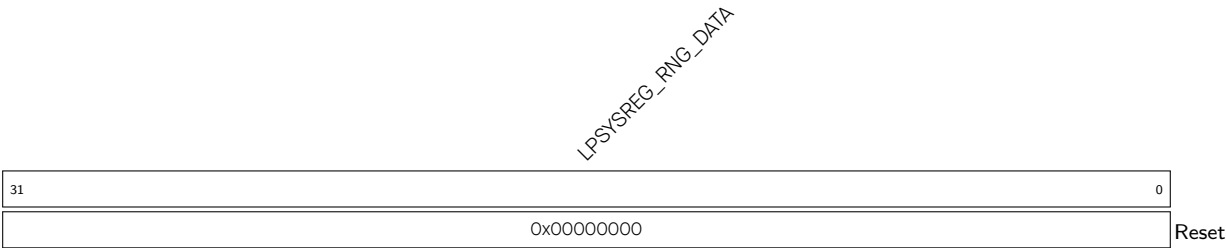
| Name                                  | Description  | Address     | Access |
|---------------------------------------|--|-------------|--------|
| <a href="#">LPSYSREG_RNG_DATA_REG</a> | Random source data                                   | 0x5011_01A4 | RO     |
| <a href="#">LPPERI_CLK_EN_REG</a>     | Integrated clock gating enable signal of RC_FAST_CLK | 0x5012_0000 | R/W    |



# 30.6 Registers

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 30.1. LPSYSREG\_RNG\_DATA\_REG (0x5011\_01A4)



**LPSYSREG\_RNG\_DATA** Random number source. (RO)

## Part VI

# Image and Voice Processing

Focusing on multimedia processing, this part classifies components related to image and voice processing, including camera controllers, video encoders, image signal processors, and voice activity detection.

## Chapter 31

### JPEG Codec

ESP32-P4's JPEG codec is an image codec, which is based on the JPEG baseline standard, for compressing (encoding) and decompressing (decoding) images to reduce the bandwidth required to transmit images or the space required to store images, making it possible to process large-resolution images. The image encoding process mainly includes discrete cosine transform (DCT), zigzag scanning, quantization, and Huffman coding. The image decoding process, which is the inverse operation of the encoding process, mainly includes Huffman decoding, inverse quantization, inverse zigzag scanning, and inverse discrete cosine transform (IDCT).

#### 31.1 Terminology

|                         |   |
|-------------------------|---|
| <b>MCU</b>              | Minimum coded unit. The basic unit of codec processing  |
| <b>baseline</b>         | A particular sequential DCT-based encoding and decoding process specified in the standard, which is required for all DCT-based decoding processes   |
| <b>image</b>            | A set of two-dimensional arrays of integer data   |
| <b>component</b>        | One of the two-dimensional arrays that comprise an image  |
| <b>data unit</b>        | An $8 \times 8$ block of pixels of one component  |
| <b>marker</b>           | A two-byte code in which the first byte is hexadecimal FF (0xFF) and the second byte is a value between 1 and hexadecimal FE (0xFE). It is served to identify the various structural parts of the compressed data formats |
| <b>restart marker</b>   | Used to isolate coded data segments and for application-specific uses, such as decoder re-synchronization and error recovery  |
| <b>restart interval</b> | The integer number of MCUs processed between two restart markers  |
| <b>scan</b>             | A single pass through the data for one or more of the components in an image  |

Figure 31.1-1 shows the schematic diagram of JPEG bitstream format. In this diagram, the dashed lines mark the structural composition of the corresponding parts of the bitstream, and the orange blocks indicate the marker codes.

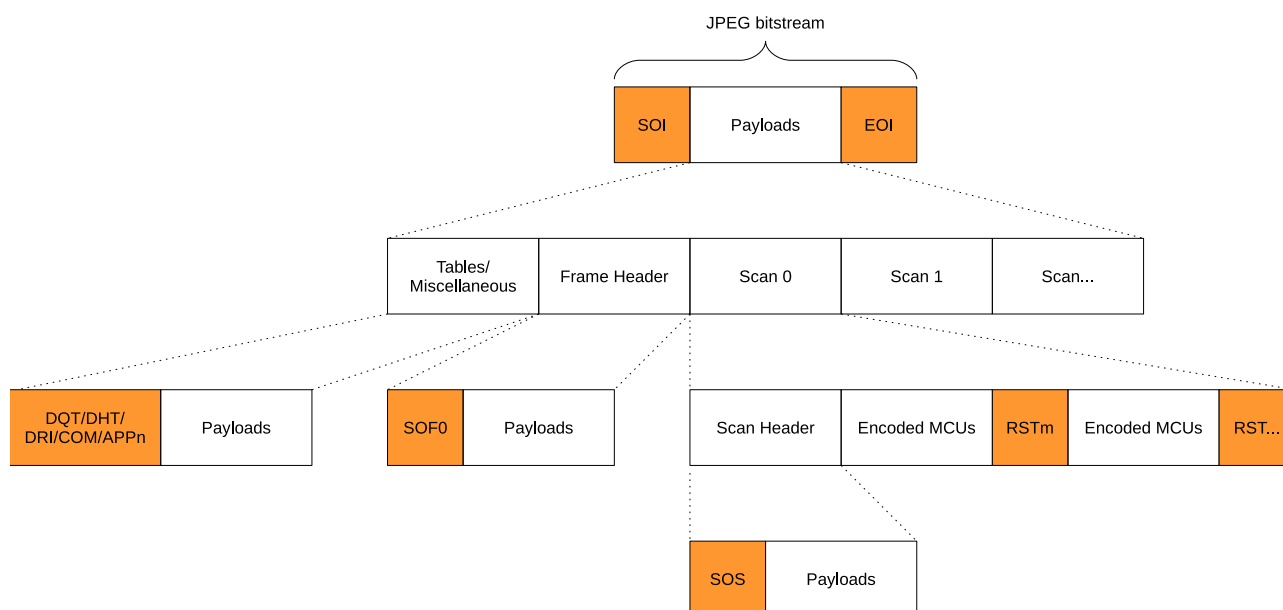


Figure 31.1-1. JPEG Bitstream Format

The marker code assignments are shown in Table 31.1-2.

Table 31.1-2. Marker Code Assignments

| Code Assignment | Marker | Description                                      |
|-----------------|--------|--|
| 0xFFC0          | SOF0   | Start of frame (Baseline DCT)                    |
| 0xFFC4          | DHT    | Define Huffman table(s)                          |
| 0xFFDm          | RSTm   | Restart with modulo 8 count “m”                  |
| 0xFFD8          | SOI    | Start of image                                   |
| 0xFFD9          | EOI    | End of image                                     |
| 0xFFDA          | SOS    | Start of scan                                    |
| 0xFFDB          | DQT    | Define quantization table(s)                     |
| 0xFFDD          | DRI    | Define restart interval                          |
| 0xFFEn          | APPn   | Reserved for application segments, “n” is 0 to F |
| 0xFFFE          | COM    | Comment  |

## 31.2 Introduction

The JPEG codec is based on the JPEG baseline standard, which specifies that an encoding process is completed through one or more scans. A scan contains one or more MCUs. MCU is the sequence of data units defined by the sampling factors of the image components in the scan, which means MCU of different image formats contains different sequence of data units, as shown in Table 31.2-1.

Table 31.2-1. The Number of Data Units in the MCU of Different Image Format

| Image Format | MCU <sup>1</sup>      |                         |                         |
|--------------|-----------------------|-------------------------|-------------------------|
|              | Luminance Component Y | Chrominance Component U | Chrominance Component V |
| YUV444       | 1 x 1                 | 1 x 1                   | 1 x 1                   |

|        |       |       |       |
|--------|-------|-------|-------|
| YUV422 | 2 x 1 | 1 x 1 | 1 x 1 |
| YUV420 | 2 x 2 | 1 x 1 | 1 x 1 |
| GRAY   | 1 x 1 | none  | none  |

<sup>1</sup> The MCU of each image format is represented by the number of data units in the horizontal direction x the number of data units in the vertical direction of each component.

At a time, the JPEG codec can only be configured as an encoder or a decoder, that is, it cannot work as an encoder and a decoder at the same time.

- When used as an encoder, it obtains the image to be compressed through 2D DMA and sends the encoded bitstream to the 2D DMA.
- When used as a decoder, it obtains the coded bitstream through 2D DMA and sends the decoded image to 2D DMA.

The workflow of JPEG codec is shown in Figure 31.2-1.

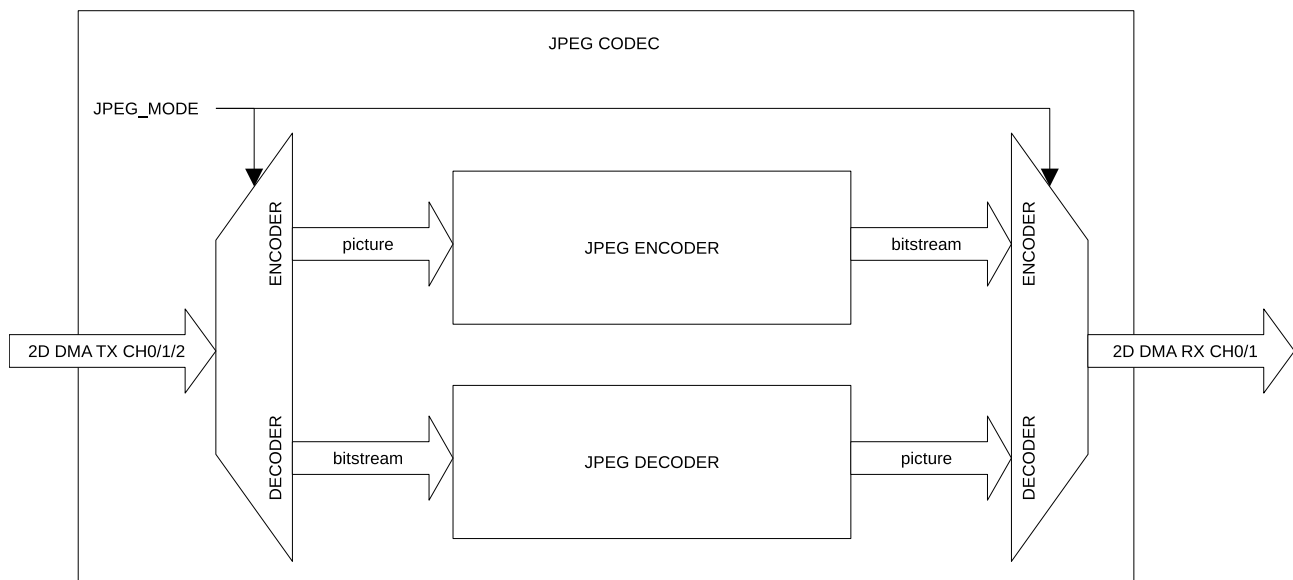


Figure 31.2-1. JPEG codec system connection block diagram

The function clock of the JPEG codec is SYS\_CLK.

## 31.3 Features

When used as an encoder, the JPEG codec has the following features:

- integrated discrete cosine transform algorithm
- integrated canonical Huffman coding
- RGB888, RGB565, YUV422 and GRAY as original input image formats
- conversion of RGB888 and RGB565 into YUV444, YUV422 or YUV420 (the only formats supported by impression) for image compression

- 4 x configurable quantization coefficient tables with 8-bit or 16-bit precision
- performance:
  - still image compression: up to 4K resolution
  - dynamic image compression: up to 1080P@40fps, 720P@70fps (excluding header encoding time)
- automatically added stuffed zero byte
- automatically added EOI marker

When used as a decoder, the JPEG codec has the following features:

- integrated inverse discrete cosine transform algorithm
- integrated Huffman decoding
- supported image formats for compressed bitstream decoding: YUV444, YUV422, YUV420, and GRAY.
- 4 x configurable quantization coefficient tables with 8-bit or 16-bit precision
- 2 x DC and 2 x AC Huffman tables
- supports image decoding of any resolution. However, the resolution of output decoded image differs from the format of the input image:
  - YUV444, GRAY: both the horizontal and vertical resolutions of the output decoded image are multiples of 8, i.e., 150 × 150 images with an output resolution of 152 × 152
  - YUV422: the horizontal resolution of the output decoded image is the multiples of 16 and the vertical resolution is multiples of 8, i.e., 150 × 150 images with an output resolution of 160 × 152
  - YUV420: both the horizontal and vertical resolutions of the output decoded image are multiples of 16, i.e., 150 × 150 images with an output resolution of 160 × 160
- performance:
  - still image decoding: up to 4K resolution
  - dynamic image decoding: up to 1080P@40fps, 720P@70fps (excluding header parsing time)

## 31.4 Architectural Overview

When the JPEG codec is configured as an encoder, its architecture is shown in Figure 31.4-1.

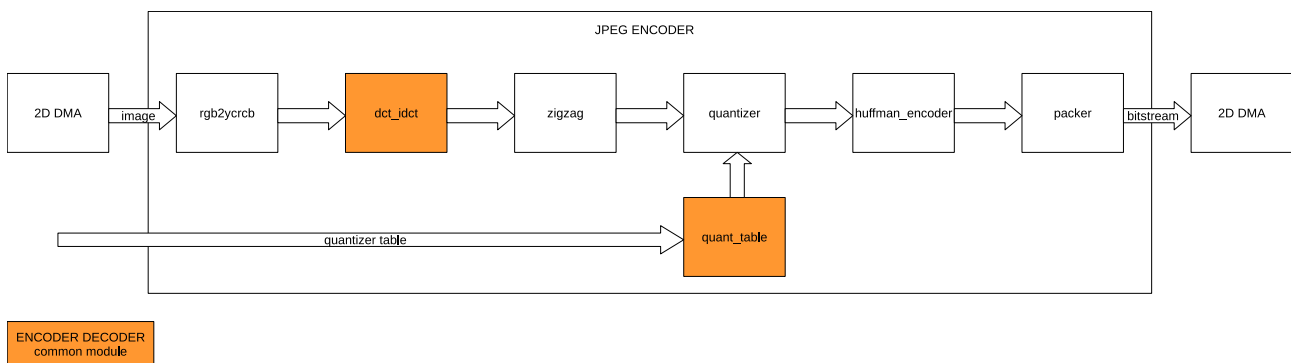


Figure 31.4-1. JPEG encoder architecture

- **rgb2ycrcb** implements the color space conversion, and converts the original image into an image format supported by the codec for compressing.
- **dct\_idct** implements two-dimensional DCT transformation of data units.
- **zigzag** performs zigzag scanning and sorting on the DCT transformed data units.
- **quant\_table** stores the quantization coefficient table delivered by the software.
- **quantizer** quantifies the zigzag sorted data units based on the quantization coefficient table stored in **quant\_table**.
- **huffman\_encoder** performs Huffman encoding on the quantized result of the data units.
- **packer** packs the Huffman-encoded data into groups of 32 bits, and outputs the final encoded bitstream.

When the JPEG codec is configured as a decoder, its architecture is shown in figure 31.4-2.

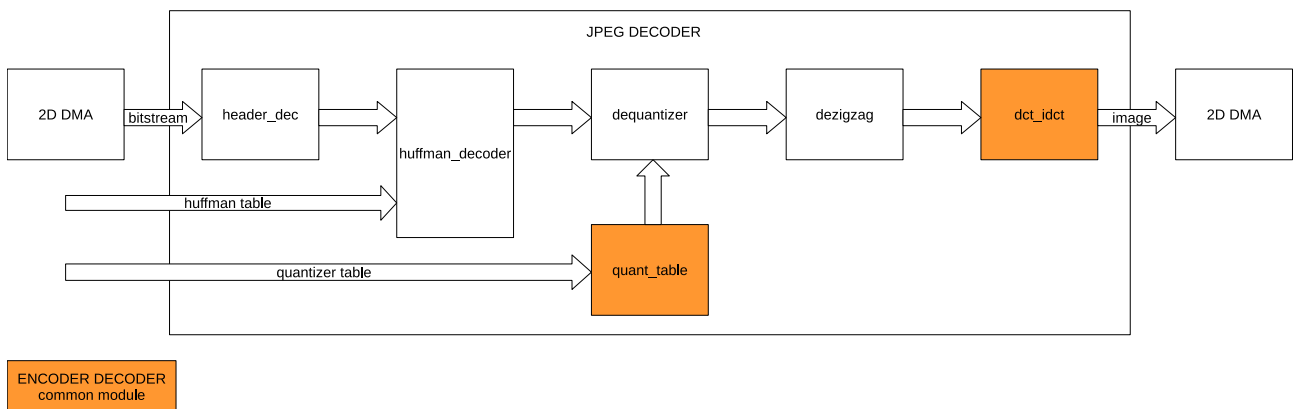


Figure 31.4-2. JPEG decoder architecture

- **header\_dec** implements bitstream extraction and marker SOS and EOI parsing, and controls the decoding process.
- **huffman\_decoder** stores the Huffman table delivered by the software, and implements Huffman decoding of the bitstream.
- **quant\_table** stores the quantization coefficient table delivered by the software.
- **dequantizer** dequantizes the Huffman decoded data based on the quantization coefficient table stored in **quant\_table**.
- **dezigzag** implements reverse zigzag scanning and sorting on the dequantized data units, and combines them into dequantized data units
- **dct\_idct** implements the two-dimensional inverse DCT transformation of the dequantized data units, and outputs the final decoded data units.

Since the JPEG codec cannot be used as an encoder and decoder at the same time, the encoder and decoder share the **quant\_table** and **dct\_idct** modules to save hardware resources.

## 31.5 Functional Description

The JPEG Codec can be configured to work as an encoder or a decoder.

## 31.5.1 JPEG Encoder

### 31.5.1.1 Pause

The JPEG encoder can be paused during the operation for other higher priority tasks. This feature is controlled by register field [JPEG\\_PAUSE\\_EN](#).

- Set [JPEG\\_PAUSE\\_EN](#) to 1, the JPEG encoder will no longer output the bitstream to the 2D DMA RX channel.
- Set [JPEG\\_PAUSE\\_EN](#) back to 0, the JPEG encoder will be resumed, and output the bitstream normally.

### 31.5.1.2 Color Space Conversion

According to the standard, the image formats supported by the JPEG encoder are YUV444, YUV422, YUV420, and GRAY. However, ESP32-P4's JPEG encoder has integrated a color space conversion function to convert RGB888 and RGB565 formats into the above-mentioned image formats supported by the encoder before encoding. In this way, the range of supported image formats is expanded.

The color space conversion formulas for converting RGB to YUV is:

$$\begin{aligned}
 Y &= (0.299 * R) + (0.587 * G) + (0.114 * B) \\
 U &= (-0.1687 * R) + (-0.3313 * G) + (0.5 * B) + 128 \\
 V &= (0.5 * R) + (-0.4187 * G) + (-0.0813 * B) + 128
 \end{aligned}$$

The image format before conversion is represented by its format as well as pixel order. Table [31.5-1](#) demonstrates the representations of the supported image formats for color space conversion:

**Table 31.5-1. Supported Image Formats for Color Space Conversion**

| <a href="#">JPEG_COLOR_SPACE</a> | Format <sup>1</sup> | <a href="#">JPEG_PIXEL_REV</a> | Pixel Order |
|----------------------------------|---------------------|--------------------------------|-------------|
| 0                                | RGB888              | 0                              | RGB         |
|                                  |                     | 1                              | BGR         |
| 1                                | YUV422 <sup>2</sup> | 0                              | YUYV        |
|                                  |                     | 1                              | UYVY        |
| 2                                | RGB565              | 0                              | RGB         |
|                                  |                     | 1                              | BGR         |
| 3                                | GRAY <sup>2</sup>   | N/A                            | YYY         |

<sup>1</sup> The image formats can be converted into other formats supported by the encoder via configuring register field [JPEG\\_SAMPLE\\_SEL](#):

- 0: YUV444
- 1: YUV422
- 2: YUV420

<sup>2</sup> Image formats YUV422 and GRAY will not be converted, regardless of the value of [JPEG\\_SAMPLE\\_SEL](#).

### 31.5.1.3 Configurable Quantization Coefficient Table

ESP32-P4 JPEG encoder has implemented four 8 x 8 quantization coefficient tables in its hardware, which allows 64 software-configurable coefficient values per table.



The precision of each quantization table is configurable via [JPEG\\_QNR\\_PRECISION](#):

- 0: low 8-bit effective
- 1: low 16-bit effective

The coefficient values for each table can be configured in FIFO mode or non-FIFO mode depending on the value of [JPEG\\_QNR\\_FIFO\\_EN](#):

- 0: non-FIFO mode, in which each coefficient is written to a specific address
- 1: FIFO mode, in which all coefficients are written to the same address

**Table 31.5-2. Position Number of Coefficients in a Quantization Coefficient Table (Example)**

|     |    |    |    |    |    |    |    |
|-----|----|----|----|----|----|----|----|
| 0   | 1  | 2  | 3  | 4  | 5  | 6  | 7  |
| 8   | 9  | 10 | 11 | 12 | 13 | 14 | 15 |
| ... |    |    |    |    |    |    |    |
| 56  | 57 | 58 | 59 | 60 | 61 | 62 | 63 |

In different modes, the configuration of the quantization coefficient table is different. Note,  $n$  ( $n = 0, 1, 2, 3$ ) indicates the number of each quantization coefficient table:

- non-FIFO mode: each quantization coefficient in a specific position of a quantization coefficient table  $n$  must be written to a specific address, which is (JPEG codec base address +  $n * 0x100 + \text{quantization coefficient position number} * 0x4$ ), in which the *quantization coefficient position number* can be 0, 1, 2, ..., 63 (see Table 31.5-2). In this mode, since each coefficient is written to a specific address, configuring the 64 quantization coefficients in sequence is not required.
- FIFO mode: all 64 quantization coefficients of the quantization table  $n$  are written to the same address, which is [JPEG\\_TnQNR\\_REG](#). In this mode, since all coefficients are written to the same address, configuring the 64 quantization coefficients one by one in sequence is required. Afterwards, the hardware will automatically store these 64 quantization coefficients in sequence as shown in Table 31.5-2.

If there are less than 4 quantization tables, the corresponding quantization table will not be written.

To use a specific quantization coefficient table  $n$  for the luminance component or the chrominance component, just set the corresponding register fields to  $n$ :

- luminance component: [JPEG\\_LQNR\\_TBL\\_SEL](#)
- chrominance component: [JPEG\\_CQNR\\_TBL\\_SEL](#)

The JPEG baseline standard recommended 8-bit precision quantization coefficient tables for the luminance component and the chrominance component are shown in Table 31.5-3 and Table 31.5-4.

**Table 31.5-3. Recommended 8-bit Precision Quantization Coefficient Table for the Luminance Component**

|    |    |    |    |    |     |     |    |
|----|----|----|----|----|-----|-----|----|
| 16 | 11 | 10 | 16 | 24 | 40  | 51  | 61 |
| 12 | 12 | 14 | 19 | 26 | 58  | 60  | 55 |
| 14 | 13 | 16 | 24 | 40 | 57  | 69  | 56 |
| 14 | 17 | 22 | 29 | 51 | 87  | 80  | 62 |
| 18 | 22 | 37 | 56 | 68 | 109 | 103 | 77 |
| 24 | 35 | 55 | 64 | 81 | 104 | 113 | 92 |

|    |    |    |    |     |     |     |     |
|----|----|----|----|-----|-----|-----|-----|
| 49 | 64 | 78 | 87 | 103 | 121 | 120 | 101 |
| 72 | 92 | 95 | 98 | 112 | 100 | 103 | 99  |

**Table 31.5-4. Recommended 8-bit Precision Quantization Coefficient Table for the Chrominance Component**

|    |    |    |    |    |    |    |    |
|----|----|----|----|----|----|----|----|
| 17 | 18 | 24 | 47 | 99 | 99 | 99 | 99 |
| 18 | 21 | 26 | 66 | 99 | 99 | 99 | 99 |
| 24 | 26 | 56 | 99 | 99 | 99 | 99 | 99 |
| 47 | 66 | 99 | 99 | 99 | 99 | 99 | 99 |
| 99 | 99 | 99 | 99 | 99 | 99 | 99 | 99 |
| 99 | 99 | 99 | 99 | 99 | 99 | 99 | 99 |
| 99 | 99 | 99 | 99 | 99 | 99 | 99 | 99 |
| 99 | 99 | 99 | 99 | 99 | 99 | 99 | 99 |

More information can be found in [ITU T.81 Recommendation](#). Adjusting the quantization table can change the compression ratio (the ratio between the uncompressed image size and compressed image size) and the quality of encoded images (the larger the quantization coefficient, the greater the compression ratio and the worse the image quality).

#### 31.5.1.4 Stuffed Zero Byte

As required in the JPEG baseline standard to avoid any marker within a Huffman-coded segment, any 0xFF byte generated by the Huffman coding should be followed by a “stuffed” zero byte.

JPEG encoder has implemented a mechanism to automatically add this “stuffed” 0x00 byte after each 0xFF byte in the Huffman-coded segment of bitstream.

Users can configure whether to add 0x00 byte after each 0xFF byte via [JPEG\\_FF\\_CHECK\\_EN](#):

- 0: not add
- 1: add (by default)

#### 31.5.1.5 EOI Marker

The end of Image (EOI) marker is used to mark the end of the bitstream of a compressed image. The EOI marker code is 0xFFD9.

JPEG encoder has implemented a mechanism to automatically add the EOI marker at the end of the bitstream.

Users can configure whether to add EOF marker via [JPEG\\_TAILER\\_EN](#):

- 0: not add
- 1: add

### 31.5.2 JPEG Decoder

The information in the bitstream must be parsed by the software, then sent to the hardware through the APB configuration bus. Note that the hardware does not support parsing any marker segments, except the SOS,

RST and EOI marker segments.

### 31.5.2.1 Multiple Chrominance Components

The frame header contains information about the number of chrominance components of the image, the ID of each component, and the sampling factors in the horizontal and vertical directions of each component.

JPEG decoder's software must parse such information and pass it to respective registers

[JPEG\\_COMPONENT\\_NUM](#), [JPEG\\_Cn\\_ID](#), [JPEG\\_Cn\\_X\\_FACTOR](#), and [JPEG\\_Cn\\_Y\\_FACTOR](#). Here, *n* can be 0, 1, 2, indicating that up to 3 chrominance components are supported by hardware. Note that if less than 3 components are involved, just do not configure the rest of the registers.

According to the value of register [JPEG\\_Cn\\_ID](#) of each chrominance component, the hardware will check whether it is consistent with the ID in the scan header information. The sampling factor indicates the number of data units of this component that an MCU contains in both the horizontal and vertical directions. So according to the value of register [JPEG\\_COMPONENT\\_NUM](#), [JPEG\\_Cn\\_X\\_FACTOR](#) and [JPEG\\_Cn\\_Y\\_FACTOR](#), the hardware can obtain the proportional relationship of chrominance components, that is, the format of the image to be decoded. See Table 31.5-5.

**Table 31.5-5. Sampling Factor and Image Format**

| <a href="#">JPEG_COMPONENT_NUM</a> | <a href="#">JPEG_Cn_X/Y_FACTOR</a>   | Format of the Image to be Decoded |
|------------------------------------|--|-----------------------------------|
| 0                                  | -  | invalid                           |
| 1                                  | CO_X_FACTOR is 1<br>CO_Y_FACTOR is 1   | GRAY                              |
| 2                                  | -  | invalid                           |
| 3                                  | CO_X_FACTOR is 1<br>CO_Y_FACTOR is 1<br>C1_X_FACTOR is 1<br>C1_Y_FACTOR is 1<br>C2_X_FACTOR is 1<br>C2_Y_FACTOR is 1 | YUV444                            |
|                                    | CO_X_FACTOR is 2<br>CO_Y_FACTOR is 1<br>C1_X_FACTOR is 1<br>C1_Y_FACTOR is 1<br>C2_X_FACTOR is 1<br>C2_Y_FACTOR is 1 | YUV422                            |
|                                    | CO_X_FACTOR is 2<br>CO_Y_FACTOR is 2<br>C1_X_FACTOR is 1<br>C1_Y_FACTOR is 1<br>C2_X_FACTOR is 1<br>C2_Y_FACTOR is 1 | YUV420                            |

Regardless of the format of the image to be decoded, the decoder only supports one scan, which contains all components. After decoding, the image will be sent to 2D DMA, so please refer to Chapter 5 [2D-DMA Controller \(2D-DMA\)](#) for the layout of the decoded image in each format.

### 31.5.2.2 Parsing RST Marker

The bitstream may have a restart (RST) marker in the scan segment. The RST marker code is 0xFFD $x$  ( $x = 0, 1, \dots, 7$ ).

JPEG decoder's hardware can parse RST markers and check whether the actual number of MCUs between two RST markers is the same as the restart interval defined in the DRI segment of the Tables/Miscellaneous segment.

Firstly, the software parses the DRI segment and pass the defined restart interval to register [JPEG\\_RESTART\\_INTERVAL](#). Then, the hardware will check whether the subsequent bitstream has an RST marker every time [JPEG\\_RESTART\\_INTERVAL](#) MCUs are decoded.

Configuring [JPEG\\_RESTART\\_INTERVAL](#) to 0 indicates the bitstream does not contain any RST marker. In this case, the hardware will not check RST markers.

### 31.5.2.3 Configurable Quantization Coefficient Table

ESP32-P4 JPEG decoder also supports 4 configurable quantization coefficient tables. Since the JPEG codec cannot be used as an encoder and decoder at the same time, decoder can share the same four configurable quantization coefficient tables with the encoder to save hardware resources.

Therefore, the configuration of decoder's quantization coefficient tables is similar to that of the encoder (see Section [31.5.1.3](#)) with some exceptions described below:

- The software needs to parse the DQT segment in the Tables/Miscellaneous segment to obtain the quantization coefficient tables of the decoder. The recommended quantization coefficient tables are the same as the encoder shown in Table [31.5-3](#) and Table [31.5-4](#).
- The precision of the quantization table $n$  is configured via higher 4 bits of register [JPEG\\_T \$n\$ \\_DQT\\_INFO](#):
  - 0: low 8-bit effective
  - 1: low 16-bit effective

The precision is also obtained from the DQT segment in the Tables/Miscellaneous segment.

- For each chrominance component, a different quantization coefficient table can be selected. The lower 4 bits of register [JPEG\\_T \$n\$ \\_DQT\\_INFO](#) specify the ID of each quantization coefficient table, and each chrominance component selects the quantization coefficient table whose ID is the value of register [JPEG\\_C \$n\$ \\_DQT\\_TBL\\_SEL](#). The ID of each quantization coefficient table is also obtained from the DQT segment in the Tables/Miscellaneous segment.

### 31.5.2.4 Configurable Huffman Table

ESP32-P4 supports up to 2 DC Huffman tables and 2 AC Huffman tables. Users can configure as many Huffman tables as needed within the limits.

Each Huffman table can be established with three types of information, which can be obtained from the DHT segment in the Tables/Miscellaneous segment:

- the number of codeword with a codeword length of 1 to 16 bits,
- the symbols corresponding to the decoded codeword
  - DC table: up to 16 symbols

- AC table: up to 256 symbols
- the minimum codeword with a codeword length of 1 to 16 bits.

Both of the DC and AC Huffman tables can be configured in a FIFO fashion or a non-FIFO fashion depending on the value of `JPEG_DHT_FIFO_EN`:

- 0: non-FIFO mode
- 1: FIFO mode

In different modes, the configuration of the Huffman table is different. Here is the configuration of DC tables $n$  ( $n = 0, 1$ ):

- non-FIFO mode: each piece in different type of information used to establish the DC $n$  Huffman table must be written to a specific address.
  - the number of codeword with a codeword length of 1 to 16 bits: JPEG codec base address + 0x500 +  $n * 0x80 + (\text{codeword length} - 1) * 0x4$ , in which *codeword length* = 1, 2, ..., 16.
  - the symbols corresponding to the decoded codeword: JPEG codec base address + 0x600 +  $n * 0x40 + \text{symbol number} * 0x4$ , in which *symbol number* = 0, 1, ..., 15.
  - the minimum codeword with a codeword length of 1 to 16 bits: JPEG codec base address + 0xF00 +  $n * 0x80 + (\text{codeword length} - 1) * 0x4$ , in which *codeword length* = 1, 2, ..., 16.

In this mode, since each piece of different type of information is written to a specific address, configuring each piece of information in sequence is not required.

- FIFO mode: all pieces of the same type of information used to establish the DC $n$  Huffman table must be written to the same address, respectively.
  - the number of codeword with a codeword length of 1 to 16 bits: `JPEG_DHT_TOTLEN_DC $n$ _REG`.
  - all symbols corresponding to the decoded codeword (DC table has up to 16 symbols): `JPEG_DHT_VAL_DC $n$ _REG`.
  - the minimum codeword with a codeword length of 1 to 16 bits: `JPEG_DHT_CODEMIN_DC $n$ _REG`.

In this mode, since all pieces of the same type of information are written to the same address, configuring each piece of same type of information one by one in sequence is required. Afterwards, the hardware will automatically store such information in sequence.

The configuration of AC $n$  ( $n = 0, 1$ ) tables is very similar to that of the DC $n$  ( $n = 0, 1$ ) tables. Here below is the configuration of AC $n$  ( $n = 0, 1$ ) tables:

- non-FIFO mode: each piece in different type of information used to establish the AC $n$  Huffman table must be written to a specific address.
  - the number of codeword with a codeword length of 1 to 16 bits: JPEG codec base address + 0x540 +  $n * 0x80 + (\text{codeword length} - 1) * 0x4$ , in which *codeword length* = 1, 2, ..., 16.
  - the symbols corresponding to the decoded codeword: JPEG codec base address + 0x680 +  $n * 0x400 + \text{symbol number} * 0x4$ , in which *symbol number* = 0, 1, ..., 256.
  - the minimum codeword with a codeword length of 1 to 16 bits: JPEG codec base address + 0xF40 +  $n * 0x80 + (\text{codeword length} - 1) * 0x4$ , in which *codeword length* = 1, 2, ..., 16.

In this mode, since each piece of different type of information is written to a specific address, configuring each piece of information in sequence is not required.

- FIFO mode: all pieces of the same type of information used to establish the AC $n$  Huffman table must be written to the same address, respectively.
  - the number of codeword with a codeword length of 1 to 16 bits: `JPEG_DHT_TOTLEN_AC $n$ _REG`.
  - all symbols corresponding to the decoded codeword (AC table has up to 256 symbols): `JPEG_DHT_VAL_AC $n$ _REG`.
  - the minimum codeword with a codeword length of 1 to 16 bits: `JPEG_DHT_CODEMIN_AC $n$ _REG`.

In this mode, since all pieces of the same type of information are written to the same address, configuring each piece of same type of information one by one in sequence is required. Afterwards, the hardware will automatically store such information in sequence.

For the minimum codeword with a codeword length of 1 to 16 bits, it should be moved left to the high bit of the 16-bit configuration data. If a codeword length does not exist, the configuration value is 0xFFFF. For example, if a minimum codeword is 0x7C, the 16-bit configuration data should be 0x7C00.

The JPEG baseline standard recommended DC and AC Huffman tables can be found in [ITU T.81 Recommendation](#).

The software can obtain the IDs of DC $n$  and AC $n$  Huffman tables by parsing the DHT segment in the Tables/Miscellaneous segment, then pass these ID to the corresponding register `JPEG_DC $n$ _DHT_ID` and `JPEG_AC $n$ _DHT_ID`.

The hardware will automatically use the DC $n$  and AC $n$  Huffman tables with the same ID from `JPEG_DC $n$ _DHT_ID` and `JPEG_AC $n$ _DHT_ID`.

### 31.5.2.5 Timeout Detection

Additionally, timeout detection is supported when the JPEG codec is working as a decoder. The hardware triggers the timeout interrupt `JPEG_DECODE_TIMEOUT_INT`:

- when the decoder stops reading the bitstream for more than  $(2^{JPEG\_DECODE\_TIMEOUT\_THRES} - 1)$  clock cycles,
- or when the number of clock cycles consumed for decoding an image exceeds the value of  $(2^{JPEG\_DECODE\_TIMEOUT\_THRES} - 1)$

In this case, the decoder will be reset depending on the configuration of `JPEG_DECODE_TIMEOUT_TASK_SEL`:

- 0: the hardware will not perform any operation, and the software is required to configure the `JPEG_SOFT_RST` or `JPEG_FSM_RST` to perform a reset operation.
- 1: the hardware will automatically reset the decoder to exit the timeout state and enter the initial state.

## 31.6 Interrupts

ESP32-P4's JPEG Codec can generate the `JPEG_INTR` interrupt signal that will be sent to the [Interrupt Matrix](#).

Interrupt signal JPEG\_INTR can be generated by the following internal interrupt sources:

- JPEG\_DONE\_INT: Triggered when a frame of image encoding or decoding ends.
- JPEG\_RLE\_PARALLEL\_ERR\_INT: Triggered when a run-length encoding error occurs.
- JPEG\_CID\_ERR\_INT: Triggered when the decoded component ID is different from the component ID configured by the software.
- JPEG\_C\_DHT\_DC\_ID\_ERR\_INT: Triggered when the decoded DC Huffman table ID of each component is not the software configured DCO Huffman table ID or DC1 Huffman table ID.
- JPEG\_C\_DHT\_AC\_ID\_ERR\_INT: Triggered when the decoded AC Huffman table ID of each component is not the software configured ACO Huffman table ID or AC1 Huffman table ID.
- JPEG\_C\_DQT\_ID\_ERR\_INT: Triggered when the decoded quantization table ID of each component is different from the software configured quantization table ID.
- JPEG\_RST\_UXP\_ERR\_INT: Triggered when the [JPEG\\_RESTART\\_INTERVAL](#) configured by the software is 0 but the RST marker is parsed by the decoder.
- JPEG\_RST\_CHECK\_NONE\_ERR\_INT: Triggered when the [JPEG\\_RESTART\\_INTERVAL](#) configured by the software is non-0 but the RST marker cannot be parsed by the decoder.
- JPEG\_RST\_CHECK\_POS\_ERR\_INT: Triggered when the MCU number between two parsed RST markers is not equal to the [JPEG\\_RESTART\\_INTERVAL](#) configured by the software.
- JPEG\_OUT\_EOF\_INT: Triggered when the EOF marker is read from the TX channel of 2D DMA.
- JPEG\_SR\_COLOR\_MODE\_ERR\_INT: This interrupt is invalid.
- JPEG\_DCT\_DONE\_INT: Triggered when the DCT or IDCT calculation of one data unit is completed.
- JPEG\_BS\_LAST\_BLOCK\_EOF\_INT: Triggered when the encoding of the last data unit is completed.
- JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT: Triggered when an image frame has multiple scans to be decoded and the SOS marker is not parsed within ([JPEG\\_SOS\\_CHECK\\_BYTE\\_NUM](#) + 1) bytes in any scan header information.
- JPEG\_SCAN\_CHECK\_POS\_ERR\_INT: Triggered when the position of the scan header information parsed by the decoder is wrong.
- JPEG\_UXP\_DET\_INT: Triggered when the marker parsed by the decoder is not supported by the hardware.
- JPEG\_EN\_FRAME\_EOF\_ERR\_INT: Triggered when the number of data units to be encoded read from 2D DMA is less than the number of data units calculated based on the image resolution configured by the software.
- JPEG\_EN\_FRAME\_EOF\_LACK\_INT: Triggered when a frame of image to be encoded is completely read from 2D DMA but the EOF marker is not read.
- JPEG\_DE\_FRAME\_EOF\_ERR\_INT: Triggered when the number of data units obtained after decoding a frame of image is different from the number of data units calculated based on the image resolution configured by the software.
- JPEG\_DE\_FRAME\_EOF\_LACK\_INT: Triggered when the bitstream of a image is completely read from 2D DMA but the EOF marker or EOI marker is not read.

- **JPEG\_SOS\_UNMATCH\_ERR\_INT**: Triggered when the number of components in the scan header information parsed by the decoder is 0 or the header length in the scan header information parsed by the decoder does not match the actual header length.
- **JPEG\_MARKER\_ERR\_FST\_SCAN\_INT**: Triggered when there is an error in the first scan header information parsed by the decoder. The errors include errors triggering **JPEG\_CID\_ERR\_INT**, errors triggering **JPEG\_C\_DHT\_DC\_ID\_ERR\_INT**, errors triggering **JPEG\_C\_DHT\_AC\_ID\_ERR\_INT**, errors triggering **JPEG\_C\_DQT\_ID\_ERR\_INT** and errors triggering **JPEG\_SOS\_UNMATCH\_ERR\_INT**.
- **JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT**: Triggered when there is an error in the non-first scan header information parsed by the decoder. The error type is the same as the errors that trigger **JPEG\_MARKER\_ERR\_FST\_SCAN\_INT**.
- **JPEG\_UNDET\_INT**: Triggered when the bitstream of an image is completely read from 2D DMA but the SOS marker is not read.
- **JPEG\_DECODE\_TIMEOUT\_INT**: Triggered when the decoder is timeout. Section [31.7.2](#) describes how this interrupt will occur.

The above interrupt sources can only be triggered when the interrupt enable register *interrupt\_source\_name*\_ENA is set to 1. Write 1 to *interrupt\_source\_name*\_CLR will clear the interrupt.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [31.8 Register Summary](#).

## 31.7 Programming Procedures

### 31.7.1 JPEG Encoder

When the JPEG codec is working as an encoder, the configuration process is:

1. Activate the JPEG codec:
  - Set [HP\\_SYS\\_CLKRST\\_JPEG\\_SYS\\_CLK\\_EN](#) to 1 to enable the JPEG codec clock;
  - Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_JPEG](#) to 0 to release the JPEG codec system level reset.
2. Configure the JPEG codec:
  - Set [JPEG\\_SOFT\\_RST](#) to 1 to reset the JPEG codec, and then set [JPEG\\_SOFT\\_RST](#) to 0 to release the JPEG codec reset.
  - Set [JPEG\\_MODE](#) to 0 to configure the JPEG codec to be used as an encoder.
  - Select the original image format by configuring the following two registers:
    - Format: [JPEG\\_COLOR\\_SPACE](#)
    - Pixel order: [JPEG\\_PIXEL\\_REV](#)



See details in Table 31.5-1.

- Select whether to add the EOI marker (0xFFD9) at the end of the bitstream by configuring [JPEG\\_TAILER\\_EN](#):
  - 0: disable
  - 1: enable
- Select the image format to be compressed by configuring [JPEG\\_SAMPLE\\_SEL](#):
  - 0: YUV444
  - 1: YUV422
  - 2: YUV420

Note that this register is valid only when the original image format is RGB. See details in Table 31.5-1.

- Configure [JPEG\\_HA](#) as the original image width and [JPEG\\_VA](#) as the original image height.
- Configure the quantization coefficient table by following the instructions in Section 31.5.1.3.

### 3. Configure 2D DMA (For detailed instructions or introduction to related concepts, please refer to Chapter 5 *2D-DMA Controller (2D-DMA)*.)

#### (a) Configure the linked list of 2D DMA TX channel.

- Set 2DEN to 1 to enable 2D function.
- Configure the Buffer address pointer as the starting address where the original image is stored.
- Configure pbyte to select the number of bytes of one pixel of the original image.
- Configure HA as the width of the original image and VA as the height of the original image.
- Configure hb as the number of pixels in the horizontal direction of an image block and vb as the number of pixels in the vertical direction of an image block.
- Configure mod as 1, which means continuous reading of image blocks of hb × vb size.
- Configure (X, Y) as the coordinate of the first pixel in the starting image block. Among them, according to the original image format and the format of the image to be compressed, there are restrictions on hb and vb, as shown in the table 31.7-1:

**Table 31.7-1. JPEG Encoder hb and vb Configuration**

| Format of Original Image | Format of the Image to be Compressed | hb              | vb              |
|--------------------------|--------------------------------------|-----------------|-----------------|
| RGB                      | YUV444                               | Multiples of 8  | Multiples of 8  |
| RGB                      | YUV422                               | Multiples of 16 | Multiples of 8  |
| RGB                      | YUV420                               | Multiples of 16 | Multiples of 16 |
| YUV422                   | YUV422                               | Multiples of 16 | Multiples of 8  |
| GRAY                     | GRAY                                 | Multiples of 8  | Multiples of 8  |

#### (b) Configure the linked list of the 2D DMA RX channel:

- Set 2DEN to 0 to enable 1D function.

- Configure the Buffer address pointer as the starting address where the encoded bitstream will be stored.
  - Configure size as the number of bytes in the space to store the encoded bitstream.
  - configure mod as 0, which means one-time reading of image blocks of  $hb \times vb$  size.
- (c) Connect 2D DMA channels to JPEG codec:
- Connect the TX channel  $n$  to the JPEG codec by configuring `DMA2D_OUT_PERI_SEL_CHn` to 0;
  - Connect the RX channel  $n$  to the JPEG codec by configuring `DMA2D_IN_PERI_SEL_CHn` to 0.
- (d) Reset 2D DMA channels:
- 2D DMA TX channel  $n$ : Set `DMA2D_OUT_RST_CHn` to 1 to reset 2D DMA TX channel  $n$ , then set `DMA2D_OUT_RST_CHn` to 0 to release the reset of 2D DMA TX channel  $n$ .
  - 2D DMA RX channel  $n$ : Set `DMA2D_IN_RST_CHn` to 1 to reset 2D DMA RX channel  $n$ , then set `DMA2D_IN_RST_CHn` to 0 to release the reset of 2D DMA RX channel  $n$ .
- (e) Select the burst length of 2D DMA channels:
- Configure `DMA2D_OUT_MEM_BURST_LENGTH_CHn` to select the burst length of 2D DMA TX channel  $n$ .
  - Configure `DMA2D_IN_MEM_BURST_LENGTH_CHn` to select the burst length of 2D DMA RX channel  $n$ .
- (f) Select the 2D DMA output image block size by configuring `DMA2D_OUT_MACRO_BLOCK_SIZE_CHn` according to the format of original image and the format of the image to be compressed. See details in Table 31.7-2:
- 0: 8x8
  - 1: 16x8
  - 2: 16x16

Table 31.7-2. `DMA2D_OUT_MACRO_BLOCK_SIZE_CHn` Configuration

| Format of Original Image | Format of the Image to be Compressed | <code>DMA2D_OUT_MACRO_BLOCK_SIZE_CHn</code> |
|--------------------------|--------------------------------------|---|
| RGB                      | YUV444                               | 0   |
| RGB                      | YUV422                               | 1   |
| RGB                      | YUV420                               | 2   |
| YUV422                   | YUV422                               | 1   |
| GRAY                     | GRAY                                 | 0   |

- (g) Enable the reorder function to improve bandwidth utilization by setting `DMA2D_OUT_REORDER_EN_CHO` to 1. Note that, this function is only available for 2D DMA TX channel0, not for any other TX channels.
- (h) Configure 2D DMA channel linked list address:
- 2D DMA TX channel: `DMA2D_OUTLINK_ADDR_CHn`
  - 2D DMA RX channel: `DMA2D_INLINK_ADDR_CHn`

4. Enable interrupt sources:
  - [DMA2D\\_OUT\\_INT\\_ENA\\_CH \$n\$ \\_REG](#)
  - [DMA2D\\_IN\\_INT\\_ENA\\_CH \$n\$ \\_REG](#)
  - [JPEG\\_INT\\_ENA\\_REG](#)
5. Start the transmission of 2D DMA channels:
  - 2D DMA TX channel: set [DMA2D\\_OUTLINK\\_START\\_CH \$n\$](#)  to 1 and then to 0
  - 2D DMA RX channel: set [DMA2D\\_INLINK\\_START\\_CH \$n\$](#)  to 1 and then to 0
6. Start the JPEG codec encoding by setting the [JPEG\\_JPEG\\_START](#) field.
7. Wait till [DMA2D\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#) becomes 1, indicating that the encoded bitstream has been completely written to the memory.

## 31.7.2 JPEG Decoder

When the JPEG codec is working as a decoder, the configuration process is:

1. Activate the JPEG codec:
  - Set [HP\\_SYS\\_CLKRST\\_JPEG\\_SYS\\_CLK\\_EN](#) to 1 to enable the JPEG codec clock
  - Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_JPEG](#) to 0 to release the JPEG codec system level reset.
2. Configure the JPEG codec:
  - Set [JPEG\\_SOFT\\_RST](#) to 1 to reset the JPEG codec, and then set [JPEG\\_SOFT\\_RST](#) to 0 to release the JPEG codec reset.
  - Set [JPEG\\_MODE](#) to 1 to configure the JPEG codec to be used as a decoder.
  - Enable the RST marker check following the instructions in Section [31.5.2.2](#), if required.
  - Configure the quantization coefficient tables by following the instructions in Section [31.5.2.3](#).
  - Configure the Huffman tables by following the instructions in Section [31.5.2.4](#).
  - Configure the width and height of the decoded image:
    - Width: write width of the decoded image to [JPEG\\_HA](#).
    - Height: write the height of the decoded image to [JPEG\\_VA](#).
    - According to different decoded image formats, [JPEG\\_HA](#) and [JPEG\\_VA](#) must meet the requirements of Table [31.7-3](#).

**Table 31.7-3. JPEG Decoder [JPEG\\_HA](#) and [JPEG\\_VA](#) Configuration**

| Format of Decoded Image | <a href="#">JPEG_HA</a> | <a href="#">JPEG_VA</a> |
|-------------------------|-------------------------|-------------------------|
| YUV444                  | Multiples of 8          | Multiples of 8          |
| YUV422                  | Multiples of 16         | Multiples of 8          |
| YUV420                  | Multiples of 16         | Multiples of 16         |
| GRAY                    | Multiples of 8          | Multiples of 8          |

3. Configure 2D DMA (For detailed instructions or introduction to related concepts, please refer to Chapter [5 2D-DMA Controller \(2D-DMA\)](#).)

(a) Configure the linked list of the 2D DMA TX channel.

- Set 2DEN to 0 to enable the 1D function.
- Configure the Buffer address pointer as the starting address where the bitstream to be decoded is stored.
- Configure the length and size as the number of bytes in the space to store the bitstream to be decoded.
- configure mod as 0, which means one-time reading of image blocks of hb x vb size.

(b) Configure the linked list of 2D DMA RX channel.

- Set 2DEN to 1 to enable 2D function.
- Configure the Buffer address pointer as the starting address where the decoded image will be stored.
- Configure pbyte to select the number of bytes of one pixel of the image which is decoded and has undergone 2D DMA color space conversion.
- Configure HA as the width of the output decoded image, configure VA as the height of the output decoded image, configure hb as the number of pixels in the horizontal direction of an image block, configure vb as the number of pixels in the vertical direction of an image block.
- Configure mod as 1, which means continuous reading of image blocks of hb × vb size.
- Configure (X, Y) as the coordinates of the first pixel in the starting image block. Among them, according to the decoded image format, there are restrictions on hb and vb, as shown in the table [31.7-4](#):

**Table 31.7-4. JPEG Decoder hb and vb Configuration**

| Decoded image format | hb              | vb              |
|----------------------|-----------------|-----------------|
| YUV444               | Multiples of 8  | Multiples of 8  |
| YUV422               | Multiples of 16 | Multiples of 8  |
| YUV420               | Multiples of 16 | Multiples of 16 |
| GRAY                 | Multiples of 8  | Multiples of 8  |

(c) Connect 2D DMA channels to JPEG codec:

- Connect the TX channel *n* to the JPEG codec by configuring [DMA2D\\_OUT\\_PERI\\_SEL\\_CHn](#) to 0;
- Connect the RX channel *n* to the JPEG codec by configuring [DMA2D\\_IN\\_PERI\\_SEL\\_CHn](#) to 0.

(d) Reset 2D DMA channels:

- 2D DMA TX channel *n*: set [DMA2D\\_OUT\\_RST\\_CHn](#) to 1 to reset 2D DMA TX channel *n*, then set [DMA2D\\_OUT\\_RST\\_CHn](#) to 0 to release the reset of 2D DMA TX channel *n*.

- 2D DMA RX channel $n$ : set `DMA2D_IN_RST_CH $n$`  to 1 to reset 2D DMA RX channel $n$ , then set `DMA2D_IN_RST_CH $n$`  to 0 to release the reset of 2D DMA RX channel $n$ .
- (e) Select the burst length of 2D DMA channels:
- Configure `DMA2D_OUT_MEM_BURST_LENGTH_CH $n$`  to select the burst length of 2D DMA TX channel $n$
  - Configure `DMA2D_IN_MEM_BURST_LENGTH_CH $n$`  to select the burst length of 2D DMA RX channel $n$
- (f) Select 2D DMA receive image block size by configuring `DMA2D_IN_MACRO_BLOCK_SIZE_CH $n$`  according to the format of the decoded image. See details in Table 31.7-5:
- 0: 8x8
  - 1: 16x8
  - 2: 16x16

Table 31.7-5. `DMA2D_IN_MACRO_BLOCK_SIZE_CH $n$`  Configuration

| Format of Decoded Image | <code>DMA2D_IN_MACRO_BLOCK_SIZE_CH<math>n</math></code> |
|-------------------------|---|
| YUV444                  | 0   |
| YUV422                  | 1   |
| YUV420                  | 2   |
| GRAY                    | 0   |

- (g) Enable the reorder function to improve bandwidth utilization by setting set `DMA2D_IN_REORDER_EN_CHO` to 1. Note that, this function is only available for 2D DMA RX channel0, not for any other RX channels.
- (h) Select whether to scramble the pixel order of the decoded image before 2D DMA color space conversion by configuring `DMA2D_IN_SCRAMBLE_SEL_PRE_CHO`:
- 0: BYTE2-1-0
  - 1: BYTE2-0-1
  - 2: BYTE1-0-2
  - 3: BYTE1-2-0
  - 4: BYTE0-2-1
  - 5: BYTE0-1-2

Configuring `DMA2D_IN_SCRAMBLE_SEL_PRE_CHO` to 5 means swapping the pixel order, for example, swapping YUV444 output by the JPEG decoder to VUY444. Note that, this function is only available for 2D DMA RX channel0, not for any other RX channels.

- (i) Select the color conversion methods by configuring `DMA2D_IN_COLOR_INPUT_SEL_CHO`, `DMA2D_IN_COLOR_3B_PROC_EN_CHO`, and `DMA2D_IN_COLOR_OUTPUT_SEL_CHO`. See details in Table 31.7-6:

Table 31.7-6. 2D DMA Color Space Conversion Configuration

| Color Space Conversion Method         | INPUT_SEL_CHO | 3B_PROC_EN_CHO | OUTPUT_SEL_CHO |
|---------------------------------------|---------------|----------------|----------------|
| YUV420 → RGB                          | 0             | 1              | 1              |
| YUV422 → RGB                          | 0             | 1              | 1              |
| YUV444 → RGB                          | 2             | 1              | 1              |
| YUV444 (only reverse the pixel order) | 2             | 0              | 1              |
| No color space conversion             | 7             | N/A            | N/A            |

Note that, this function is only available for 2D DMA RX channel0, not for any other RX channels.

- (j) Configure parameters required for the color space conversion formula, including DMA2D\_IN\_COLOR\_PARAM\_H0\_CHO, DMA2D\_IN\_COLOR\_PARAM\_H1\_CHO, DMA2D\_IN\_COLOR\_PARAM\_M0\_CHO, DMA2D\_IN\_COLOR\_PARAM\_M1\_CHO, DMA2D\_IN\_COLOR\_PARAM\_LO\_CHO, and DMA2D\_IN\_COLOR\_PARAM\_L1\_CHO. Note that, this function is only available for 2D DMA RX channel0, not for any other RX channels.
- (k) Select whether to reverse the pixel order of the image after 2D DMA color space conversion by configuring DMA2D\_IN\_SCRAMBLE\_SEL\_POST\_CHO:
- 0: BYTE2-1-0
  - 1: BYTE2-0-1
  - 2: BYTE1-0-2
  - 3: BYTE1-2-0
  - 4: BYTE0-2-1
  - 5: BYTE0-1-2

Configuration of 5 means reversing the pixel order, for example, reversing the RGB after 2D DMA color space conversion to BGR. Note that, this function is only available for 2D DMA RX channel0, not for any other RX channels.

- (l) Configure [DMA2D\\_OUTLINK\\_ADDR\\_CHn](#) as the 2D DMA TX channel linked list address, configure [DMA2D\\_INLINK\\_ADDR\\_CHn](#) as the 2D DMA RX channel linked list address.

4. Enable interrupt sources:

- [DMA2D\\_OUT\\_INT\\_ENA\\_CHn\\_REG](#)
- [DMA2D\\_IN\\_INT\\_ENA\\_CHn\\_REG](#)
- [JPEG\\_INT\\_ENA\\_REG](#)

5. Start the transmission of 2D DMA channels:

- 2D DMA TX channeln: set [DMA2D\\_OUTLINK\\_START\\_CHn](#) to 1 and then to 0
- 2D DMA RX channeln: set [DMA2D\\_INLINK\\_START\\_CHn](#) to 1 and then to 0

6. Start JPEG codec decoding by setting the [JPEG\\_JPEG\\_START](#) field.

7. Wait till DMA2D\_IN\_SUC\_EOF\_CHn\_INT becomes 1, indicating that the decoded image has been completely written to the memory.

### 31.7.3 Reset

Users can **reset** JPEG codec entirely or partially, depending on the actual scenarios, at any time during the encoding or decoding process:

- The entire JPEG codec, including all the RAMs and FIFOs as well as all the state machines: set [JPEG\\_SOFT\\_RST](#) to 1. In this case, the register configuration value will not be reset.
- Only all the RAMs and FIFOs inside the JPEG codec, for example, changing the quantization coefficient tables or Huffman tables: set [JPEG\\_FIFO\\_RST](#) to 1.
- Only all the state machines inside the JPEG codec, for example, only stop the current encoding or decoding process: set [JPEG\\_FSM\\_RST](#) to 1.

## 31.8 Register Summary

The addresses in this section are relative to JPEG Codec base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                       | Description   | Address | Access   |
|--|---|---------|----------|
| <b>Control and Configuration registers</b> |   |         |          |
| JPEG_CONFIG_REG                            | System level control and configuration register     | 0x0000  | varies   |
| JPEG_DQT_INFO_REG                          | Quantization coefficient table information register | 0x0004  | R/W      |
| JPEG_PIC_SIZE_REG                          | Image size register                                 | 0x0008  | R/W      |
| JPEG_TOQNR_REG                             | Quantization coefficient table0 register            | 0x0010  | HRO      |
| JPEG_T1QNR_REG                             | Quantization coefficient table1 register            | 0x0014  | HRO      |
| JPEG_T2QNR_REG                             | Quantization coefficient table2 register            | 0x0018  | HRO      |
| JPEG_T3QNR_REG                             | Quantization coefficient table3 register            | 0x001C  | HRO      |
| JPEG_DECODE_CONF_REG                       | Decoder configuration register                      | 0x0020  | varies   |
| JPEG_CO_REG                                | Color component0 register                           | 0x0024  | R/W      |
| JPEG_C1_REG                                | Color component1 register                           | 0x0028  | R/W      |
| JPEG_C2_REG                                | Color component2 register                           | 0x002C  | R/W      |
| JPEG_C3_REG                                | Color component3 register                           | 0x0030  | R/W      |
| JPEG_DHT_INFO_REG                          | Huffman table information register                  | 0x0034  | R/W      |
| JPEG_DHT_TOTLEN_DCO_REG                    | DC0 Huffman table codeword length register          | 0x0058  | HRO      |
| JPEG_DHT_VAI_DCO_REG                       | DC0 Huffman table symbol register                   | 0x005C  | HRO      |
| JPEG_DHT_TOTLEN_ACO_REG                    | AC0 Huffman table codeword length register          | 0x0060  | HRO      |
| JPEG_DHT_VAI_ACO_REG                       | AC0 Huffman table symbol register                   | 0x0064  | HRO      |
| JPEG_DHT_TOTLEN_DC1_REG                    | DC1 Huffman table codeword length register          | 0x0068  | HRO      |
| JPEG_DHT_VAI_DC1_REG                       | DC1 Huffman table symbol register                   | 0x006C  | HRO      |
| JPEG_DHT_TOTLEN_AC1_REG                    | AC1 Huffman table codeword length register          | 0x0070  | HRO      |
| JPEG_DHT_VAI_AC1_REG                       | AC1 Huffman table symbol register                   | 0x0074  | HRO      |
| JPEG_DHT_CODEMIN_DCO_REG                   | DC0 Huffman table minimum codeword register         | 0x0078  | HRO      |
| JPEG_DHT_CODEMIN_ACO_REG                   | AC0 Huffman table minimum codeword register         | 0x007C  | HRO      |
| JPEG_DHT_CODEMIN_DC1_REG                   | DC1 Huffman table minimum codeword register         | 0x0080  | HRO      |
| JPEG_DHT_CODEMIN_AC1_REG                   | AC1 Huffman table minimum codeword register         | 0x0084  | HRO      |
| JPEG_SYS_REG                               | System configuration register                       | 0x00F8  | R/W      |
| <b>Interrupt registers</b>                 |   |         |          |
| JPEG_INT_RAW_REG                           | Interrupt raw status register                       | 0x0038  | R/WTC/SS |
| JPEG_INT_ENA_REG                           | Interrupt enable register                           | 0x003C  | R/W      |
| JPEG_INT_ST_REG                            | Interrupt masked status register                    | 0x0040  | RO       |
| JPEG_INT_CLR_REG                           | Interrupt clear register                            | 0x0044  | WT       |
| <b>Version Register</b>                    |   |         |          |
| JPEG_VERSION_REG                           | Version control register                            | 0x00FC  | R/W      |



## 31.9 Registers

The addresses in this section are relative to the JPEG Codec base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

### Register 31.1. JPEG CONFIG REG (0x0000)

| JPEG_MODE<br>(reserved) |    |    |    |    |    |    |    |    |    |  |  |  |  |  |  |  |    |    |    |    |    |    |    |   |   |   |   | JPEG_PAUSE_EN |   | JPEG_TAILER_EN |   | JPEG_PIXEL_REV |   | JPEG_FIFO_RST |  | JPEG_SOFT_RST |  | JPEG_DECODE_TIMEOUT_TASK_SEL |  | JPEG_DECODE_TIMEOUT_THRES |  | JPEG_MEM_OCLK_FORCE_ON |  | JPEG_DHT_FIFO_EN |  | JPEG_COLOR_SPACE |  | JPEG_CNTR_TBL_SEL |  | JPEG_LQNR_TBL_SEL |  | JPEG_GNR_FIFO_EN |  | JPEG_DEBUG_DIRECT_OUT_EN |  | JPEG_DMA_LINKLIST_MODE |  | JPEG_SAMPLE_SEL |  | JPEG_FF_CHECK_EN |  | JPEG_GNR_PRESTION |  | JPEG_JPEG_START |  | JPEG_FSM_RST |  |
|-------------------------|----|----|----|----|----|----|----|----|----|--|--|--|--|--|--|--|----|----|----|----|----|----|----|---|---|---|---|---------------|---|----------------|---|----------------|---|---------------|--|---------------|--|------------------------------|--|---------------------------|--|------------------------|--|------------------|--|------------------|--|-------------------|--|-------------------|--|------------------|--|--------------------------|--|------------------------|--|-----------------|--|------------------|--|-------------------|--|-----------------|--|--------------|--|
| 31                      | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 17 |  |  |  |  |  |  |  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5             | 4 | 3              | 2 | 1              | 0 |               |  |               |  |                              |  |                           |  |                        |  |                  |  |                  |  |                   |  |                   |  |                  |  |                          |  |                        |  |                 |  |                  |  |                   |  |                 |  |              |  |
| 0                       | 00 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 32 |  |  |  |  |  |  |  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 0 | 1 | 1 | 1 | 1             | 1 | 0              | 0 | 0              | 0 | Reset         |  |               |  |                              |  |                           |  |                        |  |                  |  |                  |  |                   |  |                   |  |                  |  |                          |  |                        |  |                 |  |                  |  |                   |  |                 |  |              |  |

**JPEG\_FSM\_RST** Configures whether or not to reset the state machine of JPEG Codec.

0: Invalid. No effect

1: Reset the state machine

(WT)

**JPEG\_JPEG\_START** Configures whether or not to start compressing a new image.

0: Invalid. No effect

1: Start compressing a new image

(WT)

**JPEG\_QNR\_PRECISION** Configures the quantization coefficient table precision for the encoder.

0: 8-bit precision

1: 16-bit precision

(R/W)

**JPEG\_FF\_CHECK\_EN** Configures whether or not to add “0x00” after “0xFF”.

0: Not add

1: Add

(R/W)

**JPEG\_SAMPLE\_SEL** Configures the format of the image to be compressed.

O: YUV444

1: YUV422

2: YUV420

3: Invalid. No effect

(R/W)

Continued on the next page...

**Register 31.1. JPEG\_CONFIG\_REG (0x0000)**

Continued from the previous page...

**JPEG\_DMA\_LINKLIST\_MODE** Represents 2D DMA linked list mode.

0: Invalid. No effect

1: 2D DMA uses linked lists to configure

(RO)

**JPEG\_DEBUG\_DIRECT\_OUT\_EN** Configures whether or not to enable debug mode for encoder.

0: Disable debug mode, the encoder will work in normal mode

1: Enable debug mode, the input image will be directly output by the encoder

(R/W)

**JPEG\_QNR\_FIFO\_EN** Configures whether or not to enable FIFO mode when configuring quantization coefficient tables.

0: Disable. Use non-FIFO mode

1: Enable

(R/W)

**JPEG\_LQNR\_TBL\_SEL** Configures the luminance quantization table ID for the encoder. (R/W)

**JPEG\_CQNR\_TBL\_SEL** Configures the chrominance quantization table ID for the encoder. (R/W)

**JPEG\_COLOR\_SPACE** Configures the original image's color space.

0: RGB888

1: YUV422

2: RGB565

3: GRAY

(R/W)

**JPEG\_DHT\_FIFO\_EN** Configures whether or not to enable FIFO mode when configuring Huffman tables.

0: Disable. Use non-FIFO mode

1: Enable

Note that to read Huffman tables only non-FIFO mode is supported.

(R/W)

**JPEG\_MEM\_CLK\_FORCE\_ON** Configures whether or not to force on memory's clock gate.

0: Not force on

1: Force on

(R/W)

**JPEG\_DECODE\_TIMEOUT\_THRES** Configures decode timeout period to trigger [JPEG\\_DECODE\\_TIMEOUT\\_INT\\_RAW](#). The clock cycles of timeout period =  $2^{JPEG\_DECODE\_TIMEOUT\_THRES} - 1$ . (R/W)

Continued on the next page...

**Register 31.1. JPEG\_CONFIG\_REG (0x0000)**

Continued from the previous page...

**JPEG\_DECODE\_TIMEOUT\_TASK\_SEL** Configures the reset mode upon the decoder timeout.

0: Software uses reset to abort the decoding process

1: Hardware automatically aborts decoding process

(R/W)

**JPEG\_SOFT\_RST** Configures whether or not to apply soft reset to the JPEG Codec.

0: Release the soft reset

1: Apply soft reset to the JPEG Codec (the register configuration value will not be reset)

(R/W)

**JPEG\_FIFO\_RST** Configures whether or not to apply FIFO reset to the JPEG Codec.

0: Release the FIFO reset

1: Apply FIFO reset to the JPEG Codec

(R/W)

**JPEG\_PIXEL\_REV** Configures whether or not to reverse the original image's pixel order.

0: Not reverse

1: Reverse

(R/W)

**JPEG\_TAILER\_EN** Configures whether or not to add EOI marker "0xFFD9" at the end of bitstream.

0: Not add

1: Add

(R/W)

**JPEG\_PAUSE\_EN** Configures whether or not to pause the JPEG Codec.

0: Not pause

1: Pause

(R/W)

**JPEG\_MODE** Configures if the JPEG Codec is working as an encoder or a decoder.

0: Encoder

1: Decoder

(R/W)

Register 31.2. JPEG\_DQT\_INFO\_REG (0x0004)

|                  |    |    |    |    |   |   |   |
|------------------|----|----|----|----|---|---|---|
| JPEG_T3_DQT_INFO |    |    |    |    |   |   |   |
| JPEG_T2_DQT_INFO |    |    |    |    |   |   |   |
| JPEG_T1_DQT_INFO |    |    |    |    |   |   |   |
| JPEG_T0_DQT_INFO |    |    |    |    |   |   |   |
| 31               | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 3                |    | 2  |    | 1  |   | 0 |   |
| Reset            |    |    |    |    |   |   |   |

**JPEG\_T0\_DQT\_INFO** Configures quantization coefficient table0's precision and ID for decoder.

Bit[7:4]: Configures precision

Bit[3:0]: Configures ID

(R/W)

**JPEG\_T1\_DQT\_INFO** Configures quantization coefficient table1's precision and ID for decoder. See details in [JPEG\\_T0\\_DQT\\_INFO](#). (R/W)

**JPEG\_T2\_DQT\_INFO** Configures quantization coefficient table2's precision and ID for decoder. See details in [JPEG\\_T0\\_DQT\\_INFO](#). (R/W)

**JPEG\_T3\_DQT\_INFO** Configures quantization coefficient table3's precision and ID for decoder. See details in [JPEG\\_T0\\_DQT\\_INFO](#). (R/W)

Register 31.3. JPEG\_PIC\_SIZE\_REG (0x0008)

|         |  |  |  |  |  |  |  |     |  |  |  |  |  |  |       |
|---------|--|--|--|--|--|--|--|-----|--|--|--|--|--|--|-------|
| JPEG_HA |  |  |  |  |  |  |  |     |  |  |  |  |  |  |       |
| JPEG_VA |  |  |  |  |  |  |  |     |  |  |  |  |  |  |       |
| 31      |  |  |  |  |  |  |  |     |  |  |  |  |  |  | 0     |
| 640     |  |  |  |  |  |  |  | 480 |  |  |  |  |  |  |       |
|         |  |  |  |  |  |  |  |     |  |  |  |  |  |  | Reset |

**JPEG\_VA** Configures the image's height.

When JPEG Codec works as an encoder, the maximum configurable bits is 14.

When JPEG Codec works as a decoder, the maximum configurable bits is 16.

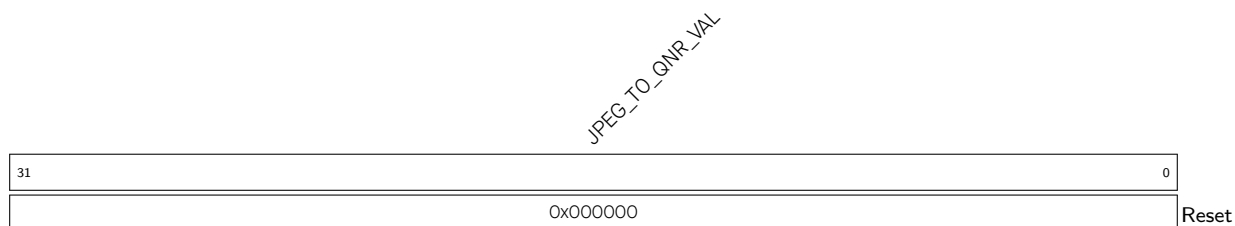
(R/W)

**JPEG\_HA** Configures the image's width.

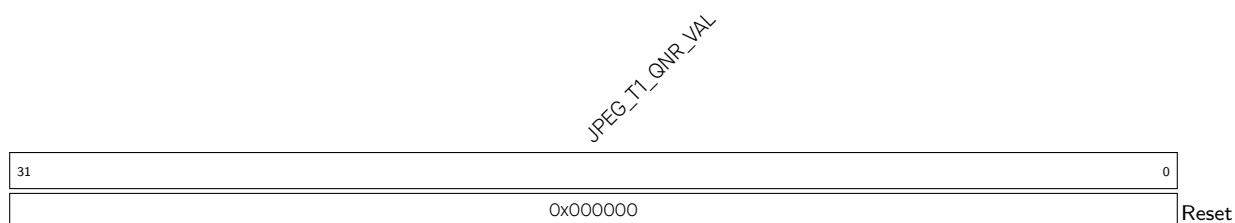
When JPEG Codec works as an encoder, the maximum configurable bits is 14.

When JPEG Codec works as a decoder, the maximum configurable bits is 16.

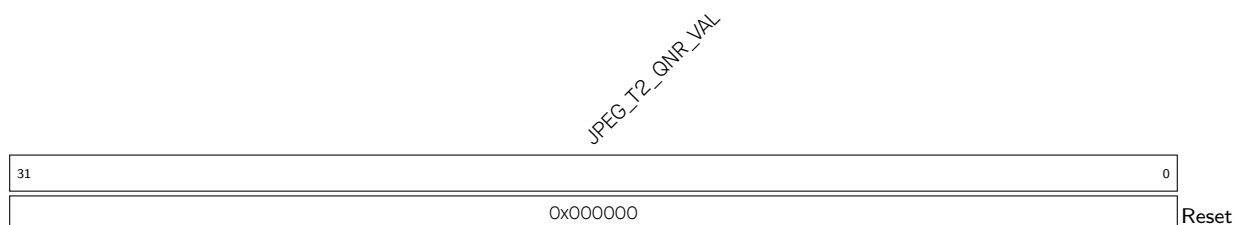
(R/W)

**Register 31.4. JPEG\_T0QNR\_REG (0x0010)**

**JPEG\_TO\_QNR\_VAL** Configures the quantization coefficients of the quantization table 0 in FIFO mode. (HRO)

**Register 31.5. JPEG\_T1QNR\_REG (0x0014)**

**JPEG\_T1\_QNR\_VAL** Configures the quantization coefficients of the quantization table 1 in FIFO mode. (HRO)

**Register 31.6. JPEG\_T2QNR\_REG (0x0018)**

**JPEG\_T2\_QNR\_VAL** Configures the quantization coefficients of the quantization table 2 in FIFO mode. (HRO)

### Register 31.7. JPEG\_T3QNR\_REG (0x001C)

Diagram of the `JPEG_T3_QNR_VAL` register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value `0x000000` is shown in the lower 24 bits, and the label "Reset" is at the bottom right.

**JPEG\_T3\_QNR\_VAL** Configures the quantization coefficients of the quantization table 3 in FIFO mode. (HRO)

### Register 31.8. JPEG\_DECODE\_CONF\_REG (0x0020)

|    |    |    |    |    |    |    |    |    |    |      |       |
|----|----|----|----|----|----|----|----|----|----|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 16 | 15   | 0     |
| 0  | 1  | 0  | 3  | 3  | 1  | 3  |    |    |    | 0x00 | Reset |

**JPEG\_RESTART\_INTERVAL** Configures the RST interval in DRI segment when decoding. (R/W)

**JPEG\_COMPONENT\_NUM** Configures the number of chrominance components in the image when decoding. (R/W)

**JPEG\_SW\_DHT\_EN** Represents the Huffman table configured by the software for the decoder. The value is always 1. (RO)

**JPEG\_SOS\_CHECK\_BYTE\_NUM** Configures the byte number to check the next SOS marker in the multi-scan image after one scan is decoded down. The actual check number is `JPEG SOS CHECK BYTE NUM + 1 (R/W)`

**JPEG\_RST\_CHECK\_BYTE\_NUM** Configures the byte number to check the next RST marker after one RST interval is decoded down. The actual check number is **JPEG\_RST\_CHECK\_BYTE\_NUM** + 1. (R/W)

**JPEG\_MULTI\_SCAN\_ERR\_CHECK** Reserved for decoder and should not be configured. (R/W)

**JPEG\_DEZIGZAG\_READY\_CTL** Reserved for decoder and should not be configured. (R/W)

**Register 31.9. JPEG\_CO\_REG (0x0024)**

|            |    |    |    |    |    |    |   |            |   |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|------------|----|----|----|----|----|----|---|------------|---|---|---|---|---|---|---|------------------|---|---|---|---|---|---|---|------------------|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| (reserved) |    |    |    |    |    |    |   | JPEG_CO_ID |   |   |   |   |   |   |   | JPEG_CO_X_FACTOR |   |   |   |   |   |   |   | JPEG_CO_Y_FACTOR |   |   |   |   |   |   |   | JPEG_CO_DQT_TBL_SEL |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         | 24 | 23 | 16 | 15 | 12 | 11 | 8 | 7          | 0 |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

Reset

**JPEG\_CO\_DQT\_TBL\_SEL** Configures the selected quantization coefficient table ID for component0 in decoder mode. (R/W)

**JPEG\_CO\_Y\_FACTOR** Configures the vertical sampling factor of component0 in decoder mode. (R/W)

**JPEG\_CO\_X\_FACTOR** Configures the horizontal sampling factor of component0 in decoder mode. (R/W)

**JPEG\_CO\_ID** Configures the ID of component0 in decoder mode. (R/W)

**Register 31.10. JPEG\_C1\_REG (0x0028)**

|            |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 31         |  |  |  |  |  |  |  | 24         |  |  |  |  |  |  |  | 23               |  |  |  |  |  |  |  | 16               |  |  |  |  |  |  |  | 15                  |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 0          |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

Reset

**JPEG\_C1\_DQT\_TBL\_SEL** Configures the selected quantization coefficient table ID for component1 in decoder mode. (R/W)

**JPEG\_C1\_Y\_FACTOR** Configures the vertical sampling factor of component1 in decoder mode. (R/W)

**JPEG\_C1\_X\_FACTOR** Configures the horizontal sampling factor of component1 in decoder mode. (R/W)

**JPEG\_C1\_ID** Configures the ID of component1 in decoder mode. (R/W)

**Register 31.11. JPEG\_C2\_REG (0x002C)**

|            |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 31         |  |  |  |  |  |  |  | 24         |  |  |  |  |  |  |  | 23               |  |  |  |  |  |  |  | 16               |  |  |  |  |  |  |  | 15                  |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 0          |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

Reset

**JPEG\_C2\_DQT\_TBL\_SEL** Configures the selected quantization coefficient table ID for component2 in decoder mode. (R/W)

**JPEG\_C2\_Y\_FACTOR** Configures the vertical sampling factor of component2 in decoder mode. (R/W)

**JPEG\_C2\_X\_FACTOR** Configures the horizontal sampling factor of component2 in decoder mode. (R/W)

**JPEG\_C2\_ID** Configures the ID of component2 in decoder mode. (R/W)

**Register 31.12. JPEG\_C3\_REG (0x0030)**

|            |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 31         |  |  |  |  |  |  |  | 24         |  |  |  |  |  |  |  | 23               |  |  |  |  |  |  |  | 16               |  |  |  |  |  |  |  | 15                  |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  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| 0          |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

Reset

**JPEG\_C3\_DQT\_TBL\_SEL** Configures the selected quantization coefficient table ID for component3 in decoder mode. (R/W)

**JPEG\_C3\_Y\_FACTOR** Configures the vertical sampling factor of component3 in decoder mode. (R/W)

**JPEG\_C3\_X\_FACTOR** Configures the horizontal sampling factor of component3 in decoder mode. (R/W)

**JPEG\_C3\_ID** Configures the ID of component3 in decoder mode. (R/W)



### Register 31.13. JPEG DHT INFO REG (0x0034)

|                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |       |
|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|-----------------|--|--|--|-----------------|--|--|--|-----------------|--|--|--|-------|
| (reserved)       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | JPEG_AC1_DHT_ID |  |  |  | JPEG_AC0_DHT_ID |  |  |  | JPEG_DC1_DHT_ID |  |  |  | JPEG_DC0_DHT_ID |  |  |  |       |
| 311615121187430  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1               |  |  |  | 0               |  |  |  | 1               |  |  |  | 0               |  |  |  | Reset |
| 0000000000000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |       |

**JPEG\_DCO\_DHT\_ID** Configures the ID of DCO Huffman table in decoder mode. (R/W)

**JPEG DC1 DHT ID** Configures the ID of DC1 Huffman table in decoder mode. (R/W)

**JPEG\_ACO\_DHT\_ID** Configures the ID of ACO Huffman table in decoder mode. (R/W)

**JPEG\_AC1\_DHT\_ID** Configures the ID of AC1 Huffman table in decoder mode. (R/W)

### Register 31.14. JPEG INT RAW REG (0x0038)

[illegible]

JPEG DONE INT RAW The raw status of JPEG DONE INT. (R/WTC/SS)

**JPEG\_RLE\_PARALLEL\_ERR\_INT\_RAW** The raw status of JPEG\_RLE\_PARALLEL\_ERR\_INT.  
(R/WTC/SS)

**JPEG CID ERR INT RAW** The raw status of JPEG CID ERR INT. (R/WTC/SS)

**JPEG\_C\_DHT\_DC\_ID\_ERR\_INT\_RAW** The raw status of JPEG\_C\_DHT\_DC\_ID\_ERR\_INT.  
(R/WTC/SS)

**JPEG C DHT AC ID ERR INT RAW** The raw status of JPEG C DHT AC ID ERR INT. (R/WTC/SS)

**JPEG C DQT ID ERR INT RAW** The raw status of JPEG C DQT ID ERR INT. (R/WTC/SS)

**JPEG RST UXP ERR INT RAW** The raw status of JPEG RST UXP ERR INT. (R/WTC/SS)

**JPEG\_RST\_CHECK\_NONE\_ERR\_INT\_RAW** The raw status of JPEG\_RST\_CHECK\_NONE\_ERR\_INT.  
(R/WTC/SS)

Continued on the next page...

**Register 31.14. JPEG\_INT\_RAW\_REG (0x0038)**

Continued from the previous page...

**JPEG\_RST\_CHECK\_POS\_ERR\_INT\_RAW** The raw status of JPEG\_RST\_CHECK\_POS\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_OUT\_EOF\_INT\_RAW** The raw status of JPEG\_OUT\_EOF\_INT. (R/WTC/SS)

**JPEG\_SR\_COLOR\_MODE\_ERR\_INT\_RAW** The raw status of JPEG\_SR\_COLOR\_MODE\_ERR\_INT.  
This interrupt is invalid. (R/WTC/SS)

**JPEG\_DCT\_DONE\_INT\_RAW** The raw status of JPEG\_DCT\_DONE\_INT. (R/WTC/SS)

**JPEG\_BS\_LAST\_BLOCK\_EOF\_INT\_RAW** The raw status of JPEG\_BS\_LAST\_BLOCK\_EOF\_INT.  
(R/WTC/SS)

**JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT\_RAW** The raw status of JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_SCAN\_CHECK\_POS\_ERR\_INT\_RAW** The raw status of JPEG\_SCAN\_CHECK\_POS\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_UXP\_DET\_INT\_RAW** The raw status of JPEG\_UXP\_DET\_INT. (R/WTC/SS)

**JPEG\_EN\_FRAME\_EOF\_ERR\_INT\_RAW** The raw status of JPEG\_EN\_FRAME\_EOF\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_EN\_FRAME\_EOF\_LACK\_INT\_RAW** The raw status of JPEG\_EN\_FRAME\_EOF\_LACK\_INT.  
(R/WTC/SS)

**JPEG\_DE\_FRAME\_EOF\_ERR\_INT\_RAW** The raw status of JPEG\_DE\_FRAME\_EOF\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_DE\_FRAME\_EOF\_LACK\_INT\_RAW** The raw status of JPEG\_DE\_FRAME\_EOF\_LACK\_INT.  
(R/WTC/SS)

**JPEG\_SOS\_UNMATCH\_ERR\_INT\_RAW** The raw status of JPEG\_SOS\_UNMATCH\_ERR\_INT.  
(R/WTC/SS)

**JPEG\_MARKER\_ERR\_FST\_SCAN\_INT\_RAW** The raw status of JPEG\_MARKER\_ERR\_FST\_SCAN\_INT.  
(R/WTC/SS)

**JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT\_RAW** The raw status of JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT.  
(R/WTC/SS)

**JPEG\_UNDET\_INT\_RAW** The raw status of JPEG\_UNDET\_INT. (R/WTC/SS)

**JPEG\_DECODE\_TIMEOUT\_INT\_RAW** The raw status of JPEG\_DECODE\_TIMEOUT\_INT. (R/WTC/SS)

### Register 31.15. JPEG\_INT\_ENA\_REG (0x003C)

[illegible]

**JPEG DONE INT ENA** Write 1 to enable JPEG DONE INT ENA. (R/W)

**JPEG RLE PARALLEL ERR INT ENA** Write 1 to enable JPEG RLE PARALLEL ERR INT. (R/W)

**JPEG CID ERR INT ENA** Write 1 to enable JPEG CID ERR INT. (R/W)

**JPEG\_C\_DHT\_DC\_ID\_ERR\_INT\_ENA** Write 1 to enable JPEG\_C\_DHT\_DC\_ID\_ERR\_INT. (R/W)

**JPEG C DHT AC ID ERR INT ENA** Write 1 to enable JPEG C DHT AC ID ERR INT. (R/W)

**JPEG\_C\_DQT\_ID\_ERR\_INT\_ENA** Write 1 to enable JPEG\_C\_DQT\_ID\_ERR\_INT. (R/W)

**JPEG\_RST\_UXP\_ERR\_INT\_ENA** Write 1 to enable JPEG\_RST\_UXP\_ERR\_INT. (R/W)

**JPEG\_RST\_CHECK\_NONE\_ERR\_INT\_ENA** Write 1 to enable JPEG\_RST\_CHECK\_NONE\_ERR\_INT.  
(R/W)

**JPEG\_RST\_CHECK\_POS\_ERR\_INT\_ENA** Write 1 to enable JPEG\_RST\_CHECK\_POS\_ERR\_INT. (R/W)

**JPEG\_OUT\_EOF\_INT\_ENA** Write 1 to enable JPEG\_OUT\_EOF\_INT. (R/W)

**JPEG\_SR\_COLOR\_MODE\_ERR\_INT\_ENA** Write 1 to enable JPEG\_SR\_COLOR\_MODE\_ERR\_INT.  
(R/W)

**JPEG DCT DONE INT ENA** Write 1 to enable JPEG DCT DONE INT. (R/W)

**JPEG\_BS\_LAST\_BLOCK\_EOF\_INT\_ENA** Write 1 to enable JPEG\_BS\_LAST\_BLOCK\_EOF\_INT. (R/W)

**JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT\_ENA** Write 1 to enable JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT.  
(R/W)

**JPEG\_SCAN\_CHECK\_POS\_ERR\_INT\_ENA** Write 1 to enable JPEG\_SCAN\_CHECK\_POS\_ERR\_INT.  
(R/W)

**JPEG UXP DET INT ENA** Write 1 to enable JPEG UXP DET INT. (R/W)

Continued on the next page...

**Register 31.15. JPEG\_INT\_ENA\_REG (0x003C)**

Continued from the previous page...

**JPEG\_EN\_FRAME\_EOF\_ERR\_INT\_ENA** Write 1 to enable JPEG\_EN\_FRAME\_EOF\_ERR\_INT. (R/W)

**JPEG\_EN\_FRAME\_EOF\_LACK\_INT\_ENA** Write 1 to enable JPEG\_EN\_FRAME\_EOF\_LACK\_INT.  
(R/W)

**JPEG\_DE\_FRAME\_EOF\_ERR\_INT\_ENA** Write 1 to enable JPEG\_DE\_FRAME\_EOF\_ERR\_INT. (R/W)

**JPEG\_DE\_FRAME\_EOF\_LACK\_INT\_ENA** Write 1 to enable JPEG\_DE\_FRAME\_EOF\_LACK\_INT.  
(R/W)

**JPEG\_SOS\_UNMATCH\_ERR\_INT\_ENA** Write 1 to enable JPEG\_SOS\_UNMATCH\_ERR\_INT. (R/W)

**JPEG\_MARKER\_ERR\_FST\_SCAN\_INT\_ENA** Write 1 to enable JPEG\_MARKER\_ERR\_FST\_SCAN\_INT.  
(R/W)

**JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT\_ENA** Write 1 to enable JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT.  
(R/W)

**JPEG\_UNDET\_INT\_ENA** Write 1 to enable JPEG\_UNDET\_INT. (R/W)

**JPEG\_DECODE\_TIMEOUT\_INT\_ENA** Write 1 to enable JPEG\_DECODE\_TIMEOUT\_INT. (R/W)

Register 31.16. JPEG\_INT\_ST\_REG (0x0040)

|            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |                            |                   |                                   |                                 |                             |                               |                               |                               |                     |                                |                                 |                               |                               |                     |                               |                                |                          |                             |                             |                              |                  |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|----------------------------|-------------------|-----------------------------------|---------------------------------|-----------------------------|-------------------------------|-------------------------------|-------------------------------|---------------------|--------------------------------|---------------------------------|-------------------------------|-------------------------------|---------------------|-------------------------------|--------------------------------|--------------------------|-----------------------------|-----------------------------|------------------------------|------------------|
| (reserved) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       | JPEG_DECODE_TIMEOUT_INT_ST | JPEG_UNDET_INT_ST | JPEG_MARKER_ERR_OTHER_SCAN_INT_ST | JPEG_MARKER_ERR_FST_SCAN_INT_ST | JPEG_SOS_UNMATCH_ERR_INT_ST | JPEG_DE_FRAME_EOF_LACK_INT_ST | JPEG_DE_FRAME_EOF_LACK_INT_ST | JPEG_EN_FRAME_EOF_LACK_INT_ST | JPEG_UXP_DET_INT_ST | JPEG_SCAN_CHECK_POS_ERR_INT_ST | JPEG_SCAN_CHECK_NONE_ERR_INT_ST | JPEG_BS_LAST_BLOCK_EOF_INT_ST | JPEG_SR_COLOR_MODE_ERR_INT_ST | JPEG_OUT_EOF_INT_ST | JPEG_RST_CHECK_POS_ERR_INT_ST | JPEG_RST_CHECK_NONE_ERR_INT_ST | JPEG_C_DQT_ID_ERR_INT_ST | JPEG_C_DHT_AC_ID_ERR_INT_ST | JPEG_C_DHT_DC_ID_ERR_INT_ST | JPEG_RLE_PARALLEL_ERR_INT_ST | JPEG_DONE_INT_ST |
| 31         | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |                            |                   |                                   |                                 |                             |                               |                               |                               |                     |                                |                                 |                               |                               |                     |                               |                                |                          |                             |                             |                              |                  |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |                            |                   |                                   |                                 |                             |                               |                               |                               |                     |                                |                                 |                               |                               |                     |                               |                                |                          |                             |                             |                              |                  |

**JPEG\_DONE\_INT\_ST** The masked interrupt status of JPEG\_DONE\_INT. (RO)

**JPEG\_RLE\_PARALLEL\_ERR\_INT\_ST** The masked interrupt status of JPEG\_RLE\_PARALLEL\_ERR\_INT. (RO)

**JPEG\_CID\_ERR\_INT\_ST** The masked interrupt status of JPEG\_CID\_ERR\_INT. (RO)

**JPEG\_C\_DHT\_DC\_ID\_ERR\_INT\_ST** The masked interrupt status of JPEG\_C\_DHT\_DC\_ID\_ERR\_INT. (RO)

**JPEG\_C\_DHT\_AC\_ID\_ERR\_INT\_ST** The masked interrupt status of JPEG\_C\_DHT\_AC\_ID\_ERR\_INT. (RO)

**JPEG\_C\_DQT\_ID\_ERR\_INT\_ST** The masked interrupt status of JPEG\_C\_DQT\_ID\_ERR\_INT. (RO)

**JPEG\_RST\_UXP\_ERR\_INT\_ST** The masked interrupt status of JPEG\_RST\_UXP\_ERR\_INT. (RO)

**JPEG\_RST\_CHECK\_NONE\_ERR\_INT\_ST** The masked interrupt status of JPEG\_RST\_CHECK\_NONE\_ERR\_INT. (RO)

**JPEG\_RST\_CHECK\_POS\_ERR\_INT\_ST** The masked interrupt status of JPEG\_RST\_CHECK\_POS\_ERR\_INT. (RO)

**JPEG\_OUT\_EOF\_INT\_ST** The masked interrupt status of JPEG\_OUT\_EOF\_INT. (RO)

**JPEG\_SR\_COLOR\_MODE\_ERR\_INT\_ST** The masked interrupt status of JPEG\_SR\_COLOR\_MODE\_ERR\_INT. (RO)

**JPEG\_DCT\_DONE\_INT\_ST** The masked interrupt status of JPEG\_DCT\_DONE\_INT. (RO)

**JPEG\_BS\_LAST\_BLOCK\_EOF\_INT\_ST** The masked interrupt status of JPEG\_BS\_LAST\_BLOCK\_EOF\_INT. (RO)

**JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT\_ST** The masked interrupt status of JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT. (RO)

**JPEG\_SCAN\_CHECK\_POS\_ERR\_INT\_ST** The masked interrupt status of JPEG\_SCAN\_CHECK\_POS\_ERR\_INT. (RO)

**JPEG\_UXP\_DET\_INT\_ST** The masked interrupt status of JPEG\_UXP\_DET\_INT. (RO)

Continued on the next page...

**Register 31.16. JPEG\_INT\_ST\_REG (0x0040)**

Continued from the previous page...

|  |   |
|--|---|
| <b>JPEG_EN_FRAME_EOF_ERR_INT_ST</b>      | The masked interrupt status of JPEG_EN_FRAME_EOF_ERR_INT. (RO)      |
| <b>JPEG_EN_FRAME_EOF_LACK_INT_ST</b>     | The masked interrupt status of JPEG_EN_FRAME_EOF_LACK_INT. (RO)     |
| <b>JPEG_DE_FRAME_EOF_ERR_INT_ST</b>      | The masked interrupt status of JPEG_DE_FRAME_EOF_ERR_INT. (RO)      |
| <b>JPEG_DE_FRAME_EOF_LACK_INT_ST</b>     | The masked interrupt status of JPEG_DE_FRAME_EOF_LACK_INT. (RO)     |
| <b>JPEG_SOS_UNMATCH_ERR_INT_ST</b>       | The masked interrupt status of JPEG_SOS_UNMATCH_ERR_INT. (RO)       |
| <b>JPEG_MARKER_ERR_FST_SCAN_INT_ST</b>   | The masked interrupt status of JPEG_MARKER_ERR_FST_SCAN_INT. (RO)   |
| <b>JPEG_MARKER_ERR_OTHER_SCAN_INT_ST</b> | The masked interrupt status of JPEG_MARKER_ERR_OTHER_SCAN_INT. (RO) |
| <b>JPEG_UNDET_INT_ST</b>                 | The masked interrupt status of JPEG_UNDET_INT. (RO)                 |
| <b>JPEG_DECODE_TIMEOUT_INT_ST</b>        | The masked interrupt status of JPEG_DECODE_TIMEOUT_INT. (RO)        |

## Register 31.17. JPEG\_INT\_CLR\_REG (0x0044)

|            |   |   |   |   |   |   |                             |    |                    |    |                                    |    |                                  |    |                              |    |                                |    |                                |    |                      |    |                                 |   |                                |   |                                |   |                                |   |                           |   |                              |   |                              |   |                               |   |                   |       |
|------------|---|---|---|---|---|---|-----------------------------|----|--------------------|----|------------------------------------|----|----------------------------------|----|------------------------------|----|--------------------------------|----|--------------------------------|----|----------------------|----|---------------------------------|---|--------------------------------|---|--------------------------------|---|--------------------------------|---|---------------------------|---|------------------------------|---|------------------------------|---|-------------------------------|---|-------------------|-------|
| (reserved) |   |   |   |   |   |   | JPEG_DECODE_TIMEOUT_INT_CLR |    | JPEG_UNDET_INT_CLR |    | JPEG_MARKER_ERR_OTHER_SCAN_INT_CLR |    | JPEG_MARKER_ERR_FST_SCAN_INT_CLR |    | JPEG_SOS_UNMATCH_ERR_INT_CLR |    | JPEG_DE_FRAME_EOF_LACK_INT_CLR |    | JPEG_EN_FRAME_EOF_LACK_INT_CLR |    | JPEG_UXP_DET_INT_CLR |    | JPEG_SCAN_CHECK_POS_ERR_INT_CLR |   | JPEG_BS_LAST_BLOCK_EOF_INT_CLR |   | JPEG_SR_COLOR_MODE_ERR_INT_CLR |   | JPEG_RST_CHECK_POS_ERR_INT_CLR |   | JPEG_C_DQT_ID_ERR_INT_CLR |   | JPEG_C_DHT_AC_ID_ERR_INT_CLR |   | JPEG_C_DHT_DC_ID_ERR_INT_CLR |   | JPEG_RLE_PARALLEL_ERR_INT_CLR |   | JPEG_DONE_INT_CLR |       |
| 31         |   |   |   |   |   |   | 25                          | 24 | 23                 | 22 | 21                                 | 20 | 19                               | 18 | 17                           | 16 | 15                             | 14 | 13                             | 12 | 11                   | 10 | 9                               | 8 | 7                              | 6 | 5                              | 4 | 3                              | 2 | 1                         | 0 |                              |   |                              |   |                               |   |                   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0  | 0                  | 0  | 0                                  | 0  | 0                                | 0  | 0                            | 0  | 0                              | 0  | 0                              | 0  | 0                    | 0  | 0                               | 0 | 0                              | 0 | 0                              | 0 | 0                              | 0 | 0                         | 0 | 0                            | 0 | 0                            | 0 | 0                             | 0 | 0                 | Reset |

**JPEG\_DONE\_INT\_CLR** Write 1 to clear JPEG\_DONE\_INT. (WT)

**JPEG\_RLE\_PARALLEL\_ERR\_INT\_CLR** Write 1 to clear JPEG\_RLE\_PARALLEL\_ERR\_INT. (WT)

**JPEG\_CID\_ERR\_INT\_CLR** Write 1 to clear JPEG\_CID\_ERR\_INT. (WT)

**JPEG\_C\_DHT\_DC\_ID\_ERR\_INT\_CLR** Write 1 to clear JPEG\_C\_DHT\_DC\_ID\_ERR\_INT. (WT)

**JPEG\_C\_DHT\_AC\_ID\_ERR\_INT\_CLR** Write 1 to clear JPEG\_C\_DHT\_AC\_ID\_ERR\_INT. (WT)

**JPEG\_C\_DQT\_ID\_ERR\_INT\_CLR** Write 1 to clear JPEG\_C\_DQT\_ID\_ERR\_INT. (WT)

**JPEG\_RST\_UXP\_ERR\_INT\_CLR** Write 1 to clear JPEG\_RST\_UXP\_ERR\_INT. (WT)

**JPEG\_RST\_CHECK\_NONE\_ERR\_INT\_CLR** Write 1 to clear JPEG\_RST\_CHECK\_NONE\_ERR\_INT. (WT)

**JPEG\_RST\_CHECK\_POS\_ERR\_INT\_CLR** Write 1 to clear JPEG\_RST\_CHECK\_POS\_ERR\_INT. (WT)

**JPEG\_OUT\_EOF\_INT\_CLR** Write 1 to clear JPEG\_OUT\_EOF\_INT. (WT)

**JPEG\_SR\_COLOR\_MODE\_ERR\_INT\_CLR** Write 1 to clear JPEG\_SR\_COLOR\_MODE\_ERR\_INT. (WT)

**JPEG\_DCT\_DONE\_INT\_CLR** Write 1 to clear JPEG\_DCT\_DONE\_INT. (WT)

**JPEG\_BS\_LAST\_BLOCK\_EOF\_INT\_CLR** Write 1 to clear JPEG\_BS\_LAST\_BLOCK\_EOF\_INT. (WT)

**JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT\_CLR** Write 1 to clear JPEG\_SCAN\_CHECK\_NONE\_ERR\_INT. (WT)

**JPEG\_SCAN\_CHECK\_POS\_ERR\_INT\_CLR** Write 1 to clear JPEG\_SCAN\_CHECK\_POS\_ERR\_INT. (WT)

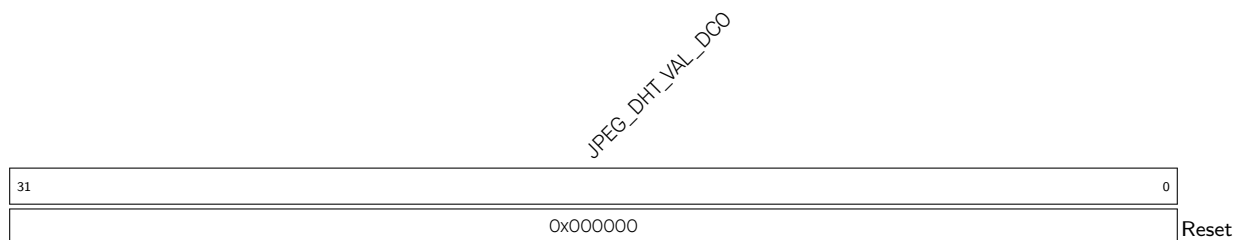
Continued on the next page...

**Register 31.17. JPEG\_INT\_CLR\_REG (0x0044)**

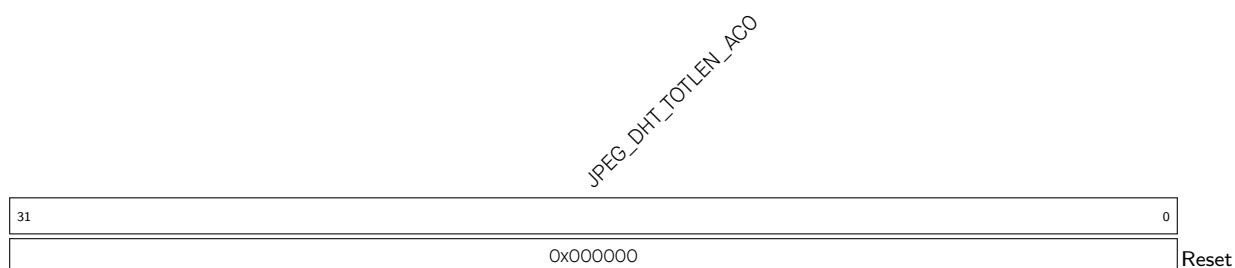
Continued from the previous page...

**JPEG\_UXP\_DET\_INT\_CLR** Write 1 to clear JPEG\_UXP\_DET\_INT. (WT)**JPEG\_EN\_FRAME\_EOF\_ERR\_INT\_CLR** Write 1 to clear JPEG\_EN\_FRAME\_EOF\_ERR\_INT. (WT)**JPEG\_EN\_FRAME\_EOF\_LACK\_INT\_CLR** Write 1 to clear JPEG\_EN\_FRAME\_EOF\_LACK\_INT. (WT)**JPEG\_DE\_FRAME\_EOF\_ERR\_INT\_CLR** Write 1 to clear JPEG\_DE\_FRAME\_EOF\_ERR\_INT. (WT)**JPEG\_DE\_FRAME\_EOF\_LACK\_INT\_CLR** Write 1 to clear JPEG\_DE\_FRAME\_EOF\_LACK\_INT. (WT)**JPEG\_SOS\_UNMATCH\_ERR\_INT\_CLR** Write 1 to clear JPEG\_SOS\_UNMATCH\_ERR\_INT. (WT)**JPEG\_MARKER\_ERR\_FST\_SCAN\_INT\_CLR** Write 1 to clear JPEG\_MARKER\_ERR\_FST\_SCAN\_INT.  
(WT)**JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT\_CLR** Write 1 to clear JPEG\_MARKER\_ERR\_OTHER\_SCAN\_INT.  
(WT)**JPEG\_UNDET\_INT\_CLR** Write 1 to clear JPEG\_UNDET\_INT. (WT)**JPEG\_DECODE\_TIMEOUT\_INT\_CLR** Write 1 to clear JPEG\_DECODE\_TIMEOUT\_INT. (WT)**Register 31.18. JPEG\_DHT\_TOTLEN\_DCO\_REG (0x0058)****JPEG\_DHT\_TOTLEN\_DCO** Configures the number of codeword with a codeword length of 1 to 16 bits for DCO Huffman table in FIFO mode. (HRO)

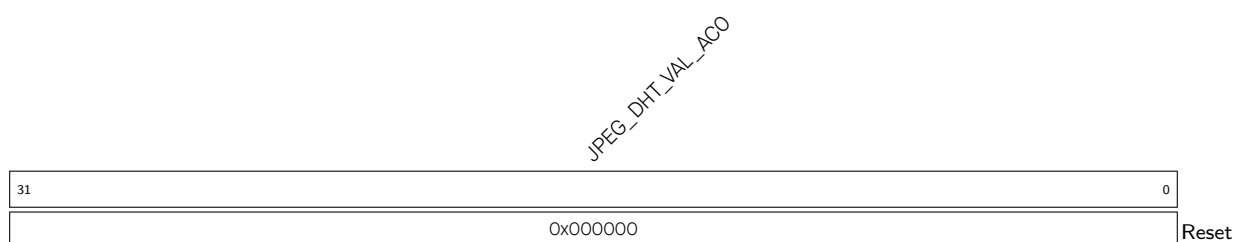


**Register 31.19. JPEG\_DHT\_VAL\_DCO\_REG (0x005C)**

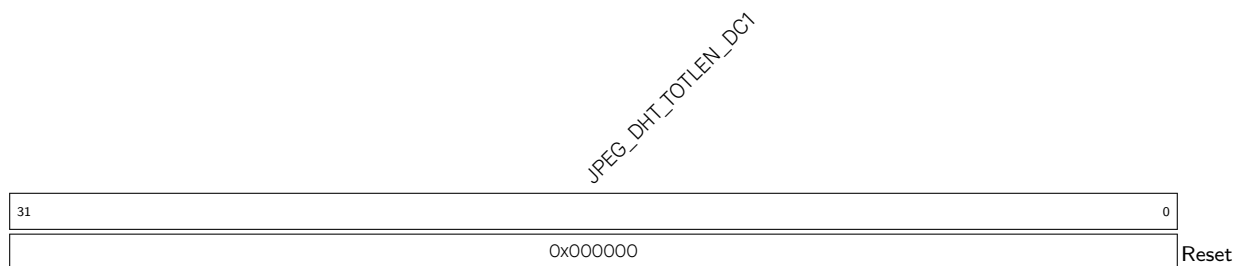
**JPEG\_DHT\_VAL\_DCO** Configures the symbols corresponding to the decoded codeword for DCO Huffman table in FIFO mode. (HRO)

**Register 31.20. JPEG\_DHT\_TOTLEN\_ACO\_REG (0x0060)**

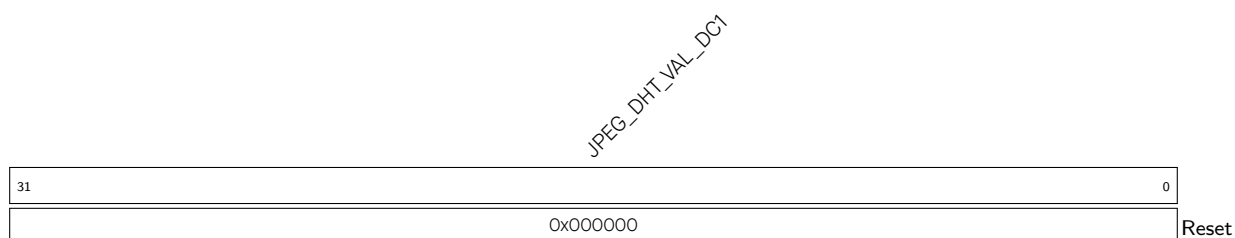
**JPEG\_DHT\_TOTLEN\_ACO** Configures the number of codeword with a codeword length of 1 to 16 bits for ACO Huffman table in FIFO mode. (HRO)

**Register 31.21. JPEG\_DHT\_VAL\_ACO\_REG (0x0064)**

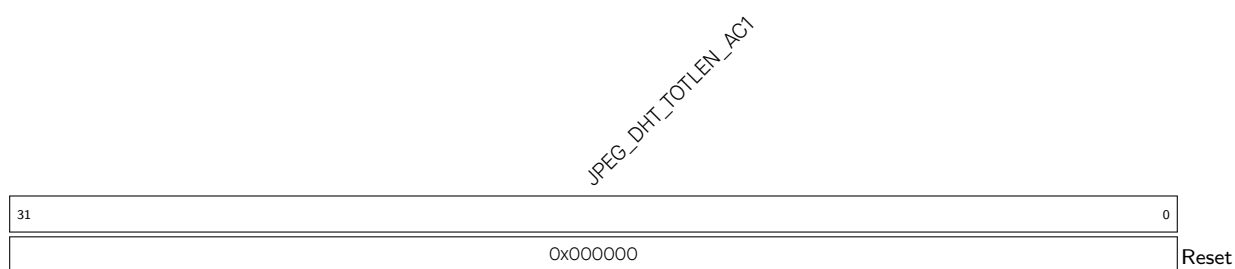
**JPEG\_DHT\_VAL\_ACO** Configures the symbols corresponding to the decoded codeword for ACO Huffman table in FIFO mode. (HRO)

**Register 31.22. JPEG\_DHT\_TOTLEN\_DC1\_REG (0x0068)**

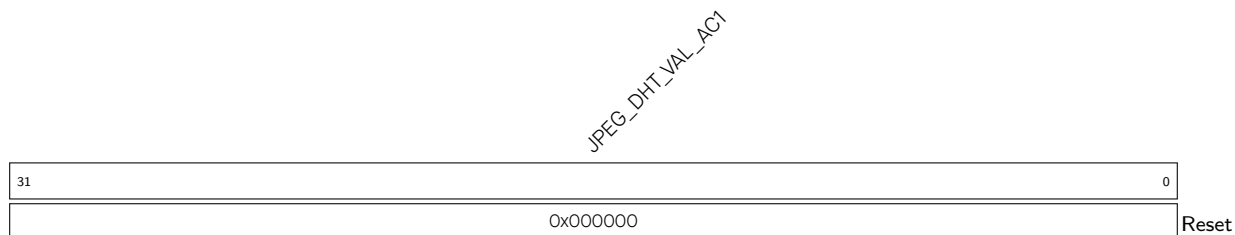
**JPEG\_DHT\_TOTLEN\_DC1** Configures the number of codeword with a codeword length of 1 to 16 bits for DC1 Huffman table in FIFO mode. (HRO)

**Register 31.23. JPEG\_DHT\_VAL\_DC1\_REG (0x006C)**

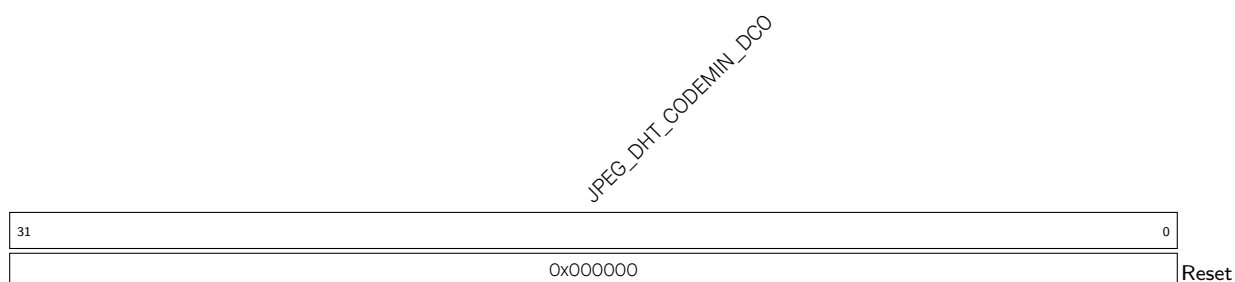
**JPEG\_DHT\_VAL\_DC1** Configures the symbols corresponding to the decoded codeword for DC1 Huffman table in FIFO mode. (HRO)

**Register 31.24. JPEG\_DHT\_TOTLEN\_AC1\_REG (0x0070)**

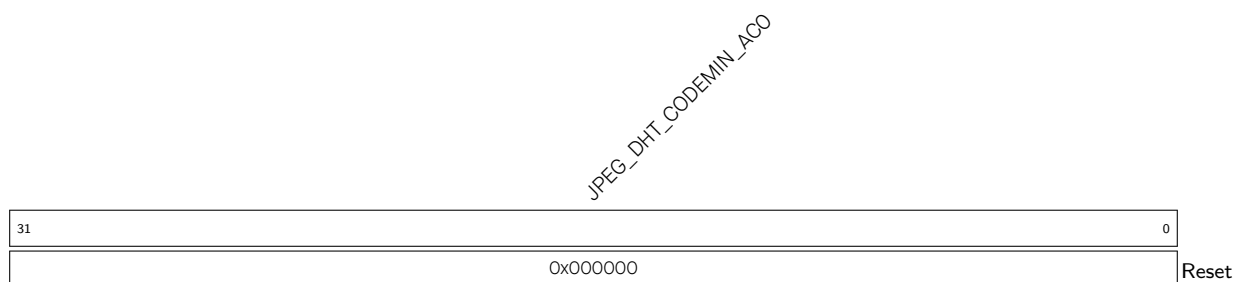
**JPEG\_DHT\_TOTLEN\_AC1** Configures the number of codeword with a codeword length of 1 to 16 bits for AC1 Huffman table in FIFO mode. (HRO)

**Register 31.25. JPEG\_DHT\_VAL\_AC1\_REG (0x0074)**

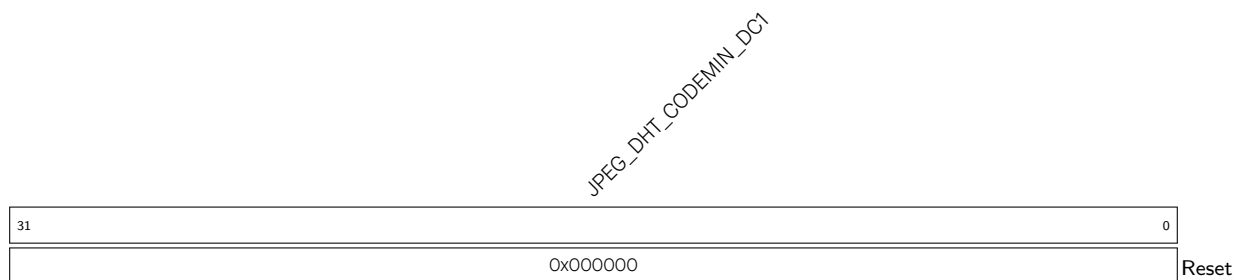
**JPEG\_DHT\_VAL\_AC1** Configures the symbols corresponding to the decoded codeword for AC1 Huffman table in FIFO mode. (HRO)

**Register 31.26. JPEG\_DHT\_CODEMIN\_DCO\_REG (0x0078)**

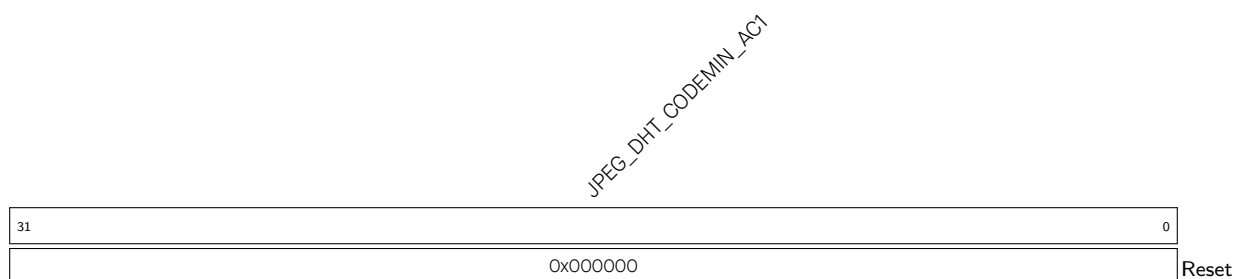
**JPEG\_DHT\_CODEMIN\_DCO** Configures the minimum codeword with a codeword length of 1 to 16 bits for DCO Huffman table in FIFO mode. The codeword should be left shifted to the MSB position of a 16-bit word. (HRO)

**Register 31.27. JPEG\_DHT\_CODEMIN\_ACO\_REG (0x007C)**

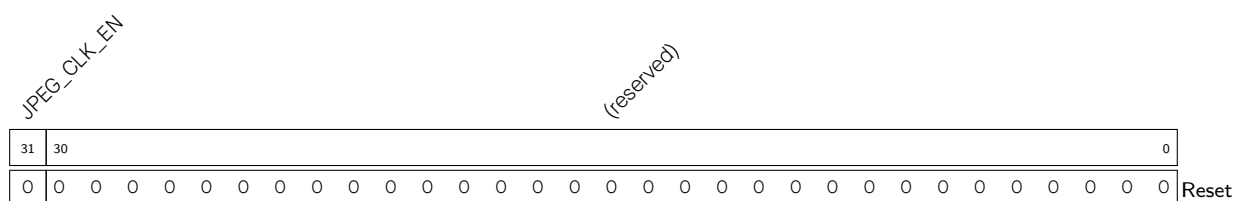
**JPEG\_DHT\_CODEMIN\_ACO** Configures the minimum codeword with a codeword length of 1 to 16 bits for ACO Huffman table in FIFO mode. The codeword should be left shifted to the MSB position of a 16-bit word. (HRO)

**Register 31.28. JPEG\_DHT\_CODEMIN\_DC1\_REG (0x0080)**

**JPEG\_DHT\_CODEMIN\_DC1** Configures the minimum codeword with a codeword length of 1 to 16 bits for DC1 Huffman table in FIFO mode. The codeword should be left shifted to the MSB position of a 16-bit word. (HRO)

**Register 31.29. JPEG\_DHT\_CODEMIN\_AC1\_REG (0x0084)**

**JPEG\_DHT\_CODEMIN\_AC1** Configures the minimum codeword with a codeword length of 1 to 16 bits for AC1 Huffman table in FIFO mode. The codeword should be left shifted to the MSB position of a 16-bit word. (HRO)

**Register 31.30. JPEG\_SYS\_REG (0x00F8)**

**JPEG\_CLK\_EN** Configures whether or not to force open register clock gate.

0: Open the clock gate only when the application writes registers

1: Force open the clock gate for register

(R/W)

Register 31.31. JPEG\_VERSION\_REG (0x00FC)

|            |    |    |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|----|----|---|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |    |    |   | JPEG_JPEG_VER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         | 28 | 27 |   |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0  | 0  | 0 | 0x2111190     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

JPEG\_JPEG\_VER   Version control. (R/W)

## Chapter 32

# Image Signal Processor (ISP)

## 32.1 Introduction

ESP32-P4 includes an image signal processor (ISP), which is a pipeline composed of various image processing algorithms.

ISP reads image data from the DVP or MIPI-CSI camera interface, or from the system memory directly, and writes the processed image data to the system memory through VDMA.

The SoC architecture of ISP is shown in Figure 32.1-1. ISP must work with other modules to read and write data and can not work alone.

- When outputting images, ISP uses CSI\_Bridge to convert data to AXI interface and stores the images to system memory through the VDMA controller. For more information about VDMA, see Chapter 4 [VDMA Controller \(VDMA\)](#)
- When the input image comes from the system memory, ISP must acquire the image data through VDMA
- When the input image comes from the MIPI-CSI camera interface, ISP must acquire the image data through CSI HOST. For details, see Chapter 35 [MIPI CSI](#)
- When the input image comes from the DVP camera interface, ISP acquire the image data through the DVP IO. For details, see Chapter 8 [GPIO Matrix and IO MUX](#)

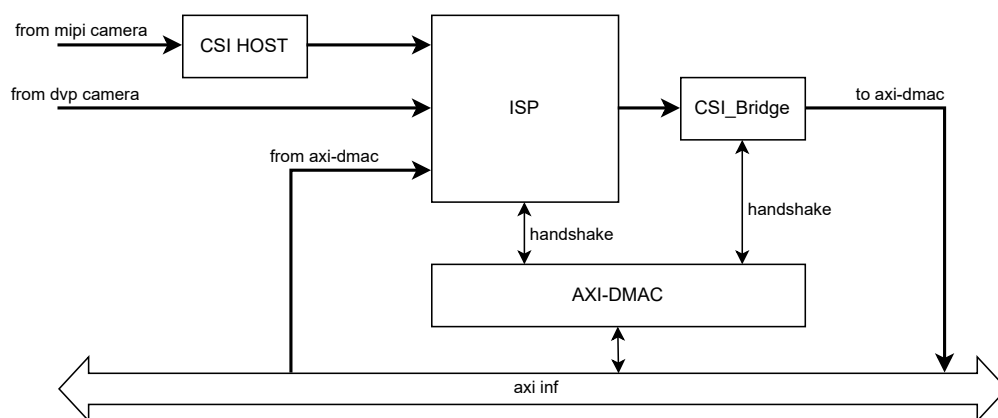


Figure 32.1-1. ESP32-P4 ISP Architecture

## 32.2 Terminology

**MIPI-CSI** Camera serial interface, a high-speed serial interface for cameras complaint with MIPI specifications  
**Image Interface** Image data interface, the output interface of CSI HOST

|            |   |
|------------|---|
|            | Classified into Image Interface 32 and Image Interface 64 based on bit width  |
| <b>DVP</b> | Digital video parallel interface, generally composed of vsync, hsync, de, and data signals  |
| <b>RAW</b> | Unprocessed data directly output from an image sensor, typically divided into R, Gr, Gb, and B channels<br>Classified into RAW8, RAW10, RAW12, etc., based on bit width |
| <b>RGB</b> | Colored image format composed of red, green, and blue colors<br>Classified into RGB888, RGB565, etc., based on the bit width of each color                              |
| <b>YUV</b> | Colored image format composed of luminance and chrominance<br>Classified into YUV444, YUV422, YUV420, etc., based on the data arrangement                               |

## 32.3 Feature List

ISP supports the following features:

- maximum resolution: 1920 x 1080
- three input channels: MIPI-CSI, DVP, and VDMA
- input formats: RAW8, RAW10, and RAW12
- output formats: RAW8, RGB888, RGB565, YUV422, and YUV420
- pipeline features:
  - Bayer filter (BF)
  - Lens shading correction (LSC)
  - Demosaic
  - Color correction matrix (CCM)
  - Gamma correction
  - RGB2YUV
  - Sharpen
  - Contrast/hue/saturation/luminance adjustment (COLOR)
  - YUV\_limit
  - YUV2RGB
  - Automatic exposure statistics (AE)
  - Automatic focus statistics (AF)
  - Automatic white balance statistics (AWB)
  - Histogram statistics (HIST)

## 32.4 Architectural Overview

ISP architecture is shown in Figure 32.4-1, consisting of ISP\_Header, ISP\_Pipeline, ISP\_Tail, and CSI\_Bridge.

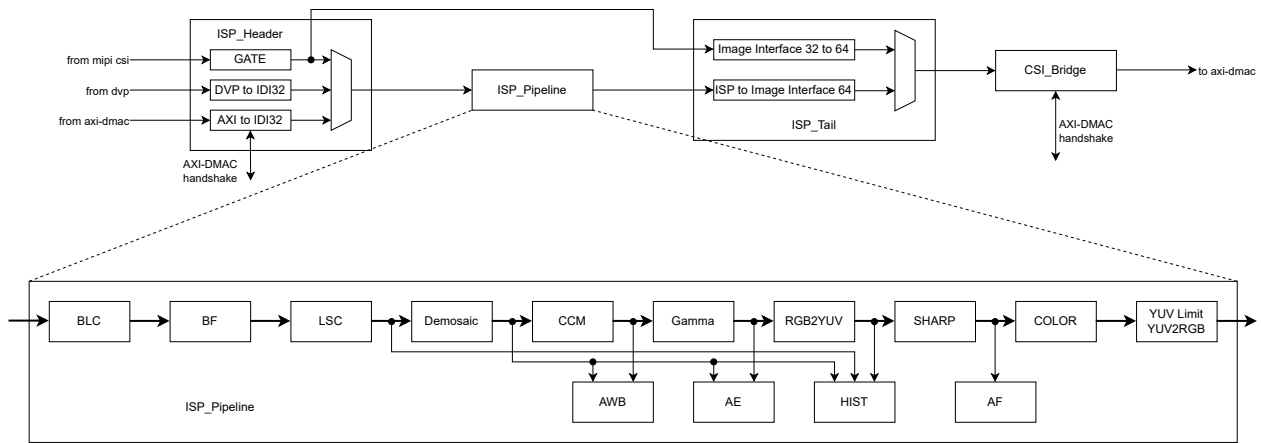


Figure 32.4-1. ISP Architecture

- ISP\_Header selects data from various input sources based on the configuration and buffers it. Then it transmits the buffered data to ISP\_Pipeline in a standardized format.
- ISP\_Pipeline serves as the core module of the ISP, containing all the algorithms for image processing.
- ISP\_Tail has two input sources, MIPI-CSI and ISP\_Pipeline. When ISP is disabled, Image Interface 32 data from MIPI-CSI is converted into Image Interface 64 format by ISP\_Tail and transmitted to CSI\_Bridge. When ISP is enabled, the output of ISP\_Pipeline is cropped and converted into Image Interface 64 format by ISP\_Tail, and then transmitted to CSI\_Bridge.
- As the output of the ISP, CSI\_Bridge transmits the images from ISP to the system memory through VDMA.

## 32.5 Functional Description

### 32.5.1 ISP\_Header

ISP\_Header serves as the input of ISP. The main features are:

- Select image data as input source based on the configuration of [ISP\\_IN\\_SRC](#)
- Buffer image data, and convert images to the format required by ISP\_Pipeline based on the configured type and size of image data
  - When MIPI-CSI is the input, set the input type via [ISP\\_DATA\\_TYPE](#)
  - When DVP is the input, set [ISP\\_DATA\\_TYPE](#) to 0, then set the data type via [ISP\\_CAM\\_DATA\\_TYPE](#)
  - When VDMA is the input, set the input type via [ISP\\_DATA\\_TYPE](#), and configure [ISP\\_DMA\\_DATA\\_TYPE](#) accordingly

### 32.5.2 ISP\_Pipeline

ISP\_Pipeline is the core of ISP, housing all the image processing algorithms. Each algorithm module can be enabled or disabled via the corresponding bit of [ISP\\_CNTL\\_REG](#). Except for modules related to color space conversion (demosaic, RGB2YUV, and YUV2RGB), other modules can be enabled or disabled dynamically without the need to shut down the ISP for reconfiguration. Moreover, once enabled, each algorithm module



generates an end-of-frame interrupt, capable of triggering an interrupt after processing each image frame.

### 32.5.2.1 Bayer Filter (BF)

This module is designed for denoising input images in the Bayer domain. The denoising strength can be adjusted using [ISP\\_SIGMA](#), and the denoising template can be fine-tuned using [ISP\\_GAU\\_TEMPLATE<sub>xx</sub>](#).

### 32.5.2.2 Lens Shading Correction (LSC)

This module is utilized for lens shading correction in the Bayer domain. It corrects the R, Gr, Gb, and B channels independently by dividing each channel into a 32 x 32 grid (equivalent to a 64 x 64 division for the entire image) and stores the correction coefficients for each channel in a lookup table (LUT).

Before using this module, calibration is necessary to obtain the LUT correction coefficients. Specifically, first we capture a white image in a scene with uniform ambient lighting. Divide the image into a 32 x 32 grid for each channel, and use the luminance at the center of the image as a reference. Calculate the luminance gain at each grid vertex based on this reference luminance. For grids extending beyond the image boundaries on the right or bottom, calculate the gain at the image boundary points. Then, use a linear relationship based on the gain of the previous point to calculate the gain at the next grid boundary. Finally, store these gains in the LUT in a left-to-right, top-to-bottom order to complete the initialization.

In the context of a 1920 x 1080 resolution image, each channel operates at 960 x 540 resolution and is divided into a 32 x 32 grid, consisting of 30 grids horizontally and 17 grids vertically. Assuming the image's luminance center aligns with its geometric center, we derive the reference luminance *ref\_lum* from the average luminance of pixels around coordinates (480, 270). Moving methodically from left to right and top to bottom, derive the actual pixel luminance *act\_lum* for each grid vertex. Using the formula  $gain = ref\_lum / act\_lum$ , we compute the correction coefficient, which is then stored sequentially in the LUT.

In cases where grids extend beyond the image boundaries, such as the vertical coordinate of the last grid reaching 543 (beyond the maximum vertical coordinate of 539), we leverage the correction coefficients *gain\_0* at coordinate 511 and *gain\_1* at coordinate 539. Then the gain for coordinate 543 can be calculated based on  $gain = gain\_0 + (gain\_1 - gain\_0) / (539 - 511) * (543 - 511)$ .

LSC employs two LUTs for storing gains related to specific color channels: Gb and B are stored in one LUT, while R and Gr are stored in the other. The gain values are represented as 10-bit fixed-point numbers, with the high 2 bits representing the integer part and the low 8 bits the fractional part. The storage order within the LUTs is detailed in Table 32.5-1. The LUTs can be accessed through specific registers:

- A write operation writes the data from [ISP\\_LUT\\_WDATA\\_REG](#) into the LUT.
- A read operation stores the data read from the LUT into [ISP\\_LUT\\_RDATA\\_REG](#).
- Trigger LUT operations via [ISP\\_LUT\\_CMD\\_REG](#). Each write to this register initiates a read or write operation on the LUT. It is required to write to all the fields within this register at the same time.

Table 32.5-1. Gain Storage Sequence in LSC LUTs

| LUT sel  | bit [19:10] | bit [9:0] |
|----------|-------------|-----------|
| LUT_Gb_B | Gb          | B         |
| LUT_R_Gr | R           | Gr        |

Before enabling LSC, `ISP_LSC_XTABLESIZE` should be configured to set the number of horizontal correction coefficients. The number is determined by  $ISP\_LSC\_XTABLESIZE = \text{fix}((line\_width - 1)/2/32) + 2$ , where  $\text{fix}()$  denotes rounding down. For example, if the input RAW image has a horizontal width of 1920 pixels, then  $ISP\_LSC\_XTABLESIZE = \text{fix}((1920 - 1)/2/32) + 2 = 29 + 2 = 31$ .

### 32.5.2.3 Demosaic

The demosaicing process converts Bayer images to RGB888 images. The conversion effect can be fine-tuned using `ISP_DEMOSAIC_GRAD_RATIO`. This register field comprises 2 integer bits and 4 fractional bits, with a default value of 1.0.

### 32.5.2.4 Color Correction Matrix (CCM)

CCM is a correction matrix for image pixels that can adjust RGB888 pixels, including white balance adjustments. The relationship between the output R', G', B' and the input R, G, B is described by the following matrix. The parameters RR, RG, RB, GR, GG, GB, BR, BG, and BB can be configured with `ISP_CCM_xx`. Each parameter is a 13-bit fixed-point number, where bit [12] is the sign bit, bits [11:0] represent the absolute value of the number, bits [11:10] the integer part, and bits [9:0] the fractional part.

$$\begin{bmatrix} R' \\ G' \\ B' \end{bmatrix} = \begin{bmatrix} RR & RG & RB \\ GR & GG & GB \\ BR & BG & BB \end{bmatrix} \times \begin{bmatrix} R \\ G \\ B \end{bmatrix} \quad (32.1)$$

### 32.5.2.5 Gamma Correction

This module is used to adjust the gamma curve of an image. The gamma curve should be configured before gamma correction is enabled. Gamma curves can be configured using registers, with each R, G, B channel having an independent curve consisting of 16 sampling points. For the X component (input value), the values are indirectly obtained through `ISP_GAMMA_R/G/B_Xn` (where n ranges from 00 to 0F). The Y component (output value) can be directly set using `ISP_GAMMA_R/G/B_Yn` (where n ranges from 00 to 0F). Once configuration is complete, writing 1 to `ISP_GAMMA_UPDATE` applies the gamma curve settings. The gamma curve is illustrated in Figure 32.5-1.

For the X component, taking the R channel as an example,

$ISP\_GAMMA\_R\_X(n) = \log_2(X(n) - X(n-1))$ . This means the nth X coordinate value is obtained by adding 2 to the power of `ISP_GAMMA_R_X(n)` to the (n-1)th X coordinate value. Specifically, for the last coordinate,  $X(0F) = 2^{ISP\_GAMMA\_R\_X(0F)} + X(0E) - 1$ . Since RGB888 in ISP uses 8-bit integers, only the configuration where  $X(0F) = 255$  is considered a valid configuration.

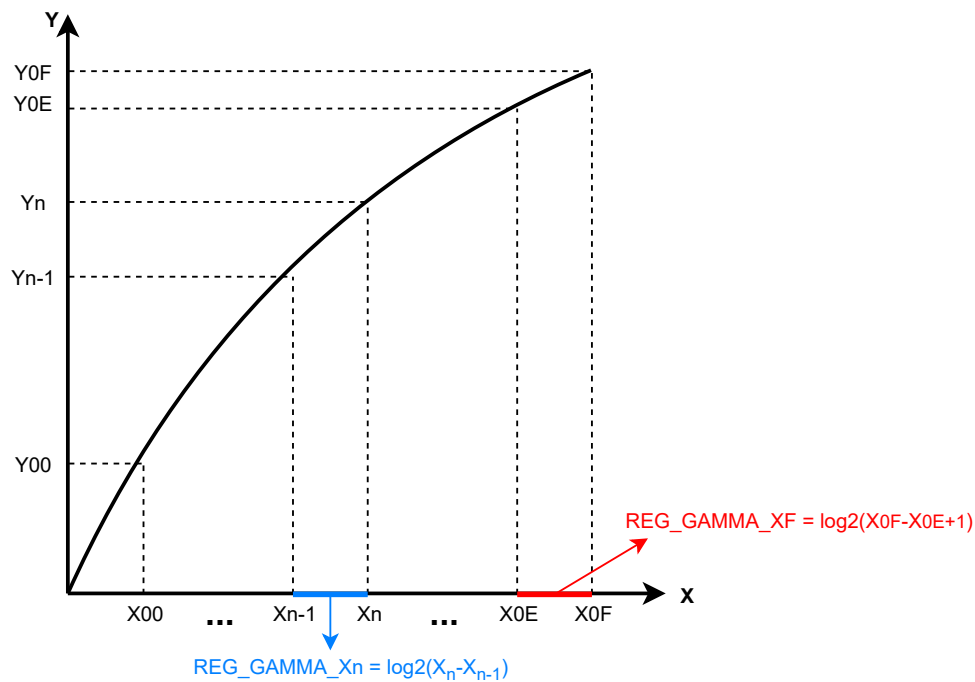


Figure 32.5-1. Gamma Curve

### 32.5.2.6 RGB2YUV

The RGB2YUV module converts RGB888 pixels into full-range YUV422 format. The conversion protocol can be configured with [ISP\\_YUV\\_MODE](#).

### 32.5.2.7 Sharpen

The sharpen module is used to sharpen images. This module separates the low-frequency and high-frequency components of the image using a low-pass filter template (such as a mean template or Gaussian template) via [ISP\\_SHARP\\_FILTER\\_COEFF](#). For low-frequency components, no processing will be done. For high-frequency components, each pixel undergoes the following processing to achieve sharpening:

- Pixels with frequencies below [ISP\\_SHARP\\_THRESHOLD\\_LOW](#) are set to 0.
- Pixels with frequencies above [ISP\\_SHARP\\_THRESHOLD\\_LOW](#) but below [ISP\\_SHARP\\_THRESHOLD\\_HIGH](#) are multiplied by the coefficient [ISP\\_SHARP\\_AMOUNT\\_LOW](#).
- Pixels with frequencies above [ISP\\_SHARP\\_THRESHOLD\\_HIGH](#) are multiplied by the coefficient [ISP\\_SHARP\\_AMOUNT\\_HIGH](#).

At the end of each frame, the maximum value of high-frequency component pixels in that frame can be obtained by reading [ISP\\_SHARP\\_GRADIENT\\_MAX](#). This value can serve as a reference for configuring settings for the next frame.

### 32.5.2.8 Contrast/Hue/Saturation/Luminance Adjustment (COLOR)

This module is designed to modify the contrast, saturation, hue, and luminance of an image using the following registers [ISP\\_COLOR\\_CONTRAST](#), [ISP\\_COLOR\\_HUE](#), [ISP\\_COLOR\\_SATURATION](#), and [ISP\\_COLOR\\_BRIGHTNESS](#).

32.5.2.9 YUV\_Limit and YUV2RGB

The YUV\_Limit module converts full-range YUV422 pixels to limited-range YUV422 pixels. This module is activated only when RGB2YUV is enabled, YUV2RGB is disabled, and [ISP\\_YUV\\_RANGE](#) is set to 1. With this configuration, the ISP output type is either YUV422 or YUV420.

YUV2RGB converts full-range YUV422 pixels to RGB888 format. The conversion protocol can be configured with [ISP\\_YUV\\_MODE](#).

**Note:**

For full-range YUV, Y, U, and V channels range from 0 to 255.

For limited-range YUV, Y channel ranges from 16 to 235, and U and V channels range from 16 to 240.

32.5.2.10 Automatic Exposure Statistics (AE)

Auto Exposure (AE) uses 25 statistical sub-windows for image luminance statistics, forming a 5 x 5 grid of statistical window. The size of these windows is set using the register [ISP\\_AE\\_BX/BY\\_REG](#). Each sub-window is numbered as shown in Figure 32.5-2. The average luminance of each sub-window, represented as an 8-bit value, can be read with [ISP\\_AE\\_Bxx\\_MEAN](#). These statistics can be utilized to implement automatic exposure algorithms for cameras.

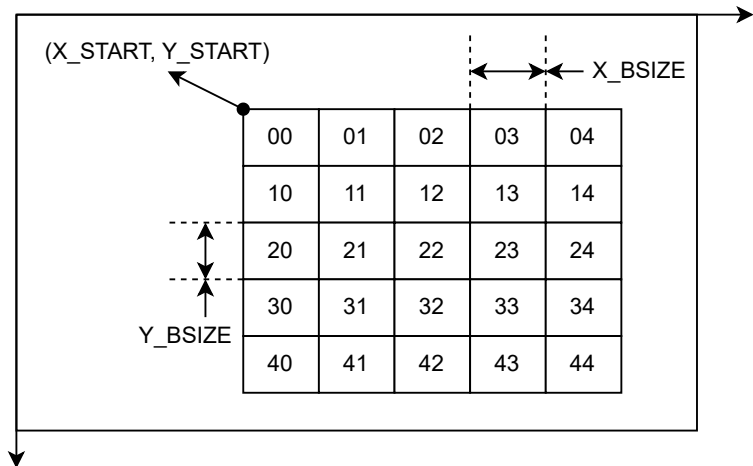


Figure 32.5-2. Sub-Window Numbering

AE utilizes two data sampling points: the output of the [Demosaic](#) module and the output of the [Gamma](#) module. These sampling points can be configured using [ISP\\_AE\\_SELECT](#).

AE also includes a simple luminance monitoring module, implemented either by hardware or software. This module calculates the average luminance of all sub-windows every [ISP\\_AE\\_MONITO\\_RPERIOD](#) frames. If the average luminance falls outside the thresholds set by [ISP\\_AE\\_MONITOR\\_TH/TL](#), interrupt for AE luminance monitoring will be triggered. Note that the luminance monitoring module does not support setting different weights for individual sub-windows. Therefore, if you wish to implement monitoring with different weights (for instance, prioritize highlights), you need to perform software-triggered manual statistics and process the statistical data accordingly.

### 32.5.2.11 Automatic Focus Statistics (AF)

AF gathers luminance and sharpness information within specified statistical windows based on the output of the [sharpen](#) module. There are 3 independent statistical windows, and the size and position of each window can be configured using [ISP\\_AF\\_H/VSCALE\\_A/B/C\\_REG](#). The module supports automatic and manual trigger modes for statistics collection. The results of luminance and sharpness statistics for each window can be accessed using [ISP\\_AF\\_LUMA/B/C](#) and [ISP\\_AF\\_SUMA/B/C](#). These statistics can be used to implement automatic focus algorithms for cameras.

AF also includes a focus scene monitoring module, which users can choose to implement hardware-based monitoring with this module or implement via software. This module evaluates cumulative changes in luminance and sharpness across all statistical windows as criteria. It performs statistics every [ISP\\_AF\\_ENV\\_PERIOD](#) frames. If consecutive statistics show a difference from baseline values for luminance and sharpness that exceeds the specified threshold, an interrupt is triggered indicating a change in the focus scene that requires refocusing. The baseline values are automatically updated after each automatic or manually triggered statistics collection. There are three methods for setting the threshold:

- Directly set the luminance and sharpness thresholds using [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_LUM](#) and [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_SUM](#)
- If [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_SUM](#) is 0, use the corresponding baseline sharpness value multiplied by [ISP\\_AF\\_ENV\\_THRESHOLD](#) (4 fractional bits) as the sharpness threshold
- If [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_LUM](#) is 0, use the corresponding baseline luminance value multiplied by [ISP\\_AF\\_ENV\\_THRESHOLD](#) (4 fractional bits) as the luminance threshold

### 32.5.2.12 Automatic White Balance Statistics (AWB)

AWB gathers white balance information for specified windows containing white patches. The coordinates of the window can be set using [ISP\\_AWB\\_H/VSCALE\\_REG](#). White patches are filtered based on luminance limits [ISP\\_AWB\\_MAX/MIN\\_LUM](#), *R/G* limits [ISP\\_AWB\\_MAX/MIN\\_RG](#), and *B/G* limits [ISP\\_AWB\\_MAX/MIN\\_BG](#).

The statistics include the number of white patches and the accumulated values of the R, G, B components for all white patches. These statistics can be obtained using [ISP\\_AWBO\\_WHITE\\_CNT](#) and [ISP\\_AWBO\\_ACC\\_R/G/B](#). They can be used to implement automatic white balance algorithms in cameras.

AWB relies on two data sampling points: the output of [Demosaic](#) and the output of [CCM](#), which can be configured with [ISP\\_AWB\\_SAMPLE](#).

### 32.5.2.13 Histogram Statistics (HIST)

HIST calculates brightness information for the image through statistical analysis. This module can define a statistical window, which can be divided into 5 x 5 sub-windows similar to AE. The configuration is done using registers [ISP\\_HIST\\_OFFSETS\\_REG](#) and [ISP\\_HIST\\_SIZE\\_REG](#). The weight of each sub-window can be independently adjusted with [ISP\\_HIST\\_WEIGHT\\_xx](#).

The statistics are presented as a histogram with 16 intervals. The x-axis of the histogram is defined using [ISP\\_HIST\\_SEG\\_x\\_x](#), and the final statistics can be retrieved using [ISP\\_HIST\\_BIN\\_x](#).

HIST involves three data sampling points: [BF](#), [demosaic](#), and [RGB2YUV](#), corresponding to RAW, RGB, and YUV data sampling points respectively. These can be configured using [ISP\\_HIST\\_MODE](#). When the sampling point

is set to RGB, RGB weighting coefficients can be adjusted via [ISP\\_HIST\\_COEFF\\_R/G/B](#).

### 32.5.3 ISP\_Tail

ISP\_Tail is the post-processing section that handles data from two input sources, ultimately outputting in Image Interface 64 format to CSI\_Bridge.

When the ISP is turned off, ISP\_Tail receives Image Interface 32 data from the MIPI CSI HOST, converts it to Image Interface 64 format, and outputs it to CSI\_Bridge. The byte order of the input Image Interface 32 data can be adjusted using [ISP\\_BYTE\\_ENDIAN\\_ORDER](#).

When the ISP is turned on, ISP\_Tail receives data from ISP\_Pipeline and processes them before outputting to CSI\_Bridge. This processing includes:

- Converting RGB888 to RGB565 based on register configurations
- Converting YUV422 to YUV420 based on register configurations
- Converting data from ISP\_Pipeline to Image Interface 64 format

### 32.5.4 Sequence Control

For modules involving matrix operations, it is necessary to buffer multiple lines of data before starting operations. In such cases, it is crucial for the module to generate an output sequence when the last few lines of image data are buffered. This output sequence can be controlled using

[ISP\\_BF/DEMOSAIC/SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TH/TL](#), to prevent buffer overflow in the CSI\_Bridge due to excessive speed. Please exercise caution when setting this register too large, as it may disrupt the normal data sequence. TH must be smaller than [ISP\\_HADR\\_NUM](#)-1, and it is recommended to set [ISP\\_BF/DEMOSAIC/SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TH/TL](#) to a value less than or equal to 8.

### 32.5.5 CSI\_Bridge

CSI\_Bridge serves as the interface between the ISP and the system memory. This module utilizes VDMA to transmit data from the ISP into the system memory. The image can be transferred either as a single block or divided into multiple blocks, which can be configured via [CSI\\_BRIG\\_DMA\\_BURST\\_LEN](#) and [CSI\\_BRIG\\_DMABLK\\_SIZE](#).

- [CSI\\_BRIG\\_DMA\\_BURST\\_LEN](#) configures the amount of 64-bit data in a VDMA burst transfer.
- [CSI\\_BRIG\\_DMABLK\\_SIZE](#) configures the number of VDMA bursts in a VDMA block transfer. If an image frame is transferred with only one block, and this block contains  $n$  VDMA bursts, then configure this field to a value greater than  $n$ . It is recommended to set it to the maximum value, 0xFFFF.

### 32.5.6 Color Mode and Byte Order

#### 32.5.6.1 Output Pixel Layout Format

When the ISP is disabled, ISP\_Tail directly receives Image Interface 32 data from the MIPI CSI HOST. The pixel layout can be referenced from Chapter [35 MIPI CSI](#). In this case, the Image Interface 32 data output from CSI HOST can go through two levels of byte ordering in ISP\_Tail and CSI\_Bridge, refer to [Byte Order](#) for details.

After the ISP is enabled and the data has been processed by the ISP\_Pipeline, the layout format of the output pixel is as shown in Table 32.5-2.

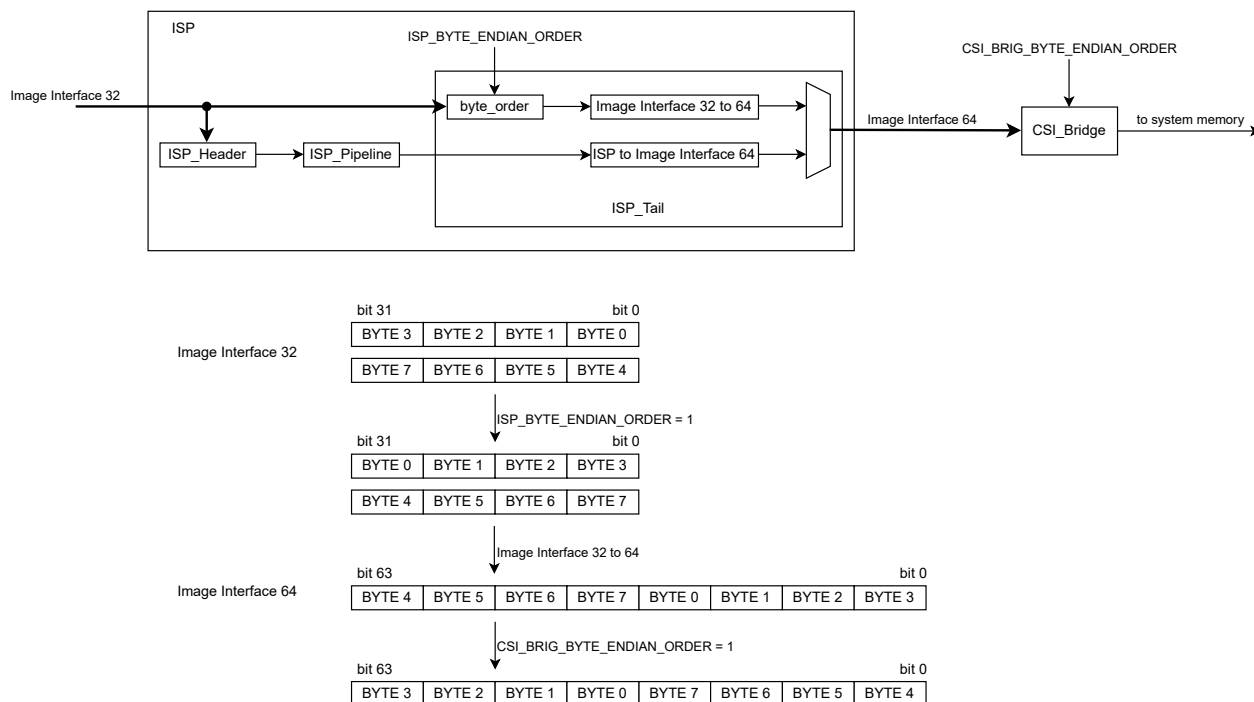
Table 32.5-2. ISP Output Pixel Layout Format

| Color Mode                        | Addr + 7       | Addr + 6       | Addr + 5       | Addr + 4       | Addr + 3       | Addr + 2       | Addr + 1       | Addr + 0       |
|-----------------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| RAW8                              | RAW7[7:0]      | RAW6[7:0]      | RAW5[7:0]      | RAW4[7:0]      | RAW3[7:0]      | RAW2[7:0]      | RAW1[7:0]      | RAW0[7:0]      |
| RGB888                            | G2[7:0]        | B2[7:0]        | R1[7:0]        | G1[7:0]        | B1[7:0]        | R0[7:0]        | G0[7:0]        | B0[7:0]        |
|                                   | B5[7:0]        | R4[7:0]        | G4[7:0]        | B4[7:0]        | R3[7:0]        | G3[7:0]        | B3[7:0]        | R2[7:0]        |
|                                   | R7[7:0]        | G7[7:0]        | B7[7:0]        | R6[7:0]        | G6[7:0]        | B6[7:0]        | R5[7:0]        | G5[7:0]        |
| RGB565                            | R3[4:0]G3[5:3] | G3[2:0]B3[4:0] | R2[4:0]G2[5:3] | G2[2:0]B2[4:0] | R1[4:0]G1[5:3] | G1[2:0]B1[4:0] | R0[4:0]G0[5:3] | G0[2:0]B0[4:0] |
| YUV422                            | Y3[7:0]        | V2[7:0]        | Y2[7:0]        | U2[7:0]        | Y1[7:0]        | V0[7:0]        | Y0[7:0]        | U0[7:0]        |
| YUV420<br>(Odd-numbered<br>rows)  | Y4[7:0]        | U4[7:0]        | Y3[7:0]        | Y2[7:0]        | U2[7:0]        | Y1[7:0]        | Y0[7:0]        | U0[7:0]        |
|                                   | U10[7:0]       | Y9[7:0]        | Y8[7:0]        | U8[7:0]        | Y7[7:0]        | Y6[7:0]        | U6[7:0]        | Y5[7:0]        |
|                                   | Y15[7:0]       | Y14[7:0]       | U14[7:0]       | Y13[7:0]       | Y12[7:0]       | U12[7:0]       | Y11[7:0]       | Y10[7:0]       |
| YUV420<br>(Even-numbered<br>rows) | Y4[7:0]        | V4[7:0]        | Y3[7:0]        | Y2[7:0]        | V2[7:0]        | Y1[7:0]        | Y0[7:0]        | V0[7:0]        |
|                                   | V10[7:0]       | Y9[7:0]        | Y8[7:0]        | V8[7:0]        | Y7[7:0]        | Y6[7:0]        | V6[7:0]        | Y5[7:0]        |
|                                   | Y15[7:0]       | Y14[7:0]       | V14[7:0]       | Y13[7:0]       | Y12[7:0]       | V12[7:0]       | Y11[7:0]       | Y10[7:0]       |

### 32.5.6.2 Byte Order

CSI\_Bridge can reorder the bytes of the input 64-bit data via `CSI_BRIG_BYTE_ENDIAN_ORDER`. ISP\_Tail can also reorder the bytes via `ISP_BYTE_ENDIAN_ORDER`. The byte ordering functionality within ISP\_Tail differs from that of CSI\_Bridge, as illustrated in Figure 32.5-3.

- **ISP\_Tail byte ordering:** This operation applies to its Image Interface 32 input. It reverses the high and low bytes of the 32-bit input data and then concatenates them to output 64-bit data. This step only functions when the ISP is disabled and is mainly used for processing Image Interface 32 YUV422 and YUV420 input types.
- **CSI\_Bridge byte ordering:** This operation acts on the 64-bit input data (i.e., the output data from ISP\_Tail) by reversing its high and low bytes.



## 32.6 Interrupts

ESP32-P4's ISP can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- `isp_interrupt`
- `csi_bridge_interrupt`

There are several internal interrupt sources from ISP that can generate the above interrupt signal. The interrupt sources from ISP are listed with their trigger conditions and the resulted interrupt signal in Table 32.6-1.

**Table 32.6-1. ISP's Internal Interrupt Sources**

| Internal Interrupt Source     | Trigger Condition  | Interrupt Signal           |
|-------------------------------|--|----------------------------|
| ISP_HEADER_IDI_FRAME_INT      | After MIPI-CSI inputs a frame. This interrupt is not affected by whether <a href="#">ISP_MIPI_DATA_EN</a> is enabled | <code>isp_interrupt</code> |
| ISP_TAIL_IDI_FRAME_INT        | After ISP_Tail outputs a frame   | <code>isp_interrupt</code> |
| ISP_YUV2RGB_FRAME_INT         | After module YUV2RGB processes a frame   | <code>isp_interrupt</code> |
| ISP_COLOR_FRAME_INT           | After module contrast/hue/saturation/luminance adjustment processes a frame  | <code>isp_interrupt</code> |
| ISP_SHARP_FRAME_INT           | After module sharpen processes a frame   | <code>isp_interrupt</code> |
| ISP_RGB2YUV_FRAME_INT         | After module RGB2YUV processes a frame   | <code>isp_interrupt</code> |
| ISP_GAMMA_FRAME_INT           | After module gamma correction processes a frame  | <code>isp_interrupt</code> |
| ISP_CCM_FRAME_INT             | After module CCM processes a frame   | <code>isp_interrupt</code> |
| ISP_DEMOSAIC_FRAME_INT        | After module demosaic processes a frame  | <code>isp_interrupt</code> |
| ISP_BF_FRAME_INT              | After module BF processes a frame  | <code>isp_interrupt</code> |
| ISP_LSC_FRAME_INT             | After module LSC processes a frame   | <code>isp_interrupt</code> |
| ISP_FRAME_INT                 | After ISP_Pipeline outputs a frame   | <code>isp_interrupt</code> |
| ISP_HIST_FDONE_INT            | After module HIST processes a frame  | <code>isp_interrupt</code> |
| ISP_AWB_FDONE_INT             | After module AWB processes a frame   | <code>isp_interrupt</code> |
| ISP_AF_ENV_INT                | When module AF detects a change in the focus scene   | <code>isp_interrupt</code> |
| ISP_AF_FDONE_INT              | After module AF processes a frame  | <code>isp_interrupt</code> |
| ISP_AE_FRAME_DONE_INT         | After module AE processes a frame  | <code>isp_interrupt</code> |
| ISP_AE_MONITOR_INT            | When module AE detects a change in the luminance   | <code>isp_interrupt</code> |
| ISP_MIPI_HNUM_UNMATCH_INT     | When the width HNUM settings do not match the actual input from MIPI-CSI   | <code>isp_interrupt</code> |
| ISP_DATA_TYPE_SETTING_ERR_INT | When DATA_TYPE settings do not match the actual input data   | <code>isp_interrupt</code> |



|                                  |   |                      |
|----------------------------------|---|----------------------|
| ISP_HVNUM_SETTING_ERR_INT        | When the width HNUM and the height VNUM settings are incorrect: Image dimensions must be even; with the RAW10 input, HNUM must be a multiple of 4 | isp_interrupt        |
| ISP_BUF_FULL_INT                 | When ISP_Header buffer is full  | isp_interrupt        |
| ISP_ASYNC_FIFO_OVF_INT           | When asynchronous FIFO of ISP_Header is overflowed  | isp_interrupt        |
| ISP_DATA_TYPE_ERR_INT            | When illegal DATA_TYPE is used for input data (not RAW8/RAW10/RAW12)  | isp_interrupt        |
| CSI_BRIG_DMA_CFG_HAS_UPDATED_INT | When VDMA configuration of CSI_Bridge is updated  | csi_bridge_interrupt |
| CSI_BRIG_CSI_ASYNC_FIFO_OVF_INT  | When asynchronous FIFO of CSI_Bridge is overflowed  | csi_bridge_interrupt |
| CSI_BRIG_CSI_BUF_OVERRUN_INT     | When CSI_Bridge buffer is overflowed  | csi_bridge_interrupt |
| CSI_BRIG_DISCARD_INT             | When any frame is discarded in CSI_Bridge   | csi_bridge_interrupt |
| CSI_BRIG_VADR_NUM_LT_INT         | When <a href="#">CSI_BRIG_VADR_NUM</a> is less than the actual value  | csi_bridge_interrupt |
| CSI_BRIG_VADR_NUM_GT_INT         | When <a href="#">CSI_BRIG_VADR_NUM</a> is greater than the actual value   | csi_bridge_interrupt |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [32.8 Register Summary](#).

## 32.7 Programming Procedures

### 32.7.1 ISP Clock Reset Configuration

1. Enable the bus clock for the ISP and CSI\_Bridge modules;
  - Set [HP\\_SYS\\_CLKRST\\_CSI\\_BRG\\_SYS\\_CLK\\_EN](#) to 1 to activate the clock for ISP and CSI\_Bridge
2. Configure the working clock for ISP;
  - Choose the clock source via [HP\\_SYS\\_CLKRST\\_ISP\\_CLK\\_SRC\\_SEL](#)
  - Configure the clock divisor via [HP\\_SYS\\_CLKRST\\_ISP\\_CLK\\_DIV\\_NUM](#)
  - Set [HP\\_SYS\\_CLKRST\\_ISP\\_CLK\\_EN](#) to 1 to activate the ISP working clock
3. Reset ISP and CSI\_Bridge modules.

- Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_CSI\\_BRG](#) to 1 and then 0 to reset ISP and CSI\_Bridge

### 32.7.2 CSI\_Bridge Configuration

1. Set the width and height of the image via [CSI\\_BRIG\\_HADR\\_NUM](#) and [CSI\\_BRIG\\_VADR\\_NUM](#). The width is measured in "64-bit" units, and the height is measured in rows;
2. Set the valid range for DATA\_TYPE via [CSI\\_BRIG\\_DATA\\_TYPE\\_MIN](#) and [CSI\\_BRIG\\_DATA\\_TYPE\\_MAX](#);
3. Specify the burst length via [CSI\\_BRIG\\_DMA\\_BURST\\_LEN](#). Ensure that this value matches the SRC\_MSIZ (length per burst) and SRC\_TR\_WIDTH (data width) of the corresponding VDMA channel. The data width for CSI\_Bridge is measured in "64-bit" units;
4. If the image is transferred in multiple blocks, specify the maximum number of VDMA bursts per block via [CSI\\_BRIG\\_DMABLK\\_SIZE](#);
5. Enable CSI\_Bridge by writing 1 to [CSI\\_BRIG\\_CSI\\_BRIG\\_EN](#).

### 32.7.3 VDMA Configuration

1. Configure the register corresponding to the channel;
  - Set SRC/DST\_MULTBLK\_TYPE to 3 (configure with linked list)
  - Configure TT\_FC
    - For CSI\_Bridge, set TT\_FC to 4 (peripheral to memory with peripheral flow control)
    - For memory to ISP, set TT\_FC to 6 (memory to peripheral with peripheral flow control)
  - Configure HS\_SEL
    - For CSI\_Bridge, set HS\_SEL\_SRC to 0 (peripheral uses hardware handshake), and set HS\_SEL\_DST to 1 (memory uses software handshake)
    - For memory to ISP, set HS\_SEL\_SRC to 1 (memory uses software handshake), and set HS\_SEL\_DST to 0 (peripheral uses hardware handshake)
  - Assign hardware handshake channels
    - For CSI\_Bridge, set SRC\_PER to 1
    - For memory to ISP, set DST\_PER to 2
  - Set SRC/DST\_TR\_WIDTH to 3 (data width of 64 bits)
2. Establish the linked list based on the configured registers.

**Note:**

The VDMA configuration outlined in this section covers essential steps. For detailed procedures, refer to Chapter 4 [VDMA Controller \(VDMA\)](#).

Ensure that image dimensions and start addresses are aligned to 8 bytes.

## 32.7.4 ISP General Configuration

1. Configure the input image size via [ISP\\_HADR\\_NUM](#) and [ISP\\_VADR\\_NUM](#)
2. Set image arrangement mode in the Bayer domain via [ISP\\_BAYER\\_MODE](#);
3. Specify the ISP output data format via [ISP\\_OUT\\_TYPE](#);
4. Configure each module in ISP\_Pipeline. Refer to the corresponding section in [32.5.2](#) for details;
5. Enable the necessary Pipeline modules by setting the fields in register [ISP\\_CNTL\\_REG](#). Ensure that the format conversion-related modules ([Demosaic](#), [RGB2YUV](#), [YUV2RGB](#)) are enabled before enabling the ISP, and that they match the final output format.

## 32.7.5 Enabling ISP for Image Capture from MIPI-CSI

1. Configure ISP and CSI\_Bridge clocks and reset as described in Section [32.7.1](#);
2. Configure CSI\_Bridge as described in Section [32.7.2](#);
3. Configure VDMA as described in Section [32.7.3](#);
4. Configure MIPI CSI HOST according to Chapter [35 MIPI CSI](#);
5. Configure ISP general settings as described in Section [32.7.4](#);
6. Select the input source as MIPI-CSI by setting [ISP\\_IN\\_SRC](#) to 0;
7. Configure the input data type via [ISP\\_DATA\\_TYPE](#);
8. Enable the ISP by setting [ISP\\_EN](#) to 1;
9. Enable MIPI-CSI data input by setting [ISP\\_MIPI\\_DATA\\_EN](#) to 1.

## 32.7.6 Enabling ISP for Image Capture from DVP

1. Configure ISP and CSI\_Bridge clocks and reset as described in Section [32.7.1](#);
2. Configure CSI\_Bridge as described in Section [32.7.2](#);
3. Configure VDMA as described in Section [32.7.3](#);
4. Configure ISP general settings as described in Section [32.7.4](#);
5. Select the input source as DVP by setting [ISP\\_IN\\_SRC](#) to 1;
6. Configure the input data type via [ISP\\_CAM\\_DATA\\_TYPE](#), and write 0 to [ISP\\_DATA\\_TYPE](#);
7. Enable the ISP by setting [ISP\\_EN](#) to 1;
8. Configure the data mode for DVP interface via [ISP\\_CAM\\_CONF\\_REG](#);
9. Reset the DVP interface by setting [ISP\\_CAM\\_RESET](#) to 1, waiting for a period, then setting it to 0;
10. Write 1 to [ISP\\_CAM\\_UPDATE\\_REG](#);
11. Enable the DVP interface by setting [ISP\\_CAM\\_EN](#) to 1;
12. Wait for [ISP\\_CAM\\_UPDATE\\_REG](#) to automatically clear for initialization.

## 32.7.7 Enabling ISP for Image Capture from VDMA

1. Configure ISP and CSI\_Bridge clocks and reset as described in Section [32.7.1](#);
2. Configure CSI\_Bridge as described in Section [32.7.2](#);
3. Configure VDMA as described in Section [32.7.3](#);
4. Configure ISP general settings as described in Section [32.7.4](#);
5. Select the input source as VDMA by setting [ISP\\_IN\\_SRC](#) to 2;
6. Configure the input data type via [ISP\\_DMA\\_DATA\\_TYPE](#) and [ISP\\_DATA\\_TYPE](#);
7. Configure the total amount of raw image data for one frame in "64-bit" units using [ISP\\_DMA\\_RAW\\_NUM\\_TOTAL](#), which value should equal image width x image height x bits per pixel/64. Then, write 1 to [ISP\\_DMA\\_RAW\\_NUM\\_TOTAL\\_SET](#) to activate the configuration;
8. Configure the burst length via [ISP\\_DMA\\_BURST\\_LEN](#), which needs to align with the VDMA configuration;
9. Write 1 to [ISP\\_DMA\\_UPDATE\\_REG](#) to update the VDMA configuration, and wait for the update to complete;
10. Send a frame of data by setting [ISP\\_DMA\\_EN](#) to 1.

## 32.7.8 LSC LUT Configuration

LSC can be configured after the ISP is enabled. Before enabling LSC, initialize the LSC LUT as follows:

1. Write to LUT;
  - Write the data to be stored in the LUT by writing to [ISP\\_LUT\\_WDATA\\_REG](#)
  - Store the data at the specified address by writing to [ISP\\_LUT\\_CMD\\_REG](#)
2. Read from LUT.
  - Retrieve the data stored at the specified address by writing to [ISP\\_LUT\\_CMD\\_REG](#)
  - Obtain the data read from the LUT by reading from [ISP\\_LUT\\_RDATA\\_REG](#)

## 32.7.9 AE Configuration

AE can be configured after the ISP is enabled as follows:

1. Select sampling points via [ISP\\_AE\\_SELECT](#);
2. Set up statistical windows;
  - Set the horizontal starting point with [ISP\\_AE\\_X\\_START](#)
  - Configure the horizontal dimension of each sub-window with [ISP\\_AE\\_X\\_BSIZE](#)
  - Set the vertical starting point with [ISP\\_AE\\_Y\\_START](#)
  - Configure the vertical dimension of each sub-window with [ISP\\_AE\\_Y\\_BSIZE](#)
  - Specify the number of pixels in each sub-window with [ISP\\_AE\\_SUBWIN\\_PIXNUM](#)
  - Set the reciprocal of the number of pixels in each sub-window with [ISP\\_AE\\_SUBWIN\\_RECIP](#) (20 fractional bits)

## 3. Enable luminance monitoring;

- If monitoring is required, set [ISP\\_AE\\_MONITOR\\_TH](#) and [ISP\\_AE\\_MONITOR\\_TL](#) to non-zero values
- Specify the monitoring statistical period in frames via [ISP\\_AE\\_MONITOR\\_PERIOD](#)

4. Enable AE by writing 1 to [ISP\\_AE\\_EN](#);

## 5. Obtain statistics;

- Clear the completion status by writing 1 to [ISP\\_AE\\_FRAME\\_DONE\\_INT\\_CLR](#)
- Initiate statistics by writing 1 to [ISP\\_AE\\_UPDATE](#). Each write to this register resets the frame count for monitoring. It is recommended to disable monitoring before manual statistics and re-enable it after completion to prevent automatic results from overwriting manual results prematurely
- Wait for the statistics to complete
  - Wait for the ISP interrupt triggered by [AE\\_FDONE\\_INT](#)
  - Or query the status using [ISP\\_AE\\_FRAME\\_DONE\\_INT\\_RAW](#)
- Obtain statistics for each sub-window by reading [ISP\\_AE\\_Bxx\\_MEAN](#)

## 6. Perform luminance monitoring.

- Wait for the ISP interrupt triggered by [AE\\_MONITOR\\_INT](#)
- Or query the status using [ISP\\_AE\\_MONITOR\\_INT\\_RAW](#)
- After detecting a change in luminance, disable luminance monitoring, re-initiate camera exposure, and then re-enable monitoring

### 32.7.10 AF Configuration

AF can be configured after the ISP is enabled as follows:

## 1. Set up three statistical windows A, B, and C, ensuring each window does not exceed 1024 x 1024;

- Set the left boundary using [ISP\\_AF\\_LPOINT\\_A/B/C](#)
- Set the right boundary using [ISP\\_AF\\_RPOINT\\_A/B/C](#)
- Set the top boundary using [ISP\\_AF\\_TPOINT\\_A/B/C](#)
- Set the bottom boundary using [ISP\\_AF\\_BPOINT\\_A/B/C](#)

2. Set the sharpness threshold via [ISP\\_AF\\_THRESHOLD](#);

## 3. Configure focus scene monitoring;

- If focus scene monitoring is required, set the monitoring period [ISP\\_AF\\_ENV\\_PERIOD](#) to a non-zero value
- There are two ways to set the threshold
  - If [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_SUM](#) or [ISP\\_AF\\_ENV\\_USER\\_THRESHOLD\\_LUM](#) is non-zero, use the specified values as thresholds for sharpness and brightness changes

- If `ISP_AF_ENV_USER_THRESHOLD_SUM` or `ISP_AF_ENV_USER_THRESHOLD_LUM` is zero, use the sharpness and brightness of the most recent statistics multiplied by `ISP_AF_ENV_THRESHOLD` (4 fractional bits) as the change threshold
4. Configure the statistical trigger mode. After each trigger completes, update the monitoring baseline;
    - If `ISP_AF_AUTO_UPDATE` is 1, it is in automatic triggering mode, which performs statistics for every frame with AF enabled. Since each statistical calculation clears the frame count for monitoring, the monitoring will be disabled
    - If `ISP_AF_AUTO_UPDATE` is 0, it is in manual triggering mode. The monitoring is working only under this condition
  5. Enable AF by writing 1 to `ISP_AF_EN`;
  6. Obtain statistics;
    - Clear the completion status by writing 1 to `ISP_AF_FDONE_INT_CLR`
    - Trigger statistics
      - With automatic triggering, statistics are performed for every frame
      - With manual triggering, write 1 to `ISP_AF_MANUAL_UPDATE` to trigger statistics manually
    - Wait for the statistics to complete
      - Wait for the ISP interrupt triggered by `AF_FDONE_INT`.
      - Or query the status using `ISP_AF_FDONE_INT_RAW`
    - Obtain sharpness statistics by reading `ISP_AF_SUMA/B/C` and obtain brightness statistics by reading `ISP_AF_LUMA/B/C`
  7. Performs focus scene monitoring.
    - Wait for the ISP interrupt triggered by `AF_ENV_INT`
    - Or query the status using `ISP_AF_ENV_INT_RAW`
    - After detecting a change in the focus scene, disable monitoring, refocus the camera, and then re-enable monitoring

### 32.7.11 AWB Configuration

AWB can be configured after the ISP is enabled.

1. Select sampling points via `ISP_AWB_SAMPLE` and write 1 to `ISP_AWB_MODE`;
2. Set up statistical windows;
  - Set the left boundary using `ISP_AWB_LPOINT`
  - Set the right boundary using `ISP_AWB_RPOINT`
  - Set the top boundary using `ISP_AWB_TPOINT`
  - Set the bottom boundary using `ISP_AWB_BPOINT`
3. Configure white patch constraints;

- Set maximum luminance with [ISP\\_AWB\\_MAX\\_LUM](#)
- Set minimum luminance with [ISP\\_AWB\\_MIN\\_LUM](#)
- Set maximum R/G ratio with [ISP\\_AWB\\_MAX\\_RG](#) (2 integer bits, 8 fractional bits)
- Set minimum R/G ratio with [ISP\\_AWB\\_MIN\\_RG](#) (2 integer bits, 8 fractional bits)
- Set maximum B/G ratio with [ISP\\_AWB\\_MAX\\_BG](#) (2 integer bits, 8 fractional bits)
- Set minimum B/G ratio with [ISP\\_AWB\\_MIN\\_BG](#) (2 integer bits, 8 fractional bits)

#### 4. Obtain statistics;

- Clear the completion status by writing 1 to [ISP\\_AWB\\_FDONE\\_INT\\_CLR](#)
- Trigger statistics by writing 0 and then 1 to [ISP\\_AWB\\_EN](#)
- Wait for the statistics to complete
  - Wait for the ISP interrupt triggered by [AWB\\_FDONE\\_INT](#)
  - Or query the status using [ISP\\_AWB\\_FDONE\\_INT\\_RAW](#)
- Get the number of white patches within the statistical window by reading [ISP\\_AWBO\\_WHITE\\_CNT](#)
- Get the accumulated values of the R, G, B components for the white patches within the statistical window by reading [ISP\\_AWBO\\_ACC\\_R/G/B](#)

## 32.7.12 HIST Configuration

HIST can be configured after the ISP is enabled.

1. Select sampling points via [ISP\\_HIST\\_MODE](#);
  - If sampling points are set to RGB, use [ISP\\_HIST\\_COEFF\\_R/G/B](#) to set RGB weights with 8 fractional bits
2. Set up statistical windows;
  - Set the horizontal start point with [ISP\\_HIST\\_X\\_OFFS](#)
  - Configure the horizontal dimension of each sub-window with [ISP\\_HIST\\_X\\_SIZE](#)
  - Set the vertical start point with [ISP\\_HIST\\_Y\\_OFFS](#)
  - Configure the vertical dimension of each sub-window with [ISP\\_HIST\\_Y\\_SIZE](#)
3. Configure histograms;
  - Set histogram interval divisions using [ISP\\_HIST\\_SEG\\_x\\_x](#)
  - Set window weights using [ISP\\_HIST\\_WEIGHT\\_xx](#) with 8 fractional bits
4. Enable HIST by writing 1 to [ISP\\_HIST\\_EN](#);
5. Obtain statistics.
  - Clear the completion status by writing 1 to [ISP\\_HIST\\_FDONE\\_INT\\_CLR](#)
  - With HIST enabled, statistics are performed at the end of every frame. Wait for the statistics to complete

- Wait for the ISP interrupt triggered by HIST\_FDONE\_INT
- Or query the status using [ISP\\_HIST\\_FDONE\\_INT\\_RAW](#).
- Obtain the statistics for each interval by reading [ISP\\_HIST\\_BIN\\_x](#).

### 32.7.13 ISP\_Pipeline Module Update Configuration

1. Disable the module via [ISP\\_CNTL\\_REG](#);
2. Wait for the interrupt from the corresponding module;
3. Update module configurations;
4. Re-enable the module.



## 32.8 Register Summary

### 32.8.1 ISP Register Summary

The addresses in this section are relative to **ISP** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <b>Configuration Registers</b>               |   |         |        |
| <a href="#">ISP_CLK_EN_REG</a>               | ISP clock control register                            | 0x0004  | R/W    |
| <a href="#">ISP_CNTL_REG</a>                 | ISP enable register                                   | 0x0008  | R/W    |
| <a href="#">ISP_HSYNC_CNT_REG</a>            | Hsync interval control register                       | 0x000C  | R/W    |
| <a href="#">ISP_FRAME_CFG_REG</a>            | Image control register                                | 0x0010  | R/W    |
| <a href="#">ISP_CCM_COEF0_REG</a>            | CCM parameter register 0                              | 0x0014  | R/W    |
| <a href="#">ISP_CCM_COEF1_REG</a>            | CCM parameter register 1                              | 0x0018  | R/W    |
| <a href="#">ISP_CCM_COEF3_REG</a>            | CCM parameter register 3                              | 0x001C  | R/W    |
| <a href="#">ISP_CCM_COEF4_REG</a>            | CCM parameter register 4                              | 0x0020  | R/W    |
| <a href="#">ISP_CCM_COEF5_REG</a>            | CCM parameter register 5                              | 0x0024  | R/W    |
| <a href="#">ISP_BF_MATRIX_CTRL_REG</a>       | BF pixel-to-matrix control register                   | 0x0028  | R/W    |
| <a href="#">ISP_BF_SIGMA_REG</a>             | BF noise reduction strength control register          | 0x002C  | R/W    |
| <a href="#">ISP_BF_GAU0_REG</a>              | BF noise reduction template register 0                | 0x0030  | R/W    |
| <a href="#">ISP_BF_GAU1_REG</a>              | BF noise reduction template register 1                | 0x0034  | R/W    |
| <a href="#">ISP_LUT_CMD_REG</a>              | LUT command register                                  | 0x0048  | WT     |
| <a href="#">ISP_LUT_WDATA_REG</a>            | LUT write register                                    | 0x004C  | R/W    |
| <a href="#">ISP_LSC_TABLESIZE_REG</a>        | LSC parameter control register                        | 0x0054  | R/W    |
| <a href="#">ISP_DEMOSAIC_MATRIX_CTRL_REG</a> | Demosaic pixel-to-matrix control register             | 0x0058  | R/W    |
| <a href="#">ISP_DEMOSAIC_GRAD_RATIO_REG</a>  | Demosaic parameter control register                   | 0x005C  | R/W    |
| <a href="#">ISP_GAMMA_CTRL_REG</a>           | Gamma correction control register                     | 0x0074  | R/W    |
| <a href="#">ISP_GAMMA_RY1_REG</a>            | Gamma curve R channel Y axis configuration register 1 | 0x0078  | R/W    |
| <a href="#">ISP_GAMMA_RY2_REG</a>            | Gamma curve R channel Y axis configuration register 2 | 0x007C  | R/W    |
| <a href="#">ISP_GAMMA_RY3_REG</a>            | Gamma curve R channel Y axis configuration register 3 | 0x0080  | R/W    |
| <a href="#">ISP_GAMMA_RY4_REG</a>            | Gamma curve R channel Y axis configuration register 4 | 0x0084  | R/W    |
| <a href="#">ISP_GAMMA_GY1_REG</a>            | Gamma curve G channel Y axis configuration register 1 | 0x0088  | R/W    |
| <a href="#">ISP_GAMMA_GY2_REG</a>            | Gamma curve G channel Y axis configuration register 2 | 0x008C  | R/W    |
| <a href="#">ISP_GAMMA_GY3_REG</a>            | Gamma curve G channel Y axis configuration register 3 | 0x0090  | R/W    |

| Name                                      | Description  | Address | Access |
|---|--|---------|--------|
| <a href="#">ISP_GAMMA_GY4_REG</a>         | Gamma curve G channel Y axis configuration register 4        | 0x0094  | R/W    |
| <a href="#">ISP_GAMMA_BY1_REG</a>         | Gamma curve B channel Y axis configuration register 1        | 0x0098  | R/W    |
| <a href="#">ISP_GAMMA_BY2_REG</a>         | Gamma curve B channel Y axis configuration register 2        | 0x009C  | R/W    |
| <a href="#">ISP_GAMMA_BY3_REG</a>         | Gamma curve B channel Y axis configuration register 3        | 0x00A0  | R/W    |
| <a href="#">ISP_GAMMA_BY4_REG</a>         | Gamma curve B channel Y axis configuration register 4        | 0x00A4  | R/W    |
| <a href="#">ISP_GAMMA_RX1_REG</a>         | Gamma curve R channel X axis configuration register 1        | 0x00A8  | R/W    |
| <a href="#">ISP_GAMMA_RX2_REG</a>         | Gamma curve R channel X axis configuration register 2        | 0x00AC  | R/W    |
| <a href="#">ISP_GAMMA_GX1_REG</a>         | Gamma curve G channel X axis configuration register 1        | 0x00B0  | R/W    |
| <a href="#">ISP_GAMMA_GX2_REG</a>         | Gamma curve G channel X axis configuration register 2        | 0x00B4  | R/W    |
| <a href="#">ISP_GAMMA_BX1_REG</a>         | Gamma curve B channel X axis configuration register 1        | 0x00B8  | R/W    |
| <a href="#">ISP_GAMMA_BX2_REG</a>         | Gamma curve B channel X axis configuration register 2        | 0x00BC  | R/W    |
| <a href="#">ISP_AE_CTRL_REG</a>           | AE control register  | 0x00C0  | varies |
| <a href="#">ISP_AE_MONITOR_REG</a>        | AE monitoring control register                               | 0x00C4  | R/W    |
| <a href="#">ISP_AE_BX_REG</a>             | AE statistical window X direction configuration register     | 0x00C8  | R/W    |
| <a href="#">ISP_AE_BY_REG</a>             | AE statistical window Y direction configuration register     | 0x00CC  | R/W    |
| <a href="#">ISP_AE_WINPIXNUM_REG</a>      | AE sub-window pixel number configuration register            | 0x00D0  | R/W    |
| <a href="#">ISP_AE_WIN_RECIPROCAL_REG</a> | AE sub-window pixel number reciprocal configuration register | 0x00D4  | R/W    |
| <a href="#">ISP_SHARP_CTRL0_REG</a>       | Sharpen control register 0                                   | 0x00F4  | R/W    |
| <a href="#">ISP_SHARP_FILTER0_REG</a>     | Sharpen low-frequency template configuration register 0      | 0x00F8  | R/W    |
| <a href="#">ISP_SHARP_FILTER1_REG</a>     | Sharpen low-frequency template configuration register 1      | 0x00FC  | R/W    |
| <a href="#">ISP_SHARP_FILTER2_REG</a>     | Sharpen low-frequency template configuration register 2      | 0x0100  | R/W    |
| <a href="#">ISP_SHARP_MATRIX_CTRL_REG</a> | Sharpen pixel-to-matrix control register                     | 0x0104  | R/W    |
| <a href="#">ISP_SHARP_CTRL1_REG</a>       | Sharpen control register 1                                   | 0x0108  | RO     |
| <a href="#">ISP_DMA_CNTL_REG</a>          | ISP VDMA input control register                              | 0x010C  | varies |
| <a href="#">ISP_DMA_RAW_DATA_REG</a>      | ISP VDMA input data amount configuration register            | 0x0110  | varies |

| Name                                       | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">ISP_CAM_CNTL_REG</a>           | ISP DVP input control register                                      | 0x0114  | R/W    |
| <a href="#">ISP_CAM_CONF_REG</a>           | ISP DVP input configuration register                                | 0x0118  | R/W    |
| <a href="#">ISP_AF_CTRL0_REG</a>           | AF control register 0   | 0x011C  | varies |
| <a href="#">ISP_AF_ENV_USER_TH_SUM_REG</a> | AF scene monitoring sharpness threshold configuration register      | 0x0128  | R/W    |
| <a href="#">ISP_AF_ENV_USER_TH_LUM_REG</a> | AF scene monitoring luminance threshold configuration register      | 0x012C  | R/W    |
| <a href="#">ISP_AF_THRESHOLD_REG</a>       | AF statistics threshold configuration register                      | 0x0130  | varies |
| <a href="#">ISP_AF_HSCALE_A_REG</a>        | AF statistical window A horizontal direction configuration register | 0x0134  | R/W    |
| <a href="#">ISP_AF_VSCALE_A_REG</a>        | AF statistical window A vertical direction configuration register   | 0x0138  | R/W    |
| <a href="#">ISP_AF_HSCALE_B_REG</a>        | AF statistical window B horizontal direction configuration register | 0x013C  | R/W    |
| <a href="#">ISP_AF_VSCALE_B_REG</a>        | AF statistical window B vertical direction configuration register   | 0x0140  | R/W    |
| <a href="#">ISP_AF_HSCALE_C_REG</a>        | AF statistical window C horizontal direction configuration register | 0x0144  | R/W    |
| <a href="#">ISP_AF_VSCALE_C_REG</a>        | AF statistical window C vertical direction configuration register   | 0x0148  | R/W    |
| <a href="#">ISP_AWB_MODE_REG</a>           | AWB control register  | 0x0164  | R/W    |
| <a href="#">ISP_AWB_HSCALE_REG</a>         | AWB statistical window horizontal direction configuration register  | 0x0168  | R/W    |
| <a href="#">ISP_AWB_VSCALE_REG</a>         | AWB statistical window vertical direction configuration register    | 0x016C  | R/W    |
| <a href="#">ISP_AWB_TH_LUM_REG</a>         | AWB white patch luminance threshold configuration register          | 0x0170  | R/W    |
| <a href="#">ISP_AWB_TH_RG_REG</a>          | AWB white patch R/G threshold configuration register                | 0x0174  | R/W    |
| <a href="#">ISP_AWB_TH_BG_REG</a>          | AWB white patch B/G threshold configuration register                | 0x0178  | R/W    |
| <a href="#">ISP_COLOR_CTRL_REG</a>         | Contrast/hue/saturation/luminance control register                  | 0x018C  | R/W    |
| <a href="#">ISP_HIST_MODE_REG</a>          | HIST control register   | 0x01A4  | R/W    |
| <a href="#">ISP_HIST_COEFF_REG</a>         | HIST RGB parameter configuration register                           | 0x01A8  | R/W    |
| <a href="#">ISP_HIST_OFFS_REG</a>          | HIST statistical window starting point configuration register       | 0x01AC  | R/W    |
| <a href="#">ISP_HIST_SIZE_REG</a>          | HIST statistical sub-window size configuration register             | 0x01B0  | R/W    |
| <a href="#">ISP_HIST_SEGO_REG</a>          | HIST X coordinate interval configuration register 0                 | 0x01B4  | R/W    |
| <a href="#">ISP_HIST_SEG1_REG</a>          | HIST X coordinate interval configuration register 1                 | 0x01B8  | R/W    |

| Name                                    | Description   | Address | Access |
|---|---|---------|--------|
| <a href="#">ISP_HIST_SEG2_REG</a>       | HIST X coordinate interval configuration register 2 | 0x01BC  | R/W    |
| <a href="#">ISP_HIST_SEG3_REG</a>       | HIST X coordinate interval configuration register 3 | 0x01C0  | R/W    |
| <a href="#">ISP_HIST_WEIGHT0_REG</a>    | HIST sub-window weight configuration register 0     | 0x01C4  | R/W    |
| <a href="#">ISP_HIST_WEIGHT1_REG</a>    | HIST sub-window weight configuration register 1     | 0x01C8  | R/W    |
| <a href="#">ISP_HIST_WEIGHT2_REG</a>    | HIST sub-window weight configuration register 2     | 0x01CC  | R/W    |
| <a href="#">ISP_HIST_WEIGHT3_REG</a>    | HIST sub-window weight configuration register 3     | 0x01D0  | R/W    |
| <a href="#">ISP_HIST_WEIGHT4_REG</a>    | HIST sub-window weight configuration register 4     | 0x01D4  | R/W    |
| <a href="#">ISP_HIST_WEIGHT5_REG</a>    | HIST sub-window weight configuration register 5     | 0x01D8  | R/W    |
| <a href="#">ISP_HIST_WEIGHT6_REG</a>    | HIST sub-window weight configuration register 6     | 0x01DC  | R/W    |
| <a href="#">ISP_YUV_FORMAT_REG</a>      | YUV format control register                         | 0x0234  | R/W    |
| <b>Status Registers</b>                 |   |         |        |
| <a href="#">ISP_LUT_RDATA_REG</a>       | LUT read register                                   | 0x0050  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_0_REG</a> | AE statistics register 0                            | 0x00D8  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_1_REG</a> | AE statistics register 1                            | 0x00DC  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_2_REG</a> | AE statistics register 2                            | 0x00E0  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_3_REG</a> | AE statistics register 3                            | 0x00E4  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_4_REG</a> | AE statistics register 4                            | 0x00E8  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_5_REG</a> | AE statistics register 5                            | 0x00EC  | RO     |
| <a href="#">ISP_AE_BLOCK_MEAN_6_REG</a> | AE statistics register 6                            | 0x00F0  | RO     |
| <a href="#">ISP_AF_SUM_A_REG</a>        | AF window A sharpness statistics register           | 0x014C  | RO     |
| <a href="#">ISP_AF_SUM_B_REG</a>        | AF window B sharpness statistics register           | 0x0150  | RO     |
| <a href="#">ISP_AF_SUM_C_REG</a>        | AF window C sharpness statistics register           | 0x0154  | RO     |
| <a href="#">ISP_AF_LUM_A_REG</a>        | AF window A luminance statistics register           | 0x0158  | RO     |
| <a href="#">ISP_AF_LUM_B_REG</a>        | AF window B luminance statistics register           | 0x015C  | RO     |
| <a href="#">ISP_AF_LUM_C_REG</a>        | AF window C luminance statistics register           | 0x0160  | RO     |
| <a href="#">ISP_AWBO_WHITE_CNT_REG</a>  | AWB white patch count statistics register           | 0x017C  | RO     |
| <a href="#">ISP_AWBO_ACC_R_REG</a>      | AWB R channel statistics register                   | 0x0180  | RO     |
| <a href="#">ISP_AWBO_ACC_G_REG</a>      | AWB G channel statistics register                   | 0x0184  | RO     |
| <a href="#">ISP_AWBO_ACC_B_REG</a>      | AWB B channel statistics register                   | 0x0188  | RO     |
| <a href="#">ISP_HIST_BINO_REG</a>       | HIST interval 0 statistics register                 | 0x01E0  | RO     |
| <a href="#">ISP_HIST_BIN1_REG</a>       | HIST interval 1 statistics register                 | 0x01E4  | RO     |
| <a href="#">ISP_HIST_BIN2_REG</a>       | HIST interval 2 statistics register                 | 0x01E8  | RO     |
| <a href="#">ISP_HIST_BIN3_REG</a>       | HIST interval 3 statistics register                 | 0x01EC  | RO     |
| <a href="#">ISP_HIST_BIN4_REG</a>       | HIST interval 4 statistics register                 | 0x01F0  | RO     |
| <a href="#">ISP_HIST_BIN5_REG</a>       | HIST interval 5 statistics register                 | 0x01F4  | RO     |

| Name                               | Description                          | Address | Access   |
|------------------------------------|--------------------------------------|---------|----------|
| <a href="#">ISP_HIST_BIN6_REG</a>  | HIST interval 6 statistics register  | 0x01F8  | RO       |
| <a href="#">ISP_HIST_BIN7_REG</a>  | HIST interval 7 statistics register  | 0x01FC  | RO       |
| <a href="#">ISP_HIST_BIN8_REG</a>  | HIST interval 8 statistics register  | 0x0200  | RO       |
| <a href="#">ISP_HIST_BIN9_REG</a>  | HIST interval 9 statistics register  | 0x0204  | RO       |
| <a href="#">ISP_HIST_BIN10_REG</a> | HIST interval 10 statistics register | 0x0208  | RO       |
| <a href="#">ISP_HIST_BIN11_REG</a> | HIST interval 11 statistics register | 0x020C  | RO       |
| <a href="#">ISP_HIST_BIN12_REG</a> | HIST interval 12 statistics register | 0x0210  | RO       |
| <a href="#">ISP_HIST_BIN13_REG</a> | HIST interval 13 statistics register | 0x0214  | RO       |
| <a href="#">ISP_HIST_BIN14_REG</a> | HIST interval 14 statistics register | 0x0218  | RO       |
| <a href="#">ISP_HIST_BIN15_REG</a> | HIST interval 15 statistics register | 0x021C  | RO       |
| <b>Interrupt Registers</b>         |                                      |         |          |
| <a href="#">ISP_INT_RAW_REG</a>    | Raw interrupt status register        | 0x0064  | R/SS/WTC |
| <a href="#">ISP_INT_ST_REG</a>     | Masked interrupt status register     | 0x0068  | RO       |
| <a href="#">ISP_INT_ENA_REG</a>    | Interrupt enable register            | 0x006C  | R/W      |
| <a href="#">ISP_INT_CLR_REG</a>    | Interrupt clear register             | 0x0070  | WT       |
| <b>Version Register</b>            |                                      |         |          |
| <a href="#">ISP_VER_DATE_REG</a>   | Version control register             | 0x0000  | R/W      |

### 32.8.2 MIPI CSI\_Bridge Register Summary

The addresses in this section are relative to **MIPI CSI\_Bridge** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description                              | Address | Access           |
|---|--|---------|------------------|
| <b>Clock Gating Control Register</b>          |  |         |                  |
| <a href="#">CSI_BRIG_CLK_EN_REG</a>           | CSI_Bridge clock gate register           | 0x0000  | R/W              |
| <b>CSI_Bridge Control Registers</b>           |  |         |                  |
| <a href="#">CSI_BRIG_CSI_EN_REG</a>           | CSI_Bridge enable register               | 0x0004  | R/W              |
| <a href="#">CSI_BRIG_BUF_FLOW_CTL_REG</a>     | CSI_Bridge buffer control register       | 0x000C  | varies           |
| <b>DMA Control Registers</b>                  |  |         |                  |
| <a href="#">CSI_BRIG_DMA_REQ_CFG_REG</a>      | DMA request control register             | 0x0008  | R/W              |
| <a href="#">CSI_BRIG_DMA_REQ_INTERVAL_REG</a> | DMA request interval register            | 0x002C  | R/W              |
| <a href="#">CSI_BRIG_DMABLK_SIZE_REG</a>      | DMA data block size control register     | 0x0030  | R/W              |
| <b>Frame Format Configuration Registers</b>   |  |         |                  |
| <a href="#">CSI_BRIG_DATA_TYPE_CFG_REG</a>    | DATA_TYPE control register               | 0x0010  | R/W              |
| <a href="#">CSI_BRIG_FRAME_CFG_REG</a>        | Image control register                   | 0x0014  | R/W              |
| <a href="#">CSI_BRIG_ENDIAN_MODE_REG</a>      | Byte order control register              | 0x0018  | R/W              |
| <b>Interrupt Registers</b>                    |  |         |                  |
| <a href="#">CSI_BRIG_INT_RAW_REG</a>          | CSI_Bridge raw interrupt status register | 0x001C  | R/<br>WTC/<br>SS |
| <a href="#">CSI_BRIG_INT_CLR_REG</a>          | CSI_Bridge interrupt clear register      | 0x0020  | WT               |

| Name                                   | Description                                 | Address | Access |
|--|---|---------|--------|
| <a href="#">CSI_BRIG_INT_ST_REG</a>    | CSI_Bridge masked interrupt status register | 0x0024  | RO     |
| <a href="#">CSI_BRIG_INT_ENA_REG</a>   | CSI_Bridge interrupt enable register        | 0x0028  | R/W    |
| <b>CSI HOST Control Register</b>       |   |         |        |
| <a href="#">CSI_BRIG_HOST_CTRL_REG</a> | CSI HOST control register                   | 0x0040  | R/W    |

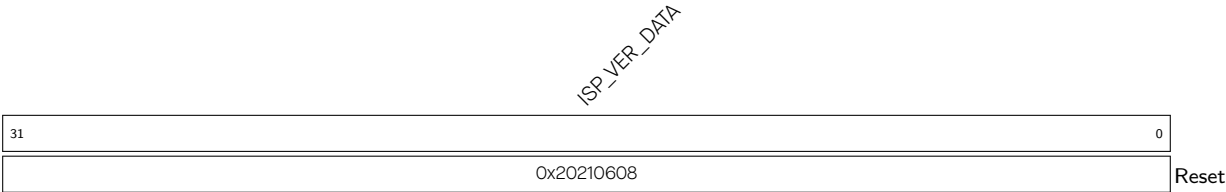
## 32.9 Registers

### 32.9.1 ISP Registers

The addresses in this section are relative to **ISP** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 32.1. ISP\_VER\_DATE\_REG (0x0000)



**ISP\_VER\_DATA** ISP version control register. (R/W)

Register 32.2. ISP\_CLK\_EN\_REG (0x0004)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|---|-------|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_MEM_CLK_FORCE_ON<br>ISP_CLK_MIP1_ID1_FORCE_ON<br>ISP_CLK_HIST_FORCE_ON<br>ISP_CLK_AWB_FORCE_ON<br>ISP_CLK_AF_FORCE_ON<br>ISP_CLK_AE_FORCE_ON<br>ISP_CLK_YUV2RGB_FORCE_ON<br>ISP_CLK_COLOR_FORCE_ON<br>ISP_CLK_SHARP_FORCE_ON<br>ISP_CLK_RGB2YUV_FORCE_ON<br>(reserved)<br>ISP_CLK_GAMMA_FORCE_ON<br>ISP_CLK_OCM_FORCE_ON<br>(reserved)<br>ISP_CLK_DEMOSAIC_FORCE_ON<br>ISP_CLK_LSC_FORCE_ON<br>(reserved)<br>ISP_CLK_EN |    |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | Reset |   |   |   |   |   |   |   |   |

**ISP\_CLK\_EN** Configures whether the ISP clock is always on.

0: The clock is enabled only during register access

1: The clock is always on

(R/W)

**ISP\_CLK\_BF\_FORCE\_ON** Configures whether to force enable the BF clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_LSC\_FORCE\_ON** Configures whether to force enable the LSC clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_DEMOSAIC\_FORCE\_ON** Configures whether to force enable the demosaic clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_CCM\_FORCE\_ON** Configures whether to force enable the CCM clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_GAMMA\_FORCE\_ON** Configures whether to force enable the gamma correction clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_RGB2YUV\_FORCE\_ON** Configures whether to force enable the RGB2YUV clock.

0: Not force enable

1: Force enable

(R/W)

Continued on the next page...



**Register 32.2. ISP\_CLK\_EN\_REG (0x0004)**

Continued from the previous page...

**ISP\_CLK\_SHARP\_FORCE\_ON** Configures whether to force enable the sharpen clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_COLOR\_FORCE\_ON** Configures whether to force enable the contrast/hue/saturation/luminance clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_YUV2RGB\_FORCE\_ON** Configures whether to force enable the YUV2RGB clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_AE\_FORCE\_ON** Configures whether to force enable the AE clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_AF\_FORCE\_ON** Configures whether to force enable the AF clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_AWB\_FORCE\_ON** Configures whether to force enable the AWB clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_HIST\_FORCE\_ON** Configures whether to force enable the HIST clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_CLK\_MIPI\_IDI\_FORCE\_ON** Configures whether to force enable the MIPI Image Interface 32 input clock.

0: Not force enable

1: Force enable

(R/W)

**ISP\_MEM\_CLK\_FORCE\_ON** Configures whether to force enable all the ISP memory clocks.

0: Not force enable

1: Force enable

(R/W)

**Register 32.3. ISP\_CNTL\_REG (0x0008)**

| ISP_OUT_TYPE |    | ISP_IN_SRC |    | ISP_DATA_TYPE |    | ISP_BYTE_ENDIAN_ORDER |    | (reserved) |   |   |   |   |   |   |   |   |   | ISP_HIST_EN |    | ISP_AWB_EN |    | ISP_AF_EN |    | ISP_AE_EN |    | ISP_YUV2RGB_EN |   | ISP_COLOR_EN |   | ISP_SHARP_EN |   | ISP_RGB2YUV_EN |   | ISP_GAMMA_EN |   | (reserved) |   | ISP_DEMOSAIC_EN |   | ISP_LSC_EN |   | ISP_BF_EN |   | (reserved) |   |   |   |   |   |   |   |   |   | ISP_EN |   | ISP_MIPI_DATA_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|
|--------------|----|------------|----|---------------|----|-----------------------|----|------------|---|---|---|---|---|---|---|---|---|-------------|----|------------|----|-----------|----|-----------|----|----------------|---|--------------|---|--------------|---|----------------|---|--------------|---|------------|---|-----------------|---|------------|---|-----------|---|------------|---|---|---|---|---|---|---|---|---|--------|---|------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 31           | 29 | 28         | 27 | 26            | 25 | 24                    | 23 |            |   |   |   |   |   |   |   |   |   | 18          | 17 | 16         | 15 | 14        | 13 | 12        | 11 | 10             | 9 | 8            | 7 | 6            | 5 | 4              | 3 | 2            | 1 | 0          |   |                 |   |            |   |           |   |            |   |   |   |   |   |   |   |   |   |        |   |                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|
| 0            | 1  | 0          | 0  | 0             | 0  | 0                     | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1           | 0  | 0          | 0  | 1         | 0  | 0         | 0  | 1              | 0 | 0            | 0 | 1            | 0 | 0              | 0 | 0            | 0 | 0          | 0 | 0               | 0 | 0          | 0 | 0         | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0      | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ISP\_MIPI\_DATA\_EN** Configures whether to enable the MIPI Image Interface 32 input.

0: Disable

1: Enable

(R/W)

**ISP\_EN** Configures whether to enable the ISP.

0: Disable

1: Enable

(R/W)

**ISP\_BF\_EN** Configures whether to enable the BF module.

0: Disable

1: Enable

(R/W)

**ISP\_LSC\_EN** Configures whether to enable the LSC module.

0: Disable

1: Enable

(R/W)

**ISP\_DEMOSAIC\_EN** Configures whether to enable the demosaic module.

0: Disable

1: Enable

(R/W)

**ISP\_CCM\_EN** Configures whether to enable the CCM module.

0: Disable

1: Enable

(R/W)

**ISP\_GAMMA\_EN** Configures whether to enable the gamma correction module.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 32.3. ISP\_CNTL\_REG (0x0008)**

Continued from the previous page...

**ISP\_RGB2YUV\_EN** Configures whether to enable the RGB2YUV module.

0: Disable

1: Enable

(R/W)

**ISP\_SHARP\_EN** Configures whether to enable the sharpen module.

0: Disable

1: Enable

(R/W)

**ISP\_COLOR\_EN** Configures whether to enable the contrast/hue/saturation/luminance module.

0: Disable

1: Enable

(R/W)

**ISP\_YUV2RGB\_EN** Configures whether to enable the YUV2RGB module.

0: Disable

1: Enable

(R/W)

**ISP\_AE\_EN** Configures whether to enable the AE module.

0: Disable

1: Enable

(R/W)

**ISP\_AF\_EN** Configures whether to enable the AF module.

0: Disable

1: Enable

(R/W)

**ISP\_AWB\_EN** Configures whether to enable the AWB module.

0: Disable

1: Enable

(R/W)

**ISP\_HIST\_EN** Configures whether to enable the HIST module.

0: Disable

1: Enable

(R/W)

**ISP\_BYTE\_ENDIAN\_ORDER** Configures the byte order for MIPI Image Interface 32 input when ISP is disabled.

0: csi\_data[31:0]

1: [7:0], [15:8], [23:16], [31:24]

(R/W)

Continued on the next page...

Register 32.3. ISP\_CNTL\_REG (0x0008)

Continued from the previous page...

**ISP\_DATA\_TYPE** Configures the input data type.

- 0: RAW8
- 1: RAW10
- 2: RAW12
- 3: invalid

(R/W)

**ISP\_IN\_SRC** Configures the input data source.

- 0: MIPI Image Interface 32 data from CSI HOST
- 1: Data from DVP
- 2: Data from VDMA
- 3: invalid

(R/W)

**ISP\_OUT\_TYPE** Configures the output data type.

- 0: RAW8
- 1: YUV422
- 2: RGB888
- 3: YUV420
- 4: RGB565
- Others: Invalid

(R/W)

Register 32.4. ISP\_HSYNC\_CNT\_REG (0x000C)



**ISP\_HSYNC\_CNT** Configures the interval between hsync and the previous vsync or line\_end when converting Image Interface 32 data to ISP data. Generally, the default value is used. Measurement unit: Number of ISP\_CLK clock cycles. (R/W)

### Register 32.5. ISP\_FRAME\_CFG\_REG (0x0010)

|   |    |    |    |    |    |    |     |    |    |       |
|---|----|----|----|----|----|----|-----|----|----|-------|
| <div>(reserved)</div> <div>ISP_HSYNC_END_EXIST</div> <div>ISP_HSYNC_START_EXIST</div> <div>ISP_BAYER_MODE</div> <div>(reserved)</div> <div>ISP_HADR_NUM</div> <div>ISP_VADR_NUM</div> |    |    |    |    |    |    |     |    |    |       |
| 31  | 30 | 29 | 28 | 27 | 26 | 24 | 23  | 12 | 11 | 0     |
| 0   | 1  | 1  | 0  | 0  | 0  | 0  | 480 |    |    | 480   |
|   |    |    |    |    |    |    |     |    |    | Reset |

**ISP\_VADR\_NUM** Configures the height of the input image, which should be set as the actual number of lines - 1. (R/W)

**ISP\_HADR\_NUM** Configures the width of the input image, which should be set as the actual width of lines - 1. (R/W)

**ISP\_BAYER\_MODE** Configures the Bayer mode of the input image.

O: BG/GR

1: GB/RG

2: GR/BG

3: RG/GB

(R/W)

**ISP\_HSYNC\_START\_EXIST** Configures whether the hsync\_start packet exists.

0: Not exist

1: Exist

(R/W)

**ISP\_HSYNC\_END\_EXIST** Configures whether the hsync\_end packet exists. This must have the same value as the [ISP\\_HSYNC\\_START\\_EXIST](#) field.

0: Not exist

1: Exist

(R/W)

### Register 32.6. ISP\_CCM\_COEFO\_REG (0x0014)

|            |  |  |  |  |  |    |  |  |  |  |  |    |  |            |  |  |  |    |  |  |  |  |  |    |  |  |  |            |  |   |  |  |  |  |  |      |  |  |  |  |  |      |  |  |  |  |  |       |
|------------|--|--|--|--|--|----|--|--|--|--|--|----|--|------------|--|--|--|----|--|--|--|--|--|----|--|--|--|------------|--|---|--|--|--|--|--|------|--|--|--|--|--|------|--|--|--|--|--|-------|
| (reserved) |  |  |  |  |  |    |  |  |  |  |  |    |  | ISP_CCM_RG |  |  |  |    |  |  |  |  |  |    |  |  |  | ISP_CCM_RR |  |   |  |  |  |  |  |      |  |  |  |  |  |      |  |  |  |  |  |       |
| 31         |  |  |  |  |  | 26 |  |  |  |  |  | 25 |  |            |  |  |  | 13 |  |  |  |  |  | 12 |  |  |  |            |  | 0 |  |  |  |  |  |      |  |  |  |  |  |      |  |  |  |  |  |       |
| 0          |  |  |  |  |  | 0  |  |  |  |  |  | 0  |  |            |  |  |  | 0  |  |  |  |  |  | 0  |  |  |  |            |  | 0 |  |  |  |  |  | 4736 |  |  |  |  |  | 1856 |  |  |  |  |  | Reset |

**ISP\_CCM\_RR** Configures the CCM RR parameter. The 12th bit is the sign bit, and bits [11:0] represent the absolute value. Bits [11:10] are the integer part, and bits [9:0] are the fractional part. (R/W)

**ISP\_CCM\_RG** Configures the CCM RG parameter, following the same bit structure and interpretation as **ISP\_CCM\_RR**. (R/W)

**Register 32.7. ISP\_CCM\_COEF1\_REG (0x0018)**

|            |   |    |   |    |   |            |  |  |  |    |  |    |            |  |  |  |  |  |       |
|------------|---|----|---|----|---|------------|--|--|--|----|--|----|------------|--|--|--|--|--|-------|
| (reserved) |   |    |   |    |   | ISP_CCM_GR |  |  |  |    |  |    | ISP_CCM_RB |  |  |  |  |  |       |
| 31         |   | 26 |   | 25 |   |            |  |  |  | 13 |  | 12 |            |  |  |  |  |  | 0     |
| 0          | 0 | 0  | 0 | 0  | 0 |            |  |  |  |    |  |    |            |  |  |  |  |  | Reset |
|            |   |    |   |    |   | 4416       |  |  |  |    |  |    | 4288       |  |  |  |  |  |       |

**ISP\_CCM\_RB** Configures the CCM RB parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**ISP\_CCM\_GR** Configures the CCM GR parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**Register 32.8. ISP\_CCM\_COEF3\_REG (0x001C)**

|            |   |    |   |    |   |            |  |  |  |    |  |    |            |  |  |  |  |  |       |
|------------|---|----|---|----|---|------------|--|--|--|----|--|----|------------|--|--|--|--|--|-------|
| (reserved) |   |    |   |    |   | ISP_CCM_GB |  |  |  |    |  |    | ISP_CCM_GG |  |  |  |  |  |       |
| 31         |   | 26 |   | 25 |   |            |  |  |  | 13 |  | 12 |            |  |  |  |  |  | 0     |
| 0          | 0 | 0  | 0 | 0  | 0 |            |  |  |  |    |  |    |            |  |  |  |  |  | Reset |
|            |   |    |   |    |   | 4352       |  |  |  |    |  |    | 1664       |  |  |  |  |  |       |

**ISP\_CCM\_GG** Configures the CCM GG parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**ISP\_CCM\_GB** Configures the CCM GB parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**Register 32.9. ISP\_CCM\_COEF4\_REG (0x0020)**

|            |   |    |   |    |   |            |  |  |  |    |  |    |            |  |  |  |  |  |       |
|------------|---|----|---|----|---|------------|--|--|--|----|--|----|------------|--|--|--|--|--|-------|
| (reserved) |   |    |   |    |   | ISP_CCM_BG |  |  |  |    |  |    | ISP_CCM_BR |  |  |  |  |  |       |
| 31         |   | 26 |   | 25 |   |            |  |  |  | 13 |  | 12 |            |  |  |  |  |  | 0     |
| 0          | 0 | 0  | 0 | 0  | 0 |            |  |  |  |    |  |    |            |  |  |  |  |  | Reset |
|            |   |    |   |    |   | 4800       |  |  |  |    |  |    | 4160       |  |  |  |  |  |       |

**ISP\_CCM\_BR** Configures the CCM BR parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**ISP\_CCM\_BG** Configures the CCM BG parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**Register 32.10. ISP\_CCM\_COEF5\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |      |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   | ISP_CCM_BB |   |   |   |   |   |   |   |   |   |   |   |   |   |      |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 13 | 12 |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |      | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1856 | Reset |

**ISP\_CCM\_BB** Configures the CCM BB parameter, following the same bit structure and interpretation as [ISP\\_CCM\\_RR](#). (R/W)

**Register 32.11. ISP\_BF\_MATRIX\_CTRL\_REG (0x0028)**

|            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                     |    |  |  |  |  |  |  |                            |    |  |  |  |  |  |  |                            |    |   |  |  |  |  |  |       |  |   |   |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|---------------------|----|--|--|--|--|--|--|----------------------------|----|--|--|--|--|--|--|----------------------------|----|---|--|--|--|--|--|-------|--|---|---|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  | ISP_BF_PADDING_MODE |  |  |  |  |  |  |  | ISP_BF_PADDING_DATA |    |  |  |  |  |  |  | ISP_BF_TAIL_PIXEN_PULSE_TH |    |  |  |  |  |  |  | ISP_BF_TAIL_PIXEN_PULSE_TL |    |   |  |  |  |  |  |       |  |   |   |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  | 25                  |  |  |  |  |  |  |  | 24                  | 23 |  |  |  |  |  |  |                            | 16 |  |  |  |  |  |  |                            | 15 | 8 |  |  |  |  |  |       |  | 7 | 0 |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0x0                 |    |  |  |  |  |  |  | 0x0                        |    |  |  |  |  |  |  | 0x0                        |    |   |  |  |  |  |  | Reset |  |   |   |  |  |  |  |  |  |  |

**ISP\_BF\_TAIL\_PIXEN\_PULSE\_TL** Configures the data control cycle for the tail-row data rate during pixel-to-matrix conversion in the BF module.

Within [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) clock cycles, only the first [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) cycles are valid. Be cautious to configure this field, to prevent data processing from being deferred to the next frame.

This feature is enabled only when both [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) and [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) are non-zero, and [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) < [ISP\\_BF\\_TAIL\\_PIXEN\\_PULSE\\_TL](#). (R/W)

**ISP\_BF\_TAIL\_PIXEN\_PULSE\_TH** Configures the valid data period of the tail-row data rate during pixel-to-matrix conversion in the BF module, which must be less than [ISP\\_HADR\\_NUM](#) - 1. (R/W)

**ISP\_BF\_PADDING\_DATA** Configures the padding data used during image edge expansion in pixel-to-matrix conversion of the BF module. (R/W)

**ISP\_BF\_PADDING\_MODE** Configures the method of image edge expansion during pixel-to-matrix conversion in the BF module.

0: Automatically padded with pixel values from the image edge

1: Padded with the data in [ISP\\_BF\\_PADDING\\_DATA](#)

(R/W)

**Register 32.12. ISP\_BF\_SIGMA\_REG (0x002C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |           |   |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------|---|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_SIGMA |   |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5         |   |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 2 |  |  | Reset |

**ISP\_SIGMA** Configures the strength of noise reduction in the BF module. Values from 2 to 20 represent increasing strength, while other values indicate maximum strength. (R/W)

**Register 32.13. ISP\_BF\_GAUO\_REG (0x0030)**

|                    |    |  |  |                    |    |  |  |                    |    |  |  |                    |    |  |  |                    |    |  |  |                    |   |  |  |                    |   |  |  |                    |   |  |  |       |  |  |  |
|--------------------|----|--|--|--------------------|----|--|--|--------------------|----|--|--|--------------------|----|--|--|--------------------|----|--|--|--------------------|---|--|--|--------------------|---|--|--|--------------------|---|--|--|-------|--|--|--|
| ISP_GAU_TEMPLATE00 |    |  |  | ISP_GAU_TEMPLATE01 |    |  |  | ISP_GAU_TEMPLATE02 |    |  |  | ISP_GAU_TEMPLATE10 |    |  |  | ISP_GAU_TEMPLATE11 |    |  |  | ISP_GAU_TEMPLATE12 |   |  |  | ISP_GAU_TEMPLATE20 |   |  |  | ISP_GAU_TEMPLATE21 |   |  |  |       |  |  |  |
| 31                 | 28 |  |  | 27                 | 24 |  |  | 23                 | 20 |  |  | 19                 | 16 |  |  | 15                 | 12 |  |  | 11                 | 8 |  |  | 7                  | 4 |  |  | 3                  | 0 |  |  |       |  |  |  |
| Oxf                |    |  |  | Oxf                |    |  |  | Oxf                |    |  |  | Oxf                |    |  |  | Oxf                |    |  |  | Oxf                |   |  |  | Oxf                |   |  |  | Oxf                |   |  |  | Reset |  |  |  |

**ISP\_GAU\_TEMPLATE21** Configures the value of coordinate 21 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE20** Configures the value of coordinate 20 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE12** Configures the value of coordinate 12 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE11** Configures the value of coordinate 11 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE10** Configures the value of coordinate 10 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE02** Configures the value of coordinate 02 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE01** Configures the value of coordinate 01 in the noise reduction template of the BF module. (R/W)

**ISP\_GAU\_TEMPLATE00** Configures the value of coordinate 00 in the noise reduction template of the BF module. (R/W)



### Register 32.14. ISP\_BF\_GAU1\_REG (0x0034)

Diagram of the ISP\_GAU\_TEMPLATE22 register structure:

- Bit 31: (reserved)
- Bits 31 down to 4: (reserved)
- Bits 3 down to 0: ISP\_GAU\_TEMPLATE22
- Value: 0xf
- Reset

**ISP\_GAU\_TEMPLATE22** Configures the value of coordinate 22 in the noise reduction template of the BF module. (R/W)

### Register 32.15. ISP\_LUT\_CMD\_REG (0x0048)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |             |  |              |  |     |  |    |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |   |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|-------------|--|--------------|--|-----|--|----|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|---|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_LUT_CMD |  | ISP_LUT_NUM |  | ISP_LUT_ADDR |  |     |  |    |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |   |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17          |  | 16          |  | 15           |  | 12  |  | 11 |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  | 0 |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0           |  | 0x0         |  |              |  | 0x0 |  |    |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |   |  |

**ISP\_LUT\_ADDR** Configures the LUT address. When **ISP\_LUT\_NUM** selects LSC LUT, [11:10] being 0 indicates selecting Gb\_B LUT, and being 1 indicates selecting R\_Gr LUT. Bits [9:0] represent the actual LUT address.

(WT)

**ISP\_LUT\_NUM** Configures the LUT selection.

0: Select LSC LUT

Others: Invalid

(WT)

**ISP\_LUT\_CMD** Configures whether to read from or write to the LUT.

0: Read from the LUT

### 1: Write to the LUT

(WT)

### Register 32.16. ISP\_LUT\_WDATA\_REG (0x004C)

Diagram of the ISP\_LUT\_WDATA register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value 0x000000 is shown inside the register box. A label 'ISP\_LUT\_WDATA' is placed above the register box. A 'Reset' label is at the bottom right.

**ISP\_LUT\_WDATA** Data to be written to the LUT, which must be configured before writing to [ISP\\_LUT\\_CMD\\_REG](#). (R/W)

Register 32.17. ISP\_LSC\_TABLESIZE\_REG (0x0054)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |       |  |  |  |   |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|-------|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_LSC_XTABLESIZE |  |  |  |       |  |  |  |   |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5                  |  |  |  | 4     |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 31                 |  |  |  | Reset |  |  |  |   |  |  |  |  |  |  |  |

**ISP\_LSC\_XTABLESIZE** Configures the number of horizontal grids in the LSC module. This value is obtained by  $fix((line_{number} - 1)/2/32) + 2$ , where  $fix()$  denotes the rounding. (R/W)

Register 32.18. ISP\_DEMOSAIC\_MATRIX\_CTRL\_REG (0x0058)

|            |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |                           |    |  |  |  |  |  |  |                                  |    |  |  |  |  |  |  |                                  |    |  |  |  |  |  |  |   |   |  |  |  |  |  |  |   |   |  |  |  |  |  |  |   |   |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  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| 31         |  |  |  |  |  |  |  | 25                        |  |  |  |  |  |  |  | 24                        | 23 |  |  |  |  |  |  |                                  | 16 |  |  |  |  |  |  |                                  | 15 |  |  |  |  |  |  |   | 8 |  |  |  |  |  |  |   | 7 |  |  |  |  |  |  |   | 0 |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  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| 0          |  |  |  |  |  |  |  | 0                         |  |  |  |  |  |  |  | 0                         |    |  |  |  |  |  |  | 0                                |    |  |  |  |  |  |  | 0                                |    |  |  |  |  |  |  | 0 |   |  |  |  |  |  |  | 0 |   |  |  |  |  |  |  | 0 |   |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  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|  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

**ISP\_DEMOSAIC\_TAIL\_PIXEN\_PULSE\_TL** Configures the data control cycle for the tail-row data rate during pixel-to-matrix conversion in the demosaic module.

Within [ISP\\_DEMOSAIC\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) clock cycles, only the first [ISP\\_DEMOSAIC\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) cycles are valid. Be cautious to configure this field, to prevent data processing from being deferred to the next frame.

This feature is enabled only when both [ISP\\_DEMOSAIC\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) and [ISP\\_DEMOSAIC\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) are non-zero, and  $ISP\_DEMOSAIC\_TAIL\_PIXEN\_PULSE\_TH < ISP\_DEMOSAIC\_TAIL\_PIXEN\_PULSE\_TL$ . (R/W)

**ISP\_DEMOSAIC\_TAIL\_PIXEN\_PULSE\_TH** Configures the valid data period of the tail-row data rate during pixel-to-matrix conversion in the demosaic module, which must be less than [ISP\\_HADR\\_NUM](#) - 1. (R/W)

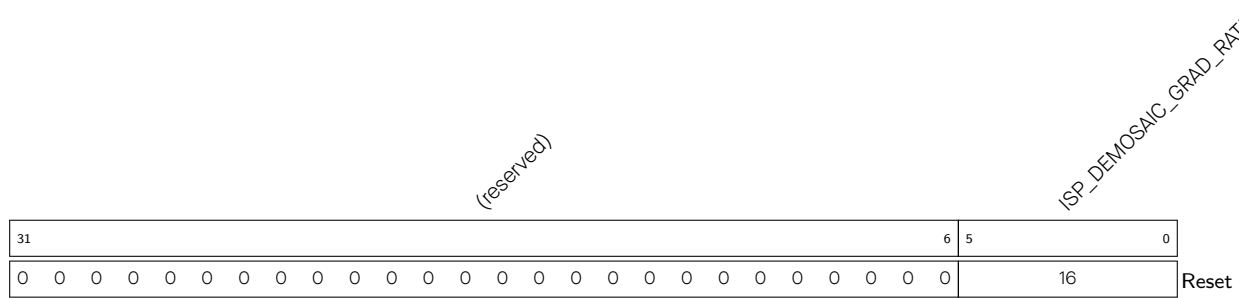
**ISP\_DEMOSAIC\_PADDING\_DATA** Configures the padding data used during image edge expansion in pixel-to-matrix conversion of the demosaic module. (R/W)

**ISP\_DEMOSAIC\_PADDING\_MODE** Configures the method of image edge expansion during pixel-to-matrix conversion in the demosaic module.

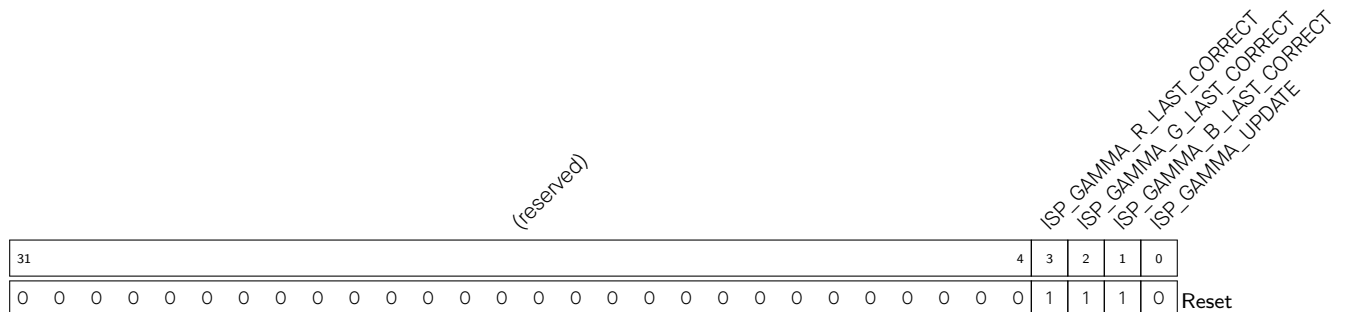
0: Automatically padded with pixel values from the image edge

1: Padded with the data in [ISP\\_DEMOSAIC\\_PADDING\\_DATA](#)

(R/W)

**Register 32.19. ISP\_DEMOSAIC\_GRAD\_RATIO\_REG (0x005C)**

**ISP\_DEMOSAIC\_GRAD\_RATIO** Configures the demosaic effect, with bits [5:4] as the integer part and bits [3:0] as the fractional part. (R/W)

**Register 32.20. ISP\_GAMMA\_CTRL\_REG (0x0074)**

**ISP\_GAMMA\_UPDATE** Configures whether to update the gamma curve parameters. Writing 1 to this field updates the gamma curve parameters. It will be automatically cleared to 0 after the update is complete. (R/W)

**ISP\_GAMMA\_B\_LAST\_CORRECT** Configures whether to enable correction for the parameters of the last interval on the X axis of B channel gamma curve.  
 0: Not enable  
 1: Enable  
 (R/W)

**ISP\_GAMMA\_G\_LAST\_CORRECT** Configures whether to enable correction for the parameters of the last interval on the X axis of G channel gamma curve.  
 0: Not enable  
 1: Enable  
 (R/W)

**ISP\_GAMMA\_R\_LAST\_CORRECT** Configures whether to enable correction for the parameters of the last interval on the X axis of X channel gamma curve.  
 0: Not enable  
 1: Enable  
 (R/W)

**Register 32.21. ISP\_GAMMA\_RY1\_REG (0x0078)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_R_Y00 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y01 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y02 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y03 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x10            |    | 0x20 |    | 0x30 |   | 0x40 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_R\_Y03** Configures the value of the 3rd point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y02** Configures the value of the 2nd point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y01** Configures the value of the 1st point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y00** Configures the value of the 0th point on the Y axis of R channel gamma curve.  
(R/W)

**Register 32.22. ISP\_GAMMA\_RY2\_REG (0x007C)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_R_Y04 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y05 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y06 |    |      |    |      |   |      |   |
| ISP_GAMMA_R_Y07 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x50            |    | 0x60 |    | 0x70 |   | 0x80 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_R\_Y07** Configures the value of the 7th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y06** Configures the value of the 6th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y05** Configures the value of the 5th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y04** Configures the value of the 4th point on the Y axis of R channel gamma curve.  
(R/W)

**Register 32.23. ISP\_GAMMA\_RY3\_REG (0x0080)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_R_Y08 |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y09 |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y0A |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y0B |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0x90            |    |    |    |    |   |   |   |
| 0xa0            |    |    |    |    |   |   |   |
| 0xb0            |    |    |    |    |   |   |   |
| 0xc0            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_R\_Y0B** Configures the value of the 11th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y0A** Configures the value of the 10th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y09** Configures the value of the 9th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y08** Configures the value of the 8th point on the Y axis of R channel gamma curve.  
(R/W)

**Register 32.24. ISP\_GAMMA\_RY4\_REG (0x0084)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_R_Y0C |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y0D |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y0E |    |    |    |    |   |   |   |
| ISP_GAMMA_R_Y0F |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0xd0            |    |    |    |    |   |   |   |
| 0xe0            |    |    |    |    |   |   |   |
| 0xf0            |    |    |    |    |   |   |   |
| 0xff            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_R\_Y0F** Configures the value of the 15th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y0E** Configures the value of the 14th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y0D** Configures the value of the 13th point on the Y axis of R channel gamma curve.  
(R/W)

**ISP\_GAMMA\_R\_Y0C** Configures the value of the 12th point on the Y axis of R channel gamma curve.  
(R/W)

**Register 32.25. ISP\_GAMMA\_GY1\_REG (0x0088)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_G_Y00 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y01 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y02 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y03 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x10            |    | 0x20 |    | 0x30 |   | 0x40 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_G\_Y03** Configures the value of the 3rd point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y02** Configures the value of the 2nd point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y01** Configures the value of the 1st point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y00** Configures the value of the 0th point on the Y axis of G channel gamma curve.  
(R/W)

**Register 32.26. ISP\_GAMMA\_GY2\_REG (0x008C)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_G_Y04 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y05 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y06 |    |      |    |      |   |      |   |
| ISP_GAMMA_G_Y07 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x50            |    | 0x60 |    | 0x70 |   | 0x80 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_G\_Y07** Configures the value of the 7th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y06** Configures the value of the 6th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y05** Configures the value of the 5th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y04** Configures the value of the 4th point on the Y axis of G channel gamma curve.  
(R/W)

**Register 32.27. ISP\_GAMMA\_GY3\_REG (0x0090)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_G_Y08 |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y09 |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y0A |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y0B |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0x90            |    |    |    |    |   |   |   |
| 0xa0            |    |    |    |    |   |   |   |
| 0xb0            |    |    |    |    |   |   |   |
| 0xc0            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_G\_Y0B** Configures the value of the 11th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y0A** Configures the value of the 10th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y09** Configures the value of the 9th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y08** Configures the value of the 8th point on the Y axis of G channel gamma curve.  
(R/W)

**Register 32.28. ISP\_GAMMA\_GY4\_REG (0x0094)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_G_Y0C |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y0D |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y0E |    |    |    |    |   |   |   |
| ISP_GAMMA_G_Y0F |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0xd0            |    |    |    |    |   |   |   |
| 0xe0            |    |    |    |    |   |   |   |
| 0xf0            |    |    |    |    |   |   |   |
| 0xff            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_G\_Y0F** Configures the value of the 15th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y0E** Configures the value of the 14th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y0D** Configures the value of the 13th point on the Y axis of G channel gamma curve.  
(R/W)

**ISP\_GAMMA\_G\_Y0C** Configures the value of the 12th point on the Y axis of G channel gamma curve.  
(R/W)

**Register 32.29. ISP\_GAMMA\_BY1\_REG (0x0098)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_B_Y00 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y01 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y02 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y03 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x10            |    | 0x20 |    | 0x30 |   | 0x40 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_B\_Y03** Configures the value of the 3rd point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y02** Configures the value of the 2nd point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y01** Configures the value of the 1st point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y00** Configures the value of the 0th point on the Y axis of B channel gamma curve.  
(R/W)

**Register 32.30. ISP\_GAMMA\_BY2\_REG (0x009C)**

|                 |    |      |    |      |   |      |   |
|-----------------|----|------|----|------|---|------|---|
| ISP_GAMMA_B_Y04 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y05 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y06 |    |      |    |      |   |      |   |
| ISP_GAMMA_B_Y07 |    |      |    |      |   |      |   |
| 31              | 24 | 23   | 16 | 15   | 8 | 7    | 0 |
| 0x50            |    | 0x60 |    | 0x70 |   | 0x80 |   |
| Reset           |    |      |    |      |   |      |   |

**ISP\_GAMMA\_B\_Y07** Configures the value of the 7th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y06** Configures the value of the 6th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y05** Configures the value of the 5th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y04** Configures the value of the 4th point on the Y axis of B channel gamma curve.  
(R/W)



**Register 32.31. ISP\_GAMMA\_BY3\_REG (0x00A0)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_B_Y08 |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y09 |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y0A |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y0B |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0x90            |    |    |    |    |   |   |   |
| 0xa0            |    |    |    |    |   |   |   |
| 0xb0            |    |    |    |    |   |   |   |
| 0xc0            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_B\_Y0B** Configures the value of the 11th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y0A** Configures the value of the 10th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y09** Configures the value of the 9th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y08** Configures the value of the 8th point on the Y axis of B channel gamma curve.  
(R/W)

**Register 32.32. ISP\_GAMMA\_BY4\_REG (0x00A4)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_GAMMA_B_Y0C |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y0D |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y0E |    |    |    |    |   |   |   |
| ISP_GAMMA_B_Y0F |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0xd0            |    |    |    |    |   |   |   |
| 0xe0            |    |    |    |    |   |   |   |
| 0xf0            |    |    |    |    |   |   |   |
| 0xff            |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_GAMMA\_B\_Y0F** Configures the value of the 15th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y0E** Configures the value of the 14th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y0D** Configures the value of the 13th point on the Y axis of B channel gamma curve.  
(R/W)

**ISP\_GAMMA\_B\_Y0C** Configures the value of the 12th point on the Y axis of B channel gamma curve.  
(R/W)

**Register 32.33. ISP\_GAMMA\_RX1\_REG (0x00A8)**

|            |   |   |   |   |   |   |   |                 |    |                 |    |                 |    |                 |    |                 |    |                 |   |                 |   |                 |   |   |       |
|------------|---|---|---|---|---|---|---|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|---|-----------------|---|-----------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   | ISP_GAMMA_R_X00 |    | ISP_GAMMA_R_X01 |    | ISP_GAMMA_R_X02 |    | ISP_GAMMA_R_X03 |    | ISP_GAMMA_R_X04 |    | ISP_GAMMA_R_X05 |   | ISP_GAMMA_R_X06 |   | ISP_GAMMA_R_X07 |   |   |       |
| 31         |   |   |   |   |   |   |   | 24              | 23 | 21              | 20 | 18              | 17 | 15              | 14 | 12              | 11 | 9               | 8 | 6               | 5 | 3               | 2 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4 |                 | 4 |                 | 4 |   | Reset |

**ISP\_GAMMA\_R\_X07** Configures the width of the 7th interval on the X axis of R channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_R\_X06** Configures the width of the 6th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X05** Configures the width of the 5th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X04** Configures the width of the 4th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X03** Configures the width of the 3rd interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X02** Configures the width of the 2nd interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X01** Configures the width of the 1st interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X00** Configures the width of the 0th interval on the X axis of R channel gamma curve. (R/W)

**Register 32.34. ISP\_GAMMA\_RX2\_REG (0x00AC)**

|            |   |   |   |   |   |   |   |                 |    |    |    |                 |    |    |    |                 |    |   |   |                 |   |   |   |                 |       |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |
|------------|---|---|---|---|---|---|---|-----------------|----|----|----|-----------------|----|----|----|-----------------|----|---|---|-----------------|---|---|---|-----------------|-------|--|--|-----------------|--|--|--|-----------------|--|--|--|-----------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   | ISP_GAMMA_R_X08 |    |    |    | ISP_GAMMA_R_X09 |    |    |    | ISP_GAMMA_R_X0A |    |   |   | ISP_GAMMA_R_X0B |   |   |   | ISP_GAMMA_R_X0C |       |  |  | ISP_GAMMA_R_X0D |  |  |  | ISP_GAMMA_R_X0E |  |  |  | ISP_GAMMA_R_X0F |  |  |  |
| 31         |   |   |   |   |   |   |   | 24              | 23 | 21 | 20 | 18              | 17 | 15 | 14 | 12              | 11 | 9 | 8 | 6               | 5 | 3 | 2 | 0               |       |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4               | 4  |    | 4  |                 | 4  |    | 4  |                 | 4  |   | 4 |                 | 4 |   | 4 |                 | Reset |  |  |                 |  |  |  |                 |  |  |  |                 |  |  |  |

**ISP\_GAMMA\_R\_X0F** Configures the width of the 15th interval on the X axis of R channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_R\_X0E** Configures the width of the 14th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X0D** Configures the width of the 13th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X0C** Configures the width of the 12th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X0B** Configures the width of the 11th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X0A** Configures the width of the 10th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X09** Configures the width of the 9th interval on the X axis of R channel gamma curve. (R/W)

**ISP\_GAMMA\_R\_X08** Configures the width of the 8th interval on the X axis of R channel gamma curve. (R/W)

**Register 32.35. ISP\_GAMMA\_GX1\_REG (0x00B0)**

|            |   |   |   |   |   |   |   |                 |    |                 |    |                 |    |                 |    |                 |    |                 |   |                 |   |                 |   |   |       |
|------------|---|---|---|---|---|---|---|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|---|-----------------|---|-----------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   | ISP_GAMMA_G_X00 |    | ISP_GAMMA_G_X01 |    | ISP_GAMMA_G_X02 |    | ISP_GAMMA_G_X03 |    | ISP_GAMMA_G_X04 |    | ISP_GAMMA_G_X05 |   | ISP_GAMMA_G_X06 |   | ISP_GAMMA_G_X07 |   |   |       |
| 31         |   |   |   |   |   |   |   | 24              | 23 | 21              | 20 | 18              | 17 | 15              | 14 | 12              | 11 | 9               | 8 | 6               | 5 | 3               | 2 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4 |                 | 4 |                 | 4 |   | Reset |

**ISP\_GAMMA\_G\_X07** Configures the width of the 7th interval on the X axis of G channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_G\_X06** Configures the width of the 6th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X05** Configures the width of the 5th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X04** Configures the width of the 4th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X03** Configures the width of the 3rd interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X02** Configures the width of the 2nd interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X01** Configures the width of the 1st interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X00** Configures the width of the 0th interval on the X axis of G channel gamma curve. (R/W)

**Register 32.36. ISP\_GAMMA\_GX2\_REG (0x00B4)**

|            |   |   |   |   |   |   |   |                 |    |                 |    |                 |    |                 |    |                 |    |                 |   |                 |   |                 |   |   |       |
|------------|---|---|---|---|---|---|---|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|---|-----------------|---|-----------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   | ISP_GAMMA_G_X08 |    | ISP_GAMMA_G_X09 |    | ISP_GAMMA_G_X0A |    | ISP_GAMMA_G_X0B |    | ISP_GAMMA_G_X0C |    | ISP_GAMMA_G_X0D |   | ISP_GAMMA_G_X0E |   | ISP_GAMMA_G_X0F |   |   |       |
| 31         |   |   |   |   |   |   |   | 24              | 23 | 21              | 20 | 18              | 17 | 15              | 14 | 12              | 11 | 9               | 8 | 6               | 5 | 3               | 2 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4 |                 | 4 |                 | 4 |   | Reset |

**ISP\_GAMMA\_G\_X0F** Configures the width of the 15th interval on the X axis of G channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_G\_X0E** Configures the width of the 14th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X0D** Configures the width of the 13th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X0C** Configures the width of the 12th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X0B** Configures the width of the 11th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X0A** Configures the width of the 10th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X09** Configures the width of the 9th interval on the X axis of G channel gamma curve. (R/W)

**ISP\_GAMMA\_G\_X08** Configures the width of the 8th interval on the X axis of G channel gamma curve. (R/W)

**Register 32.37. ISP\_GAMMA\_BX1\_REG (0x00B8)**

| (reserved) |   |   |   |   |   |   |    | ISP_GAMMA_B_X00 |   |  |    | ISP_GAMMA_B_X01 |  |  |    | ISP_GAMMA_B_X02 |  |  |    | ISP_GAMMA_B_X03 |  |  |    | ISP_GAMMA_B_X04 |  |  |   | ISP_GAMMA_B_X05 |  |  |   | ISP_GAMMA_B_X06 |  |  |   | ISP_GAMMA_B_X07 |  |   |       |
|------------|---|---|---|---|---|---|----|-----------------|---|--|----|-----------------|--|--|----|-----------------|--|--|----|-----------------|--|--|----|-----------------|--|--|---|-----------------|--|--|---|-----------------|--|--|---|-----------------|--|---|-------|
| 31         |   |   |   |   |   |   | 24 | 23              |   |  | 21 | 20              |  |  | 18 | 17              |  |  | 15 | 14              |  |  | 12 | 11              |  |  | 9 | 8               |  |  | 6 | 5               |  |  | 3 | 2               |  | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0               | 4 |  |    | 4               |  |  |    | 4               |  |  |    | 4               |  |  |    | 4               |  |  |   | 4               |  |  |   | 4               |  |  |   | 4               |  |   | Reset |

**ISP\_GAMMA\_B\_X07** Configures the width of the 7th interval on the X axis of B channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_B\_X06** Configures the width of the 6th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X05** Configures the width of the 5th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X04** Configures the width of the 4th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X03** Configures the width of the 3rd interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X02** Configures the width of the 2nd interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X01** Configures the width of the 1st interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X00** Configures the width of the 0th interval on the X axis of B channel gamma curve. (R/W)

**Register 32.38. ISP\_GAMMA\_BX2\_REG (0x00BC)**

|            |   |   |   |   |   |   |   |                 |    |                 |    |                 |    |                 |    |                 |    |                 |   |                 |   |                 |   |   |       |
|------------|---|---|---|---|---|---|---|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|----|-----------------|---|-----------------|---|-----------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   | ISP_GAMMA_B_X08 |    | ISP_GAMMA_B_X09 |    | ISP_GAMMA_B_X0A |    | ISP_GAMMA_B_X0B |    | ISP_GAMMA_B_X0C |    | ISP_GAMMA_B_X0D |   | ISP_GAMMA_B_X0E |   | ISP_GAMMA_B_X0F |   |   |       |
| 31         |   |   |   |   |   |   |   | 24              | 23 | 21              | 20 | 18              | 17 | 15              | 14 | 12              | 11 | 9               | 8 | 6               | 5 | 3               | 2 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4  |                 | 4 |                 | 4 |                 | 4 |   | Reset |

**ISP\_GAMMA\_B\_X0F** Configures the width of the 15th interval on the X axis of B channel gamma curve. Refer to section [32.5.2.5](#) for configuration. (R/W)

**ISP\_GAMMA\_B\_X0E** Configures the width of the 14th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X0D** Configures the width of the 13th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X0C** Configures the width of the 12th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X0B** Configures the width of the 11th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X0A** Configures the width of the 10th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X09** Configures the width of the 9th interval on the X axis of B channel gamma curve. (R/W)

**ISP\_GAMMA\_B\_X08** Configures the width of the 8th interval on the X axis of B channel gamma curve. (R/W)

**Register 32.39. ISP\_AE\_CTRL\_REG (0x00C0)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |   |               |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|---|---------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_AE_SELECT |   | ISP_AE_UPDATE |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2             | 1 | 0             |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 | 0             | Reset |

**ISP\_AE\_UPDATE** Configures AE statistics sampling. With AE enabled, writing 1 triggers a statistics collection. (WT)

**ISP\_AE\_SELECT** Configures the AE sampling point.

0: Use data output from the demosaic module

1: Use data output from the gamma correction module

(R/W)

**Register 32.40. ISP\_AE\_MONITOR\_REG (0x00C4)**

|            |   |   |   |   |   |   |   |   |   |                       |    |    |  |   |  |                   |    |  |  |  |   |                   |       |  |  |   |  |
|------------|---|---|---|---|---|---|---|---|---|-----------------------|----|----|--|---|--|-------------------|----|--|--|--|---|-------------------|-------|--|--|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   | ISP_AE_MONITOR_PERIOD |    |    |  |   |  | ISP_AE_MONITOR_TH |    |  |  |  |   | ISP_AE_MONITOR_TL |       |  |  |   |  |
| 31         |   |   |   |   |   |   |   |   |   |                       | 22 | 21 |  |   |  | 16                | 15 |  |  |  | 8 | 7                 |       |  |  | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                     | 0  |    |  | 0 |  |                   | 0  |  |  |  |   |                   | Reset |  |  |   |  |

Reset

**ISP\_AE\_MONITOR\_TL** Configures the lower threshold for AE luminance monitoring. (R/W)**ISP\_AE\_MONITOR\_TH** Configures the upper threshold for AE luminance monitoring. (R/W)**ISP\_AE\_MONITOR\_PERIOD** Configures the frame interval for AE monitoring. (R/W)**Register 32.41. ISP\_AE\_BX\_REG (0x00C8)**

|            |   |   |   |   |   |   |   |   |   |                |    |  |  |  |  |  |  |  |    |     |                |  |  |  |  |   |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|----------------|----|--|--|--|--|--|--|--|----|-----|----------------|--|--|--|--|---|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   | ISP_AE_X_START |    |  |  |  |  |  |  |  |    |     | ISP_AE_X_BSIZE |  |  |  |  |   |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   | 22             | 21 |  |  |  |  |  |  |  | 11 | 10  |                |  |  |  |  | 0 |  |  |  |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              |    |  |  |  |  |  |  |  |    | 384 |                |  |  |  |  |   |  |  |  | Reset |

Reset

**ISP\_AE\_X\_BSIZE** Configures the horizontal size of each sub-window. (R/W)**ISP\_AE\_X\_START** Configures the starting coordinate of the AE statistical window in the horizontal direction. (R/W)**Register 32.42. ISP\_AE\_BY\_REG (0x00CC)**

|            |   |   |   |   |   |   |   |   |   |                |    |  |  |  |  |  |  |  |    |    |                |  |  |  |  |   |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|----------------|----|--|--|--|--|--|--|--|----|----|----------------|--|--|--|--|---|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   | ISP_AE_Y_START |    |  |  |  |  |  |  |  |    |    | ISP_AE_Y_BSIZE |  |  |  |  |   |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   | 22             | 21 |  |  |  |  |  |  |  | 11 | 10 |                |  |  |  |  | 0 |  |  |  |  |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0  |  |  |  |  |  |  |  |    |    | 216            |  |  |  |  |   |  |  |  |  | Reset |

Reset

**ISP\_AE\_Y\_BSIZE** Configures the vertical dimension of each sub-window. (R/W)**ISP\_AE\_Y\_START** Configures the starting coordinate of the AE statistical window in the vertical direction. (R/W)



**Register 32.43. ISP\_AE\_WINPIXNUM\_REG (0x00D0)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_AE_SUBWIN_PIXNUM |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17                   | 16 |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 82944                |    |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

**ISP\_AE\_SUBWIN\_PIXNUM** Configures the number of pixels in each sub-window. (R/W)

**Register 32.44. ISP\_AE\_WIN\_RECIPROCAL\_REG (0x00D4)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_AE_SUBWIN_RECIP |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 20                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 19 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**ISP\_AE\_SUBWIN\_RECIP** Configures the reciprocal of the number of pixels in each sub-window. It is a 20-bit fractional number, with [19:0] representing the fractional part. (R/W)

**Register 32.45. ISP\_SHARP\_CTRL0\_REG (0x00F4)**

|                       |  |  |  |  |  |  |  |                      |    |  |  |  |  |  |  |                          |    |    |  |  |  |  |  |                         |  |   |   |  |  |  |  |       |  |  |   |
|-----------------------|--|--|--|--|--|--|--|----------------------|----|--|--|--|--|--|--|--------------------------|----|----|--|--|--|--|--|-------------------------|--|---|---|--|--|--|--|-------|--|--|---|
| ISP_SHARP_AMOUNT_HIGH |  |  |  |  |  |  |  | ISP_SHARP_AMOUNT_LOW |    |  |  |  |  |  |  | ISP_SHARP_THRESHOLD_HIGH |    |    |  |  |  |  |  | ISP_SHARP_THRESHOLD_LOW |  |   |   |  |  |  |  |       |  |  |   |
| 31                    |  |  |  |  |  |  |  | 24                   | 23 |  |  |  |  |  |  |                          | 16 | 15 |  |  |  |  |  |                         |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 0                     |  |  |  |  |  |  |  | 0                    |    |  |  |  |  |  |  | 0                        |    |    |  |  |  |  |  | 0                       |  |   |   |  |  |  |  | Reset |  |  |   |

**ISP\_SHARP\_THRESHOLD\_LOW** Configures the threshold for sharpening high-frequency details. Refer to section 32.5.2.7 for configuration. (R/W)

**ISP\_SHARP\_THRESHOLD\_HIGH** Configures the threshold for sharpening high-frequency edges. Refer to section 32.5.2.7 for configuration. (R/W)

**ISP\_SHARP\_AMOUNT\_LOW** Configures the gain for sharpening high-frequency details. Refer to section 32.5.2.7 for configuration. (R/W)

**ISP\_SHARP\_AMOUNT\_HIGH** Configures the gain for sharpening high-frequency edges. Refer to section 32.5.2.7 for configuration. (R/W)

**Register 32.46. ISP\_SHARP\_FILTER0\_REG (0x00F8)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                        |  |   |    |                        |  |  |   |                        |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|------------------------|--|---|----|------------------------|--|--|---|------------------------|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | ISP_SHARP_FILTER_COE02 |  |   |    | ISP_SHARP_FILTER_COE01 |  |  |   | ISP_SHARP_FILTER_COE00 |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15 | 14                     |  |   | 10 | 9                      |  |  | 5 | 4                      |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1                      |  | 2 |    | 1                      |  |  |   |                        |  |  |   |

Reset

**ISP\_SHARP\_FILTER\_COE00** Configures the value of coordinate 00 in the low-pass filter template of the sharpen module. (R/W)

**ISP\_SHARP\_FILTER\_COE01** Configures the value of coordinate 01 in the low-pass filter template of the sharpen module. (R/W)

**ISP\_SHARP\_FILTER\_COE02** Configures the value of coordinate 02 in the low-pass filter template of the sharpen module. (R/W)

**Register 32.47. ISP\_SHARP\_FILTER1\_REG (0x00FC)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                        |  |   |    |                        |  |  |   |                        |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|------------------------|--|---|----|------------------------|--|--|---|------------------------|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | ISP_SHARP_FILTER_COE12 |  |   |    | ISP_SHARP_FILTER_COE11 |  |  |   | ISP_SHARP_FILTER_COE10 |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15 | 14                     |  |   | 10 | 9                      |  |  | 5 | 4                      |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 2                      |  | 4 |    | 2                      |  |  |   |                        |  |  |   |

Reset

**ISP\_SHARP\_FILTER\_COE10** Configures the value of coordinate 10 in the low-pass filter template of the sharpen module. (R/W)

**ISP\_SHARP\_FILTER\_COE11** Configures the value of coordinate 11 in the low-pass filter template of the sharpen module. (R/W)

**ISP\_SHARP\_FILTER\_COE12** Configures the value of coordinate 12 in the low-pass filter template of the sharpen module. (R/W)

Register 32.48. ISP\_SHARP\_FILTER2\_REG (0x0100)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                        |  |  |    |                        |  |   |   |                        |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|------------------------|--|--|----|------------------------|--|---|---|------------------------|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | ISP_SHARP_FILTER_COE22 |  |  |    | ISP_SHARP_FILTER_COE21 |  |   |   | ISP_SHARP_FILTER_COE20 |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15 | 14                     |  |  | 10 | 9                      |  |   | 5 | 4                      |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1                      |  |  | 2  |                        |  | 1 |   |                        |  |  | Reset |

- ISP\_SHARP\_FILTER\_COE20 Configures the value of coordinate 20 in the low-pass filter template of the sharpen module. (R/W)
- ISP\_SHARP\_FILTER\_COE21 Configures the value of coordinate 21 in the low-pass filter template of the sharpen module. (R/W)
- ISP\_SHARP\_FILTER\_COE22 Configures the value of coordinate 22 in the low-pass filter template of the sharpen module. (R/W)

**Register 32.49. ISP\_SHARP\_MATRIX\_CTRL\_REG (0x0104)**

|                 |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                        |    |  |  |  |  |  |  |                               |    |  |  |  |  |  |  |                               |    |  |  |  |  |  |  |     |   |  |  |  |  |  |  |       |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|------------------------|----|--|--|--|--|--|--|-------------------------------|----|--|--|--|--|--|--|-------------------------------|----|--|--|--|--|--|--|-----|---|--|--|--|--|--|--|-------|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | ISP_SHARP_PADDING_MODE |  |  |  |  |  |  |  | ISP_SHARP_PADDING_DATA |    |  |  |  |  |  |  | ISP_SHARP_TAIL_PIXEN_PULSE_TH |    |  |  |  |  |  |  | ISP_SHARP_TAIL_PIXEN_PULSE_TL |    |  |  |  |  |  |  |     |   |  |  |  |  |  |  |       |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 25                     |  |  |  |  |  |  |  | 24                     | 23 |  |  |  |  |  |  |                               | 16 |  |  |  |  |  |  |                               | 15 |  |  |  |  |  |  |     | 8 |  |  |  |  |  |  |       | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0                      |  |  |  |  |  |  |  | 0                      |    |  |  |  |  |  |  | 0x0                           |    |  |  |  |  |  |  | 0x0                           |    |  |  |  |  |  |  | 0x0 |   |  |  |  |  |  |  | Reset |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**ISP\_SHARP\_TAIL\_PIXEN\_PULSE\_TL** Configures the data control cycle for the tail-row data rate during pixel-to-matrix conversion in the sharpen module.

Within [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) clock cycles, only the first [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) cycles are valid. Be cautious to configure this field, to prevent data processing from being deferred to the next frame.

This feature is enabled only when both [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TL](#) and [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) are non-zero, and [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TH](#) < [ISP\\_SHARP\\_TAIL\\_PIXEN\\_PULSE\\_TL](#). (R/W)

**ISP\_SHARP\_TAIL\_PIXEN\_PULSE\_TH** Configures the valid data period of the tail-row data rate during pixel-to-matrix conversion in the sharpen module, which must be less than [ISP\\_HADR\\_NUM](#) - 1. (R/W)

**ISP\_SHARP\_PADDING\_DATA** Configures the padding data used during image edge expansion in pixel-to-matrix conversion of the sharpen module. (R/W)

**ISP\_SHARP\_PADDING\_MODE** Configures the method of image edge expansion during pixel-to-matrix conversion in the sharpen module.

0: Automatically padded with pixel values from the image edge

1: Padded with the data in [ISP\\_SHARP\\_PADDING\\_DATA](#)

(R/W)

**Register 32.50. ISP\_SHARP\_CTRL1\_REG (0x0108)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_SHARP_GRADIENT_MAX |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                      |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0                    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**ISP\_SHARP\_GRADIENT\_MAX** Represents the maximum pixel value of high-frequency components in the sharpen module, automatically refreshed every frame. (RO)

**Register 32.51. ISP\_DMA\_CNTL\_REG (0x010C)**

|                  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|------------------|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|
| ISP_DMA_INTERVAL |  |  |  |  |  |  |  |  |  |  |  | ISP_DMA_BURST_LEN |  |  |  |  |  |  |  |  |  |  |  | ISP_DMA_DATA_TYPE |  |  |  |  |  |  |  |  |  |  |  | ISP_DMA_UPDATE_REG |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| 31               |  |  |  |  |  |  |  |  |  |  |  | 20                |  |  |  |  |  |  |  |  |  |  |  | 19                |  |  |  |  |  |  |  |  |  |  |  | 8                  |  |  |  |  |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  |  |  |  |  | 2     |  |  |  |  |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |
| 0x1              |  |  |  |  |  |  |  |  |  |  |  | 0x80              |  |  |  |  |  |  |  |  |  |  |  | 0x2a              |  |  |  |  |  |  |  |  |  |  |  | 0                  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |

**ISP\_DMA\_EN** Configures whether to trigger VDMA transfer of one frame of data.

0: Not trigger

1: Trigger

(WT)

**ISP\_DMA\_UPDATE\_REG** Configures whether to update the configuration for [ISP\\_DMA\\_DATA\\_TYPE](#), [ISP\\_DMA\\_BURST\\_LEN](#), and [ISP\\_DMA\\_INTERVAL](#).

0: Not update

1: Update, will be automatically cleared to 0 after the update is complete

(R/W)

**ISP\_DMA\_DATA\_TYPE** Configures the Image Interface data\_type for the transferred data.

0x2A: RAW8

0x2B: RAW10

0x2C: RAW12

Others: Invalid

(R/W)

**ISP\_DMA\_BURST\_LEN** Configures the burst length for one VDMA transfer, which needs to align with the VDMA configuration. (R/W)

**ISP\_DMA\_INTERVAL** Configures the interval of VDMA requests. 12'b1: 1 clock cycle, 12'b11: 2 clock cycles, etc. (R/W)

Register 32.52. ISP\_DMA\_RAW\_DATA\_REG (0x0110)

|                           |    |   |   |   |   |   |   |   |   |            |   |  |  |  |  |  |  |  |  |                       |    |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |
|---------------------------|----|---|---|---|---|---|---|---|---|------------|---|--|--|--|--|--|--|--|--|-----------------------|----|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|---|
| ISP_DMA_RAW_NUM_TOTAL_SET |    |   |   |   |   |   |   |   |   | (reserved) |   |  |  |  |  |  |  |  |  | ISP_DMA_RAW_NUM_TOTAL |    |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |
| 31                        | 30 |   |   |   |   |   |   |   |   |            |   |  |  |  |  |  |  |  |  | 22                    | 21 |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  | 0 |
| 0                         | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 |  |  |  |  |  |  |  |  |                       |    |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |   |

**ISP\_DMA\_RAW\_NUM\_TOTAL** Configures the amount of 64-bit data in a frame of image. (R/W)

**ISP\_DMA\_RAW\_NUM\_TOTAL\_SET** Configures whether to update the configuration for [ISP\\_DMA\\_RAW\\_NUM\\_TOTAL](#).

0: Not update

1: Update

(WT)

Register 32.53. ISP\_CAM\_CNTL\_REG (0x0114)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |   |   |   |               |   |       |  |                    |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|---|---|---|---------------|---|-------|--|--------------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_CAM_CLK_INV |   |   |   | ISP_CAM_RESET |   |       |  | ISP_CAM_UPDATE_REG |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4               | 3 | 2 | 1 | 0             |   |       |  |                    |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 0 | 1 | 0 | 0             | 0 | Reset |  |                    |  |  |  |

**ISP\_CAM\_EN** Configures whether to enable the input via the DVP interface.

0: Disable

1: Enable

(R/W)

**ISP\_CAM\_UPDATE\_REG** Configures whether to update the configuration for [ISP\\_CAM\\_CONF\\_REG](#).

0: Not update

1: Update

(R/W)

**ISP\_CAM\_RESET** Configures whether to reset the DVP input configuration.

0: Not reset

1: Reset

(R/W)

**ISP\_CAM\_CLK\_INV** Configures whether to invert the DVP clock.

0: Not invert

1: Invert

(R/W)

**Register 32.54. ISP\_CAM\_CONF\_REG (0x0118)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |    |    |    |                            |   |   |      |                   |  |  |  |                   |   |   |       |                |  |  |  |                   |  |  |  |                    |  |  |  |                    |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|----|----|----|----------------------------|---|---|------|-------------------|--|--|--|-------------------|---|---|-------|----------------|--|--|--|-------------------|--|--|--|--------------------|--|--|--|--------------------|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_CAM_VSYNC_FILTER_EN |    |    |    | ISP_CAM_VSYNC_FILTER_THRES |   |   |      | ISP_CAM_VSYNC_INV |  |  |  | ISP_CAM_HSYNC_INV |   |   |       | ISP_CAM_DE_INV |  |  |  | ISP_CAM_DATA_TYPE |  |  |  | ISP_CAM_2BYTE_MODE |  |  |  | ISP_CAM_DATA_ORDER |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                      | 14 | 13 | 11 | 10                         | 9 | 8 | 7    |                   |  |  |  |                   |   | 2 | 1     | 0              |  |  |  |                   |  |  |  |                    |  |  |  |                    |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                       | 0  |    |    | 0                          | 0 | 0 | 0x2a |                   |  |  |  |                   | 0 | 0 | Reset |                |  |  |  |                   |  |  |  |                    |  |  |  |                    |  |  |  |

Reset

**ISP\_CAM\_DATA\_ORDER** Configures the order of DVP input data.

0: cam\_data\_in

1: cam\_data\_in[7:0], cam\_data\_in[15:8]

(R/W)

**ISP\_CAM\_2BYTE\_MODE** Configures whether to enable the 2-byte mode.

0: Disable

1: Enable

(R/W)

**ISP\_CAM\_DATA\_TYPE** Configures the format of DVP input data.

0x2a: RAW8

0x2b: RAW10

0x2c: RAW12

(R/W)

**ISP\_CAM\_DE\_INV** Configures whether to invert the DVP de signal.

0: Not invert

1: Invert

(R/W)

**ISP\_CAM\_HSYNC\_INV** Configures whether to invert the DVP hsync signal.

0: Not invert

1: Invert

(R/W)

**ISP\_CAM\_VSYNC\_INV** Configures whether to invert the DVP vsync signal.

0: Not invert

1: Invert

(R/W)

**ISP\_CAM\_VSYNC\_FILTER\_THRES** Configures vsync filtering. Vsyzns shorter than this length will be filtered out. (R/W)**ISP\_CAM\_VSYNC\_FILTER\_EN** Configures whether to enable the vsync filtering.

0: Disable

1: Enable

(R/W)

### Register 32.55. ISP\_AF\_CTRL0\_REG (0x011C)

|                 |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                      |  |  |  |  |  |            |  |        |  |  |  |                      |  |        |  |  |  |            |  |           |  |  |  |                    |  |   |  |  |  |  |  |       |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|------------|--|--------|--|--|--|----------------------|--|--------|--|--|--|------------|--|-----------|--|--|--|--------------------|--|---|--|--|--|--|--|-------|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | ISP_AF_ENV_PERIOD |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  | ISP_AF_ENV_THRESHOLD |  |  |  |  |  | (reserved) |  |        |  |  |  | ISP_AF_MANUAL_UPDATE |  |        |  |  |  | (reserved) |  |           |  |  |  | ISP_AF_AUTO_UPDATE |  |   |  |  |  |  |  |       |  |  |  |  |  |
| 31<br>24        |  |  |  |  |  |  |  | 23<br>16          |  |  |  |  |  |  |  | 15<br>12   |  |  |  |  |  |  |  | 11<br>8              |  |  |  |  |  |            |  | 7<br>5 |  |  |  |                      |  | 4<br>3 |  |  |  |            |  | 1<br>0    |  |  |  |                    |  |   |  |  |  |  |  |       |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0                 |  |  |  |  |  |  |  | 0 0 0 0    |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |            |  | 0 0 0  |  |  |  |                      |  | 0      |  |  |  |            |  | 0 0 0 0 0 |  |  |  |                    |  | 0 |  |  |  |  |  | Reset |  |  |  |  |  |

**ISP\_AF\_AUTO\_UPDATE** Configures whether to enable AF automatic statistics.

0: Disable automatic statistics, and manual trigger is required

1: Enable automatic statistics, and AF will perform statistics for every frame with the AF module enabled

(R/W)

**ISP\_AF\_MANUAL\_UPDATE** Configures AF manual statistics. With AF automatic statistics disabled, writing 1 triggers a statistics collection. (WT)

**ISP\_AF\_ENV\_THRESHOLD** Configures the threshold for AF scene monitoring. If **ISP\_AF\_ENV\_USER\_THRESHOLD\_SUM** or **ISP\_AF\_ENV\_USER\_THRESHOLD\_LUM** is 0, an interrupt for scene monitoring will be triggered when the changes in sharpness or luminance exceed the product of the baseline value and this field for two consecutive times. 4 fractional bits. (R/W)

**ISP\_AF\_ENV\_PERIOD** Configures the statistical interval frames for AF scene monitoring. Setting this filed to 0 disables the scene monitoring. (R/W)

### Register 32.56. ISP\_AF\_ENV\_USER\_TH\_SUM\_REG (0x0128)

Diagram of the `ISP_AF_ENV_USER_THRESHOLD_SUM` register. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. The value `0x000000` is shown below the register, indicating the reset value.

|                                      |   |
|--------------------------------------|---|
| <b>ISP_AF_ENV_USER_THRESHOLD_SUM</b> | Configures the threshold for sharpness change in AF scene monitoring. (R/W) |
|--------------------------------------|---|



**Register 32.57. ISP\_AF\_ENV\_USER\_TH\_LUM\_REG (0x012C)**

|            |    |          |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|----|----------|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |    |          | ISP_AF_ENV_USER_THRESHOLD_LUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         | 30 | 29       |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0  | 0x000000 |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

**ISP\_AF\_ENV\_USER\_THRESHOLD\_LUM** Configures the threshold for luminance change in AF scene monitoring. (R/W)

**Register 32.58. ISP\_AF\_THRESHOLD\_REG (0x0130)**

|                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved)       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_AF_THRESHOLD |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 3116             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 150              |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0000000000000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 256              |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ISP\_AF\_THRESHOLD** Configures the sharpness threshold for AF statistics. (R/W)

**Register 32.59. ISP\_AF\_HSCALE\_A\_REG (0x0134)**

|            |    |    |   |                 |  |  |  |  |  |  |  |  |  |  |    |            |    |    |   |                 |  |  |  |  |  |  |  |  |  |   |       |
|------------|----|----|---|-----------------|--|--|--|--|--|--|--|--|--|--|----|------------|----|----|---|-----------------|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | ISP_AF_LPOINT_A |  |  |  |  |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AF_RPOINT_A |  |  |  |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                 |  |  |  |  |  |  |  |  |  |  | 16 | 15         | 12 | 11 |   |                 |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 1               |  |  |  |  |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 128             |  |  |  |  |  |  |  |  |  |   | Reset |

**ISP\_AF\_RPOINT\_A** Configures the right boundary coordinate of AF statistical window A, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_LPOINT\_A** Configures the left boundary coordinate of AF statistical window A, recommended to be greater than or equal to 2. (R/W)

**Register 32.60. ISP\_AF\_VSCALE\_A\_REG (0x0138)**

|            |    |    |   |                 |  |  |  |  |  |  |    |            |    |    |   |                 |  |  |  |  |  |  |   |       |
|------------|----|----|---|-----------------|--|--|--|--|--|--|----|------------|----|----|---|-----------------|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | ISP_AF_TPOINT_A |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AF_BPOINT_A |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                 |  |  |  |  |  |  | 16 | 15         | 12 | 11 |   |                 |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 1               |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 128             |  |  |  |  |  |  |   | Reset |

**ISP\_AF\_BPOINT\_A** Configures the bottom boundary coordinate of AF statistical window A, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_TPOINT\_A** Configures the top boundary coordinate of AF statistical window A, recommended to be greater than or equal to 2. (R/W)

**Register 32.61. ISP\_AF\_HSCALE\_B\_REG (0x013C)**

|            |    |    |   |                 |  |  |  |  |  |  |    |            |    |    |   |                 |  |  |  |  |  |  |  |       |
|------------|----|----|---|-----------------|--|--|--|--|--|--|----|------------|----|----|---|-----------------|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | ISP_AF_LPOINT_B |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AF_RPOINT_B |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 |   |                 |  |  |  |  |  |  | 16 | 15         | 12 | 11 | 0 |                 |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0 | 1               |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 128             |  |  |  |  |  |  |  | Reset |

**ISP\_AF\_RPOINT\_B** Configures the right boundary coordinate of AF statistical window B, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_LPOINT\_B** Configures the left boundary coordinate of AF statistical window B, recommended to be greater than or equal to 2. (R/W)

**Register 32.62. ISP\_AF\_VSCALE\_B\_REG (0x0140)**

|            |    |    |   |                 |  |  |  |  |  |  |    |            |    |    |   |                 |  |  |  |  |  |  |   |       |
|------------|----|----|---|-----------------|--|--|--|--|--|--|----|------------|----|----|---|-----------------|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | ISP_AF_TPOINT_B |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AF_BPOINT_B |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                 |  |  |  |  |  |  | 16 | 15         | 12 | 11 |   |                 |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 1               |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 128             |  |  |  |  |  |  |   | Reset |

**ISP\_AF\_BPOINT\_B** Configures the bottom boundary coordinate of AF statistical window B, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_TPOINT\_B** Configures the top boundary coordinate of AF statistical window B, recommended to be greater than or equal to 2. (R/W)

**Register 32.63. ISP\_AF\_HSCALE\_C\_REG (0x0144)**

|            |    |    |   |                 |  |  |    |    |  |    |    |            |   |   |   |                 |  |  |  |  |  |  |   |
|------------|----|----|---|-----------------|--|--|----|----|--|----|----|------------|---|---|---|-----------------|--|--|--|--|--|--|---|
| (reserved) |    |    |   | ISP_AF_LPOINT_C |  |  |    |    |  |    |    | (reserved) |   |   |   | ISP_AF_RPOINT_C |  |  |  |  |  |  |   |
| 31         | 28 | 27 |   |                 |  |  | 16 | 15 |  | 12 | 11 |            |   |   |   |                 |  |  |  |  |  |  | 0 |
| 0          | 0  | 0  | 0 | 1               |  |  |    |    |  |    |    | 0          | 0 | 0 | 0 | 128             |  |  |  |  |  |  |   |

Reset

**ISP\_AF\_RPOINT\_C** Configures the right boundary coordinate of AF statistical window C, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_LPOINT\_C** Configures the left boundary coordinate of AF statistical window C, recommended to be greater than or equal to 2. (R/W)

**Register 32.64. ISP\_AF\_VSCALE\_C\_REG (0x0148)**

|            |    |    |   |                 |  |  |    |    |  |    |    |            |   |   |   |                 |  |  |  |  |  |  |   |
|------------|----|----|---|-----------------|--|--|----|----|--|----|----|------------|---|---|---|-----------------|--|--|--|--|--|--|---|
| (reserved) |    |    |   | ISP_AF_TPOINT_C |  |  |    |    |  |    |    | (reserved) |   |   |   | ISP_AF_BPOINT_C |  |  |  |  |  |  |   |
| 31         | 28 | 27 |   |                 |  |  | 16 | 15 |  | 12 | 11 |            |   |   |   |                 |  |  |  |  |  |  | 0 |
| 0          | 0  | 0  | 0 | 1               |  |  |    |    |  |    |    | 0          | 0 | 0 | 0 | 128             |  |  |  |  |  |  |   |

Reset

**ISP\_AF\_BPOINT\_C** Configures the bottom boundary coordinate of AF statistical window C, recommended to be less than HNUM-1. (R/W)

**ISP\_AF\_TPOINT\_C** Configures the top boundary coordinate of AF statistical window C, recommended to be greater than or equal to 2. (R/W)

**Register 32.65. ISP\_AWB\_MODE\_REG (0x0164)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |       |   |            |   |              |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------|---|-------|---|------------|---|--------------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_AWB_SAMPLE |   |       |   | (reserved) |   | ISP_AWB_MODE |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5              | 4 | 3     | 2 | 1          | 0 |              |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 3 | Reset |   |            |   |              |  |

Reset

**ISP\_AWB\_MODE** Configures whether to enable the AWB algorithm.

- 1: Enable
  - Others: Invalid
- (R/W)

**ISP\_AWB\_SAMPLE** Configures the AWB sampling point.

- 0: Use data output before processed by CCM
  - 1: Use data output after processed by CCM
- (R/W)

**Register 32.66. ISP\_AWB\_HSCALE\_REG (0x0168)**

|            |    |    |   |                |  |  |  |  |  |  |    |            |    |    |   |                |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|----|----|---|----------------|--|--|--|--|--|--|----|------------|----|----|---|----------------|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | ISP_AWB_LPOINT |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AWB_RPOINT |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                |  |  |  |  |  |  | 16 | 15         | 12 | 11 |   |                |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 0              |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 1919           |  |  |  |  |  |  |  |  |  |  |   | Reset |

Reset

**ISP\_AWB\_RPOINT** Configures the right boundary coordinate of the AWB statistical window. (R/W)**ISP\_AWB\_LPOINT** Configures the left boundary coordinate of the AWB statistical window. (R/W)**Register 32.67. ISP\_AWB\_VSCALE\_REG (0x016C)**

|            |    |    |   |                |  |  |  |  |  |  |    |            |    |    |   |                |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|----|----|---|----------------|--|--|--|--|--|--|----|------------|----|----|---|----------------|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | ISP_AWB_TPOINT |  |  |  |  |  |  |    | (reserved) |    |    |   | ISP_AWB_BPOINT |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                |  |  |  |  |  |  | 16 | 15         | 12 | 11 |   |                |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 0              |  |  |  |  |  |  |    | 0          | 0  | 0  | 0 | 1079           |  |  |  |  |  |  |  |  |  |  |   | Reset |

Reset

**ISP\_AWB\_BPOINT** Configures the bottom boundary coordinate of the AWB statistical window. (R/W)**ISP\_AWB\_TPOINT** Configures the top boundary coordinate of the AWB statistical window. (R/W)**Register 32.68. ISP\_AWB\_TH\_LUM\_REG (0x0170)**

|            |   |   |   |   |   |                 |     |  |  |  |  |  |  |  |  |            |    |   |   |   |   |                 |    |  |  |  |  |  |    |       |  |  |  |  |   |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|-----------------|-----|--|--|--|--|--|--|--|--|------------|----|---|---|---|---|-----------------|----|--|--|--|--|--|----|-------|--|--|--|--|---|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   | ISP_AWB_MAX_LUM |     |  |  |  |  |  |  |  |  | (reserved) |    |   |   |   |   | ISP_AWB_MIN_LUM |    |  |  |  |  |  |    |       |  |  |  |  |   |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   | 26              |     |  |  |  |  |  |  |  |  |            | 16 |   |   |   |   |                 | 15 |  |  |  |  |  | 10 |       |  |  |  |  | 9 |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0               | 765 |  |  |  |  |  |  |  |  |            | 0  | 0 | 0 | 0 | 0 | 0               | 0  |  |  |  |  |  |    | Reset |  |  |  |  |   |  |  |  |  |  |  |  |   |

Reset

**ISP\_AWB\_MIN\_LUM** Configures the lower limit of R+G+B luminance for AWB white patch filtering. (R/W)**ISP\_AWB\_MAX\_LUM** Configures the upper limit of R+G+B luminance for AWB white patch filtering. (R/W)

**Register 32.69. ISP\_AWB\_TH\_RG\_REG (0x0174)**

|            |  |  |  |  |  |                |  |  |  |  |  |            |  |  |  |  |  |                |  |  |  |  |  |       |
|------------|--|--|--|--|--|----------------|--|--|--|--|--|------------|--|--|--|--|--|----------------|--|--|--|--|--|-------|
| (reserved) |  |  |  |  |  | ISP_AWB_MAX_RG |  |  |  |  |  | (reserved) |  |  |  |  |  | ISP_AWB_MIN_RG |  |  |  |  |  |       |
| 312625     |  |  |  |  |  | 1615           |  |  |  |  |  | 109        |  |  |  |  |  | 0              |  |  |  |  |  |       |
| 000000     |  |  |  |  |  | 0x3ff          |  |  |  |  |  | 000000     |  |  |  |  |  | 0              |  |  |  |  |  | Reset |

Reset

**ISP\_AWB\_MIN\_RG** Configures the lower limit of R/G ratio for AWB white point filtering. Bits [9:8] are the integer part, and bits [7:0] are the fractional part. (R/W)

**ISP\_AWB\_MAX\_RG** Configures the upper limit of R/G ratio for AWB white point filtering. Bits [9:8] are the integer part, and bits [7:0] are the fractional part. (R/W)

**Register 32.70. ISP\_AWB\_TH\_BG\_REG (0x0178)**

|            |  |  |  |  |  |                |  |  |  |  |  |            |  |  |  |  |  |                |  |  |  |  |  |       |
|------------|--|--|--|--|--|----------------|--|--|--|--|--|------------|--|--|--|--|--|----------------|--|--|--|--|--|-------|
| (reserved) |  |  |  |  |  | ISP_AWB_MAX_BG |  |  |  |  |  | (reserved) |  |  |  |  |  | ISP_AWB_MIN_BG |  |  |  |  |  |       |
| 312625     |  |  |  |  |  | 1615           |  |  |  |  |  | 109        |  |  |  |  |  | 0              |  |  |  |  |  |       |
| 0000000    |  |  |  |  |  | 0x3ff          |  |  |  |  |  | 0000000    |  |  |  |  |  | 0              |  |  |  |  |  | Reset |

Reset

**ISP\_AWB\_MIN\_BG** Configures the lower limit of B/G ratio for AWB white point filtering. Bits [9:8] are the integer part, and bits [7:0] are the fractional part. (R/W)

**ISP\_AWB\_MAX\_BG** Configures the upper limit of B/G ratio for AWB white point filtering. Bits [9:8] are the integer part, and bits [7:0] are the fractional part. (R/W)

**Register 32.71. ISP\_COLOR\_CTRL\_REG (0x018C)**

|                                 |    |  |  |  |  |  |  |                               |    |  |  |  |  |  |  |                          |   |  |  |  |  |  |  |                                 |   |  |  |  |  |  |  |       |
|---------------------------------|----|--|--|--|--|--|--|-------------------------------|----|--|--|--|--|--|--|--------------------------|---|--|--|--|--|--|--|---------------------------------|---|--|--|--|--|--|--|-------|
| <div>ISP_COLOR_BRIGHTNESS</div> |    |  |  |  |  |  |  | <div>ISP_COLOR_CONTRAST</div> |    |  |  |  |  |  |  | <div>ISP_COLOR_HUE</div> |   |  |  |  |  |  |  | <div>ISP_COLOR_SATURATION</div> |   |  |  |  |  |  |  |       |
| 31                              | 24 |  |  |  |  |  |  | 23                            | 16 |  |  |  |  |  |  | 15                       | 8 |  |  |  |  |  |  | 7                               | 0 |  |  |  |  |  |  |       |
| 0x0                             |    |  |  |  |  |  |  | 0x80                          |    |  |  |  |  |  |  | 0x0                      |   |  |  |  |  |  |  | 0x80                            |   |  |  |  |  |  |  | Reset |

**ISP\_COLOR\_SATURATION** Configures the saturation. Bit [7] is the integer part, and bits [6:0] are the fractional part. (R/W)

**ISP\_COLOR\_HUE** Configures the hue, calculated as  $360 * (ISP\_COLOR\_HUE/256)$  degrees. (R/W)

**ISP\_COLOR\_CONTRAST** Configures the saturation. Bit [7] is the integer part, and bits [6:0] are the fractional part. (R/W)

**ISP\_COLOR\_BRIGHTNESS** Configures the brightness in two's complement. (R/W)

**Register 32.72. ISP\_HIST\_MODE\_REG (0x01A4)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_HIST_MODE |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3             | 2     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 4             | Reset |   |

**ISP\_HIST\_MODE** Configures the HIST sampling mode.

- 0: RAW\_B
  - 1: RAW\_GB
  - 2: RAW\_GR
  - 3: RAW\_R
  - 4: RGB
  - 5: YUV\_Y
  - 6: YUV\_U
  - 7: YUV\_V
- (R/W)

**Register 32.73. ISP\_HIST\_COEFF\_REG (0x01A8)**

|            |   |   |   |   |   |   |   |                  |    |  |  |  |  |  |  |                  |    |  |  |  |  |  |  |                  |   |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|------------------|----|--|--|--|--|--|--|------------------|----|--|--|--|--|--|--|------------------|---|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   | ISP_HIST_COEFF_R |    |  |  |  |  |  |  | ISP_HIST_COEFF_G |    |  |  |  |  |  |  | ISP_HIST_COEFF_B |   |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   | 24               | 23 |  |  |  |  |  |  | 16               | 15 |  |  |  |  |  |  | 8                | 7 |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 85               |    |  |  |  |  |  |  | 85               |    |  |  |  |  |  |  | 85               |   |  |  |  |  |  |  |   |

Reset

Reset

**ISP\_HIST\_COEFF\_B** Configures the B weight for RGB to brightness conversion when HIST statistics mode set to RGB. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_COEFF\_G** Configures the G weight for RGB to brightness conversion when HIST statistics mode set to RGB. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_COEFF\_R** Configures the R weight for RGB to brightness conversion when HIST statistics mode set to RGB. Bits [7:0] are the fractional part. (R/W)

**Register 32.74. ISP\_HIST\_OFFS\_REG (0x01AC)**

|            |   |   |   |                 |    |  |  |  |  |  |  |  |  |  |   |            |    |   |   |                 |    |    |  |  |  |  |  |  |       |  |  |  |   |
|------------|---|---|---|-----------------|----|--|--|--|--|--|--|--|--|--|---|------------|----|---|---|-----------------|----|----|--|--|--|--|--|--|-------|--|--|--|---|
| (reserved) |   |   |   | ISP_HIST_X_OFFS |    |  |  |  |  |  |  |  |  |  |   | (reserved) |    |   |   | ISP_HIST_Y_OFFS |    |    |  |  |  |  |  |  |       |  |  |  |   |
| 31         |   |   |   | 28              | 27 |  |  |  |  |  |  |  |  |  |   | 16         | 15 |   |   |                 | 12 | 11 |  |  |  |  |  |  |       |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0               | 0  |  |  |  |  |  |  |  |  |  | 0 | 0          | 0  | 0 | 0 |                 |    |    |  |  |  |  |  |  | Reset |  |  |  |   |

Reset

**ISP\_HIST\_Y\_OFFS** Configures the starting coordinate of the HIST statistics window in the vertical direction. (R/W)

**ISP\_HIST\_X\_OFFS** Configures the starting coordinate of the HIST statistics window in the horizontal direction. (R/W)

**Register 32.75. ISP\_HIST\_SIZE\_REG (0x01B0)**

|            |   |   |   |   |   |   |   |                 |    |  |  |  |  |  |  |            |    |   |   |   |   |   |   |                 |   |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|-----------------|----|--|--|--|--|--|--|------------|----|---|---|---|---|---|---|-----------------|---|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   | ISP_HIST_X_SIZE |    |  |  |  |  |  |  | (reserved) |    |   |   |   |   |   |   | ISP_HIST_Y_SIZE |   |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   | 25              | 24 |  |  |  |  |  |  | 16         | 15 |   |   |   |   |   |   | 9               | 8 |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 18              |    |  |  |  |  |  |  | 0          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 32              |   |  |  |  |  |  |  | Reset |

Reset

**ISP\_HIST\_Y\_SIZE** Configures the vertical dimension of the HIST sub-window. (R/W)

**ISP\_HIST\_X\_SIZE** Configures the horizontal dimension of the HIST sub-window. (R/W)

**Register 32.76. ISP\_HIST\_SEGO\_REG (0x01B4)**

|                  |    |    |    |    |   |    |   |  |  |    |  |  |  |       |  |
|------------------|----|----|----|----|---|----|---|--|--|----|--|--|--|-------|--|
| ISP_HIST_SEG_0_1 |    |    |    |    |   |    |   |  |  |    |  |  |  |       |  |
| ISP_HIST_SEG_1_2 |    |    |    |    |   |    |   |  |  |    |  |  |  |       |  |
| ISP_HIST_SEG_2_3 |    |    |    |    |   |    |   |  |  |    |  |  |  |       |  |
| ISP_HIST_SEG_3_4 |    |    |    |    |   |    |   |  |  |    |  |  |  |       |  |
| 31               | 24 | 23 | 16 | 15 | 8 | 7  | 0 |  |  |    |  |  |  |       |  |
| 16               |    | 32 |    |    |   | 48 |   |  |  | 64 |  |  |  | Reset |  |

**ISP\_HIST\_SEG\_3\_4** Configures the threshold between the HIST interval 3 and 4. (R/W)

**ISP\_HIST\_SEG\_2\_3** Configures the threshold between the HIST interval 2 and 3. (R/W)

**ISP\_HIST\_SEG\_1\_2** Configures the threshold between the HIST interval 1 and 2. (R/W)

**ISP\_HIST\_SEG\_0\_1** Configures the threshold between the HIST interval 0 and 1. (R/W)

**Register 32.77. ISP\_HIST\_SEG1\_REG (0x01B8)**

|                  |    |    |    |     |   |     |   |
|------------------|----|----|----|-----|---|-----|---|
| ISP_HIST_SEG_4_5 |    |    |    |     |   |     |   |
| ISP_HIST_SEG_5_6 |    |    |    |     |   |     |   |
| ISP_HIST_SEG_6_7 |    |    |    |     |   |     |   |
| ISP_HIST_SEG_7_8 |    |    |    |     |   |     |   |
| 31               | 24 | 23 | 16 | 15  | 8 | 7   | 0 |
| 80               |    | 96 |    | 112 |   | 128 |   |
| Reset            |    |    |    |     |   |     |   |

**ISP\_HIST\_SEG\_7\_8** Configures the threshold between the HIST interval 7 and 8. (R/W)

**ISP\_HIST\_SEG\_6\_7** Configures the threshold between the HIST interval 6 and 7. (R/W)

**ISP\_HIST\_SEG\_5\_6** Configures the threshold between the HIST interval 5 and 6. (R/W)

**ISP\_HIST\_SEG\_4\_5** Configures the threshold between the HIST interval 4 and 5. (R/W)

**Register 32.78. ISP\_HIST\_SEG2\_REG (0x01BC)**

|                    |    |     |    |     |   |     |   |
|--------------------|----|-----|----|-----|---|-----|---|
| ISP_HIST_SEG_8_9   |    |     |    |     |   |     |   |
| ISP_HIST_SEG_9_10  |    |     |    |     |   |     |   |
| ISP_HIST_SEG_10_11 |    |     |    |     |   |     |   |
| ISP_HIST_SEG_11_12 |    |     |    |     |   |     |   |
| 31                 | 24 | 23  | 16 | 15  | 8 | 7   | 0 |
| 144                |    | 160 |    | 176 |   | 192 |   |
| Reset              |    |     |    |     |   |     |   |

**ISP\_HIST\_SEG\_11\_12** Configures the threshold between the HIST interval 11 and 12. (R/W)

**ISP\_HIST\_SEG\_10\_11** Configures the threshold between the HIST interval 10 and 11. (R/W)

**ISP\_HIST\_SEG\_9\_10** Configures the threshold between the HIST interval 9 and 10. (R/W)

**ISP\_HIST\_SEG\_8\_9** Configures the threshold between the HIST interval 8 and 9. (R/W)



**Register 32.79. ISP\_HIST\_SEG3\_REG (0x01C0)**

|            |   |   |   |   |   |   |   |                    |    |  |  |  |  |  |  |                    |    |    |  |  |  |  |  |                    |  |   |   |  |  |  |  |       |  |  |   |
|------------|---|---|---|---|---|---|---|--------------------|----|--|--|--|--|--|--|--------------------|----|----|--|--|--|--|--|--------------------|--|---|---|--|--|--|--|-------|--|--|---|
| (reserved) |   |   |   |   |   |   |   | ISP_HIST_SEG_12_13 |    |  |  |  |  |  |  | ISP_HIST_SEG_13_14 |    |    |  |  |  |  |  | ISP_HIST_SEG_14_15 |  |   |   |  |  |  |  |       |  |  |   |
| 31         |   |   |   |   |   |   |   | 24                 | 23 |  |  |  |  |  |  |                    | 16 | 15 |  |  |  |  |  |                    |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 208                |    |  |  |  |  |  |  | 224                |    |    |  |  |  |  |  | 240                |  |   |   |  |  |  |  | Reset |  |  |   |

**ISP\_HIST\_SEG\_14\_15** Configures the threshold between the HIST interval 14 and 15. (R/W)

**ISP\_HIST\_SEG\_13\_14** Configures the threshold between the HIST interval 13 and 14. (R/W)

**ISP\_HIST\_SEG\_12\_13** Configures the threshold between the HIST interval 12 and 13. (R/W)

**Register 32.80. ISP\_HIST\_WEIGHT0\_REG (0x01C4)**

|                    |    |  |  |  |  |  |  |                    |    |  |  |  |  |  |  |                    |   |  |  |  |  |  |  |                    |   |  |  |  |  |  |  |       |
|--------------------|----|--|--|--|--|--|--|--------------------|----|--|--|--|--|--|--|--------------------|---|--|--|--|--|--|--|--------------------|---|--|--|--|--|--|--|-------|
| ISP_HIST_WEIGHT_00 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_01 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_02 |   |  |  |  |  |  |  | ISP_HIST_WEIGHT_03 |   |  |  |  |  |  |  |       |
| 31                 | 24 |  |  |  |  |  |  | 23                 | 16 |  |  |  |  |  |  | 15                 | 8 |  |  |  |  |  |  | 7                  | 0 |  |  |  |  |  |  |       |
| 1                  |    |  |  |  |  |  |  | 1                  |    |  |  |  |  |  |  | 1                  |   |  |  |  |  |  |  | 1                  |   |  |  |  |  |  |  | Reset |

**ISP\_HIST\_WEIGHT\_03** Configures the weight of HIST sub-window 03. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_02** Configures the weight of HIST sub-window 02. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_01** Configures the weight of HIST sub-window 01. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_00** Configures the weight of HIST sub-window 00. Bits [7:0] are the fractional part. (R/W)

**Register 32.81. ISP\_HIST\_WEIGHT1\_REG (0x01C8)**

|                    |  |  |  |  |  |  |  |                    |    |  |  |  |  |  |  |                    |    |    |  |  |  |  |  |                    |  |   |   |  |  |  |  |       |  |  |   |
|--------------------|--|--|--|--|--|--|--|--------------------|----|--|--|--|--|--|--|--------------------|----|----|--|--|--|--|--|--------------------|--|---|---|--|--|--|--|-------|--|--|---|
| ISP_HIST_WEIGHT_04 |  |  |  |  |  |  |  | ISP_HIST_WEIGHT_10 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_11 |    |    |  |  |  |  |  | ISP_HIST_WEIGHT_12 |  |   |   |  |  |  |  |       |  |  |   |
| 31                 |  |  |  |  |  |  |  | 24                 | 23 |  |  |  |  |  |  |                    | 16 | 15 |  |  |  |  |  |                    |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 1                  |  |  |  |  |  |  |  | 1                  |    |  |  |  |  |  |  | 1                  |    |    |  |  |  |  |  | 1                  |  |   |   |  |  |  |  | Reset |  |  |   |

**ISP\_HIST\_WEIGHT\_12** Configures the weight of HIST sub-window 12. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_11** Configures the weight of HIST sub-window 11. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_10** Configures the weight of HIST sub-window 10. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_04** Configures the weight of HIST sub-window 04. Bits [7:0] are the fractional part. (R/W)

**Register 32.82. ISP\_HIST\_WEIGHT2\_REG (0x01CC)**

|                    |  |  |  |  |  |  |  |                    |    |  |  |  |  |  |  |                    |    |    |  |  |  |  |  |                    |  |   |   |  |  |  |  |       |  |  |   |
|--------------------|--|--|--|--|--|--|--|--------------------|----|--|--|--|--|--|--|--------------------|----|----|--|--|--|--|--|--------------------|--|---|---|--|--|--|--|-------|--|--|---|
| ISP_HIST_WEIGHT_13 |  |  |  |  |  |  |  | ISP_HIST_WEIGHT_14 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_20 |    |    |  |  |  |  |  | ISP_HIST_WEIGHT_21 |  |   |   |  |  |  |  |       |  |  |   |
| 31                 |  |  |  |  |  |  |  | 24                 | 23 |  |  |  |  |  |  |                    | 16 | 15 |  |  |  |  |  |                    |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 1                  |  |  |  |  |  |  |  | 1                  |    |  |  |  |  |  |  | 1                  |    |    |  |  |  |  |  | 1                  |  |   |   |  |  |  |  | Reset |  |  |   |

**ISP\_HIST\_WEIGHT\_21** Configures the weight of HIST sub-window 21. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_20** Configures the weight of HIST sub-window 20. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_14** Configures the weight of HIST sub-window 14. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_13** Configures the weight of HIST sub-window 13. Bits [7:0] are the fractional part. (R/W)

**Register 32.83. ISP\_HIST\_WEIGHT3\_REG (0x01D0)**

|                    |    |  |  |  |  |  |  |                    |    |  |  |  |  |  |  |                    |   |  |  |  |  |  |  |                    |   |  |  |  |  |  |  |       |
|--------------------|----|--|--|--|--|--|--|--------------------|----|--|--|--|--|--|--|--------------------|---|--|--|--|--|--|--|--------------------|---|--|--|--|--|--|--|-------|
| ISP_HIST_WEIGHT_22 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_23 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_24 |   |  |  |  |  |  |  | ISP_HIST_WEIGHT_30 |   |  |  |  |  |  |  |       |
| 31                 | 24 |  |  |  |  |  |  | 23                 | 16 |  |  |  |  |  |  | 15                 | 8 |  |  |  |  |  |  | 7                  | 0 |  |  |  |  |  |  |       |
| 232                |    |  |  |  |  |  |  | 1                  |    |  |  |  |  |  |  | 1                  |   |  |  |  |  |  |  | 1                  |   |  |  |  |  |  |  | Reset |

**ISP\_HIST\_WEIGHT\_30** Configures the weight of HIST sub-window 30. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_24** Configures the weight of HIST sub-window 24. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_23** Configures the weight of HIST sub-window 23. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_22** Configures the weight of HIST sub-window 22. Bits [7:0] are the fractional part. (R/W)

**Register 32.84. ISP\_HIST\_WEIGHT4\_REG (0x01D4)**

|                    |  |  |  |  |  |  |  |                    |    |  |  |  |  |  |  |                    |    |    |  |  |  |  |  |                    |  |   |   |  |  |  |  |       |  |  |   |
|--------------------|--|--|--|--|--|--|--|--------------------|----|--|--|--|--|--|--|--------------------|----|----|--|--|--|--|--|--------------------|--|---|---|--|--|--|--|-------|--|--|---|
| ISP_HIST_WEIGHT_31 |  |  |  |  |  |  |  | ISP_HIST_WEIGHT_32 |    |  |  |  |  |  |  | ISP_HIST_WEIGHT_33 |    |    |  |  |  |  |  | ISP_HIST_WEIGHT_34 |  |   |   |  |  |  |  |       |  |  |   |
| 31                 |  |  |  |  |  |  |  | 24                 | 23 |  |  |  |  |  |  |                    | 16 | 15 |  |  |  |  |  |                    |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 1                  |  |  |  |  |  |  |  | 1                  |    |  |  |  |  |  |  | 1                  |    |    |  |  |  |  |  | 1                  |  |   |   |  |  |  |  | Reset |  |  |   |

**ISP\_HIST\_WEIGHT\_34** Configures the weight of HIST sub-window 34. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_33** Configures the weight of HIST sub-window 33. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_32** Configures the weight of HIST sub-window 32. Bits [7:0] are the fractional part. (R/W)

**ISP\_HIST\_WEIGHT\_31** Configures the weight of HIST sub-window 31. Bits [7:0] are the fractional part. (R/W)



**Register 32.87. ISP\_YUV\_FORMAT\_REG (0x0234)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_YUV_RANGE<br>ISP_YUV_MODE |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2                             | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | Reset |

**ISP\_YUV\_MODE** Configures the YUV output mode.

0: ITU-R BT.601

1: ITU-R BT.709

(R/W)

**ISP\_YUV\_RANGE** Configures the YUV output range.

0: Full range (YUV2RGB)

1: Limit range (YUV\_Limit)

(R/W)

**Register 32.88. ISP\_LUT\_RDATA\_REG (0x0050)**

|               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| ISP_LUT_RDATA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 0x000000      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| Reset         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**ISP\_LUT\_RDATA** Data read from the LUT. Read from this field after configuring [ISP\\_LUT\\_CMD](#). (RO)

**Register 32.89. ISP\_AE\_BLOCK\_MEAN\_O\_REG (0x00D8)**

|                 |  |  |  |    |  |  |  |                 |  |  |  |    |  |  |  |                 |  |  |  |   |  |  |  |                 |  |  |  |   |  |  |  |
|-----------------|--|--|--|----|--|--|--|-----------------|--|--|--|----|--|--|--|-----------------|--|--|--|---|--|--|--|-----------------|--|--|--|---|--|--|--|
| ISP_AE_B00_MEAN |  |  |  |    |  |  |  | ISP_AE_B01_MEAN |  |  |  |    |  |  |  | ISP_AE_B02_MEAN |  |  |  |   |  |  |  | ISP_AE_B03_MEAN |  |  |  |   |  |  |  |
| 31              |  |  |  | 24 |  |  |  | 23              |  |  |  | 16 |  |  |  | 15              |  |  |  | 8 |  |  |  | 7               |  |  |  | 0 |  |  |  |
| 0               |  |  |  | 0  |  |  |  | 0               |  |  |  | 0  |  |  |  | 0               |  |  |  | 0 |  |  |  | Reset           |  |  |  |   |  |  |  |

**ISP\_AE\_B03\_MEAN** Represents the statistics from AE sub-window 03. (RO)

**ISP\_AE\_B02\_MEAN** Represents the statistics from AE sub-window 02. (RO)

**ISP\_AE\_B01\_MEAN** Represents the statistics from AE sub-window 01. (RO)

**ISP\_AE\_B00\_MEAN** Represents the statistics from AE sub-window 00. (RO)

**Register 32.90. ISP\_AE\_BLOCK\_MEAN\_1\_REG (0x00DC)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_AE_B04_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B10_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B11_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B12_MEAN |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0               |    |    |    |    |   |   |   |

Reset

**ISP\_AE\_B12\_MEAN** Represents the statistics from AE sub-window 12. (RO)

**ISP\_AE\_B11\_MEAN** Represents the statistics from AE sub-window 11. (RO)

**ISP\_AE\_B10\_MEAN** Represents the statistics from AE sub-window 10. (RO)

**ISP\_AE\_B04\_MEAN** Represents the statistics from AE sub-window 04. (RO)

**Register 32.91. ISP\_AE\_BLOCK\_MEAN\_2\_REG (0x00E0)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_AE_B13_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B14_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B20_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B21_MEAN |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0               |    |    |    |    |   |   |   |

Reset

**ISP\_AE\_B21\_MEAN** Represents the statistics from AE sub-window 21. (RO)

**ISP\_AE\_B20\_MEAN** Represents the statistics from AE sub-window 20. (RO)

**ISP\_AE\_B14\_MEAN** Represents the statistics from AE sub-window 14. (RO)

**ISP\_AE\_B13\_MEAN** Represents the statistics from AE sub-window 13. (RO)

**Register 32.92. ISP\_AE\_BLOCK\_MEAN\_3\_REG (0x00E4)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_AE_B22_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B23_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B24_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B30_MEAN |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0               |    |    |    |    |   |   |   |

Reset

**ISP\_AE\_B30\_MEAN** Represents the statistics from AE sub-window 30. (RO)

**ISP\_AE\_B24\_MEAN** Represents the statistics from AE sub-window 24. (RO)

**ISP\_AE\_B23\_MEAN** Represents the statistics from AE sub-window 23. (RO)

**ISP\_AE\_B22\_MEAN** Represents the statistics from AE sub-window 22. (RO)

**Register 32.93. ISP\_AE\_BLOCK\_MEAN\_4\_REG (0x00E8)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_AE_B31_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B32_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B33_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B34_MEAN |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0               |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_AE\_B34\_MEAN** Represents the statistics from AE sub-window 34. (RO)

**ISP\_AE\_B33\_MEAN** Represents the statistics from AE sub-window 33. (RO)

**ISP\_AE\_B32\_MEAN** Represents the statistics from AE sub-window 32. (RO)

**ISP\_AE\_B31\_MEAN** Represents the statistics from AE sub-window 31. (RO)

**Register 32.94. ISP\_AE\_BLOCK\_MEAN\_5\_REG (0x00EC)**

|                 |    |    |    |    |   |   |   |
|-----------------|----|----|----|----|---|---|---|
| ISP_AE_B40_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B41_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B42_MEAN |    |    |    |    |   |   |   |
| ISP_AE_B43_MEAN |    |    |    |    |   |   |   |
| 31              | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
| 0               |    |    |    |    |   |   |   |
| Reset           |    |    |    |    |   |   |   |

**ISP\_AE\_B43\_MEAN** Represents the statistics from AE sub-window 43. (RO)

**ISP\_AE\_B42\_MEAN** Represents the statistics from AE sub-window 42. (RO)

**ISP\_AE\_B41\_MEAN** Represents the statistics from AE sub-window 41. (RO)

**ISP\_AE\_B40\_MEAN** Represents the statistics from AE sub-window 40. (RO)

**Register 32.95. ISP\_AE\_BLOCK\_MEAN\_6\_REG (0x00F0)**

|                 |    |    |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|-----------------|----|----|-------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ISP_AE_B44_MEAN |    |    |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| (reserved)      |    |    |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31              | 24 | 23 |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |
| 0               |    |    | 0     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|                 |    |    | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**ISP\_AE\_B44\_MEAN** Represents the statistics from AE sub-window 44. (RO)

**Register 32.96. ISP\_AF\_SUM\_A\_REG (0x014C)**

|            |    |             |   |
|------------|----|-------------|---|
| (reserved) |    | ISP_AF_SUMA |   |
| 31         | 30 | 29          | 0 |
| 0          | 0  | 0x000000    |   |

Reset

**ISP\_AF\_SUMA** Represents the sharpness statistics from AF window A. (RO)

**Register 32.97. ISP\_AF\_SUM\_B\_REG (0x0150)**

|            |    |             |   |
|------------|----|-------------|---|
| (reserved) |    | ISP_AF_SUMB |   |
| 31         | 30 | 29          | 0 |
| 0          | 0  | 0x000000    |   |

Reset

**ISP\_AF\_SUMB** Represents the sharpness statistics from AF window B. (RO)

**Register 32.98. ISP\_AF\_SUM\_C\_REG (0x0154)**

|            |    |             |   |
|------------|----|-------------|---|
| (reserved) |    | ISP_AF_SUMC |   |
| 31         | 30 | 29          | 0 |
| 0          | 0  | 0x000000    |   |

Reset

**ISP\_AF\_SUMC** Represents the sharpness statistics from AF window C. (RO)

**Register 32.99. ISP\_AF\_LUM\_A\_REG (0x0158)**

|            |    |             |   |
|------------|----|-------------|---|
| (reserved) |    | ISP_AF_LUMA |   |
| 31         | 28 | 27          | 0 |
| 0          | 0  | 0           | 0 |

Reset

**ISP\_AF\_LUMA** Represents the luminance statistics from AF window A. (RO)



**Register 32.100. ISP\_AF\_LUM\_B\_REG (0x015C)**

|            |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|----|--|--|--|----|--|--|--|---|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|---|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  | ISP_AF_LUMB |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  | 28 |  |  |  | 27 |  |  |  |   |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  | 0 |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  | 0  |  |  |  | 0  |  |  |  | 0 |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |   |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**ISP\_AF\_LUMB** Represents the luminance statistics from AF window B. (RO)

**Register 32.101. ISP\_AF\_LUM\_C\_REG (0x0160)**

|            |    |    |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | ISP_AF_LUMC |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0  | 0  | 0 | 0           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ISP\_AF\_LUMC** Represents the luminance statistics from AF window C. (RO)

**Register 32.102. ISP\_AWBO\_WHITE\_CNT\_REG (0x017C)**

|            |   |   |   |   |   |   |    |                    |   |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|----|--------------------|---|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |    | ISP_AWBO_WHITE_CNT |   |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   | 24 |                    |   |  |  |  |  |  |  |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  | Reset |

**ISP\_AWBO\_WHITE\_CNT** Represents the number of white patches within the AWB statistical window. (RO)

**Register 32.103. ISP\_AWBO\_ACC\_R\_REG (0x0180)**

|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| ISP_AWBO_ACC_R |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ISP\_AWBO\_ACC\_R** Represents the accumulated value of the R component for white patches within the AWB statistical window. (RO)

**Register 32.104. ISP\_AWBO\_ACC\_G\_REG (0x0184)**

|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |       |
|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|-------|
| ISP_AWBO_ACC_G |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 31 | 0     |
|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | Reset |

**ISP\_AWBO\_ACC\_G** Represents the accumulated value of the G component for white patches within the AWB statistical window. (RO)

**Register 32.105. ISP\_AWBO\_ACC\_B\_REG (0x0188)**

|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |       |
|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|-------|
| ISP_AWBO_ACC_B |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 31 | 0     |
|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | Reset |

**ISP\_AWBO\_ACC\_B** Represents the accumulated value of the B component for white patches within the AWB statistical window. (RO)

**Register 32.106. ISP\_HIST\_BIN0\_REG (0x01E0)**

|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |
|------------|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------|---|
| (reserved) |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_HIST_BIN_0 |   |
|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |
| 31         | 17 | 16 |   |   |   |   |   |   |   |   |   |   |   |   |   | 0              |   |
| 0          | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0 |
|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                | 0 |
| Reset      |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |

**ISP\_HIST\_BIN\_0** Represents the number of pixels where the luminance falls in the range of interval 0 in the HIST statistical window. (RO)

**Register 32.107. ISP\_HIST\_BIN1\_REG (0x01E4)**

|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |
|------------|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------|---|
| (reserved) |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_HIST_BIN_1 |   |
|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |
| 31         | 17 | 16 |   |   |   |   |   |   |   |   |   |   |   |   |   | 0              |   |
| 0          | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0 |
|            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                | 0 |
| Reset      |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |

**ISP\_HIST\_BIN\_1** Represents the number of pixels where the luminance falls in the range of interval 1 in the HIST statistical window. (RO)

**Register 32.108. ISP\_HIST\_BIN2\_REG (0x01E8)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_HIST_BIN_2 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17             | 16 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              |    |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ISP\_HIST\_BIN\_2** Represents the number of pixels where the luminance falls in the range of interval 2 in the HIST statistical window. (RO)

**Register 32.109. ISP\_HIST\_BIN3\_REG (0x01EC)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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**ISP\_HIST\_BIN\_3** Represents the number of pixels where the luminance falls in the range of interval 3 in the HIST statistical window. (RO)

**Register 32.110. ISP\_HIST\_BIN4\_REG (0x01F0)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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**ISP\_HIST\_BIN\_4** Represents the number of pixels where the luminance falls in the range of interval 4 in the HIST statistical window. (RO)

**Register 32.111. ISP\_HIST\_BIN5\_REG (0x01F4)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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**ISP\_HIST\_BIN\_5** Represents the number of pixels where the luminance falls in the range of interval 5 in the HIST statistical window. (RO)

**Register 32.112. ISP\_HIST\_BIN6\_REG (0x01F8)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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Reset

**ISP\_HIST\_BIN\_6** Represents the number of pixels where the luminance falls in the range of interval 6 in the HIST statistical window. (RO)

**Register 32.113. ISP\_HIST\_BIN7\_REG (0x01FC)**

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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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Reset

**ISP\_HIST\_BIN\_7** Represents the number of pixels where the luminance falls in the range of interval 7 in the HIST statistical window. (RO)

**Register 32.114. ISP\_HIST\_BIN8\_REG (0x0200)**

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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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Reset

**ISP\_HIST\_BIN\_8** Represents the number of pixels where the luminance falls in the range of interval 8 in the HIST statistical window. (RO)

**Register 32.115. ISP\_HIST\_BIN9\_REG (0x0204)**

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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**ISP\_HIST\_BIN\_9** Represents the number of pixels where the luminance falls in the range of interval 9 in the HIST statistical window. (RO)

**Register 32.116. ISP\_HIST\_BIN10\_REG (0x0208)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ISP_HIST_BIN_10 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 17                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**ISP\_HIST\_BIN\_10** Represents the number of pixels where the luminance falls in the range of interval 10 in the HIST statistical window. (RO)

**Register 32.117. ISP\_HIST\_BIN11\_REG (0x020C)**

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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**ISP\_HIST\_BIN\_11** Represents the number of pixels where the luminance falls in the range of interval 11 in the HIST statistical window. (RO)

**Register 32.118. ISP\_HIST\_BIN12\_REG (0x0210)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ISP_HIST_BIN_12 |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17              | 16    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

**ISP\_HIST\_BIN\_12** Represents the number of pixels where the luminance falls in the range of interval 12 in the HIST statistical window. (RO)

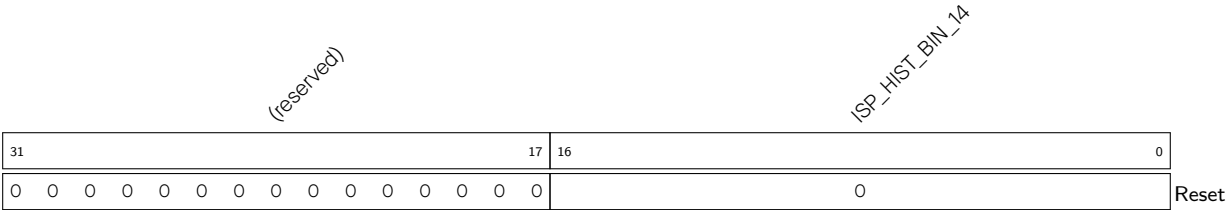
**Register 32.119. ISP\_HIST\_BIN13\_REG (0x0214)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

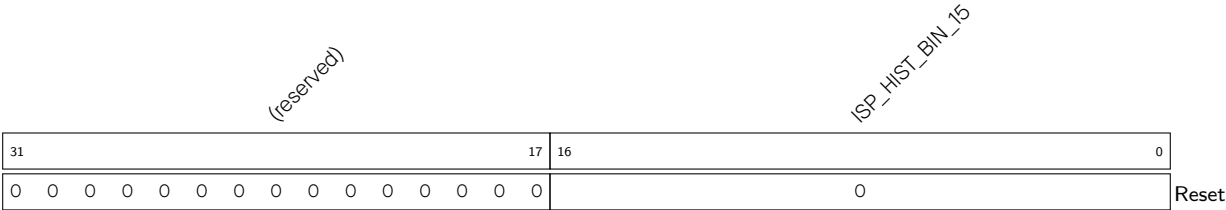
**ISP\_HIST\_BIN\_13** Represents the number of pixels where the luminance falls in the range of interval 13 in the HIST statistical window. (RO)

Register 32.120. ISP\_HIST\_BIN14\_REG (0x0218)



ISP\_HIST\_BIN\_14 Represents the number of pixels where the luminance falls in the range of interval 14 in the HIST statistical window. (RO)

Register 32.121. ISP\_HIST\_BIN15\_REG (0x021C)



ISP\_HIST\_BIN\_15 Represents the number of pixels where the luminance falls in the range of interval 15 in the HIST statistical window. (RO)

**Register 32.122. ISP\_INT\_RAW\_REG (0x0064)**

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>ISP_HEADER_IDI_FRAME_INT_RAW</div> <div>ISP_TAIL_IDI_FRAME_INT_RAW</div> <div>ISP_YUV2RGB_FRAME_INT_RAW</div> <div>ISP_COLOR_FRAME_INT_RAW</div> <div>ISP_SHARP_FRAME_INT_RAW</div> <div>ISP_RGB2YUV_FRAME_INT_RAW</div> <div>ISP_GAMMA_FRAME_INT_RAW</div> <div>ISP_CCM_FRAME_INT_RAW</div> <div>(reserved)</div> <div>ISP_DEMOSAIC_FRAME_INT_RAW</div> <div>ISP_BF_FRAME_INT_RAW</div> <div>ISP_LSC_FRAME_INT_RAW</div> <div>(reserved)</div> <div>ISP_FRAME_INT_RAW</div> <div>ISP_HIST_FDONE_INT_RAW</div> <div>ISP_AWB_FDONE_INT_RAW</div> <div>ISP_AF_ENV_INT_RAW</div> <div>ISP_AF_FDONE_INT_RAW</div> <div>ISP_AE_FRAME_DONE_INT_RAW</div> <div>ISP_AE_MONITOR_INT_RAW</div> <div>(reserved)</div> <div>ISP_MIPI_HNUM_UNMATCH_INT_RAW</div> <div>ISP_DATA_TYPE_SETTING_ERR_INT_RAW</div> <div>ISP_HVNUM_SETTING_ERR_INT_RAW</div> <div>ISP_BUF_FULL_INT_RAW</div> <div>ISP_ASYNC_FIFO_OVF_INT_RAW</div> <div>ISP_DATA_TYPE_ERR_INT_RAW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**ISP\_DATA\_TYPE\_ERR\_INT\_RAW** The raw interrupt status of ISP\_DATA\_TYPE\_ERR\_INT. (R/SS/WTC)

**ISP\_ASYNC\_FIFO\_OVF\_INT\_RAW** The raw interrupt status of ISP\_ASYNC\_FIFO\_OVF\_INT. (R/SS/WTC)

**ISP\_BUF\_FULL\_INT\_RAW** The raw interrupt status of ISP\_BUF\_FULL\_INT. (R/SS/WTC)

**ISP\_HVNUM\_SETTING\_ERR\_INT\_RAW** The raw interrupt status of ISP\_HVNUM\_SETTING\_ERR\_INT. (R/SS/WTC)

**ISP\_DATA\_TYPE\_SETTING\_ERR\_INT\_RAW** The raw interrupt status of ISP\_DATA\_TYPE\_SETTING\_ERR\_INT. (R/SS/WTC)

**ISP\_MIPI\_HNUM\_UNMATCH\_INT\_RAW** The raw interrupt status of ISP\_MIPI\_HNUM\_UNMATCH\_INT. (R/SS/WTC)

**ISP\_AE\_MONITOR\_INT\_RAW** The raw interrupt status of ISP\_AE\_MONITOR\_INT. (R/SS/WTC)

**ISP\_AE\_FRAME\_DONE\_INT\_RAW** The raw interrupt status of ISP\_AE\_FRAME\_DONE\_INT. (R/SS/WTC)

**ISP\_AF\_FDONE\_INT\_RAW** The raw interrupt status of ISP\_AF\_FDONE\_INT. (R/SS/WTC)

**ISP\_AF\_ENV\_INT\_RAW** The raw interrupt status of ISP\_AF\_ENV\_INT. (R/SS/WTC)

**ISP\_AWB\_FDONE\_INT\_RAW** The raw interrupt status of ISP\_AWB\_FDONE\_INT. (R/SS/WTC)

**ISP\_HIST\_FDONE\_INT\_RAW** The raw interrupt status of ISP\_HIST\_FDONE\_INT. (R/SS/WTC)

**ISP\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_FRAME\_INT. (R/SS/WTC)

**ISP\_LSC\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_LSC\_FRAME\_INT. (R/SS/WTC)

**ISP\_BF\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_BF\_FRAME\_INT. (R/SS/WTC)

**ISP\_DEMOSAIC\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_DEMOSAIC\_FRAME\_INT. (R/SS/WTC)

**ISP\_CCM\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_CCM\_FRAME\_INT. (R/SS/WTC)

Continued on the next page...

**Register 32.122. ISP\_INT\_RAW\_REG (0x0064)**

Continued from the previous page...

**ISP\_GAMMA\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_GAMMA\_FRAME\_INT. (R/SS/WTC)

**ISP\_RGB2YUV\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_RGB2YUV\_FRAME\_INT.  
(R/SS/WTC)

**ISP\_SHARP\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_SHARP\_FRAME\_INT. (R/SS/WTC)

**ISP\_COLOR\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_COLOR\_FRAME\_INT. (R/SS/WTC)

**ISP\_YUV2RGB\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_YUV2RGB\_FRAME\_INT.  
(R/SS/WTC)

**ISP\_TAIL\_IDI\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_TAIL\_IDI\_FRAME\_INT. (R/SS/WTC)

**ISP\_HEADER\_IDI\_FRAME\_INT\_RAW** The raw interrupt status of ISP\_HEADER\_IDI\_FRAME\_INT.  
(R/SS/WTC)



**Register 32.123. ISP\_INT\_ST\_REG (0x0068)**

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>ISP_HEADER_IDI_FRAME_INT_ST</div> <div>ISP_TAIL_IDI_FRAME_INT_ST</div> <div>ISP_YUV2RGB_FRAME_INT_ST</div> <div>ISP_COLOR_FRAME_INT_ST</div> <div>ISP_SHARP_FRAME_INT_ST</div> <div>ISP_RGB2YUV_FRAME_INT_ST</div> <div>ISP_GAMMA_FRAME_INT_ST</div> <div>ISP_CCM_FRAME_INT_ST</div> <div>(reserved)</div> <div>ISP_DEMOSAIC_FRAME_INT_ST</div> <div>ISP_BF_FRAME_INT_ST</div> <div>ISP_LSC_FRAME_INT_ST</div> <div>(reserved)</div> <div>ISP_FRAME_INT_ST</div> <div>ISP_HIST_FDONE_INT_ST</div> <div>ISP_AWB_FDONE_INT_ST</div> <div>ISP_AF_ENV_INT_ST</div> <div>ISP_AF_FDONE_INT_ST</div> <div>ISP_AE_FRAME_DONE_INT_ST</div> <div>ISP_AE_MONITOR_INT_ST</div> <div>(reserved)</div> <div>ISP_MIPI_HNUM_UNMATCH_INT_ST</div> <div>ISP_DATA_TYPE_SETTING_ERR_INT_ST</div> <div>ISP_HVNUM_SETTING_ERR_INT_ST</div> <div>ISP_BUF_FULL_INT_ST</div> <div>ISP_ASYNC_FIFO_OVF_INT_ST</div> <div>ISP_DATA_TYPE_ERR_INT_ST</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**ISP\_DATA\_TYPE\_ERR\_INT\_ST** The masked interrupt status of ISP\_DATA\_TYPE\_ERR\_INT. (RO)

**ISP\_ASYNC\_FIFO\_OVF\_INT\_ST** The masked interrupt status of ISP\_ASYNC\_FIFO\_OVF\_INT. (RO)

**ISP\_BUF\_FULL\_INT\_ST** The masked interrupt status of ISP\_BUF\_FULL\_INT. (RO)

**ISP\_HVNUM\_SETTING\_ERR\_INT\_ST** The masked interrupt status of ISP\_HVNUM\_SETTING\_ERR\_INT. (RO)

**ISP\_DATA\_TYPE\_SETTING\_ERR\_INT\_ST** The masked interrupt status of ISP\_DATA\_TYPE\_SETTING\_ERR\_INT. (RO)

**ISP\_MIPI\_HNUM\_UNMATCH\_INT\_ST** The masked interrupt status of ISP\_MIPI\_HNUM\_UNMATCH\_INT. (RO)

**ISP\_AE\_MONITOR\_INT\_ST** The masked interrupt status of ISP\_AE\_MONITOR\_INT. (RO)

**ISP\_AE\_FRAME\_DONE\_INT\_ST** The masked interrupt status of ISP\_AE\_FRAME\_DONE\_INT. (RO)

**ISP\_AF\_FDONE\_INT\_ST** The masked interrupt status of ISP\_AF\_FDONE\_INT. (RO)

**ISP\_AF\_ENV\_INT\_ST** The masked interrupt status of ISP\_AF\_ENV\_INT. (RO)

**ISP\_AWB\_FDONE\_INT\_ST** The masked interrupt status of ISP\_AWB\_FDONE\_INT. (RO)

**ISP\_HIST\_FDONE\_INT\_ST** The masked interrupt status of ISP\_HIST\_FDONE\_INT. (RO)

**ISP\_FRAME\_INT\_ST** The masked interrupt status of ISP\_FRAME\_INT. (RO)

**ISP\_LSC\_FRAME\_INT\_ST** The masked interrupt status of ISP\_LSC\_FRAME\_INT. (RO)

**ISP\_BF\_FRAME\_INT\_ST** The masked interrupt status of ISP\_BF\_FRAME\_INT. (RO)

**ISP\_DEMOSAIC\_FRAME\_INT\_ST** The masked interrupt status of ISP\_DEMOSAIC\_FRAME\_INT. (RO)

**ISP\_CCM\_FRAME\_INT\_ST** The masked interrupt status of ISP\_CCM\_FRAME\_INT. (RO)

**ISP\_GAMMA\_FRAME\_INT\_ST** The masked interrupt status of ISP\_GAMMA\_FRAME\_INT. (RO)

**ISP\_RGB2YUV\_FRAME\_INT\_ST** The masked interrupt status of ISP\_RGB2YUV\_FRAME\_INT. (RO)

Continued on the next page...

**Register 32.123. ISP\_INT\_RAW\_REG (0x0064)**

Continued from the previous page...

**ISP\_SHARP\_FRAME\_INT\_ST** The masked interrupt status of ISP\_SHARP\_FRAME\_INT. (RO)

**ISP\_COLOR\_FRAME\_INT\_ST** The raw interrupt status of ISP\_COLOR\_FRAME\_INT. (RO)

**ISP\_YUV2RGB\_FRAME\_INT\_ST** The masked interrupt status of ISP\_YUV2RGB\_FRAME\_INT. (RO)

**ISP\_TAIL\_IDI\_FRAME\_INT\_ST** The masked interrupt status of ISP\_TAIL\_IDI\_FRAME\_INT. (RO)

**ISP\_HEADER\_IDI\_FRAME\_INT\_ST** The masked interrupt status of ISP\_HEADER\_IDI\_FRAME\_INT.  
(RO)

### Register 32.124. ISP\_INT\_ENA\_REG (0x006C)

[illegible]

**ISP\_DATA\_TYPE\_ERR\_INT\_ENA** Write 1 to enable ISP\_DATA\_TYPE\_ERR\_INT. (R/W)

**ISP\_ASYNC\_FIFO\_OVF\_INT\_ENA** Write 1 to enable ISP\_ASYNC\_FIFO\_OVF\_INT. (R/W)

**ISP\_BUF\_FULL\_INT\_ENA** Write 1 to enable ISP\_BUF\_FULL\_INT. (R/W)

**ISP\_HVNUM\_SETTING\_ERR\_INT\_ENA** Write 1 to enable ISP\_HVNUM\_SETTING\_ERR\_INT. (R/W)

ISP\_DATA\_TYPE\_SETTING\_ERR\_INT\_ENA Write 1 to enable ISP\_DATA\_TYPE\_SETTING\_ERR\_INT.  
(R/W)

**ISP\_MIPI\_HNUM\_UNMATCH\_INT\_ENA** Write 1 to enable ISP\_MIPI\_HNUM\_UNMATCH\_INT. (R/W)

**ISP\_AE\_MONITOR\_INT\_ENA** Write 1 to enable ISP\_AE\_MONITOR\_INT. (R/W)

**ISP\_AE\_FRAME\_DONE\_INT\_ENA** Write 1 to enable ISP\_AE\_FRAME\_DONE\_INT. (R/W)

**ISP\_AF\_FDONE\_INT\_ENA** Write 1 to enable ISP\_AF\_FDONE\_INT. (R/W)

**ISP\_AF\_ENV\_INT\_ENA** Write 1 to enable ISP\_AF\_ENV\_INT. (R/W)

**ISP\_AWB\_FDONE\_INT\_ENA** Write 1 to enable ISP\_AWB\_FDONE\_INT. (R/W)

**ISP\_HIST\_FDONE\_INT\_ENA** Write 1 to enable ISP\_HIST\_FDONE\_INT. (R/W)

**ISP\_FRAME\_INT\_ENA** Write 1 to enable ISP\_FRAME\_INT. (R/W)

**ISP\_LSC\_FRAME\_INT\_ENA** Write 1 to enable ISP\_LSC\_FRAME\_INT. (R/W)

**ISP\_BF\_FRAME\_INT\_ENA** Write 1 to enable ISP\_BF\_FRAME\_INT. (R/W)

**ISP\_DEMOSAIC\_FRAME\_INT\_ENA** Write 1 to enable ISP\_DEMOSAIC\_FRAME\_INT. (R/W)

**ISP\_CCM\_FRAME\_INT\_ENA** Write 1 to enable ISP\_CCM\_FRAME\_INT. (R/W)

**ISP\_GAMMA\_FRAME\_INT\_ENA** Write 1 to enable ISP\_GAMMA\_FRAME\_INT. (R/W)

**ISP\_RGB2YUV\_FRAME\_INT\_ENA** Write 1 to enable ISP\_RGB2YUV\_FRAME\_INT. (R/W)

**ISP SHARP FRAME INT ENA** Write 1 to enable ISP SHARP FRAME INT. (R/W)

Continued on the next page...

**Register 32.124. ISP\_INT\_RAW\_REG (0x0064)**

Continued from the previous page...

**ISP\_COLOR\_FRAME\_INT\_ENA** Write 1 to enable ISP\_COLOR\_FRAME\_INT. (R/W)

**ISP\_YUV2RGB\_FRAME\_INT\_ENA** Write 1 to enable ISP\_YUV2RGB\_FRAME\_INT. (R/W)

**ISP\_TAIL\_IDI\_FRAME\_INT\_ENA** Write 1 to enable ISP\_TAIL\_IDI\_FRAME\_INT. (R/W)

**ISP\_HEADER\_IDI\_FRAME\_INT\_ENA** Write 1 to enable ISP\_HEADER\_IDI\_FRAME\_INT. (R/W)

### Register 32.125. ISP\_INT\_CLR\_REG (0x0070)

[illegible]

**ISP\_DATA\_TYPE\_ERR\_INT\_CLR** Write 1 to clear ISP\_DATA\_TYPE\_ERR\_INT. (WT)

**ISP\_ASYNC\_FIFO\_OVF\_INT\_CLR** Write 1 to clear ISP\_ASYNC\_FIFO\_OVF\_INT. (WT)

**ISP\_BUF\_FULL\_INT\_CLR** Write 1 to clear ISP\_BUF\_FULL\_INT. (WT)

**ISP\_HVNUM\_SETTING\_ERR\_INT\_CLR** Write 1 to clear ISP\_HVNUM\_SETTING\_ERR\_INT. (WT)

**ISP\_DATA\_TYPE\_SETTING\_ERR\_INT\_CLR** Write 1 to clear ISP\_DATA\_TYPE\_SETTING\_ERR\_INT. (WT)

**ISP\_MIPI\_HNUM\_UNMATCH\_INT\_CLR** Write 1 to clear ISP\_MIPI\_HNUM\_UNMATCH\_INT. (WT)

**ISP\_AE\_MONITOR\_INT\_CLR** Write 1 to clear ISP\_AE\_MONITOR\_INT. (WT)

**ISP AE FRAME DONE INT CLR** Write 1 to clear ISP AE FRAME DONE INT. (WT)

**ISP\_AF\_FDONE\_INT\_CLR** Write 1 to clear ISP\_AF\_FDONE\_INT. (WT)

**ISP\_AF\_ENV\_INT\_CLR** Write 1 to clear ISP\_AF\_ENV\_INT. (WT)

ISP AWB FDONE INT CLR Write 1 to clear ISP AWB FDONE INT. (WT)

**ISP\_HIST\_FDONE\_INT\_CLR** Write 1 to clear ISP\_HIST\_FDONE\_INT. (WT)

**ISP\_FRAME\_INT\_CLR** Write 1 to clear ISP\_FRAME\_INT. (WT)

**ISP\_LSC\_FRAME\_INT\_CLR** Write 1 to clear ISP\_LSC\_FRAME\_INT. (WT)

**ISP BF FRAME INT CLR** Write 1 to clear ISP BF FRAME INT. (WT)

**ISP\_DEMOSAIC\_FRAME\_INT\_CLR** Write 1 to clear ISP\_DEMOSAIC\_FRAME\_INT. (WT)

**ISP\_CCM\_FRAME\_INT\_CLR** Write 1 to clear ISP\_CCM\_FRAME\_INT. (WT)

**ISP\_GAMMA\_FRAME\_INT\_CLR** Write 1 to clear ISP\_GAMMA\_FRAME\_INT. (WT)

**ISP\_RGB2YUV\_FRAME\_INT\_CLR** Write 1 to clear ISP\_RGB2YUV\_FRAME\_INT. (WT)

**ISP SHARP FRAME INT CLR** Write 1 to clear ISP SHARP FRAME INT. (WT)

**ISP\_COLOR\_FRAME\_INT\_CLR** Write 1 to clear ISP\_COLOR\_FRAME\_INT. (WT)

Continued on the next page...

**Register 32.125. ISP\_INT\_CLR\_REG (0x0070)**

Continued from the previous page...

**ISP\_YUV2RGB\_FRAME\_INT\_CLR** Write 1 to clear ISP\_YUV2RGB\_FRAME\_INT. (WT)**ISP\_TAIL\_IDI\_FRAME\_INT\_CLR** Write 1 to clear ISP\_TAIL\_IDI\_FRAME\_INT. (WT)**ISP\_HEADER\_IDI\_FRAME\_INT\_CLR** Write 1 to clear ISP\_HEADER\_IDI\_FRAME\_INT. (WT)**32.9.2 MIPI CSI\_Bridge Registers**

The addresses in this section are relative to **MIPI CSI\_Bridge** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 32.126. CSI\_BRIG\_CLK\_EN\_REG (0x0000)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_CLK_EN |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1               | 0 |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               | 0 | 0 | 0 | Reset |

**CSI\_BRIG\_CLK\_EN** Configures whether the CSI\_Bridge clock is always on.

0: The clock is on only during register access

1: The clock is always on

(R/W)

**Register 32.127. CSI\_BRIG\_CSI\_EN\_REG (0x0004)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_CSI_BRIG_EN |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                    | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | Reset |

**CSI\_BRIG\_CSI\_BRIG\_EN** Configures whether to enable CSI\_Bridge.

0: Disable

1: Enable

(R/W)

### Register 32.128. CSI\_BRIG\_BUF\_FLOW\_CTL\_REG (0x000C)

|            |    |                        |    |            |    |                             |       |
|------------|----|------------------------|----|------------|----|-----------------------------|-------|
| (reserved) |    | CSI_BRIG_CSI_BUF_DEPTH |    | (reserved) |    | CSI_BRIG_CSI_BUF_AFULL_THRD |       |
| 31         | 30 | 29                     | 16 | 15         | 14 | 13                          | 0     |
| 0          | 0  | 0                      | 0  | 0          | 0  | 2040                        | Reset |

|                                    |   |
|------------------------------------|---|
| <b>CSI_BRIG_CSI_BUF_AFULL_THRD</b> | Configures the size threshold at which the CSI_Bridge buffer is about to be full. (R/W) |
|------------------------------------|---|

**CSI\_BRIG\_CSI\_BUF\_DEPTH** Represents the size of the CSI\_Bridge buffer in use. (RO)

### Register 32.129. CSI\_BRIG\_DMA\_REQ\_CFG\_REG (0x0008)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_BRIG_DMA_CFG_UPD_BY_BLK |  | CSI_BRIG_DMA_BURST_LEN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12                          |  | 0                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                           |  | 128                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |

**CSI\_BRIG\_DMA\_BURST\_LEN** Configures the amount of 64-bit data in a VDMA burst transfer. (R/W)

**CSI\_BRIG\_DMA\_CFG\_UPD\_BY\_BLK** Configures **CSI\_BRIG\_DMA\_CFG\_UPD\_BY\_BLK** when **CSI\_BRIG\_DMA\_BURST\_LEN** and **CSI\_BRIG\_DMABLK\_SIZE** are updated.

0: Update upon completion of each VDMA block transfer

1: Update at the end of each frame transfer

(R/W)

**Register 32.130. CSI\_BRIG\_DMA\_REQ\_INTERVAL\_REG (0x002C)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_BRIG_DMA_REQ_INTERVAL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x01                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**CSI\_BRIG\_DMA\_REQ\_INTERVAL** Configures the interval of VDMA requests. 16'b1: 1 clock cycle, 16'b11: 2 clock cycles, 16'hFFFF: 16 clock cycles, etc. (R/W)

**Register 32.131. CSI\_BRIG\_DMABLK\_SIZE\_REG (0x0030)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**CSI\_BRIG\_DMABLK\_SIZE** Configures the number of VDMA bursts in a VDMA block transfer. (R/W)

**Register 32.132. CSI\_BRIG\_DATA\_TYPE\_CFG\_REG (0x0010)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |            |  |  |  |                        |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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|  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**CSI\_BRIG\_DATA\_TYPE\_MIN** Configures the minimum value of DATA\_TYPE for valid pixels. (R/W)

**CSI\_BRIG\_DATA\_TYPE\_MAX** Configures the maximum value of DATA\_TYPE for valid pixels. (R/W)



### Register 32.133. CSI\_BRIG\_FRAME\_CFG\_REG (0x0014)

|            |   |   |   |   |   |   |    |    |     |  |  |  |  |  |  |  |  |  |  |     |    |                   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |   |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|----|----|-----|--|--|--|--|--|--|--|--|--|--|-----|----|-------------------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|---|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   | CSI_BRIG_VADR_NUM_CHECK<br>CSI_BRIG_HAS_HSYNC_E |    |    |     |  |  |  |  |  |  |  |  |  |  |     |    | CSI_BRIG_HADR_NUM |  |  |  |  |  |  |  |  |  |  |  |       |  |  |   | CSI_BRIG_VADR_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   | 26  | 25 | 24 | 23  |  |  |  |  |  |  |  |  |  |  |     | 12 | 11                |  |  |  |  |  |  |  |  |  |  |  |       |  |  | 0 |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 1  | 480 |  |  |  |  |  |  |  |  |  |  | 480 |    |                   |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |   |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**CSI\_BRIG\_VADR\_NUM** Configures the height of an image frame. Measurement unit: line. (R/W)

**CSI\_BRIG\_HADR\_NUM** Configures the amount of 64-bit data in the width of an image frame. (R/W)

**CSI\_BRIG\_HAS\_HSYNC\_E** Configures whether the Image Interface 64 input includes HSYNC\_START and HSYNC\_END packets.

0: Not included

1: Included

(R/W)

**CSI\_BRIG\_VADR\_NUM\_CHECK** Configures whether to enable line number checking.

0: Disable

1: Enable

(R/W)

### Register 32.134. CSI\_BRIG\_ENDIAN\_MODE\_REG (0x0018)

[illegible]

**CSI\_BRIG\_BYTE\_ENDIAN\_ORDER** Configures the byte order of 64-bit data.

0: Byte order remains unchanged

1: Reverse the high and low bytes

(R/W)

### Register 32.135. CSI\_BRIG\_INT\_RAW\_REG (0x001C)

Register 0x00000000: CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT\_RAW

31 (reserved) 6 5 4 3 2 1 0

CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT\_RAW  
CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT\_RAW  
CSI\_BRIG\_DISCARD\_INT\_RAW  
CSI\_BRIG\_VADR\_NUM\_LT\_INT\_RAW  
CSI\_BRIG\_VADR\_NUM\_GT\_INT\_RAW  
Reset

**CSI\_BRIG\_VADR\_NUM\_GT\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_VADR\_NUM\_GT\_INT.  
(R/WTC/SS)

**CSI\_BRIG\_VADR\_NUM\_LT\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_VADR\_NUM\_LT\_INT.  
(R/WTC/SS)

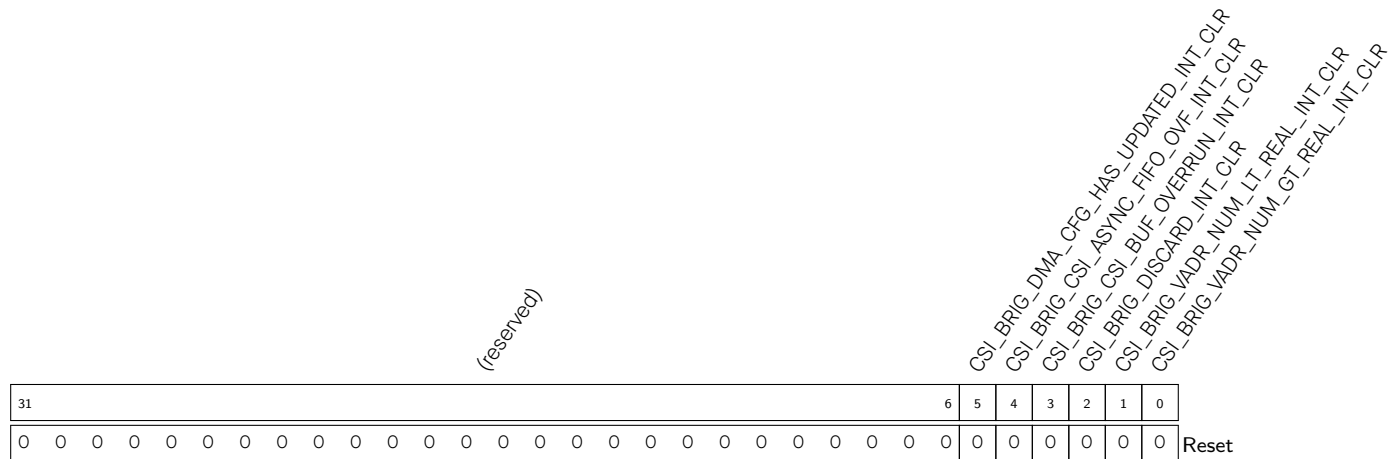
**CSI\_BRIG\_DISCARD\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_DISCARD\_INT. (R/WTC/SS)

**CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT. (R/WTC/SS)

**CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT. (R/WTC/SS)

**CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT\_RAW** The raw interrupt status of CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT. (R/WTC/SS)

### Register 32.136. CSI\_BRIG\_INT\_CLR\_REG (0x0020)



**CSI\_BRIG\_VADR\_NUM\_GT\_REAL\_INT\_CLR** Write 1 to clear CSI\_BRIG\_VADR\_NUM\_GT\_REAL\_INT.  
(WT)

**CSI\_BRIG\_VADR\_NUM\_LT\_REAL\_INT\_CLR** Write 1 to clear CSI\_BRIG\_VADR\_NUM\_LT\_REAL\_INT.  
(WT)

**CSI\_BRIG\_DISCARD\_INT\_CLR** Write 1 to clear CSI\_BRIG\_DISCARD\_INT. (WT)

**CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT\_CLR** Write 1 to clear CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT. (WT)

**CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT\_CLR** Write 1 to clear CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT.  
(WT)

**CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT\_CLR** Write 1 to clear CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT.  
(WT)

### Register 32.137. CSI\_BRIG\_INT\_ST\_REG (0x0024)

Diagram of the 32-bit CS1 register structure:

- Bits 31 to 6: (reserved)
- Bit 5: CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT\_ST
- Bit 4: CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT\_ST
- Bit 3: CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT\_ST
- Bit 2: CSI\_BRIG\_DISCARD\_INT\_ST
- Bit 1: CSI\_BRIG\_VADR\_NUM\_LT\_INT\_ST
- Bit 0: CSI\_BRIG\_VADR\_NUM\_GT\_INT\_ST

**CSI\_BRIG\_VADR\_NUM\_GT\_INT\_ST** The masked interrupt status of CSI\_BRIG\_VADR\_NUM\_GT\_INT.  
(RO)

|                                    |  |
|------------------------------------|--|
| <b>CSI_BRIG_VADR_NUM_LT_INT_ST</b> | The masked interrupt status of CSI_BRIG_VADR_NUM_LT_INT. |
| (RO)                               |  |

**CSI\_BRIG\_DISCARD\_INT\_ST** The masked interrupt status of CSI\_BRIG\_DISCARD\_INT. (RO)

|  |   |
|--|---|
| <b>CSI_BRIG_CSI_BUF_OVERRUN_INT_ST</b> | The masked interrupt status of CSI_BRIG_CSI_BUF_OVERRUN_INT. (RO) |
|--|---|

|   |  |
|---|--|
| <b>CSI_BRIG_CSI_ASYNC_FIFO_OVF_INT_ST</b> | The masked interrupt status of CSI_BRIG_CSI_ASYNC_FIFO_OVF_INT. (RO) |
|---|--|

|                                     |   |
|-------------------------------------|---|
| CSI_BRIG_DMA_CFG_HAS_UPDATED_INT_ST | The masked interrupt status of CSI_BRIG_DMA_CFG_HAS_UPDATED_INT. (RO) |
|-------------------------------------|---|

## Register 32.138. CSI\_BRIG\_INT\_ENA\_REG (0x0028)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------------|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_DMA_CFG_HAS_UPDATED_INT_ENA |   |       |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_CSI_ASYNC_FIFO_OVF_INT_ENA  |   |       |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_CSI_BUF_OVERRUN_INT_ENA     |   |       |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_DISCARD_INT_ENA             |   |       |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_VADR_NUM_LT_INT_ENA         |   |       |   |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_VADR_NUM_GT_INT_ENA         |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5 | 4 | 3 | 2 | 1                                    | 0 | Reset |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0     | 0 |

**CSI\_BRIG\_VADR\_NUM\_GT\_INT\_ENA** Write 1 to enable CSI\_BRIG\_VADR\_NUM\_GT\_INT. (R/W)

**CSI\_BRIG\_VADR\_NUM\_LT\_INT\_ENA** Write 1 to enable CSI\_BRIG\_VADR\_NUM\_LT\_INT. (R/W)

**CSI\_BRIG\_DISCARD\_INT\_ENA** Write 1 to enable CSI\_BRIG\_DISCARD\_INT. (R/W)

**CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT\_ENA** Write 1 to enable CSI\_BRIG\_CSI\_BUF\_OVERRUN\_INT. (R/W)

**CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT\_ENA** Write 1 to enable CSI\_BRIG\_CSI\_ASYNC\_FIFO\_OVF\_INT. (R/W)

**CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT\_ENA** Write 1 to enable CSI\_BRIG\_DMA\_CFG\_HAS\_UPDATED\_INT. (R/W)

## Register 32.139. CSI\_BRIG\_HOST\_CTRL\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_BRIG_CSI_ENABLECLK |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                      | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1                      | Reset |

**CSI\_BRIG\_CSI\_ENABLECLK** Configures whether to enable the clock lane of CSI PHY.

0: Disable

1: Enable

(R/W)

## Chapter 33

### Pixel-Processing Accelerator (PPA)

#### 33.1 Overview

ESP32-P4 includes a pixel-processing accelerator (PPA) designed for 2D image display. This module realizes hardware-level acceleration of image algorithms and implements functions such as image rotation, scaling, mirroring, and blending.

PPA consists of two functional modules: scaling-rotation-mirroring (SRM) and image blending (BLEND). The SRM module implements image rotation, scaling, and XY-axis mirroring functions, while the BLEND module achieves the blending of two layers of the same size based on the Alpha channel, i.e., transparency.

PPA processes images in units of pixel block. These pixel blocks are acquired from memory through 2D-DMA. The connection between PPA and 2D-DMA is shown in Figure 33.1-1.

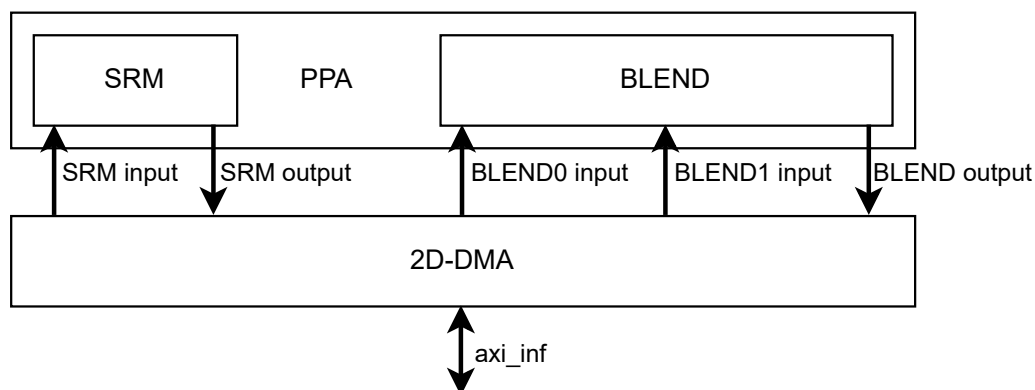


Figure 33.1-1. PPA 2D-DMA Connection

#### 33.2 Terminology

To better illustrate the functions of the PPA module, the following terms are used in this chapter:

- image** A complete image stored in the system memory
- image block** A portion cropped from an image at a certain size, with the maximum size equivalent to the entire image. i.e., hb, vb size under 2D-DMA 2D-MOD0.
- pixel block** A portion cropped from an image block. SRM reads and writes data in pixel blocks.

#### 33.3 Features

- Image rotation, scaling, and mirroring by SRM:

- Input formats: ARGB8888, RGB888, RGB565, YUV420
- Output formats: ARGB8888, RGB888, RGB565, YUV420
- Counterclockwise rotation angles: 0°, 90°, 180°, 270°
- Horizontal and vertical scaling with scaling factors of 4-bit integer part and 8-bit fractional part
- Horizontal and vertical mirroring
- Blending two layers of the same size and filling images with specific pixels by BLEND:
  - Input formats: ARGB8888, RGB888, RGB565, L4, L8, A4, A8
  - Output formats: ARGB8888, RGB888, RGB565
  - Layer blending based on the Alpha channel. If layers lack an Alpha channel, it can be provided through register configuration.
  - Special color filtering by setting color-key ranges of foreground and background layers

## 33.4 Architectural Overview

As shown in figure 33.4-1, there are two independent functional modules in PPA: SRM and BLEND.

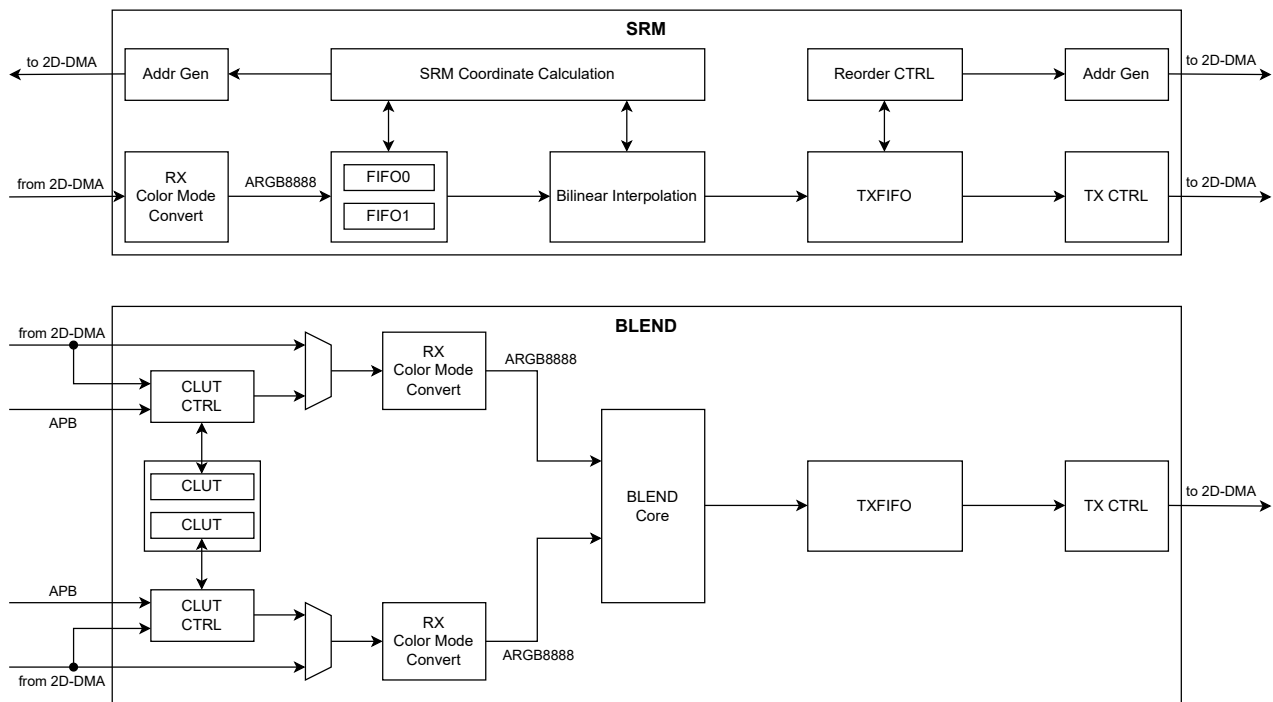


Figure 33.4-1. PPA Architecture

For SRM, SRM Coordinate Calculation scans coordinates of the output pixel blocks and calculates coordinates of the corresponding input pixel blocks. Addr Gen calculates the address according to the input pixel block coordinates and sends them to 2D-DMA. After that, the PPA receives the pixel block data from 2D-DMA, converts it into ARGB8888 format according to the register configuration, and stores it into the RX FIFO (a ping-pong FIFO composed of two SRAMs, each of which can store the whole pixel block). When a complete pixel block is cached, Bilinear Interpolation reads the input pixels from RX FIFO, interpolates them to get the

output pixels, and outputs them to TX FIFO. Reorder CTRL then calculates the output pixel block coordinates and address according to the register configuration and sends them to 2D-DMA. At the same time, Reorder CTRL takes out the corresponding pixels from TX FIFO according to the output pixel block coordinates and sends them to 2D-DMA, which saves them to the corresponding address.

For BLEND, PPA also receives data from 2D-DMA and converts it to ARGB8888 format based on the input data type. Yet the converted pixels will be processed directly by the BLEND Core algorithm module, enter the TX FIFO, and ultimately output to the system memory through 2D-DMA. Unlike SRM, BLEND does not need to calculate the address itself as it is completely controlled by 2D-DMA through a linked list.

## 33.5 Functional Description

### 33.5.1 PPA Color Spaces

PPA supports both true color and pseudo color. True color refers to a color representation in which each pixel in a color image consists of three primary color components: R (red), G (green), and B (blue). Each of these components directly determines the intensity of the corresponding primary color on the display device. The true color formats supported by PPA include ARGB8888, RGB888, and RGB565.

Pseudo color refers to a color representation in which the color of each pixel in a color image is not directly determined by the numerical values of the primary color components. Instead, the pixel value serves as an entry into a Color Look-Up Table (CLUT) to retrieve the corresponding A, R, G, and B values. PPA supports CLUT entry addresses with 8-bit or 4-bit width.

In addition, SRM supports the YUV420 data format. The storage order of supported color formats in memory is shown in Table 33.5-1.

Table 33.5-1. Pixel Storage Order

| Color Format                              | Start Addr + 3 | Start Addr + 2 | Start Addr + 1 | Start Addr + 0 |
|---|----------------|----------------|----------------|----------------|
| ARGB8888                                  | A0[7:0]        | R0[7:0]        | G0[7:0]        | B0[7:0]        |
| RGB888                                    | B1[7:0]        | R0[7:0]        | G0[7:0]        | B0[7:0]        |
|   | G2[7:0]        | B2[7:0]        | R1[7:0]        | G1[7:0]        |
|   | R3[7:0]        | G3[7:0]        | B3[7:0]        | R2[7:0]        |
| RGB565                                    | R1[4:0]G1[5:3] | G1[2:0]B1[4:0] | R0[4:0]G0[5:3] | G0[2:0]B0[4:0] |
| L8  | L3[7:0]        | L2[7:0]        | L1[7:0]        | L0[7:0]        |
| L4  | L7[3:0]L6[3:0] | L5[3:0]L4[3:0] | L3[3:0]L2[3:0] | L1[3:0]L0[3:0] |
| A8  | A3[7:0]        | A2[7:0]        | A1[7:0]        | A0[7:0]        |
| A4  | A7[3:0]A6[3:0] | A5[3:0]A4[3:0] | A3[3:0]A2[3:0] | A1[3:0]A0[3:0] |
| YUV420<br>Odd rows<br>such as 1, 3, 5...  | U2[7:0]        | Y1[7:0]        | Y0[7:0]        | U0[7:0]        |
|   | Y4[7:0]        | U4[7:0]        | Y3[7:0]        | Y2[7:0]        |
|   | Y7[7:0]        | Y6[7:0]        | U6[7:0]        | Y5[7:0]        |
| YUV420<br>Even rows<br>such as 2, 4, 6... | V2[7:0]        | Y1[7:0]        | Y0[7:0]        | V0[7:0]        |
|   | Y4[7:0]        | V4[7:0]        | Y3[7:0]        | Y2[7:0]        |
|   | Y7[7:0]        | Y6[7:0]        | V6[7:0]        | Y5[7:0]        |



### 33.5.1.1 SRM Color Space

SRM supports ARGB8888, RGB888, RGB565, and YUV420 formats for both input and output. The input format is configured by `PPA_SRM_RX_CM`, while the output format is configured by `PPA_SRM_TX_CM`. The SRM input pixel processing steps are shown in Figure 33.5-1.

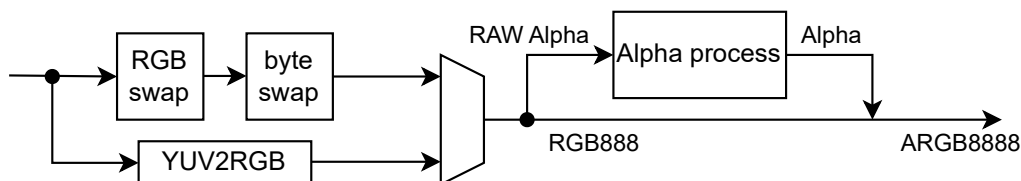


Figure 33.5-1. PPA SRM Input Pixel Processing

SRM supports RGB and byte swapping for ARGB8888, RGB888, and RGB565 input formats. The specific configurations are as follows:

- Set `PPA_SRM_RX_RGB_SWAP_EN` to 1 to reverse RGB to BGR and ARGB to BGRA.
- Set `PPA_SRM_RX_BYTE_SWAP_EN` to 1 to reverse bytes 0, 1 and 2, 3 respectively, i.e., {0, 1, 2, 3} will be reverted to {1, 0, 3, 2}. RGB888 would not be affected by this configuration as it only has three bytes per pixel.

SRM uses ARGB8888 when processing images internally. When the input lacks an Alpha channel, the default Alpha channel value for the image is set to 255. The Alpha channel can be further configured using the `PPA_SRM_FIX_ALPHA_REG` register, as shown in Figure 33.5-2. For specific configuration effects, please refer to Table 33.5-2.

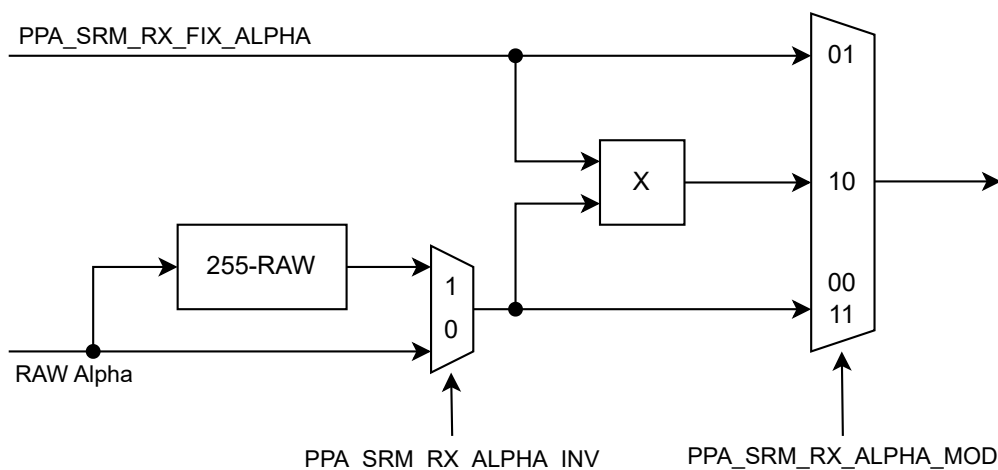


Figure 33.5-2. PPA SRM Alpha Configuration Logic

Table 33.5-2. PPA SRM Alpha Configuration

| <code>PPA_SRM_RX_ALPHA_INV</code> | <code>PPA_SRM_RX_ALPHA_MOD</code> | Output   |
|-----------------------------------|-----------------------------------|--|
| 0                                 | 00/11                             | Original Alpha value   |
|                                   | 01                                | The configuration value of <code>PPA_SRM_RX_FIX_ALPHA</code> |

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Table 33.5-2 – ...Continued from the previous page

| PPA_SRM_RX_ALPHA_INV | PPA_SRM_RX_ALPHA_MOD | Output   |
|----------------------|----------------------|--|
|                      | 10                   | The high 8 bits of the value obtained by multiplying the original Alpha value with <a href="#">PPA_SRM_RX_FIX_ALPHA</a>                                  |
| 1                    | 00/11                | The value obtained by subtracting the original Alpha value from 255  |
|                      | 01                   | The configuration value of <a href="#">PPA_SRM_RX_FIX_ALPHA</a>  |
|                      | 10                   | The high 8 bits of the value obtained by multiplying the result of subtracting the original Alpha value from 255 by <a href="#">PPA_SRM_RX_FIX_ALPHA</a> |

Note that when the input or output format is YUV, further configuration of YUV to RGB color conversion is required.

When the input format is YUV420, the input YUV data range needs to be configured as full-range or limit-range via the [PPA\\_YUV\\_RX\\_RANGE](#) field, and the protocol used for YUV to RGB conversion needs to be configured as BT601 or BT709 via the [PPA\\_YUV2RGB\\_PROTOCOL](#) field. The conversion formulas are as follows:

- $YUV_{full}$  to  $YUV_{limit}$ 
  - $Y_{limit} = \frac{220}{256}Y_{full} + 16$
  - $U_{limit} = \frac{225}{256}U_{full} + 16$
  - $V_{limit} = \frac{225}{256}V_{full} + 16$
- $YUV_{limit}$  to RGB in BT601
  - $R = \frac{298}{256}Y_{limit} + \frac{409}{256}V_{limit} - \frac{56906}{256}$
  - $G = \frac{298}{256}Y_{limit} - \frac{100}{256}U_{limit} - \frac{208}{256}V_{limit} + \frac{34707}{256}$
  - $B = \frac{298}{256}Y_{limit} + \frac{516}{256}U_{limit} - \frac{70836}{256}$
- $YUV_{limit}$  to RGB in BT709
  - $R = \frac{298}{256}Y_{limit} + \frac{459}{256}V_{limit} - \frac{63367}{256}$
  - $G = \frac{298}{256}Y_{limit} - \frac{55}{256}U_{limit} - \frac{136}{256}V_{limit} + \frac{19681}{256}$
  - $B = \frac{298}{256}Y_{limit} + \frac{541}{256}U_{limit} - \frac{73918}{256}$

When the output format is YUV420, the output YUV data range needs to be configured as full-range or limit-range via the [PPA\\_YUV\\_TX\\_RANGE](#) field, and the protocol used for YUV to RGB conversion needs to be configured as BT601 or BT709 via the [PPA\\_RGB2YUV\\_PROTOCOL](#) field. The conversion formulas are as follows:

- $YUV_{limit}$  to  $YUV_{full}$ 
  - $Y_{full} = \frac{298}{256}Y_{limit} + \frac{4768}{256}$
  - $U_{full} = \frac{291}{256}U_{limit} + \frac{4550}{256}$
  - $V_{full} = \frac{291}{256}V_{limit} + \frac{4550}{256}$
- RGB to  $YUV_{limit}$  in BT601

$$\begin{aligned}
- Y_{limit} &= \frac{4096}{256} + \frac{66}{256}R + \frac{129}{256}G + \frac{25}{256}B \\
- U_{limit} &= \frac{32768}{256} - \frac{38}{256}R - \frac{74}{256}G + \frac{112}{256}B \\
- V_{limit} &= \frac{32768}{256} + \frac{112}{256}R - \frac{94}{256}G - \frac{18}{256}B
\end{aligned}$$

- RGB to  $YUV_{limit}$  in BT709

$$\begin{aligned}
- Y_{limit} &= \frac{4096}{256} + \frac{47}{256}R + \frac{157}{256}G + \frac{16}{256}B \\
- U_{limit} &= \frac{32768}{256} - \frac{26}{256}R - \frac{86}{256}G + \frac{112}{256}B \\
- V_{limit} &= \frac{32768}{256} + \frac{112}{256}R - \frac{102}{256}G - \frac{10}{256}B
\end{aligned}$$

### 33.5.1.2 BLEND Color Space

For the input format, BLEND supports ARGB8888, RGB888, RGB565, L4, L8, A4, and A8. The input color format of the foreground and background layers can be configured respectively via the [PPA\\_BLEND0/1\\_RX\\_CM](#) field. Among the above input formats, A4 and A8 only support the foreground layer, and when the input format is L4 or A4, the size of the image block, hb, and the offset in the image, x, must be an even number. For the output format, BLEND supports ARGB8888, RGB888, and RGB565, which can be configured via the [PPA\\_BLEND\\_TX\\_CM](#) field.

BLEND's RGB conversion, byte conversion, and alpha channel configuration are consistent with SRM input. Additionally, when the foreground layer data format is A4 or A8, the input data will be Alpha channel values. In this case, if [PPA\\_BLEND\\_BYPASS](#) is set as 1, the foreground layer's input Alpha value replaces the background layer's Alpha channel and output. If set as 0, it will be a normal BLEND operation, and the foreground layer's RGB values will be specified by [PPA\\_BLEND\\_RGB\\_REG](#).

When the input data format is L4 or L8, it requires to first initialize the CLUT for BLEND. BLEND has two CLUTs with a depth of 256 and a width of 32. There are two initialization modes: FIFO and MEM.

- Write 0 to [PPA\\_APB\\_FIFO\\_MASK](#) to enter the FIFO mode.  
In the FIFO mode, access to CLUT is achieved by reading/writing [PPA\\_RDWR\\_WORD\\_BLENDx\\_CLUT](#), where 0 corresponds to the background channel CLUT and 1 corresponds to the foreground channel CLUT.  
Each time this register is read/written, the corresponding read/write address is automatically incremented by 1. The read/write address can be reset by writing 1 and then 0 to [PPA\\_BLENDx\\_CLUT\\_MEM\\_RST](#). The read address can be reset by writing 1 then 0 to [PPA\\_BLENDx\\_CLUT\\_MEM\\_RDADDR\\_RST](#).
- Write 1 to [PPA\\_APB\\_FIFO\\_MASK](#) to enter the MEM mode.  
In the MEM mode, CLUT can be directly accessed through addresses. The CLUT addresses in the PPA's bus address range are as shown in Table 33.5-3.

Table 33.5-3. BLEND CLUT Address

| addr[11:10]                                      | addr[9:2]                    | addr[1:0] |
|--|------------------------------|-----------|
| 01: Select BLEND0 CLUT<br>10: Select BLEND1 CLUT | CLUT actual address, 0 ~ 255 | 00        |

### 33.5.2 PPA 2D-DMA Linked List Configuration

PPA exchanges data with the system memory via 2D-DMA. For both SRM and BLEND, it is necessary to configure the 2D-DMA linked list information for the required image block operations in one go. The 2D-DMA linked list is shown in Figure 33.5-3. For detailed information, please refer to [5 2D-DMA Controller \(2D-DMA\)](#).

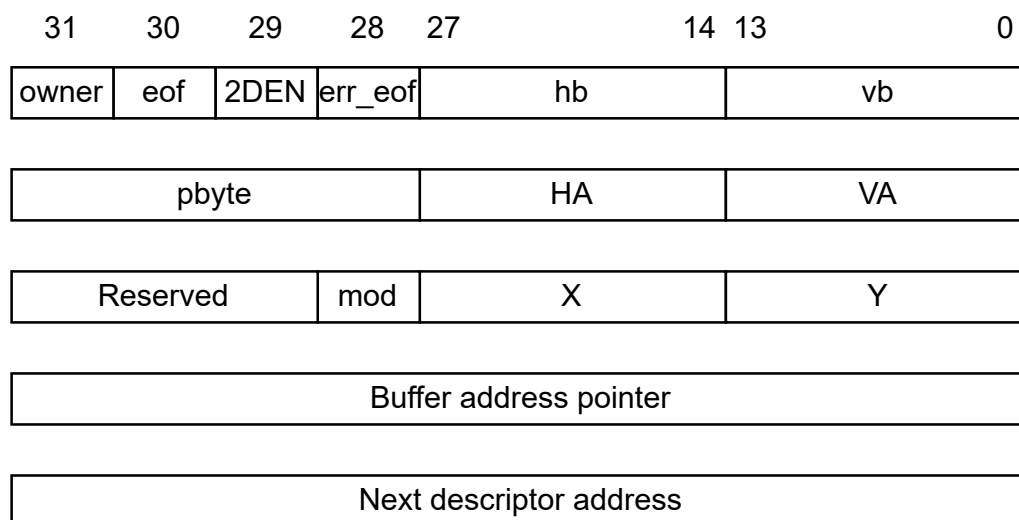


Figure 33.5-3. 2D-DMA Linked List

The corresponding linked list parameters of PPA are shown in Table 33.5-4.

Table 33.5-4. PPA Linked List Configuration

| Field   | Configuration  |
|---------|--|
| owner   | 1  |
| eof     | 1  |
| 2DEN    | 1  |
| err_eof | 0  |
| hb      | Horizontal size of the image block.<br>Must be even if the input or output data format is YUV420   |
| vb      | Vertical size of the image block.<br>Must be even if the input or output data format is YUV420   |
| pbyte   | ARGB8888: 5 (4 byte/pixel)<br>RGB888: 4 (3 byte/pixel)<br>RGB565: 3 (2 byte/pixel)<br>YUV420: 2 (1.5 byte/pixel)<br>A8/L8: 1 (1 byte/pixel)<br>A4/L4: 0 (0.5 byte/pixel) |

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Table 33.5-4 – ...Continued from the previous page

| Field                   | Configuration   |
|-------------------------|---|
| HA                      | Horizontal size of the entire image.<br>Must be even if the input or output data format is YUV420                                   |
| VA                      | Vertical size of the entire image.<br>Must be even if the input or output data format is YUV420                                     |
| mod                     | 0   |
| X                       | Horizontal offset of the image block within the image (offset starts from 0).<br>Must be even if the input or output data is YUV420 |
| Y                       | Vertical offset of the image block within the image (offset starts from 0).<br>Must be even if the input or output data is YUV420   |
| Buffer address pointer  | Starting address of the image   |
| Next descriptor address | N/A   |

### 33.5.2.1 SRM Special Configuration

Once the 2D-DMA linked lists for input and output image blocks are configured, SRM needs to select the required pixel blocks from the input image block memory space and process them in units of pixel blocks. The processed pixel blocks are then stored in the corresponding memory space of the output image block. Throughout this process, the starting address of each pixel block needs to be controlled by SRM. To realize this functionality, write 1 to the `DMA2D_IN/OUT_DSCR_PORT_EN_CHx` field of the corresponding channel of the 2D-DMA to enable the descriptor interface (also called DSCR-PORT in 2D-DMA), allowing PPA to control the starting address of the next pixel block in real-time.

For the data input, SRM must receive a complete pixel block each time. When the pixel block selection reaches the boundary of the image block, 2D-DMA needs to automatically pad the pixel block beyond the boundary. This can be achieved by configuring the `DMA2D_OUT_DSCR_PORT_BLK_V/H_CHx` field of the corresponding channel of 2D-DMA to the pixel block size. The pixel block size is 18x18 when the input data is ARGB8888, RGB888, or RGB565; and 20x20 when the input data is YUV420.

## 33.5.3 Scaling - Rotation - Mirroring (SRM)

### 33.5.3.1 Basic Functionality

SRM supports scaling, rotation, and mirroring. It first scales the image based on the origin point, then rotates it around the center point ( $X_{middle}$ ,  $Y_{middle}$ ), and finally mirrors it horizontally and vertically based on the center point ( $X_{target}$ ,  $Y_{target}$ ), as shown in Figure 33.5-4. Scaling, rotation, and mirroring parameters are all configured through registers:

- `PPA_SRM_SCAL_X_INT`: Integer part of the horizontal scaling factor
- `PPA_SRM_SCAL_X_FRAG`: Fractional part of the horizontal scaling factor

- `PPA_SRM_SCAL_Y_INT`: Integer part of the vertical scaling factor
- `PPA_SRM_SCAL_Y_FRAG`: Fractional part of the vertical scaling factor
- `PPA_SRM_ROTATE_ANGLE`: Counterclockwise rotation angle
- `PPA_SRM_MIRROR_X`: Enable horizontal mirroring
- `PPA_SRM_MIRROR_Y`: Enable vertical mirroring

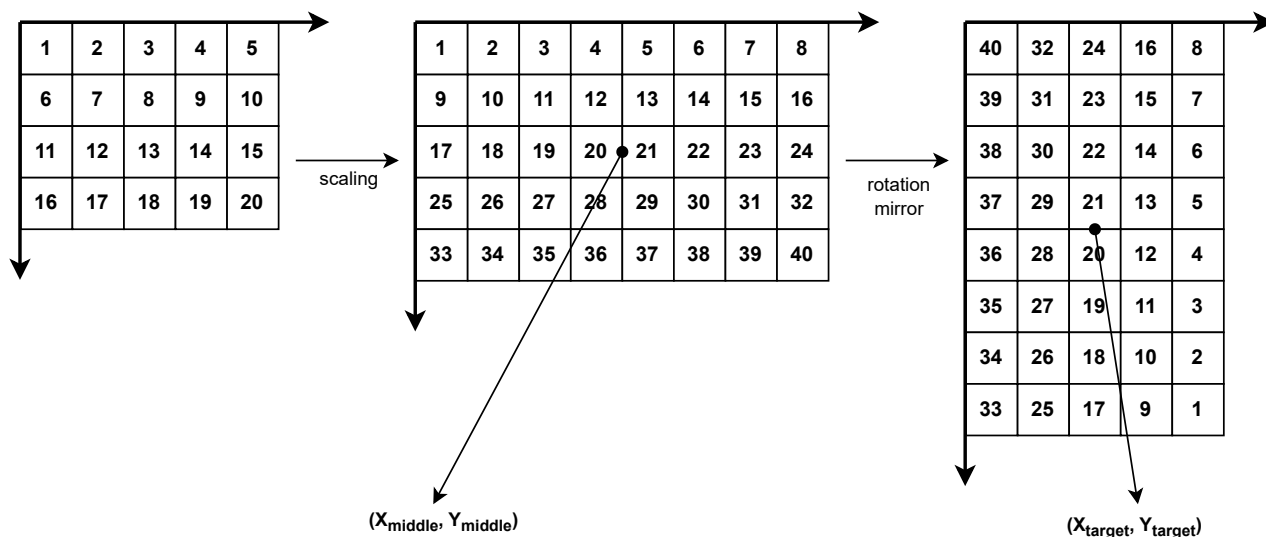


Figure 33.5-4. SRM Procedure

### 33.5.3.2 Pixel Block Rearrangement

When the output pixel block is small, initiating a 2D-DMA transfer for each pixel block would result in low bus bandwidth utilization. To improve bus bandwidth utilization, SRM can cache and concatenate output pixel blocks into a larger pixel block before outputting them all at once. This feature is enabled by default and can be disabled by setting `PPA_SRM_MACRO_BK_RO_BYPASS` to 1.

Once pixel block rearrangement is enabled, under certain conditions, the output pixel blocks will be automatically rearranged and concatenated, as specified in Table 33.5-5.

- For the output pixel block in ARGB8888/RGB888 format, if its vertical height is less than or equal to 32, and the horizontal width is less than or equal to 16, pixel block rearrangement will be automatically enabled.
- For the output pixel block in RGB565 format, if its vertical height is less than or equal to 32, and the horizontal width is less than or equal to 32, pixel block rearrangement will be automatically enabled.
- For the output pixel block in YUV420 format, if its vertical height is less than or equal to 32, and horizontal width is less than or equal to 32, pixel block rearrangement will be automatically enabled.

Table 33.5-5. Number of Pixel Block Rearrangements in SRM Output

| ARGB8888/RGB888 |                      | RGB565          |                      | YUV420                 |                      |
|-----------------|----------------------|-----------------|----------------------|------------------------|----------------------|
| Horizontal Size | Rearrangement Number | Horizontal Size | Rearrangement Number | Horizontal Size (Even) | Rearrangement Number |
| 1               | 32                   | 1               | 64                   | 2                      | 32                   |
| 2               | 16                   | 2               | 32                   | 4                      | 16                   |
| 3               | 10                   | 3               | 20                   | 6                      | 10                   |
| 4               | 8                    | 4               | 16                   | 8                      | 8                    |
| 5               | 6                    | 5               | 12                   | 10                     | 6                    |
| 6               | 5                    | 6               | 10                   | 12                     | 5                    |
| 7               | 4                    | 7               | 9                    | 14                     | 4                    |
| 8               | 4                    | 8               | 8                    | 16                     | 4                    |
| 9               | 3                    | 9               | 7                    | 18                     | 3                    |
| 10              | 3                    | 10              | 6                    | 20-32                  | 2                    |
| 11              | 2                    | 11              | 5                    |                        |                      |
| 12              | 2                    | 12              | 5                    |                        |                      |
| 13              | 2                    | 13              | 4                    |                        |                      |
| 14              | 2                    | 14              | 4                    |                        |                      |
| 15              | 2                    | 15              | 4                    |                        |                      |
| 16              | 2                    | 16              | 4                    |                        |                      |
|                 |                      | 17              | 3                    |                        |                      |
|                 |                      | 18              | 3                    |                        |                      |
|                 |                      | 19-32           | 2                    |                        |                      |

### 33.5.4 Layer Blending (BLEND)

#### 33.5.4.1 Basic Functionality

BLEND combines two image blocks of the same size using the Alpha channel and then outputs the result. The blending formula is as follows, where  $A_b$  is the Alpha channel of the background layer,  $A_f$  is the Alpha channel of the foreground layer,  $C_b$  corresponds to the R, G, and B components of the background layer, and  $C_f$  corresponds to the R, G, B components of the foreground layer:

- $A_{out} = A_b + A_f - A_b * A_f$
- $C_{out} = (C_b * A_b * (1 - A_f) + C_f * A_f) / (A_b + A_f - A_b * A_f)$

Additionally, BLEND supports color-keying based on pixel color. By configuring color ranges via [PPA\\_CK\\_FG/BG\\_HIGH/LOW\\_REG](#), BLEND allows for image segmentation into four distinct regions, each subjected to different operations:

- When the foreground pixel falls within the color-key range and the background pixel falls outside the color-key range, output the background pixel.
- When the background pixel falls within the color-key range and the foreground pixel falls outside the color-key range, the output depends on the value of [PPA\\_COLORKEY\\_FG\\_BG\\_REVERSE](#). If 0, output the background pixel; if 1, output the foreground pixel.

- When both the background and foreground pixels fall within the color-key range, the output is set to the color defined by [PPA\\_COLORKEY\\_DEFAULT\\_R/G/B](#).
- When neither the background nor foreground pixels fall within the color-key range, output follows the normal Alpha Blending process.

When [PPA\\_BLEND\\_BYPASS](#) is set to 1, BLEND directly outputs the background layer data. If the foreground input data type is A4/A8 at this time, the foreground input data will replace the background input data's Alpha channel and then be output.

### 33.5.4.2 Filled Image Output

BLEND also supports filled image output. When this feature is enabled, only the output side of BLEND works, continuously outputting the filled image. The size and data of the filled image can be configured via [PPA\\_BLEND\\_TX\\_SIZE\\_REG](#) and [PPA\\_BLEND\\_TX\\_FIX\\_PIXEL](#).

## 33.6 Interrupts

ESP32-P4's PPA can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- PPA\_INTR

The following interrupt sources can generate PPA\_INTR interrupt signal:

- PPA\_SRM\_PARAM\_CFG\_INT: Triggered when invalid parameters are configured in the SRM mode. You can acquire the specific error type through [PPA\\_SRM\\_PARAM\\_ERR\\_ST\\_REG](#), as shown in Table 33.6-1.
- PPA\_SRM\_EOF\_INT: Triggered when SRM workflow reaches EOF.
- PPA\_BLEND\_EOF\_INT:: Triggered when BLEND workflow reaches EOF.

**Table 33.6-1. SRM Parameter Error Type**

| Error Type                                   | Detail   |
|--|--|
| <a href="#">PPA_TX_DSCR_VB_ERR_ST</a>        | The sum of the vertical size of the output image block from SRM and the vertical offset Y specified in the output descriptor exceeds the total vertical size of the image configured in the output descriptor (VA)     |
| <a href="#">PPA_TX_DSCR_HB_ERR_ST</a>        | The sum of the horizontal size of the output image block from SRM and the vertical offset X specified in the output descriptor exceeds the total horizontal size of the image configured in the output descriptor (HA) |
| <a href="#">PPA_Y_RX_SCAL_EQUAL_O_ERR_ST</a> | The vertical scaling factor for the input image block in SRM is set to 0   |
| <a href="#">PPA_RX_DSCR_VB_ERR_ST</a>        | The sum of the vertical size VB and the vertical offset Y in the SRM input descriptor exceeds the overall vertical size VA in the output descriptor  |

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Table 33.6-1 – ...Continued from the previous page

| Error Type                                    | Detail  |
|---|---|
| <a href="#">PPA_YDST_LEN_TOO_SAMLL_ERR_ST</a> | The vertical size of the image block after SRM scaling is 0. For example, if the vertical size of the image block is 14 and the vertical scaling factor is 1/16 without rotation, the scaled vertical size of the image block becomes 0 |
| <a href="#">PPA_YDST_LEN_TOO_LARGE_ERR_ST</a> | The vertical size of the image block after SRM scaling exceeds 8191   |
| <a href="#">PPA_X_RX_SCAL_EQUAL_O_ERR_ST</a>  | The horizontal scaling factor for the input image block in SRM is 0   |
| <a href="#">PPA_RX_DSCR_HB_ERR_ST</a>         | The sum of the horizontal size HB of the input image block configured in the SRM input descriptor and the horizontal offset X exceeds the entire image's horizontal size HA configured in the output descriptor                         |
| <a href="#">PPA_XDST_LEN_TOO_SAMLL_ERR_ST</a> | The horizontal size of the image block after SRM scaling is 0   |
| <a href="#">PPA_XDST_LEN_TOO_LARGE_ERR_ST</a> | The horizontal size of the image block after SRM scaling exceeds 8191   |
| <a href="#">PPA_X_YUV420_RX_SCALE_ERR_ST</a>  | The input descriptor parameters HA/hb/X happen to be odd numbers when the SRM input format is YUV420  |
| <a href="#">PPA_Y_YUV420_RX_SCALE_ERR_ST</a>  | The input descriptor parameters VA/vb/Y happen to be odd numbers when the SRM input format is YUV420  |
| <a href="#">PPA_X_YUV420_TX_SCALE_ERR_ST</a>  | The output descriptor parameters HA/hb/X happen to be odd numbers when the SRM output format is YUV420  |
| <a href="#">PPA_Y_YUV420_TX_SCALE_ERR_ST</a>  | The output descriptor parameters VA/vb/Y happen to be odd numbers when the SRM output format is YUV420  |

## 33.7 Programming Procedures

### 33.7.1 PPA Clock Reset Configuration

1. Enable the clock of the PPA and 2D-DMA modules:
  - Write 1 to [HP\\_SYS\\_CLKRST\\_PPA\\_SYS\\_CLK\\_EN](#) to enable the PPA clock
  - Write 1 to [HP\\_SYS\\_CLKRST\\_DMA2D\\_SYS\\_CLK\\_EN](#) to enable the 2D-DMA clock
2. Reset the PPA and 2D-DMA modules:
  - Write 1 and then 0 to [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_PPA](#) reset PPA
  - Write 1 and then 0 to [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_DMA2D](#) reset 2D-DMA

### 33.7.2 SRM Configuration

1. Refer to Section [33.7.1](#) to enable and reset PPA and 2D-DMA.
2. Configure the inlink and outlink of 2D-DMA. For detailed parameters, please refer to Table [33.5-4](#).
3. Select the input and output channels of 2D-DMA:
  - Write 0x1 to [DMA2D\\_OUT\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA output channel to the PPA SRM input

- Write 0x1 to [DMA2D\\_IN\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA input channel to the PPA SRM output
4. Enable descriptor interface for 2D-DMA channels used by PPA:
    - Write 1 to [DMA2D\\_OUT\\_DSCR\\_PORT\\_EN\\_CHx](#) to enable descriptor interface
    - Write 1 to [DMA2D\\_IN\\_DSCR\\_PORT\\_EN\\_CHx](#) to enable descriptor interface
  5. Configure the descriptor interface completion parameters of 2D-DMA:
    - Configure the horizontal completion parameters via [DMA2D\\_OUT\\_DSCR\\_PORT\\_BLK\\_H\\_CHx](#) to 20 for YUV420, or to 18 for other color modes
    - Configure the vertical completion parameters via [DMA2D\\_OUT\\_DSCR\\_PORT\\_BLK\\_V\\_CHx](#) to 20 for YUV420, or to 18 for other color modes
  6. Enable the input and output channels of 2D-DMA:
    - Write 1 to [DMA2D\\_OUTLINK\\_START\\_CHx](#) to enable the output channel of 2D-DMA
    - Write 1 to [DMA2D\\_INLINK\\_START\\_CHx](#) to enable the input channel of 2D-DMA
  7. Configure SRM parameters:
    - Configure SRM input data format via [PPA\\_SRM\\_RX\\_CM](#)
    - Configure SRM output data format via [PPA\\_SRM\\_TX\\_CM](#)
    - Configure the integer part of the horizontal scaling factor via [PPA\\_SRM\\_SCAL\\_X\\_INT](#)
    - Configure the fractional part of the horizontal scaling factor via [PPA\\_SRM\\_SCAL\\_X\\_FRAG](#)
    - Configure the integer part of the vertical scaling factor via [PPA\\_SRM\\_SCAL\\_Y\\_INT](#)
    - Configure the fractional part of the vertical scaling factor via [PPA\\_SRM\\_SCAL\\_Y\\_FRAG](#)
    - Configure the counterclockwise rotation angle via [PPA\\_SRM\\_ROTATE\\_ANGLE](#)
    - Enable horizontal mirroring via [PPA\\_SRM\\_MIRROR\\_X](#)
    - Enable vertical mirroring via [PPA\\_SRM\\_MIRROR\\_Y](#)
  8. Write 1 to [PPA\\_SCAL\\_ROTATE\\_START](#) to start the SRM workflow.

### 33.7.3 BLEND CLUT Configuration

1. In the FIFO mode:
  - Write 0 to [PPA\\_APB\\_FIFO\\_MASK](#) to enter the FIFO mode
  - Write data to [PPA\\_RDWR\\_WORD\\_BLEND0\\_CLUT](#) to initialize the background layer's CLUT
  - Write data to [PPA\\_RDWR\\_WORD\\_BLEND1\\_CLUT](#) to initialize the foreground layer's CLUT
2. In the MEM mode:
  - Write 1 to [PPA\\_APB\\_FIFO\\_MASK](#) to enter the MEM mode
  - Initialize the CLUT by writing data directly to the corresponding address, referring to Table [33.5-3](#)

### 33.7.4 BLEND Configuration

1. Refer to Section [33.7.1](#) to enable and reset PPA and 2D-DMA.
2. Configure the input and output link lists of 2D-DMA. For detailed parameters, please refer to Table [33.5-4](#).
3. Select the input and output channels of 2D-DMA:
  - Write 0x2 to [DMA2D\\_OUT\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA output channel to PPA BLEND for background layer input
  - Write 0x3 to [DMA2D\\_OUT\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA output channel to PPA BLEND for foreground layer input
  - Write 0x2 to [DMA2D\\_IN\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA input channel to PPA BLEND for output
4. Enable the input and output channels for 2D-DMA. The x in the registers refers to the two channels allocated to BLEND foreground and background respectively:
  - Write 1 to [DMA2D\\_OUTLINK\\_START\\_CHx](#) to enable the output channel of 2D-DMA
  - Write 1 to [DMA2D\\_INLINK\\_START\\_CHx](#) to enable the input channel of 2D-DMA
5. Configure BLEND parameter:
  - Configure the data type for the background layer input of BLEND via [PPA\\_BLEND0\\_RX\\_CM](#). If the format is L4/L8, initialize the CLUT first as described in [33.7.3](#)
  - Configure the data type for the background layer input of BLEND via [PPA\\_BLEND1\\_RX\\_CM](#). If the format is L4/L8, initialize the CLUT first as described in [33.7.3](#)
  - Configure the output data format of BLEND via [PPA\\_BLEND\\_TX\\_CM](#)
  - Configure the upper and lower limits of the color-key for the background layer via [PPA\\_CK\\_BG\\_HIGH\\_REG](#) and [PPA\\_CK\\_BG\\_LOW\\_REG](#)
  - Configure the upper and lower limits of the color-key for the foreground layer via [PPA\\_CK\\_FG\\_HIGH\\_REG](#) and [PPA\\_CK\\_FG\\_LOW\\_REG](#)
  - Configure the default value and behavior for the color-key via [PPA\\_CK\\_DEFAULT\\_REG](#)
  - Write 1 to [PPA\\_BLEND\\_EN](#) to enable BLEND
6. Write 1 to [PPA\\_BLEND\\_TRANS\\_MODE\\_UPDATE](#) to start BLEND workflow

### 33.7.5 BLEND Image Filling Configuration

1. Refer to Section [33.7.1](#) to enable and reset PPA and 2D-DMA.
2. Configure the input link lists of 2D-DMA (output link lists of PPA BLEND). For detailed parameters, please refer to Table [33.5-4](#).
3. Write 0x2 to [DMA2D\\_IN\\_PERI\\_SEL\\_CHx](#) to allocate one 2D-DMA input channel to PPA BLEND output.
4. Write 1 to [DMA2D\\_INLINK\\_START\\_CHx](#) to enable the output channel of 2D-DMA.
5. Configure BLEND parameters:
  - Configure the output data format of BLEND via [PPA\\_BLEND\\_TX\\_CM](#)

- Write 1 to [PPA\\_BLEND\\_FIX\\_PIXEL\\_FILL\\_EN](#) to enable image filling
- Configure the pixel value for image filling via [PPA\\_BLEND\\_TX\\_FIX\\_PIXEL](#)
- Configure the filled image size via [PPA\\_BLEND\\_HB](#) and [PPA\\_BLEND\\_VB](#)

6. Write 1 to [PPA\\_BLEND\\_TRANS\\_MODE\\_UPDATE](#) to start BLEND workflow.

### 33.7.6 Error Handling

- Refer to Section [33.7.1](#) to reset the whole PPA, and configure again.
- Or write 1 and then 0 to reset SRM and BLEND via [PPA\\_SCAL\\_ROTATE\\_RST](#), [PPA\\_BLEND\\_RST](#), and configure again.

**Note:**

- The 2D-DMA configurations mentioned in this chapter involve only key steps. For detailed procedures, please refer to [5 2D-DMA Controller \(2D-DMA\)](#).
- In this chapter, DMA2D\_OUT corresponds to the PPA input direction, and DMA2D\_IN corresponds to the PPA output direction.

## 33.8 Register Summary

The addresses in this section are relative to the Pixel-Processing Accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                     | Description   | Address | Access           |
|--|---|---------|------------------|
| <b>Configuration Registers</b>           |   |         |                  |
| <a href="#">PPA_BLEND0_CLUT_DATA_REG</a> | CLUT SRAM data read/write register of BLEND background layer  | 0x0000  | R/W              |
| <a href="#">PPA_BLEND1_CLUT_DATA_REG</a> | CLUT SRAM data read/write register of BLEND foreground layer  | 0x0004  | R/W              |
| <a href="#">PPA_CLUT_CONF_REG</a>        | Configures BLEND CLUT   | 0x000C  | R/W              |
| <a href="#">PPA_SRM_COLOR_MODE_REG</a>   | Configures SRM color space                                    | 0x0020  | R/W              |
| <a href="#">PPA_BLEND_COLOR_MODE_REG</a> | Configures BLEND color space                                  | 0x0024  | R/W              |
| <a href="#">PPA_SRM_BYTE_ORDER_REG</a>   | Configures SRM byte order                                     | 0x0028  | R/W              |
| <a href="#">PPA_BLEND_BYTE_ORDER_REG</a> | Configures BLEND byte order                                   | 0x002C  | R/W              |
| <a href="#">PPA_BLEND_TRANS_MODE_REG</a> | Configures the BLEND mode                                     | 0x0034  | varies           |
| <a href="#">PPA_SRM_FIX_ALPHA_REG</a>    | Configures SRM Alpha channel                                  | 0x0038  | R/W              |
| <a href="#">PPA_BLEND_TX_SIZE_REG</a>    | Configures BLEND image filling size                           | 0x003C  | R/W              |
| <a href="#">PPA_BLEND_FIX_ALPHA_REG</a>  | Configures BLEND Alpha override                               | 0x0040  | R/W              |
| <a href="#">PPA_BLEND_RGB_REG</a>        | Configures RGB color  | 0x0048  | R/W              |
| <a href="#">PPA_BLEND_FIX_PIXEL_REG</a>  | Configures BLEND image filling pixel                          | 0x004C  | R/W              |
| <a href="#">PPA_CK_FG_LOW_REG</a>        | Configures the foreground color-key lower threshold of BLEND  | 0x0050  | R/W              |
| <a href="#">PPA_CK_FG_HIGH_REG</a>       | Configures the foreground color-key higher threshold of BLEND | 0x0054  | R/W              |
| <a href="#">PPA_CK_BG_LOW_REG</a>        | Configures the background color-key lower threshold of BLEND  | 0x0058  | R/W              |
| <a href="#">PPA_CK_BG_HIGH_REG</a>       | Configures the background color-key higher threshold of BLEND | 0x005C  | R/W              |
| <a href="#">PPA_CK_DEFAULT_REG</a>       | Configures the default color-key value of BLEND               | 0x0060  | R/W              |
| <a href="#">PPA_SRM_SCAL_ROTATE_REG</a>  | Configures the SRM mode                                       | 0x0064  | varies           |
| <a href="#">PPA_SRM_MEM_PD_REG</a>       | Configures SRM memory   | 0x0068  | R/W              |
| <a href="#">PPA_REG_CONF_REG</a>         | Enables register clock  | 0x006C  | R/W              |
| <b>Interrupt Registers</b>               |   |         |                  |
| <a href="#">PPA_INT_RAW_REG</a>          | Raw status interrupt  | 0x0010  | R/<br>WTC/<br>SS |
| <a href="#">PPA_INT_ST_REG</a>           | Masked interrupt  | 0x0014  | RO               |
| <a href="#">PPA_INT_ENA_REG</a>          | Interrupt enable bits   | 0x0018  | R/W              |
| <a href="#">PPA_INT_CLR_REG</a>          | Interrupt clear bits  | 0x001C  | WT               |
| <b>Status Registers</b>                  |   |         |                  |

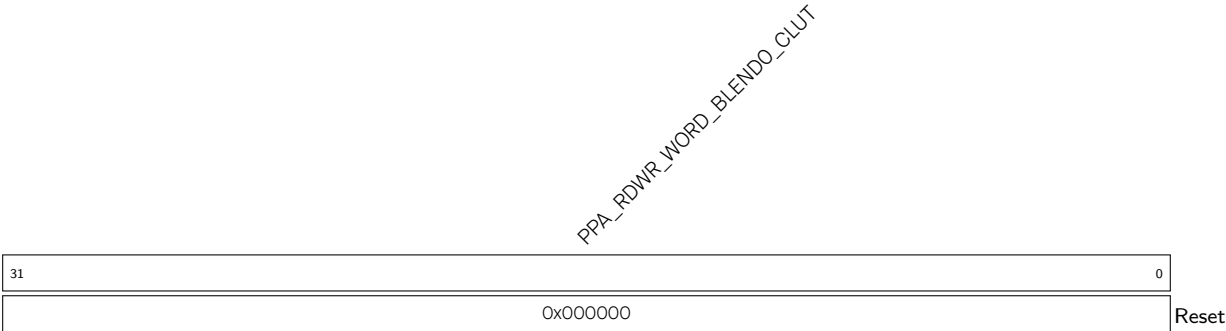
| Name                                     | Description                             | Address | Access |
|--|---|---------|--------|
| <a href="#">PPA_CLUT_CNT_REG</a>         | BLEND CLUT write counter register       | 0x0070  | RO     |
| <a href="#">PPA_BLEND_ST_REG</a>         | BLEND status register                   | 0x0074  | RO     |
| <a href="#">PPA_SRM_PARAM_ERR_ST_REG</a> | SRM configuration error status register | 0x0078  | RO     |
| <a href="#">PPA_SRM_STATUS_REG</a>       | SRM FSM register                        | 0x007C  | RO     |
| <b>Version Register</b>                  |   |         |        |
| <a href="#">PPA_DATE_REG</a>             | PPA Version register                    | 0x0100  | R/W    |

### 33.9 Registers

The addresses in this section are relative to the Pixel-Processing Accelerator base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

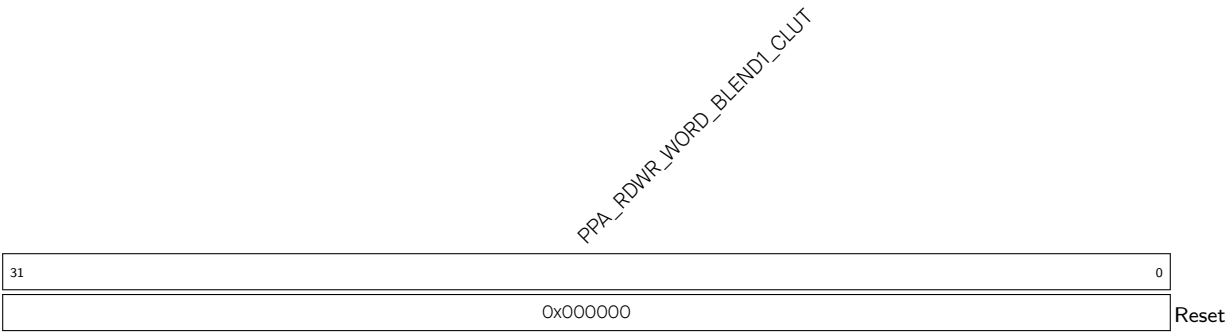
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 33.1. PPA\_BLEND0\_CLUT\_DATA\_REG (0x0000)



**PPA\_RDWR\_WORD\_BLEND0\_CLUT** Configures BLEND background layer CLUT access in FIFO mode. (R/W)

Register 33.2. PPA\_BLEND1\_CLUT\_DATA\_REG (0x0004)



**PPA\_RDWR\_WORD\_BLEND1\_CLUT** Configures BLEND foreground layer CLUT access in FIFO mode. (R/W)

## Register 33.3. PPA\_CLUT\_CONF\_REG (0x000C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |       |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|-------|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PPA_BLEND0_CLUT_MEM_CLK_ENA<br>PPA_BLEND0_CLUT_MEM_FORCE_PU<br>PPA_BLEND0_CLUT_MEM_FORCE_PD<br>PPA_BLEND1_CLUT_MEM_RDADDR_RST<br>PPA_BLEND1_CLUT_MEM_RST<br>PPA_BLEND0_CLUT_MEM_RST<br>PPA_APB_FIFO_MASK |   |   |   |   |       |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8 | 7  | 6 | 5 | 4 | 3 | 2     | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | Reset |   |   |  |  |

**PPA\_APB\_FIFO\_MASK** Configures the access mode of BLEND CLUT

1'b0: Access CLUT in FIFO mode. For details, please refer to [33.5.1.2](#).

1'b1: Access CLUT in MEM mode. For details, please refer to [33.5.1.2](#).

(R/W)

**PPA\_BLEND0\_CLUT\_MEM\_RST** Configures whether to reset BLEND0 CLUT.

0: Release reset

1: Reset

(R/W)

**PPA\_BLEND1\_CLUT\_MEM\_RST** Configures whether to reset BLEND1 CLUT.

0: Release reset

1: Reset

(R/W)

**PPA\_BLEND0\_CLUT\_MEM\_RDADDR\_RST** Configures whether to reset BLEND0 CLUT read address in FIFO mode.

0: Release reset

1: Reset

(R/W)

**PPA\_BLEND1\_CLUT\_MEM\_RDADDR\_RST** Configures whether to reset BLEND1 CLUT read address in FIFO mode.

0: Release reset

1: Reset

(R/W)

**PPA\_BLEND\_CLUT\_MEM\_FORCE\_PD** Configures whether to enable the force power down of BLEND CLUT.

0: Disable

1: Enable

(R/W)

Continued on the next page...



**Register 33.3. PPA\_CLUT\_CONF\_REG (0x000C)**

Continued from the previous page...

**PPA\_BLEND\_CLUT\_MEM\_FORCE\_PU** Configures whether to enable the force power up of BLEND CLUT.

0: Disable

1: Enable

(R/W)

**PPA\_BLEND\_CLUT\_MEM\_CLK\_ENA** Configures whether to enable the force clock on of BLEND CLUT.

0: Disable

1: Enable

(R/W)

Register 33.4. PPA\_SRM\_COLOR\_MODE\_REG (0x0020)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |   |   |                      |    |   |   |                  |   |   |       |                  |   |   |  |               |  |  |  |               |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|---|---|---|----------------------|----|---|---|------------------|---|---|-------|------------------|---|---|--|---------------|--|--|--|---------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PPA_RGB2YUV_PROTOCOL |   |   |   | PPA_YUV2RGB_PROTOCOL |    |   |   | PPA_YUV_TX_RANGE |   |   |       | PPA_YUV_RX_RANGE |   |   |  | PPA_SRM_TX_CM |  |  |  | PPA_SRM_RX_CM |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 12                   |   |   |   | 11                   | 10 | 9 | 8 | 7                | 4 |   |       |                  | 3 | 0 |  |               |  |  |  |               |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0                    | 0  | 0 | 0 | 0                | 0 | 0 | Reset |                  |   |   |  |               |  |  |  |               |  |  |  |

**PPA\_SRM\_RX\_CM** Configures the input image color format for SRM.

- 0: ARGB8888
  - 1: RGB888
  - 2: RGB565
  - 8: YUV420
  - Others: Reserved
- (R/W)

**PPA\_SRM\_TX\_CM** Configures the output image color format for SRM.

- 0: ARGB8888
  - 1: RGB888
  - 2: RGB565
  - 8: YUV420
  - Others: Reserved
- (R/W)

**PPA\_YUV\_RX\_RANGE** Configures the YUV range when the SRM input format is YUV.

- 0: limit range
  - 1: full range
- (R/W)

**PPA\_YUV\_TX\_RANGE** Configures the YUV range when the SRM output format is YUV.

- 0: limit range
  - 1: full range
- (R/W)

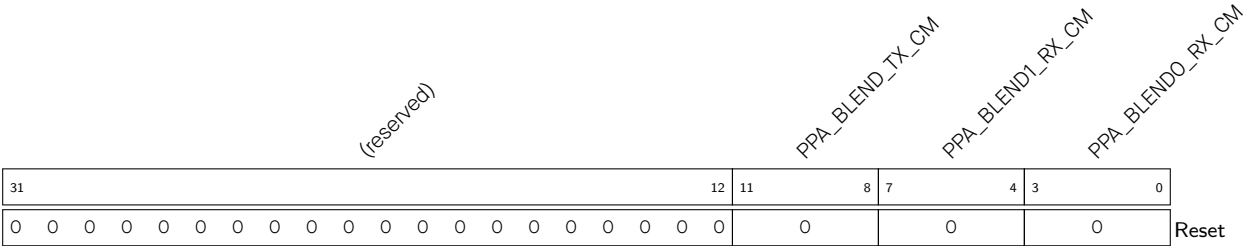
**PPA\_YUV2RGB\_PROTOCOL** Configures the protocol used for the SRM input direction YUV to RGB.

- 0: BT601
  - 1: BT709
- (R/W)

**PPA\_RGB2YUV\_PROTOCOL** Configures the protocol used for the SRM output direction RGB to YUV.

- 0: BT601
  - 1: BT709
- (R/W)

Register 33.5. PPA\_BLEND\_COLOR\_MODE\_REG (0x0024)



**PPA\_BLEND0\_RX\_CM** Configures the input image color format for BLEND background layer.

- 0: ARGB8888
- 1: RGB888
- 2: RGB565
- 4: L8
- 5: L4
- Others: Reserved

(R/W)

**PPA\_BLEND1\_RX\_CM** Configures the input image color format for BLEND foreground layer.

- 0: ARGB8888
- 1: RGB888
- 2: RGB565
- 4: L8
- 5: L4
- 6: A8
- 7: A4
- Others: Reserved

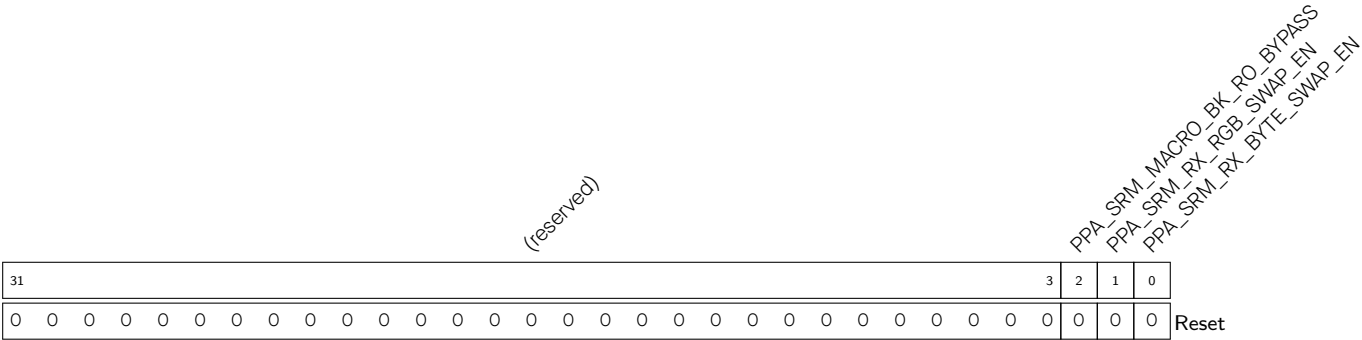
(R/W)

**PPA\_BLEND\_TX\_CM** Configures the output image color format of BLEND.

- 0: ARGB8888
- 1: RGB888
- 2: RGB565
- Others: Reserved

(R/W)

Register 33.6. PPA\_SRM\_BYTE\_ORDER\_REG (0x0028)



**PPA\_SRM\_RX\_BYTE\_SWAP\_EN** Configures whether to swap the SRM valid data input in byte.

0: Not swap

1: Swap

(R/W)

**PPA\_SRM\_RX\_RGB\_SWAP\_EN** Configures whether to swap the order of each channel when the SRM input is RGB or ARGB.

0: Not swap

1: Swap RGB to BGR, and ARGB to BGRA

(R/W)

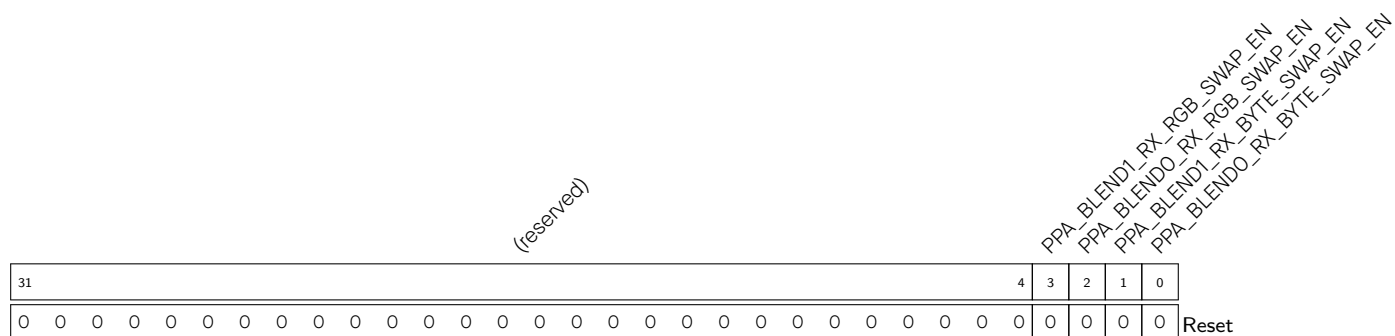
**PPA\_SRM\_MACRO\_BK\_RO\_BYPASS** Configures whether to enable the pixel block order function

0: Enable and automatically calculate if the current block needs to be reordered

1: Disable

(R/W)

### Register 33.7. PPA\_BLEND\_BYTE\_ORDER\_REG (0x002C)



|                            |   |
|----------------------------|---|
| PPA_BLEND0_RX_BYTE_SWAP_EN | Configures whether to swap the BLEND background layer valid data input in byte. |
|----------------------------|---|

0: Not swap

1: Swap

(R/W)

**PPA\_BLEND1\_RX\_BYTE\_SWAP\_EN** Configures whether to swap the BLEND foreground layer valid data input in byte.

0: Not swap

1: Swap

(R/W)

**PPA\_BLEND0\_RX\_RGB\_SWAP\_EN** Configures whether to swap the order of each channel when the BLEND background layer input is RGB or ARGB.

0: Not swap

### 1: Swap RGB to BGR, and ARGB to BGRA

(R/W)

**PPA\_BLEND1\_RX\_RGB\_SWAP\_EN** Configures whether to swap the order of each channel when the BLEND foreground layer input is RGB or ARGB.

0: Not swap

1: Swap RGB to BGR, and ARGB to BGRA

(R/W)

### Register 33.8. PPA\_BLEND\_TRANS\_MODE\_REG (0x0034)

[illegible]

**PPA\_BLEND\_EN** Configures whether to enable BLEND.

0: Disable

1: Enable

(R/W)

**PPA\_BLEND\_BYPASS** Configures whether to bypass BLEND and directly output the background layer.

0: Bypass

1: Not bypass

(R/W)

**PPA\_BLEND\_FIX\_PIXEL\_FILL\_EN** Configures whether to enable filled image output.

0: Disable

1: Enable, where only BLEND TX works and the output pixel and size are configured by `PPA_BLEND_TX_SIZE_REG` and `PPA_BLEND_TX_FIX_PIXEL`.

(R/W)

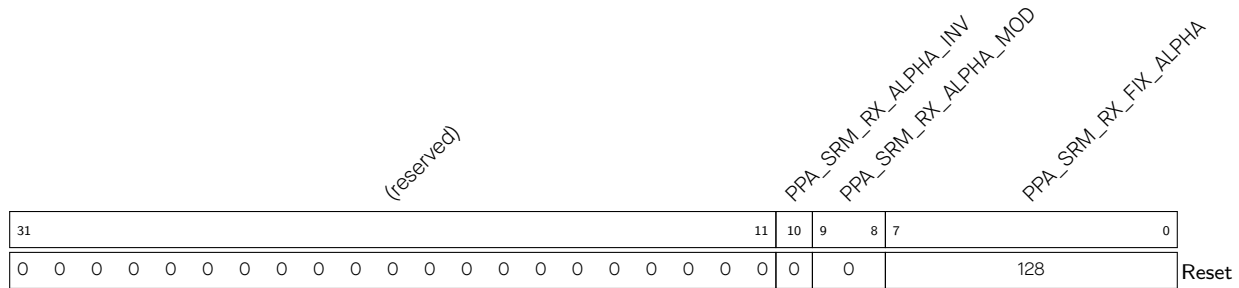
PPA\_BLEND\_TRANS\_MODE\_UPDATE Write 1 to update the transfer mode, active  
PPA\_BLEND\_FIX\_PIXEL\_FILL\_EN, and start BLEND workflow. (WT)

**A\_BLEND\_RST** Configures whether to reset BLEND.

0: Release reset

1: Reset

(R/W)

**Register 33.9. PPA\_SRM\_FIX\_ALPHA\_REG (0x0038)**

**PPA\_SRM\_RX\_FIX\_ALPHA** Configures the Alpha channel value of SRM. (R/W)

**PPA\_SRM\_RX\_ALPHA\_MOD** Configures the Alpha mode of SRM input data.

1: Use the value of [PPA\\_SRM\\_RX\\_FIX\\_ALPHA](#)

2: Use the value of the higher eight bits of the original Alpha value multiplied by [PPA\\_SRM\\_RX\\_FIX\\_ALPHA](#)

Others: Use the value of the original Alpha value

(R/W)

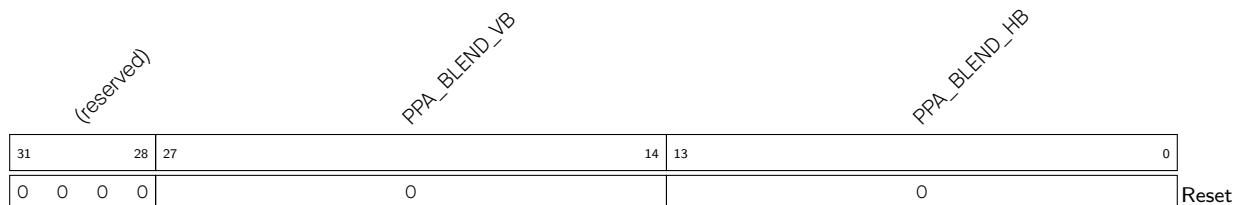
**PPA\_SRM\_RX\_ALPHA\_INV** Configures whether to invert the original Alpha value of SRM.

0: Not invert

1: Invert to 255 minus the original Alpha value

For data formats without Alpha channels, the original Alpha value is 255.

(R/W)

**Register 33.10. PPA\_BLEND\_TX\_SIZE\_REG (0x003C)**

**PPA\_BLEND\_HB** Configures the horizontal width of image block that would be filled in the image filling mode. Measurement unit: pixel. (R/W)

**PPA\_BLEND\_VB** Configures the vertical width of image block that would be filled in the image filling mode. Measurement unit: pixel. (R/W)

### Register 33.11. PPA\_BLEND\_FIX\_ALPHA\_REG (0x0040)

|                       |  |  |  |  |  |  |  |  |  |  |                         |    |    |    |                         |     |    |    |                         |  |     |       |                         |   |  |  |                         |  |  |  |                         |  |  |  |
|-----------------------|--|--|--|--|--|--|--|--|--|--|-------------------------|----|----|----|-------------------------|-----|----|----|-------------------------|--|-----|-------|-------------------------|---|--|--|-------------------------|--|--|--|-------------------------|--|--|--|
| (reserved)            |  |  |  |  |  |  |  |  |  |  | PPA_BLEND1_RX_ALPHA_INV |    |    |    | PPA_BLEND0_RX_ALPHA_INV |     |    |    | PPA_BLEND1_RX_ALPHA_MOD |  |     |       | PPA_BLEND0_RX_ALPHA_MOD |   |  |  | PPA_BLEND1_RX_FIX_ALPHA |  |  |  | PPA_BLEND0_RX_FIX_ALPHA |  |  |  |
| 31                    |  |  |  |  |  |  |  |  |  |  | 22                      | 21 | 20 | 19 | 18                      | 17  | 16 | 15 | 8                       |  |     |       | 7                       | 0 |  |  |                         |  |  |  |                         |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  | 0                       | 0  | 0  | 0  | 0                       | 128 |    |    |                         |  | 128 | Reset |                         |   |  |  |                         |  |  |  |                         |  |  |  |

**PPA\_BLEND0\_RX\_FIX\_ALPHA** Configures the Alpha channel value of the BLEND background layer.  
(R/W)

|                         |  |
|-------------------------|--|
| PPA_BLEND1_RX_FIX_ALPHA | Configures the Alpha channel value of the BLEND foreground layer.<br>(R/W) |
|-------------------------|--|

**PPA\_BLEND0\_RX\_ALPHA\_MOD** Configures the Alpha mode of BLEND background layer data.

- 1: Use the value of `PPA_BLEND0_RX_FIX_ALPHA`
- 2: Use the value of the higher eight bits of the original Alpha value multiplied by `PPA_BLEND0_RX_FIX_ALPHA`
- Others: Use the value of the original Alpha value

(R/W)

**PPA\_BLEND1\_RX\_ALPHA\_MOD** Configures the Alpha mode of BLEND foreground layer data.

- 1: Use the value of `PPA_BLEND1_RX_FIX_ALPHA`
- 2: Use the value of the higher eight bits of the original Alpha value multiplied by `PPA_BLEND1_RX_FIX_ALPHA`
- Others: Use the value of the original Alpha value

(R/W)

**PPA\_BLEND0\_RX\_ALPHA\_INV** Configures whether to invert the original Alpha value of the BLEND background layer data.

- 0: Not invert  
1: Invert to 255 minus the original Alpha value

For data formats without Alpha channels, the original Alpha value is 255.

(R/W)

**PPA\_BLEND1\_RX\_ALPHA\_INV** Configures whether to invert the original Alpha value of the BLEND foreground layer data.

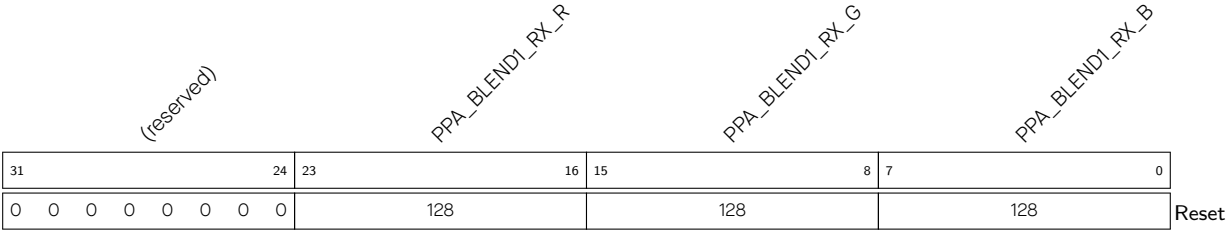
- 0: Not invert  
1: Invert to 255 minus the original Alpha value

For data formats without Alpha channels, the original Alpha value is 255.

(R/W)



Register 33.12. PPA\_BLEND\_RGB\_REG (0x0048)

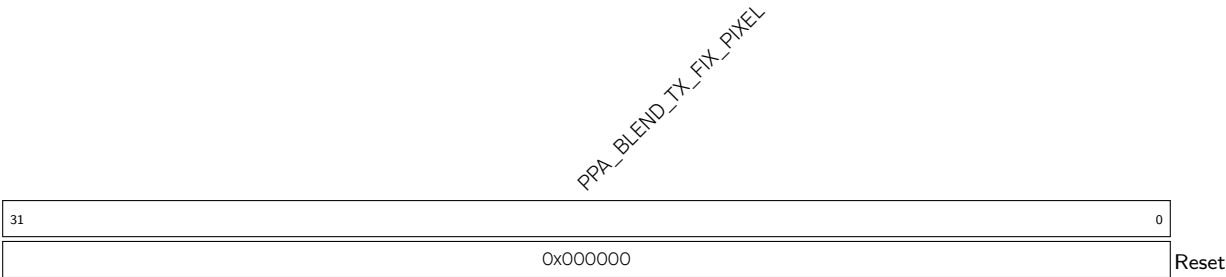


**PPA\_BLEND1\_RX\_B** Configures the B channel value when the BLEND foreground layer is in A4/A8.  
(R/W)

**PPA\_BLEND1\_RX\_G** Configures the G channel value when the BLEND foreground layer is in A4/A8.  
(R/W)

**PPA\_BLEND1\_RX\_R** Configures the R channel value when the BLEND foreground layer is in A4/A8.  
(R/W)

Register 33.13. PPA\_BLEND\_FIX\_PIXEL\_REG (0x004C)



**PPA\_BLEND\_TX\_FIX\_PIXEL** Configures the pixel in the BLEND image filling mode.  
[31:24]: A, [23:16]:R, [15:8]: G, [7:0]: B.  
(R/W)

Register 33.14. PPA\_CK\_FG\_LOW\_REG (0x0050)

|            |    |    |    |    |   |   |   |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |
|------------|----|----|----|----|---|---|---|-----------------------|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |   |   |   | PPA_COLORKEY_FG_R_LOW |  |  |  |  |  |  |  | PPA_COLORKEY_FG_G_LOW |  |  |  |  |  |  |  | PPA_COLORKEY_FG_B_LOW |  |  |  |  |  |  |  |
| 31         | 24 | 23 | 16 | 15 | 8 | 7 | 0 |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0xff                  |  |  |  |  |  |  |  | 0xff                  |  |  |  |  |  |  |  | 0xff                  |  |  |  |  |  |  |  |

Reset

**PPA\_COLORKEY\_FG\_B\_LOW** Configures the color-key lower threshold of the B channel value of the BLEND foreground layer. (R/W)

**PPA\_COLORKEY\_FG\_G\_LOW** Configures the color-key lower threshold of the G channel value of the BLEND foreground layer. (R/W)

**PPA\_COLORKEY\_FG\_R\_LOW** Configures the color-key lower threshold of the R channel value of the BLEND foreground layer. (R/W)

Register 33.15. PPA\_CK\_FG\_HIGH\_REG (0x0054)

|            |    |    |    |    |   |   |   |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |
|------------|----|----|----|----|---|---|---|------------------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |   |   |   | PPA_COLORKEY_FG_R_HIGH |  |  |  |  |  |  |  | PPA_COLORKEY_FG_G_HIGH |  |  |  |  |  |  |  | PPA_COLORKEY_FG_B_HIGH |  |  |  |  |  |  |  |
| 31         | 24 | 23 | 16 | 15 | 8 | 7 | 0 |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0x0                    |  |  |  |  |  |  |  | 0x0                    |  |  |  |  |  |  |  | 0x0                    |  |  |  |  |  |  |  |

Reset

**PPA\_COLORKEY\_FG\_B\_HIGH** Configures the color-key higher threshold of the B channel value of the BLEND foreground layer. (R/W)

**PPA\_COLORKEY\_FG\_G\_HIGH** Configures the color-key higher threshold of the G channel value of the BLEND foreground layer. (R/W)

**PPA\_COLORKEY\_FG\_R\_HIGH** Configures the color-key higher threshold of the R channel value of the BLEND foreground layer. (R/W)

Register 33.16. PPA\_CK\_BG\_LOW\_REG (0x0058)

|            |    |    |    |    |   |   |   |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |
|------------|----|----|----|----|---|---|---|-----------------------|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |   |   |   | PPA_COLORKEY_BG_R_LOW |  |  |  |  |  |  |  | PPA_COLORKEY_BG_G_LOW |  |  |  |  |  |  |  | PPA_COLORKEY_BG_B_LOW |  |  |  |  |  |  |  |
| 31         | 24 | 23 | 16 | 15 | 8 | 7 | 0 |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0xff                  |  |  |  |  |  |  |  | 0xff                  |  |  |  |  |  |  |  | 0xff                  |  |  |  |  |  |  |  |

Reset

**PPA\_COLORKEY\_BG\_B\_LOW** Configures the color-key lower threshold of the B channel value of the BLEND background layer. (R/W)

**PPA\_COLORKEY\_BG\_G\_LOW** Configures the color-key lower threshold of the G channel value of the BLEND background layer. (R/W)

**PPA\_COLORKEY\_BG\_R\_LOW** Configures the color-key lower threshold of the R channel value of the BLEND background layer. (R/W)

Register 33.17. PPA\_CK\_BG\_HIGH\_REG (0x005C)

|            |    |    |    |    |   |   |   |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |
|------------|----|----|----|----|---|---|---|------------------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|
| (reserved) |    |    |    |    |   |   |   | PPA_COLORKEY_BG_R_HIGH |  |  |  |  |  |  |  | PPA_COLORKEY_BG_G_HIGH |  |  |  |  |  |  |  | PPA_COLORKEY_BG_B_HIGH |  |  |  |  |  |  |  |
| 31         | 24 | 23 | 16 | 15 | 8 | 7 | 0 |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0x0                    |  |  |  |  |  |  |  | 0x0                    |  |  |  |  |  |  |  | 0x0                    |  |  |  |  |  |  |  |

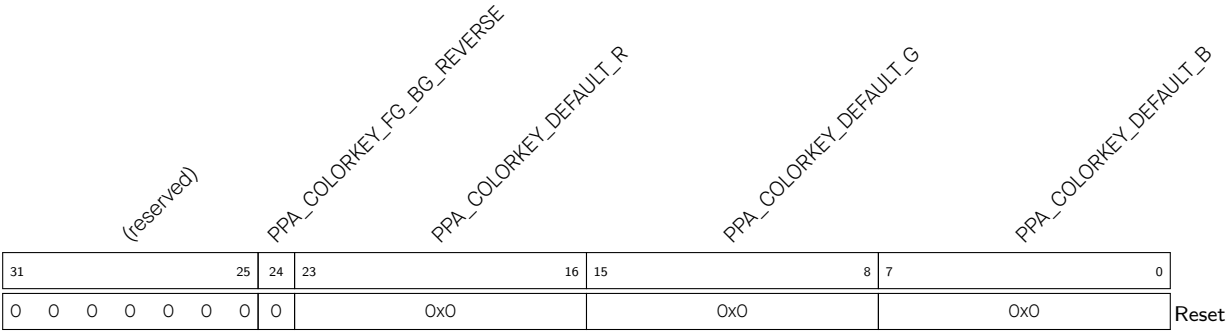
Reset

**PPA\_COLORKEY\_BG\_B\_HIGH** Configures the color-key higher threshold of the B channel value of the BLEND background layer. (R/W)

**PPA\_COLORKEY\_BG\_G\_HIGH** Configures the color-key higher threshold of the G channel value of the BLEND background layer. (R/W)

**PPA\_COLORKEY\_BG\_R\_HIGH** Configures the color-key higher threshold of the R channel value of the BLEND background layer. (R/W)

Register 33.18. PPA\_CK\_DEFAULT\_REG (0x0060)



**PPA\_COLORKEY\_DEFAULT\_B** Configures the default B channel value of BLEND color-key. (R/W)

**PPA\_COLORKEY\_DEFAULT\_G** Configures the default G channel value of BLEND color-key. (R/W)

**PPA\_COLORKEY\_DEFAULT\_R** Configures the default R channel value of BLEND color-key. (R/W)

**PPA\_COLORKEY\_FG\_BG\_REVERSE** Configures the workflow when when a pixel is within the back-ground color-key range but not within the foreground color-key range.  
0: Output background pixel  
1: Output foreground pixel  
(R/W)

**Register 33.19. PPA\_SRM\_SCAL\_ROTATE\_REG (0x0064)**

|   |    |    |    |    |    |    |    |    |    |   |  |  |  |    |    |  |  |  |  |    |   |  |  |   |       |  |  |  |  |  |  |  |  |  |
|---|----|----|----|----|----|----|----|----|----|---|--|--|--|----|----|--|--|--|--|----|---|--|--|---|-------|--|--|--|--|--|--|--|--|--|
| <div>(reserved)</div> <div>PPA_SRM_MIRROR_Y</div> <div>PPA_SRM_MIRROR_X</div> <div>PPA_SCAL_ROTATE_START</div> <div>PPA_SCAL_ROTATE_RST</div> <div>PPA_SRM_ROTATE_ANGLE</div> <div>PPA_SRM_SCAL_Y_FRAG</div> <div>PPA_SRM_SCAL_Y_INT</div> <div>PPA_SRM_SCAL_X_FRAG</div> <div>PPA_SRM_SCAL_X_INT</div> |    |    |    |    |    |    |    |    |    |   |  |  |  |    |    |  |  |  |  |    |   |  |  |   |       |  |  |  |  |  |  |  |  |  |
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 20 |   |  |  |  | 19 | 12 |  |  |  |  | 11 | 8 |  |  | 7 | 0     |  |  |  |  |  |  |  |  |  |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |    | 1 |  |  |  |    | 0  |  |  |  |  | 1  |   |  |  |   | Reset |  |  |  |  |  |  |  |  |  |

Reset

**PPA\_SRM\_SCAL\_X\_INT** Configures the integer part of the horizontal scaling factor for SRM. (R/W)

**PPA\_SRM\_SCAL\_X\_FRAG** Configures the fragment part of the horizontal scaling factor for SRM. (R/W)

**PPA\_SRM\_SCAL\_Y\_INT** Configures the integer part of the vertical scaling factor for SRM. (R/W)

**PPA\_SRM\_SCAL\_Y\_FRAG** Configures the fragment part of the vertical scaling factor for SRM. (R/W)

**PPA\_SRM\_ROTATE\_ANGLE** Configures the counterclockwise rotation angle for the SRM.

- 0: 0 degree
  - 1: 90 degree
  - 2: 180 degree
  - 3: 270 degree
- (R/W)

**PPA\_SCAL\_ROTATE\_RST** Configures whether to reset SRM.

- 0: Release reset
  - 1: Reset
- (R/W)

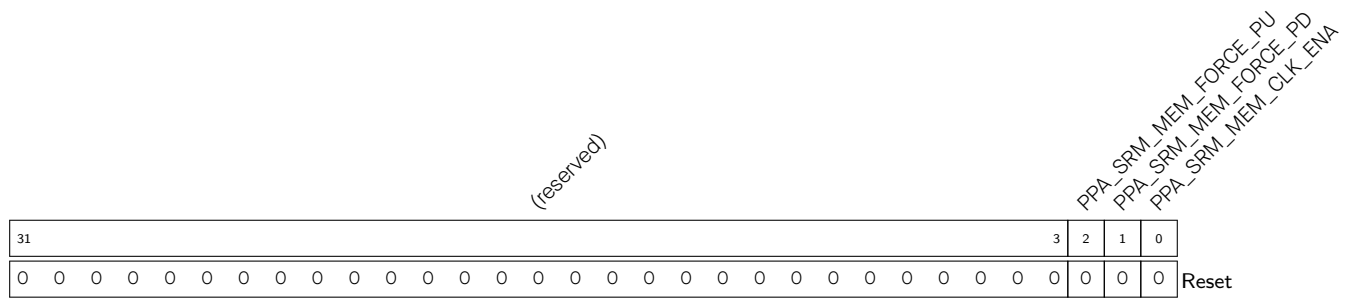
**PPA\_SCAL\_ROTATE\_START** Write 1 to enable SRM. (WT)

**PPA\_SRM\_MIRROR\_X** Configures whether to enable the horizontal mirroring for SRM.

- 0: Disable
  - 1: Enable
- (R/W)

**PPA\_SRM\_MIRROR\_Y** Configures whether to enable the vertical mirroring for SRM.

- 0: Disable
  - 1: Enable
- (R/W)

**Register 33.20. PPA\_SRM\_MEM\_PD\_REG (0x0068)**

**PPA\_SRM\_MEM\_CLK\_ENA** Configures whether to enable the force enable of the SRM MEM clock.

0: Disable

1: Enable

(R/W)

**PPA\_SRM\_MEM\_FORCE\_PD** Configures whether to enable the force power down of SRM MEM.

0: Disable

1: Enable

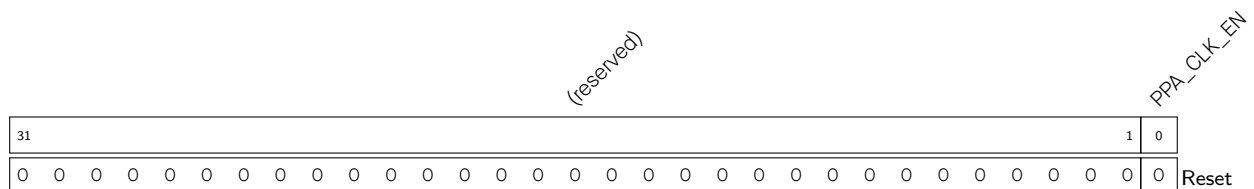
(R/W)

**PPA\_SRM\_MEM\_FORCE\_PU** Configures whether to enable the force power up of SRM MEM.

0: Disable

1: Enable

(R/W)

**Register 33.21. PPA\_REG\_CONF\_REG (0x006C)**

**PPA\_CLK\_EN** Configures whether to keep the PPA register clock always on.

0: Clock only turns on when there's a register access

1: Clock always on

(R/W)

**Register 33.22. PPA\_INT\_RAW\_REG (0x0010)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PPA_SRM_PARAM_CFG_ERR_INT_RAW<br>PPA_BLEND_EOF_INT_RAW<br>PPA_SRM_EOF_INT_RAW |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3   | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | Reset |

**PPA\_SRM\_EOF\_INT\_RAW** The raw interrupt status of PPA SRM EOF.

0: No PPA SRM EOF occurred

1: PPA SRM EOF occurred

(R/WTC/SS)

**PPA\_BLEND\_EOF\_INT\_RAW** The raw interrupt status of PPA BLEND EOF.

0: No PPA BLEND EOF occurred

1: PPA BLEND EOF occurred

(R/WTC/SS)

**PPA\_SRM\_PARAM\_CFG\_ERR\_INT\_RAW** The raw interrupt status of PPA SRM parameter error.

Check [PPA\\_SRM\\_PARAM\\_ERR\\_ST\\_REG](#) to get the specific error.

0: No PPA SRM parameter error occurred

1: PPA SRM parameter error occurred

(R/WTC/SS)

**Register 33.23. PPA\_INT\_ST\_REG (0x0014)**

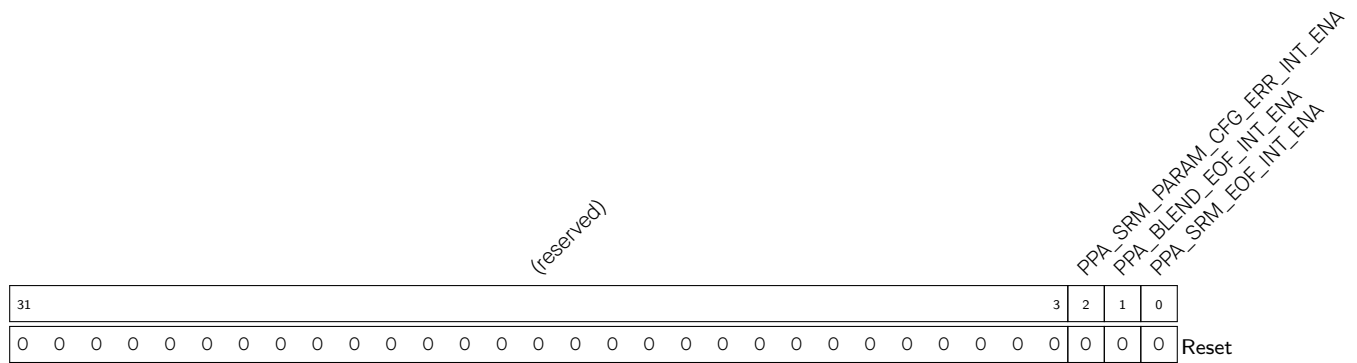
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PPA_SRM_PARAM_CFG_ERR_INT_ST<br>PPA_BLEND_EOF_INT_ST<br>PPA_SRM_EOF_INT_ST |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | Reset |

**PPA\_SRM\_EOF\_INT\_ST** The masked interrupt status of PPA\_SRM\_EOF\_INT. (RO)

**PPA\_BLEND\_EOF\_INT\_ST** The masked interrupt status of PPA\_BLEND\_EOF\_INT. (RO)

**PPA\_SRM\_PARAM\_CFG\_ERR\_INT\_ST** The masked interrupt status of PPA\_SRM\_PARAM\_CFG\_ERR\_INT. (RO)

## Register 33.24. PPA\_INT\_ENA\_REG (0x0018)



**PPA\_SRM\_EOF\_INT\_ENA** Configures whether to enable the maskable interrupt PPA\_SRM\_EOF\_INT.

0: Not trigger the PPA interrupt

1: Trigger the PPA interrupt

(R/W)

**PPA\_BLEND\_EOF\_INT\_ENA** Configures whether to enable the maskable interrupt PPA\_BLEND\_EOF\_INT.

0: Not trigger the PPA interrupt

1: Trigger the PPA interrupt

(R/W)

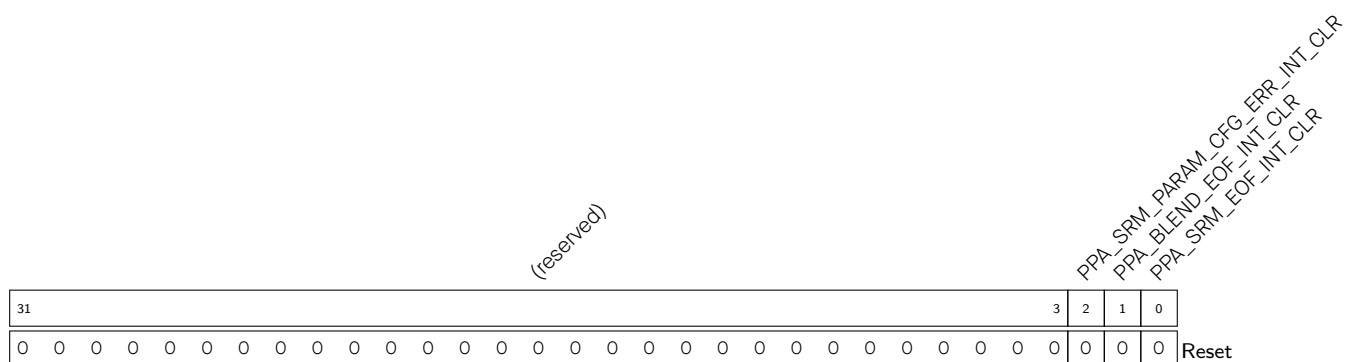
**PPA\_SRM\_PARAM\_CFG\_ERR\_INT\_ENA** Configures whether to enable the maskable interrupt PPA\_SRM\_RX\_YSCAL\_ERR\_INT.

0: Not trigger the PPA interrupt

1: Trigger the PPA interrupt

(R/W)

## Register 33.25. PPA\_INT\_CLR\_REG (0x001C)



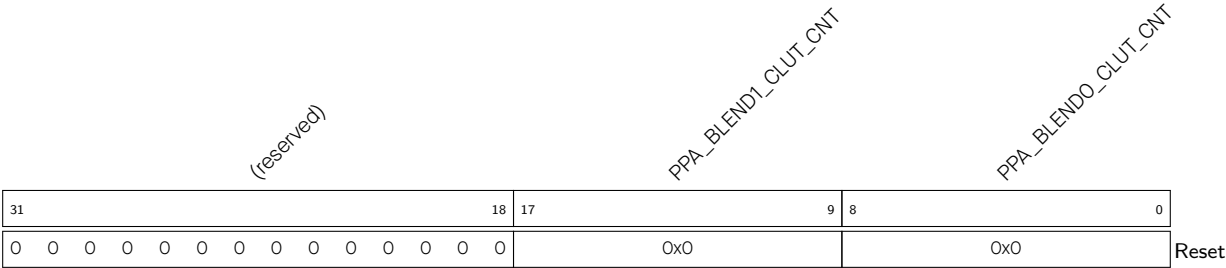
**PPA\_SRM\_EOF\_INT\_CLR** Write 1 to clear [PPA\\_SRM\\_EOF\\_INT\\_RAW](#). (WT)

**PPA\_BLEND\_EOF\_INT\_CLR** Write 1 to clear [PPA\\_BLEND\\_EOF\\_INT\\_RAW](#). (WT)

**PPA\_SRM\_PARAM\_CFG\_ERR\_INT\_CLR** Write 1 to clear [PPA\\_SRM\\_PARAM\\_CFG\\_ERR\\_INT\\_RAW](#). (WT)



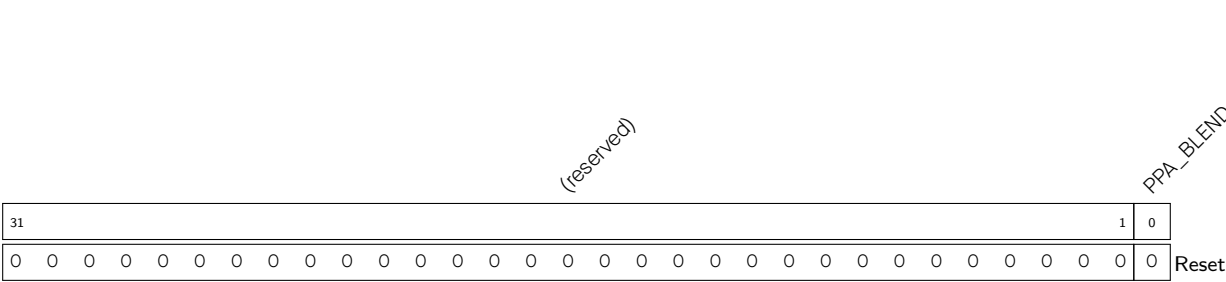
Register 33.26. PPA\_CLUT\_CNT\_REG (0x0070)



**PPA\_BLEND0\_CLUT\_CNT** Represents the current write address of the BLEND background layer CLUT in FIFO mode. (RO)

**PPA\_BLEND1\_CLUT\_CNT** Represents the current write address of the BLEND foreground layer CLUT in FIFO mode. (RO)

Register 33.27. PPA\_BLEND\_ST\_REG (0x0074)



**PPA\_BLEND\_SIZE\_DIFF\_ST** Represents whether the size of the BLEND background and foreground images are consistent.

0: Consistent

1: Different

(RO)

Register 33.28. PPA\_SRM\_PARAM\_ERR\_ST\_REG (0x0078)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PPA_Y_YUV420_TX_SCALE_ERR_ST<br>PPA_X_YUV420_TX_SCALE_ERR_ST<br>PPA_Y_YUV420_RX_SCALE_ERR_ST<br>PPA_X_YUV420_RX_SCALE_ERR_ST<br>PPA_XDST_LEN_TOO_LARGE_ERR_ST<br>PPA_XDST_LEN_TOO_SAMLL_ERR_ST<br>PPA_RX_DSCR_HB_ERR_ST<br>PPA_X_RX_SCAL_EQUAL_O_ERR_ST<br>PPA_YDST_LEN_TOO_LARGE_ERR_ST<br>PPA_YDST_LEN_TOO_SAMLL_ERR_ST<br>PPA_Y_RX_DSCR_VB_ERR_ST<br>PPA_TX_DSCR_HB_ERR_ST<br>PPA_TX_DSCR_VB_ERR_ST |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 14   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |       |

**PPA\_TX\_DSCR\_VB\_ERR\_ST** Represents whether the vertical size of the SRM output image block plus the vertical offset Y configured in the output list exceeds the vertical size of the entire image configured in the output list, VA.

0: Not exceeded

1: Exceeded

(RO)

**PPA\_TX\_DSCR\_HB\_ERR\_ST** Represents whether the horizontal size of the SRM output image block plus the vertical offset X configured in the output list exceeds the horizontal size of the entire image configured in the output list, HA.

0: Not exceeded

1: Exceeded

(RO)

**PPA\_Y\_RX\_SCAL\_EQUAL\_O\_ERR\_ST** Represents whether the vertical direction scaling factor of the SRM input image block is 0.

0: Not 0

1: 0

(RO)

**PPA\_RX\_DSCR\_VB\_ERR\_ST** Represents whether the sum of the vertical direction image block size VB configured in the SRM input list and the vertical offset Y exceeds the entire image's vertical size VA.

0: Not exceeded

1: Exceeded

(RO)

**PPA\_YDST\_LEN\_TOO\_SAMLL\_ERR\_ST** Represents whether the vertical size of the image block after scaling in the SRM is 0.

0: Not 0

1: 0

(RO)

Continued on the next page...

**Register 33.28. PPA\_SRM\_PARAM\_ERR\_ST\_REG (0x0078)**

Continued from the previous page...

**PPA\_YDST\_LEN\_TOO\_LARGE\_ERR\_ST** Represents whether the vertical size of the image block after scaling in the SRM is larger than 8191.

0: Within 8191

1: Larger than 8191

(RO)

**PPA\_X\_RX\_SCAL\_EQUAL\_O\_ERR\_ST** Represents whether the horizontal direction scaling factor of the SRM input image block is 0.

0: Not 0

1: 0

(RO)

**PPA\_RX\_DSCR\_HB\_ERR\_ST** Represents whether the sum of the horizontal direction image block size HB configured in the SRM input list and the horizontal offset X exceeds the entire image's horizontal size HA.

0: Not exceeded

1: Exceeded

(RO)

**PPA\_XDST\_LEN\_TOO\_SAMLL\_ERR\_ST** Represents whether the horizontal size of the image block after scaling in the SRM is 0.

0: Not 0

1: 0

(RO)

**PPA\_XDST\_LEN\_TOO\_LARGE\_ERR\_ST** Represents whether the horizontal size of the image block after scaling in the SRM is larger than 8191.

0: Within 8191

1: Larger than 8191

(RO)

**PPA\_X\_YUV420\_RX\_SCALE\_ERR\_ST** Represents whether the parameters HA/HB/X of the SRM input list are odd when the input format is YUV420.

0: Even

1: Odd

(RO)

**PPA\_Y\_YUV420\_RX\_SCALE\_ERR\_ST** Represents whether the parameters VA/VB/Y of the SRM input list are odd when the input format is YUV420.

0: Even

1: Odd

(RO)

Continued on the next page...

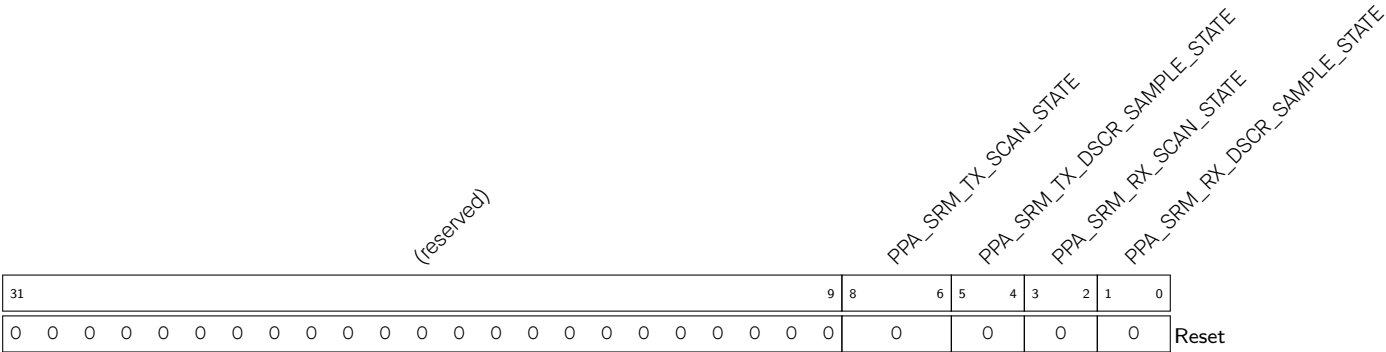
Register 33.28. PPA\_SRM\_PARAM\_ERR\_ST\_REG (0x0078)

Continued from the previous page...

**PPA\_X\_YUV420\_TX\_SCALE\_ERR\_ST** Represents whether the parameters HA/HB/X of the SRM output list are odd when the output format is YUV420.  
0: Even  
1: Odd  
(RO)

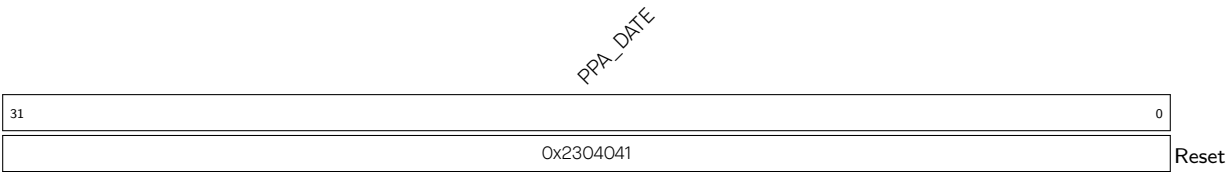
**PPA\_Y\_YUV420\_TX\_SCALE\_ERR\_ST** Represents whether the parameters VA/VB/Y of the SRM output list are odd when the output format is YUV420.  
0: Even  
1: Odd  
(RO)

Register 33.29. PPA\_SRM\_STATUS\_REG (0x007C)



**PPA\_SRM\_RX\_DSCR\_SAMPLE\_STATE** Reserved. (RO)  
**PPA\_SRM\_RX\_SCAN\_STATE** Reserved. (RO)  
**PPA\_SRM\_TX\_DSCR\_SAMPLE\_STATE** Reserved. (RO)  
**PPA\_SRM\_TX\_SCAN\_STATE** Reserved. (RO)

Register 33.30. PPA\_DATE\_REG (0x0100)



**PPA\_DATE** Version control register. (R/W)

## Chapter 34

# LCD and Camera Controller (LCD\_CAM)

## 34.1 Overview

The LCD and Camera controller (LCD\_CAM) on the ESP32-P4, consisting of an independent LCD control module and a camera control module, is a versatile component designed to facilitate interfacing with both LCDs and cameras.

The LCD module provides an LCD interface that can connect to RGB, Motorola 6800 (MOTO6800), and Intel 8080 (I8080) compatible LCD devices. The LCD module is responsible for sending video data to the display.

The Camera module provides one parallel camera interface that can connect to external digital video port (DVP) cameras in 8/16-bit modes. It manages communication with the camera to capture images or video frames.

The LCD\_CAM controller offers flexibility for projects that involve both displaying information on screens and working with cameras for image or video processing.

## 34.2 Features

LCD\_CAM has the following features:

- Supports the following operation modes:
  - LCD master TX mode
  - Camera slave RX mode
  - Camera master RX mode
- Supports simultaneous connection to an external LCD and a camera
- When interfacing with an external LCD, the following is supported:
  - 8/16/24-bit parallel output modes
  - RGB, MOTO6800, and I8080 LCD formats
  - LCD data retrieved from internal memory or external memory via GDMA
- When interfacing with an external camera (i.e., DVP image sensor), the following is supported:
  - 8/16-bit parallel input modes
  - Camera data stored in internal or external memory via GDMA
- Supports interrupts

## 34.3 Functional Description

### 34.3.1 Block Diagram

Figure 34.3-1 shows the structure of LCD\_CAM which includes:

- One TX control unit (LCD\_Ctrl)
- One RX control unit (Camera\_Ctrl)
- One asynchronous TX FIFO (Async TX FIFO) for communicating with external devices, e.g., LCDs
- One asynchronous RX FIFO (Async RX FIFO) for communicating with external devices, e.g., cameras
- Two clock generators (LCD\_Clock Generator and CAM\_Clock Generator) for generating clocks for each module
- Two format converters (RGB/YUV Converter) for converting video data into various formats

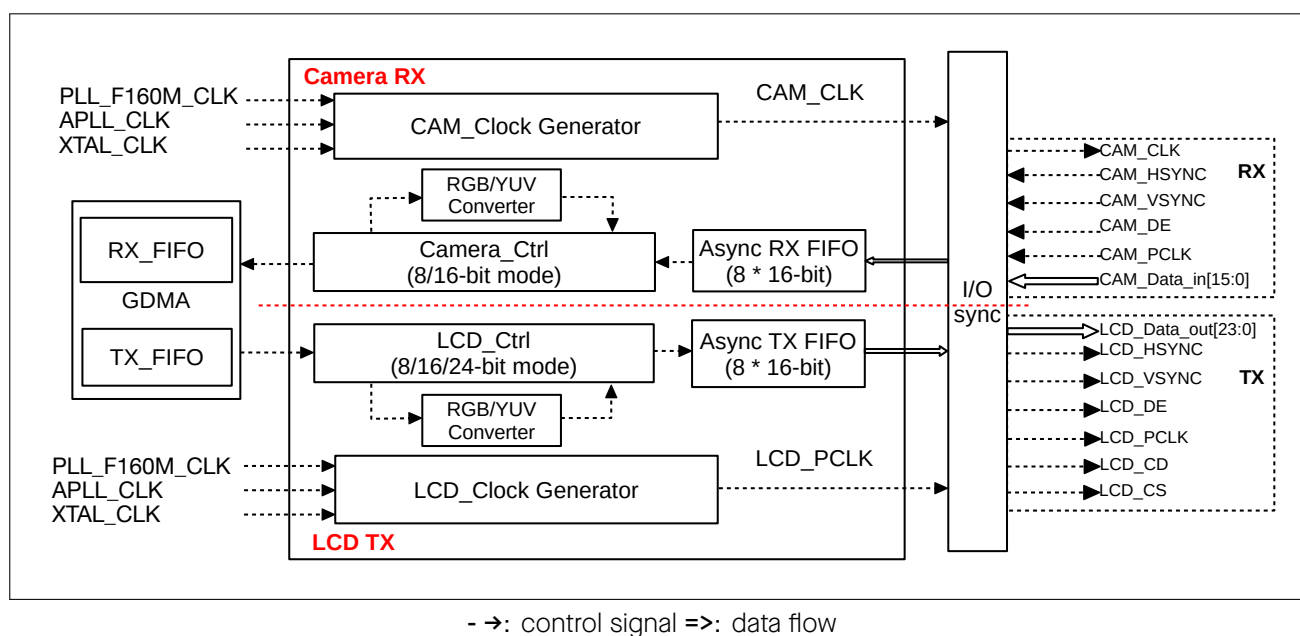


Figure 34.3-1. LCD\_CAM Block Diagram

### 34.3.2 Signal Description

Table 34.3-1 shows the input and output signals required for the operation of the LCD and Camera controller.

The definition of the three operation modes is as follows:

- **Camera Slave RX Mode:** In this mode, the Camera module is the receiver of control signals.
- **Camera Master RX Mode:** In this mode, the Camera module sends clock signals to the slave, which will transmit data to the master upon receiving the signals.
- **LCD Master TX Mode:** In this mode, the LCD module initiates communication with the slave and sends control signals to the slave.

Table 34.3-1. LCD\_CAM Input and Output Signal Descriptions

| Operation Mode        | Signal <sup>1</sup>            | Direction | Function  |
|-----------------------|--------------------------------|-----------|---|
| Camera Slave RX Mode  | CAM_PCLK                       | Input     | Camera pixel clock signal                                 |
|                       | CAM_VSYNC                      | Input     | Vertical synchronization signal (VSYNC) <sup>3</sup>      |
|                       | CAM_HSYNC                      | Input     | Horizontal synchronization signal (HSYNC) <sup>3</sup>    |
|                       | CAM_DE                         | Input     | Horizontal enable signal (DE) <sup>3</sup>                |
|                       | CAM_Data_in[N:0] <sup>2</sup>  | Input     | Camera parallel input data bus, 8/16-bit modes supported  |
| Camera Master RX Mode | CAM_PCLK                       | Input     | Camera pixel clock input signal                           |
|                       | CAM_CLK                        | Output    | Camera master clock output signal                         |
|                       | CAM_VSYNC                      | Input     | Vertical synchronization signal <sup>3</sup>              |
|                       | CAM_HSYNC                      | Input     | Horizontal synchronization signal <sup>3</sup>            |
|                       | CAM_DE                         | Input     | Horizontal enable signal <sup>3</sup>                     |
|                       | CAM_Data_in[N:0] <sup>2</sup>  | Input     | Camera parallel input data bus, 8/16-bit modes supported  |
| LCD Master TX Mode    | LCD_PCLK                       | Output    | LCD pixel clock signal                                    |
|                       | LCD_HSYNC                      | Output    | Horizontal synchronization signal in RGB format           |
|                       | LCD_VSYNC                      | Output    | Vertical synchronization signal in RGB format             |
|                       | LCD_DE                         | Output    | Horizontal enable signal in RGB format                    |
|                       | LCD_CD                         | Output    | Command and data (CD) signal in I8080 format              |
|                       | LCD_CS                         | Output    | Chip select (CS) signal in I8080/MOT06800 format          |
|                       | LCD_Data_out[M:0] <sup>2</sup> | Output    | LCD parallel output data bus, 8/16/24-bit modes supported |

<sup>1</sup> All the signals must be mapped to the chip's pins via GPIO matrix. For more information, see Chapter 8 [GPIO Matrix and IO MUX](#).

<sup>2</sup> For the input signals with 8 or 16-bit width,  $N = 7$  or  $15$  respectively. For the output signals with 8, 16, or 24-bit width,  $M = 7, 15, \text{ or } 23$  respectively.

<sup>3</sup> If [LCD\\_CAM\\_CAM\\_VH\\_DE\\_MODE\\_EN](#) is set, i.e., VSYNC + HSYNC mode is selected, then VSYNC, HSYNC, and DE signals control the data. In this case, users need to wire the three signal lines. If [LCD\\_CAM\\_CAM\\_VH\\_DE\\_MODE\\_EN](#) is cleared, i.e., DE mode is selected, then VSYNC and DE signals control the data. In this case, wiring HSYNC signal line is not a must. But in this case, the YUV-RGB conversion function of the Camera module is not available.

### 34.3.3 LCD\_CAM Module Clocks

#### 34.3.3.1 LCD Clock

The clocks used in the LCD module are generated from clock sources by the LCD\_Clock Generator, see Figure 34.3-2. The clocks include:

- Master clock: LCD\_CLK, divided from the clock sources
- Pixel clock: LCD\_PCLK, divided from LCD\_CLK

[HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_EN](#) is used to enable [LCD\\_CLK\\_SRC](#) (the clock source), and [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_SRC\\_SEL](#) is used to select [LCD\\_CLK\\_SRC](#) from one of the following clock sources:

- 0: XTAL\_CLK
- 1: PLL\_F160M\_CLK
- 2: APLL\_CLK
- 3: Disable LCD clock source

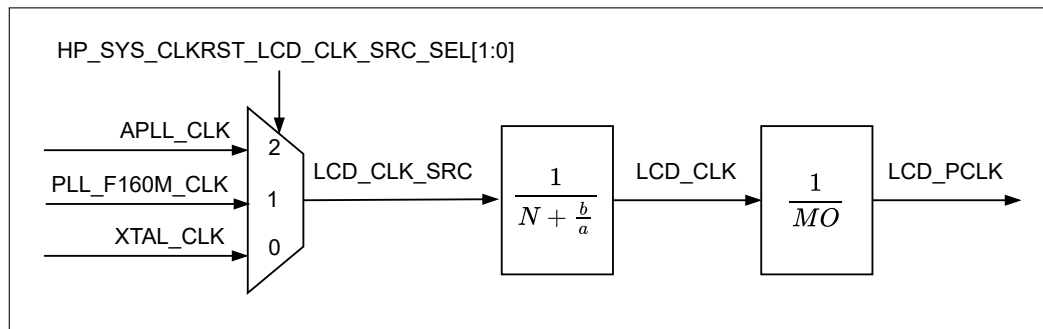


Figure 34.3-2. LCD Clock

The following formula shows the relation between the frequency of [LCD\\_CLK](#) ( $f_{\text{LCD\_CLK}}$ ) and [LCD\\_CLK\\_SRC](#) ( $f_{\text{LCD\_CLK\_SRC}}$ ):

$$f_{\text{LCD\_CLK}} = \frac{f_{\text{LCD\_CLK\_SRC}}}{N + \frac{b}{a}}$$

The values of  $N$ ,  $a$ , and  $b$  are related to [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUM](#), [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUMERATOR](#), and [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_DENOMINATOR](#). Specifically,

- When [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUM](#) = 0,  $N = 1$ . The values of  $a$  and  $b$  do not take effect. The divider is always 1.
- When [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUM](#) >= 1,  $N = \text{HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_NUM} + 1$ .
  - For integer divider, please clear [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUMERATOR](#) and [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_DENOMINATOR](#).
  - For fractional divider,  $b = \text{HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_NUMERATOR}$ ,  $a = \text{HP\_SYS\_CLKRST\_LCD\_CLK\_DIV\_DENOMINATOR}$ . The value of [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_NUMERATOR](#) should be smaller than the value of [HP\\_SYS\\_CLKRST\\_LCD\\_CLK\\_DIV\\_DENOMINATOR](#).

The following formula shows the relation between the frequencies of [LCD\\_PCLK](#) ( $f_{\text{LCD\_PCLK}}$ ) and [LCD\\_CLK](#) ( $f_{\text{LCD\_CLK}}$ ):

$$f_{\text{LCD\_PCLK}} = \frac{f_{\text{LCD\_CLK}}}{\text{MO}}$$

MO is determined by [LCD\\_CAM\\_LCD\\_CLK\\_EQU\\_SYSCLK](#) and [LCD\\_CAM\\_LCD\\_CLKCNT\\_N](#), specifically:

- When [LCD\\_CAM\\_LCD\\_CLK\\_EQU\\_SYSCLK](#) = 1, MO = 1.



- When `LCD_CAM_LCD_CLK_EQU_SYSCLK = 0`, `MO = LCD_CAM_LCD_CLKCNT_N + 1`.

#### Notes:

- `LCD_CAM_LCD_CLKCNT_N` must not be configured as 0.
- Using fractional divider may introduce clock jitters. In case `LCD_CLK` and `LCD_PCLK` can not be generated from `PLL_F160M_CLK` by integer divider, `APLL_CLK` can be used as the clock source. For more information, please refer to Chapter 9 *Reset and Clock*.

### 34.3.3.2 Camera Clock

The clocks used in the Camera module are generated from clock sources by the CAM\_Clock Generator, see Figure 34.3-3. The clocks include:

- Master clock: `CAM_CLK`, master clock output from the Camera module, divided from the clock sources.
- Pixel clock: `CAM_PCLK`, clock input from camera slave.

`HP_SYS_CLKRST_CAM_CLK_EN` is used to enable the `CAM_CLK_SRC` (the clock source), and `HP_SYS_CLKRST_CAM_CLK_SRC_SEL` is used to select `CAM_CLK_SRC` from one of the following clock sources:

- 0: `XTAL_CLK`
- 1: `PLL_F160M_CLK`
- 2: `APLL_CLK`
- 3: Disable camera clock source

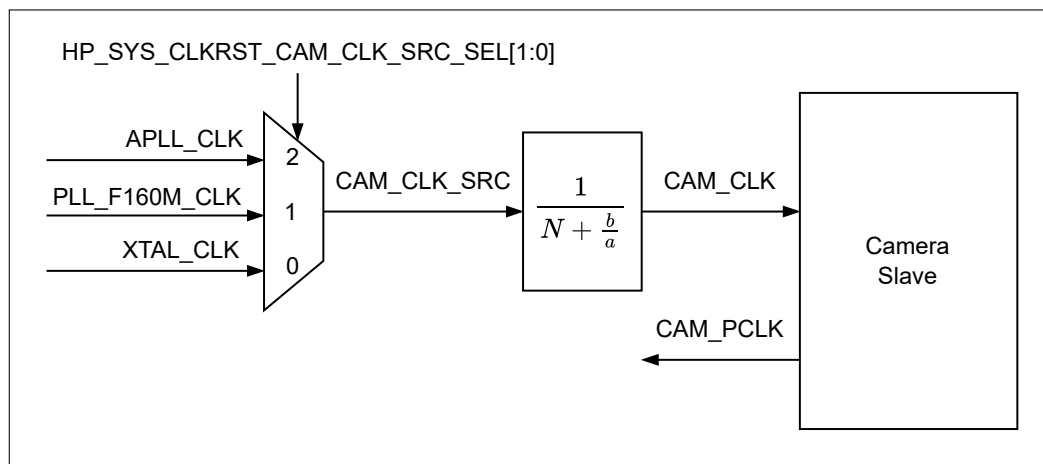


Figure 34.3-3. Camera Clock

The following formula shows the relation between the frequencies of `CAM_CLK` ( $f_{CAM\_CLK}$ ) and the divider's clock source ( $f_{CAM\_CLK\_SRC}$ ):

$$f_{CAM\_CLK} = \frac{f_{CAM\_CLK\_SRC}}{N + \frac{b}{a}}$$

$N$  is an integer value between 2 and 256. The value of  $N$  corresponds to the value of `HP_SYS_CLKRST_CAM_CLK_DIV_NUM` as follows:

- When `HP_SYS_CLKRST_CAM_CLK_DIV_NUM = 0`,  $N = 256$ .

- When `HP_SYS_CLKRST_CAM_CLK_DIV_NUM` = 1,  $N = 2$ .
- When `HP_SYS_CLKRST_CAM_CLK_DIV_NUM` = other value,  $N = \text{HP\_SYS\_CLKRST\_CAM\_CLK\_DIV\_NUM}$ .

$b$  corresponds to the value of `HP_SYS_CLKRST_CAM_CLK_DIV_NUMERATOR`, and  $a$  to the value of `HP_SYS_CLKRST_CAM_CLK_DIV_DENOMINATOR`.

- For integer divider, please clear `HP_SYS_CLKRST_CAM_CLK_DIV_NUMERATOR` and `HP_SYS_CLKRST_CAM_CLK_DIV_DENOMINATOR`.
- For fractional divider, the value of `HP_SYS_CLKRST_CAM_CLK_DIV_NUMERATOR` should be smaller than the value of `HP_SYS_CLKRST_CAM_CLK_DIV_DENOMINATOR`.

### 34.3.4 LCD\_CAM Reset

LCD\_CAM module has the following reset registers that can reset different parts of the module:

- `HP_SYS_CLKRST_RST_EN_LCDCAM`: Setting this register will reset the whole LCD\_CAM module.
- `LCD_CAM_LCD_RESET`: Setting this register will reset the whole LCD module, including the LCD control unit (LCD\_Ctrl), the RGB/YUV Converter, and Async TX FIFO. Configuring this register will not affect the Camera module.
- `LCD_CAM_CAM_RESET`: Setting this register will reset the whole Camera module, including the Camera control unit (Camera\_Ctrl), the RGB/YUV Converter, and Async RX FIFO. Configuring this register will not affect the LCD module.
- `LCD_CAM_LCD_AFIFO_RESET`: Setting this register will reset the Async TX FIFO without affecting other parts in the module. For example, setting this reset register every time the LCD finishes sending a frame can prevent transmission errors of the previous frame from affecting the transmission of the next frame.
- `LCD_CAM_CAM_AFIFO_RESET`: Setting this register will reset the Async RX FIFO without affecting other parts in the module. For example, setting this reset register every time the Camera finishes receiving a frame can prevent transmission errors of the previous frame from affecting the receiving of the next frame.

#### Notes:

- The reset register `HP_SYS_CLKRST_RST_EN_LCDCAM` is not self-clearing, meaning writing 1 enables the reset, and writing 0 releases the reset.
- All the above reset registers, except for `HP_SYS_CLKRST_RST_EN_LCDCAM`, are self-clearing, meaning that after writing 1, the hardware will generate a reset pulse and automatically clear the register.
- The module clocks `LCD_CLK` and `CAM_CLK` must be configured first before the module and FIFO are reset.

### 34.3.5 LCD\_CAM Data Format Control

#### 34.3.5.1 LCD Data Format Control

When the data is transmitted by the LCD module, it undergoes three stages of processing:

1. Stage One: Data preprocessing  
The LCD module processes the input data from GDMA and sends it to the YUV-RGB converter.

## 2. Stage Two: Data color space conversion

The YUV-RGB converter processes the data. If the YUV-RGB converter is disabled, the data remains unchanged at this stage.

## 3. Stage Three: Data post-processing

The LCD module gets data from the YUV-RGB converter for post-processing and then transmits the data to GPIO.

**Note:**

The output data from the previous stage is the input data for the subsequent stage.

The detailed configuration of each stage is described below.

### Stage One: Data Preprocessing

At this stage, configure the following registers to adjust the bit width, bit order, and byte order of the data from GDMA.

- [LCD\\_CAM\\_LCD\\_BYTE\\_MODE](#)
  - 0: The data width of the LCD input from GDMA is 8 bits.
  - 1: The data width of the LCD input from GDMA is 16 bits.
  - 2: The data width of the LCD input from GDMA is 24 bits.
- [LCD\\_CAM\\_LCD\\_BIT\\_ORDER](#)
  - 0: Do not invert.
  - 1: Invert the input data bit order.
- [LCD\\_CAM\\_LCD\\_BYTE\\_ORDER](#)
  - 0: Do not invert.
  - 1: Invert data byte order, only valid in 16/24-bit modes.

For the detailed configuration, see Table [34.3-2](#).

Table 34.3-2. LCD Data Format Control – Stage One

| GDMA Data Order <sup>1</sup> | LCD_CAM_LCD_BYTE_MODE | LCD_CAM_LCD_BIT_ORDER | LCD_CAM_LCD_BYTE_ORDER <sup>2</sup> | Output Data Order <sup>3,4</sup> |
|------------------------------|-----------------------|-----------------------|-------------------------------------|----------------------------------|
| B0,B1,B2,B3,B4,B5            | 0                     | 0                     | 0                                   | {B0}{B1}{B2}{B3}{B4}{B5}         |
|                              |                       | 1                     | 0                                   | {B0'}{B1'}{B2'}{B3'}{B4'}{B5'}   |
|                              | 1                     | 0                     | 0                                   | {B1,B0}{B3,B2}{B5,B4}            |
|                              |                       |                       | 1                                   | {B0,B1}{B2,B3}{B4,B5}            |
|                              |                       | 1                     | 0                                   | {B1',B0'}{B3',B2'}{B5',B4'}      |
|                              |                       |                       | 1                                   | {B0',B1'}{B2',B3'}{B4',B5'}      |
|                              | 2                     | 0                     | 0                                   | {B2,B1,B0}{B5,B4,B3}             |
|                              |                       |                       | 1                                   | {B0,B1,B2}{B3,B4,B5}             |
|                              |                       | 1                     | 0                                   | {B2',B1',B0'}{B5',B4',B3'}       |
|                              |                       |                       | 1                                   | {B0',B1',B2'}{B3',B4',B5'}       |

<sup>1</sup> B0 ~ B5 represent the bytes of the data from GDMA, from low address to high address.

<sup>2</sup> Only the configuration listed in the table is valid. Other configurations may cause unexpected data errors.

<sup>3</sup> In output data, the bits in {} are in big-endian, and are in parallel with each other, while the data of {} is in serial with the data of other {}. Data is sent out from left to right. Take {B0}{B1}{B2}{B3} as an example. The bits in {B0} are in parallel with each other, but are in serial with the bits in {B1}{B2}{B3}. {B0} is sent out first.

<sup>4</sup> In output data, Bn'[7:0] = Bn[0:7] (n = 0,1,2,3,4,5).

### Stage Two: Data Color Space Conversion

At this stage, the data undergoes color space conversion. For detailed configurations, please refer to Section 34.3.6.

#### Note:

Users can skip Stage Two by configuring `LCD_CAM_LCD_CONV_ENABLE` as 0, in which case the output of Stage One will directly become the input of Stage Three.

### Stage Three: Data Post-processing

At this stage, configure the following registers to adjust the bit and byte order of the output data.

- `LCD_CAM_LCD_WIRE_MODE`
  - 0: The bit width of the data transmitted to GPIO is 8 bits.
  - 1: The bit width of the data transmitted to GPIO 16 bits.
  - 2: The bit width of the data transmitted to GPIO is 24 bits.
- `LCD_CAM_LCD_DOUT_BIT_ORDER`
  - 0: Do not invert.
  - 1: Invert the output data bit order.
- `LCD_CAM_LCD_DOUT_BYTE_SWIZZLE_ENABLE`
  - 0: Disable LCD output data byte reordering.
  - 1: Enable LCD output data byte reordering by configuring `LCD_CAM_LCD_DOUT_BYTE_SWIZZLE_MODE`. For the reordering results see Table 34.3-3.

Table 34.3-3. LCD Output Data Reordering

| Stage Three Input Data Byte Order <sup>1</sup> | LCD_CAM_LCD_DOUT_BYTE_SWIZZLE_MODE <sup>2</sup> | Stage Three Output Data Byte Order <sup>3</sup> |
|--|---|---|
| B0,B1,B2,B3,B4,B5                              | 0   | B1,B0,B3,B2,B5,B4                               |
|  | 1   | B0,B2,B1,B3,B5,B4                               |
|  | 2   | B1,B0,B2,B4,B3,B5                               |
|  | 3   | B1,B2,B0,B4,B5,B3                               |
|  | 4   | B2,B0,B1,B5,B3,B4                               |
|  | 5   | B2,B1,B0,B5,B4,B3                               |

<sup>1</sup> B0 ~ B5 represent the bytes of the input data in stage three, i.e., the input data is arranged in a little-endian byte sequence. For example, when the valid data width of the input data is 16 bits, the original input data sequence B1,B0,B3,B2,B5,B4 is converted to B0,B1,B2,B3,B4,B5.

<sup>2</sup> Only the values listed in the table are valid. Other values may cause unexpected data errors.

<sup>3</sup> The byte order of data that is ultimately transmitted to GPIO is determined by the “Stage Three Output Data Byte Order” and the bit width. For example, if the “Stage Three Output Data Byte Order” is B1,B0,B2,B4,B3,B5 and the transmitted data width is 16 bits, then the transmitted data byte order would be {B0,B1}{B4,B2}{B5,B3}. In this sequence, the data within each {} is in big-endian parallel format, and the data in each {} is in serial with the data in other {}. Data is transmitted from left to right. In this particular example, the data in {B0,B1} are in parallel with each other, while the data in {B0,B1} is in serial with the data in {B4,B2} and {B5,B3}. {B0,B1} is transmitted first.

### 34.3.5.2 Camera Data Format Control

When the Camera module receives data, configure the following registers to adjust the bit/byte order of the data sent to GDMA.

- [LCD\\_CAM\\_CAM\\_2BYTE\\_EN](#)
  - 0: The data width of the Camera input is 8 bits.
  - 1: The data width of the Camera input is 16 bits.
- [LCD\\_CAM\\_CAM\\_BIT\\_ORDER](#)
  - 0: Do not invert.
  - 1: Invert data bit order.
    - \* Invert CAM\_DATA\_in[7:0] to CAM\_DATA\_in[0:7] in 8-bit mode.
    - \* Invert CAM\_DATA\_in[15:0] to CAM\_DATA\_in[0:15] in 16-bit mode.
- [LCD\\_CAM\\_CAM\\_BYTE\\_ORDER](#)
  - 0: Do not invert.
  - 1: Invert data byte order, only valid in 16-bit mode.

For the detailed configuration, see Table [34.3-4](#).

Table 34.3-4. Camera Data Format Control

| RX Data Order <sup>1</sup> | LCD_CAM_CAM<br>_2BYTE_EN | LCD_CAM_CAM<br>_BIT_ORDER <sup>2</sup> | LCD_CAM_CAM<br>_BYTE_ORDER <sup>2</sup> | GDMA<br>Order <sup>3,4</sup> | Data |
|----------------------------|--------------------------|--|---|------------------------------|------|
| {B0}{B1}{B2}{B3}           | 0                        | 0                                      | 0                                       | B0,B1,B2,B3                  |      |
|                            |                          | 1                                      | 0                                       | BO',B1',B2',B3'              |      |
| {B1,B0}{B3,B2}             | 1                        | 0                                      | 0                                       | B0,B1,B2,B3                  |      |
|                            |                          |  | 1                                       | B1,B0,B3,B2                  |      |
|                            |                          | 1                                      | 0                                       | BO',B1',B2',B3'              |      |
|                            |                          |  | 1                                       | B1',BO',B3',B2'              |      |

<sup>1</sup> In RX data, the bits in {} are in big-endian, and are in parallel with each other, while the data in {} is in serial with the data in other {}. Data is received from left to right. Take {B0}{B1}{B2}{B3} as an example. The bits in {B0} are in parallel with each other, but are in serial with the bits in {B1}{B2}{B3}. {B0} is received first.

<sup>2</sup> Only the configuration listed in the table is valid. Other configurations may cause unexpected data errors.

<sup>3</sup> B0 ~ B3 represent the bytes of the data to GDMA, from low address to high address.

<sup>4</sup> In the data to GDMA,  $Bn'[7:0] = Bn[0:7]$  ( $n = 0,1,2,3$ ).

**Note:**

If only one byte is received each time, CAM\_Data\_in[7:0] is valid data. For such case, users must connect CAM\_Data\_in[7:0] with the master.

### 34.3.6 YUV-RGB Data Format Conversion

LCD\_CAM is capable of converting data formats between YUV and RGB. The LCD module and Camera module each have a data format converter. The converters support format conversion:

- under BT601 and BT709 standards
- between RGB565 (full/limited range) and YUV422/420/411 (full/limited range) formats
- between YUV422/420/411 (full/limited range) formats
- The converter in the LCD module also supports conversion:
  - from YUV422/420/411 (full/limited range) to RGB888 (full/limited range)
  - from RGB565 (full/limited range) to YUV444 (full/limited range)
  - from YUV422/420/411 (full/limited range) to YUV444 (full/limited range)

#### 34.3.6.1 YUV Formats

In LCD\_CAM module, assume that there are 8 pixels to be transmitted, corresponding to YUV data  $[Y_i, U_i, V_i]$  ( $i = 1 \sim 8$ ). Then:

- In YUV422 mode, the LCD sends (or the camera receives) the data as follows:

|       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $Y_1$ | $U_1$ | $Y_2$ | $V_2$ | $Y_3$ | $U_3$ | $Y_4$ | $V_4$ | $Y_5$ | $U_5$ | $Y_6$ | $V_6$ | $Y_7$ | $U_7$ | $Y_8$ | $V_8$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|

- In YUV420 mode, the LCD sends (or the camera receives) the data as follows:

|       |       |       |       |       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $Y_1$ | $U_1$ | $Y_2$ | $Y_3$ | $U_3$ | $Y_4$ | $Y_5$ | $V_5$ | $Y_6$ | $Y_7$ | $V_7$ | $Y_8$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|

- In YUV411 mode, the LCD sends (or the camera receives) the data as follows:

|       |       |       |       |       |       |       |       |       |       |       |       |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| $Y_1$ | $U_1$ | $Y_2$ | $Y_3$ | $V_3$ | $Y_4$ | $Y_5$ | $U_5$ | $Y_6$ | $Y_7$ | $V_7$ | $Y_8$ |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|

### 34.3.6.2 Format Conversion Configuration

The configuration process for the format conversion in the Camera module is almost identical to that in the LCD module. Therefore, we will illustrate the process using the example of format conversion in the LCD module.

1. Enable YUV-RGB format converter by setting [LCD\\_CAM\\_LCD\\_CONV\\_ENABLE](#).
2. Configure the valid bit width of the input data by configuring [LCD\\_CAM\\_LCD\\_CONV\\_MODE\\_8BITS\\_ON](#):
  - 0: The valid bit width is 16 bits.
  - 1: The valid bit width is 8 bits.
3. Configure the valid bit width of the output data:
  - For the format conversion in the Camera module, the valid bit width of the output data is equal to that of the input data.
  - For the format conversion in the LCD module, when [LCD\\_CAM\\_LCD\\_WIRE\\_MODE](#) is:
    - 2: The valid bit width of the format converter's output data is 24 bits.
    - Other value: The valid bit width of the format converter's output data is equal to that of the input data.
4. Select the standard by configuring [LCD\\_CAM\\_LCD\\_CONV\\_PROTOCOL\\_MODE](#):
  - 0: BT601 standard
  - 1: BT709 standard
5. Configure the conversion mode:
  - In 24-bit output mode:

**Table 34.3-5. Conversion Mode Control in 24-bit Mode**

| Conversion Mode | TRANS_MODE <sup>1</sup> | YUV_MODE <sup>2</sup> | YUV2YUV_MODE <sup>3</sup> |
|-----------------|-------------------------|-----------------------|---------------------------|
| RGB565 → YUV444 | 1                       | -                     | 3                         |
| YUV422 → RGB888 | 0                       | 0                     | 3                         |
| YUV420 → RGB888 | 0                       | 1                     | 3                         |
| YUV411 → RGB888 | 0                       | 2                     | 3                         |
| YUV422 → YUV444 | 1                       | 0                     | 0/1/2                     |
| YUV420 → YUV444 | 1                       | 1                     | 0/1/2                     |
| YUV411 → YUV444 | 1                       | 2                     | 0/1/2                     |

<sup>1</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_TRANS\\_MODE](#)<sup>2</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_YUV\\_MODE](#)<sup>3</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_YUV2YUV\\_MODE](#)

- In other output modes:

**Table 34.3-6. Conversion Mode Control in Other Modes**

| Conversion Mode | TRANS_MODE <sup>1</sup> | YUV_MODE <sup>2</sup> | YUV2YUV_MODE <sup>3</sup> |
|-----------------|-------------------------|-----------------------|---------------------------|
| RGB565 → YUV422 | 1                       | 0                     | 3                         |
| RGB565 → YUV420 | 1                       | 1                     | 3                         |
| RGB565 → YUV411 | 1                       | 2                     | 3                         |
| YUV422 → RGB565 | 0                       | 0                     | 3                         |
| YUV420 → RGB565 | 0                       | 1                     | 3                         |
| YUV411 → RGB565 | 0                       | 2                     | 3                         |
| YUV422 → YUV420 | 1                       | 0                     | 1                         |
| YUV422 → YUV411 | 1                       | 0                     | 2                         |
| YUV420 → YUV422 | 1                       | 1                     | 0                         |
| YUV420 → YUV411 | 1                       | 1                     | 2                         |
| YUV411 → YUV422 | 1                       | 2                     | 0                         |
| YUV411 → YUV420 | 1                       | 2                     | 1                         |

<sup>1</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_TRANS\\_MODE](#)<sup>2</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_YUV\\_MODE](#)<sup>3</sup> The value of [LCD\\_CAM\\_LCD\\_CONV\\_YUV2YUV\\_MODE](#)

6. Configure the color range for the input data by configuring [LCD\\_CAM\\_LCD\\_CONV\\_DATA\\_IN\\_MODE](#):

- 0: limited color range<sup>1</sup>
- 1: full color range<sup>2</sup>

7. Configure the color range for the output data by configuring [LCD\\_CAM\\_LCD\\_CONV\\_DATA\\_OUT\\_MODE](#):

- 0: limited color range<sup>1</sup>
- 1: full color range<sup>2</sup>



**Note:**

1. If the limited color range is selected,
  - the color range of RGB is: 16 ~ 240.
  - the color range of YUV is:
    - Y: 16 ~ 240.
    - U-V: 16 ~ 235.
2. If the full color range is selected, the color range of RGB or YUV is 0 ~ 255.

### 34.3.7 LCD\_CAM Timing

#### 34.3.7.1 LCD Timing (RGB Format)

Figure 34.3-4 shows the LCD frame structure.

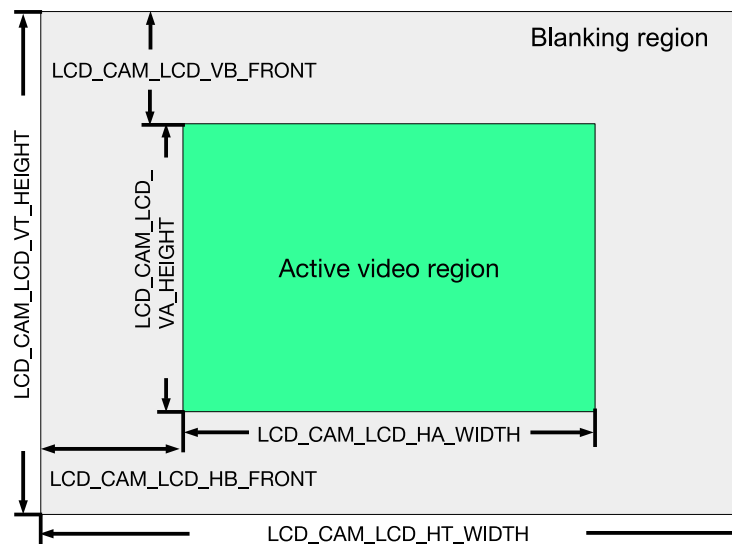


Figure 34.3-4. LCD Frame Structure

As depicted in the figure, the frame structure can be set up with the following registers:

- [LCD\\_CAM\\_LCD\\_VT\\_HEIGHT](#)
- [LCD\\_CAM\\_LCD\\_VA\\_HEIGHT](#)
- [LCD\\_CAM\\_LCD\\_HB\\_FRONT](#)
- [LCD\\_CAM\\_LCD\\_HT\\_WIDTH](#)
- [LCD\\_CAM\\_LCD\\_HA\\_WIDTH](#)
- [LCD\\_CAM\\_VB\\_FRONT](#)

Figure 34.3-5 shows the timing of an LCD full frame.

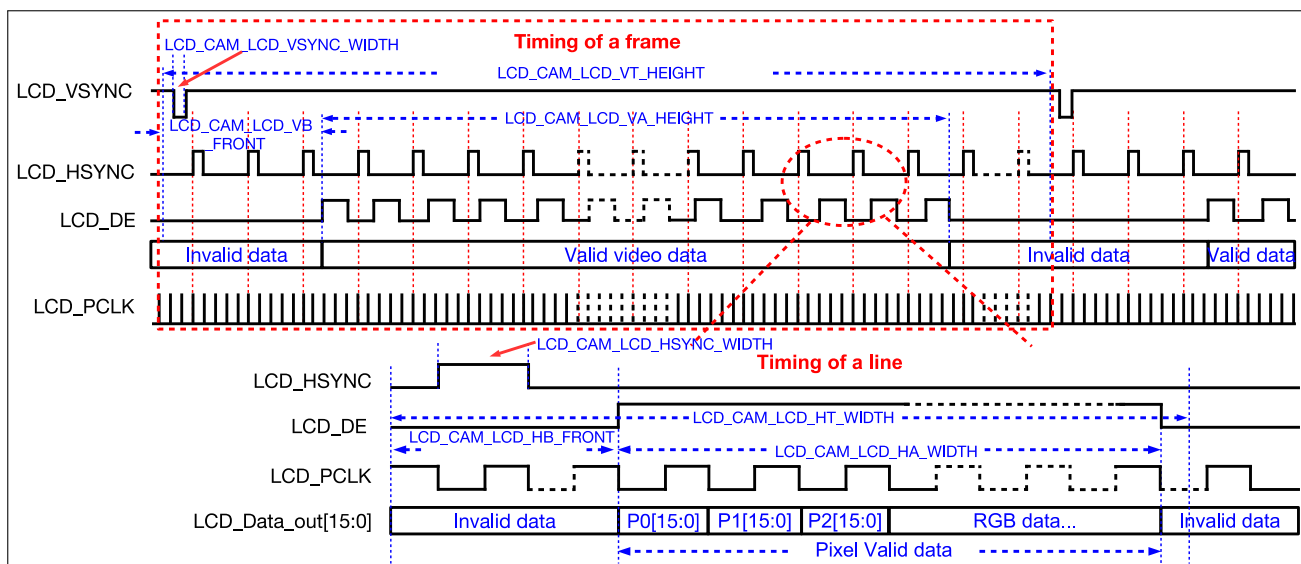


Figure 34.3-5. LCD Timing (RGB Format)

**Note:**

When configuring the parameters shown in the figures above, please note that the parameter is equal to the register value + 1. For example, if the expected VSYNC width is 1, then please configure `LCD_CAM_LCD_VSYNC_WIDTH` to 0. For more information, see the register description.

### 34.3.7.2 LCD Timing (I8080/MOTO6800 Format)

Figure 34.3-6 shows the LCD timing sequence in I8080/MOTO6800 format.

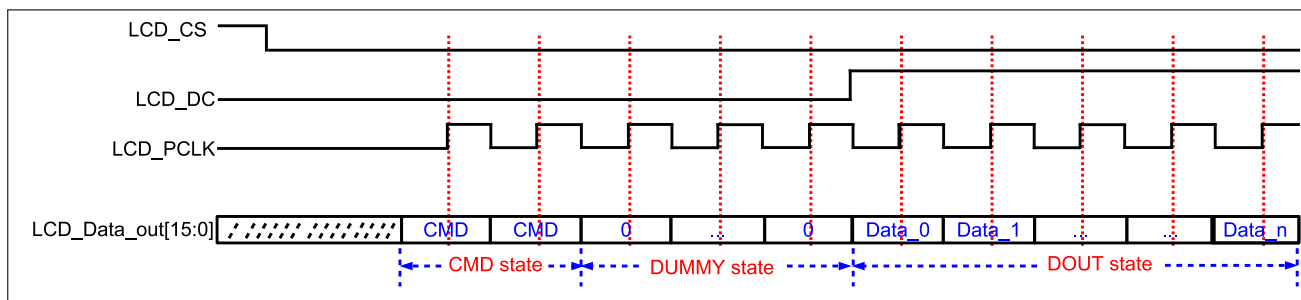


Figure 34.3-6. LCD Timing (I8080/MOTO6800 Format)

## 34.4 Interrupts

ESP32-P4's LCD\_CAM can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- `LCD_CAM_INTR`

The following internal interrupt sources from LCD\_CAM can generate `LCD_CAM_INTR`:

- `LCD_CAM_CAM_HS_INT`: Triggered when the Camera module receives lines more than or equal to the value of `LCD_CAM_CAM_LINE_INT_NUM` + 1.
- `LCD_CAM_CAM_VSYNC_INT`: Triggered when the Camera module receives a whole frame.

- LCD\_CAM\_LCD\_TRANS\_DONE\_INT: Triggered when the LCD module finishes the transmission.
- LCD\_CAM\_LCD\_VSYNC\_INT: Triggered when the LCD module transmits a whole frame.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

## 34.5 Software Configuration Process

**Note:**

Updating the configurations of the LCD module or the Camera module requires setting the LCD\_CAM\_LCD\_UPDATE and LCD\_CAM\_CAM\_UPDATE respectively to synchronize registers from the APB clock domain to the LCD/camera clock domain. Check the configuration examples below for more details.

### 34.5.1 Configure LCD (RGB Format) as TX Mode

Follow the steps below to configure LCD (RGB format) as TX mode via software:

1. Configure clock according to Section [34.3.3](#).
2. Configure signal pins according to Table [34.3-1](#) and Chapter [8 GPIO Matrix and IO MUX](#).
3. Enable corresponding interrupts, see Section [34.4](#).
4. Enable RGB format by setting [LCD\\_CAM\\_LCD\\_RGB\\_MODE\\_EN](#).
5. Configure frame structure according to Section [34.3.71](#).
6. Set [LCD\\_CAM\\_LCD\\_UPDATE](#) so that the configurations take effect.
7. Reset TX control unit (LCD\_Ctrl) and Async TX FIFO as described in Section [34.3.4](#).
8. Configure GDMA outlink, see Chapter [4 VDMA Controller \(VDMA\)](#).
9. Start transmitting data:
  - Wait till LCD slave gets ready.
  - Set [LCD\\_CAM\\_LCD\\_START](#) to start transmitting data.
10. Wait for the interrupt signals set in Step [3](#).
11. In frame intervals during data transmission, check if [LCD\\_CAM\\_LCD\\_NEXT\\_FRAME\\_EN](#) is set:
  - If yes, set [LCD\\_CAM\\_LCD\\_UPDATE](#) (repeating the steps above) to continue transmitting next frame.
  - If not, LCD stops transmitting data.
12. Clear [LCD\\_CAM\\_LCD\\_START](#) if data transmission is done.

### 34.5.2 Configure LCD (I8080/MOTO6800 Format) as TX Mode

Follow the steps below to configure LCD (I8080/MOTO6800 format) as TX mode via software:

1. Configure clock according to Section [34.3.3](#).

2. Configure signal pins according to Table [34.3-1](#) and Chapter [8 GPIO Matrix and IO MUX](#).
3. Enable corresponding interrupts, see Section [34.4](#).
4. Clear [LCD\\_CAM\\_LCD\\_RGB\\_MODE\\_EN](#) to disable RGB format.
5. Configure CMD phase with [LCD\\_CAM\\_LCD\\_CMD](#), [LCD\\_CAM\\_LCD\\_CMD\\_2\\_CYCLE\\_EN](#), and [LCD\\_CAM\\_LCD\\_LATTER\\_CMD\\_VALUE](#).
6. Configure DUMMY phase with [LCD\\_CAM\\_LCD\\_DUMMY](#) and [LCD\\_CAM\\_LCD\\_DUMMY\\_CYCLELEN](#).
7. Configure DOUT phase with [LCD\\_CAM\\_LCD\\_DOUT](#), depending on the output mode:
  - In a fixed-length output<sup>1</sup>, configure data length in [LCD\\_CAM\\_LCD\\_DOUT\\_CYCLELEN](#).
  - In a continuous output<sup>2</sup>, set [LCD\\_CAM\\_LCD\\_ALWAYS\\_OUT\\_EN](#). Users do not need to configure [LCD\\_CAM\\_LCD\\_DOUT\\_CYCLELEN](#).

**Note:**

- (a) In a fixed-length output, the LCD module stops sending data once the data length reaches the value set in [LCD\\_CAM\\_LCD\\_DOUT\\_CYCLELEN](#).
- (b) In a continuous output, LCD module keeps sending data till:
  - [LCD\\_CAM\\_LCD\\_START](#) is cleared;
  - or [LCD\\_CAM\\_LCD\\_RESET](#) is set;
  - or all the data in GDMA is sent out.

8. Configure the CD signal mode, including the default value of the CD signal and the values at each phase, see the description of [LCD\\_CAM\\_LCD\\_MISC\\_REG](#).
9. Set [LCD\\_CAM\\_LCD\\_UPDATE](#) so that the configurations take effect.
10. Reset TX control unit (LCD\_Ctrl) and Async TX FIFO as described in Section [34.3.4](#).
11. Configure GDMA outlink, see Chapter [4 VDMA Controller \(VDMA\)](#).
12. Start transmitting data:
  - Wait till LCD slave gets ready.
  - Set [LCD\\_CAM\\_LCD\\_START](#) to start transmitting data.
13. Wait for the interrupt signals set in Step 2.
14. Clear [LCD\\_CAM\\_LCD\\_START](#) if data transmission is done.

**Notes:**

No matter in which format, RGB or I8080/MOTO6800, the rules below must be followed when accessing internal and external memory via GDMA:

- If LCD data bus is configured to 8-bit parallel output mode, then
  - The pixel clock frequency must be less than 80 MHz.
  - If YUV-RGB format conversion is being used at the same time, the pixel clock frequency must be less than 60 MHz.
- If LCD data bus is configured to 16-bit parallel output mode, then

- The pixel clock frequency must be less than 40 MHz.
- If YUV-RGB format conversion is being used at the same time, the pixel clock frequency must be less than 30 MHz.

### 34.5.3 Configure Camera as RX Mode

Follow the steps below to configure the Camera as RX mode via software:

1. Configure clock according to Section 34.3.3. Note that in slave mode, the module clock frequency should be twice as fast as the PCLK frequency of the image sensor.
2. Configure signal pins according to Table 34.3-1 and Chapter 8 *GPIO Matrix and IO MUX*.
3. Set or clear `LCD_CAM_CAM_VH_DE_MODE_EN` according to the control signal HSYNC.
4. Set needed RX data format according to Section 34.3.5.2.
5. Set `LCD_CAM_CAM_UPDATE` so that the configurations take effect.
6. Reset RX control unit (Camera\_Ctrl) and Async RX FIFO as described in Section 34.3.4.
7. Enable corresponding interrupts, see Section 34.4.
8. Configure GDMA inlink, and set the length of RX data in `LCD_CAM_CAM_REC_DATA_BYTELEN`.
9. Start receiving data:
  - In master mode, when the slave is ready, set `LCD_CAM_CAM_START` to start receiving data.
  - In slave mode, set `LCD_CAM_CAM_START`. Receiving data starts after the master provides clock signal and control signal.
10. Receive data and store the data to GDMA. Then corresponding interrupts set in Step 7 will be generated.

#### Notes:

- No matter in which operation mode, camera master RX mode or camera slave RX mode, the rules below must be followed when accessing internal memory via GDMA:
  - If 8-bit parallel data input mode is selected, then
    - \* The pixel clock frequency must be less than 80 MHz.
    - \* If YUV-RGB format is being used at the same time, the pixel clock frequency must be less than 60 MHz.
  - If 16-bit parallel data input mode is selected, then
    - \* The pixel clock frequency must be less than 40 MHz.
    - \* If YUV-RGB format conversion is being used at the same time, the pixel clock frequency must be less than 30 MHz.

#### Note:

If both LCD and camera are connected externally at the same time, it is necessary to ensure that the maximum data throughput on the interface is less than the total data bandwidth of GDMA when accessing internal/external storage. The default frequency of APB\_CLK is 80 MHz in this scenario. For more information about APB\_CLK, see Chapter 9 [Reset and Clock](#).

## 34.6 Register Summary

The addresses in this section are relative to LCD\_CAM base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description                                   | Address | Access |
|--|---|---------|--------|
| <b>LCD Module Configuration Registers</b>      |   |         |        |
| <a href="#">LCD_CAM_LCD_CLOCK_REG</a>          | LCD clock configuration register              | 0x0000  | R/W    |
| <a href="#">LCD_CAM_LCD_RGB_YUV_REG</a>        | LCD data format conversion register           | 0x0010  | R/W    |
| <a href="#">LCD_CAM_LCD_USER_REG</a>           | LCD user configuration register               | 0x0014  | varies |
| <a href="#">LCD_CAM_LCD_MISC_REG</a>           | LCD MISC configuration register               | 0x0018  | varies |
| <a href="#">LCD_CAM_LCD_CTRL_REG</a>           | LCD signal configuration register             | 0x001C  | R/W    |
| <a href="#">LCD_CAM_LCD_CTRL1_REG</a>          | LCD signal configuration register 1           | 0x0020  | R/W    |
| <a href="#">LCD_CAM_LCD_CTRL2_REG</a>          | LCD signal configuration register 2           | 0x0024  | R/W    |
| <a href="#">LCD_CAM_LCD_FIRST_CMD_VAL_REG</a>  | LCD command value configuration register      | 0x0028  | R/W    |
| <a href="#">LCD_CAM_LCD_LATTER_CMD_VAL_REG</a> | LCD command value configuration register      | 0x002C  | R/W    |
| <a href="#">LCD_CAM_LCD_DLY_MODE_CFG1_REG</a>  | LCD data/signal delay configuration register  | 0x0030  | R/W    |
| <a href="#">LCD_CAM_LCD_DLY_MODE_CFG2_REG</a>  | LCD signal delay mode configuration register  | 0x0038  | R/W    |
| <b>Camera Module Configuration Registers</b>   |   |         |        |
| <a href="#">LCD_CAM_CAM_CTRL_REG</a>           | Camera clock configuration                    | 0x0004  | R/W    |
| <a href="#">LCD_CAM_CAM_CTRL1_REG</a>          | Camera control register                       | 0x0008  | varies |
| <a href="#">LCD_CAM_CAM_RGB_YUV_REG</a>        | Camera data format conversion register        | 0x000C  | R/W    |
| <b>Interrupt Registers</b>                     |   |         |        |
| <a href="#">LCD_CAM_LC_DMA_INT_ENA_REG</a>     | LCD_CAM GDMA interrupt enable register        | 0x0064  | R/W    |
| <a href="#">LCD_CAM_LC_DMA_INT_RAW_REG</a>     | LCD_CAM GDMA raw interrupt status register    | 0x0068  | RO     |
| <a href="#">LCD_CAM_LC_DMA_INT_ST_REG</a>      | LCD_CAM GDMA masked interrupt status register | 0x006C  | RO     |
| <a href="#">LCD_CAM_LC_DMA_INT_CLR_REG</a>     | LCD_CAM GDMA interrupt clear register         | 0x0070  | WO     |
| <b>Version Control Register</b>                |   |         |        |
| <a href="#">LCD_CAM_LC_DATE_REG</a>            | Version control register                      | 0x00FC  | R/W    |

## 34.7 Registers

The addresses in this section are relative to LCD\_CAM base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 34.1. LCD\_CAM\_LCD\_CLOCK\_REG (0x0000)**

|                |     |            |  |  |  |  |  |  |                       |   |                            |     |                           |  |                          |       |
|----------------|-----|------------|--|--|--|--|--|--|-----------------------|---|----------------------------|-----|---------------------------|--|--------------------------|-------|
| LCD_CAM_CLK_EN |     | (reserved) |  |  |  |  |  |  | LCD_CAM_LCD_CLK_CNT_N |   | LCD_CAM_LCD_CLK_EQU_SYSCLK |     | LCD_CAM_LCD_CLK_IDLE_EDGE |  | LCD_CAM_LCD_CLK_OUT_EDGE |       |
|                |     |            |  |  |  |  |  |  |                       |   |                            |     |                           |  |                          |       |
| 31             | 30  |            |  |  |  |  |  |  | 9                     | 8 | 7                          | 6   | 5                         |  |                          | 0     |
| 0              | 0x0 |            |  |  |  |  |  |  | 0                     | 0 | 1                          | 0x3 |                           |  |                          | Reset |

**LCD\_CAM\_LCD\_CLKCNT\_N** Determines the frequency of the LCD pixel clock LCD\_PCLK together with [LCD\\_CAM\\_LCD\\_CLK\\_EQU\\_SYSCLK](#).

When [LCD\\_CAM\\_LCD\\_CLK\\_EQU\\_SYSCLK](#) = 0,

$$f_{LCD\_PCLK} = f_{LCD\_CLK} / (LCD\_CAM\_LCD\_CLKCNT\_N + 1)$$

Note: this field must not be configured to 0.

(R/W)

**LCD\_CAM\_LCD\_CLK\_EQU\_SYSCLK** Determines the frequency of the LCD pixel clock LCD\_PCLK together with [LCD\\_CAM\\_LCD\\_CLK\\_EQU\\_SYSCLK](#).

$$0: f_{LCD\_PCLK} = f_{LCD\_CLK} / (LCD\_CAM\_LCD\_CLKCNT\_N + 1)$$

$$1: f_{LCD\_PCLK} = f_{LCD\_CLK}$$

(R/W)

**LCD\_CAM\_LCD\_CLK\_IDLE\_EDGE** Indicates the level of LCD\_PCLK in idle state.

0: LCD\_PCLK is low.

1: LCD\_PCLK is high.

(R/W)

**LCD\_CAM\_LCD\_CLK\_OUT\_EDGE** Indicates the level of LCD\_PCLK in the first half clock cycle.

0: LCD\_PCLK is low.

1: LCD\_PCLK is high.

(R/W)

**LCD\_CAM\_CLK\_EN** Set this bit to force enable the clock for all configuration registers. Clock gate is not used. (R/W)

**Register 34.2. LCD\_CAM\_LCD\_RGB\_YUV\_REG (0x0010)**

|  |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div>LCD_CAM_LCD_CONV_ENABLE<br/>LCD_CAM_LCD_CONV_TRANS_MODE<br/>LCD_CAM_LCD_CONV_MODE_8BITS_ON<br/>LCD_CAM_LCD_CONV_DATA_IN_MODE<br/>LCD_CAM_LCD_CONV_DATA_OUT_MODE<br/>LCD_CAM_LCD_CONV_PROTOCOL_MODE<br/>LCD_CAM_LCD_CONV_YUV_MODE<br/>(reserved)<br/>LCD_CAM_LCD_CONV_YUV2YUV_MODE<br/>LCD_CAM_LCD_CONV_8BITS_DATA_INV<br/><br/>(reserved)</div> |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 3  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LCD\_CAM\_LCD\_CONV\_8BITS\_DATA\_INV** Configures whether to swap every two 8-bit GDMA input data.

0: Do not swap.

1: Swap.

(R/W)

**LCD\_CAM\_LCD\_CONV\_YUV2YUV\_MODE** Configures data format conversion in YUV-to-YUV mode.

0: Data is converted to YUV422 format.

1: Data is converted to YUV420 format.

2: Data is converted to YUV411 format.

3: Data format conversion is disabled.

Only valid when [LCD\\_CAM\\_LCD\\_CONV\\_TRANS\\_MODE](#) = 1.

(R/W)

**LCD\_CAM\_LCD\_CONV\_YUV\_MODE** Configures the YUV format of input data in YUV-to-YUV mode and YUV-to-RGB mode.

0: Input data is in YUV422 format.

1: Input data is in YUV420 format.

2: Input data is in YUV411 format.

(R/W)

**LCD\_CAM\_LCD\_CONV\_PROTOCOL\_MODE** Configures the data format conversion standard.

0: BT601.

1: BT709.

(R/W)

**LCD\_CAM\_LCD\_CONV\_DATA\_OUT\_MODE** Configures the color range for output data.

0: Limited color range.

1: Full color range.

(R/W)

**LCD\_CAM\_LCD\_CONV\_DATA\_IN\_MODE** Configures the color range for input data.

0: Limited color range.

1: Full color range.

(R/W)

Continued on the next page...



**Register 34.2. LCD\_CAM\_LCD\_RGB\_YUV\_REG (0x0010)**

Continued from the previous page...

**LCD\_CAM\_LCD\_CONV\_MODE\_8BITS\_ON** Configures the valid bit width of the YUV-RGB converter's input data.

0: 16 bits.

1: 8 bits.

(R/W)

**LCD\_CAM\_LCD\_CONV\_TRANS\_MODE** Configures the RGB or YUV format for data conversion.

0: Converted to RGB format.

1: Converted to YUV format.

(R/W)

**LCD\_CAM\_LCD\_CONV\_ENABLE** Configures whether to enable YUV-RGB converter.

0: Bypass the converter.

1: Enable the converter.

(R/W)

**Register 34.3. LCD\_CAM\_LCD\_USER\_REG (0x0014)**

|                            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |  |                            |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|------|--|----------------------------|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LCD_CAM_LCD_CMD_2_CYCLE_EN |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |      |  | LCD_CAM_LCD_DUMMY_CYCLELEN |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  | LCD_CAM_LCD_RESET |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_START |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_CMD |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DUMMY |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DOUT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_BYTE_ORDER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_BIT_ORDER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_UPDATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_BYTE_MODE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DOUT_BIT_ORDER |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DOUT_BYTE_SWIZZLE_ENABLE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DOUT_BYTE_SWIZZLE_MODE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_ALWAYS_OUT_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_DOUT_CYCLELEN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 14 | 13 | 12   |  |                            |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                          | 0  |    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x01 |  |                            |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LCD\_CAM\_LCD\_DOUT\_CYCLELEN** Configures the period of the LCD module's data output phase (DOUT). The actual period duration = the value of this field + 1. (R/W)

**LCD\_CAM\_LCD\_ALWAYS\_OUT\_EN** Enables continuous output of the LCD module. In this mode, the LCD module continuously outputs data during the DOUT phase, until [LCD\\_CAM\\_LCD\\_START](#) is cleared or [LCD\\_CAM\\_LCD\\_RESET](#) is set. (R/W)

**LCD\_CAM\_LCD\_DOUT\_BYTE\_SWIZZLE\_MODE** Configures LCD output data byte reordering. For details please refer to Table [34.3-3](#). (R/W)

**LCD\_CAM\_LCD\_DOUT\_BYTE\_SWIZZLE\_ENABLE** Configures whether to enable LCD output data byte reordering.  
 0: Disable  
 1: Enable  
 (R/W)

**LCD\_CAM\_LCD\_DOUT\_BIT\_ORDER** Configures whether to invert the LCD output data bit order.  
 0: Do not invert.  
 1: Invert the bit order. In n-bit mode, LCD\_DATA\_in[n-1:0] is inverted to LCD\_DATA\_in[0:n-1].  
 (R/W)

**LCD\_CAM\_LCD\_BYTE\_MODE** Configures the data bit width from GDMA.  
 0: 8-bit  
 1: 16-bit  
 2: 24-bit  
 (R/W)

**LCD\_CAM\_LCD\_UPDATE** Configures whether to update the LCD register configurations.  
 0: Do not update.  
 1: Update configurations. This bit is cleared by hardware.  
 (R/W)

**LCD\_CAM\_LCD\_BIT\_ORDER** Configures whether to invert the bit order of the LCD input data.  
 0: Do not invert.  
 1: Invert the bit order. In n-bit mode, LCD\_DATA\_in[n-1:0] is inverted to LCD\_DATA\_in[0:n-1].  
 (R/W)

Continued on the next page...

**Register 34.3. LCD\_CAM\_LCD\_USER\_REG (0x0014)**

Continued from the previous page...

**LCD\_CAM\_LCD\_BYTE\_ORDER** Configures whether to invert the byte order of the LCD input data.

0: Do not invert.

1: Invert data byte order, only valid in 16/24-bit mode.

(R/W)

**LCD\_CAM\_LCD\_DOUT** Configures the LCD DOUT phase.

0: Disable.

1: The LCD module sends data in RGB/I8080 format.

(R/W)

**LCD\_CAM\_LCD\_DUMMY** Configures the LCD DUMMY phase.

0: Disable.

1: Enable the DUMMY phase when LCD initiates.

(R/W)

**LCD\_CAM\_LCD\_CMD** Configures the LCD CMD phase.

0: Disable.

1: The LCD module sends commands.

(R/W)

**LCD\_CAM\_LCD\_START** When set to 1, the LCD module starts transmitting data. (R/W)

**LCD\_CAM\_LCD\_RESET** When set to 1, the LCD module is reset. (WO)

**LCD\_CAM\_LCD\_DUMMY\_CYCLELEN** Configures DUMMY cycles. DUMMY cycles = this value + 1.

(R/W)

**LCD\_CAM\_LCD\_CMD\_2\_CYCLE\_EN** Configures the number of cycles of the Command phase.

0: One cycle.

1: Two cycles.

(R/W)

**Register 34.4. LCD\_CAM\_LCD\_MISC\_REG (0x0018)**

|  |    |    |    |    |    |    |      |                          |  |  |     |                          |   |  |   |                                     |       |   |  |
|--|----|----|----|----|----|----|------|--------------------------|--|--|-----|--------------------------|---|--|---|-------------------------------------|-------|---|--|
| LCD_CAM_LCD_CD_IDLE_EDGE<br>LCD_CAM_LCD_CD_CMD_SET<br>LCD_CAM_LCD_CD_DUMMY_SET<br>LCD_CAM_LCD_CD_DATA_SET<br>LCD_CAM_LCD_AFIFO_RESET<br>LCD_CAM_LCD_BK_EN<br>LCD_CAM_LCD_NEXT_FRAME_EN |    |    |    |    |    |    |      | LCD_CAM_LCD_VBK_CYCLELEN |  |  |     | LCD_CAM_LCD_VFK_CYCLELEN |   |  |   | LCD_CAM_LCD_WIRE_MODE<br>(reserved) |       |   |  |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24   | 12                       |  |  |     | 11                       | 6 |  | 5 | 4                                   | 3     | 0 |  |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x00 |                          |  |  | 0x3 |                          | 0 |  | 0 |                                     | Reset |   |  |

Reset

**LCD\_CAM\_LCD\_WIRE\_MODE** Configures the bit width of LCD output data to GPIO.

0: 8-bit

1: 16-bit

2: 24-bit

(R/W)

**LCD\_CAM\_LCD\_VFK\_CYCLELEN** Configures the clock cycles of the setup time in LCD non-RGB mode. Setup clock cycles = this value + 1. (R/W)**LCD\_CAM\_LCD\_VBK\_CYCLELEN** Configures the clock cycles of the hold time in LCD non-RGB mode. Hold clock cycles = this value + 1. (R/W)**LCD\_CAM\_LCD\_NEXT\_FRAME\_EN** Configures whether to send the next frame.

0: The LCD module stops when the current frame is sent out.

1: The LCD module continues sending the next frame when the current frame is sent out.

(R/W)

**LCD\_CAM\_LCD\_BK\_EN** Configures whether to enable blanking region when LCD sends data.

0: No blanking region.

1: Enable blanking region.

(R/W)

**LCD\_CAM\_LCD\_AFIFO\_RESET** When set to 1, Async TX FIFO is reset. (WO)**LCD\_CAM\_LCD\_CD\_DATA\_SET** Configures LCD\_CD value in DOUT phase for LCD I8080 mode.0: LCD\_CD = [LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)1: LCD\_CD = [!LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)

(R/W)

**LCD\_CAM\_LCD\_CD\_DUMMY\_SET** Configures LCD\_CD value in DUMMY phase for LCD I8080 mode.0: LCD\_CD = [LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)1: LCD\_CD = [!LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)

(R/W)

**LCD\_CAM\_LCD\_CD\_CMD\_SET** Configures LCD\_CD value in CMD phase for LCD I8080 mode.0: LCD\_CD = [LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)1: LCD\_CD = [!LCD\\_CAM\\_LCD\\_CD\\_IDLE\\_EDGE](#)

(R/W)

**LCD\_CAM\_LCD\_CD\_IDLE\_EDGE** The default value of LCD\_CD. (R/W)

Register 34.5. LCD\_CAM\_LCD\_CTRL\_REG (0x001C)

|                         |    |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                       |    |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
|-------------------------|----|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|-----------------------|----|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|---|----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|---|
| LCD_CAM_LCD_RGB_MODE_EN |    |  |  |  |  |  |  |  |  | LCD_CAM_LCD_VT_HEIGHT |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_VA_HEIGHT |    |  |  |  |  |  |  |  |  | LCD_CAM_LCD_HB_FRONT |  |  |  |  |  |  |  |  |   |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
| 31                      | 30 |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  | 21                    | 20 |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |   | 11 | 10 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  | 0 |
| 0                       | 0  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  | 0                     |    |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  | 0 |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |   |

Reset

**LCD\_CAM\_LCD\_HB\_FRONT** Configures the value of ([HSYNC\\_POSITION](#) + [HSYNC\\_WIDTH](#) + horizontal back porch). (R/W)

**LCD\_CAM\_LCD\_VA\_HEIGHT** Configures the vertical active height of a frame. (R/W)

**LCD\_CAM\_LCD\_VT\_HEIGHT** Configures the vertical total height of a frame. (R/W)

**LCD\_CAM\_LCD\_RGB\_MODE\_EN** Configures whether to enable RGB mode.

0: Disable RGB mode.

1: Enable RGB mode and input VSYNC, HSYNC, and DE signals.

(R/W)

Register 34.6. LCD\_CAM\_LCD\_CTRL1\_REG (0x0020)

|                      |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|----------------------|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|
| LCD_CAM_LCD_HT_WIDTH |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_HA_WIDTH |  |  |  |  |  |  |  |  |  |  |  | LCD_CAM_LCD_VB_FRONT |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| 31                   |  |  |  |  |  |  |  |  |  |  |  | 20                   |  |  |  |  |  |  |  |  |  |  |  | 19                   |  |  |  |  |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |
| 0                    |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |

Reset

**LCD\_CAM\_LCD\_VB\_FRONT** Configures the value of ([VSYNC\\_WIDTH](#) + vertical back porch). (R/W)

**LCD\_CAM\_LCD\_HA\_WIDTH** Configures the horizontal active width of a frame. (R/W)

**LCD\_CAM\_LCD\_HT\_WIDTH** Configures the horizontal total width of a frame. (R/W)

**Register 34.7. LCD\_CAM\_LCD\_CTRL2\_REG (0x0024)**

|                            |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
|----------------------------|----|--|----|----|--|----|--|----|----|---|---|---|---|---|---|-------|
| LCD_CAM_LCD_HSYNC_POSITION |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_HSYNC_IDLE_POL |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_HSYNC_WIDTH    |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| (reserved)                 |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_HS_BLANK_EN    |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_DE_IDLE_POL    |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_VSYNC_IDLE_POL |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| LCD_CAM_LCD_VSYNC_WIDTH    |    |  |    |    |  |    |  |    |    |   |   |   |   |   |   |       |
| 31                         | 24 |  | 23 | 22 |  | 16 |  | 15 | 10 |   | 9 | 8 | 7 | 6 | 0 |       |
| 0                          |    |  | 0  | 1  |  | 0  |  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 1 | Reset |

Reset

**LCD\_CAM\_LCD\_VSYNC\_WIDTH** Configures the width of LCD\_VSYNC active pulse in a line. Expected width = this value + 1. (R/W)

**LCD\_CAM\_LCD\_VSYNC\_IDLE\_POL** Configures the idle value of LCD\_VSYNC.

0: The idle value is low.

1: The idle value is high.

(R/W)

**LCD\_CAM\_LCD\_DE\_IDLE\_POL** Configures the idle value of LCD\_DE.

0: The idle value is low.

1: The idle value is high.

(R/W)

**LCD\_CAM\_LCD\_HS\_BLANK\_EN** Configures the LCD\_HSYNC output in RGB mode.

0: LCD\_HSYNC is output only in active video lines.

1: LCD\_HSYNC can be output in vertical blanking intervals.

(R/W)

**LCD\_CAM\_LCD\_HSYNC\_WIDTH** Configures the width of LCD\_HSYNC active pulse. Expected width = this value +1. (R/W)

**LCD\_CAM\_LCD\_HSYNC\_IDLE\_POL** Configures the idle value of LCD\_HSYNC.

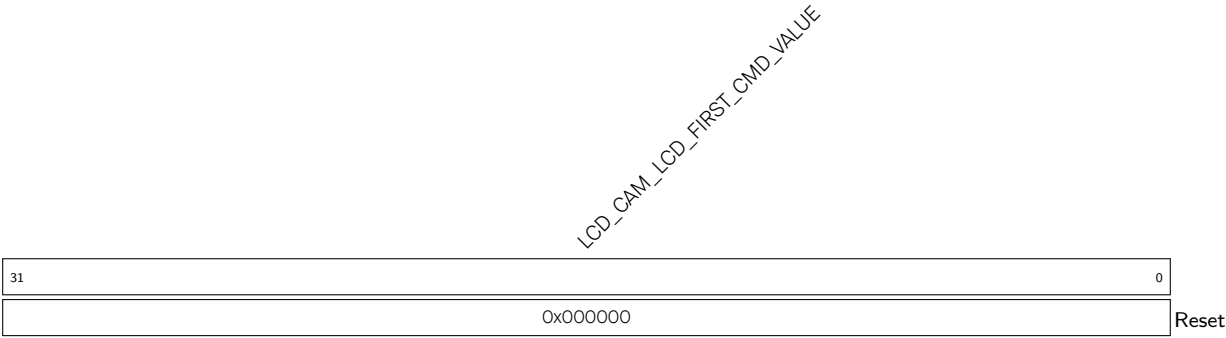
0: The idle value is low.

1: The idle value is high.

(R/W)

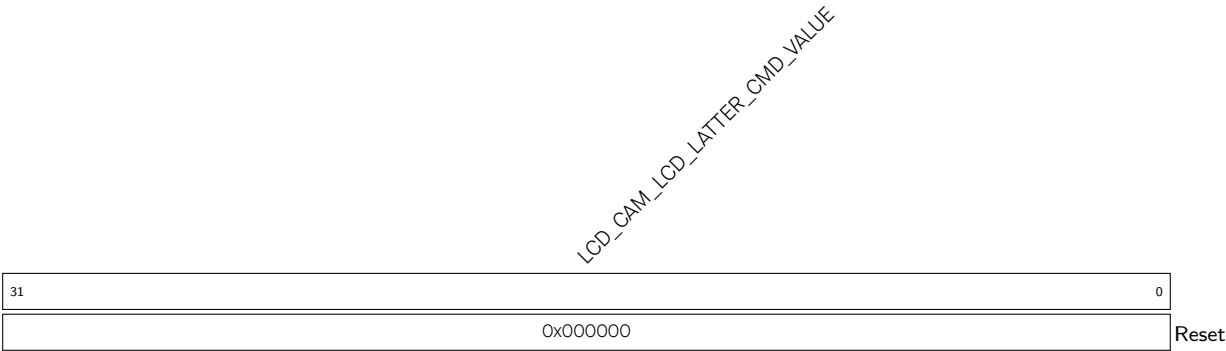
**LCD\_CAM\_LCD\_HSYNC\_POSITION** Configures the position of LCD\_HSYNC active pulse. Expected position = this value + 1. Unit is a pixel. (R/W)

Register 34.8. LCD\_CAM\_LCD\_FIRST\_CMD\_VAL\_REG (0x0028)



**LCD\_CAM\_LCD\_FIRST\_CMD\_VALUE** Configures the value of the transmitted command when the LCD module is in the first cycle of the CMD phase. (R/W)

Register 34.9. LCD\_CAM\_LCD\_LATTER\_CMD\_VAL\_REG (0x002C)



**LCD\_CAM\_LCD\_LATTER\_CMD\_VALUE** Configures the value of the transmitted command when the LCD module is in the second cycle of the CMD phase. (R/W)

**Register 34.10. LCD\_CAM\_LCD\_DLY\_MODE\_CFG1\_REG (0x0030)**

|            |    |    |    |    |    |    |    |                        |     |                        |     |                     |     |                     |     |                     |     |                     |     |                     |     |                     |     |                     |     |                     |     |                     |     |                     |       |
|------------|----|----|----|----|----|----|----|------------------------|-----|------------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-----|---------------------|-------|
| (reserved) |    |    |    |    |    |    |    | LCD_CAM_LCD_VSYNC_MODE |     | LCD_CAM_LCD_HSYNC_MODE |     | LCD_CAM_LCD_DE_MODE |     | LCD_CAM_LCD_CD_MODE |     | LCD_CAM_DOUT23_MODE |     | LCD_CAM_DOUT22_MODE |     | LCD_CAM_DOUT21_MODE |     | LCD_CAM_DOUT20_MODE |     | LCD_CAM_DOUT19_MODE |     | LCD_CAM_DOUT18_MODE |     | LCD_CAM_DOUT17_MODE |     | LCD_CAM_DOUT16_MODE |       |
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23                     | 22  | 21                     | 20  | 19                  | 18  | 17                  | 16  | 15                  | 14  | 13                  | 12  | 11                  | 10  | 9                   | 8   | 7                   | 6   | 5                   | 4   | 3                   | 2   | 1                   | 0     |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x0                    | 0x0 | 0x0                    | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | 0x0 | 0x0                 | Reset |

**LCD\_CAM\_DOUT $n$ \_MODE ( $n$ : 16 - 23)** Configures the delay of the output data bit ( $n$ ).

- 0: No delay.
  - 1: Delayed at the rising edge of LCD\_CLK.
  - 2: Delayed at the falling edge of LCD\_CLK.
- (R/W)

**LCD\_CAM\_LCD\_CD\_MODE** Configures the delay of LCD\_CD output signal.

- 0: No delay.
  - 1: Delayed at the rising edge of LCD\_CLK.
  - 2: Delayed at the falling edge of LCD\_CLK.
- (R/W)

**LCD\_CAM\_LCD\_DE\_MODE** Configures the delay of LCD\_DE output signal.

- 0: No delay.
  - 1: Delayed at the rising edge of LCD\_CLK.
  - 2: Delayed at the falling edge of LCD\_CLK.
- (R/W)

**LCD\_CAM\_LCD\_HSYNC\_MODE** Configures the delay of LCD\_HSYNC output signal.

- 0: No delay.
  - 1: Delayed at the rising edge of LCD\_CLK.
  - 2: Delayed at the falling edge of LCD\_CLK.
- (R/W)

**LCD\_CAM\_LCD\_VSYNC\_MODE** Configures the delay of LCD\_VSYNC output signal.

- 0: No delay.
  - 1: Delayed at the rising edge of LCD\_CLK.
  - 2: Delayed at the falling edge of LCD\_CLK.
- (R/W)



Register 34.11. LCD\_CAM\_LCD\_DLY\_MODE\_CFG2\_REG (0x0038)

|                     |    |                     |    |                     |    |                     |    |                     |    |                     |    |                    |    |                    |    |                    |    |                    |    |                    |    |                    |   |                    |   |                    |   |                    |   |                    |   |
|---------------------|----|---------------------|----|---------------------|----|---------------------|----|---------------------|----|---------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|----|--------------------|---|--------------------|---|--------------------|---|--------------------|---|--------------------|---|
| LCD_CAM_DOUT15_MODE |    | LCD_CAM_DOUT14_MODE |    | LCD_CAM_DOUT13_MODE |    | LCD_CAM_DOUT12_MODE |    | LCD_CAM_DOUT11_MODE |    | LCD_CAM_DOUT10_MODE |    | LCD_CAM_DOUT9_MODE |    | LCD_CAM_DOUT8_MODE |    | LCD_CAM_DOUT7_MODE |    | LCD_CAM_DOUT6_MODE |    | LCD_CAM_DOUT5_MODE |    | LCD_CAM_DOUT4_MODE |   | LCD_CAM_DOUT3_MODE |   | LCD_CAM_DOUT2_MODE |   | LCD_CAM_DOUT1_MODE |   | LCD_CAM_DOUT0_MODE |   |
| 31                  | 30 | 29                  | 28 | 27                  | 26 | 25                  | 24 | 23                  | 22 | 21                  | 20 | 19                 | 18 | 17                 | 16 | 15                 | 14 | 13                 | 12 | 11                 | 10 | 9                  | 8 | 7                  | 6 | 5                  | 4 | 3                  | 2 | 1                  | 0 |
| 0x0                 |    | 0x0                 |    | 0x0                 |    | 0x0                 |    | 0x0                 |    | 0x0                 |    | 0x0                |    | 0x0                |    | 0x0                |    | 0x0                |    | 0x0                |    | 0x0                |   | 0x0                |   | 0x0                |   | 0x0                |   | Reset              |   |

**LCD\_CAM\_DOUT<sub>*n*</sub>\_MODE** (*n*: 0 - 15) Configures the delay of the output data bit *n*.

- 0: No delay.
- 1: Delayed at the rising edge of LCD\_CLK.
- 2: Delayed at the falling edge of LCD\_CLK.

(R/W)

**Register 34.12. LCD\_CAM\_CAM\_CTRL\_REG (0x0004)**

|            |  |  |  |  |  |  |  |   |                                |       |
|------------|--|--|--|--|--|--|--|---|--------------------------------|-------|
| (reserved) |  |  |  |  |  |  |  |   | LCD_CAM_CAM_VS_EOF_EN          |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_LINE_INT_EN        |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_BIT_ORDER          |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_BYTE_ORDER         |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_UPDATE             |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_VSYNC_FILTER_THRES |       |
|            |  |  |  |  |  |  |  |   | LCD_CAM_CAM_STOP_EN            |       |
| 31         |  |  |  |  |  |  |  |   | 1                              | 0     |
| 0x0        |  |  |  |  |  |  |  | 0 | 0                              | Reset |

**LCD\_CAM\_CAM\_STOP\_EN** Configures whether to stop the Camera module.

0: Do not stop.

1: The Camera module stops when GDMA RX FIFO is full.

(R/W)

**LCD\_CAM\_CAM\_VSYNC\_FILTER\_THRES** Configures the filter threshold value for CAM\_VSYNC signal. (R/W)

**LCD\_CAM\_CAM\_UPDATE** Configures whether to update the Camera register configurations.

0: No effect.

1: Update configurations. This bit is cleared by hardware.

(R/W)

**LCD\_CAM\_CAM\_BYTE\_ORDER** Configures whether to invert the byte order of the Camera's input data.

0: Do not invert.

1: Invert data byte order, only valid in 16-bit mode.

(R/W)

**LCD\_CAM\_CAM\_BIT\_ORDER** Configures whether to invert the bit order of the Camera's input data.

0: Do not invert.

1: Invert the bit order. In n-bit mode, CAM\_DATA\_in[n-1:0] is inverted to CAM\_DATA\_in[0:n-1]. n = 8 or 15.

(R/W)

**LCD\_CAM\_CAM\_LINE\_INT\_EN** Configures whether the RAW bit of [LCD\\_CAM\\_CAM\\_HS\\_INT](#) can generate.

0: Disable the interrupt, i.e., [LCD\\_CAM\\_CAM\\_HS\\_INT\\_RAW](#) cannot generate.

1: Enable the interrupt, i.e., [LCD\\_CAM\\_CAM\\_HS\\_INT\\_RAW](#) can generate.

(R/W)

**LCD\_CAM\_CAM\_VS\_EOF\_EN** Configures whether to enable CAM\_VSYNC to generate in\_suc\_eof.

0: in\_suc\_eof is controlled by [LCD\\_CAM\\_CAM\\_REC\\_DATA\\_BYTELEN](#).

1: in\_suc\_eof is controlled by CAM\_VSYNC.

(R/W)

### Register 34.13. LCD\_CAM\_CAM\_CTRL1\_REG (0x0008)

|    |    |    |    |    |    |    |    |    |    |    |     |    |    |      |       |
|----|----|----|----|----|----|----|----|----|----|----|-----|----|----|------|-------|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 |     | 16 | 15 |      | 0     |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x0 |    |    | 0x00 | Reset |

**LCD\_CAM\_CAM\_REC\_DATA\_BYTELEN** Configures the data byte length received by the Camera module. When the length of received data reaches this value + 1, GDMA in\_suc\_eof\_int is triggered. (R/W)

**LCD\_CAM\_CAM\_LINE\_INT\_NUM** Configures the number of video lines. When the number of video lines reaches this value + 1, **LCD\_CAM\_CAM\_HS\_INT** is triggered. (R/W)

**LCD\_CAM\_CAM\_CLK\_INV** Configures whether to invert the input signal CAM\_PCLK.  
0: Do not invert.  
1: Invert.  
(R/W)

|                                    |   |
|------------------------------------|---|
| <b>LCD_CAM_CAM_VSYNC_FILTER_EN</b> | Configures whether to enable CAM_VSYNC filter function. |
| 0: Bypass.                         |   |
| 1: Enable.                         |   |
| (R/W)                              |   |

**LCD\_CAM\_CAM\_2BYTE\_EN** Configures the width of input data.  
 0: 8 bits.  
 1: 16 bits.  
 (R/W)

**LCD\_CAM\_CAM\_DE\_INV** Configures whether to invert the input signal CAM\_DE.  
0: Do not invert.  
1: Invert.  
(R/W)

**LCD\_CAM\_CAM\_HSYNC\_INV** Configures whether to invert the input signal CAM\_HSYNC.  
0: Do not invert.  
1: Invert.  
(R/W)

**LCD\_CAM\_CAM\_VSYNC\_INV** Configures whether to invert the input signal CAM\_VSYNC.  
0: Do not invert.  
1: Invert.  
(R/W)

Continued on the next page...

**Register 34.13. LCD\_CAM\_CAM\_CTRL1\_REG (0x0008)**

Continued from the previous page...

**LCD\_CAM\_CAM\_VH\_DE\_MODE\_EN** Configures the input control signals.

0: VSYNC and DE signals control the data. In this case, wiring HSYNC signal line is not a must. But in this case, the YUV-RGB conversion function of the camera module is not available.

1: VSYNC, HSYNC, and DE signals control the data. In this case, users need to wire the three signal lines.

(R/W)

**LCD\_CAM\_CAM\_START** Camera module start signal. (R/W)

**LCD\_CAM\_CAM\_RESET** When set to 1, the Camera module is reset. (WO)

**LCD\_CAM\_CAM\_AFIFO\_RESET** When set to 1, the Camera Async RX FIFO is reset. (WO)

**Register 34.14. LCD\_CAM\_CAM\_RGB\_YUV\_REG (0x000C)**

|  |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <div style="display: flex; justify-content: space-between;"> <div> <div>LCD_CAM_CAM_CONV_ENABLE</div> <div>LCD_CAM_CAM_CONV_TRANS_MODE</div> <div>LCD_CAM_CAM_CONV_MODE_8BITS_ON</div> <div>LCD_CAM_CAM_CONV_DATA_IN_MODE</div> <div>LCD_CAM_CAM_CONV_DATA_OUT_MODE</div> <div>LCD_CAM_CAM_CONV_PROTOCOL_MODE</div> <div>LCD_CAM_CAM_CONV_YUV_MODE</div> <div>LCD_CAM_CAM_CONV_YUV2YUV_MODE</div> <div>LCD_CAM_CAM_CONV_8BITS_DATA_INV</div> </div> <div>(reserved)</div> </div> |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 3  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**LCD\_CAM\_CAM\_CONV\_8BITS\_DATA\_INV** Configures whether to swap every two bytes of input data.

0: Do not invert.

1: Invert.

(R/W)

**LCD\_CAM\_CAM\_CONV\_YUV2YUV\_MODE** Configures the data format conversion in YUV-to-YUV mode.

0: Data is converted to YUV422 format.

1: Data is converted to YUV420 format.

2: Data is converted to YUV411 format.

3: Disabled.

Valid only when [LCD\\_CAM\\_CAM\\_CONV\\_TRANS\\_MODE](#) = 1.

(R/W)

**LCD\_CAM\_CAM\_CONV\_YUV\_MODE** Configures the YUV format of the Camera input data in YUV-to-YUV mode or YUV-to-RGB mode.

0: Data is converted to YUV422 format.

1: Data is converted to YUV420 format.

2: Data is converted to YUV411 format.

(R/W)

**LCD\_CAM\_CAM\_CONV\_PROTOCOL\_MODE** Configures the data format conversion standard.

0: BT601.

1: BT709.

(R/W)

**LCD\_CAM\_CAM\_CONV\_DATA\_OUT\_MODE** Configures the color range for the YUV-RGB converter's output data.

0: Limited color range.

1: Full color range.

(R/W)

Continued on the next page...

Register 34.14. LCD\_CAM\_CAM\_RGB\_YUV\_REG (0x000C)

Continued from the previous page...

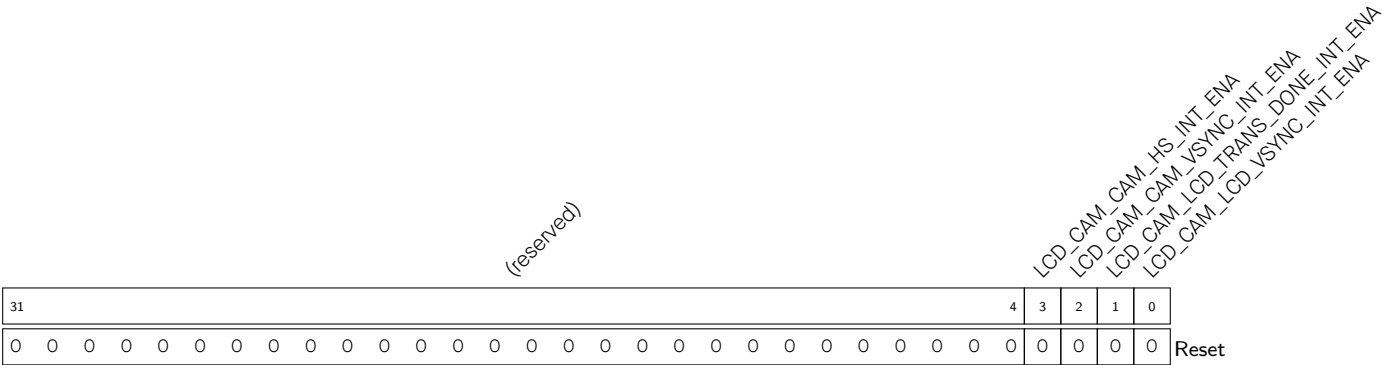
**LCD\_CAM\_CAM\_CONV\_DATA\_IN\_MODE** Configures the color range for the YUV-RGB converter's input data.  
0: Limited color range.  
1: Full color range.  
(R/W)

**LCD\_CAM\_CAM\_CONV\_MODE\_8BITS\_ON** Configures the bit width of the YUV-RGB converter's input data.  
0: 16-bit mode.  
1: 8-bit mode.  
(R/W)

**LCD\_CAM\_CAM\_CONV\_TRANS\_MODE** Configures the data conversion format.  
0: Data is converted to RGB format.  
1: Data is converted to YUV format.  
(R/W)

**LCD\_CAM\_CAM\_CONV\_ENABLE** Configures whether to enable the YUV-RGB converter.  
0: Bypass.  
1: Enable.  
(R/W)

Register 34.15. LCD\_CAM\_LC\_DMA\_INT\_ENA\_REG (0x0064)



**LCD\_CAM\_LCD\_VSYNC\_INT\_ENA** Write 1 to enable [LCD\\_CAM\\_LCD\\_VSYNC\\_INT](#). (R/W)

**LCD\_CAM\_LCD\_TRANS\_DONE\_INT\_ENA** Write 1 to enable [LCD\\_CAM\\_LCD\\_TRANS\\_DONE\\_INT](#). (R/W)

**LCD\_CAM\_CAM\_VSYNC\_INT\_ENA** Write 1 to enable [LCD\\_CAM\\_CAM\\_VSYNC\\_INT](#). (R/W)

**LCD\_CAM\_CAM\_HS\_INT\_ENA** Write 1 to enable [LCD\\_CAM\\_CAM\\_HS\\_INT](#). (R/W)

Register 34.16. LCD\_CAM\_LC\_DMA\_INT\_RAW\_REG (0x0068)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LCD_CAM_CAM_HS_INT_RAW<br>LCD_CAM_CAM_VSYNC_INT_RAW<br>LCD_CAM_LCD_TRANS_DONE_INT_RAW<br>LCD_CAM_LCD_VSYNC_INT_RAW |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | Reset |

**LCD\_CAM\_LCD\_VSYNC\_INT\_RAW** The raw interrupt status of [LCD\\_CAM\\_LCD\\_VSYNC\\_INT](#). (RO)

**LCD\_CAM\_LCD\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of [LCD\\_CAM\\_LCD\\_TRANS\\_DONE\\_INT](#). (RO)

**LCD\_CAM\_CAM\_VSYNC\_INT\_RAW** The raw interrupt status of [LCD\\_CAM\\_CAM\\_VSYNC\\_INT](#). (RO)

**LCD\_CAM\_CAM\_HS\_INT\_RAW** The raw interrupt status of [LCD\\_CAM\\_CAM\\_HS\\_INT](#). (RO)

Register 34.17. LCD\_CAM\_LC\_DMA\_INT\_ST\_REG (0x006C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LCD_CAM_CAM_HS_INT_ST<br>LCD_CAM_CAM_VSYNC_INT_ST<br>LCD_CAM_LCD_TRANS_DONE_INT_ST<br>LCD_CAM_LCD_VSYNC_INT_ST |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | Reset |

**LCD\_CAM\_LCD\_VSYNC\_INT\_ST** The masked interrupt status of [LCD\\_CAM\\_LCD\\_VSYNC\\_INT](#). (RO)

**LCD\_CAM\_LCD\_TRANS\_DONE\_INT\_ST** The masked interrupt status of [LCD\\_CAM\\_LCD\\_TRANS\\_DONE\\_INT](#). (RO)

**LCD\_CAM\_CAM\_VSYNC\_INT\_ST** The masked interrupt status of [LCD\\_CAM\\_CAM\\_VSYNC\\_INT](#). (RO)

**LCD\_CAM\_CAM\_HS\_INT\_ST** The masked interrupt status of [LCD\\_CAM\\_CAM\\_HS\\_INT](#). (RO)

Register 34.18. LCD\_CAM\_LC\_DMA\_INT\_CLR\_REG (0x0070)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LCD_CAM_CAM_HS_INT_CLR<br>LCD_CAM_CAM_VSYNC_INT_CLR<br>LCD_CAM_LCD_TRANS_DONE_INT_CLR<br>LCD_CAM_LCD_VSYNC_INT_CLR |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4 | 3 | 2 | 1  | 0 | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 |       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- LCD\_CAM\_LCD\_VSYNC\_INT\_CLR Write 1 to clear [LCD\\_CAM\\_LCD\\_VSYNC\\_INT](#). (WO)
- LCD\_CAM\_LCD\_TRANS\_DONE\_INT\_CLR Write 1 to clear [LCD\\_CAM\\_LCD\\_TRANS\\_DONE\\_INT](#). (WO)
- LCD\_CAM\_CAM\_VSYNC\_INT\_CLR Write 1 to clear [LCD\\_CAM\\_CAM\\_VSYNC\\_INT](#). (WO)
- LCD\_CAM\_CAM\_HS\_INT\_CLR Write 1 to clear [LCD\\_CAM\\_CAM\\_HS\\_INT](#). (WO)

Register 34.19. LCD\_CAM\_LC\_REG\_DATE\_REG (0x00FC)

|            |   |   |   |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |   |  |       |
|------------|---|---|---|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|---|--|-------|
| (reserved) |   |   |   | LCD_CAM_LC_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 31 | 28 | 27 | 0 |  |       |
| 0          | 0 | 0 | 0 | 0x2303090       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |   |  | Reset |

- LCD\_CAM\_LC\_DATE Version control register. (R/W)



## Chapter 35

### MIPI CSI

#### 35.1 Introduction

The MIPI CSI module of ESP32-P4 provides a standard interface with camera modules for mobile devices, such as smartphones, tablets, and other portable electronics. It connects cameras to application processors in mobile devices, enabling high-speed data transfer and efficient communication between the camera and the host system.

ESP32-P4 MIPI CSI implements a MIPI RX D-PHY and a MIPI CSI-2 host controller. It provides one clock lane and two data lanes, supporting a data transmission of up to 1.5 Gbps per lane to communicate with camera sensors compliant with the [MIPI CSI-2 specification](#).

**Note:**

The [MIPI CSI-2 specification](#) defines the communication between image application processors and cameras. It is part of the communication protocols defined by MIPI Alliance standards, designed for chip-to-chip communication in mobile systems.

#### 35.2 Terminology

This section covers terminology used to describe the functionality of MIPI CSI.

|                    |  |
|--------------------|--|
| <b>MIPI CSI-2</b>  | MIPI Alliance Specification for Camera Serial Interface 2. It receives camera data through the PHY Protocol Interface (PPI) from the MIPI RX D-PHY and outputs data through a 32-bit image interface to the Image Signal Processor (ISP).                  |
| <b>MIPI D-PHY</b>  | MIPI Alliance Specification for the source synchronous physical layer. It implements the physical layer of universal lanes for the MIPI D-PHY interface, which receives clock and data from MIPI camera sensors through one clock lane and two data lanes. |
| <b>PPI</b>         | PHY Protocol Interface defined in MIPI Alliance Specification. It connects the CSI-2 host controller and D-PHY.  |
| <b>ISP</b>         | Image Signal Processor, used to process images received from the camera. For more details about ISP, please refer to Chapter <a href="#">32 Image Signal Processor (ISP)</a> .   |
| <b>Transmitter</b> | The device that transmits data, usually a MIPI camera.   |
| <b>Receiver</b>    | The device that receives data, in this chapter, the ESP32-P4 chip.   |
| <b>Clock lane</b>  | The clock lane of the MIPI D-PHY interface, used to transmit high-speed differential clock signals.  |

|                                       |  |
|---------------------------------------|--|
| <b>Data lane</b>                      | The data lane of the MIPI D-PHY interface, used to transmit data and commands.   |
| <b>Line</b>                           | The line of the data lane of the MIPI D-PHY interface; each data lane consists of two lines: P and N.  |
| <b>Sequence</b>                       | A string of state codes received through the data lane, controlling the MIPI RX D-PHY to enter other modes from Control mode.  |
| <b>Control mode</b>                   | One of the operating modes of the MIPI RX D-PHY, used to receive requests from the transmitter. All other modes return to this mode.   |
| <b>High-Speed Data Reception mode</b> | One of the operating modes of the MIPI RX D-PHY, used to receive data in burst mode.   |
| <b>Escape mode</b>                    | One of the operating modes of the MIPI RX D-PHY, used to support low-speed asynchronous communication on the data lane to maintain a low-power state.                              |
| <b>Ultra Low Power State (ULPS)</b>   | One of the operating modes of the MIPI RX D-PHY, in which the clock lane and data lane are in idle state, maintaining the lowest power consumption except for the Shut-Down state. |
| <b>Test code</b>                      | Specific control or configuration codes used to manage and test the MIPI D-PHY, such as setting operational mode.  |

## 35.3 Feature List

MIPI CSI in ESP32-P4 supports the following features:

- MIPI RX D-PHY compliant with MIPI D-PHY interface specification revision 1.1
- MIPI CSI-2 host compliant with MIPI CSI-2 specification
- Two data lanes, each with a rate ranging from 80 Mbps to 1.5 Gbps
- Ultra Low Power State in Escape mode
- 32-bit image interface with ISP
- Various input image formats:
  - RGB888/RGB666/RGB565
  - YUV422/YUV420
  - RAW8/RAW10/RAW12
- Error detection and correction at PHY level, packet level, line level, and frame level
- Electromagnetic Interference (EMI) mitigation by data scrambling

**Note:**

ESP32-P4 does not support different virtual channels defined in the MIPI specification, so virtual channel numbers in the packet header are ignored.

## 35.4 Architectural Overview

Figure 35.4-1 shows the architecture of MIPI CSI and its connection to other system components. The MIPI CSI consists of the following components:

- **MIPI RX D-PHY:** Implements the physical link layer, including one clock lane (CP/CN) and two data lanes (D0P/D0N and D1P/D1N) to connect with cameras.
- **MIPI CSI-2 host:** Implements the CSI-2 protocol, receives camera data from D-PHY, and outputs through the Image Interface, which includes:
  - **Pipeline:** Registers PPI signals.
  - **Descrambler:** Converts PPI scrambled data to its original values when enabled.
  - **PHY adaptation layer:** Manages the PHY interface, including PHY error handling.
  - **Packet analyzer:** Processes received data from lanes, including data lane merging, header decoding, and various error detection and correction.
  - **Image interface:** Reorders pixels into 32-bit Image Interface data and generates timing-accurate video synchronization signals.
  - **Error management:** Monitors and notifies about error conditions on the CSI-2 link.
  - **Register bank:** Provides access to configuration and control registers.
- **PPI interface:** Connects the MIPI RX D-PHY and the MIPI CSI-2 host controller.
- **Test code interface:** Sends configuration details from the MIPI CSI-2 host controller to the MIPI RX D-PHY.

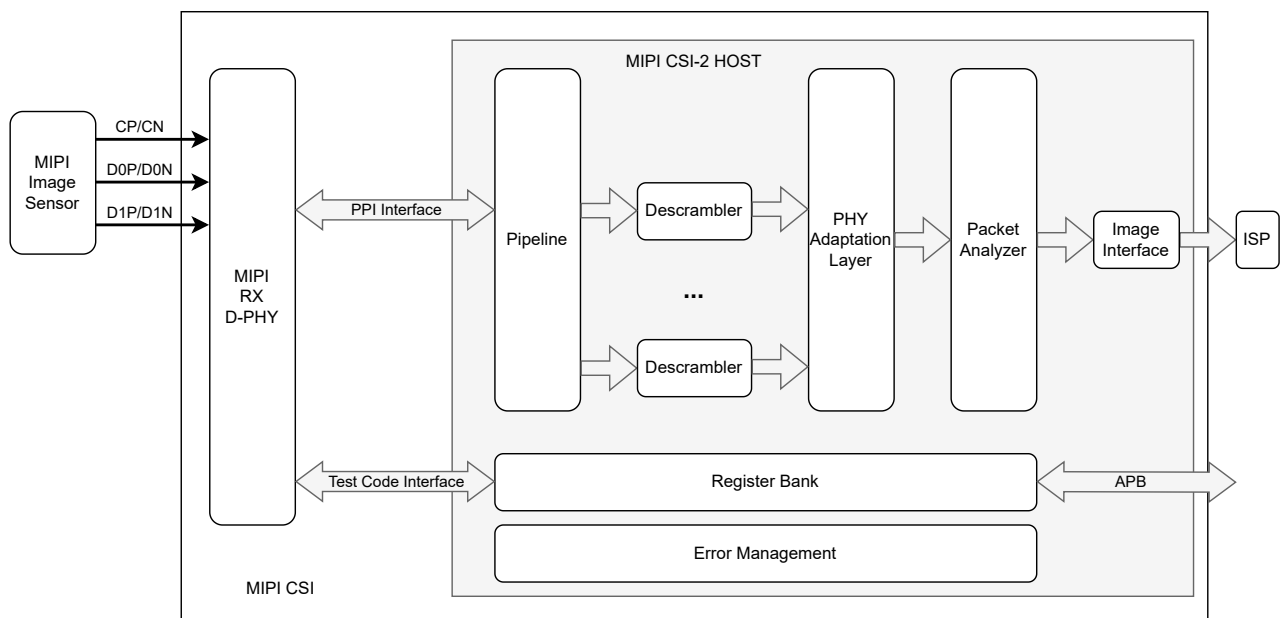


Figure 35.4-1. MIPI CSI Architecture

## 35.5 Functional Description

This section introduces the operating states and modes of the MIPI RX D-PHY and the major functions that facilitate the use of MIPI CSI. For detailed configurations, refer to Section [35.7 Programming Procedures](#).

### 35.5.1 Data Lane State

The functions of the transmitter determine the data lane state by driving certain line levels. During normal operation, either an HS-TX or an LP-TX is driving a lane.

- HS-TX: High-Speed transaction. An HS-TX always drives the lane differentially. It operates in two states: HS-0 and HS-1. When HS-TX drives the lane, the lane remains in High-Speed Data Reception mode.
  - HS-0: Transmits differential data 0 in High-Speed Data Reception mode.
  - HS-1: Transmits differential data 1 in High-Speed Data Reception mode.
- LP-TX: Low-Power transaction. The two LP-TXs drive the two lines of a lane independently and single-ended. It operates in four states: LP-00, LP-01, LP-10, and LP-11. When LP-TX drives the lane, the lane is in Control mode or Escape mode.
  - LP-00: A bridge state between other LP states (LP-01, LP-10, LP-11) in Control Mode or Escape Mode. When in Ultra Low Power State (ULPS), lanes are also in the LP-00 state.
  - LP-01: Transmits data 0 in Escape mode, or indicates entry into High-Speed Data Reception mode from Control mode.  
The complete sequence for entering High-Speed Data Reception mode is: LP-11 → LP-01 → LP-00
  - LP-10: Transmits data 1 in Escape mode, or indicates entry into Escape mode or Turnaround mode from Control mode.  
The complete sequence for entering Escape mode is: LP-11 → LP-10 → LP-00 → LP-01 → LP-00.  
The complete sequence for entering the Turnaround mode is: LP-11 → LP-10 → LP-00 → LP-10 → LP-00
  - LP-11: The stop state, i.e., the default idle state of a lane.

**Note:**

The Turnaround mode is used for switching the data transmission direction. This mode is not used in the ESP32-P4 MIPI CSI, and will not be further explained in this chapter.

Figure [35.5-1](#) shows the lane line levels for High-Speed (HS) and Low-Power (LP) transactions.

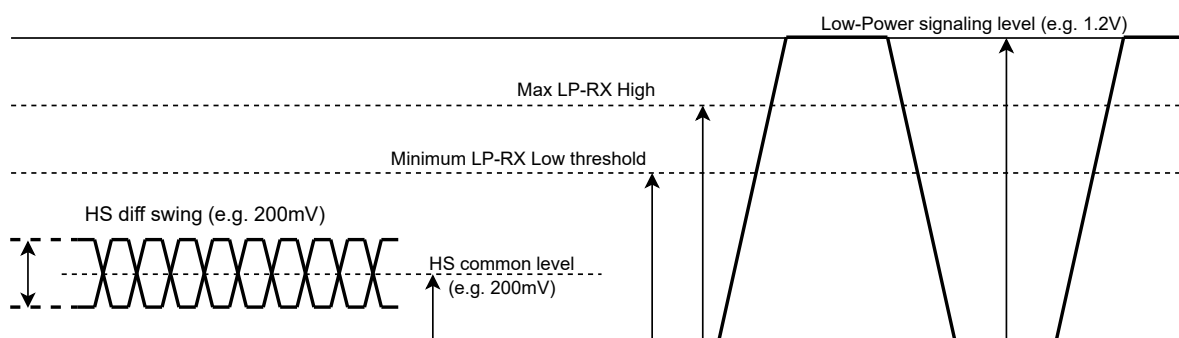


Figure 35.5-1. Level of MIPI Data Lane Lines

Table 35.5-1 shows the available line states.

Table 35.5-1. Lane State Descriptions

| State Code | DP Line | DN Line | Corresponding State in Different Modes |              |             |
|------------|---------|---------|--|--------------|-------------|
|            |         |         | High-Speed Data Reception Mode         | Control Mode | Escape Mode |
| HS-0       | HS Low  | HS High | 0                                      | N/A          | N/A         |
| HS-1       | HS High | HS Low  | 1                                      | N/A          | N/A         |
| LP-00      | LP Low  | LP Low  | N/A                                    | Bridge       | Space       |
| LP-01      | LP Low  | LP High | N/A                                    | HS-Rqst      | 0           |
| LP-10      | LP High | LP Low  | N/A                                    | LP-Rqst      | 1           |
| LP-11      | LP High | LP High | N/A                                    | Stop         | N/A         |

## 35.5.2 MIPI RX D-PHY Operation

Figure 35.5-2 illustrates the various states and modes of the MIPI RX D-PHY during initialization and active state. Detailed descriptions of each states and modes are presented in the following sections.

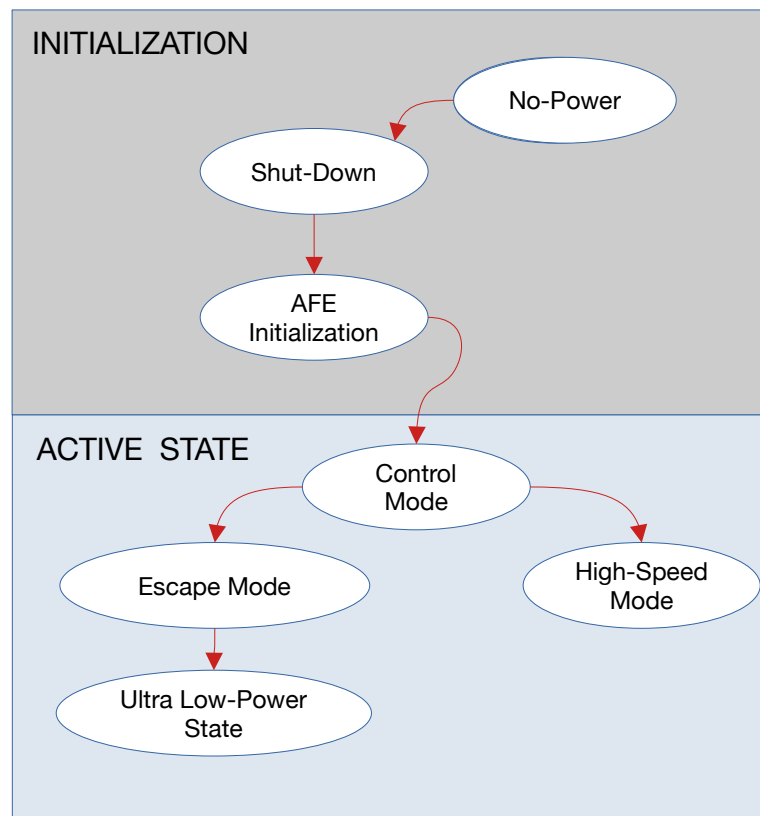


Figure 35.5-2. MIPI RX D-PHY Operating States and Modes

### 35.5.2.1 No-Power State

In the No-Power state, no supply voltage is applied to the PHY.

The MIPI RX D-PHY of MIPI CSI is in No-Power state when the power supply VDD\_HP\_*n* (n: 0-3) and VDD\_MIPI\_DPHY are off.

### 35.5.2.2 Shut-Down State

Shut-Down state refers to the idle state.

In Shut-Down state, the PHY disables all analog blocks, resets all digital logic, and sets the DOP/DON, D1P/D1N, and CP/CN lanes to high impedance (Hi-Z). Activating the Shut-Down state ensures the lowest power consumption. To enable the Shut-Down state of the PHY, set [CSI\\_HOST\\_DPHY\\_RSTZ](#) and [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#) to 0.

Before leaving the Shut-Down state, configure several parameters, including the lane number to be used and the lane operation frequency range.

The MIPI RX D-PHY consists of two data lanes. Configure [CSI\\_HOST\\_N\\_LANES](#) to select either one or both data lanes. These configurations should remain static or stable before exiting the Shut-Down state.

Depending on the specific requirements for the MIPI RX D-PHY, additional configuration steps might be necessary. By default, the PHY operates within a lower range of 80-110 Mbps. To accommodate higher bit rates, adjust the HS frequency ranges (the `hsfreorange` field) in test code [HS RX Control of lane 0](#) with the appropriate code. It is recommended to perform this adjustment in the Shut-Down state, as the control interface is independent of the rest of the MIPI RX D-PHY.

The different ranges supported are shown in Table 35.5-2. The hsfreqrange field indicates the HS operating frequency range and is accessible through test code 0x44. For detailed configuration, please refer to Section 35.5.3 *MIPI RX D-PHY Configuration*.

**Table 35.5-2. Frequency Ranges Supported by MIPI RX D-PHY**

| Frequency Range (Mbps) | hsfreqrange[5:0] |
|------------------------|------------------|
| 80-89                  | 000000           |
| 90-99                  | 010000           |
| 100-109                | 100000           |
| 110-129                | 000001           |
| 130-139                | 010001           |
| 140-149                | 100001           |
| 150-169                | 000010           |
| 170-179                | 010010           |
| 180-199                | 100010           |
| 200-219                | 000011           |
| 220-239                | 010011           |
| 240-249                | 100011           |
| 250-269                | 000100           |
| 270-299                | 010100           |
| 300-329                | 000101           |
| 330-359                | 010101           |
| 360-399                | 100101           |
| 400-449                | 000110           |
| 450-499                | 010110           |
| 500-549                | 000111           |
| 550-599                | 010111           |
| 600-649                | 001000           |
| 650-699                | 011000           |
| 700-749                | 001001           |
| 750-799                | 011001           |
| 800-849                | 101001           |
| 850-899                | 111001           |
| 900-949                | 001010           |
| 950-999                | 011010           |
| 1000-1049              | 101010           |
| 1050-1099              | 111010           |
| 1100-1149              | 001011           |
| 1150-1199              | 011011           |
| 1200-1249              | 101011           |
| 1250-1299              | 111011           |
| 1300-1349              | 001100           |
| 1350-1399              | 011100           |
| 1400-1449              | 101100           |

| Frequency Range (Mbps) | hsfreqrange[5:0] |
|------------------------|------------------|
| 1450-1500              | 111100           |

When [CSI\\_HOST\\_DPHY\\_RSTZ](#) and [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#) are set to 1, the MIPI RX D-PHY leaves the Shut-Down state and starts the initialization procedure.

### 35.5.2.3 AFE Initialization

After releasing [CSI\\_HOST\\_DPHY\\_RSTZ](#) and [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#), the PHY begins an initialization sequence for normal operation. It is recommended to release [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#) before [CSI\\_HOST\\_DPHY\\_RSTZ](#). Additionally, ensure that [CSI\\_DPHY\\_CFG\\_CLK](#) (refer to Table 9.2-5 in Chapter 9 *Reset and Clock* for details) is available and stable at this point.

The initialization sequence includes several steps, such as enabling internal blocks and performing internal calibrations. Once completed, control transfers to the lanes, which manage power for LP/HS requests from the transmitter by enabling or disabling the corresponding receivers.

Set [CSI\\_HOST\\_PHY\\_STOPSTATEDATA\\_n](#) and [CSI\\_HOST\\_PHY\\_STOPSTATECLK](#) to 1 to perform all initialization steps. In this state, both clock and data lanes are in stop state (LP-11).

The initialization period (TINIT) is a protocol-dependent parameter with a minimum duration of 100 ns, as defined by the specification. After setting [CSI\\_HOST\\_PHY\\_STOPSTATEDATA\\_n](#) and [CSI\\_HOST\\_PHY\\_STOPSTATECLK](#) to 1, the software should wait more than 100 ns before starting camera data reception.

### 35.5.2.4 Control Mode

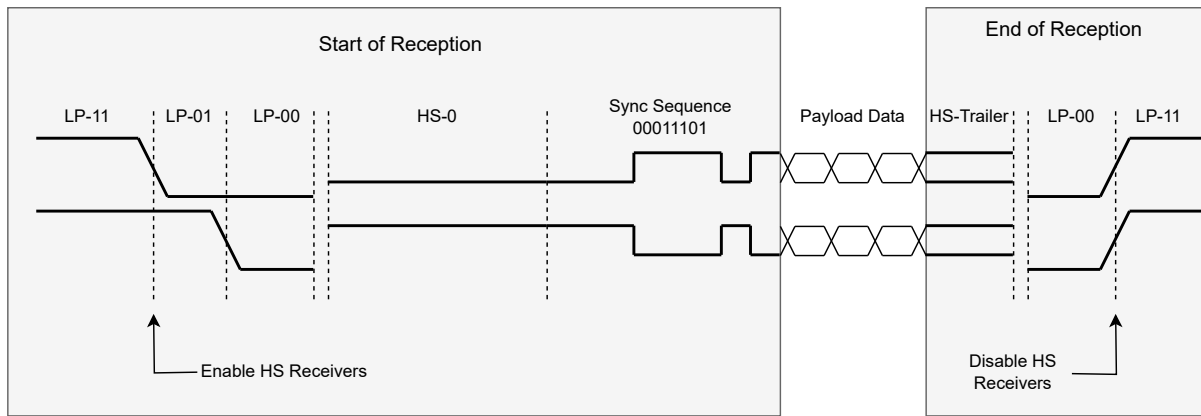
After completing AFE initialization, the MIPI RX D-PHY remains in Control mode by default. It receives the LP-11 state code (stop state) on the lines until a request is made. Upon receiving a request, the PHY enters either High-Speed Data Reception mode, Escape mode, or Ultra Low Power State. All requests must begin and end with the lanes in the stop state.

### 35.5.2.5 High-Speed Data Reception Mode

In High-Speed Data Reception mode, the PHY receives data in bursts. The lane operates in high-speed mode only during these bursts.

As shown in Figure 35.5-3, a burst consists of three parts: the low-power initialization sequence, the high-speed data payload, and the end of reception sequence.





**Figure 35.5-3. MIPI CSI HS Data Reception Sequence**

The receiver enters high-speed mode following the low-power sequence of [LP-11 > LP-01 > LP-00]. Synchronization is achieved through a sync sequence of “00011101”. After synchronization, the PHY receives high-speed data until a transition from LP-00 to LP-11 is detected on the lane.

### 35.5.2.6 Escape Mode

Escape mode allows asynchronous communication using data lanes at low speed. During Escape mode, the lane remains in low-power state. A data lane enters this mode after Escape mode request sequence [LP-11 > LP-10 > LP-00 > LP-01 > LP-00]. If an LP-11 state code is detected before the lane reaches LP-00, the request will be aborted, and the lane will return to stop state. Upon entering Escape mode, the transmitter sends an 8-bit command to indicate a requested action.

MIPI CSI only supports Ultra Low Power State (ULPS) in escape mode. The 8-bit command to enter ULPS is “b00011110”. If the entry command is not valid, it will be ignored, and the receiver will wait until the transmitter returns to the stop state.

#### Ultra Low Power State

Ultra Low Power State involves the lowest power consumption, except for the Shut-Down state.

For data lanes, this mode is activated by sending an Ultra Low Power State entry command “00011110”. After that, the clock lane and data lanes enter the space state (LP-00).

Figure 35.5-4 shows the ULPS sequences for clock and data lanes.

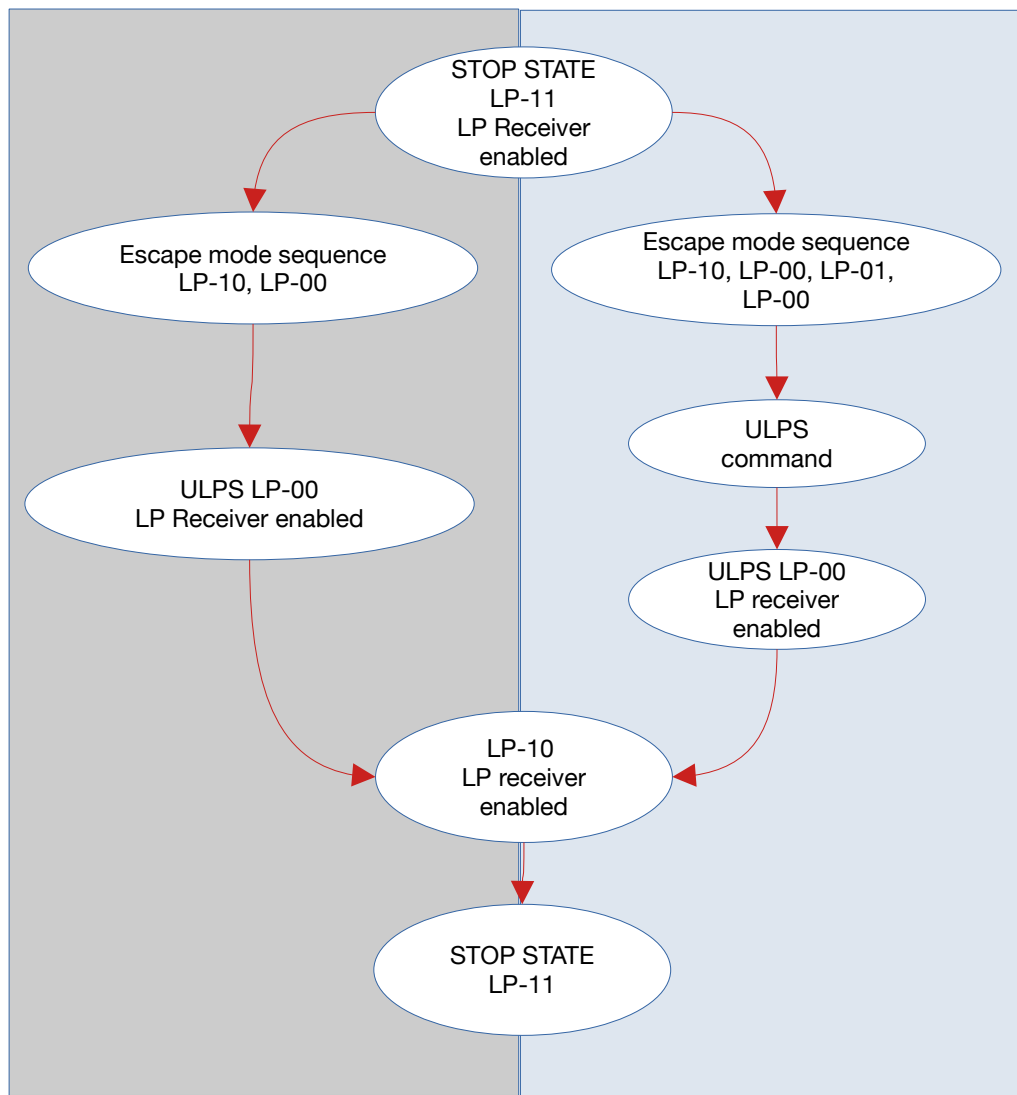


Figure 35.5-4. ULPS Sequences for Clock and Data Lanes

### 35.5.3 MIPI RX D-PHY Configuration

The MIPI RX D-PHY includes test codes for configuring MIPI RX D-PHY operation. Refer to Section 35.5.3.2 for all supported test codes.

#### 35.5.3.1 MIPI RX D-PHY Programming Interface

The MIPI RX D-PHY test code programming involves two steps: first, program the test code into the registers; second, provide the test data to the tester's inputs.

Before configuring a test code, perform the following steps:

- Write 0 to [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#) and [CSI\\_HOST\\_DPHY\\_RSTZ](#) to shut down and reset the PHY.
- It is also recommended to set [CSI\\_HOST\\_PHY\\_TESTCLR](#) to 1 to apply a reset pulse before the first configuration of any test code.

Next, configure the test code by following these steps:

- Set the test code.

The test code loads when `CSI_HOST_PHY_TESTEN` is set to 1 and with the falling edge on `CSI_HOST_PHY_TESTCLK`.

- Ensure that `CSI_HOST_PHY_TESTCLK` is set to 1.
- Set `CSI_HOST_PHY_TESTDIN` to the 8-bit test code.
- Set `CSI_HOST_PHY_TESTEN` to 1.
- Set `CSI_HOST_PHY_TESTCLK` to 0. The falling edge on `CSI_HOST_PHY_TESTCLK` latches the value of `CSI_HOST_PHY_TESTDIN[7:0]` as the current test code.
- Set `CSI_HOST_PHY_TESTEN` to 0.
- Enter the test data.

The test data programs to the latest loaded test code when `CSI_HOST_PHY_TESTEN` is 0 and with the rising edge on `CSI_HOST_PHY_TESTCLK`.

- Set `CSI_HOST_PHY_TESTCLK` to 0, if not done already.
- Set `CSI_HOST_PHY_TESTDIN` to the 8-bit test data.
- Set `CSI_HOST_PHY_TESTCLK` to 1. The rising edge on `CSI_HOST_PHY_TESTCLK` programs the test data internally.
- Repeat the above steps to add more test data for the same test code.

Set `CSI_HOST_PHY_TESTCLR` to 1 to reset a test code. This is necessary only before the first programming operation or if you wish to reset the PHY's configuration to its default value.

Figure 35.5-5 shows a timing diagram for the MIPI RX D-PHY control interface. After programming a test code, `CSI_HOST_PHY_TESTDOUT` asynchronously outputs the relevant data associated with the specific test code. This data may include read-back information or other meaningful signals.

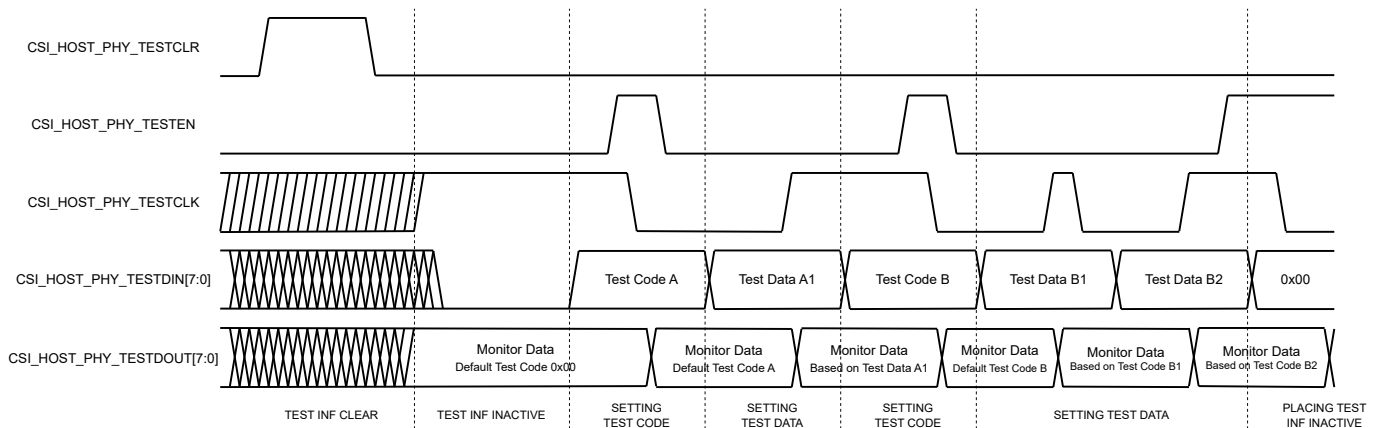


Figure 35.5-5. Control Interface Timing Diagram

**Note:**

Some test codes require two write data operations. In the first operation, the value of `CSI_HOST_PHY_TESTCLK` changes from 1 to 0. Ensure that the falling edge in the clock does not occur when `CSI_HOST_PHY_TESTEN` is set to 1. Otherwise, the current test data will be latched as an erroneous test code.

It is highly recommended to set the test interface to an inactive state by programming the test code 0x00 when not

used, as shown in the final sequence in Figure 35.5-5.

### 35.5.3.2 MIPI RX D-PHY Test Code

The MIPI RX D-PHY is configured through test codes via [CSI\\_HOST\\_PHY\\_TEST\\_CTRL0\\_REG](#) and [CSI\\_HOST\\_PHY\\_TEST\\_CTRL1\\_REG](#). Refer to Section 35.5.3.1 *MIPI RX D-PHY Programming Interface* for more details.

#### Normal Operation

Use the following test code to enable normal operation of the PHY and the wake-up state of the test interface. In this mode, the test interface is inactive.

- **Test Code:** 0x00
- **Test Data:** None

#### HS RX Control of Lane 0

Use the following test code to select the HS operating frequency range (hsfreqrange).

- **Test Code:** 0x44
- **Test Data:**

Table 35.5-3. Test Data in HS RX Control of Lane 0

| w-1'b0           | w-6'b0   | w-1'b0   |
|------------------|--|----------|
| Program Selector | HS operating frequency range selection (hsfreqrange) | Reserved |

When Program Selector is 0, Test Data[6:1] programs hsfreqrange.

- **Test Dout:**

Table 35.5-4. Test Dout in HS RX Control of Lane 0

| r-1'b0 | r-6'b0   | r-1'b0 |
|--------|--|--------|
| 1'b0   | HS operating frequency range selection (hsfreqrange) | 1'b0   |

When [CSI\\_HOST\\_PHY\\_TESTDIN](#)[7] is 0, Test Dout[6:1] reflects the value of the programmed hsfreqrange.

#### Others

Other test codes are reserved.

## 35.5.4 Descrambler

Data scrambling uses randomization techniques to mitigate electromagnetic interference (EMI) and radio frequency (RF) self-interference. This spreads the transmission energy of the link across a wider frequency band.

The transmitted data is scrambled with a Pseudo-Random-Bit-Stream (PRBS) to reduce the likelihood of repetitive patterns on a lane basis. The PRBS is generated using a Linear Feedback Shift Register (LFSR) that implements the generator polynomial:

$$G(x) = x^{16} + x^5 + x^4 + x^3 + 1 \quad (35.1)$$

Each data lane has an instance of the de-scrambling block. Set [CSI\\_HOST\\_SCRAMBLE\\_ENABLE](#) to 1 to enable this block. Each lane can be configured with a different 16-bit LFSR seed value via [CSI\\_HOST\\_SCRAMBLE\\_SEED\\_LANE \$n\$](#) .

The default seed values after resetting the controller are listed in [35.5-5](#).

**Table 35.5-5. Scrambler PRBS Initial Seed Values for Lane 1 and Lane 2**

| Lane | Initial Seed Value |
|------|--------------------|
| 1    | 0x1008             |
| 2    | 0x1188             |

### 35.5.5 Error Management

The MIPI CSI-2 host analyzes received packets to identify protocol errors. Possible errors are listed in [Table 35.5-6](#). These errors serve as interrupt sources and can generate the CSI\_INTR signal. See [Section 35.6 Interrupts](#) for more details.

**Table 35.5-6. Detectable Errors by MIPI CSI-2 Host**

| Error/Interrupt Source                 | Description  | Corresponding Register Field  |
|--|--|---|
| PHY_ERRSOTSYNCHS_ $n$ ( $n$ : 0-1)     | Start-of-transmission error (no synchronization achieved) on data lane $n$ | <a href="#">CSI_HOST_ST_PHY_ERRSOTSYNCHS_<math>n</math> (<math>n</math>: 0-1)</a>     |
| ERR_ECC_DOUBLE                         | Header ECC contains at least two errors (unrecoverable)                    | <a href="#">CSI_HOST_ST_ERR_ECC_DOUBLE</a>  |
| SHORTER_PAYLOAD                        | Reported word count exceeds received word count (unrecoverable)            | <a href="#">CSI_HOST_ST_SHORTER_PAYLOAD</a>   |
| ERR_F_BNDRY_MATCH_VC $n$ ( $n$ : 0-15) | Error matching frame start with frame end for virtual channel $n$          | <a href="#">CSI_HOST_ST_ERR_F_BNDRY_MATCH_VC<math>n</math> (<math>n</math>: 0-15)</a> |
| ERR_F_SEQ_VC $n$ ( $n$ : 0-15)         | Incorrect frame sequence detected on virtual channel $n$                   | <a href="#">CSI_HOST_ST_ERR_F_SEQ_VC<math>n</math> (<math>n</math>: 0-15)</a>         |
| ERR_FRAME_DATA_VC $n$ ( $n$ : 0-15)    | At least one CRC error in the last received frame on virtual channel $n$   | <a href="#">CSI_HOST_ST_ERR_FRAME_DATA_VC<math>n</math> (<math>n</math>: 0-15)</a>    |
| ERR_CRC_VC $n$ ( $n$ : 0-15)           | Payload CRC error detected on virtual channel $n$                          | <a href="#">CSI_HOST_ST_ERR_CRC_VC<math>n</math> (<math>n</math>: 0-15)</a>           |
| ERR_ID_VC $n$ ( $n$ : 0-15)            | Unrecognized or unimplemented data type detected on virtual channel $n$    | <a href="#">CSI_HOST_ST_ERR_ID_VC<math>n</math> (<math>n</math>: 0-15)</a>            |

|  |  |  |
|--|--|--|
| ERR_ECC_CORRECTED_VC $n$ ( $n$ : 0-15) | Checksum error detected on virtual channel $n$                                       | CSI_HOST_ST_ERR_ECC_CORRECTED_VC $n$ ( $n$ : 0-15) |
| PHY_ERRSOTHS_ $n$ ( $n$ : 0-1)         | Start-of-transmission error (synchronization can still be achieved) on data lane $n$ | CSI_HOST_ST_PHY_ERRSOTHS_ $n$ ( $n$ : 0-1)         |
| PHY_ERRESC_ $n$ ( $n$ : 0-1)           | Escape entry error (ULPS) on data lane $n$   | CSI_HOST_ST_PHY_ERRESC_ $n$ ( $n$ : 0-1)           |

**Note:**

MIPI CSI does not support virtual channel interleaving. Before starting transmission, verify which virtual channel is in use. Additionally, read error information from the specified virtual channel to detect any errors.

A reset is recommended for all errors in “\*\_FATAL\_REG” registers.

## 35.6 Interrupts

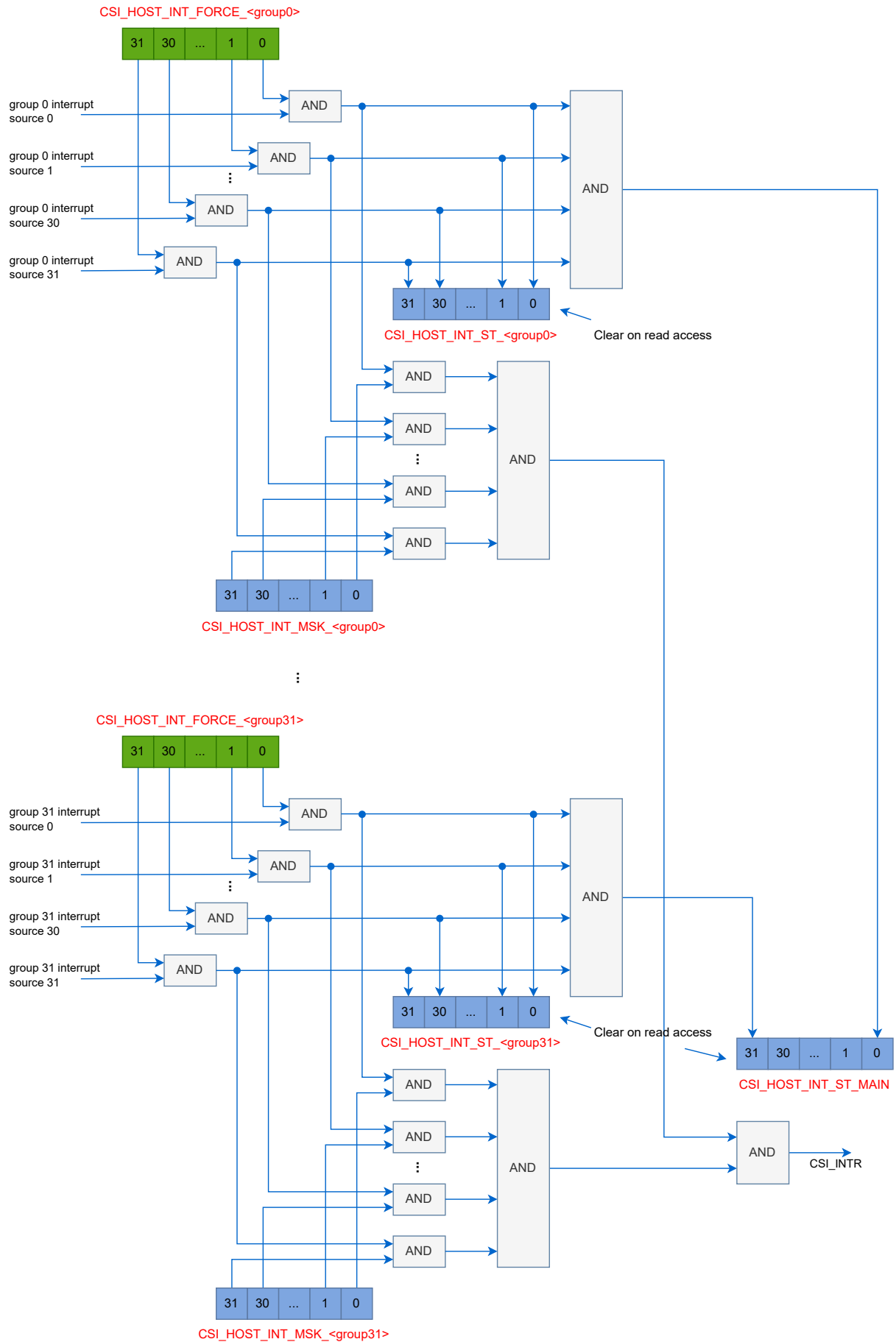
ESP32-P4's MIPI CSI can generate the CSI\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#).

The CSI\_HOST\_INT\_ST\_<group> registers report error conditions and trigger the CSI\_INTR interrupt signal.

You can mask the interrupt pin by using the CSI\_HOST\_INT\_MSK\_<group> registers. All errors are masked by default. Set any bit of these registers to 1 to enable the specific error interrupt. The error asserts the respective bit in the CSI\_HOST\_INT\_ST\_<group> register. The CSI\_HOST\_INT\_ST\_<group> registers clear after a read operation.

Setting any bit of the Interrupt Force registers (CSI\_HOST\_INT\_FORCE\_<group>) to 1 triggers the corresponding interrupt without needing to activate the error conditions. These registers are for test purposes.

Figure [35.6-1](#) shows the interrupt mechanism:



The interrupt signal CSI\_INTR can be generated by the following internal interrupt sources (see Table 35.5-6 *Detectable Errors by MIPI CSI-2 Host* for details interrupt source description):

- PHY Fatal Interrupt:
  - PHY\_ERRSOTSYNCHS\_ *n* (*n*: 0-1)
- Packet Fatal Interrupt:
  - ERR\_ECC\_DOUBLE
  - SHORTER\_PAYLOAD
- Boundary Frame Fatal Interrupt:
  - ERR\_F\_BNDRY\_MATCH\_VC*n* (*n*: 0-15)
- Sequence Frame Fatal Interrupt:
  - ERR\_F\_SEQ\_VC*n* (*n*: 0-15)
- CRC Frame Fatal Interrupt:
  - ERR\_FRAME\_DATA\_VC*n* (*n*: 0-15)
- Payload CRC Fatal Interrupt:
  - ERR\_CRC\_VC*n* (*n*: 0-15)
- Data ID Interrupt:
  - ERR\_ID\_VC*n* (*n*: 0-15)
- ECC Corrected Interrupt:
  - ERR\_ECC\_CORRECTED\_VC*n* (*n*: 0-15)
- PHY Interrupt:
  - PHY\_ERRSOTHS\_ *n* (*n*: 0-1)
  - PHY\_ERRESC\_ *n* (*n*: 0-1)

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 *Interrupt Matrix* > Section 11.2 *Interrupt Terminology in ESP32-P4*.

## 35.7 Programming Procedures

This section describes how to configure the MIPI RX D-PHY and the MIPI CSI-2 host for image data reception. MIPI CSI receives image data only in high-speed data reception mode.

### 35.7.1 Start High-Speed Data Reception

#### 35.7.1.1 Clock and Reset

- Set `HP_SYS_CLKRST_CSI_HOST_SYS_CLK_EN` to 1 to enable the MIPI CSI clock.



- Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_CSI\\_HOST](#) to 0 to release the MIPI CSI reset.
- Configure [HP\\_SYS\\_CLKRST\\_MIPI\\_CSI\\_DPHY\\_CLK\\_SRC\\_SEL](#) to select a proper clock source for the MIPI RX D-PHY configuration clock.
- Set [HP\\_SYS\\_CLKRST\\_MIPI\\_CSI\\_DPHY\\_CFG\\_CLK\\_EN](#) to 1 to enable the MIPI RX D-PHY configuration clock.
- Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_CSI\\_BRG](#) to 1 to release the CSI\_Bridge module of the ISP and reset the ISP.

### 35.7.1.2 MIPI RX D-PHY and MIPI Host Initialization

- Clear [CSI\\_HOST\\_CSI2\\_RESETN](#) to reset the CSI\_HOST controller logic.
- Set [CSI\\_HOST\\_PHY\\_TESTCLR](#) to 1, then clear [CSI\\_HOST\\_PHY\\_TESTCLR](#) to reset the test code logic.
- Configure the MIPI RX D-PHY frequency range in test code 0x44 using the MIPI RX D-PHY programming interface.
- Configure [CSI\\_HOST\\_N\\_LANES](#) to define the number of active lanes in the system.
- Set [CSI\\_HOST\\_PHY\\_SHUTDOWNZ](#) and [CSI\\_HOST\\_DPHY\\_RSTZ](#) to 1 to release the MIPI RX D-PHY from the reset state.
- Set the corresponding bit in the [CSI\\_HOST\\_INT\\_MSK\\_\\*\\_REG](#) register to 1 to enable the error interrupt.
- Configure the descrambler function if needed.
- Set [CSI\\_HOST\\_CSI2\\_RESETN](#) to 1 to release the CSI\_HOST reset.
- Wait until [CSI\\_HOST\\_PHY\\_STOPSTATEDATA\\_n](#) and [CSI\\_HOST\\_PHY\\_STOPSTATECLK](#) are 1.
- Start the camera image capture.

### 35.7.2 Stop High-Speed Data Reception

- Disable related channels in . Wait until is disabled. Refer to Chapter [4 VDMA Controller \(VDMA\)](#).
- Reset the ISP. Refer to Chapter [32 Image Signal Processor \(ISP\)](#).
- Set [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_CSI\\_HOST](#) to 1 to reset the MIPI CSI.

## 35.8 Register Summary

The addresses in this section are relative to CSI Host base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <b>Version Register</b>                          |   |         |        |
| <a href="#">CSI_HOST_VERSION_REG</a>             | CSI_HOST version control register                   | 0x0000  | RO     |
| <b>Configuration Registers</b>                   |   |         |        |
| <a href="#">CSI_HOST_N_LANES_REG</a>             | Active lane number configuration register           | 0x0004  | R/W    |
| <a href="#">CSI_HOST_CSI2_RESETN_REG</a>         | CSI_HOST reset control register                     | 0x0008  | R/W    |
| <a href="#">CSI_HOST_PHY_SHUTDOWNZ_REG</a>       | RX D-PHY Shut-Down state control register           | 0x0040  | R/W    |
| <a href="#">CSI_HOST_DPHY_RSTZ_REG</a>           | RX D-PHY reset control register                     | 0x0044  | R/W    |
| <a href="#">CSI_HOST_PHY_RX_REG</a>              | RX D-PHY RX-related signal status register          | 0x0048  | RO     |
| <a href="#">CSI_HOST_PHY_TEST_CTRL0_REG</a>      | RX D-PHY test code interface control register 0     | 0x0050  | R/W    |
| <a href="#">CSI_HOST_PHY_TEST_CTRL1_REG</a>      | RX D-PHY test code interface control register 1     | 0x0054  | varies |
| <a href="#">CSI_HOST_SCRAMBLING_REG</a>          | Descrambler enable register                         | 0x0300  | R/W    |
| <a href="#">CSI_HOST_SCRAMBLING_SEED1_REG</a>    | Data lane 0 Descrambler seed value control register | 0x0304  | R/W    |
| <a href="#">CSI_HOST_SCRAMBLING_SEED2_REG</a>    | Data lane 1 Descrambler seed value control register | 0x0308  | R/W    |
| <b>Interrupt Registers</b>                       |   |         |        |
| <a href="#">CSI_HOST_INT_ST_MAIN_REG</a>         | Main interrupt status register                      | 0x000C  | RC     |
| <a href="#">CSI_HOST_INT_ST_PHY_FATAL_REG</a>    | RX D-PHY fatal interrupt status register            | 0x00E0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_PHY_FATAL_REG</a>   | RX D-PHY fatal interrupt mask register              | 0x00E4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_PHY_FATAL_REG</a> | RX D-PHY fatal interrupt force register             | 0x00E8  | R/W    |
| <a href="#">CSI_HOST_INT_ST_PKT_FATAL_REG</a>    | Packet fatal interrupt status register              | 0x00F0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_PKT_FATAL_REG</a>   | Packet fatal interrupt mask register                | 0x00F4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_PKT_FATAL_REG</a> | Packet fatal interrupt force register               | 0x00F8  | R/W    |
| <a href="#">CSI_HOST_INT_ST_PHY_REG</a>          | RX D-PHY interrupt status register                  | 0x0110  | RC     |
| <a href="#">CSI_HOST_INT_MSK_PHY_REG</a>         | RX D-PHY interrupt mask register                    | 0x0114  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_PHY_REG</a>       | RX D-PHY interrupt force register                   | 0x0118  | R/W    |

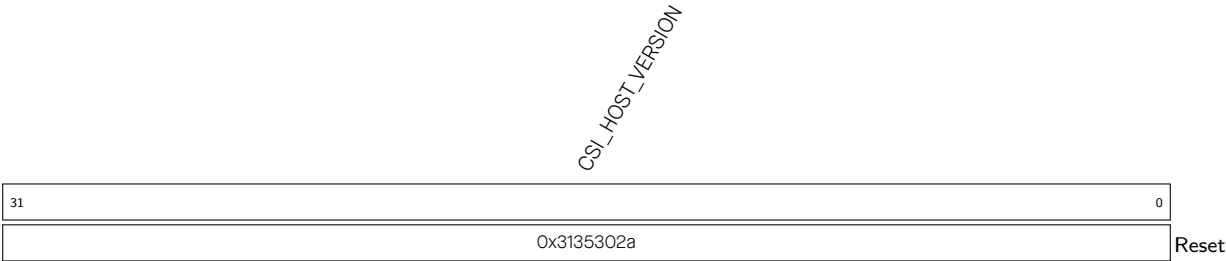
| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">CSI_HOST_INT_ST_BNDRY_FRAME_FATAL_REG</a>    | Frame boundary fatal interrupt status register                | 0x0280  | RC     |
| <a href="#">CSI_HOST_INT_MSK_BNDRY_FRAME_FATAL_REG</a>   | Frame boundary fatal interrupt mask register                  | 0x0284  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_BNDRY_FRAME_FATAL_REG</a> | Frame boundary fatal interrupt force register                 | 0x0288  | R/W    |
| <a href="#">CSI_HOST_INT_ST_SEQ_FRAME_FATAL_REG</a>      | Frame sequence fatal interrupt status register                | 0x0290  | RC     |
| <a href="#">CSI_HOST_INT_MSK_SEQ_FRAME_FATAL_REG</a>     | Frame sequence fatal interrupt mask register                  | 0x0294  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_SEQ_FRAME_FATAL_REG</a>   | Frame sequence fatal interrupt force register                 | 0x0298  | R/W    |
| <a href="#">CSI_HOST_INT_ST_CRC_FRAME_FATAL_REG</a>      | Frame CRC fatal interrupt status register                     | 0x02A0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_CRC_FRAME_FATAL_REG</a>     | Frame CRC fatal interrupt mask register                       | 0x02A4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_CRC_FRAME_FATAL_REG</a>   | Frame CRC fatal interrupt force register                      | 0x02A8  | R/W    |
| <a href="#">CSI_HOST_INT_ST_PLD_CRC_FATAL_REG</a>        | Payload CRC fatal interrupt status register                   | 0x02B0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_PLD_CRC_FATAL_REG</a>       | Payload CRC fatal interrupt mask register                     | 0x02B4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_PLD_CRC_FATAL_REG</a>     | Payload CRC fatal interrupt force register                    | 0x02B8  | R/W    |
| <a href="#">CSI_HOST_INT_ST_DATA_ID_REG</a>              | Data ID interrupt status register                             | 0x02C0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_DATA_ID_REG</a>             | Data ID interrupt mask register                               | 0x02C4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_DATA_ID_REG</a>           | Data ID interrupt force register                              | 0x02C8  | R/W    |
| <a href="#">CSI_HOST_INT_ST_ECC_CORRECTED_REG</a>        | Header error detected and corrected interrupt status register | 0x02D0  | RC     |
| <a href="#">CSI_HOST_INT_MSK_ECC_CORRECTED_REG</a>       | Header error detected and corrected interrupt mask register   | 0x02D4  | R/W    |
| <a href="#">CSI_HOST_INT_FORCE_ECC_CORRECTED_REG</a>     | Header error detected and corrected interrupt force register  | 0x02D8  | R/W    |
| <b>Status Register</b>                                   |   |         |        |
| <a href="#">CSI_HOST_PHY_STOPSTATE_REG</a>               | RX D-PHY stop state signal status register                    | 0x004C  | RO     |

### 35.9 Registers

The addresses in this section are relative to CSI Host base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

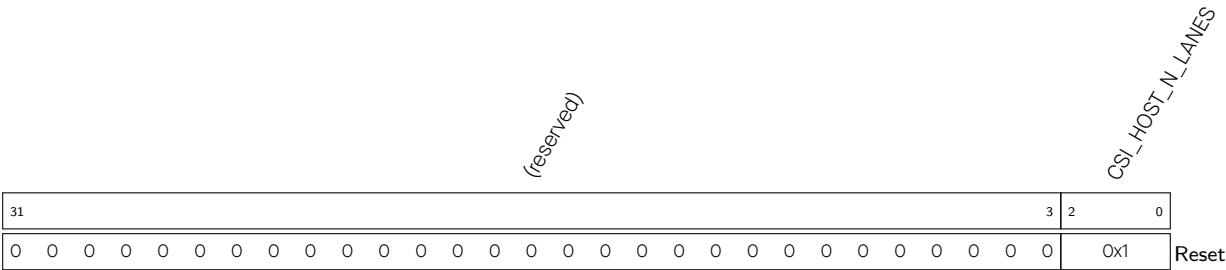
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 35.1. CSI\_HOST\_VERSION\_REG (0x0000)



**CSI\_HOST\_VERSION** Version control register. (RO)

Register 35.2. CSI\_HOST\_N\_LANES\_REG (0x0004)

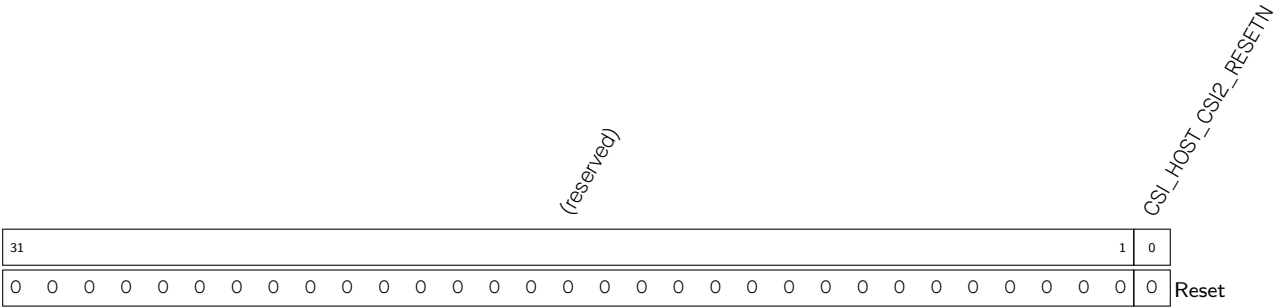


**CSI\_HOST\_N\_LANES** Configures the number of active lanes that the MIPI CSI-2 host uses to receive the camera device data. This can only be updated when the RX D-PHY lane is in stop state.

- 0: Data lane 0 is active
- 1: Both data lane 0 and data lane 1 are active
- Other values: Invalid

(R/W)

Register 35.3. CSI\_HOST\_CSI2\_RESETN\_REG (0x0008)



**CSI\_HOST\_CSI2\_RESETN** Configures whether to reset the internal logic of the MIPI CSI-2 host controller.

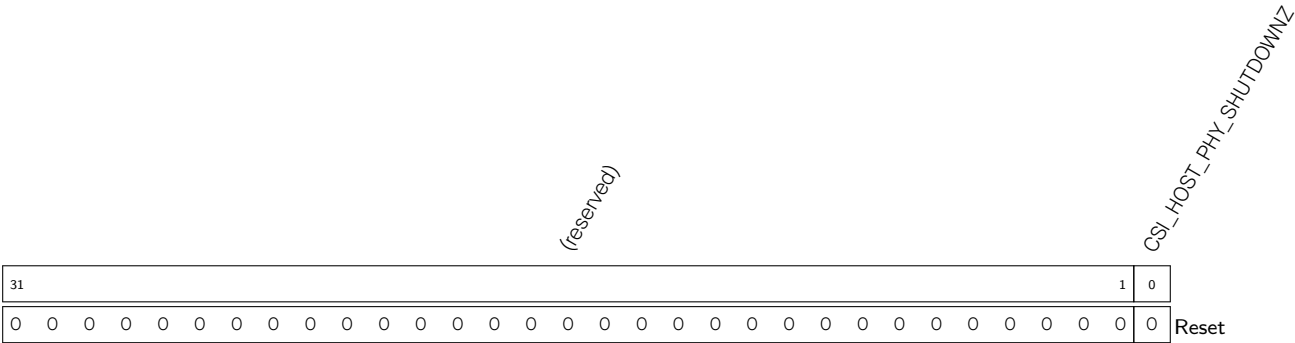
0: Reset

1: Release the reset

This register only affects the internal logic of the controller. It will not reset the configuration to default values.

(R/W)

Register 35.4. CSI\_HOST\_PHY\_SHUTDOWNZ\_REG (0x0040)



**CSI\_HOST\_PHY\_SHUTDOWNZ** Configures whether to enable the Shut-Down state of the RX D-PHY.

0: Enable

1: Disable

(R/W)

## Register 35.5. CSI\_HOST\_DPHY\_RSTZ\_REG (0x0044)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_DPHY_RSTZ |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                  | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**CSI\_HOST\_DPHY\_RSTZ** Configures whether to reset the RX D-PHY digital circuitry.

0: Reset

1: Release the reset

(R/W)

## Register 35.6. CSI\_HOST\_PHY\_RX\_REG (0x0048)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |    |    |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |    | CSI_HOST_PHY_RXCLKACTIVEHS<br>CSI_HOST_PHY_RXULPSCLKNOT |    |    |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_PHY_RXULPSESC_1<br>CSI_HOST_PHY_RXULPSESC_0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   | 18 | 17  | 16 | 15 |   |   |   |   |   |   |   |   |   |   | 2 | 1 | 0          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0   | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**CSI\_HOST\_PHY\_RXULPSESC\_***n* (*n*: 0-1) Represents whether data lane *n* has entered the Ultra Low Power State.

0: Entered

1: Not entered

(RO)

**CSI\_HOST\_PHY\_RXULPSCLKNOT** Represents whether RX D-PHY clock lane has entered the Ultra Low Power State.

0: Entered

1: Not entered

(RO)

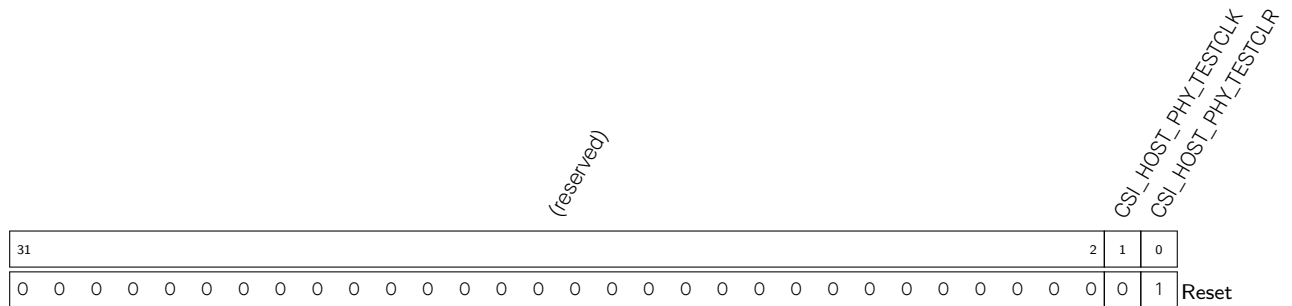
**CSI\_HOST\_PHY\_RXCLKACTIVEHS** Represents whether RX D-PHY clock lane is actively receiving a DDR clock.

0: Not actively receiving

1: Actively receiving

(RO)

## Register 35.7. CSI\_HOST\_PHY\_TEST\_CTRL0\_REG (0x0050)



**CSI\_HOST\_PHY\_TESTCLR** Configures whether to initialize the test code interface.

0: Not initialize

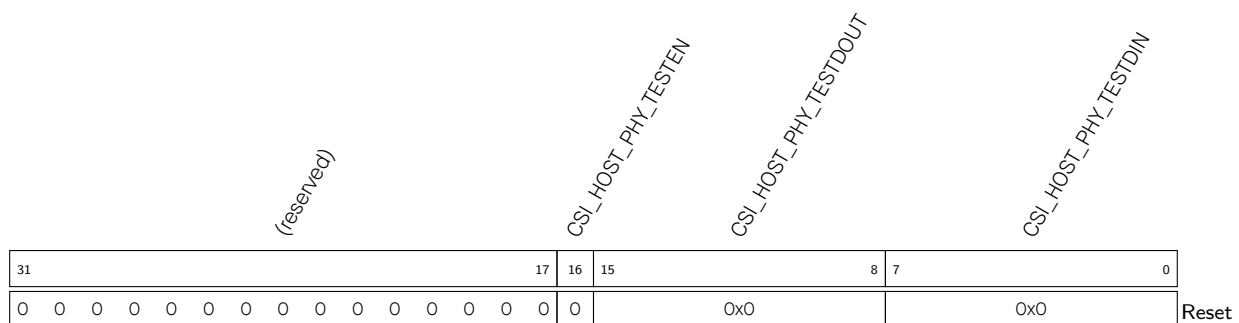
1: Initialize

To ensure the analog programmability default values are preset, this bit must be set to 1 then clear to 0 after power-up.

(R/W)

**CSI\_HOST\_PHY\_TESTCLK** Configures clock to capture [CSI\\_HOST\\_PHY\\_TESTDIN](#) bus contents into D-PHY test code logic, with [CSI\\_HOST\\_PHY\\_TESTEN](#) controlling the operation selection. (R/W)

## Register 35.8. CSI\_HOST\_PHY\_TEST\_CTRL1\_REG (0x0054)



**CSI\_HOST\_PHY\_TESTDIN** Configures the 8-bit data input of the test code interface for programming internal registers and accessing test functionalities. (R/W)

**CSI\_HOST\_PHY\_TESTDOUT** Represents the 8-bit data output of the test code interface for reading data and other probing functionalities. (RO)

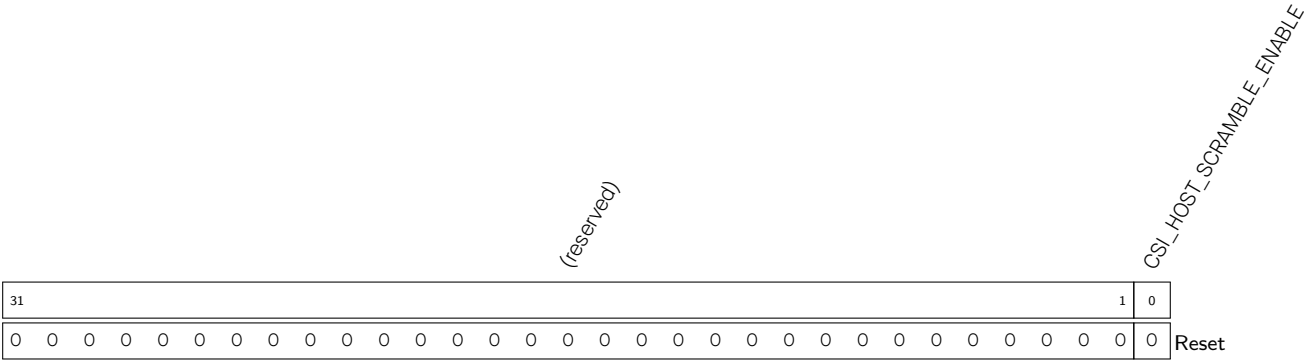
**CSI\_HOST\_PHY\_TESTEN** Configures whether to performs the test data write operation of the test code interface on the rising edge or the falling edge of [CSI\\_HOST\\_PHY\\_TESTCLK](#).

0: On the rising edge

1: On the falling edge

(R/W)

Register 35.9. CSI\_HOST\_SCRAMBLING\_REG (0x0300)



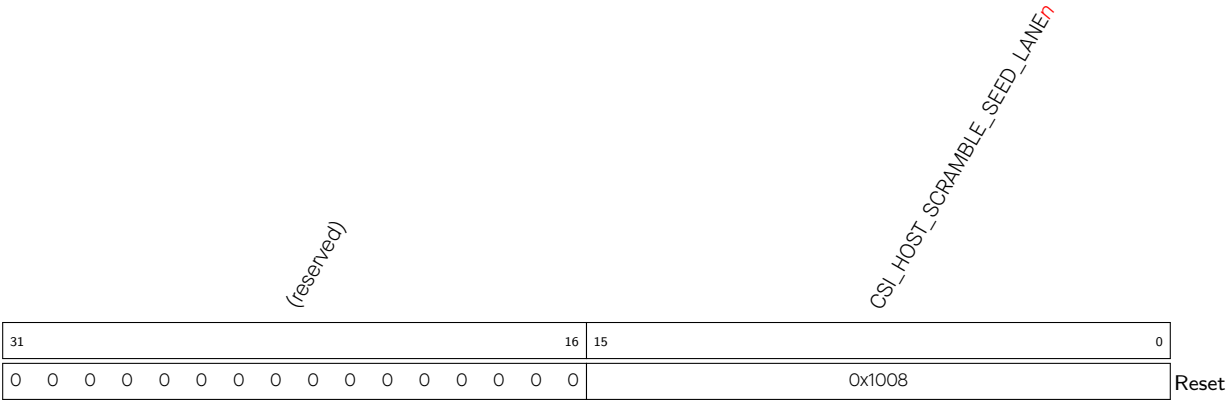
**CSI\_HOST\_SCRAMBLE\_ENABLE** Configures whether to enable the descrambler.

0: Disable

1: Enable

(R/W)

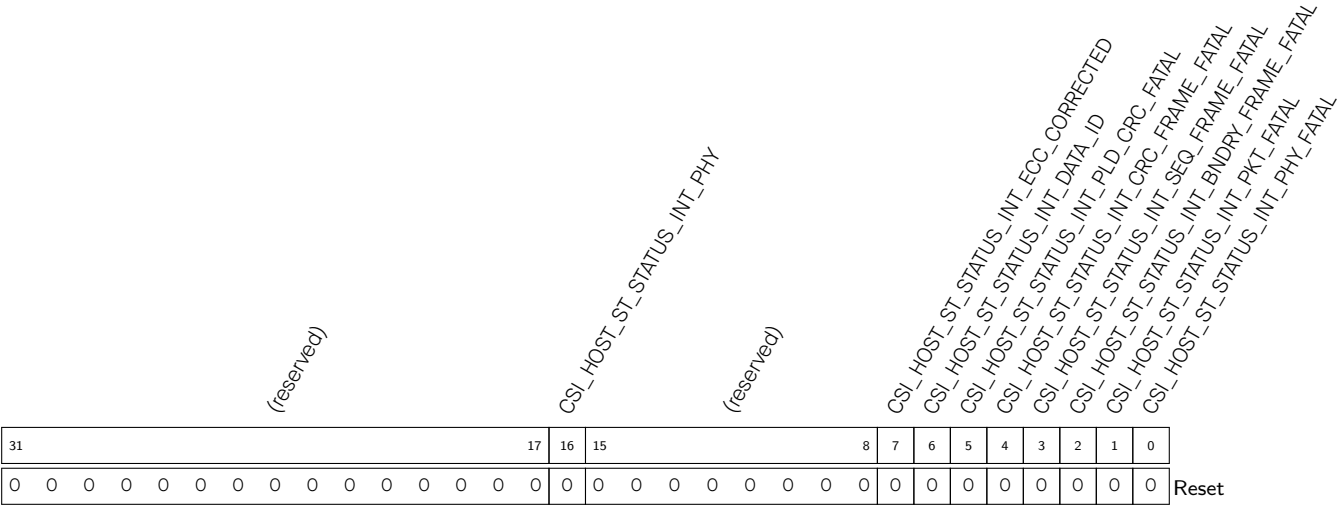
Register 35.10. CSI\_HOST\_SCRAMBLING\_SEED<sub>*n*</sub>\_REG (*n*: 1-2) (0x0300 + 0x04\**n*)



**CSI\_HOST\_SCRAMBLE\_SEED\_LANE<sub>*n-1*</sub>** Configures the seed value used by the descrambler for lane *n-1*. (R/W)

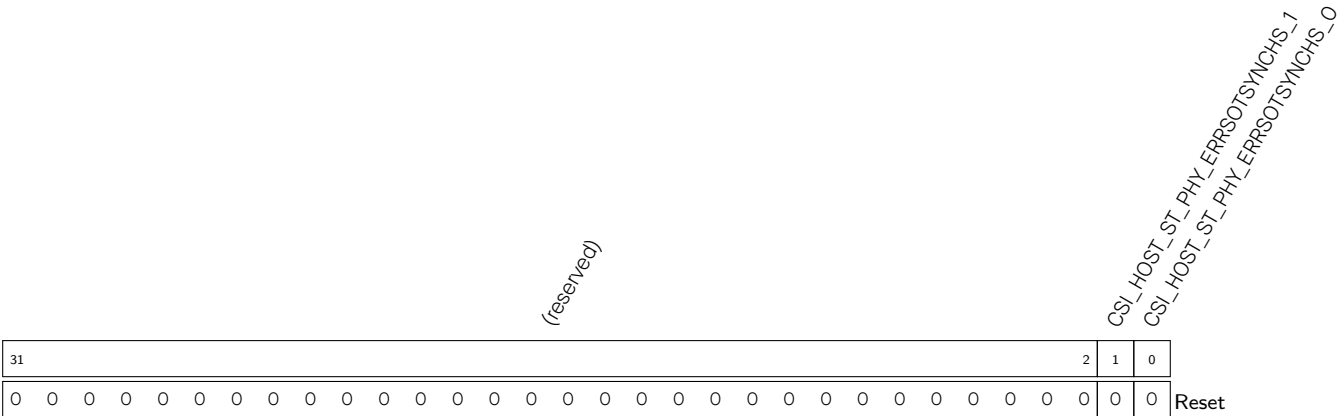


Register 35.11. CSI\_HOST\_INT\_ST\_MAIN\_REG (0x000C)



- CSI\_HOST\_ST\_STATUS\_INT\_PHY\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_PHY\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_PKT\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_PKT\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_BNDRY\_FRAME\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_BNDRY\_FRAME\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_SEQ\_FRAME\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_SEQ\_FRAME\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_CRC\_FRAME\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_CRC\_FRAME\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_PLD\_CRC\_FATAL Represents the status of CSI\_HOST\_INT\_ST\_PLD\_CRC\_FATAL\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_DATA\_ID Represents the status of CSI\_HOST\_INT\_ST\_DATA\_ID\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_ECC\_CORRECTED Represents the status of CSI\_HOST\_INT\_ST\_ECC\_CORRECTED\_REG. (RC)
- CSI\_HOST\_ST\_STATUS\_INT\_PHY Represents the status of CSI\_HOST\_INT\_PHY\_REG. (RC)

Register 35.12. CSI\_HOST\_INT\_ST\_PHY\_FATAL\_REG (0x00E0)



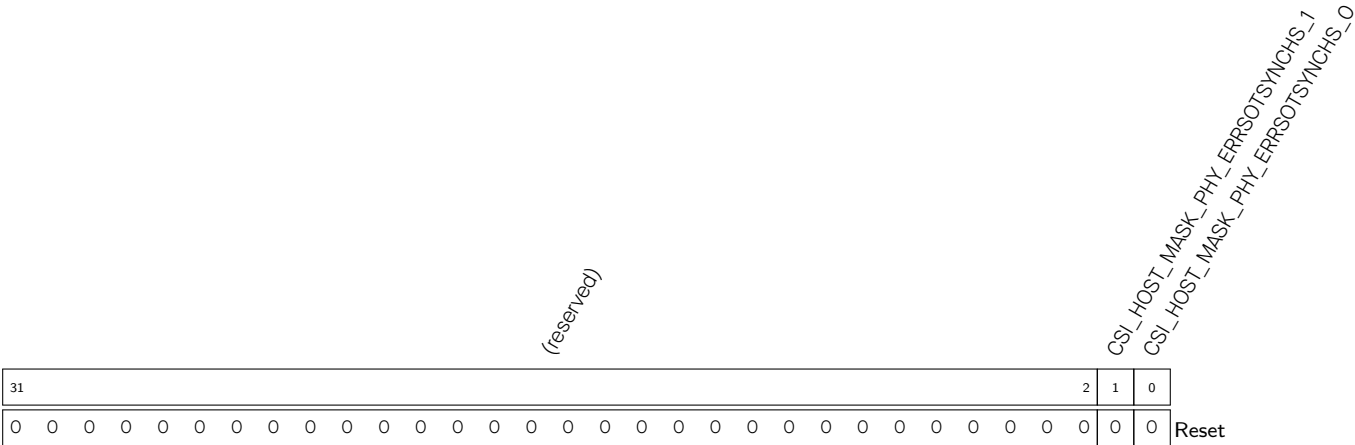
CSI\_HOST\_ST\_PHY\_ERRSOTSYNCHS\_ *n* (*n*: 0-1) Represents whether the PHY\_ERRSOTSYNCHS\_ *n* error occurs.

0: Do not occur

1: Occur

(RC)

Register 35.13. CSI\_HOST\_INT\_MSK\_PHY\_FATAL\_REG (0x00E4)



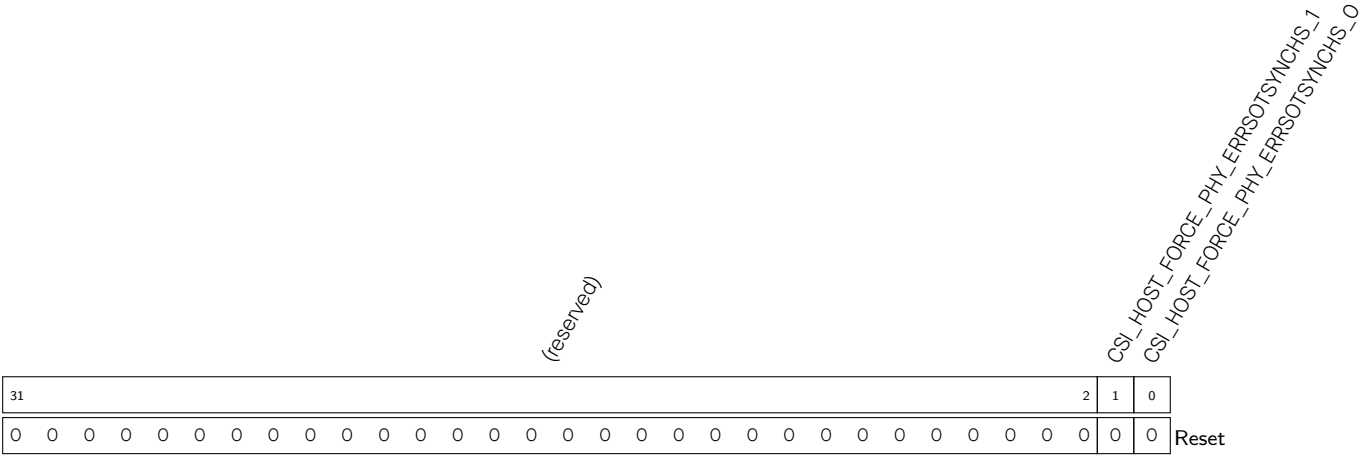
CSI\_HOST\_MASK\_PHY\_ERRSOTSYNCHS\_ *n* (*n*: 0-1) Configures whether to mask CSI\_HOST\_ST\_PHY\_ERRSOTSYNCHS\_ *n*.

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.14. CSI\_HOST\_INT\_FORCE\_PHY\_FATAL\_REG (0x00E8)



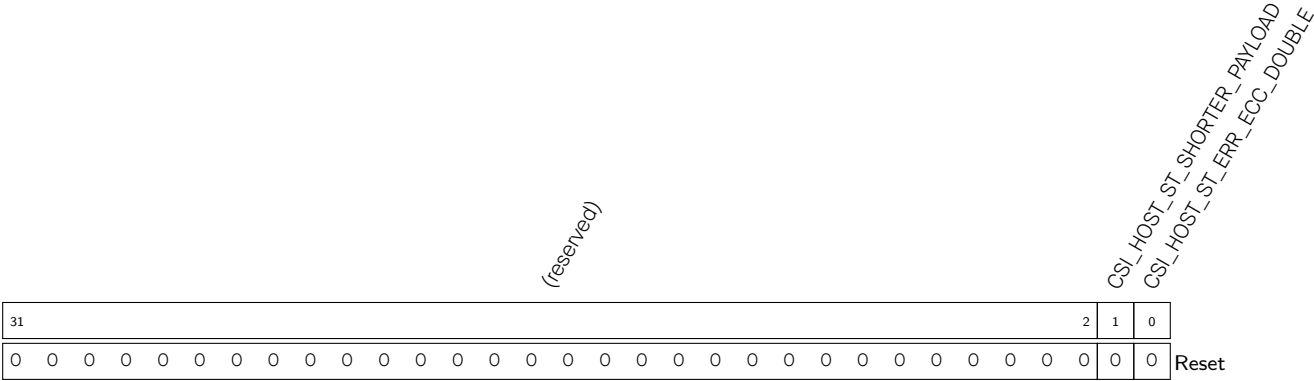
**CSI\_HOST\_FORCE\_PHY\_ERRSOTSYNCHS\_n** (*n*: 0-1) Configures whether to force set [CSI\\_HOST\\_ST\\_PHY\\_ERRSOTSYNCHS\\_n](#) to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.15. CSI\_HOST\_INT\_ST\_PKT\_FATAL\_REG (0x00F0)



**CSI\_HOST\_ST\_ERR\_ECC\_DOUBLE** Represents whether the ERR\_ECC\_DOUBLE error occurs.

0: Do not occur

1: Occur

(RC)

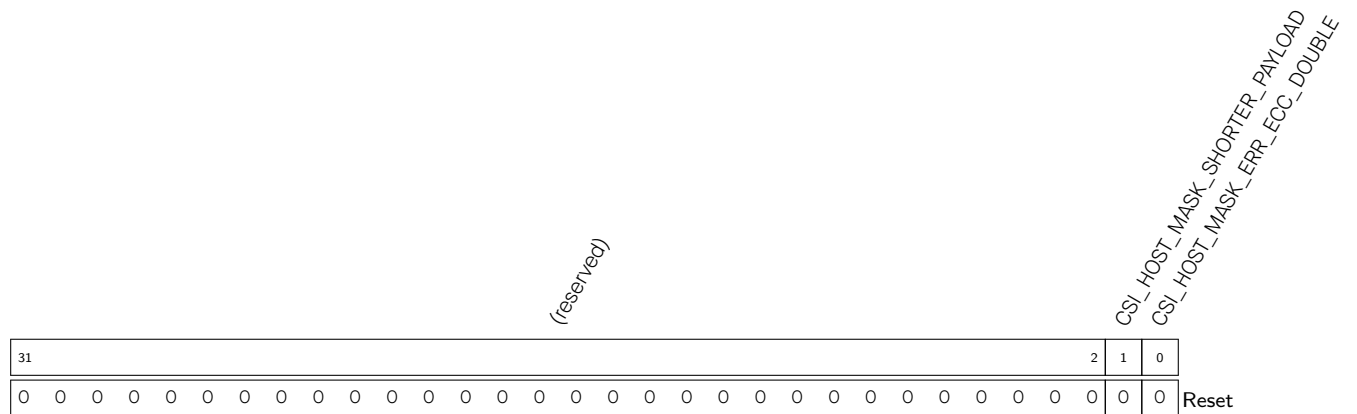
**CSI\_HOST\_ST\_SHORTER\_PAYLOAD** Represents whether the SHORTER\_PAYLOAD error occurs.

0: Do not occur

1: Occur

(RC)

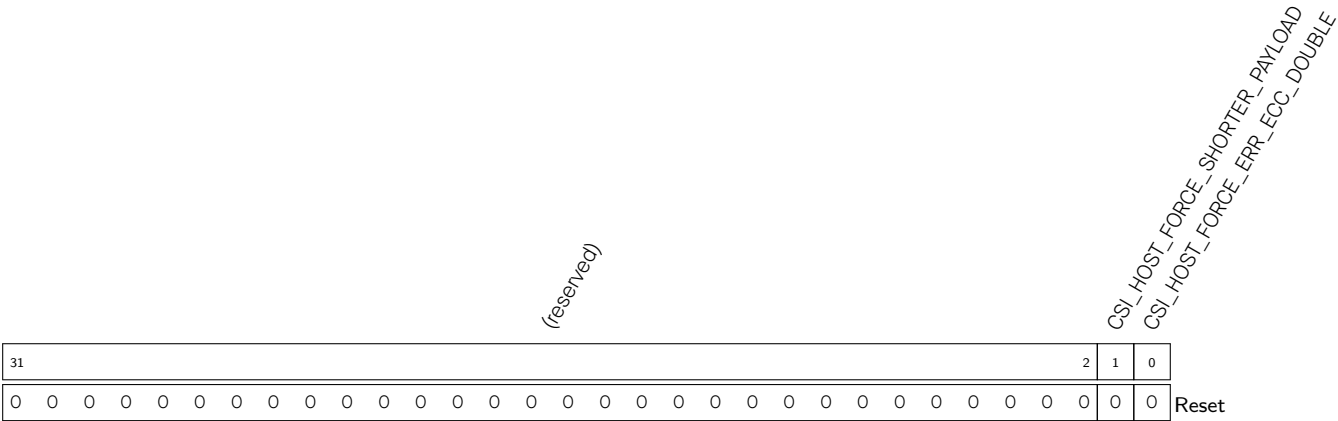
### Register 35.16. CSI\_HOST\_INT\_MSK\_PKT\_FATAL\_REG (0x00F4)



|                               |            |         |    |      |
|-------------------------------|------------|---------|----|------|
| CSI_HOST_MASK_ERR_ECC_DOUBLE  | Configures | whether | to | mask |
| CSI_HOST_ST_ERR_ECC_DOUBLE.   |            |         |    |      |
| 0: Mask the error interrupt   |            |         |    |      |
| 1: Enable the error interrupt |            |         |    |      |
| (R/W)                         |            |         |    |      |

| CSI_HOST_MASK_SHORTER_PAYLOAD | Configures | whether | to | mask |
|-------------------------------|------------|---------|----|------|
| CSI_HOST_ST_SHORTER_PAYLOAD.  |            |         |    |      |
| 0: Mask the error interrupt   |            |         |    |      |
| 1: Enable the error interrupt |            |         |    |      |
| (R/W)                         |            |         |    |      |

Register 35.17. CSI\_HOST\_INT\_FORCE\_PKT\_FATAL\_REG (0x00F8)



CSI\_HOST\_FORCE\_ERR\_ECC\_DOUBLE

Configures whether to force set CSI\_HOST\_ST\_ERR\_ECC\_DOUBLE to 1.

0: Do not force set

1: Force set

(R/W)

CSI\_HOST\_FORCE\_SHORTER\_PAYLOAD

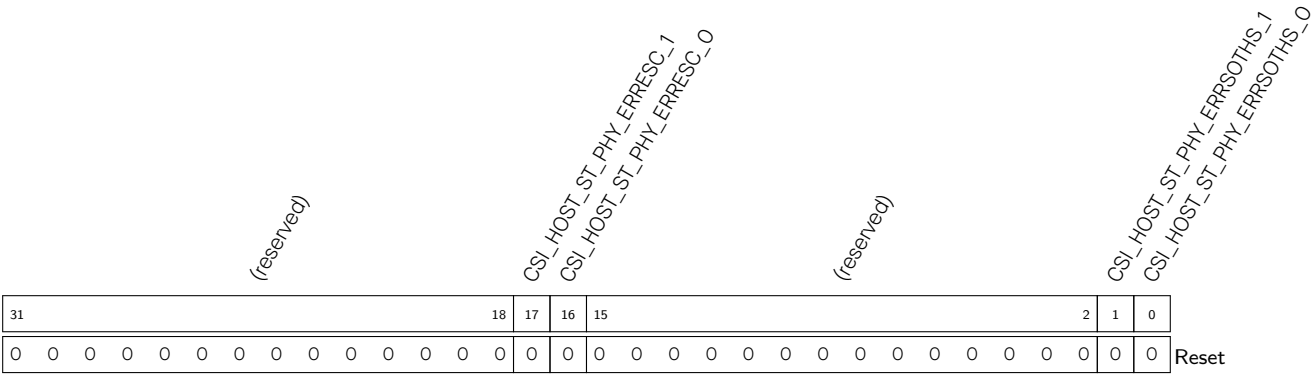
Configures whether to force set CSI\_HOST\_ST\_SHORTER\_PAYLOAD to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.18. CSI\_HOST\_INT\_ST\_PHY\_REG (0x0110)



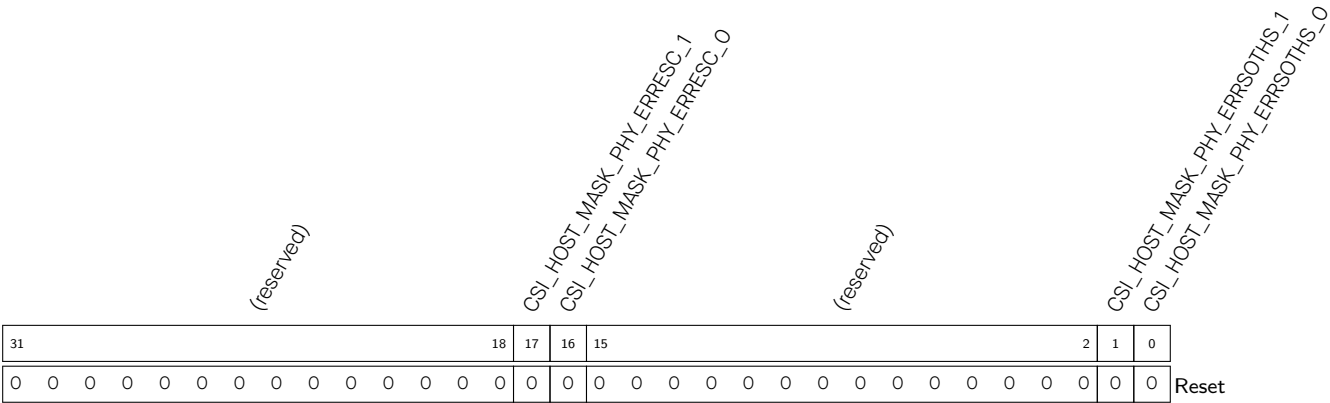
**CSI\_HOST\_ST\_PHY\_ERRSOTHS\_ *n* (*n*: 0-1)** Represents whether the PHY\_ERRSOTHS\_ *n* error occurs.

- 0: Do not occur
- 1: Occur (RC)

**CSI\_HOST\_ST\_PHY\_ERRESC\_ *n* (*n*: 0-1)** Represents whether the PHY\_ERRESC\_ *n* error occurs.

- 0: Do not occur
- 1: Occur (RC)

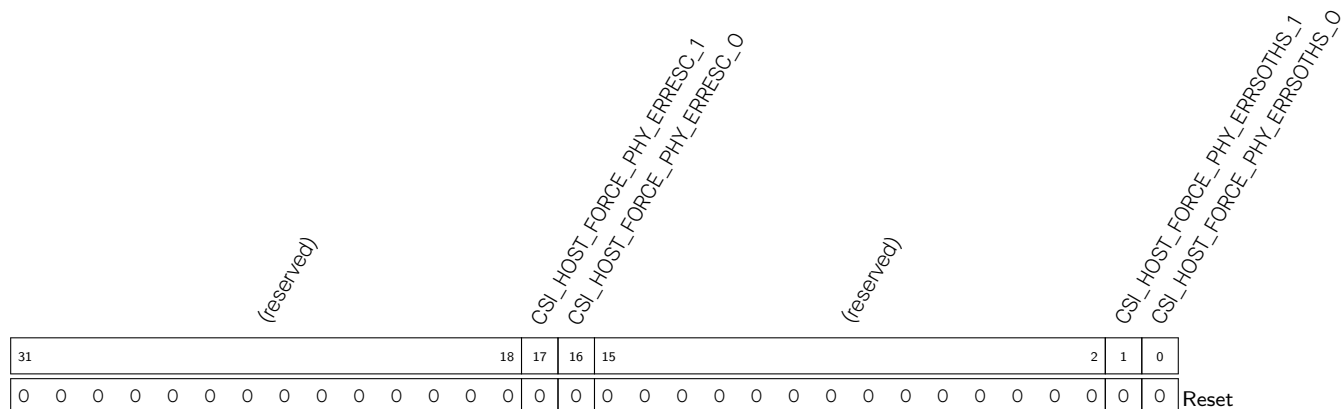
Register 35.19. CSI\_HOST\_INT\_MSK\_PHY\_REG (0x0114)



**CSI\_HOST\_MASK\_PHY\_ERRSOTHS\_ *n* (*n*: 0-1)** Configures whether to mask [CSI\\_HOST\\_ST\\_PHY\\_ERRSOTHS\\_ \*n\*](#).  
0: Mask the error interrupt  
1: Enable the error interrupt  
(R/W)

**CSI\_HOST\_MASK\_PHY\_ERRESC\_ *n* (*n*: 0-1)** Configures whether to mask [CSI\\_HOST\\_ST\\_PHY\\_ERRESC\\_ \*n\*](#).  
0: Mask the error interrupt  
1: Enable the error interrupt  
(R/W)

### Register 35.20. CSI\_HOST\_INT\_FORCE\_PHY\_REG (0x0118)



|  |                                 |
|--|---------------------------------|
| CSI_HOST_FORCE_PHY_ERRSOTHS_n (n: 0-1) | Configures whether to force set |
|--|---------------------------------|

CSI\_HOST\_ST\_PHY\_ERRSOTHS\_*n* to 1.

0: Do not force set

1: Force set

(R/W)

|                             |                                 |
|-----------------------------|---------------------------------|
| CSI_HOST_FORCE_PHY_ERRESC_0 | Configures whether to force set |
|-----------------------------|---------------------------------|

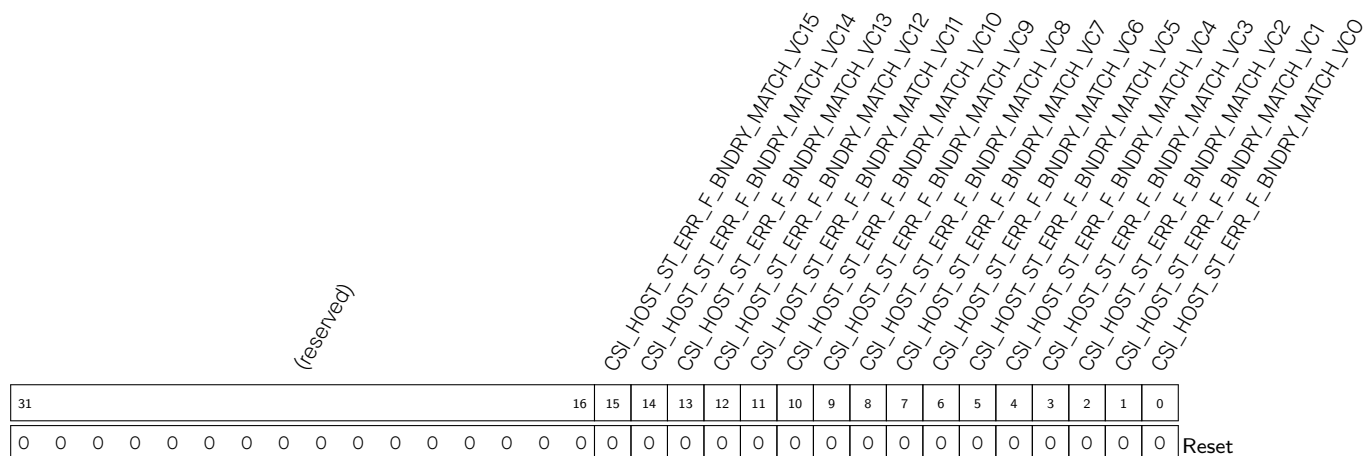
CSI\_HOST\_ST\_PHY\_ERRESC\_ *n* to 1.

0: Do not force set

1: Force set

(R/W)

### Register 35.21. CSI\_HOST\_INT\_ST\_BNDRY\_FRAME\_FATAL\_REG (0x0280)



CSI\_HOST\_ST\_ERR\_F\_BNDRY\_MATCH\_VC*n* (*n*: 0-15) Represents whether the  
ERR F BNDRY MATCH VC*n* error occurs.

0: Do not occur

1: Occur

(RC)



Register 35.22. CSI\_HOST\_INT\_MSK\_BNDRY\_FRAME\_FATAL\_REG (0x0284)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC15<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC14<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC13<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC12<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC11<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC10<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC9<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC8<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC7<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC6<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC5<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC4<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC3<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC2<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC1<br>CSI_HOST_MASK_ERR_F_BNDRY_MATCH_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

CSI\_HOST\_MASK\_ERR\_F\_BNDRY\_MATCH\_VC $n$  ( $n$ : 0-15) Configures whether to mask  
 CSI\_HOST\_ST\_ERR\_F\_BNDRY\_MATCH\_VC $n$ .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.23. CSI\_HOST\_INT\_FORCE\_BNDRY\_FRAME\_FATAL\_REG (0x0288)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC15<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC14<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC13<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC12<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC11<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC10<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC9<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC8<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC7<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC6<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC5<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC4<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC3<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC2<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC1<br>CSI_HOST_FORCE_ERR_F_BNDRY_MATCH_VC0 |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | Reset |   |   |   |   |   |   |   |

CSI\_HOST\_FORCE\_ERR\_F\_BNDRY\_MATCH\_VC $n$  ( $n$ : 0-15) Configures whether to force set  
 CSI\_HOST\_ST\_ERR\_F\_BNDRY\_MATCH\_VC $n$  to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.24. CSI\_HOST\_INT\_ST\_SEQ\_FRAME\_FATAL\_REG (0x0290)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_ST_ERR_F_SEQ_VC15<br>CSI_HOST_ST_ERR_F_SEQ_VC14<br>CSI_HOST_ST_ERR_F_SEQ_VC13<br>CSI_HOST_ST_ERR_F_SEQ_VC12<br>CSI_HOST_ST_ERR_F_SEQ_VC11<br>CSI_HOST_ST_ERR_F_SEQ_VC10<br>CSI_HOST_ST_ERR_F_SEQ_VC9<br>CSI_HOST_ST_ERR_F_SEQ_VC8<br>CSI_HOST_ST_ERR_F_SEQ_VC7<br>CSI_HOST_ST_ERR_F_SEQ_VC6<br>CSI_HOST_ST_ERR_F_SEQ_VC5<br>CSI_HOST_ST_ERR_F_SEQ_VC4<br>CSI_HOST_ST_ERR_F_SEQ_VC3<br>CSI_HOST_ST_ERR_F_SEQ_VC2<br>CSI_HOST_ST_ERR_F_SEQ_VC1<br>CSI_HOST_ST_ERR_F_SEQ_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

CSI\_HOST\_ST\_ERR\_F\_SEQ\_VC $n$  ( $n$ : 0-15) Represents whether the ERR\_F\_SEQ\_VC $n$  error occurs.

0: Do not occur

1: Occur

(RC)

Register 35.25. CSI\_HOST\_INT\_MSK\_SEQ\_FRAME\_FATAL\_REG (0x0294)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_MASK_ERR_F_SEQ_VC15<br>CSI_HOST_MASK_ERR_F_SEQ_VC14<br>CSI_HOST_MASK_ERR_F_SEQ_VC13<br>CSI_HOST_MASK_ERR_F_SEQ_VC12<br>CSI_HOST_MASK_ERR_F_SEQ_VC11<br>CSI_HOST_MASK_ERR_F_SEQ_VC10<br>CSI_HOST_MASK_ERR_F_SEQ_VC9<br>CSI_HOST_MASK_ERR_F_SEQ_VC8<br>CSI_HOST_MASK_ERR_F_SEQ_VC7<br>CSI_HOST_MASK_ERR_F_SEQ_VC6<br>CSI_HOST_MASK_ERR_F_SEQ_VC5<br>CSI_HOST_MASK_ERR_F_SEQ_VC4<br>CSI_HOST_MASK_ERR_F_SEQ_VC3<br>CSI_HOST_MASK_ERR_F_SEQ_VC2<br>CSI_HOST_MASK_ERR_F_SEQ_VC1<br>CSI_HOST_MASK_ERR_F_SEQ_VC0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

CSI\_HOST\_MASK\_ERR\_F\_SEQ\_VC $n$  ( $n$ : 0-15) Configures whether to mask

CSI\_HOST\_ST\_ERR\_F\_SEQ\_VC $n$ .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.26. CSI\_HOST\_INT\_FORCE\_SEQ\_FRAME\_FATAL\_REG (0x0298)

|            |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   | CSI_HOST_FORCE_ERR_F_SEQ_VC15<br>CSI_HOST_FORCE_ERR_F_SEQ_VC14<br>CSI_HOST_FORCE_ERR_F_SEQ_VC13<br>CSI_HOST_FORCE_ERR_F_SEQ_VC12<br>CSI_HOST_FORCE_ERR_F_SEQ_VC11<br>CSI_HOST_FORCE_ERR_F_SEQ_VC10<br>CSI_HOST_FORCE_ERR_F_SEQ_VC9<br>CSI_HOST_FORCE_ERR_F_SEQ_VC8<br>CSI_HOST_FORCE_ERR_F_SEQ_VC7<br>CSI_HOST_FORCE_ERR_F_SEQ_VC6<br>CSI_HOST_FORCE_ERR_F_SEQ_VC5<br>CSI_HOST_FORCE_ERR_F_SEQ_VC4<br>CSI_HOST_FORCE_ERR_F_SEQ_VC3<br>CSI_HOST_FORCE_ERR_F_SEQ_VC2<br>CSI_HOST_FORCE_ERR_F_SEQ_VC1<br>CSI_HOST_FORCE_ERR_F_SEQ_VC0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1  | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

CSI\_HOST\_FORCE\_ERR\_F\_SEQ\_VC $n$  ( $n$ : 0-15) Configures whether to force set CSI\_HOST\_ST\_ERR\_F\_SEQ\_VC $n$  to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.27. CSI\_HOST\_INT\_ST\_CRC\_FRAME\_FATAL\_REG (0x02A0)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_ST_ERR_FRAME_DATA_VC15<br>CSI_HOST_ST_ERR_FRAME_DATA_VC14<br>CSI_HOST_ST_ERR_FRAME_DATA_VC13<br>CSI_HOST_ST_ERR_FRAME_DATA_VC12<br>CSI_HOST_ST_ERR_FRAME_DATA_VC11<br>CSI_HOST_ST_ERR_FRAME_DATA_VC10<br>CSI_HOST_ST_ERR_FRAME_DATA_VC9<br>CSI_HOST_ST_ERR_FRAME_DATA_VC8<br>CSI_HOST_ST_ERR_FRAME_DATA_VC7<br>CSI_HOST_ST_ERR_FRAME_DATA_VC6<br>CSI_HOST_ST_ERR_FRAME_DATA_VC5<br>CSI_HOST_ST_ERR_FRAME_DATA_VC4<br>CSI_HOST_ST_ERR_FRAME_DATA_VC3<br>CSI_HOST_ST_ERR_FRAME_DATA_VC2<br>CSI_HOST_ST_ERR_FRAME_DATA_VC1<br>CSI_HOST_ST_ERR_FRAME_DATA_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

CSI\_HOST\_ST\_ERR\_FRAME\_DATA\_VC $n$  ( $n$ : 0-15) Represents whether the ERR\_FRAME\_DATA\_VC $n$  error occurs.

0: Do not occur

1: Occur

(RC)

Register 35.28. CSI\_HOST\_INT\_MSK\_CRC\_FRAME\_FATAL\_REG (0x02A4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_MASK_ERR_FRAME_DATA_VC15<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC14<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC13<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC12<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC11<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC10<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC9<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC8<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC7<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC6<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC5<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC4<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC3<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC2<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC1<br>CSI_HOST_MASK_ERR_FRAME_DATA_VC0 |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | Reset |   |   |   |   |   |   |   |

CSI\_HOST\_MASK\_ERR\_FRAME\_DATA\_VC $n$  ( $n$ : 0-15) Configures whether to mask

[CSI\\_HOST\\_ST\\_ERR\\_FRAME\\_DATA\\_VC \$n\$](#) .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.29. CSI\_HOST\_INT\_FORCE\_CRC\_FRAME\_FATAL\_REG (0x02A8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_FORCE_ERR_FRAME_DATA_VC15<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC14<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC13<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC12<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC11<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC10<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC9<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC8<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC7<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC6<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC5<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC4<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC3<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC2<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC1<br>CSI_HOST_FORCE_ERR_FRAME_DATA_VC0 |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | Reset |   |   |   |   |   |   |   |

CSI\_HOST\_FORCE\_ERR\_FRAME\_DATA\_VC $n$  ( $n$ : 0-15) Configures whether to force set

[CSI\\_HOST\\_ST\\_ERR\\_FRAME\\_DATA\\_VC \$n\$](#)  to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.30. CSI\_HOST\_INT\_ST\_PLD\_CRC\_FATAL\_REG (0x02B0)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_ST_ERR_CRC_VC15<br>CSI_HOST_ST_ERR_CRC_VC14<br>CSI_HOST_ST_ERR_CRC_VC13<br>CSI_HOST_ST_ERR_CRC_VC12<br>CSI_HOST_ST_ERR_CRC_VC11<br>CSI_HOST_ST_ERR_CRC_VC10<br>CSI_HOST_ST_ERR_CRC_VC9<br>CSI_HOST_ST_ERR_CRC_VC8<br>CSI_HOST_ST_ERR_CRC_VC7<br>CSI_HOST_ST_ERR_CRC_VC6<br>CSI_HOST_ST_ERR_CRC_VC5<br>CSI_HOST_ST_ERR_CRC_VC4<br>CSI_HOST_ST_ERR_CRC_VC3<br>CSI_HOST_ST_ERR_CRC_VC2<br>CSI_HOST_ST_ERR_CRC_VC1<br>CSI_HOST_ST_ERR_CRC_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**CSI\_HOST\_ST\_ERR\_CRC\_VC $n$  ( $n$ : 0-15)** Represents whether the ERR\_CRC\_VC $n$  error occurs.

0: Do not occur

1: Occur

(RC)

Register 35.31. CSI\_HOST\_INT\_MSK\_PLD\_CRC\_FATAL\_REG (0x02B4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_MASK_ERR_CRC_VC15<br>CSI_HOST_MASK_ERR_CRC_VC14<br>CSI_HOST_MASK_ERR_CRC_VC13<br>CSI_HOST_MASK_ERR_CRC_VC12<br>CSI_HOST_MASK_ERR_CRC_VC11<br>CSI_HOST_MASK_ERR_CRC_VC10<br>CSI_HOST_MASK_ERR_CRC_VC9<br>CSI_HOST_MASK_ERR_CRC_VC8<br>CSI_HOST_MASK_ERR_CRC_VC7<br>CSI_HOST_MASK_ERR_CRC_VC6<br>CSI_HOST_MASK_ERR_CRC_VC5<br>CSI_HOST_MASK_ERR_CRC_VC4<br>CSI_HOST_MASK_ERR_CRC_VC3<br>CSI_HOST_MASK_ERR_CRC_VC2<br>CSI_HOST_MASK_ERR_CRC_VC1<br>CSI_HOST_MASK_ERR_CRC_VC0 |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**CSI\_HOST\_MASK\_ERR\_CRC\_VC $n$  ( $n$ : 0-15)** Configures whether to mask

[CSI\\_HOST\\_ST\\_ERR\\_CRC\\_VC \$n\$](#) .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.32. CSI\_HOST\_INT\_FORCE\_PLD\_CRC\_FATAL\_REG (0x02B8)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_FORCE_ERR_CRC_VC15<br>CSI_HOST_FORCE_ERR_CRC_VC14<br>CSI_HOST_FORCE_ERR_CRC_VC13<br>CSI_HOST_FORCE_ERR_CRC_VC12<br>CSI_HOST_FORCE_ERR_CRC_VC11<br>CSI_HOST_FORCE_ERR_CRC_VC10<br>CSI_HOST_FORCE_ERR_CRC_VC9<br>CSI_HOST_FORCE_ERR_CRC_VC8<br>CSI_HOST_FORCE_ERR_CRC_VC7<br>CSI_HOST_FORCE_ERR_CRC_VC6<br>CSI_HOST_FORCE_ERR_CRC_VC5<br>CSI_HOST_FORCE_ERR_CRC_VC4<br>CSI_HOST_FORCE_ERR_CRC_VC3<br>CSI_HOST_FORCE_ERR_CRC_VC2<br>CSI_HOST_FORCE_ERR_CRC_VC1<br>CSI_HOST_FORCE_ERR_CRC_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**CSI\_HOST\_FORCE\_ERR\_CRC\_VC $n$  ( $n$ : 0-15)** Configures whether to force set **CSI\_HOST\_ST\_ERR\_CRC\_VC $n$**  to 1.

0: Do not force set  
 1: Force set  
 (R/W)

Register 35.33. CSI\_HOST\_INT\_ST\_DATA\_ID\_REG (0x02C0)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_ST_ERR_ID_VC15<br>CSI_HOST_ST_ERR_ID_VC14<br>CSI_HOST_ST_ERR_ID_VC13<br>CSI_HOST_ST_ERR_ID_VC12<br>CSI_HOST_ST_ERR_ID_VC11<br>CSI_HOST_ST_ERR_ID_VC10<br>CSI_HOST_ST_ERR_ID_VC9<br>CSI_HOST_ST_ERR_ID_VC8<br>CSI_HOST_ST_ERR_ID_VC7<br>CSI_HOST_ST_ERR_ID_VC6<br>CSI_HOST_ST_ERR_ID_VC5<br>CSI_HOST_ST_ERR_ID_VC4<br>CSI_HOST_ST_ERR_ID_VC3<br>CSI_HOST_ST_ERR_ID_VC2<br>CSI_HOST_ST_ERR_ID_VC1<br>CSI_HOST_ST_ERR_ID_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**CSI\_HOST\_ST\_ERR\_ID\_VC $n$  ( $n$ : 0-15)** Represents whether the ERR\_ID\_VC $n$  error occurs.

0: Do not occur  
 1: Occur  
 (RC)

Register 35.34. CSI\_HOST\_INT\_MSK\_DATA\_ID\_REG (0x02C4)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_MASK_ERR_ID_VC15<br>CSI_HOST_MASK_ERR_ID_VC14<br>CSI_HOST_MASK_ERR_ID_VC13<br>CSI_HOST_MASK_ERR_ID_VC12<br>CSI_HOST_MASK_ERR_ID_VC11<br>CSI_HOST_MASK_ERR_ID_VC10<br>CSI_HOST_MASK_ERR_ID_VC9<br>CSI_HOST_MASK_ERR_ID_VC8<br>CSI_HOST_MASK_ERR_ID_VC7<br>CSI_HOST_MASK_ERR_ID_VC6<br>CSI_HOST_MASK_ERR_ID_VC5<br>CSI_HOST_MASK_ERR_ID_VC4<br>CSI_HOST_MASK_ERR_ID_VC3<br>CSI_HOST_MASK_ERR_ID_VC2<br>CSI_HOST_MASK_ERR_ID_VC1<br>CSI_HOST_MASK_ERR_ID_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**CSI\_HOST\_MASK\_ERR\_ID\_VC $n$  ( $n$ : 0-15)** Configures whether to mask **CSI\_HOST\_ST\_ERR\_ID\_VC $n$** .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)

Register 35.35. CSI\_HOST\_INT\_FORCE\_DATA\_ID\_REG (0x02C8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_FORCE_ERR_ID_VC15<br>CSI_HOST_FORCE_ERR_ID_VC14<br>CSI_HOST_FORCE_ERR_ID_VC13<br>CSI_HOST_FORCE_ERR_ID_VC12<br>CSI_HOST_FORCE_ERR_ID_VC11<br>CSI_HOST_FORCE_ERR_ID_VC10<br>CSI_HOST_FORCE_ERR_ID_VC9<br>CSI_HOST_FORCE_ERR_ID_VC8<br>CSI_HOST_FORCE_ERR_ID_VC7<br>CSI_HOST_FORCE_ERR_ID_VC6<br>CSI_HOST_FORCE_ERR_ID_VC5<br>CSI_HOST_FORCE_ERR_ID_VC4<br>CSI_HOST_FORCE_ERR_ID_VC3<br>CSI_HOST_FORCE_ERR_ID_VC2<br>CSI_HOST_FORCE_ERR_ID_VC1<br>CSI_HOST_FORCE_ERR_ID_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |  |

**CSI\_HOST\_FORCE\_ERR\_ID\_VC $n$  ( $n$ : 0-15)** Configures whether to force set **CSI\_HOST\_ST\_ERR\_ID\_VC $n$**  to 1.

0: Do not force set

1: Force set

(R/W)

## Register 35.36. CSI\_HOST\_INT\_ST\_ECC\_CORRECTED\_REG (0x02D0)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_ST_ERR_ECC_CORRECTED_VC15<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC14<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC13<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC12<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC11<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC10<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC9<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC8<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC7<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC6<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC5<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC4<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC3<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC2<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC1<br>CSI_HOST_ST_ERR_ECC_CORRECTED_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

CSI\_HOST\_ST\_ERR\_ECC\_CORRECTED\_VC $n$  ( $n$ : 0-15) Represents whether the  
 ERR\_ECC\_CORRECTED\_VC $n$  error occurs.

0: Do not occur

1: Occur

(RC)

## Register 35.37. CSI\_HOST\_INT\_MSK\_ECC\_CORRECTED\_REG (0x02D4)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_MASK_ERR_ECC_CORRECTED_VC15<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC14<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC13<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC12<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC11<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC10<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC9<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC8<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC7<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC6<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC5<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC4<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC3<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC2<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC1<br>CSI_HOST_MASK_ERR_ECC_CORRECTED_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |

CSI\_HOST\_MASK\_ERR\_ECC\_CORRECTED\_VC $n$  ( $n$ : 0-15) Configures whether to mask  
 CSI\_HOST\_ST\_ERR\_ECC\_CORRECTED\_VC $n$ .

0: Mask the error interrupt

1: Enable the error interrupt

(R/W)



Register 35.38. CSI\_HOST\_INT\_FORCE\_ECC\_CORRECTED\_REG (0x02D8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC15<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC14<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC13<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC12<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC11<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC10<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC9<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC8<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC7<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC6<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC5<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC4<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC3<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC2<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC1<br>CSI_HOST_FORCE_ERR_ECC_CORRECTED_VC0 |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

**CSI\_HOST\_FORCE\_ERR\_ECC\_CORRECTED\_VC $n$  ( $n$ : 0-15)** Configures whether to force set **CSI\_HOST\_ST\_ERR\_ECC\_CORRECTED\_VC $n$**  to 1.

0: Do not force set

1: Force set

(R/W)

Register 35.39. CSI\_HOST\_PHY\_STOPSTATE\_REG (0x004C)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |    |    |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |   |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |   |   |       |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|----|----|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|---|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|---|---|-------|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | CSI_HOST_PHY_STOPSTATECLK |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |    |    |  |  |  |  |  |  |  |  |  |  | CSI_HOST_PHY_STOPSTATEDATA_1 |  |  |  |  |   |  |  |  |  |  |  |  |  | CSI_HOST_PHY_STOPSTATEDATA_0 |  |  |  |  |  |  |   |   |       |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                        |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  | 16 | 15 |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  | 2 |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  | 1 | 0 |       |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                         |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  | 0  | 0  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  | 0 |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  | 0 | 0 | Reset |  |  |  |  |

**CSI\_HOST\_PHY\_STOPSTATEDATA\_ $n$  ( $n$ : 0-1)** Represents whether data lane  $n$  is in stop state.

0: Not in stop state

1: In stop state

(RO)

**CSI\_HOST\_PHY\_STOPSTATECLK** Represents whether clock lane in stop state.

0: Not in stop state

1: In stop state

(RO)

## Chapter 36

# Voice Activity Detection (VAD)

## 36.1 Introduction

ESP32-P4 integrates a Voice Activity Detection (VAD) module. This module facilitates the hardware implementation of the first-stage algorithm for voice wake-up and other multimedia functions. Additionally, it provides hardware support for low-power voice wake-up solutions.

## 36.2 Feature List

The VAD module has the following features:

- VAD algorithm processes voice data frame by frame, with each frame containing 256 data points. The data sampling rate is 8 kHz, and the bit width is 16 bits
- 2 KB buffer that stores up to 4 frames of data
- Independent system wake-up source
- Configurable interrupt sources
- Flexible configuration of algorithm parameters

## 36.3 Architectural Overview

Figure [36.3-1](#) is the block diagram of the ESP32-P4 VAD module. The VAD module includes:

- Energy threshold check
- FFT (Fast Fourier Transform) calculation
- LTSD (Long-Term Spectral Divergence) calculation

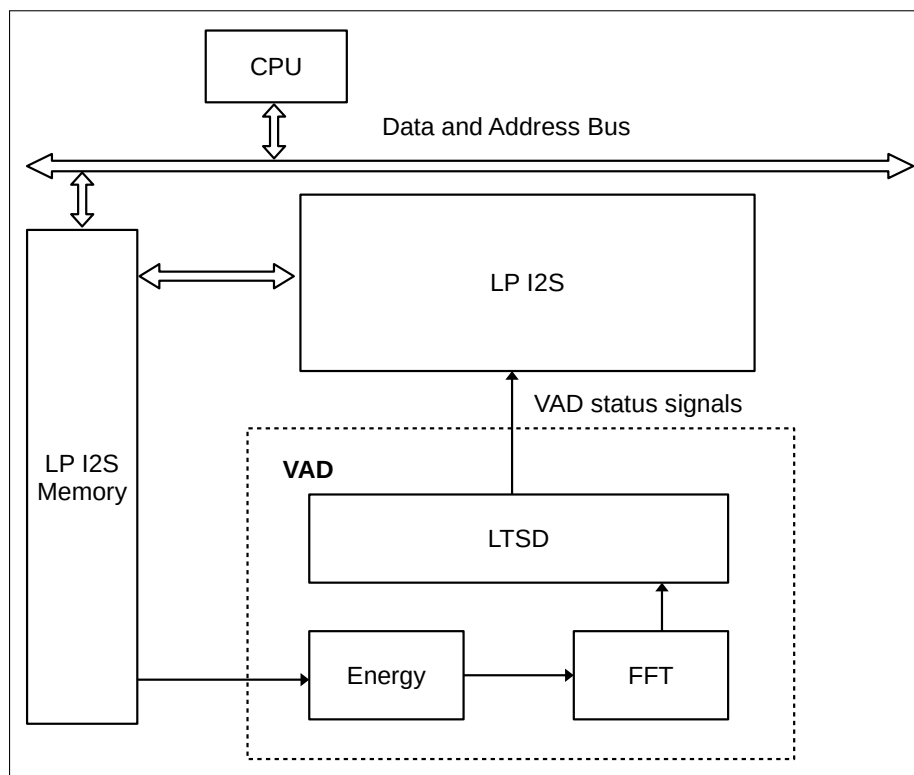


Figure 36.3-1. ESP32-P4 VAD Architecture

The VAD module reads 8 kHz, 16-bit wide audio data from LP I2S memory. It processes the data through three stages: energy detection, FFT, and LTSD. Then the module detects the voice activity status and sends the VAD status signal to the LP I2S module, which is used to generate the corresponding interrupt and wake-up signal.

## 36.4 Functional Description

The ESP32-P4's VAD module offers flexible and configurable functionality. Users can adjust algorithm parameters and wake-up sources to meet their specific needs.

### 36.4.1 Algorithm Parameter Configuration

#### Number of Initial Frames

When the VAD module starts running, it first enters an initialization phase before normal operation. During this phase, it automatically learns noise parameters. The duration of the initialization phase depends on the number of initial frames configured by the user. Proper setting of initial frames can effectively suppress noise and significantly reduce false positives. However, if the initialization phase is extended over too many frames, voice activity within these frames may be missed. Therefore, please configure an appropriate number of initial frames based on actual conditions.

It is recommended to place the device in the target environment noise during the initialization, and set the number of initial frames to 100-200 frames.

Users can configure the number of initial frames via [LP\\_I2S\\_PARAM\\_INIT\\_FRAME\\_NUM](#).

**Note:**

It is recommended to let the VAD module learn noise parameters during the initialization. However, the VAD module will also continuously learn and update noise parameters during normal operation. Therefore, in scenarios where the false positive rate during initial frames is not a concern, the number of initial frames can be reduced, allowing the VAD module to enter the normal operation more quickly.

**Energy Threshold**

The VAD module sets an energy threshold before the voice activity detection. Setting the threshold can filter out low-energy voice activities (e.g., distant voices) from triggering a wake-up. Appropriate energy threshold setting can effectively reduce false positives and conserve power.

It defines the energy value of a speech frame as the mean square of one-frame data. The VAD module calculates the sum of squares of one-frame data in real-time. If this sum is less than the energy threshold multiplied by 256, subsequent calculations will not be performed. Users can configure the energy threshold via [LP\\_I2S\\_PARAM\\_MIN\\_ENERGY](#).

**Band Energy Check**

The band energy check assesses the proportion of band energy within the overall frequency spectrum. Enabling the band energy check in varying environments can help reduce false positives; however, it may also reduce true positives. Users should determine whether to enable or disable the band energy check based on the environment.

Users can enable or disable the band energy check via [LP\\_I2S\\_PARAM\\_SKIP\\_BAND\\_ENERGY](#).

- 0: Enable band energy check
- 1: Disable band energy check

**Voice Activity Detection**

The VAD module has two voice activity status: voice activity status and non-voice activity status, managed by voice frame counter `speech_count` and non-voice frame counter `silent_count`. These counters control transitions between the status as follows:

- **Non-voice activity status:**
  - When voice activities are detected in the current frame, the count value of `speech_count` increases by 1.
  - When voice activities are not detected in the current frame, the count value of `speech_count` decreases by 1 (down to a minimum of 0).
  - If the count value of `speech_count` is greater than [LP\\_I2S\\_PARAM\\_HANGOVER\\_SPEECH](#), the VAD module enters the voice activity status and resets `silent_count` to 0.
  - Under the non-voice activity status, the VAD module continuously learns and updates noise information.
- **Voice activity status:**
  - When voice activities are detected in the current frame, the count value of `speech_count` increases by 1, and the count value of `silent_count` decreases by 1 (down to a minimum of 0).

- When voice activities are not detected in the current frame, the count value of `silent_count` increases by 1:
  - \* If the count value of `speech_count` is greater than `LP_I2S_PARAM_MIN_SPEECH_COUNT`, and
    - The count value of `silent_count` is greater than `LP_I2S_PARAM_HANGOVER_SILENT`, the VAD module transitions to the non-voice activity status and resets both `speech_count` and `silent_count` to 0;
    - The count value of `silent_count` is less than `LP_I2S_PARAM_HANGOVER_SILENT`, the VAD module maintains the voice activity status.
  - \* If the count value of `speech_count` is less than or equal to `LP_I2S_PARAM_MIN_SPEECH_COUNT`, the VAD module transitions directly to the non-voice activity status and resets `speech_count` to 0.
- Under the voice activity status, the VAD module pauses updating noise information. When the count value of `speech_count` exceeds `LP_I2S_PARAM_MAX_SPEECH_COUNT`, indicating stability in the new environment, it resumes learning and updating noise information.

### Status Registers

The VAD module provides several key operational variables as status registers (read-only) to facilitate user debugging. The status registers include:

- `LP_I2S_VAD_FLAG`: Represents the current voice activity detection status. 1 represents the VAD module is in the voice activity status, while 0 represents it is in the non-voice activity status.
- `LP_I2S_ENERGY_ENOUGH`: Represents whether the current frame passes the energy threshold check. 1 represents the current frame passes the energy threshold check, while 0 represents not pass.
- `LP_I2S_SPEECH_COUNT_OB`: Represents the count value of the voice frame counter, `speech_count`.
- `LP_I2S_SILENT_COUNT_OB`: Represents the count value of the non-voice frame counter, `silent_count`.

## 36.4.2 Wake-up Source Configuration

When the VAD module is in the voice activity status, it triggers the wake-up source `LP_I2S_WAKEUP`. Users can configure the wake-up source (please refer to Chapter [42 LP I2S Controller](#)), enabling the VAD to become one of the wake-up sources for ESP32-P4.

## 36.5 Interrupts

ESP32-P4's VAD module shares the same interrupt signal `LP_I2S_INTR` with the LP I2S module. The following interrupt sources can generate the interrupt signal:

- `LP_I2S_VAD_DONE_INT`: Triggered when the VAD completes processing one frame of data.
- `LP_I2S_VAD_RESET_DONE_INT`: Triggered when the VAD is reset.

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [36.7 Register Summary](#).

## 36.6 Programming Procedure

### 36.6.1 Automatic Operation Mode

1. Configure the VAD parameters as described in Section [36.4.1](#).
2. Enable the VAD automatic detection mode by writing 1 to [LP\\_I2S\\_VAD\\_EN](#).
3. Configure the LP I2S to operate in 16-bit receive mode and start receiving data in 16-bit format. The received data will be stored in the LP I2S memory.
4. The VAD module will automatically perform operations on each frame of data after the LP I2S receives the complete frame.
5. (Optional) When the VAD module triggers a wake-up source/interrupt signal, the LP I2S memory already contains the voice frame that triggered the VAD wake-up, along with the previous three voice frames. Users can read these four frames of voice data from the LP I2S memory via the LP core for subsequent processing. For details on the size of the LP I2S memory and data reading methods, please refer to Chapter [42 LP I2S Controller](#) > Section [42.8.3 Internal Memory](#).

### 36.6.2 Manual Operation Mode

1. Configure the VAD parameters as described in Section [36.4.1](#).
2. Manually store the voice data in the LP I2S memory. For details, refer to Chapter [42 LP I2S Controller](#) > Section [42.8.3 Internal Memory](#).
3. With all the voice data stored in the memory, write 1 to [LP\\_I2S\\_VAD\\_FORCE\\_START](#), then the VAD will perform operations on one frame of data.
4. When the VAD module completes processing one frame of data, [LP\\_I2S\\_VAD\\_DONE\\_INT](#) interrupt will be generated.

## 36.7 Register Summary

The addresses in this section are relative to VAD base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                  | Description                                   | Address | Access |
|---------------------------------------|---|---------|--------|
| <b>VAD Registers</b>                  |   |         |        |
| <a href="#">LP_I2S_VAD_CONF_REG</a>   | Operation control register                    | 0x0000  | varies |
| <a href="#">LP_I2S_VAD_RESULT_REG</a> | Voice activity status register                | 0x0004  | RO     |
| <a href="#">LP_I2S_VAD_PARAM0_REG</a> | Parameter configuration register 0            | 0x0080  | R/W    |
| <a href="#">LP_I2S_VAD_PARAM1_REG</a> | Parameter configuration register 1            | 0x0084  | R/W    |
| <a href="#">LP_I2S_VAD_OBO_REG</a>    | Status register for key operational variables | 0x00B0  | RO     |

## 36.8 Registers

The addresses in this section are relative to VAD base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 36.1. LP\_I2S\_VAD\_CONF\_REG (0x0000)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_I2S_VAD_FORCE_START<br>LP_I2S_VAD_RESET<br>LP_I2S_VAD_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3 | 2   | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**LP\_I2S\_VAD\_EN** Configures whether to enable the automatic operation mode.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_VAD\_RESET** Configures whether to reset the VAD module.

0: Not reset

1: Reset

(WT)

**LP\_I2S\_VAD\_FORCE\_START** Configures whether to trigger the manual operation on one frame of data.

0: Not trigger

1: Trigger

(WT)

**Register 36.2. LP\_I2S\_VAD\_RESULT\_REG (0x0004)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_I2S_ENERGY_ENOUGH<br>LP_I2S_VAD_FLAG |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2                                       | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LP\_I2S\_VAD\_FLAG** Represents the voice activity status. For details, see Section 36.4.1. (RO)

**LP\_I2S\_ENERGY\_ENOUGH** Represents whether the current frame passes the energy threshold check. For details, see Section 36.4.1. (RO)



**Register 36.3. LP\_I2S\_VAD\_PARAM0\_REG (0x0080)**

|            |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |       |  |
|------------|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|-------|--|
| (reserved) |  |  |  |  |  |  |  | LP_I2S_PARAM_INIT_FRAME_NUM |  |  |  |  |  |  |  | LP_I2S_PARAM_MIN_ENERGY |  |  |  |  |  |  |  |       |  |
| 312524     |  |  |  |  |  |  |  | 1615                        |  |  |  |  |  |  |  | 0                       |  |  |  |  |  |  |  |       |  |
| 00000000   |  |  |  |  |  |  |  | 200                         |  |  |  |  |  |  |  | 5000                    |  |  |  |  |  |  |  | Reset |  |

**LP\_I2S\_PARAM\_MIN\_ENERGY** Configures the energy threshold. For details, see Section 36.4.1. (R/W)

**LP\_I2S\_PARAM\_INIT\_FRAME\_NUM** Configures the number of initial frames. For details, see Section 36.4.1. (R/W)

**Register 36.4. LP\_I2S\_VAD\_PARAM1\_REG (0x0084)**

|                               |  |    |  |     |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |    |  |    |  |  |  |   |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |    |  |    |  |                              |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |                               |  |    |  |    |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
|-------------------------------|--|----|--|-----|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|----|--|----|--|--|--|---|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|----|--|----|--|------------------------------|--|--|--|---|--|--|--|-------|--|--|--|--|--|--|--|-------------------------------|--|----|--|----|--|--|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|---|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|
| LP_I2S_PARAM_SKIP_BAND_ENERGY |  |    |  |     |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |    |  |    |  |  |  |   |  |  |  | LP_I2S_PARAM_HANGOVER_SILENT |  |  |  |  |  |  |  |  |  |  |  |    |  |    |  | LP_I2S_PARAM_HANGOVER_SPEECH |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  | LP_I2S_PARAM_MAX_SPEECH_COUNT |  |    |  |    |  |  |  |  |  |  |  |  |  |  |  | LP_I2S_PARAM_MIN_SPEECH_COUNT |  |  |  |  |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |
| 31                            |  | 30 |  |     |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  | 24 |  | 23 |  |  |  |   |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  | 16 |  | 15 |  |                              |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |                               |  | 11 |  | 10 |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  | 4 |  | 3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |
| 0                             |  |    |  | 0x0 |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |    |  | 30 |  |  |  | 3 |  |  |  | 100                          |  |  |  |  |  |  |  |  |  |  |  |    |  |    |  |                              |  |  |  | 3 |  |  |  | Reset |  |  |  |  |  |  |  |                               |  |    |  |    |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |   |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |

**LP\_I2S\_PARAM\_MIN\_SPEECH\_COUNT** Configures the transition between voice activity status. For details, see Section 36.4.1. (R/W)

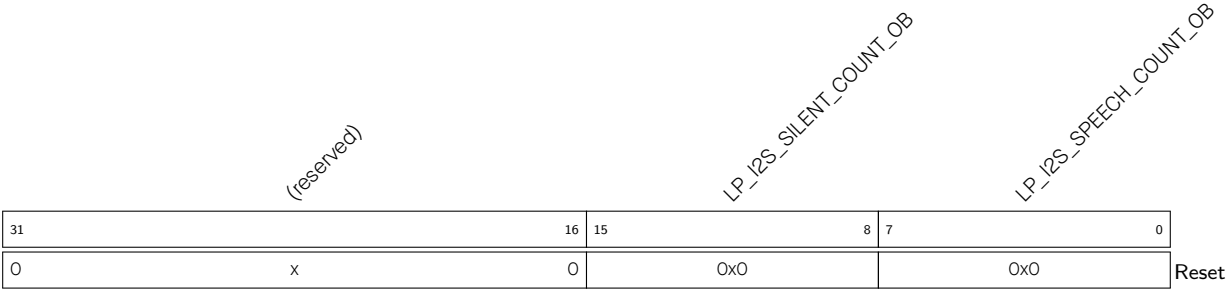
**LP\_I2S\_PARAM\_MAX\_SPEECH\_COUNT** Configures the transition between voice activity status. For details, see Section 36.4.1. (R/W)

**LP\_I2S\_PARAM\_HANGOVER\_SPEECH** Configures the transition between voice activity status. For details, see Section 36.4.1. (R/W)

**LP\_I2S\_PARAM\_HANGOVER\_SILENT** Configures the transition between voice activity status. For details, see Section 36.4.1. (R/W)

**LP\_I2S\_PARAM\_SKIP\_BAND\_ENERGY** Configures the transition between voice activity status. For details, see Section 36.4.1. (R/W)

Register 36.5. LP\_I2S\_VAD\_OB0\_REG (0x00B0)



**LP\_I2S\_SPEECH\_COUNT\_OB** Represents the count value of the voice frame counter, speech\_count. For details, see Section 36.4.1. (RO)

**LP\_I2S\_SILENT\_COUNT\_OB** Represents the count value of the non-voice frame counter, silent\_count. For details, see Section 36.4.1. (RO)

## Part VII

# Connectivity Interface

This part addresses the connectivity aspects of the system, describing components related to various communication interfaces like I2C, I2S, SPI, UART, USB, and more. The part also covers interfaces to generate signals used in remote control, motor control, LED control, etc.

## Chapter 37

### UART Controller (UART)

#### 37.1 Overview

A UART is a character-oriented data link for asynchronous communication between devices. Such communication does not add clock signals to the data sent. Therefore, in order to communicate successfully, the transmitter and the receiver must operate at the same baud rate with the same stop bit(s) and parity bit(s).

A UART data frame usually begins with one start bit, followed by data bits, one parity bit (optional), and one or more stop bits. UART controllers on ESP32-P4 support various lengths of data bits and stop bits. These controllers also support software and hardware flow control as well as GDMA for high-speed data transfer. This allows developers to use multiple UART ports at minimal software cost.

ESP32-P4 has six UART controllers, including five regular UARTs and one low-power (LP) UART. These UARTs are compatible with various UART devices, and support Infrared Data Association (IrDA) and RS485 communication. In this chapter, the five regular UART controllers are referred to as UART $n$ , in which  $n$  denotes 0, 1, 2, 3, or 4. LP UART is the cut-down version of the regular UART, with a separate group of registers. For differences between UART and LP UART, please refer to Table 37.2-1.

#### 37.2 Features

Table 37.2-1 lists the feature comparison between UART and LP UART:

Table 37.2-1. UART and LP UART Feature Comparison

| UART Feature  | LP UART Feature  |
|---|--|
| Programmable baud rate up to 5 MBaud  |  |
| 128 x 8 bit RAM respectively for the TX channel and RX channel of a UART controller | 20 x 8-bit RAM, shared by the TX FIFO and RX FIFO of LP UART |
| Full-duplex asynchronous communication  |  |
| Data bits (5 to 8 bits)   |  |
| Stop bits (1, 1.5, or 2 bits)   |  |
| Parity bit  |  |
| Special character AT_CMD detection  |  |
| RS485 protocol  | —  |
| IrDA protocol   | —  |

Cont'd on next page

Table 37.2-1 – cont'd from previous page

| UART Feature   | LP_UART Feature   |
|--|---|
| High-speed data communication using GDMA   | —   |
| Receive timeout  |   |
| UART as wakeup source  |   |
| Software and hardware flow control   |   |
| Three prescalable clock sources:<br>1. XTAL_CLK<br>2. RC_FAST_CLK<br>3. PLL_F80M_CLK | Three prescalable clock sources:<br>1. RC_FAST_CLK<br>2. XTAL_DIV_CLK<br>3. PLL_F8M_CLK |

The following description mainly covers regular UART controllers.

## 37.3 UART Structure

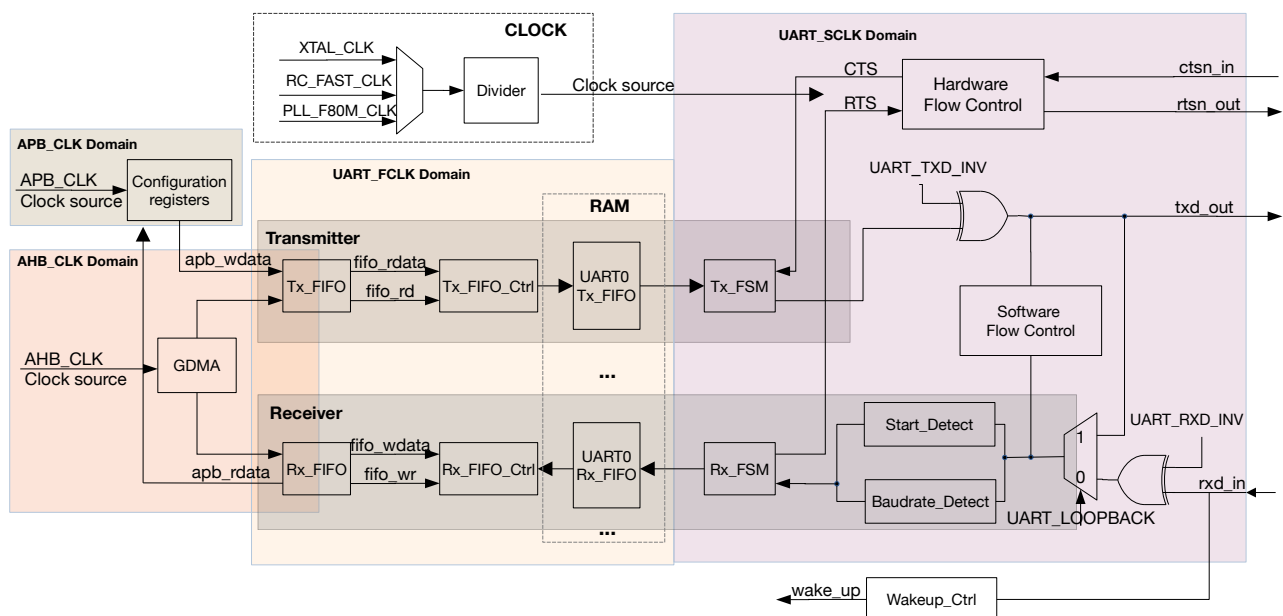


Figure 37.3-1. UART Structure

Figure 37.3-1 shows the basic structure of a UART controller. A UART controller works in four clock domains, namely APB\_CLK, AHB\_CLK, UART\_SCLK, and UART\_FCLK. APB\_CLK and AHB\_CLK are synchronized but with different frequencies (APB\_CLK is derived from AHB\_CLK by division), and likewise UART\_SCLK and UART\_FCLK are synchronized but with different frequencies (UART\_SCLK is derived from UART\_FCLK by division). UART\_FCLK has three clock sources: PLL\_F80M\_CLK, RC\_FAST\_CLK, and crystal clock XTAL\_CLK (for details, please refer to Chapter 9 *Reset and Clock*), which are selected by configuring HP\_SYS\_UART $n$ \_CLK\_SRC\_SEL. The selected clock source is divided by a divider to generate UART\_SCLK clock signals. The divisor is configured by HP\_SYS\_CLKRST\_UART $n$ \_SCLK\_DIV\_NUM for the integral part, HP\_SYS\_CLKRST\_UART $n$ \_SCLK\_DIV\_DENOMINATOR for the denominator of the fractional part, and HP\_SYS\_CLKRST\_UART $n$ \_SCLK\_DIV\_NUMERATOR for the numerator of the fractional part. The divisor ranges from 1 ~ 256. Only regular UART has such a divider; LP UART does not.

A UART controller can be broken down into two parts based on functions: a transmitter and a receiver.

The transmitter contains a TX FIFO (i.e., Tx\_FIFO in Figure 37.3-1), which buffers data to be sent. Software can write data to Tx\_FIFO via the APB bus, or move data to Tx\_FIFO using GDMA. Tx\_FIFO\_Ctrl controls writing and reading Tx\_FIFO. When Tx\_FIFO is not empty, Tx\_FSM reads data bits in the data frame via Tx\_FIFO\_Ctrl, and converts them into a bitstream. The levels of output bitstream signal txd\_out can be inverted by configuring the [UART\\_TXD\\_INV](#) field.

The receiver contains an RX FIFO (i.e., Rx\_FIFO in Figure 37.3-1), which buffers data to be processed. The input bitstream signal rxd\_in is transferred to the UART controller, and its level can be inverted by configuring [UART\\_RXD\\_INV](#) field. Baudrate\_Detect measures the baud rate of input bitstream signal rxd\_in by detecting its minimum pulse width. Start\_Detect detects the start bit in a data frame. If the start bit is detected, Rx\_FSM stores data bits in the data frame into Rx\_FIFO by Rx\_FIFO\_Ctrl. Software can read data from Rx\_FIFO via the APB bus, or receive data using GDMA.

HW\_Flow\_Ctrl controls rxd\_in and txd\_out data flows by standard UART RTS and CTS flow control signals (rtsn\_out and ctsn\_in). SW\_Flow\_Ctrl controls data flows by adding special characters to outgoing data and detecting special characters in incoming data. When a UART controller is in Light-sleep mode (see Chapter 13 [Low-Power Management](#) for more details), a wake\_up signal can be generated in four ways and sent to RTC, which then wakes up the ESP32-P4 chip. For more information about wakeup, please refer to Section 37.4.8.

## 37.4 Functional Description

### 37.4.1 Clock and Reset

UART controllers are asynchronous. Their register configuration module works in the APB\_CLK domain. TX FIFO and RX FIFO work across the AHB\_CLK and UART\_FCLK domains. The UART RAM control unit works in the UART\_FCLK domain. The UART transmission and reception control module works in the UART\_SCLK domain, i.e., UART Core's clock domain.

When the frequency of the UART\_SCLK is higher than the frequency needed to generate the baud rate, the UART Core can be clocked at a lower frequency by the divider, in order to reduce power consumption. Usually, the UART Core's clock frequency is lower than the APB\_CLK's frequency, and can be divided by the largest divisor when higher than the frequency needed to generate the baud rate. The frequency of the UART Core's clock can also be at most twice higher than the APB\_CLK. The clock for the UART transmitter and the UART receiver can be controlled independently. To enable the clock for the UART transmitter, [UART\\_TX\\_SCLK\\_EN](#) shall be set; to enable the clock for the UART receiver, [UART\\_RX\\_SCLK\\_EN](#) shall be set.

To ensure that the configured register values are synchronized from APB\_CLK domain to the UART\_SCLK domain, please follow the procedures in Section 37.5.

To reset the whole UART, please:

- Enable the UART Core's clock by setting [HP\\_SYS\\_CLKRST\\_UARTn\\_CLK\\_EN](#) to 1.
- Write 1 to [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_UARTn\\_CORE](#).
- Clear [HP\\_SYS\\_CLKRST\\_RST\\_EN\\_UARTn\\_CORE](#) to 0.

## 37.4.2 UART FIFO

The transmitter and the receiver on the UART controller each use a 128 x 8-bit RAM, and access their respective RAM through a separate 4 x 8-bit asynchronous FIFO interface. The RAM and asynchronous FIFO interface for the transmitter and the receiver are independent and cannot be shared.

UART Tx\_FIFO is reset by setting [UART\\_TXFIFO\\_RST](#). UART Rx\_FIFO is reset by setting [UART\\_RXFIFO\\_RST](#).

Data to be sent is written to TX FIFO via the APB bus or using GDMA, read automatically, and converted from a frame into a bitstream by hardware Tx\_FSM. Data received is converted from a bitstream into a frame by hardware Rx\_FSM, written into RX FIFO, and then stored into RAM via the APB bus or using GDMA. The five UART controllers share one GDMA channel.

The empty signal threshold for Tx\_FIFO is configured by setting [UART\\_TXFIFO\\_EMPTY\\_THRHD](#). When data stored in Tx\_FIFO is less than [UART\\_TXFIFO\\_EMPTY\\_THRHD](#), a UART\_TXFIFO\_EMPTY\_INT interrupt is generated. The full signal threshold for Rx\_FIFO is configured by setting [UART\\_RXFIFO\\_FULL\\_THRHD](#). When data stored in Rx\_FIFO is greater than or equal to [UART\\_RXFIFO\\_FULL\\_THRHD](#), a UART\_RXFIFO\_FULL\_INT interrupt is generated. In addition, when Rx\_FIFO receives more data than its capacity, a UART\_RXFIFO\_OVF\_INT interrupt is generated.

UART $n$  can access FIFO via register [UART\\_FIFO\\_REG](#). You can put data into TX FIFO by writing [UART\\_RXFIFO\\_RD\\_BYTE](#), and get data in RX FIFO by reading [UART\\_RXFIFO\\_RD\\_BYTE](#).

## 37.4.3 Baud Rate Generation and Detection

### 37.4.3.1 Baud Rate Generation

Before a UART controller sends or receives data, the baud rate should be configured by setting corresponding registers. The baud rate generator of a UART controller functions by dividing the input clock source. It can divide the clock source by a fractional amount. The divisor is configured by [UART\\_CLKDIV\\_SYNC\\_REG](#): [UART\\_CLKDIV](#) for the integral part, and [UART\\_CLKDIV\\_FRAG](#) for the fractional part. When using the 80 MHz input clock, the UART controller supports a maximum baud rate of 5 MBaud.

The divisor of the baud rate divider is equal to

$$UART\_CLKDIV + \frac{UART\_CLKDIV\_FRAG}{16}$$

meaning that the final baud rate is equal to

$$\frac{INPUT\_FREQ}{UART\_CLKDIV + \frac{UART\_CLKDIV\_FRAG}{16}}$$

where INPUT\_FREQ is the frequency of UART Core's source clock. For example, if [UART\\_CLKDIV](#) = 694 and [UART\\_CLKDIV\\_FRAG](#) = 7, then the divisor value is

$$694 + \frac{7}{16} = 694.4375$$

When [UART\\_CLKDIV\\_FRAG](#) is 0, the baud rate generator is an integer clock divider where an output pulse is generated every [UART\\_CLKDIV](#) input pulses.

When [UART\\_CLKDIV\\_FRAG](#) is not 0, the divider is fractional and the output baud rate clock pulses are not strictly uniform. As shown in Figure 37.4-1, for every 16 output pulses, the generator divides either

( $\text{UART\_CLKDIV} + 1$ ) input pulses or  $\text{UART\_CLKDIV}$  input pulses per output pulse. A total of  $\text{UART\_CLKDIV\_FRAG}$  output pulses are generated by dividing ( $\text{UART\_CLKDIV} + 1$ ) input pulses, and the remaining ( $16 - \text{UART\_CLKDIV\_FRAG}$ ) output pulses are generated by dividing  $\text{UART\_CLKDIV}$  input pulses.

The output pulses are interleaved as shown in Figure 37.4-1 below, to make the output timing more uniform:

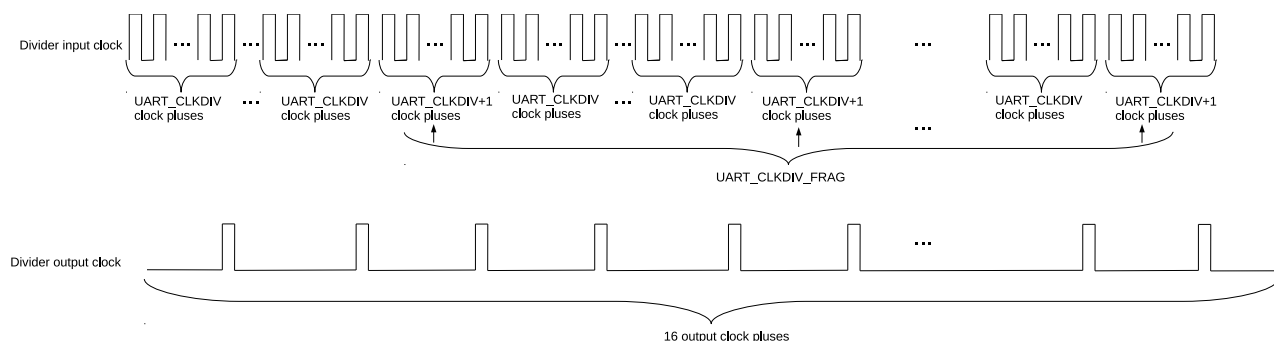


Figure 37.4-1. UART Controllers Division

To support IrDA (see Section 37.4.7 for details), the fractional clock divider for IrDA data transmission generates clock signals divided by  $16 \times \text{UART\_CLKDIV\_SYNC\_REG}$ . This divider works similarly as the one elaborated above: it takes  $\text{UART\_CLKDIV}/16$  as the integer value and the lowest four bits of  $\text{UART\_CLKDIV}$  as the fractional value.

### 37.4.3.2 Baud Rate Detection

Automatic baud rate detection (Autobaud) on UARTs is enabled by setting  $\text{UART\_AUTOBAUD\_EN}$ . The Baudrate\_Detect module shown in Figure 37.4-2 filters any noise whose pulse width is shorter than  $\text{UART\_GLITCH\_FLT}$ .

Before communication starts, the transmitter could send random data to the receiver for baud rate detection.  $\text{UART\_LOWPULSE\_MIN\_CNT}$  stores the minimum low pulse width,  $\text{UART\_HIGHPULSE\_MIN\_CNT}$  stores the minimum high pulse width,  $\text{UART\_POSEDGE\_MIN\_CNT}$  stores the minimum pulse width between two positive edges, and  $\text{UART\_NEGEDGE\_MIN\_CNT}$  stores the minimum pulse width between two negative edges. These four fields are read by software to determine the transmitter's baud rate.

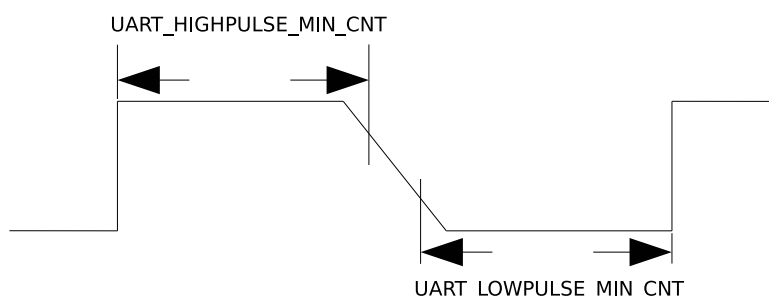


Figure 37.4-2. The Timing Diagram of Weak UART Signals Along Negative Edges

The baud rate can be determined in the following three ways:

1. Normally, to avoid sampling erroneous data along positive or negative edges in a metastable state, which results in the inaccuracy of  $\text{UART\_LOWPULSE\_MIN\_CNT}$  or  $\text{UART\_HIGHPULSE\_MIN\_CNT}$ , use a



weighted average of these two values to eliminate errors for 1-bit pulses. In this case, the baud rate is calculated as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_LOWPULSE\_MIN\_CNT} + \text{UART\_HIGHPULSE\_MIN\_CNT} + 2)/2}$$

2. If UART signals are weak along negative edges as shown in Figure 37.4-2, which leads to an inaccurate average of `UART_LOWPULSE_MIN_CNT` and `UART_HIGHPULSE_MIN_CNT`, use `UART_POSEDGE_MIN_CNT` to determine the transmitter's baud rate as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_POSEDGE\_MIN\_CNT} + 1)/2}$$

3. If UART signals are weak along positive edges, use `UART_NEGEDGE_MIN_CNT` to determine the transmitter's baud rate as follows:

$$B_{\text{uart}} = \frac{f_{\text{clk}}}{(\text{UART\_NEGEDGE\_MIN\_CNT} + 1)/2}$$

### 37.4.4 UART Data Frame

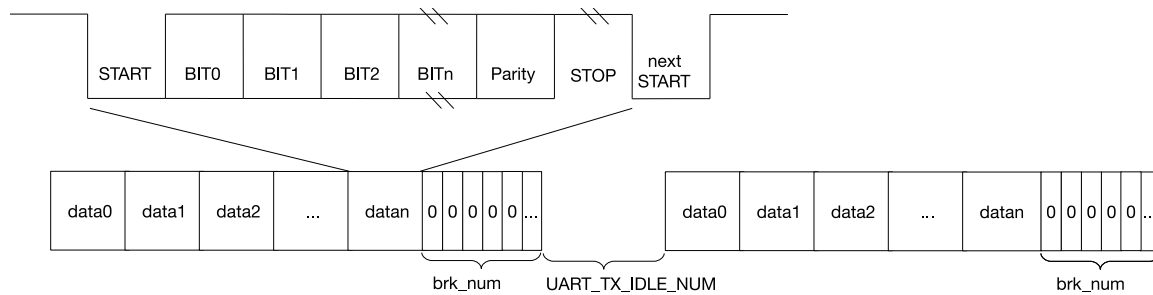


Figure 37.4-3. Structure of UART Data Frame

Figure 37.4-3 shows the basic structure of a data frame. A frame starts with one start bit, and ends with stop bits which can be 1, 1.5, or 2 bit-long, configured by `UART_STOP_BIT_NUM` (in RS485 mode turnaround delay may be added. See details in Section 37.4.6.2). The start bit is logical low, whereas stop bits are logical high.

The actual data length can be anywhere between 5 ~ 8 bit, configured by `UART_BIT_NUM`. When `UART_PARITY_EN` is set, a parity bit is added after data bits. `UART_PARITY` is used to choose even parity or odd parity. When the receiver detects a parity bit error in the data received, a `UART_PARITY_ERR_INT` interrupt is generated, and the data received will still be stored into RX FIFO. When the receiver detects a data frame error, a `UART_FRM_ERR_INT` interrupt is generated, and the data received by default is stored into RX FIFO.

If all data in `Tx_FIFO` has been sent, a `UART_TX_DONE_INT` interrupt is generated. After this, if the `UART_TXD_BRK` bit is set, then the transmitter will enter the break condition and send several NULL characters in which the TX data line is logical low. The number of NULL characters is configured by `UART_TX_BRK_NUM`. Once the transmitter has sent all NULL characters, a `UART_TX_BRK_DONE_INT` interrupt is generated. The minimum interval between data frames can be configured using `UART_TX_IDLE_NUM`. If the transmitter stays idle for `UART_TX_IDLE_NUM` or more time, a `UART_TX_BRK_IDLE_DONE_INT` interrupt is generated.

The receiver can also detect the Break conditions when the RX data line detects any low logical level for one NULL character transmission, and a `UART_BRK_DET_INT` interrupt will be triggered to detect when a break condition has been completed.

The receiver can detect the current bus state through the timeout interrupt `UART_RXFIFO_TOUT_INT`. The `UART_RXFIFO_TOUT_INT` interrupt will be triggered when the bus is in the idle state for more than `UART_RX_TOUT_THRHD` bit time on current baud rate after the receiver has received at least one byte. You can use this interrupt to detect whether all the data from the transmitter has been sent.

### 37.4.5 AT\_CMD Character Structure

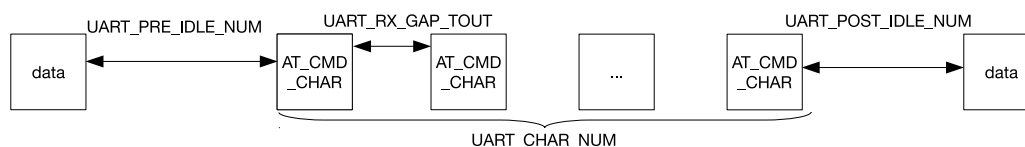


Figure 37.4-4. AT\_CMD Character Structure

Figure 37.4-4 is the structure of a special character `AT_CMD`. If the receiver constantly receives `AT_CMD_CHAR` and the following conditions are met, a `UART_AT_CMD_CHAR_DET_INT` interrupt is generated.

- The interval between the first `AT_CMD_CHAR` and the last non-`AT_CMD_CHAR` character is at least `UART_PRE_IDLE_NUM` cycles.
- The interval between two `AT_CMD_CHAR` characters is less than `UART_RX_GAP_TOUT` in the unit of baud rate cycles.
- The number of `AT_CMD_CHAR` characters is equal to or greater than `UART_CHAR_NUM`.
- The interval between the last `AT_CMD_CHAR` character and next non-`AT_CMD_CHAR` character is at least `UART_POST_IDLE_NUM` cycles.

Note: Given that the interval between `AT_CMD_CHAR` characters is less than `UART_RX_GAP_TOUT` in the unit of baud rate cycles, the `APB_CLK` frequency is suggested not to be lower than 8 MHz.

### 37.4.6 RS485

The five regular UART controllers support RS485 communication mode. In this mode differential signals are used to transmit data, so it can communicate over longer distances at higher bit rates than RS232. RS485 has two-wire half-duplex and four-wire full-duplex options. UART controllers support two-wire half-duplex transmission and bus snooping.

#### 37.4.6.1 Driver Control

As shown in Figure 37.4-5, in a two-wire multidrop network, an external RS485 transceiver is needed for differential to single-ended conversion or the other way around. An RS485 transceiver contains a driver and a receiver. When a UART controller is not in transmitter mode, the connection to the differential line can be broken by disabling the driver. When `DE` is 1, the driver is enabled; when `DE` is 0, the driver is disabled.

The UART receiver converts differential signals to single-ended signals via an external receiver. `RE` is the enable control signal for the receiver. When `RE` is 0, the receiver is enabled; when `RE` is 1, the receiver is disabled. If `RE` is configured as 0, the UART controller is allowed to snoop data on the bus, including the data sent by itself.

DE can be controlled by either software or hardware. To reduce the cost of software, in our design DE is controlled by hardware. As shown in Figure 37.4-5, DE is connected to dtrn\_out of UART (please refer to Section 37.4.9.1 for more details).

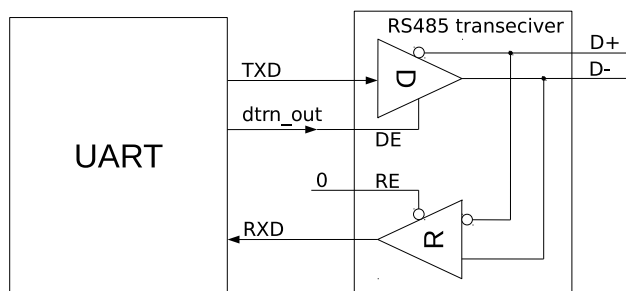


Figure 37.4-5. Driver Control Diagram in RS485 Mode

### 37.4.6.2 Turnaround Delay

By default, the UART controllers work in receiver mode. When a UART controller is switched from transmitter mode to receiver mode, the RS485 protocol requires a turnaround delay of one cycle after the stop bit. The UART transmitter supports adding a turnaround delay of one cycle before the start bit or after the stop bit. When `UART_DLO_EN` is set, a turnaround delay of one cycle is added before the start bit; when `UART_DL1_EN` is set, a turnaround delay of one cycle is added after the stop bit.

### 37.4.6.3 Bus Snooping

In a two-wire multidrop network, UART controllers support bus snooping if RE of the external RS485 transceiver is 0. By default, a UART controller is not allowed to transmit and receive data simultaneously. If `UART_RS485TX_RX_EN` is set and the external RS485 transceiver is configured as in Figure 37.4-5, a UART controller may receive data in transmitter mode and snoop the bus. If `UART_RS485RXBY_TX_EN` is set, a UART controller may transmit data in receiver mode.

The two UART controllers can snoop the data sent by themselves. In transmitter mode, when a UART controller monitors a collision between the data sent and the data received, a `UART_RS485_CLASH_INT` is generated; when a UART controller monitors a data frame error, a `UART_RS485_FRM_ERR_INT` interrupt is generated; when a UART controller monitors a parity bit error, a `UART_RS485_PARITY_ERR_INT` is generated.

## 37.4.7 IrDA

IrDA protocol consists of three layers, namely the physical layer, the link access protocol, and the link management protocol. The UART controllers implement IrDA's physical layer. In IrDA encoding, a UART controller supports data rates up to 115.2 kbit/s (SIR, or serial infrared mode). As shown in Figure 37.4-6, the IrDA encoder converts a non-return to zero code (NRZ) signal to a return to zero inverted code (RZI) signal and sends it to the external driver and infrared LED. This encoder uses modulated signals whose pulse width is 3/16 bits to indicate logic "0", and low levels to indicate logic "1". The IrDA decoder receives signals from the infrared receiver and converts them to NRZ signals. In most cases, the receiver is high when it is idle, and the parity bit of the encoder output is opposite to that of the decoder input. If a low pulse is detected, it indicates that a start bit has been received.

When IrDA function is enabled, one bit is divided into 16 clock cycles. If the bit to be sent is zero, then the 9th, 10th, and 11th clock cycle are high.

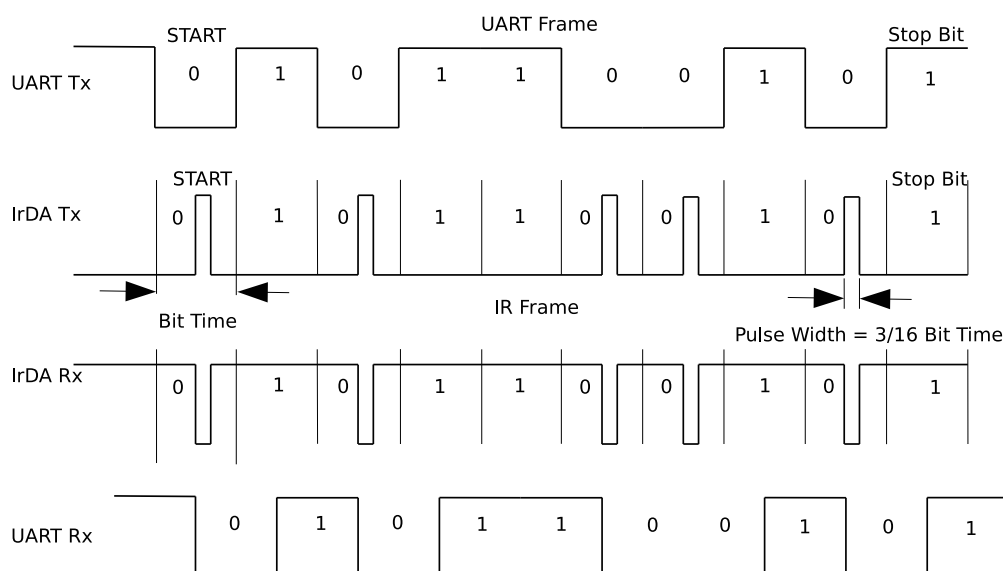


Figure 37.4-6. The Timing Diagram of Encoding and Decoding in SIR mode

The IrDA transceiver is half-duplex, meaning that it cannot send and receive data simultaneously. As shown in Figure 37.4-7, IrDA function is enabled by setting `UART_IRDA_EN`. When `UART_IRDA_TX_EN` is set to 1, the IrDA transceiver is enabled to send data and not allowed to receive data; when `UART_IRDA_TX_EN` is reset to 0, the IrDA transceiver is enabled to receive data and not allowed to send data.

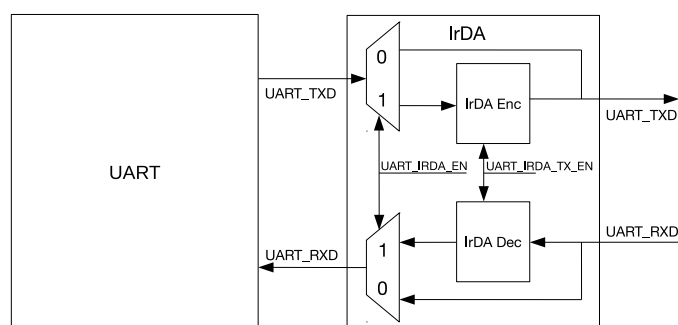


Figure 37.4-7. IrDA Encoding and Decoding Diagram

### 37.4.8 Wakeup

UART can be set as wakeup source. When a UART controller is in Light-sleep mode, a wake\_up signal can be generated in four ways and be sent to the RTC module, which then wakes up ESP32-P4.

- `UART_WK_MODE_SEL` = 0: When all the clocks are disabled, the chip can be woken up by reverting RXD for multiple cycles until the number of positive edges is greater than or equal to `UART_ACTIVE_THRESHOLD` + 3.
- `UART_WK_MODE_SEL` = 1: UART Core keeps working, so the UART receiver can still receive data and store the received data in RX FIFO. When the number of data bytes in RX FIFO is greater than `UART_RX_WAKE_UP_THRHD`, the chip can be woken up from the Light-sleep mode.
- `UART_WK_MODE_SEL` = 2: When the UART receiver detects a start bit, the chip will be woken up.

- **UART\_WK\_MODE\_SEL** = 3: When the UART receiver receives a specific character sequence, the chip will be woken up. The wakeup characters can be defined by configuring **UART\_WK\_CHAR0**, **UART\_WK\_CHAR1**, **UART\_WK\_CHAR2**, **UART\_WK\_CHAR3**, and **UART\_WK\_CHAR4**. These characters can be formed into different character sequences by configuring **UART\_CHAR\_NUM** and **UART\_WK\_CHAR\_MASK**, as shown in Table 37.4-1. Once the sequence is detected, the chip will be woken up. For the last configuration in Table 37.4-1, UART will detect for CHAR0 ~ CHAR4 in order.

Table 37.4-1. UART\_CHAR\_WAKEUP Mode Configuration

| UART_CHAR_NAME | UART_WP_CHAR_MASK | Character Sequence            |
|----------------|-------------------|-------------------------------|
| 1              | 0xF               | CHAR4                         |
| 2              | 0x7               | CHAR3/CHAR4                   |
| 3              | 0x3               | CHAR2/CHAR3/CHAR4             |
| 4              | 0x1               | CHAR1/CHAR2/CHAR3/CHAR4       |
| 5              | 0x0               | CHAR0/CHAR1/CHAR2/CHAR3/CHAR4 |

After the chip is woken up by UART, it is necessary to clear the wake\_up signal by transmitting data to UART in Active mode or resetting the whole UART, otherwise the number of rising edges required for the next wakeup will be reduced.

### 37.4.9 Flow Control

UART controllers have two ways to control data flow, namely hardware flow control and software flow control. Hardware flow control is achieved using output signal rtsn\_out and input signal ctsn\_in. Software flow control is achieved by inserting special characters in the data flow sent and detecting special characters in the data flow received.

### 37.4.9.1 Hardware Flow Control

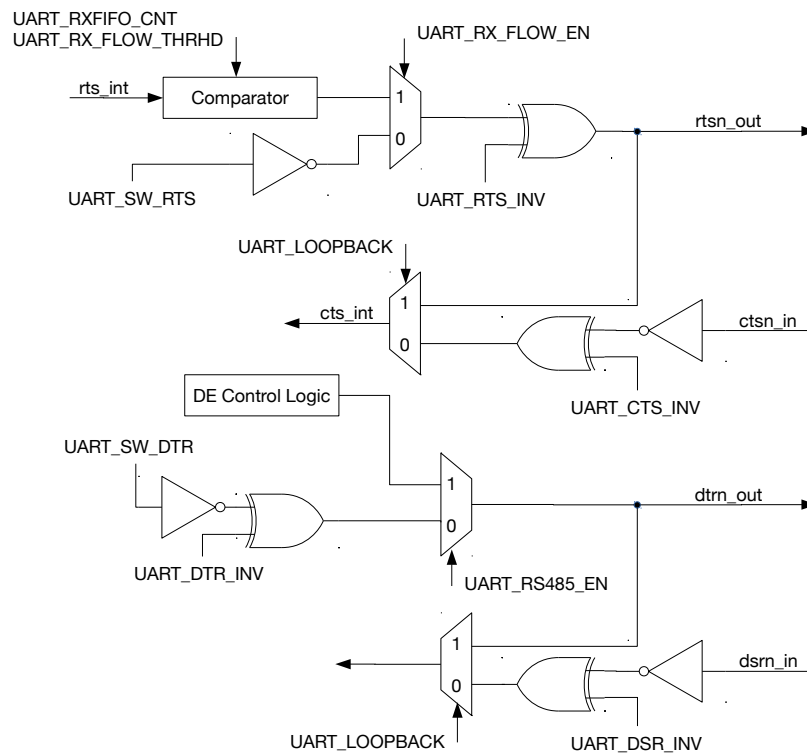


Figure 37.4-8. Hardware Flow Control Diagram

Figure 37.4-8 shows the hardware flow control of a UART controller. Hardware flow control uses output signal `rtsn_out` and input signal `dsrn_in`. Figure 37.4-9 illustrates how these signals are connected between UART on ESP32-P4 (hereinafter referred to as IUO) and the external UART (hereinafter referred to as EUO).

When `rtsn_out` of IUO is low, EUO is allowed to send data. When `rtsn_out` of IUO is high, EUO is notified to stop sending data until `rtsn_out` of IUO returns to low. The output signal `rtsn_out` can be controlled in two ways.

- Software control: Enter this mode by clearing `UART_RX_FLOW_EN` to 0. In this mode, the level of `rtsn_out` is changed by configuring `UART_SW_RTS`.
- Hardware control: Enter this mode by setting `UART_RX_FLOW_EN` to 1. In this mode, `rtsn_out` is pulled high when data in Rx\_FIFO exceeds `UART_RX_FLOW_THRHD`.

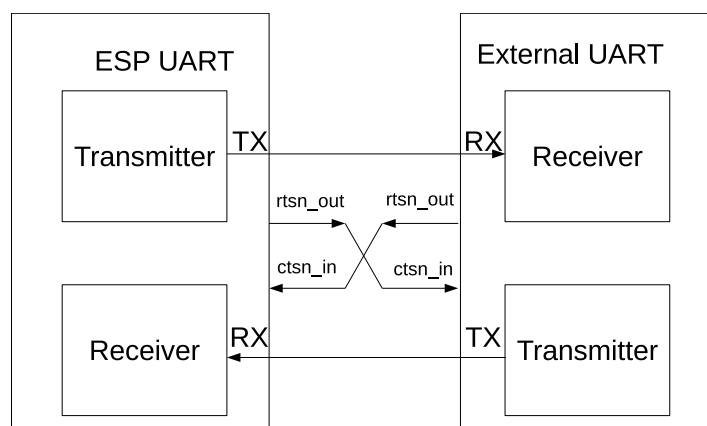


Figure 37.4-9. Connection between Hardware Flow Control Signals

When `ctsn_in` of IUO is low, IUO is allowed to send data; when `ctsn_in` is high, IUO is not allowed to send data. When IUO detects an edge change of `ctsn_in`, a `UART_CTS_CHG_INT` interrupt is generated.

If `dtrn_out` of IUO is high, it indicates that IUO is ready to transmit data. `dtrn_out` is generated by configuring the `UART_SW_DTR` field. When the IUO transmitter detects an edge change of `dtrn_in`, a `UART_DSR_CHG_INT` interrupt is generated. After this interrupt is detected, software can obtain the level of input signal `dtrn_in` by reading `UART_DSRN`. If `dtrn_in` is high, it indicates that EUO is ready to transmit data.

In a two-wire RS485 multidrop network enabled by setting `UART_RS485_EN`, `dtrn_out` is generated by hardware and used for transmit/receive turnaround. When data transmission starts, `dtrn_out` is pulled high and the external driver is enabled; when data transmission completes, `dtrn_out` is pulled low and the external driver is disabled. Please note that when there is a turnaround delay of one cycle added after the stop bit, `dtrn_out` is pulled low after the delay.

UART loopback test is enabled by setting `UART_LOOPBACK`. In the test, UART output signal `txd_out` is connected to its input signal `rx_d_in`, `rtsn_out` is connected to `ctsn_in`, and `dtrn_out` is connected to `dtrn_in`. If the data sent matches the data received, it indicates that UART controllers are working properly.

### 37.4.9.2 Software Flow Control

Instead of CTS/RTS lines, software flow control uses XON/XOFF characters to start or stop data transmission. Such flow control is enabled by setting `UART_SW_FLOW_CON_EN` to 1.

When using software flow control, hardware automatically detects if there are XON/XOFF characters in the data flow received, and generate a `UART_SW_XOFF_INT` or a `UART_SW_XON_INT` interrupt accordingly. If an XOFF character is detected, the transmitter stops data transmission once the current byte has been transmitted; if an XON character is detected, the transmitter starts data transmission. In addition, software can force the transmitter to stop sending data by setting `UART_FORCE_XOFF`, or to start sending data by setting `UART_FORCE_XON`.

Software determines whether to insert flow control characters based on the remaining room in RX FIFO. When `UART_SEND_XOFF` is set, the transmitter sends an XOFF character configured by `UART_XOFF_CHAR` after the current byte in transmission; when `UART_SEND_XON` is set, the transmitter sends an XON character configured by `UART_XON_CHAR` after the current byte in transmission. If the RX FIFO of a UART controller stores more data than `UART_XOFF_THRESHOLD`, `UART_SEND_XOFF` is set by hardware. As a result, the transmitter sends an XOFF character configured by `UART_XOFF_CHAR` after the current byte in transmission. If the RX FIFO of a

UART controller stores less data than `UART_XON_THRESHOLD`, `UART_SEND_XON` is set by hardware. As a result, the transmitter sends an XON character configured by `UART_XON_CHAR` after the current byte in transmission.

In full-duplex mode, when the UART receiver receives an XOFF character, the UART transmitter is not allowed to send any data including XOFF even if the UART receiver receives more data than its threshold. To avoid deadlocks in software flow control or overflow caused thereby, you can set `UART_XON_XOFF_STILL_SEND`. In this way, the UART transmitter can still send an XOFF character when it is not allowed to send any data.

### 37.4.10 GDMA Mode

The five UART controllers on ESP32-P4 share one TX/RX GDMA (General Direct Memory Access) channel via UHCI (Universal Host Controller Interface). In GDMA mode, UART controllers support the decoding and encoding of HCI data packets. The `UHCI_UART_SEL` field determines which UART controller occupies the GDMA TX/RX channel.

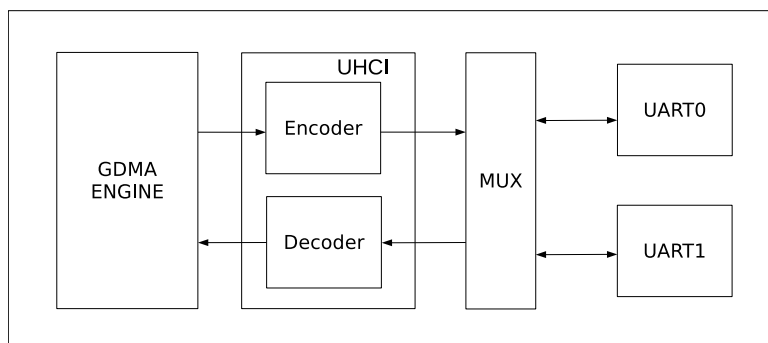


Figure 37.4-10. Data Transfer in GDMA Mode

Figure 37.4-10 shows how data is transferred using GDMA. Before GDMA receives data, software prepares an inlink. `GDMA_INLINK_ADDR_CH $n$`  points to the first receive descriptor in the inlink. After `GDMA_INLINK_START_CH $n$`  is set, UHCI sends data that UART has received to the decoder. The decoded data is then stored into the RAM pointed by the inlink under the control of GDMA.

Before GDMA sends data, software prepares an outlink and data to be sent. `GDMA_OUTLINK_ADDR_CH $n$`  points to the first transmit descriptor in the outlink. After `GDMA_OUTLINK_START_CH $n$`  is set, GDMA reads data from the RAM pointed by outlink. The data is then encoded by the encoder, and sent sequentially by the UART transmitter.

HCI data packets have separators at the beginning and the end, with data bits in the middle (separators + data bits + separators). The encoder inserts separators in front of and after data bits, and replaces data bits identical to separators with special characters. The decoder removes separators in front of and after data bits, and replaces special characters with separators. There can be more than one continuous separator at the beginning and the end of a data packet. The separator is configured by `UHCI_SEPER_CHAR`, 0xC0 by default. The special character is configured by `UHCI_ESC_SEQO_CHAR0` (0xDB by default) and `UHCI_ESC_SEQO_CHAR1` (0xDD by default). When all data has been sent, a `GDMA_OUT_TOTAL_EOF_CH $n$ _INT` interrupt is generated. When all data has been received, a `GDMA_IN_SUC_EOF_CH $n$ _INT` is generated.



### 37.4.11 Interrupts

ESP32-P4's UART<sub>n</sub> and UHCI can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- UART<sub>n</sub>\_INTR
- UHCI\_INTR

There are several internal interrupt sources from UART<sub>n</sub> and UHCI that can generate the above interrupt signals.

UART<sub>n</sub> interrupt sources are listed as follows:

- UART\_AT\_CMD\_CHAR\_DET\_INT: Triggered when the receiver detects an AT\_CMD character.
- UART\_RS485\_CLASH\_INT: Triggered when a collision is detected between the transmitter and the receiver in RS485 mode.
- UART\_RS485\_FRM\_ERR\_INT: Triggered when an error is detected in the data frame sent by the transmitter in RS485 mode.
- UART\_RS485\_PARITY\_ERR\_INT: Triggered when an error is detected in the parity bit sent by the transmitter in RS485 mode.
- UART\_TX\_DONE\_INT: Triggered when all data in the transmitter's TX FIFO has been sent.
- UART\_TX\_BRK\_IDLE\_DONE\_INT: Triggered when the transmitter stays idle for the minimum interval (threshold) after sending the last data bit.
- UART\_TX\_BRK\_DONE\_INT: Triggered when the transmitter has sent all NULL characters after all data in TX FIFO had been sent.
- UART\_GLITCH\_DET\_INT: Triggered when the receiver detects a glitch in the middle of the start bit.
- UART\_SW\_XOFF\_INT: Triggered when [UART\\_SW\\_FLOW\\_CON\\_EN](#) is set and the receiver receives a XOFF character.
- UART\_SW\_XON\_INT: Triggered when [UART\\_SW\\_FLOW\\_CON\\_EN](#) is set and the receiver receives a XON character.
- UART\_RXFIFO\_TOUT\_INT: Triggered when the receiver has received at least one byte, and the bus remains idle for [UART\\_RX\\_TOUT\\_THRHD](#) bit time.
- UART\_BRK\_DET\_INT: Triggered when the receiver detects a NULL character (i.e., logic 0 for one NULL character transmission) after stop bits.
- UART\_CTS\_CHG\_INT: Triggered when the receiver detects an edge change of CTS<sub>n</sub> signals.
- UART\_DSR\_CHG\_INT: Triggered when the receiver detects an edge change of DSR<sub>n</sub> signals.
- UART\_RXFIFO\_OVF\_INT: Triggered when the amount of data received by the receiver exceeds the storage capacity of the FIFO.
- UART\_FRM\_ERR\_INT: Triggered when the receiver detects a data frame error.
- UART\_PARITY\_ERR\_INT: Triggered when the receiver detects a parity error.
- UART\_TXFIFO\_EMPTY\_INT: Triggered when TX FIFO stores less data than what [UART\\_TXFIFO\\_EMPTY\\_THRHD](#) specifies.

- UART\_RXFIFO\_FULL\_INT: Triggered when the receiver receives more data than what [UART\\_RXFIFO\\_FULL\\_THRHD](#) specifies.
- UART\_WAKEUP\_INT: Triggered when UART is woken up.

UHCI interrupt sources are listed as follows:

- UHCI\_APP\_CTRL1\_INT: Triggered when software sets [UHCI\\_APP\\_CTRL1\\_INT\\_RAW](#).
- UHCI\_APP\_CTRL0\_INT: Triggered when software sets [UHCI\\_APP\\_CTRL0\\_INT\\_RAW](#).
- UHCI\_OUTLINK\_EOF\_ERR\_INT: Triggered when an EOF error is detected in a transmit descriptor.
- UHCI\_SEND\_A\_REG\_Q\_INT: Triggered when UHCI has sent a series of short packets using `always_send`.
- UHCI\_SEND\_S\_REG\_Q\_INT: Triggered when UHCI has sent a series of short packets using `single_send`.
- UHCI\_TX\_HUNG\_INT: Triggered when UHCI takes too long to read RAM using a GDMA transmit channel.
- UHCI\_RX\_HUNG\_INT: Triggered when UHCI takes too long to receive data using a GDMA receive channel.
- UHCI\_TX\_START\_INT: Triggered when GDMA detects a separator character.
- UHCI\_RX\_START\_INT: Triggered when a separator character has been sent.

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [37.6 Register Summary](#).

## 37.5 Programming Procedures

### 37.5.1 Register Type

All UART registers are in the APB\_CLK domain.

UART configuration registers can be classified into two groups. One group of registers are read in the APB\_CLK or AHB\_CLK domains, so once such registers are configured no extra operations are required. The other group of registers are read in the UART\_SCLK domain, and therefore need to implement the clock domain crossing design. Once these registers are configured, the configured values need to be synchronized to the UART Core's clock domain by writing to [UART\\_REG\\_UPDATE](#). Once all values have been synchronized, [UART\\_REG\\_UPDATE](#) will be automatically cleared by hardware. After configuring registers that need synchronization, it is recommended to check whether [UART\\_REG\\_UPDATE](#) is 0. This is to ensure that register values configured before have already been synchronized.

To distinguish between these two groups of registers easily, all registers that implement the clock domain crossing design have the `_SYNC` suffix, and are put together in Section [37.6](#). Those without the `_SYNC` suffix in Section [37.6](#) are configuration registers that require no clock domain crossing.

## 37.5.2 Detailed Steps

Figure 37.5-1 illustrates the process to program UART controllers, namely initialize UART, configure registers, enable the UART transmitter or receiver, and finish data transmission.

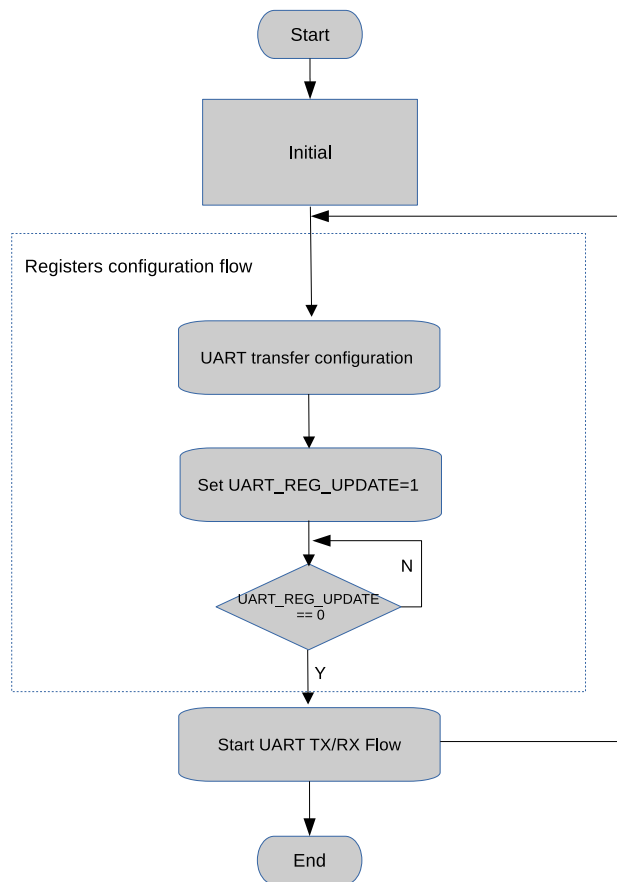


Figure 37.5-1. UART Programming Procedures

### 37.5.2.1 Initializing UART $n$

To initialize UART $n$ :

- Write 1 to `HP_SYS_CLKRST_RST_EN_UART $n$ _APB`.
- Clear `HP_SYS_CLKRST_RST_EN_UART $n$ _APB` to 0.
- Write 1 to `HP_SYS_CLKRST_RST_EN_UART $n$ _CORE`.
- Clear `HP_SYS_CLKRST_RST_EN_UART $n$ _CORE` to 0.

### 37.5.2.2 Configuring UART $n$ Communication

To configure UART $n$  communication:

- Wait for `UART_REG_UPDATE` to become 0, which indicates the completion of the last synchronization.
- Select the clock source via `HP_SYS_CLKRST_UART $n$ _CLK_SRC_SEL`.
- Configure divisor of the divider via `HP_SYS_CLKRST_UART $n$ _SCLK_DIV_NUM`, `HP_SYS_CLKRST_UART $n$ _SCLK_DIV_DENOMINATOR`, and

[HP\\_SYS\\_CLKRST\\_UARTn\\_SCLK\\_DIV\\_NUMERATOR](#).

- Configure the baud rate for transmission via [UART\\_CLKDIV](#) and [UART\\_CLKDIV\\_FRAG](#).
- Configure data length via [UART\\_BIT\\_NUM](#).
- Configure odd or even parity check via [UART\\_PARITY\\_EN](#) and [UART\\_PARITY](#).
- Optional steps depending on application ...
- Synchronize the configured values to the Core Clock domain by writing 1 to [UART\\_REG\\_UPDATE](#).

### 37.5.2.3 Enabling UARTn

To enable UARTn transmitter:

- Configure TX FIFO's empty threshold via [UART\\_TXFIFO\\_EMPTY\\_THRHD](#).
- Disable UART\_TXFIFO\_EMPTY\_INT interrupt by clearing [UART\\_TXFIFO\\_EMPTY\\_INT\\_ENA](#).
- Write data to be sent to [UART\\_RXFIFO\\_RD\\_BYTE](#).
- Clear UART\_TXFIFO\_EMPTY\_INT interrupt by setting [UART\\_TXFIFO\\_EMPTY\\_INT\\_CLR](#).
- Enable UART\_TXFIFO\_EMPTY\_INT interrupt by setting [UART\\_TXFIFO\\_EMPTY\\_INT\\_ENA](#).
- Check [UART\\_TXFIFO\\_EMPTY\\_INT\\_ST](#) and wait for the completion of data transmission.

To enable UARTn receiver:

- Configure RX FIFO's full threshold via [UART\\_RXFIFO\\_FULL\\_THRHD](#).
- Enable UART\_RXFIFO\_FULL\_INT interrupt by setting [UART\\_RXFIFO\\_FULL\\_INT\\_ENA](#).
- Check [UART\\_RXFIFO\\_FULL\\_INT\\_ST](#) and wait until the RX FIFO is full.
- Read data from RX FIFO via [UART\\_RXFIFO\\_RD\\_BYTE](#), and obtain the number of bytes received in RX FIFO via [UART\\_RXFIFO\\_CNT](#).

## 37.6 Register Summary

### 37.6.1 UART Register Summary

The addresses in this section are relative to UART Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description                                   | Address | Access   |
|---|---|---------|----------|
| <b>FIFO Configuration</b>                         |   |         |          |
| <a href="#">UART_FIFO_REG</a>                     | FIFO data register                            | 0x0000  | RO       |
| <a href="#">UART_TOUT_CONF_SYNC_REG</a>           | UART threshold and allocation configuration   | 0x0064  | R/W      |
| <b>UART Interrupt Register</b>                    |   |         |          |
| <a href="#">UART_INT_RAW_REG</a>                  | Raw interrupt status                          | 0x0004  | R/WTC/SS |
| <a href="#">UART_INT_ST_REG</a>                   | Masked interrupt status                       | 0x0008  | RO       |
| <a href="#">UART_INT_ENA_REG</a>                  | Interrupt enable bits                         | 0x000C  | R/W      |
| <a href="#">UART_INT_CLR_REG</a>                  | Interrupt clear bits                          | 0x0010  | WT       |
| <b>Configuration Register</b>                     |   |         |          |
| <a href="#">UART_CLKDIV_SYNC_REG</a>              | Clock divider configuration                   | 0x0014  | R/W      |
| <a href="#">UART_RX_FILT_REG</a>                  | RX filter configuration                       | 0x0018  | R/W      |
| <a href="#">UART_CONFO_SYNC_REG</a>               | Configuration register 0                      | 0x0020  | R/W      |
| <a href="#">UART_CONF1_REG</a>                    | Configuration register 1                      | 0x0024  | R/W      |
| <a href="#">UART_HWFC_CONF_SYNC_REG</a>           | Hardware flow control configuration           | 0x002C  | R/W      |
| <a href="#">UART_SLEEP_CONFO_REG</a>              | UART sleep configuration register 0           | 0x0030  | R/W      |
| <a href="#">UART_SLEEP_CONF1_REG</a>              | UART sleep configuration register 1           | 0x0034  | R/W      |
| <a href="#">UART_SLEEP_CONF2_REG</a>              | UART sleep configuration register 2           | 0x0038  | R/W      |
| <a href="#">UART_SWFC_CONFO_SYNC_REG</a>          | Software flow control character configuration | 0x003C  | varies   |
| <a href="#">UART_SWFC_CONF1_REG</a>               | Software flow control character configuration | 0x0040  | R/W      |
| <a href="#">UART_TXBRK_CONF_SYNC_REG</a>          | TX break character configuration              | 0x0044  | R/W      |
| <a href="#">UART_IDLE_CONF_SYNC_REG</a>           | Frame end idle time configuration             | 0x0048  | R/W      |
| <a href="#">UART_RS485_CONF_SYNC_REG</a>          | RS485 mode configuration                      | 0x004C  | R/W      |
| <a href="#">UART_CLK_CONF_REG</a>                 | UART core clock configuration                 | 0x0088  | R/W      |
| <a href="#">UART_REG_UPDATE_REG</a>               | UART register configuration update            | 0x0098  | R/W/SC   |
| <a href="#">UART_ID_REG</a>                       | UART ID register                              | 0x009C  | R/W      |
| <b>Status Register</b>                            |   |         |          |
| <a href="#">UART_STATUS_REG</a>                   | UART status register                          | 0x001C  | RO       |
| <a href="#">UART_MEM_TX_STATUS_REG</a>            | TX FIFO write and read offset address         | 0x0068  | RO       |
| <a href="#">UART_MEM_RX_STATUS_REG</a>            | Rx FIFO write and read offset address         | 0x006C  | RO       |
| <a href="#">UART_FSM_STATUS_REG</a>               | UART transmit and receive status              | 0x0070  | RO       |
| <a href="#">UART_AFIFO_STATUS_REG</a>             | UART asynchronous FIFO status                 | 0x0090  | RO       |
| <b>AT Escape Sequence Selection Configuration</b> |   |         |          |
| <a href="#">UART_AT_CMD_PRECNT_SYNC_REG</a>       | Pre-sequence timing configuration             | 0x0050  | R/W      |
| <a href="#">UART_AT_CMD_POSTCNT_SYNC_REG</a>      | Post-sequence timing configuration            | 0x0054  | R/W      |
| <a href="#">UART_AT_CMD_GAP_TOUT_SYNC_REG</a>     | Timeout configuration                         | 0x0058  | R/W      |

| Name                                      | Description                                   | Address | Access |
|---|---|---------|--------|
| <a href="#">UART_AT_CMD_CHAR_SYNC_REG</a> | AT escape sequence detection configuration    | 0x005C  | R/W    |
| <b>Autobaud Register</b>                  |   |         |        |
| <a href="#">UART_POSPULSE_REG</a>         | Autobaud high pulse register                  | 0x0074  | RO     |
| <a href="#">UART_NEGPULSE_REG</a>         | Autobaud low pulse register                   | 0x0078  | RO     |
| <a href="#">UART_LOWPULSE_REG</a>         | Autobaud minimum low pulse duration register  | 0x007C  | RO     |
| <a href="#">UART_HIGHPULSE_REG</a>        | Autobaud minimum high pulse duration register | 0x0080  | RO     |
| <a href="#">UART_RXD_CNT_REG</a>          | Autobaud edge change count register           | 0x0084  | RO     |
| <b>Version Register</b>                   |   |         |        |
| <a href="#">UART_DATE_REG</a>             | UART version control register                 | 0x008C  | R/W    |

## 37.6.2 LP UART Register Summary

The addresses in this section are relative to LP UART base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description                                    | Address | Access   |
|---|--|---------|----------|
| <b>FIFO Configuration</b>                   |  |         |          |
| <a href="#">LP_UART_FIFO_REG</a>            | FIFO data register                             | 0x0000  | RO       |
| <a href="#">LP_UART_TOUT_CONF_SYNC_REG</a>  | LP UART threshold and allocation configuration | 0x0064  | R/W      |
| <b>LP UART Interrupt Register</b>           |  |         |          |
| <a href="#">LP_UART_INT_RAW_REG</a>         | Raw interrupt status                           | 0x0004  | R/WTC/SS |
| <a href="#">LP_UART_INT_ST_REG</a>          | Masked interrupt status                        | 0x0008  | RO       |
| <a href="#">LP_UART_INT_ENA_REG</a>         | Interrupt enable bits                          | 0x000C  | R/W      |
| <a href="#">LP_UART_INT_CLR_REG</a>         | Interrupt clear bits                           | 0x0010  | WT       |
| <b>Configuration Register</b>               |  |         |          |
| <a href="#">LP_UART_CLKDIV_SYNC_REG</a>     | Clock divider configuration                    | 0x0014  | R/W      |
| <a href="#">LP_UART_RX_FILT_REG</a>         | RX filter configuration                        | 0x0018  | R/W      |
| <a href="#">LP_UART_CONFO_SYNC_REG</a>      | Configuration register 0                       | 0x0020  | R/W      |
| <a href="#">LP_UART_CONF1_REG</a>           | Configuration register 1                       | 0x0024  | R/W      |
| <a href="#">LP_UART_HWFC_CONF_SYNC_REG</a>  | Hardware flow control configuration            | 0x002C  | R/W      |
| <a href="#">LP_UART_SLEEP_CONFO_REG</a>     | LP UART sleep configuration register 0         | 0x0030  | R/W      |
| <a href="#">LP_UART_SLEEP_CONF1_REG</a>     | LP UART sleep configuration register 1         | 0x0034  | R/W      |
| <a href="#">LP_UART_SLEEP_CONF2_REG</a>     | LP UART sleep configuration register 2         | 0x0038  | R/W      |
| <a href="#">LP_UART_SWFC_CONFO_SYNC_REG</a> | Software flow control character configuration  | 0x003C  | varies   |
| <a href="#">LP_UART_SWFC_CONF1_REG</a>      | Software flow control character configuration  | 0x0040  | R/W      |
| <a href="#">LP_UART_TXBRK_CONF_SYNC_REG</a> | TX break character configuration               | 0x0044  | R/W      |
| <a href="#">LP_UART_IDLE_CONF_SYNC_REG</a>  | Frame end idle time configuration              | 0x0048  | R/W      |
| <a href="#">LP_UART_CLK_CONF_REG</a>        | LP UART core clock configuration               | 0x0088  | R/W      |

| Name  | Description                                    | Address | Access |
|---|--|---------|--------|
| <a href="#">LP_UART_REG_UPDATE_REG</a>            | LP UART register configuration update register | 0x0098  | R/W/SC |
| <a href="#">LP_UART_ID_REG</a>                    | LP UART ID register                            | 0x009C  | R/W    |
| <b>Status Register</b>                            |  |         |        |
| <a href="#">LP_UART_STATUS_REG</a>                | LP UART status register                        | 0x001C  | RO     |
| <a href="#">LP_UART_MEM_TX_STATUS_REG</a>         | TX FIFO write and read offset address          | 0x0068  | RO     |
| <a href="#">LP_UART_MEM_RX_STATUS_REG</a>         | RX FIFO write and read offset address          | 0x006C  | RO     |
| <a href="#">LP_UART_FSM_STATUS_REG</a>            | LP UART transmit and receive status            | 0x0070  | RO     |
| <a href="#">LP_UART_AFIFO_STATUS_REG</a>          | LP UART asynchronous FIFO Status               | 0x0090  | RO     |
| <b>AT Escape Sequence Selection Configuration</b> |  |         |        |
| <a href="#">LP_UART_AT_CMD_PRECNT_SYNC_REG</a>    | Pre-sequence timing configuration              | 0x0050  | R/W    |
| <a href="#">LP_UART_AT_CMD_POSTCNT_SYNC_REG</a>   | Post-sequence timing configuration             | 0x0054  | R/W    |
| <a href="#">LP_UART_AT_CMD_GAPTOOUT_SYNC_REG</a>  | Timeout configuration                          | 0x0058  | R/W    |
| <a href="#">LP_UART_AT_CMD_CHAR_SYNC_REG</a>      | AT escape sequence detection configuration     | 0x005C  | R/W    |
| <b>Version Register</b>                           |  |         |        |
| <a href="#">LP_UART_DATE_REG</a>                  | LP UART version register                       | 0x008C  | R/W    |

### 37.6.3 UHCI Register Summary

The addresses in this section are relative to UHCI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                  | Description                            | Address | Access |
|---------------------------------------|--|---------|--------|
| <b>Configuration Register</b>         |  |         |        |
| <a href="#">UHCI_CONFO_REG</a>        | UHCI configuration register            | 0x0000  | R/W    |
| <a href="#">UHCI_CONF1_REG</a>        | UHCI configuration register            | 0x0014  | varies |
| <a href="#">UHCI_ESCAPE_CONF_REG</a>  | Escape character configuration         | 0x0020  | R/W    |
| <a href="#">UHCI_HUNG_CONF_REG</a>    | Timeout configuration                  | 0x0024  | R/W    |
| <a href="#">UHCI_ACK_NUM_REG</a>      | UHCI ACK number configuration          | 0x0028  | varies |
| <a href="#">UHCI_QUICK_SENT_REG</a>   | UHCI quick send configuration register | 0x0030  | varies |
| <a href="#">UHCI_REG_Q0_WORD0_REG</a> | Q0 WORD0 quick send register           | 0x0034  | R/W    |
| <a href="#">UHCI_REG_Q0_WORD1_REG</a> | Q0 WORD1 quick send register           | 0x0038  | R/W    |
| <a href="#">UHCI_REG_Q1_WORD0_REG</a> | Q1 WORD0 quick send register           | 0x003C  | R/W    |
| <a href="#">UHCI_REG_Q1_WORD1_REG</a> | Q1 WORD1 quick send register           | 0x0040  | R/W    |
| <a href="#">UHCI_REG_Q2_WORD0_REG</a> | Q2 WORD0 quick send register           | 0x0044  | R/W    |
| <a href="#">UHCI_REG_Q2_WORD1_REG</a> | Q2 WORD1 quick send register           | 0x0048  | R/W    |
| <a href="#">UHCI_REG_Q3_WORD0_REG</a> | Q3 WORD0 quick send register           | 0x004C  | R/W    |
| <a href="#">UHCI_REG_Q3_WORD1_REG</a> | Q3 WORD1 quick send register           | 0x0050  | R/W    |
| <a href="#">UHCI_REG_Q4_WORD0_REG</a> | Q4 WORD0 quick send register           | 0x0054  | R/W    |
| <a href="#">UHCI_REG_Q4_WORD1_REG</a> | Q4 WORD1 quick send register           | 0x0058  | R/W    |
| <a href="#">UHCI_REG_Q5_WORD0_REG</a> | Q5 WORD0 quick send register           | 0x005C  | R/W    |

| Name                                  | Description                              | Address | Access |
|---------------------------------------|--|---------|--------|
| <a href="#">UHCI_REG_Q5_WORD1_REG</a> | Q5 WORD1 quick send register             | 0x0060  | R/W    |
| <a href="#">UHCI_REG_Q6_WORD0_REG</a> | Q6 WORD0 quick send register             | 0x0064  | R/W    |
| <a href="#">UHCI_REG_Q6_WORD1_REG</a> | Q6 WORD1 quick register                  | 0x0068  | R/W    |
| <a href="#">UHCI_ESC_CONF0_REG</a>    | Escape sequence configuration register 0 | 0x006C  | R/W    |
| <a href="#">UHCI_ESC_CONF1_REG</a>    | Escape sequence configuration register 1 | 0x0070  | R/W    |
| <a href="#">UHCI_ESC_CONF2_REG</a>    | Escape sequence configuration register 2 | 0x0074  | R/W    |
| <a href="#">UHCI_ESC_CONF3_REG</a>    | Escape sequence configuration register 3 | 0x0078  | R/W    |
| <a href="#">UHCI_PKT_THRES_REG</a>    | Configuration register for packet length | 0x007C  | R/W    |
| <b>UHCI Interrupt Register</b>        |  |         |        |
| <a href="#">UHCI_INT_RAW_REG</a>      | Raw interrupt status                     | 0x0004  | varies |
| <a href="#">UHCI_INT_ST_REG</a>       | Masked interrupt status                  | 0x0008  | RO     |
| <a href="#">UHCI_INT_ENA_REG</a>      | Interrupt enable bits                    | 0x000C  | R/W    |
| <a href="#">UHCI_INT_CLR_REG</a>      | Interrupt clear bits                     | 0x0010  | WT     |
| <b>UHCI Status Register</b>           |  |         |        |
| <a href="#">UHCI_STATE0_REG</a>       | UHCI receive status                      | 0x0018  | RO     |
| <a href="#">UHCI_STATE1_REG</a>       | UHCI transmit status                     | 0x001C  | RO     |
| <a href="#">UHCI_RX_HEAD_REG</a>      | UHCI packet header register              | 0x002C  | RO     |
| <b>Version Register</b>               |  |         |        |
| <a href="#">UHCI_DATE_REG</a>         | UHCI version control register            | 0x0080  | R/W    |



## 37.7 Registers

### 37.7.1 UART Registers

The addresses in this section are relative to UART Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 37.1. UART\_FIFO\_REG (0x0000)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UART_RXFIFO_RD_BYTE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8                   | 7 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**UART\_RXFIFO\_RD\_BYTE** Represents the data UART *n* read from FIFO.  
Measurement unit: byte. (RO)

**Register 37.2. UART\_TOUT\_CONF\_SYNC\_REG (0x0064)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |                 |  |       |  |  |  |  |  |   |  |  |  |   |  |   |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|-----------------|--|-------|--|--|--|--|--|---|--|--|--|---|--|---|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_RX_TOUT_THRHD |  |  |  |  |  |  |  |  |  |  |  | UART_RX_TOUT_FLOW_DIS |  |  |  | UART_RX_TOUT_EN |  |       |  |  |  |  |  |   |  |  |  |   |  |   |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12                 |  |  |  |  |  |  |  |  |  |  |  | 11                    |  |  |  |                 |  |       |  |  |  |  |  | 2 |  |  |  | 1 |  | 0 |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0xa                |  |  |  |  |  |  |  |  |  |  |  | 0                     |  |  |  | 0               |  | Reset |  |  |  |  |  |   |  |  |  |   |  |   |  |

**UART\_RX\_TOUT\_EN** Configures whether or not to enable UART receiver's timeout function.  
0: Disable  
1: Enable  
(R/W)

**UART\_RX\_TOUT\_FLOW\_DIS** Configures whether or not to disable the idle status counter when hardware flow control is enabled.  
0: Enable  
1: Disable  
(R/W)

**UART\_RX\_TOUT\_THRHD** Configures the amount of time that the bus can remain idle before timeout.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)

Register 37.3. UART\_INT\_RAW\_REG (0x0004)

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |   |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|---|----|----|----|----|----|----|----|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | UART_WAKEUP_INT_RAW<br>UART_AT_CMD_CHAR_DET_INT_RAW<br>UART_RS485_CLASH_INT_RAW<br>UART_RS485_FRM_ERR_INT_RAW<br>UART_RS485_PARITY_ERR_INT_RAW<br>UART_TX_DONE_INT_RAW<br>UART_TX_BRK_IDLE_DONE_INT_RAW<br>UART_GLITCH_DET_INT_RAW<br>UART_SW_XON_INT_RAW<br>UART_SW_XOFF_INT_RAW<br>UART_RXFIFO_TOUT_INT_RAW<br>UART_BRK_DET_INT_RAW<br>UART_CTS_CHG_INT_RAW<br>UART_DSR_CHG_INT_RAW<br>UART_RXFIFO_EMPTY_INT_RAW<br>UART_FRM_ERR_INT_RAW<br>UART_PARITY_ERR_INT_RAW<br>UART_TXFIFO_FULL_INT_RAW |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17  | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 1 | 0 | Reset |   |   |   |   |

**UART\_RXFIFO\_FULL\_INT\_RAW** The raw interrupt status of UART\_RXFIFO\_FULL\_INT. (R/WTC/SS)

**UART\_TXFIFO\_EMPTY\_INT\_RAW** The raw interrupt status of UART\_TXFIFO\_EMPTY\_INT. (R/WTC/SS)

**UART\_PARITY\_ERR\_INT\_RAW** The raw interrupt status of UART\_PARITY\_ERR\_INT. (R/WTC/SS)

**UART\_FRM\_ERR\_INT\_RAW** The raw interrupt status of UART\_FRM\_ERR\_INT. (R/WTC/SS)

**UART\_RXFIFO\_OVF\_INT\_RAW** The raw interrupt status of UART\_RXFIFO\_OVF\_INT. (R/WTC/SS)

**UART\_DSR\_CHG\_INT\_RAW** The raw interrupt status of UART\_DSR\_CHG\_INT. (R/WTC/SS)

**UART\_CTS\_CHG\_INT\_RAW** The raw interrupt status of UART\_CTS\_CHG\_INT. (R/WTC/SS)

**UART\_BRK\_DET\_INT\_RAW** The raw interrupt status of UART\_BRK\_DET\_INT. (R/WTC/SS)

**UART\_RXFIFO\_TOUT\_INT\_RAW** The raw interrupt status of UART\_RXFIFO\_TOUT\_INT. (R/WTC/SS)

**UART\_SW\_XON\_INT\_RAW** The raw interrupt status of UART\_SW\_XON\_INT. (R/WTC/SS)

**UART\_SW\_XOFF\_INT\_RAW** UART\_SW\_XOFF\_INT. (R/WTC/SS)

**UART\_GLITCH\_DET\_INT\_RAW** The raw interrupt status of UART\_GLITCH\_DET\_INT. (R/WTC/SS)

**UART\_TX\_BRK\_DONE\_INT\_RAW** The raw interrupt status of UART\_TX\_BRK\_DONE\_INT. (R/WTC/SS)

**UART\_TX\_BRK\_IDLE\_DONE\_INT\_RAW** The raw interrupt status of UART\_TX\_BRK\_IDLE\_DONE\_INT.  
(R/WTC/SS)

**UART\_TX\_DONE\_INT\_RAW** The raw interrupt status of UART\_TX\_DONE\_INT. (R/WTC/SS)

**UART\_RS485\_PARITY\_ERR\_INT\_RAW** The raw interrupt status of UART\_RS485\_PARITY\_ERR\_INT.  
(R/WTC/SS)

**UART\_RS485\_FRM\_ERR\_INT\_RAW** The raw interrupt status of UART\_RS485\_FRM\_ERR\_INT.  
(R/WTC/SS)

Continued on the next page...

**Register 37.3. UART\_INT\_RAW\_REG (0x0004)**

Continued from the previous page...

**UART\_RS485\_CLASH\_INT\_RAW** The raw interrupt status of UART\_RS485\_CLASH\_INT. (R/WTC/SS)

**UART\_AT\_CMD\_CHAR\_DET\_INT\_RAW** The raw interrupt status of UART\_AT\_CMD\_CHAR\_DET\_INT.  
(R/WTC/SS)

**UART\_WAKEUP\_INT\_RAW** The raw interrupt status of UART\_WAKEUP\_INT. (R/WTC/SS)

**Register 37.4. UART\_INT\_ST\_REG (0x0008)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |  |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|--|----|----|----|----|----|----|----|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | UART_WAKEUP_INT_ST<br>UART_AT_CMD_CHAR_DET_INT_ST<br>UART_RS485_CLASH_INT_ST<br>UART_RS485_FRM_ERR_INT_ST<br>UART_RS485_PARITY_ERR_INT_ST<br>UART_TX_DONE_INT_ST<br>UART_TX_BRK_IDLE_DONE_INT_ST<br>UART_GLITCH_DET_INT_ST<br>UART_SW_XON_INT_ST<br>UART_SW_XOFF_INT_ST<br>UART_RXFIFO_TOUT_INT_ST<br>UART_CTS_CHG_INT_ST<br>UART_DSR_CHG_INT_ST<br>UART_RXFIFO_OVF_INT_ST<br>UART_FRM_ERR_INT_ST<br>UART_PARITY_ERR_INT_ST<br>UART_TXFIFO_EMPTY_INT_ST<br>UART_RXFIFO_FULL_INT_ST |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17   | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | Reset |   |   |   |   |

**UART\_RXFIFO\_FULL\_INT\_ST** The masked interrupt status of UART\_RXFIFO\_FULL\_INT. (RO)

**UART\_TXFIFO\_EMPTY\_INT\_ST** The masked interrupt status of UART\_TXFIFO\_EMPTY\_INT. (RO)

**UART\_PARITY\_ERR\_INT\_ST** The masked interrupt status of UART\_PARITY\_ERR\_INT. (RO)

**UART\_FRM\_ERR\_INT\_ST** The masked interrupt status of UART\_FRM\_ERR\_INT. (RO)

**UART\_RXFIFO\_OVF\_INT\_ST** The masked interrupt status of UART\_RXFIFO\_OVF\_INT. (RO)

**UART\_DSR\_CHG\_INT\_ST** The masked interrupt status of UART\_DSR\_CHG\_INT. (RO)

**UART\_CTS\_CHG\_INT\_ST** The masked interrupt status of UART\_CTS\_CHG\_INT. (RO)

**UART\_BRK\_DET\_INT\_ST** The masked interrupt status of UART\_BRK\_DET\_INT. (RO)

**UART\_RXFIFO\_TOUT\_INT\_ST** The masked interrupt status of UART\_RXFIFO\_TOUT\_INT. (RO)

**UART\_SW\_XON\_INT\_ST** The masked interrupt status of UART\_SW\_XON\_INT. (RO)

**UART\_SW\_XOFF\_INT\_ST** The masked interrupt status of UART\_SW\_XOFF\_INT. (RO)

**UART\_GLITCH\_DET\_INT\_ST** The masked interrupt status of UART\_GLITCH\_DET\_INT. (RO)

**UART\_TX\_BRK\_DONE\_INT\_ST** The masked interrupt status of UART\_TX\_BRK\_DONE\_INT. (RO)

**UART\_TX\_BRK\_IDLE\_DONE\_INT\_ST** The masked interrupt status of UART\_TX\_BRK\_IDLE\_DONE\_INT. (RO)

**UART\_TX\_DONE\_INT\_ST** The masked interrupt status of UART\_TX\_DONE\_INT. (RO)

**UART\_RS485\_PARITY\_ERR\_INT\_ST** The masked interrupt status of UART\_RS485\_PARITY\_ERR\_INT. (RO)

**UART\_RS485\_FRM\_ERR\_INT\_ST** The masked interrupt status of UART\_RS485\_FRM\_ERR\_INT. (RO)

**UART\_RS485\_CLASH\_INT\_ST** The masked interrupt status of UART\_RS485\_CLASH\_INT. (RO)

**UART\_AT\_CMD\_CHAR\_DET\_INT\_ST** The masked interrupt status of UART\_AT\_CMD\_CHAR\_DET\_INT. (RO)

**UART\_WAKEUP\_INT\_ST** The masked interrupt status of UART\_WAKEUP\_INT. (RO)

**Register 37.5. UART\_INT\_ENA\_REG (0x000C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_WAKEUP_INT_ENA<br>UART_AT_CMD_CHAR_DET_INT_ENA<br>UART_RS485_CLASH_INT_ENA<br>UART_RS485_FRM_ERR_INT_ENA<br>UART_RS485_PARITY_ERR_INT_ENA<br>UART_TX_DONE_INT_ENA<br>UART_TX_BRK_IDLE_DONE_INT_ENA<br>UART_GLITCH_DET_INT_ENA<br>UART_SW_XOFF_INT_ENA<br>UART_SW_XON_INT_ENA<br>UART_RXFIFO_TOUT_INT_ENA<br>UART_CTS_CHG_INT_ENA<br>UART_DSR_CHG_INT_ENA<br>UART_RXFIFO_OVF_INT_ENA<br>UART_FRM_ERR_INT_ENA<br>UART_PARITY_ERR_INT_ENA<br>UART_TXFIFO_EMPTY_INT_ENA<br>UART_RXFIFO_FULL_INT_ENA |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 20   | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   | Reset |

**UART\_RXFIFO\_FULL\_INT\_ENA** Write 1 to enable UART\_RXFIFO\_FULL\_INT. (R/W)

**UART\_TXFIFO\_EMPTY\_INT\_ENA** Write 1 to enable UART\_TXFIFO\_EMPTY\_INT. (R/W)

**UART\_PARITY\_ERR\_INT\_ENA** Write 1 to enable UART\_PARITY\_ERR\_INT. (R/W)

**UART\_FRM\_ERR\_INT\_ENA** Write 1 to enable UART\_FRM\_ERR\_INT. (R/W)

**UART\_RXFIFO\_OVF\_INT\_ENA** Write 1 to enable UART\_RXFIFO\_OVF\_INT. (R/W)

**UART\_DSR\_CHG\_INT\_ENA** Write 1 to enable UART\_DSR\_CHG\_INT. (R/W)

**UART\_CTS\_CHG\_INT\_ENA** Write 1 to enable UART\_CTS\_CHG\_INT. (R/W)

**UART\_BRK\_DET\_INT\_ENA** Write 1 to enable UART\_BRK\_DET\_INT. (R/W)

**UART\_RXFIFO\_TOUT\_INT\_ENA** Write 1 to enable UART\_RXFIFO\_TOUT\_INT. (R/W)

**UART\_SW\_XON\_INT\_ENA** Write 1 to enable UART\_SW\_XON\_INT. (R/W)

**UART\_SW\_XOFF\_INT\_ENA** Write 1 to enable UART\_SW\_XOFF\_INT. (R/W)

**UART\_GLITCH\_DET\_INT\_ENA** Write 1 to enable UART\_GLITCH\_DET\_INT. (R/W)

**UART\_TX\_BRK\_DONE\_INT\_ENA** Write 1 to enable UART\_TX\_BRK\_DONE\_INT. (R/W)

**UART\_TX\_BRK\_IDLE\_DONE\_INT\_ENA** Write 1 to enable UART\_TX\_BRK\_IDLE\_DONE\_INT. (R/W)

**UART\_TX\_DONE\_INT\_ENA** Write 1 to enable UART\_TX\_DONE\_INT. (R/W)

**UART\_RS485\_PARITY\_ERR\_INT\_ENA** Write 1 to enable UART\_RS485\_PARITY\_ERR\_INT. (R/W)

**UART\_RS485\_FRM\_ERR\_INT\_ENA** Write 1 to enable UART\_RS485\_FRM\_ERR\_INT. (R/W)

**UART\_RS485\_CLASH\_INT\_ENA** Write 1 to enable UART\_RS485\_CLASH\_INT. (R/W)

**UART\_AT\_CMD\_CHAR\_DET\_INT\_ENA** Write 1 to enable UART\_AT\_CMD\_CHAR\_DET\_INT. (R/W)

**UART\_WAKEUP\_INT\_ENA** Write 1 to enable UART\_WAKEUP\_INT. (R/W)

**Register 37.6. UART\_INT\_CLR\_REG (0x0010)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |  |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|--|----|----|----|----|----|----|----|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | UART_WAKEUP_INT_CLR<br>UART_AT_CMD_CHAR_DET_INT_CLR<br>UART_RS485_CLASH_INT_CLR<br>UART_RS485_FRM_ERR_INT_CLR<br>UART_RS485_PARITY_ERR_INT_CLR<br>UART_TX_DONE_INT_CLR<br>UART_TX_BRK_IDLE_DONE_INT_CLR<br>UART_GLITCH_DET_INT_CLR<br>UART_SW_XOFF_INT_CLR<br>UART_SW_XON_INT_CLR<br>UART_RXFIFO_TOUT_INT_CLR<br>UART_BRK_DET_INT_CLR<br>UART_CTS_CHG_INT_CLR<br>UART_DSR_CHG_INT_CLR<br>UART_RXFIFO_OVF_INT_CLR<br>UART_FRM_ERR_INT_CLR<br>UART_PARITY_ERR_INT_CLR<br>UART_TXFIFO_EMPTY_INT_CLR<br>UART_RXFIFO_FULL_INT_CLR |    |    |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17   | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | Reset |   |   |   |   |

**UART\_RXFIFO\_FULL\_INT\_CLR** Write 1 to clear UART\_RXFIFO\_FULL\_INT. (WT)

**UART\_TXFIFO\_EMPTY\_INT\_CLR** Write 1 to clear UART\_TXFIFO\_EMPTY\_INT. (WT)

**UART\_PARITY\_ERR\_INT\_CLR** Write 1 to clear UART\_PARITY\_ERR\_INT. (WT)

**UART\_FRM\_ERR\_INT\_CLR** Write 1 to clear UART\_FRM\_ERR\_INT. (WT)

**UART\_RXFIFO\_OVF\_INT\_CLR** Write 1 to clear UART\_RXFIFO\_OVF\_INT. (WT)

**UART\_DSR\_CHG\_INT\_CLR** Write 1 to clear UART\_DSR\_CHG\_INT. (WT)

**UART\_CTS\_CHG\_INT\_CLR** Write 1 to clear UART\_CTS\_CHG\_INT. (WT)

**UART\_BRK\_DET\_INT\_CLR** Write 1 to clear UART\_BRK\_DET\_INT. (WT)

**UART\_RXFIFO\_TOUT\_INT\_CLR** Write 1 to clear UART\_RXFIFO\_TOUT\_INT. (WT)

**UART\_SW\_XON\_INT\_CLR** Write 1 to clear UART\_SW\_XON\_INT. (WT)

**UART\_SW\_XOFF\_INT\_CLR** Write 1 to clear UART\_SW\_XOFF\_INT. (WT)

**UART\_GLITCH\_DET\_INT\_CLR** Write 1 to clear UART\_GLITCH\_DET\_INT. (WT)

**UART\_TX\_BRK\_DONE\_INT\_CLR** Write 1 to clear UART\_TX\_BRK\_DONE\_INT. (WT)

**UART\_TX\_BRK\_IDLE\_DONE\_INT\_CLR** Write 1 to clear UART\_TX\_BRK\_IDLE\_DONE\_INT. (WT)

**UART\_TX\_DONE\_INT\_CLR** Write 1 to clear UART\_TX\_DONE\_INT. (WT)

**UART\_RS485\_PARITY\_ERR\_INT\_CLR** Write 1 to clear UART\_RS485\_PARITY\_ERR\_INT. (WT)

**UART\_RS485\_FRM\_ERR\_INT\_CLR** Write 1 to clear UART\_RS485\_FRM\_ERR\_INT. (WT)

**UART\_RS485\_CLASH\_INT\_CLR** Write 1 to clear UART\_RS485\_CLASH\_INT. (WT)

**UART\_AT\_CMD\_CHAR\_DET\_INT\_CLR** Write 1 to clear UART\_AT\_CMD\_CHAR\_DET\_INT. (WT)

**UART\_WAKEUP\_INT\_CLR** Write 1 to clear UART\_WAKEUP\_INT. (WT)

Register 37.7. UART\_CLKDIV\_SYNC\_REG (0x0014)

|            |   |   |   |   |   |   |   |                  |     |    |    |            |   |   |   |    |    |   |   |             |       |   |  |  |       |
|------------|---|---|---|---|---|---|---|------------------|-----|----|----|------------|---|---|---|----|----|---|---|-------------|-------|---|--|--|-------|
| (reserved) |   |   |   |   |   |   |   | UART_CLKDIV_FRAG |     |    |    | (reserved) |   |   |   |    |    |   |   | UART_CLKDIV |       |   |  |  |       |
| 31         |   |   |   |   |   |   |   | 24               | 23  | 20 | 19 |            |   |   |   | 12 | 11 |   |   |             |       | 0 |  |  |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0x0 |    |    |            | 0 | 0 | 0 | 0  | 0  | 0 | 0 | 0           | 0x2b6 |   |  |  | Reset |

- UART\_CLKDIV Configures the integral part of the divisor for baud rate generation. (R/W)
- UART\_CLKDIV\_FRAG Configures the fractional part of the divisor for baud rate generation. (R/W)

Register 37.8. UART\_RX\_FILT\_REG (0x0018)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UART_GLITCH_FILT_EN |   | UART_GLITCH_FILT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9 | 8                   | 7 | 0                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

- UART\_GLITCH\_FILT Configures the width of a pulse to be filtered.  
Measurement unit: UART Core's clock cycle.  
Pulses whose width is lower than this value will be ignored. (R/W)
- UART\_GLITCH\_FILT\_EN Configures whether or not to enable RX signal filter.  
0: Disable  
1: Enable  
(R/W)

**Register 37.9. UART\_CONFO\_SYNC\_REG (0x0020)**

| (reserved) |    |    |    |    |    |    |    | UART_TXFIFO_RST |    | UART_RXFIFO_RST |    | UART_SW_RSTS |    | UART_MEM_CLK_EN |    | UART_AUTOBAUD_EN |   | UART_ERR_WD_MASK |   | UART_DIS_RX_DAT_OVF |   | UART_TXD_INV |   | UART_RXD_INV |   | UART_IRDA_EN |  | UART_FLOW_EN |  | UART_LOOPBACK |  | UART_IRDA_RX_INV |  | UART_IRDA_TX_INV |  | UART_IRDA_WCTL |  | UART_IRDA_TX_EN |  | UART_IRDA_DPLX |  | UART_TXD_BRK |  | UART_STOP_BIT_NUM |  | UART_BIT_NUM |  | UART_PARITY_EN |  | UART_PARITY |  |
|------------|----|----|----|----|----|----|----|-----------------|----|-----------------|----|--------------|----|-----------------|----|------------------|---|------------------|---|---------------------|---|--------------|---|--------------|---|--------------|--|--------------|--|---------------|--|------------------|--|------------------|--|----------------|--|-----------------|--|----------------|--|--------------|--|-------------------|--|--------------|--|----------------|--|-------------|--|
| 31         | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17              | 16 | 15              | 14 | 13           | 12 | 11              | 10 | 9                | 8 | 7                | 6 | 5                   | 4 | 3            | 2 | 1            | 0 |              |  |              |  |               |  |                  |  |                  |  |                |  |                 |  |                |  |              |  |                   |  |              |  |                |  |             |  |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0               | 0  | 0               | 0  | 0            | 0  | 0               | 0  | 0                | 0 | 0                | 0 | 1                   |   | 3            |   | 0            | 0 | Reset        |  |              |  |               |  |                  |  |                  |  |                |  |                 |  |                |  |              |  |                   |  |              |  |                |  |             |  |

Reset

**UART\_PARITY** Configures the parity check mode.

0: Even parity

1: Odd parity

(R/W)

**UART\_PARITY\_EN** Configures whether or not to enable UART parity check.

0: Disable

1: Enable

(R/W)

**UART\_BIT\_NUM** Configures the number of data bits.

0: 5 bits

1: 6 bits

2: 7 bits

3: 8 bits

(R/W)

**UART\_STOP\_BIT\_NUM** Configures the number of stop bits.

0: Invalid. No effect

1: 1 bit

2: 1.5 bits

3: 2 bits

(R/W)

**UART\_TXD\_BRK** Configures whether or not to send NULL characters when finishing data transmission.

0: Not send

1: Send

(R/W)

**UART\_IRDA\_DPLX** Configures whether or not to enable IrDA loopback test.

0: Disable

1: Enable

(R/W)

**UART\_IRDA\_TX\_EN** Configures whether or not to enable the IrDA transmitter.

0: Disable

1: Enable

(R/W)

Continued on the next page...



**Register 37.9. UART\_CONFO\_SYNC\_REG (0x0020)**

Continued from the previous page...

**UART\_IRDA\_WCTL** Configures the 11th bit of the IrDA transmitter.

0: This bit is 0.

1: This bit is the same as the 10th bit.

(R/W)

**UART\_IRDA\_TX\_INV** Configures whether or not to invert the level of the IrDA transmitter.

0: Not invert

1: Invert

(R/W)

**UART\_IRDA\_RX\_INV** Configures whether or not to invert the level of the IrDA receiver.

0: Not invert

1: Invert

(R/W)

**UART\_LOOPBACK** Configures whether or not to enable UART loopback test.

0: Disable

1: Enable

(R/W)

**UART\_TX\_FLOW\_EN** Configures whether or not to enable flow control for the transmitter.

0: Disable

1: Enable

(R/W)

**UART\_IRDA\_EN** Configures whether or not to enable IrDA protocol.

0: Disable

1: Enable

(R/W)

**UART\_RXD\_INV** Configures whether or not to invert the level of UART RXD signal.

0: Not invert

1: Invert

(R/W)

**UART\_TXD\_INV** Configures whether or not to invert the level of UART TXD signal.

0: Not invert

1: Invert

(R/W)

**UART\_DIS\_RX\_DAT\_OVF** Configures whether or not to disable data overflow detection for the UART receiver.

0: Enable

1: Disable

(R/W)

Continued on the next page...

**Register 37.9. UART\_CONFO\_SYNC\_REG (0x0020)**

Continued from the previous page...

**UART\_ERR\_WR\_MASK** Configures whether or not to store the received data with errors into FIFO.

- 0: Store
  - 1: Not store
- (R/W)

**UART\_AUTOBAUD\_EN** Configures whether or not to enable baud rate detection.

- 0: Disable
  - 1: Enable
- (R/W)

**UART\_MEM\_CLK\_EN** Configures whether or not to enable clock gating for UART memory.

- 0: Disable
  - 1: Enable
- (R/W)

**UART\_SW\_RTS** Configures the RTS signal used in software flow control.

- 0: The UART transmitter is not allowed to send data.
  - 1: The UART transmitted is allowed to send data.
- (R/W)

**UART\_RXFIFO\_RST** Configures whether or not to reset the UART RX FIFO.

- 0: Not reset
  - 1: Reset
- (R/W)

**UART\_TXFIFO\_RST** Configures whether or not to reset the UART TX FIFO.

- 0: Not reset
  - 1: Reset
- (R/W)

**Register 37.10. UART\_CONF1\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |                         |    |    |  |  |  |  |  |                        |  |  |   |   |  |  |  |       |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|-------------------------|----|----|--|--|--|--|--|------------------------|--|--|---|---|--|--|--|-------|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   | UART_CLK_EN<br>UART_SW_DTR<br>UART_DTR_INV<br>UART_RTS_INV<br>UART_DSR_INV<br>UART_CTS_INV |    |    |    |    |    | UART_TXFIFO_EMPTY_THRHD |    |    |  |  |  |  |  | UART_RXFIFO_FULL_THRHD |  |  |   |   |  |  |  |       |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |  | 22 | 21 | 20 | 19 | 18 | 17                      | 16 | 15 |  |  |  |  |  |                        |  |  | 8 | 7 |  |  |  |       |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0x60                    |    |    |  |  |  |  |  | 0x60                   |  |  |   |   |  |  |  | Reset |  |  |  |  |   |

**UART\_RXFIFO\_FULL\_THRHD** Configures the threshold for RX FIFO being full.  
Measurement unit: byte. (R/W)

**UART\_TXFIFO\_EMPTY\_THRHD** Configures the threshold for TX FIFO being empty.  
Measurement unit: byte. (R/W)

**UART\_CTS\_INV** Configures whether or not to invert the level of UART CTS signal.  
0: Not invert  
1: Invert  
(R/W)

**UART\_DSR\_INV** Configures whether or not to invert the level of UART DSR signal.  
0: Not invert  
1: Invert  
(R/W)

**UART\_RTS\_INV** Configures whether or not to invert the level of UART RTS signal.  
0: Not invert  
1: Invert  
(R/W)

**UART\_DTR\_INV** Configures whether or not to invert the level of UART DTR signal.  
0: Not invert  
1: Invert  
(R/W)

**UART\_SW\_DTR** Configures the DTR signal used in software flow control.  
0: Data to be transmitted is not ready.  
1: Data to be transmitted is ready.  
(R/W)

**UART\_CLK\_EN** Configures clock gating.  
0: Support clock only when the application writes registers.  
1: Always force the clock on for registers.  
(R/W)

**Register 37.11. UART\_HWFC\_CONF\_SYNC\_REG (0x002C)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |     |                    |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|-----|--------------------|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_RX_FLOW_EN |     | UART_RX_FLOW_THRHD |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 | 8   | 7                  | 0     |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0               | 0x0 |                    | Reset |

**UART\_RX\_FLOW\_THRHD** Configures the maximum number of data bytes that can be received during hardware flow control.

Measurement unit: byte. (R/W)

**UART\_RX\_FLOW\_EN** Configures whether or not to enable the UART receiver.

0: Disable

1: Enable

(R/W)

**Register 37.12. UART\_SLEEP\_CONFO\_REG (0x0030)**

|               |  |  |  |  |  |  |  |               |    |  |  |  |  |  |  |               |    |    |  |  |  |  |  |               |  |   |   |  |  |  |  |       |  |  |   |
|---------------|--|--|--|--|--|--|--|---------------|----|--|--|--|--|--|--|---------------|----|----|--|--|--|--|--|---------------|--|---|---|--|--|--|--|-------|--|--|---|
| UART_WK_CHAR4 |  |  |  |  |  |  |  | UART_WK_CHAR3 |    |  |  |  |  |  |  | UART_WK_CHAR2 |    |    |  |  |  |  |  | UART_WK_CHAR1 |  |   |   |  |  |  |  |       |  |  |   |
| 31            |  |  |  |  |  |  |  | 24            | 23 |  |  |  |  |  |  |               | 16 | 15 |  |  |  |  |  |               |  | 8 | 7 |  |  |  |  |       |  |  | 0 |
| 0x0           |  |  |  |  |  |  |  | 0x0           |    |  |  |  |  |  |  | 0x0           |    |    |  |  |  |  |  | 0x0           |  |   |   |  |  |  |  | Reset |  |  |   |

**UART\_WK\_CHAR1** Configures wakeup character 1. (R/W)

**UART\_WK\_CHAR2** Configures wakeup character 2. (R/W)

**UART\_WK\_CHAR3** Configures wakeup character 3. (R/W)

**UART\_WK\_CHAR4** Configures wakeup character 4. (R/W)

**Register 37.13. UART\_SLEEP\_CONF1\_REG (0x0034)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  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|  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UART\_WK\_CHAR0** Configures wakeup character 0. (R/W)

**Register 37.14. UART\_SLEEP\_CONF2\_REG (0x0038)**

|            |    |    |    |                  |     |    |    |                   |     |   |   |                  |   |  |  |                       |      |  |  |                       |       |  |  |
|------------|----|----|----|------------------|-----|----|----|-------------------|-----|---|---|------------------|---|--|--|-----------------------|------|--|--|-----------------------|-------|--|--|
| (reserved) |    |    |    | UART_WK_MODE_SEL |     |    |    | UART_WK_CHAR_MASK |     |   |   | UART_WK_CHAR_NUM |   |  |  | UART_RX_WAKE_UP_THRHD |      |  |  | UART_ACTIVE_THRESHOLD |       |  |  |
| 31         | 28 | 27 | 26 | 25               | 21  | 20 | 18 | 17                | 10  | 9 | 0 |                  |   |  |  |                       |      |  |  |                       |       |  |  |
| 0          | 0  | 0  | 0  | 0                | 0x0 |    |    |                   | 0x5 |   |   |                  | 1 |  |  |                       | 0xf0 |  |  |                       | Reset |  |  |

**UART\_ACTIVE\_THRESHOLD** Configures the number of RXD edge changes to wake up the chip in wakeup mode 0. (R/W)

**UART\_RX\_WAKE\_UP\_THRHD** Configures the number of received data bytes to wake up the chip in wakeup mode 1. (R/W)

**UART\_WK\_CHAR\_NUM** Configures the number of wakeup characters. (R/W)

**UART\_WK\_CHAR\_MASK** Configures whether or not to mask wakeup characters.

0: Not mask

1: Mask

(R/W)

**UART\_WK\_MODE\_SEL** Configures which wakeup mode to select. See Section [37.4.8 Wakeup](#) for the explanation of each mode.

0: Mode 0

1: Mode 1

2: Mode 2

3: Mode 3

(R/W)

Register 37.15. UART\_SWFC\_CONFO\_SYNC\_REG (0x003C)

|            |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |                |  |    |  |               |  |    |  |                 |  |    |  |                |  |      |  |                 |  |  |  |                     |  |      |  |                          |  |   |  |                |  |       |  |  |  |  |  |               |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|----------------|--|----|--|---------------|--|----|--|-----------------|--|----|--|----------------|--|------|--|-----------------|--|--|--|---------------------|--|------|--|--------------------------|--|---|--|----------------|--|-------|--|--|--|--|--|---------------|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  | UART_SEND_XOFF |  |    |  | UART_SEND_XON |  |    |  | UART_FORCE_XOFF |  |    |  | UART_FORCE_XON |  |      |  | UART_XONOFF_DEL |  |  |  | UART_SW_FLOW_CON_EN |  |      |  | UART_XON_XOFF_STILL_SEND |  |   |  | UART_XOFF_CHAR |  |       |  |  |  |  |  | UART_XON_CHAR |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  | 22             |  | 21 |  | 20            |  | 19 |  | 18              |  | 17 |  | 16             |  | 15   |  | 8               |  |  |  |                     |  |      |  | 7                        |  | 0 |  |                |  |       |  |  |  |  |  |               |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0              |  | 0  |  | 0             |  | 0  |  | 0               |  | 0  |  | 0              |  | 0x13 |  |                 |  |  |  |                     |  | 0x11 |  |                          |  |   |  |                |  | Reset |  |  |  |  |  |               |  |  |  |  |  |  |  |

**UART\_XON\_CHAR** Configures the XON character for flow control. (R/W)

**UART\_XOFF\_CHAR** Configures the XOFF character for flow control. (R/W)

**UART\_XON\_XOFF\_STILL\_SEND** Configures whether the UART transmitter can send XON or XOFF characters when it is disabled.

0: Cannot send

1: Can send

(R/W)

**UART\_SW\_FLOW\_CON\_EN** Configures whether or not to enable software flow control.

0: Disable

1: Enable

(R/W)

**UART\_XONOFF\_DEL** Configures whether or not to remove flow control characters from the received data.

0: Not move

1: Move

(R/W)

**UART\_FORCE\_XON** Configures whether the transmitter continues to sending data.

0: Not send

1: Send

(R/W)

**UART\_FORCE\_XOFF** Configures whether or not to stop the transmitter from sending data.

0: Not stop

1: Stop

(R/W)

**UART\_SEND\_XON** Configures whether or not to send XON characters.

0: Not send

1: Send

(R/W/SS/SC)

**UART\_SEND\_XOFF** Configures whether or not to send XOFF characters.

0: Not send

1: Send

(R/W/SS/SC)

**Register 37.16. UART\_SWFC\_CONF1\_REG (0x0040)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |    |  |  |  |  |  |  |                    |   |   |  |  |  |  |  |       |  |   |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|----|--|--|--|--|--|--|--------------------|---|---|--|--|--|--|--|-------|--|---|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_XOFF_THRESHOLD |    |  |  |  |  |  |  | UART_XON_THRESHOLD |   |   |  |  |  |  |  |       |  |   |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                  | 15 |  |  |  |  |  |  |                    | 8 | 7 |  |  |  |  |  |       |  | 0 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0xe0                |    |  |  |  |  |  |  | 0x0                |   |   |  |  |  |  |  | Reset |  |   |

**UART\_XON\_THRESHOLD** Configures the threshold for data in RX FIFO to send XON characters in software flow control.

Measurement unit: byte. (R/W)

**UART\_XOFF\_THRESHOLD** Configures the threshold for data in RX FIFO to send XOFF characters in software flow control.

Measurement unit: byte. (R/W)

**Register 37.17. UART\_TXBRK\_CONF\_SYNC\_REG (0x0044)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_TX_BRK_NUM |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8               | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Oxa             |   |   |  |  |  |  |  | Reset |  |

**UART\_TX\_BRK\_NUM** Configures the number of NULL characters to be sent after finishing data transmission.

Valid only when UART\_TXD\_BRK is 1. (R/W)

**Register 37.18. UART\_IDLE\_CONF\_SYNC\_REG (0x0048)**

|                         |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
|-------------------------|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)              |  |  |  |  |  |  |  |  |  |  |  | UART_TX_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  | UART_RX_IDLE_THRHD |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |
| 31                      |  |  |  |  |  |  |  |  |  |  |  | 20               |  |  |  |  |  |  |  |  |  |  |  | 19                 |  |  |  |  |  |  |  |  |  |  |  | 10    |  |  |  |  |  |  |  |  |  |  |  | 9 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  | 0x100            |  |  |  |  |  |  |  |  |  |  |  | 0x100              |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |

**UART\_RX\_IDLE\_THRHD** Configures the threshold to generate a frame end signal when the receiver takes more time to receive one data byte data.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

**UART\_TX\_IDLE\_NUM** Configures the interval between two data transfers.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

Register 37.19. UART\_RS485\_CONF\_SYNC\_REG (0x004C)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  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 |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 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|  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |

Reset

**UART\_RS485\_EN** Configures whether or not to enable RS485 mode.

0: Disable

1: Enable

(R/W)

**UART\_DLO\_EN** Configures whether or not to add a turnaround delay of 1 bit before the start bit.

0: Not add

1: Add

(R/W)

**UART\_DL1\_EN** Configures whether or not to add a turnaround delay of 1 bit after the stop bit.

0: Not add

1: Add

(R/W)

**UART\_RS485TX\_RX\_EN** Configures whether or not to enable the receiver for data reception when the transmitter is transmitting data in RS485 mode.

0: Disable

1: Enable

(R/W)

**UART\_RS485RXBY\_TX\_EN** Configures whether to enable the RS485 transmitter for data transmission when the RS485 receiver is busy.

0: Disable

1: Enable

(R/W)

**UART\_RS485\_RX\_DLY\_NUM** Configures the delay of internal data signals in the receiver.

Measurement unit: bit time (the time to transmit 1 bit).. (R/W)

**UART\_RS485\_TX\_DLY\_NUM** Configures the delay of internal data signals in the transmitter.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)



Register 37.20. UART\_CLK\_CONF\_REG (0x0088)

|            |    |    |    |                  |    |    |   |                  |  |  |  |                 |  |  |  |                 |  |  |  |            |  |  |  |  |  |       |  |  |  |  |   |  |  |  |   |
|------------|----|----|----|------------------|----|----|---|------------------|--|--|--|-----------------|--|--|--|-----------------|--|--|--|------------|--|--|--|--|--|-------|--|--|--|--|---|--|--|--|---|
| (reserved) |    |    |    | UART_RX_RST_CORE |    |    |   | UART_TX_RST_CORE |  |  |  | UART_RX_SCLK_EN |  |  |  | UART_TX_SCLK_EN |  |  |  | (reserved) |  |  |  |  |  |       |  |  |  |  |   |  |  |  | 0 |
| 31         | 28 | 27 | 26 | 25               | 24 | 23 |   |                  |  |  |  |                 |  |  |  |                 |  |  |  |            |  |  |  |  |  |       |  |  |  |  | 0 |  |  |  |   |
| 0          | 0  | 0  | 0  | 0                | 0  | 1  | 1 | 0                |  |  |  |                 |  |  |  |                 |  |  |  |            |  |  |  |  |  | Reset |  |  |  |  |   |  |  |  |   |

Reset

**UART\_TX\_SCLK\_EN** Configures whether or not to enable UART TX clock.

0: Disable

1: Enable

(R/W)

**UART\_RX\_SCLK\_EN** Configures whether or not to enable UART RX clock.

0: Disable

1: Enable

(R/W)

**UART\_TX\_RST\_CORE** Write 1 and then write 0 to reset UART TX. (R/W)**UART\_RX\_RST\_CORE** Write 1 and then write 0 to reset UART RX. (R/W)

Register 37.21. UART\_STATUS\_REG (0x001C)

|          |    |    |    |           |   |   |   |           |    |  |  |            |    |    |    |                 |   |   |   |          |   |   |  |           |       |  |  |           |  |  |  |            |  |  |  |                 |  |  |  |
|----------|----|----|----|-----------|---|---|---|-----------|----|--|--|------------|----|----|----|-----------------|---|---|---|----------|---|---|--|-----------|-------|--|--|-----------|--|--|--|------------|--|--|--|-----------------|--|--|--|
| UART_TXD |    |    |    | UART_RTSN |   |   |   | UART_DTRN |    |  |  | (reserved) |    |    |    | UART_TXFIFO_CNT |   |   |   | UART_RXD |   |   |  | UART_CTSN |       |  |  | UART_DSRN |  |  |  | (reserved) |  |  |  | UART_RXFIFO_CNT |  |  |  |
| 31       | 30 | 29 | 28 | 24        |   |   |   | 23        | 16 |  |  |            | 15 | 14 | 13 | 12              | 8 |   |   |          | 7 | 0 |  |           |       |  |  |           |  |  |  |            |  |  |  |                 |  |  |  |
| 1        | 1  | 1  | 0  | 0         | 0 | 0 | 0 | 0         |    |  |  | 1          | 1  | 0  | 0  | 0               | 0 | 0 | 0 | 0        | 0 |   |  |           | Reset |  |  |           |  |  |  |            |  |  |  |                 |  |  |  |

Reset

**UART\_RXFIFO\_CNT** Represents the number of valid data bytes in RX FIFO. (RO)**UART\_DSRN** Represents the level of the internal UART DSR signal. (RO)**UART\_CTSN** Represents the level of the internal UART CTS signal. (RO)**UART\_RXD** Represents the level of the internal UART RXD signal. (RO)**UART\_TXFIFO\_CNT** Represents the number of valid data bytes in RX FIFO. (RO)**UART\_DTRN** Represents the level of the internal UART DTR signal. (RO)**UART\_RTSN** Represents the level of the internal UART RTS signal. (RO)**UART\_TXD** Represents the level of the internal UART TXD signal. (RO)

**Register 37.22. UART\_MEM\_TX\_STATUS\_REG (0x0068)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |            |  |  |  |  |  |  |                    |  |  |  |  |  |  |       |   |  |  |  |  |  |  |   |  |  |  |  |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|------------|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|-------|---|--|--|--|--|--|--|---|--|--|--|--|--|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_TX_SRAM_RADDR |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  | UART_TX_SRAM_WADDR |  |  |  |  |  |  |       |   |  |  |  |  |  |  |   |  |  |  |  |  |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                 |  |  |  |  |  |  | 16         |  |  |  |  |  |  | 9                  |  |  |  |  |  |  | 8     | 7 |  |  |  |  |  |  | 0 |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0                |  |  |  |  |  |  | 0          |  |  |  |  |  |  | 0x0                |  |  |  |  |  |  | Reset |   |  |  |  |  |  |  |   |  |  |  |  |  |  |

Reset

**UART\_TX\_SRAM\_WADDR** Represents the offset address to write TX FIFO. (RO)**UART\_TX\_SRAM\_RADDR** Represents the offset address to read TX FIFO. (RO)**Register 37.23. UART\_MEM\_RX\_STATUS\_REG (0x006C)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_RX_SRAM_WADDR |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  | UART_RX_SRAM_RADDR |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                 |  |  |  |  |  |  |  | 16         |  |  |  |  |  |  |  | 9                  |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x80               |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  | 0x80               |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

Reset

**UART\_RX\_SRAM\_RADDR** Represents the offset address to read RX FIFO. (RO)**UART\_RX\_SRAM\_WADDR** Represents the offset address to write RX FIFO. (RO)**Register 37.24. UART\_FSM\_STATUS\_REG (0x0070)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                 |   |                 |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------|---|-----------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UART_ST_UTX_OUT |   | UART_ST_URX_OUT |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8 | 7               | 4 | 3               | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0               |   | 0               |   |

Reset

**UART\_ST\_URX\_OUT** Represents the status of the receiver. (RO)**UART\_ST\_UTX\_OUT** Represents the status of the transmitter. (RO)

**Register 37.25. UART\_AFIFO\_STATUS\_REG (0x0090)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UART_RX_AFIFO_EMPTY<br>UART_RX_AFIFO_FULL<br>UART_TX_AFIFO_EMPTY<br>UART_TX_AFIFO_FULL |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0  | 1 | 0 | Reset |   |

**UART\_TX\_AFIFO\_FULL** Represents whether or not the APB TX asynchronous FIFO is full.

0: Not full

1: Full

(RO)

**UART\_TX\_AFIFO\_EMPTY** Represents whether or not the APB TX asynchronous FIFO is empty.

0: Not empty

1: Empty

(RO)

**UART\_RX\_AFIFO\_FULL** Represents whether or not the APB RX asynchronous FIFO is full.

0: Not full

1: Full

(RO)

**UART\_RX\_AFIFO\_EMPTY** Represents whether or not the APB RX asynchronous FIFO is empty.

0: Not empty

1: Empty

(RO)

**Register 37.26. UART\_AT\_CMD\_PRECNT\_SYNC\_REG (0x0050)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_PRE_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x901             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UART\_PRE\_IDLE\_NUM** Configures the idle time before the receiver receives the first AT\_CMD.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

### Register 37.27. UART\_AT\_CMD\_POSTCNT\_SYNC\_REG (0x0054)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_POST_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x901              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UART\_POST\_IDLE\_NUM** Configures the interval between the last AT\_CMD and subsequent data.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)

Register 37.28. UART\_AT\_CMD\_GAPTOUT\_SYNC\_REG (0x0058)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_RX_GAP_TOUT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 16                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UART\_RX\_GAP\_TOUT** Configures the interval between two AT\_CMD characters.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)

### Register 37.29. UART\_AT\_CMD\_CHAR\_SYNC\_REG (0x005C)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_CHAR_NUM |  |  |  |  |  |  |  | UART_AT_CMD_CHAR |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15            |  |  |  |  |  |  |  | 7                |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x3           |  |  |  |  |  |  |  | 0x2b             |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**UART\_AT\_CMD\_CHAR** Configures the AT\_CMD character. (R/W)

**UART\_CHAR\_NUM** Configures the number of continuous AT\_CMD characters a receiver can receive.  
(R/W)

**Register 37.30. UART\_POSPULSE\_REG (0x0074)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_POSEDGE_MIN_CNT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0xffff               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UART\_POSEDGE\_MIN\_CNT** Represents the minimal input clock counter value between two positive edges. It is used for baud rate detection. (RO)

**Register 37.31. UART\_NEGPULSE\_REG (0x0078)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UART_NEGEDGE_MIN_CNT |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11                   |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0fff                 |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |

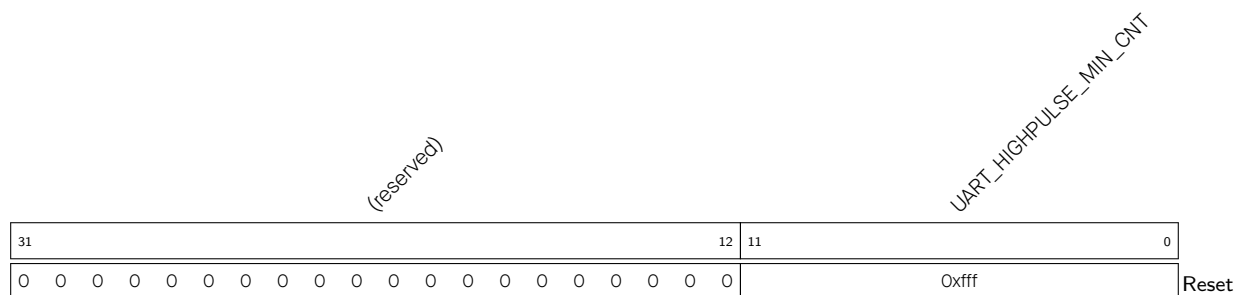
**UART\_NEGEDGE\_MIN\_CNT** Represents the minimal input clock counter value between two negative edges. It is used for baud rate detection. (RO)

**Register 37.32. UART\_LOWPULSE\_REG (0x007C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   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 |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  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|  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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|  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

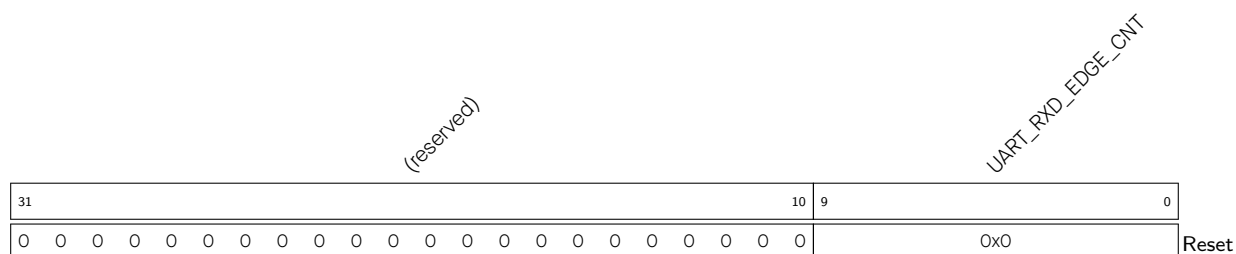
**UART\_LOWPULSE\_MIN\_CNT** Represents the minimum duration time of a low-level pulse. It is used for baud rate detection.

Measurement unit: APB\_CLK clock cycle. (RO)

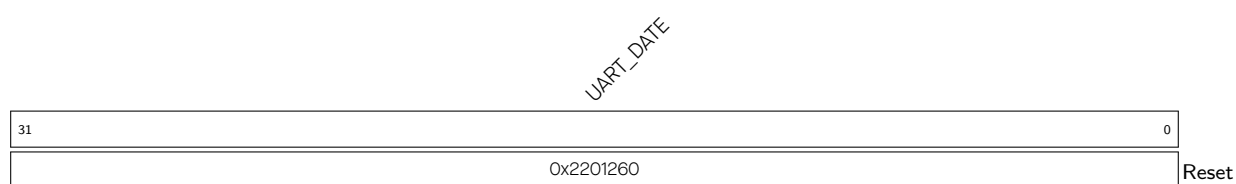
**Register 37.33. UART\_HIGHPULSE\_REG (0x0080)**

**UART\_HIGHPULSE\_MIN\_CNT** Represents the maximum duration time for a high-level pulse. It is used for baud rate detection.

Measurement unit: APB\_CLK clock cycle. (RO)

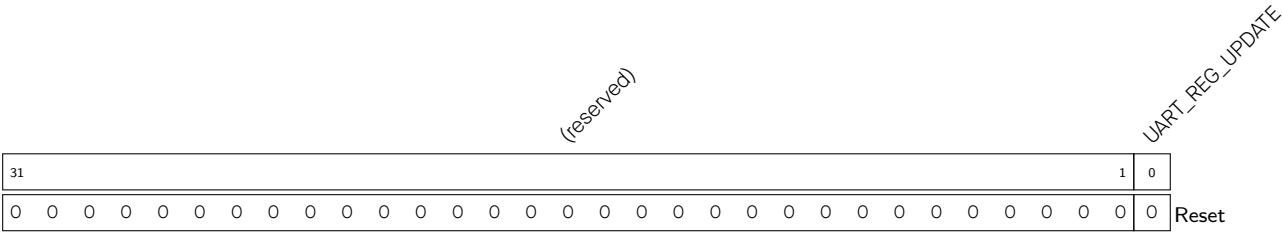
**Register 37.34. UART\_RXD\_CNT\_REG (0x0084)**

**UART\_RXD\_EDGE\_CNT** Represents the number of RXD edge changes. It is used for baud rate detection. (RO)

**Register 37.35. UART\_DATE\_REG (0x008C)**

**UART\_DATE** Version control register. (R/W)

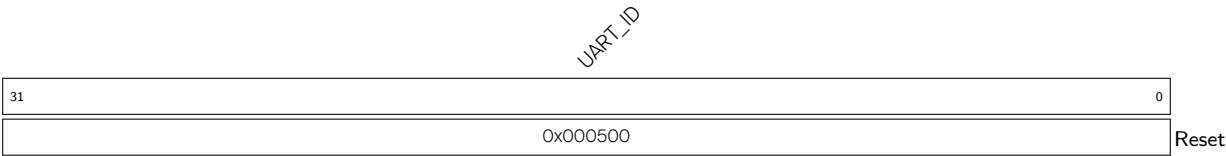
Register 37.36. UART\_REG\_UPDATE\_REG (0x0098)



**UART\_REG\_UPDATE** Configures whether or not to synchronize registers.

- 0: Not synchronize
- 1: Synchronize (R/W/SC)

Register 37.37. UART\_ID\_REG (0x009C)



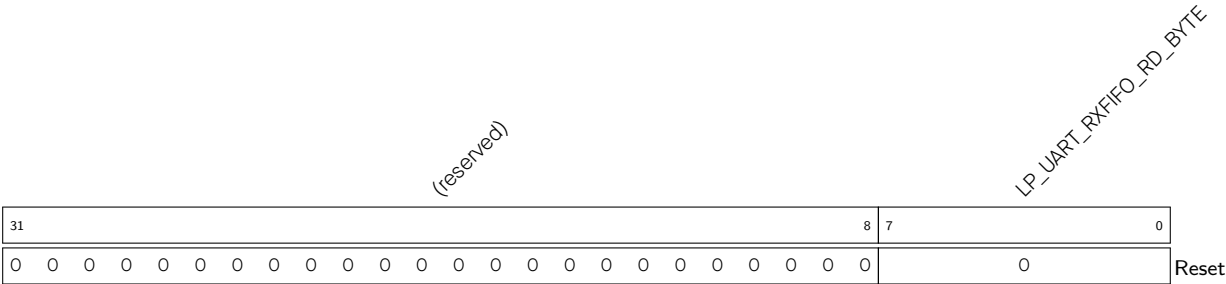
**UART\_ID** Configures the UART ID. (R/W)

### 37.7.2  LP UART Registers

The addresses in this section are relative to LP UART base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

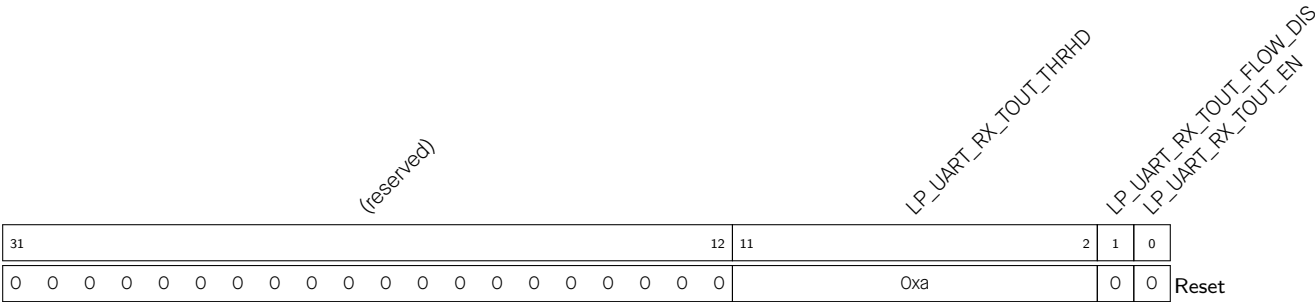
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 37.38. LP\_UART\_FIFO\_REG (0x0000)



**LP\_UART\_RXFIFO\_RD\_BYTE** Represents the data LP UART *n* read from FIFO.  
Measurement unit: byte. (RO)

Register 37.39. LP\_UART\_TOUT\_CONF\_SYNC\_REG (0x0064)



**LP\_UART\_RX\_TOUT\_EN** Configures whether or not to enable LP UART receiver’s timeout function.  
0: Disable  
1: Enable  
(R/W)

**LP\_UART\_RX\_TOUT\_FLOW\_DIS** Configures whether or not to disable the idle status counter when hardware flow control is enabled.  
0: Invalid. No effect  
1: Disable  
(R/W)

**LP\_UART\_RX\_TOUT\_THRHD** Configures the amount of time that the bus can remain idle before time-out.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)



## Register 37.40. LP\_UART\_INT\_RAW\_REG (0x0004)

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |   |                                 |    |            |   |    |   |    |    |    |    |    |   |   |   |   |   |   |   |                         |   |                                  |   |                             |  |                            |  |                         |  |                        |  |                             |  |                         |  |                         |  |                         |  |                            |  |                         |  |                           |  |                              |  |                             |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|---|---------------------------------|----|------------|---|----|---|----|----|----|----|----|---|---|---|---|---|---|---|-------------------------|---|----------------------------------|---|-----------------------------|--|----------------------------|--|-------------------------|--|------------------------|--|-----------------------------|--|-------------------------|--|-------------------------|--|-------------------------|--|----------------------------|--|-------------------------|--|---------------------------|--|------------------------------|--|-----------------------------|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_WAKEUP_INT_RAW |   | LP_UART_AT_CMD_CHAR_DET_INT_RAW |    | (reserved) |   |    |   |    |    |    |    |    |   |   |   |   |   |   |   | LP_UART_TX_DONE_INT_RAW |   | LP_UART_TX_BRK_IDLE_DONE_INT_RAW |   | LP_UART_TX_BRK_DONE_INT_RAW |  | LP_UART_GLITCH_DET_INT_RAW |  | LP_UART_SW_XOFF_INT_RAW |  | LP_UART_SW_XON_INT_RAW |  | LP_UART_RXFIFO_TOUT_INT_RAW |  | LP_UART_BRK_DET_INT_RAW |  | LP_UART_CTS_CHG_INT_RAW |  | LP_UART_DSR_CHG_INT_RAW |  | LP_UART_RXFIFO_OVF_INT_RAW |  | LP_UART_FRM_ERR_INT_RAW |  | LP_UART_PARTY_ERR_INT_RAW |  | LP_UART_TXFIFO_EMPTY_INT_RAW |  | LP_UART_RXFIFO_FULL_INT_RAW |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 20                     |   | 19                              | 18 | 17         |   | 15 |   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2                       | 1 | 0                                |   |                             |  |                            |  |                         |  |                        |  |                             |  |                         |  |                         |  |                         |  |                            |  |                         |  |                           |  |                              |  |                             |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                      | 0 | 0                               | 0  | 0          | 0 | 0  | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 1                                | 0 | Reset                       |  |                            |  |                         |  |                        |  |                             |  |                         |  |                         |  |                         |  |                            |  |                         |  |                           |  |                              |  |                             |  |

**LP\_UART\_RXFIFO\_FULL\_INT\_RAW** The raw interrupt status of LP\_UART\_RXFIFO\_FULL\_INT. (R/WTC/SS)

**LP\_UART\_TXFIFO\_EMPTY\_INT\_RAW** The raw interrupt status of LP\_UART\_TXFIFO\_EMPTY\_INT. (R/WTC/SS)

**LP\_UART\_PARITY\_ERR\_INT\_RAW** The raw interrupt status of LP\_UART\_PARITY\_ERR\_INT. (R/WTC/SS)

**LP\_UART\_FRM\_ERR\_INT\_RAW** The raw interrupt status of LP\_UART\_FRM\_ERR\_INT. (R/WTC/SS)

**LP\_UART\_RXFIFO\_OVF\_INT\_RAW** The raw interrupt status of LP\_UART\_RXFIFO\_OVF\_INT. (R/WTC/SS)

**LP\_UART\_DSR\_CHG\_INT\_RAW** The raw interrupt status of LP\_UART\_DSR\_CHG\_INT. (R/WTC/SS)

**LP\_UART\_CTS\_CHG\_INT\_RAW** The raw interrupt status of LP\_UART\_CTS\_CHG\_INT. (R/WTC/SS)

**LP\_UART\_BRK\_DET\_INT\_RAW** The raw interrupt status of LP\_UART\_BRK\_DET\_INT. (R/WTC/SS)

**LP\_UART\_RXFIFO\_TOUT\_INT\_RAW** The raw interrupt status of LP\_UART\_RXFIFO\_TOUT\_INT. (R/WTC/SS)

**LP\_UART\_SW\_XON\_INT\_RAW** The raw interrupt status of LP\_UART\_SW\_XON\_INT. (R/WTC/SS)

**LP\_UART\_SW\_XOFF\_INT\_RAW** LP\_UART\_SW\_XOFF\_INT. (R/WTC/SS)

**LP\_UART\_GLITCH\_DET\_INT\_RAW** The raw interrupt status of LP\_UART\_GLITCH\_DET\_INT. (R/WTC/SS)

**LP\_UART\_TX\_BRK\_DONE\_INT\_RAW** The raw interrupt status of LP\_UART\_TX\_BRK\_DONE\_INT. (R/WTC/SS)

**LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT\_RAW** The raw interrupt status of LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT. (R/WTC/SS)

Continued on the next page...

**Register 37.40. LP\_UART\_INT\_RAW\_REG (0x0004)**

Continued from the previous page...

**LP\_UART\_TX\_DONE\_INT\_RAW** The raw interrupt status of LP\_UART\_TX\_DONE\_INT. (R/WTC/SS)

**LP\_UART\_AT\_CMD\_CHAR\_DET\_INT\_RAW** The raw interrupt status of LP\_UART\_AT\_CMD\_CHAR\_DET\_INT. (R/WTC/SS)

**LP\_UART\_WAKEUP\_INT\_RAW** The raw interrupt status of LP\_UART\_WAKEUP\_INT. (R/WTC/SS)

Register 37.41. LP\_UART\_INT\_ST\_REG (0x0008)

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |   |    |   |    |    |    |    |    |   |   |   |   |       |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|---|----|---|----|----|----|----|----|---|---|---|---|-------|---|---|---|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | LP_UART_WAKEUP_INT_ST<br>LP_UART_AT_CMD_CHAR_DET_INT_ST<br>(reserved) |    |   |    |    |    |    |    |   |   |   |   |       |   |   |   | LP_UART_TX_DONE_INT_ST<br>LP_UART_TX_BRK_IDLE_DONE_INT_ST<br>LP_UART_TX_BRK_GLITCH_DET_INT_ST<br>LP_UART_SW_XON_INT_ST<br>LP_UART_SW_XOFF_INT_ST<br>LP_UART_BRK_DET_INT_ST<br>LP_UART_CTS_CHG_INT_ST<br>LP_UART_DSR_CHG_INT_ST<br>LP_UART_RXFIFO_OVF_INT_ST<br>LP_UART_FRM_ERR_INT_ST<br>LP_UART_PARITY_ERR_INT_ST<br>LP_UART_TXFIFO_EMPTY_INT_ST<br>LP_UART_RXFIFO_FULL_INT_ST |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17  | 15 |   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5     | 4 | 3 | 2 | 1   | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0   | 0  | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | Reset |   |   |   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_UART\_RXFIFO\_FULL\_INT\_ST** The masked interrupt status of LP\_UART\_RXFIFO\_FULL\_INT. (RO)

**LP\_UART\_TXFIFO\_EMPTY\_INT\_ST** The masked interrupt status of LP\_UART\_TXFIFO\_EMPTY\_INT. (RO)

**LP\_UART\_PARITY\_ERR\_INT\_ST** The masked interrupt status of LP\_UART\_PARITY\_ERR\_INT. (RO)

**LP\_UART\_FRM\_ERR\_INT\_ST** The masked interrupt status of LP\_UART\_FRM\_ERR\_INT. (RO)

**LP\_UART\_RXFIFO\_OVF\_INT\_ST** The masked interrupt status of LP\_UART\_RXFIFO\_OVF\_INT. (RO)

**LP\_UART\_DSR\_CHG\_INT\_ST** The masked interrupt status of LP\_UART\_DSR\_CHG\_INT. (RO)

**LP\_UART\_CTS\_CHG\_INT\_ST** The masked interrupt status of LP\_UART\_CTS\_CHG\_INT. (RO)

**LP\_UART\_BRK\_DET\_INT\_ST** The masked interrupt status of LP\_UART\_BRK\_DET\_INT. (RO)

**LP\_UART\_RXFIFO\_TOUT\_INT\_ST** The masked interrupt status of LP\_UART\_RXFIFO\_TOUT\_INT. (RO)

**LP\_UART\_SW\_XON\_INT\_ST** The masked interrupt status of LP\_UART\_SW\_XON\_INT. (RO)

**LP\_UART\_SW\_XOFF\_INT\_ST** The masked interrupt status of LP\_UART\_SW\_XOFF\_INT. (RO)

**LP\_UART\_GLITCH\_DET\_INT\_ST** The masked interrupt status of LP\_UART\_GLITCH\_DET\_INT. (RO)

**LP\_UART\_TX\_BRK\_DONE\_INT\_ST** The masked interrupt status of LP\_UART\_TX\_BRK\_DONE\_INT. (RO)

**LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT\_ST** The masked interrupt status of LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT. (RO)

**LP\_UART\_TX\_DONE\_INT\_ST** The masked interrupt status of LP\_UART\_TX\_DONE\_INT. (RO)

**LP\_UART\_AT\_CMD\_CHAR\_DET\_INT\_ST** The masked interrupt status of LP\_UART\_AT\_CMD\_CHAR\_DET\_INT. (RO)

**LP\_UART\_WAKEUP\_INT\_ST** The masked interrupt status of LP\_UART\_WAKEUP\_INT. (RO)

**Register 37.42. LP\_UART\_INT\_ENA\_REG (0x000C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |   |    |   |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|---|----|---|----|----|----|----|----|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | LP_UART_WAKEUP_INT_ENA<br>LP_UART_AT_CMD_CHAR_DET_INT_ENA<br>(reserved)<br>LP_UART_TX_DONE_INT_ENA<br>LP_UART_TX_BRK_IDLE_DONE_INT_ENA<br>LP_UART_TX_BRK_DONE_INT_ENA<br>LP_UART_GLITCH_DET_INT_ENA<br>LP_UART_SW_XON_INT_ENA<br>LP_UART_SW_XOFF_INT_ENA<br>LP_UART_RXFIFO_TOUT_INT_ENA<br>LP_UART_BRK_DET_INT_ENA<br>LP_UART_CTS_CHG_INT_ENA<br>LP_UART_DSR_CHG_INT_ENA<br>LP_UART_RXFIFO_OVF_INT_ENA<br>LP_UART_FRM_ERR_INT_ENA<br>LP_UART_PARITY_ERR_INT_ENA<br>LP_UART_TXFIFO_EMPTY_INT_ENA |    |   |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17  | 15 |   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0   | 0  | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | Reset |   |   |   |   |

**LP\_UART\_RXFIFO\_FULL\_INT\_ENA** Write 1 to enable LP\_UART\_RXFIFO\_FULL\_INT. (R/W)

**LP\_UART\_TXFIFO\_EMPTY\_INT\_ENA** Write 1 to enable LP\_UART\_TXFIFO\_EMPTY\_INT. (R/W)

**LP\_UART\_PARITY\_ERR\_INT\_ENA** Write 1 to enable LP\_UART\_PARITY\_ERR\_INT. (R/W)

**LP\_UART\_FRM\_ERR\_INT\_ENA** Write 1 to enable LP\_UART\_FRM\_ERR\_INT. (R/W)

**LP\_UART\_RXFIFO\_OVF\_INT\_ENA** Write 1 to enable LP\_UART\_RXFIFO\_OVF\_INT. (R/W)

**LP\_UART\_DSR\_CHG\_INT\_ENA** Write 1 to enable LP\_UART\_DSR\_CHG\_INT. (R/W)

**LP\_UART\_CTS\_CHG\_INT\_ENA** Write 1 to enable LP\_UART\_CTS\_CHG\_INT. (R/W)

**LP\_UART\_BRK\_DET\_INT\_ENA** Write 1 to enable LP\_UART\_BRK\_DET\_INT. (R/W)

**LP\_UART\_RXFIFO\_TOUT\_INT\_ENA** Write 1 to enable LP\_UART\_RXFIFO\_TOUT\_INT. (R/W)

**LP\_UART\_SW\_XON\_INT\_ENA** Write 1 to enable LP\_UART\_SW\_XON\_INT. (R/W)

**LP\_UART\_SW\_XOFF\_INT\_ENA** Write 1 to enable LP\_UART\_SW\_XOFF\_INT. (R/W)

**LP\_UART\_GLITCH\_DET\_INT\_ENA** Write 1 to enable LP\_UART\_GLITCH\_DET\_INT. (R/W)

**LP\_UART\_TX\_BRK\_DONE\_INT\_ENA** Write 1 to enable LP\_UART\_TX\_BRK\_DONE\_INT. (R/W)

**LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT\_ENA** Write 1 to enable LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT. (R/W)

**LP\_UART\_TX\_DONE\_INT\_ENA** Write 1 to enable LP\_UART\_TX\_DONE\_INT. (R/W)

**LP\_UART\_AT\_CMD\_CHAR\_DET\_INT\_ENA** Write 1 to enable LP\_UART\_AT\_CMD\_CHAR\_DET\_INT. (R/W)

**LP\_UART\_WAKEUP\_INT\_ENA** Write 1 to enable LP\_UART\_WAKEUP\_INT. (R/W)

**Register 37.43. LP\_UART\_INT\_CLR\_REG (0x0010)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |  |    |   |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|--|----|---|----|----|----|----|----|---|---|---|---|---|-------|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    | LP_UART_WAKEUP_INT_CLR<br>LP_UART_AT_CMD_CHAR_DET_INT_CLR<br>(reserved)<br>LP_UART_TX_DONE_INT_CLR<br>LP_UART_TX_BRK_IDLE_DONE_INT_CLR<br>LP_UART_TX_BRK_DONE_INT_CLR<br>LP_UART_GLITCH_DET_INT_CLR<br>LP_UART_SW_XOFF_INT_CLR<br>LP_UART_SW_XON_INT_CLR<br>LP_UART_RXFIFO_TOUT_INT_CLR<br>LP_UART_BRK_DET_INT_CLR<br>LP_UART_CTS_CHG_INT_CLR<br>LP_UART_DSR_CHG_INT_CLR<br>LP_UART_RXFIFO_OVF_INT_CLR<br>LP_UART_FRM_ERR_INT_CLR<br>LP_UART_PARITY_ERR_INT_CLR<br>LP_UART_TXFIFO_EMPTY_INT_CLR<br>LP_UART_RXFIFO_FULL_INT_CLR |    |   |    |    |    |    |    |   |   |   |   |   |       |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 20 | 19 | 18 | 17   | 15 |   | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4     | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | Reset |   |   |   |   |

**LP\_UART\_RXFIFO\_FULL\_INT\_CLR** Write 1 to clear LP\_UART\_RXFIFO\_FULL\_INT. (WT)

**LP\_UART\_TXFIFO\_EMPTY\_INT\_CLR** Write 1 to clear LP\_UART\_TXFIFO\_EMPTY\_INT. (WT)

**LP\_UART\_PARITY\_ERR\_INT\_CLR** Write 1 to clear LP\_UART\_PARITY\_ERR\_INT. (WT)

**LP\_UART\_FRM\_ERR\_INT\_CLR** Write 1 to clear LP\_UART\_FRM\_ERR\_INT. (WT)

**LP\_UART\_RXFIFO\_OVF\_INT\_CLR** Write 1 to clear LP\_UART\_RXFIFO\_OVF\_INT. (WT)

**LP\_UART\_DSR\_CHG\_INT\_CLR** Write 1 to clear LP\_UART\_DSR\_CHG\_INT. (WT)

**LP\_UART\_CTS\_CHG\_INT\_CLR** Write 1 to clear LP\_UART\_CTS\_CHG\_INT. (WT)

**LP\_UART\_BRK\_DET\_INT\_CLR** Write 1 to clear LP\_UART\_BRK\_DET\_INT. (WT)

**LP\_UART\_RXFIFO\_TOUT\_INT\_CLR** Write 1 to clear LP\_UART\_RXFIFO\_TOUT\_INT. (WT)

**LP\_UART\_SW\_XON\_INT\_CLR** Write 1 to clear LP\_UART\_SW\_XON\_INT. (WT)

**LP\_UART\_SW\_XOFF\_INT\_CLR** Write 1 to clear LP\_UART\_SW\_XOFF\_INT. (WT)

**LP\_UART\_GLITCH\_DET\_INT\_CLR** Write 1 to clear LP\_UART\_GLITCH\_DET\_INT. (WT)

**LP\_UART\_TX\_BRK\_DONE\_INT\_CLR** Write 1 to clear LP\_UART\_TX\_BRK\_DONE\_INT. (WT)

**LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT\_CLR** Write 1 to clear LP\_UART\_TX\_BRK\_IDLE\_DONE\_INT. (WT)

**LP\_UART\_TX\_DONE\_INT\_CLR** Write 1 to clear LP\_UART\_TX\_DONE\_INT. (WT)

**LP\_UART\_AT\_CMD\_CHAR\_DET\_INT\_CLR** Write 1 to clear LP\_UART\_AT\_CMD\_CHAR\_DET\_INT. (WT)

**LP\_UART\_WAKEUP\_INT\_CLR** Write 1 to clear LP\_UART\_WAKEUP\_INT. (WT)

**Register 37.44. LP\_UART\_CLKDIV\_SYNC\_REG (0x0014)**

|            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |    |  |  |  |            |  |  |  |    |  |  |  |                |  |  |  |  |  |  |  |    |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |       |  |  |  |
|------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|----|--|--|--|------------|--|--|--|----|--|--|--|----------------|--|--|--|--|--|--|--|----|--|--|--|---|--|--|--|-------|--|--|--|--|--|--|--|-------|--|--|--|
| (reserved) |  |  |  |  |  |  |  | LP_UART_CLKDIV_FRAG |  |  |  |  |  |  |  |    |  |  |  | (reserved) |  |  |  |    |  |  |  | LP_UART_CLKDIV |  |  |  |  |  |  |  |    |  |  |  |   |  |  |  |       |  |  |  |  |  |  |  |       |  |  |  |
| 31         |  |  |  |  |  |  |  | 24                  |  |  |  |  |  |  |  | 23 |  |  |  | 20         |  |  |  | 19 |  |  |  | 12             |  |  |  |  |  |  |  | 11 |  |  |  | 0 |  |  |  |       |  |  |  |  |  |  |  |       |  |  |  |
| 0          |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0  |  |  |  | 0          |  |  |  | 0  |  |  |  | 0x0            |  |  |  |  |  |  |  | 0  |  |  |  | 0 |  |  |  | 0x2b6 |  |  |  |  |  |  |  | Reset |  |  |  |

**LP\_UART\_CLKDIV** Configures the integral part of the divisor for baud rate generation. (R/W)

**LP\_UART\_CLKDIV\_FRAG** Configures the fractional part of the divisor for baud rate generation. (R/W)

**Register 37.45. LP\_UART\_RX\_FILT\_REG (0x0018)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |     |                     |   |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|-----|---------------------|---|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_GLITCH_FILT_EN |     | LP_UART_GLITCH_FILT |   |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                      | 8   | 7                   | 0 |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                      | 0x8 |                     |   |  |  |  |  |  |  |  | Reset |  |

**LP\_UART\_GLITCH\_FILT** Configures the width of a pulse to be filtered.

Measurement unit: UART Core's clock cycle.

Pulses whose width is lower than this value will be ignored. (R/W)

**LP\_UART\_GLITCH\_FILT\_EN** Configures whether or not to enable RX signal filter.

0: Disable

1: Enable

(R/W)

**Register 37.46. LP\_UART\_CONFO\_SYNC\_REG (0x0020)**

|            |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |    |    |    |    |    |            |  |  |  |  |  |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|----|----|----|----|----|------------|--|--|--|--|--|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   | LP_UART_TXFIFO_RST<br>LP_UART_RXFIFO_RST<br>LP_UART_SW_RST<br>LP_UART_MEM_CLK_EN<br>(reserved)<br>LP_UART_ERR_WD_MASK<br>LP_UART_DS_RX_DAT_OVF<br>LP_UART_TXD_INV<br>(reserved)<br>LP_UART_RXD_INV<br>LP_UART_TX_FLOW_EN<br>LP_UART_LOOPBACK |    |    |    |    |    |    |    |    |    |    |    |    |    | (reserved) |  |  |  |  |  |   |   | LP_UART_TXD_BRK<br>LP_UART_STOP_BIT_NUM<br>LP_UART_BIT_NUM<br>LP_UART_PARITY_EN<br>LP_UART_PARITY |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   | 24   | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 |            |  |  |  |  |  | 7 | 6 | 5   | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          |  |  |  |  |  | 0 | 0 | 1   | 3 | 0 | 0 | Reset |   |

**LP\_UART\_PARITY** Configures the parity check mode.

0: Even parity

1: Odd parity

(R/W)

**LP\_UART\_PARITY\_EN** Configures whether or not to enable LP UART parity check.

0: Disable

1: Enable

(R/W)

**LP\_UART\_BIT\_NUM** Configures the number of data bits.

0: 5 bits

1: 6 bits

2: 7 bits

3: 8 bits

(R/W)

**LP\_UART\_STOP\_BIT\_NUM** Configures the number of stop bits.

0: Invalid. No effect

1: 1 bit

2: 1.5 bits

3: 2 bits

(R/W)

**LP\_UART\_TXD\_BRK** Configures whether or not to send NULL characters when finishing data transmission.

0: Not send

1: Send

(R/W)

**LP\_UART\_LOOPBACK** Configures whether or not to enable LP UART loopback test.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 37.46. LP\_UART\_CONFO\_SYNC\_REG (0x0020)**

Continued from the previous page...

**LP\_UART\_TX\_FLOW\_EN** Configures whether or not to enable flow control for the transmitter.

0: Disable

1: Enable

(R/W)

**LP\_UART\_RXD\_INV** Configures whether or not to invert the level of LP UART RXD signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_TXD\_INV** Configures whether or not to invert the level of LP UART TXD signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_DIS\_RX\_DAT\_OVF** Configures whether or not to disable data overflow detection for the LP UART receiver.

0: Enable

1: Disable

(R/W)

**LP\_UART\_ERR\_WR\_MASK** Configures whether or not to store the received data with errors into FIFO.

0: Store

1: Not store

(R/W)

**LP\_UART\_MEM\_CLK\_EN** Configures whether or not to enable clock gating for LP UART memory.

0: Disable

1: Enable

(R/W)

**LP\_UART\_SW\_RTS** Configures the RTS signal used in software flow control.

0: The LP UART transmitter is not allowed to send data.

1: The LP UART transmitted is allowed to send data.

(R/W)

**LP\_UART\_RXFIFO\_RST** Configures whether or not to reset the LP UART RX FIFO.

0: Not reset

1: Reset

(R/W)

**LP\_UART\_TXFIFO\_RST** Configures whether or not to reset the LP UART TX FIFO.

0: Not reset

1: Reset

(R/W)



**Register 37.47. LP\_UART\_CONF1\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |   |   |                |    |    |    |                |     |    |    |                 |  |   |   |                 |    |     |  |                 |   |  |   |                 |   |   |   |                            |  |   |  |            |  |  |  |                           |  |  |  |            |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|----------------|----|----|----|----------------|-----|----|----|-----------------|--|---|---|-----------------|----|-----|--|-----------------|---|--|---|-----------------|---|---|---|----------------------------|--|---|--|------------|--|--|--|---------------------------|--|--|--|------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | LP_UART_CLK_EN |    |    |    | LP_UART_SW_DTR |     |    |    | LP_UART_DTR_INV |  |   |   | LP_UART_RTS_INV |    |     |  | LP_UART_DSR_INV |   |  |   | LP_UART_CTS_INV |   |   |   | LP_UART_TXFIFO_EMPTY_THRHD |  |   |  | (reserved) |  |  |  | LP_UART_RXFIFO_FULL_THRHD |  |  |  | (reserved) |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 22             | 21 | 20 | 19 | 18             | 17  | 16 | 15 |                 |  |   |   | 11              | 10 |     |  | 8               | 7 |  |   |                 |   | 3 | 2 |                            |  | 0 |  |            |  |  |  |                           |  |  |  |            |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0  | 0  | 0  | 0              | 0xc |    |    |                 |  | 0 | 0 | 0               | 0  | 0xc |  |                 |   |  | 0 | 0               | 0 | 0 | 0 | Reset                      |  |   |  |            |  |  |  |                           |  |  |  |            |  |  |  |

**LP\_UART\_RXFIFO\_FULL\_THRHD** Configures the threshold for RX FIFO being full.

Measurement unit: byte. (R/W)

**LP\_UART\_TXFIFO\_EMPTY\_THRHD** Configures the threshold for TX FIFO being empty.

Measurement unit: byte. (R/W)

**LP\_UART\_CTS\_INV** Configures whether or not to invert the level of LP UART CTS signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_DSR\_INV** Configures whether or not to invert the level of LP UART DSR signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_RTS\_INV** Configures whether or not to invert the level of LP UART RTS signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_DTR\_INV** Configures whether or not to invert the level of LP UART DTR signal.

0: Not invert

1: Invert

(R/W)

**LP\_UART\_SW\_DTR** Configures the DTR signal used in software flow control.

0: Data to be transmitted is not ready.

1: Data to be transmitted is ready.

(R/W)

**LP\_UART\_CLK\_EN** Configures clock gating.

0: Support clock only when the application writes registers.

1: Always force the clock on for registers.

(R/W)

**Register 37.48. LP\_UART\_HWFC\_CONF\_SYNC\_REG (0x002C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |     |                       |   |            |  |       |   |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|-----|-----------------------|---|------------|--|-------|---|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_RX_FLOW_EN |     | LP_UART_RX_FLOW_THRHD |   | (reserved) |  |       |   |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                  | 8   | 7                     | 3 |            |  | 2     | 0 |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                  | 0x0 |                       |   | 0 0 0      |  | Reset |   |  |

**LP\_UART\_RX\_FLOW\_THRHD** Configures the maximum number of data bytes that can be received during hardware flow control.

Measurement unit: byte. (R/W)

**LP\_UART\_RX\_FLOW\_EN** Configures whether or not to enable the LP UART receiver.

0: Disable

1: Enable

(R/W)

**Register 37.49. LP\_UART\_SLEEP\_CONFO\_REG (0x0030)**

|                  |  |  |  |  |    |    |  |                  |  |  |    |    |  |  |  |                  |   |   |  |  |  |  |   |                  |  |  |  |  |  |  |  |       |
|------------------|--|--|--|--|----|----|--|------------------|--|--|----|----|--|--|--|------------------|---|---|--|--|--|--|---|------------------|--|--|--|--|--|--|--|-------|
| LP_UART_WK_CHAR4 |  |  |  |  |    |    |  | LP_UART_WK_CHAR3 |  |  |    |    |  |  |  | LP_UART_WK_CHAR2 |   |   |  |  |  |  |   | LP_UART_WK_CHAR1 |  |  |  |  |  |  |  |       |
| 31               |  |  |  |  | 24 | 23 |  |                  |  |  | 16 | 15 |  |  |  |                  | 8 | 7 |  |  |  |  | 0 |                  |  |  |  |  |  |  |  |       |
| 0x0              |  |  |  |  |    |    |  | 0x0              |  |  |    |    |  |  |  | 0x0              |   |   |  |  |  |  |   | 0x0              |  |  |  |  |  |  |  | Reset |

**LP\_UART\_WK\_CHAR1** Configures wakeup character 1. (R/W)

**LP\_UART\_WK\_CHAR2** Configures wakeup character 2. (R/W)

**LP\_UART\_WK\_CHAR3** Configures wakeup character 3. (R/W)

**LP\_UART\_WK\_CHAR4** Configures wakeup character 4. (R/W)

**Register 37.50. LP\_UART\_SLEEP\_CONF1\_REG (0x0034)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_WK_CHAR0 |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0              |   |   |  |  |  |  |  | Reset |  |

**LP\_UART\_WK\_CHAR0** Configures wakeup character 0. (R/W)

### Register 37.51. LP\_UART\_SLEEP\_CONF2\_REG (0x0038)

|            |  |  |  |                     |  |                      |    |                     |  |                          |  |            |    |   |    |                          |  |   |  |    |    |  |   |      |  |  |  |
|------------|--|--|--|---------------------|--|----------------------|----|---------------------|--|--------------------------|--|------------|----|---|----|--------------------------|--|---|--|----|----|--|---|------|--|--|--|
| (reserved) |  |  |  | LP_UART_WK_MODE_SEL |  | LP_UART_WK_CHAR_MASK |    | LP_UART_WK_CHAR_NUM |  | LP_UART_RX_WAKE_UP_THRHD |  | (reserved) |    |   |    | LP_UART_ACTIVE_THRESHOLD |  |   |  |    |    |  |   |      |  |  |  |
| 31         |  |  |  | 28                  |  | 27                   | 26 | 25                  |  | 21                       |  | 20         | 18 |   | 17 | 13                       |  |   |  | 12 | 10 |  | 9 | 0    |  |  |  |
| 0          |  |  |  | 0                   |  | 0                    | 0  | 0x0                 |  | 0x5                      |  | 1          |    | 0 |    |                          |  | 0 |  | 0  | 0  |  | 0 | 0xf0 |  |  |  |
| Reset      |  |  |  |                     |  |                      |    |                     |  |                          |  |            |    |   |    |                          |  |   |  |    |    |  |   |      |  |  |  |

**LP\_UART\_ACTIVE\_THRESHOLD** Configures the number of RXD edge changes to wake up the chip in wakeup mode 0. (R/W)

**LP\_UART\_RX\_WAKE\_UP\_THRHD** Configures the number of received data bytes to wake up the chip in wakeup mode 1. (R/W)

**LP\_UART\_WK\_CHAR\_NUM** Configures the number of wakeup characters. (R/W)

**LP\_UART\_WK\_CHAR\_MASK** Configures whether or not to mask wakeup characters.

0: Not mask

1: Mask

(R/W)

**LP\_UART\_WK\_MODE\_SEL** Configures which wakeup mode to select.

0: Mode 0

1: Mode 1

2: Mode 2

### 3: Mode 3

(R/W)

### Register 37.52. LP\_UART\_SWFC\_CONFO\_SYNC\_REG (0x003C)

|                     |  |  |  |  |  |  |  |  |  |                   |  |    |    |    |    |    |    |                  |    |   |  |  |  |  |  |                    |  |   |   |  |  |  |  |                   |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |
|---------------------|--|--|--|--|--|--|--|--|--|-------------------|--|----|----|----|----|----|----|------------------|----|---|--|--|--|--|--|--------------------|--|---|---|--|--|--|--|-------------------|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|
| (reserved)          |  |  |  |  |  |  |  |  |  | LP_UART_SEND_XOFF |  |    |    |    |    |    |    | LP_UART_SEND_XON |    |   |  |  |  |  |  | LP_UART_FORCE_XOFF |  |   |   |  |  |  |  | LP_UART_FORCE_XON |  |  |  |  |  |  |  | LP_UART_SW_FLOW_CON_EN |  |  |  |  |  |  |  | LP_UART_XON_XOFF_STILL_SEND |  |  |  |  |  |  |  | LP_UART_XOFF_CHAR |  |  |  |  |  |  |  | LP_UART_XON_CHAR |  |  |  |  |  |  |  |
| 31                  |  |  |  |  |  |  |  |  |  | 23                |  | 22 | 21 | 20 | 19 | 18 | 17 | 16               | 15 | 8 |  |  |  |  |  |                    |  | 7 | 0 |  |  |  |  |                   |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  | 0 0               |  | 0  | 0  | 0  | 0  | 0  | 0  | 0x13             |    |   |  |  |  |  |  | 0x11               |  |   |   |  |  |  |  | Reset             |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |

**LP\_UART\_XON\_CHAR** Configures the XON character for flow control. (R/W)

**LP\_UART\_XOFF\_CHAR** Configures the XOFF character for flow control. (R/W)

**LP\_UART\_XON\_XOFF\_STILL\_SEND** Configures whether the LP UART transmitter can send XON or XOFF characters when it is disabled.

0: Cannot send

1: Can send

(R/W)

**LP\_UART\_SW\_FLOW\_CON\_EN** Configures whether or not to enable software flow control.

0: Disable

1: Enable

(R/W)

**LP\_UART\_XONOFF\_DEL** Configures whether or not to remove flow control characters from the received data.

0: Not move

1: Move

(R/W)

**LP\_UART\_FORCE\_XON** Configures whether the transmitter continues to sending data.

0: Not send

1: Send

(R/W)

**LP\_UART\_FORCE\_XOFF** Configures whether or not to stop the transmitter from sending data.

0: Not stop

1: Stop

(R/W)

**LP\_UART\_SEND\_XON** Configures whether or not to send XON characters.

0: Not send

1: Send

(R/W/SS/SC)

**LP\_UART\_SEND\_XOFF** Configures whether or not to send XOFF characters.

0: Not send

1: Send

(R/W/SS/SC)

Register 37.53. LP\_UART\_SWFC\_CONF1\_REG (0x0040)

|                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |            |  |  |  |                       |  |  |  |            |  |  |  |
|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|------------|--|--|--|-----------------------|--|--|--|------------|--|--|--|
| (reserved)       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_XOFF_THRESHOLD |  |  |  | (reserved) |  |  |  | LP_UART_XON_THRESHOLD |  |  |  | (reserved) |  |  |  |
| 311615111087320  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |            |  |  |  |                       |  |  |  |            |  |  |  |
| 0000000000000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0xc                    |  |  |  | 000        |  |  |  | 0x0                   |  |  |  | 000Reset   |  |  |  |

**LP\_UART\_XON\_THRESHOLD** Configures the threshold for data in RX FIFO to send XON characters in software flow control.

Measurement unit: byte. (R/W)

**LP\_UART\_XOFF\_THRESHOLD** Configures the threshold for data in RX FIFO to send XOFF characters in software flow control.

Measurement unit: byte. (R/W)

Register 37.54. LP\_UART\_TXBRK\_CONF\_SYNC\_REG (0x0044)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_TX_BRK_NUM |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                  | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0xa                |   |   |  |  |  |  |  | Reset |  |

**LP\_UART\_TX\_BRK\_NUM** Configures the number of NULL characters to be sent after finishing data transmission.

Valid only when LP\_UART\_TXD\_BRK is 1. (R/W)

**Register 37.55. LP\_UART\_IDLE\_CONF\_SYNC\_REG (0x0048)**

|            |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  | LP_UART_TX_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  | LP_UART_RX_IDLE_THRHD |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  | 20                  |  |  |  |  |  |  |  |  |  |  |  | 19                    |  |  |  |  |  |  |  |  |  |  |  | 10 |  |  |  |  |  |  |  |  |  |  |  | 9 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  |  |  |  |  | 0                     |  |  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  | 0x100 |  |  |  |  |  |  |  |  |  |  |  | 0x100 |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |

**LP\_UART\_RX\_IDLE\_THRHD** Configures the threshold to generate a frame end signal when the receiver takes more time to receive one data byte data.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

**LP\_UART\_TX\_IDLE\_NUM** Configures the interval between two data transfers.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

**Register 37.56. LP\_UART\_CLK\_CONF\_REG (0x0088)**

|            |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  |                     |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|----|--|--|--|----|--|--|--|----|--|--|--|---------------------|--|--|--|----|--|--|--|----|--|--|--|---|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |    |  |  |  |    |  |  |  |    |  |  |  | LP_UART_RX_RST_CORE |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  | LP_UART_TX_RST_CORE |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  | LP_UART_RX_SCLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_TX_SCLK_EN |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  | 28 |  |  |  | 27 |  |  |  | 26 |  |  |  | 25                  |  |  |  | 24 |  |  |  | 23 |  |  |  |   |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  | 0  |  |  |  | 0  |  |  |  | 0  |  |  |  | 0                   |  |  |  | 0  |  |  |  | 1  |  |  |  | 1 |  |  |  | 0                   |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  | Reset              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_UART\_TX\_SCLK\_EN** Configures whether or not to enable LP UART TX clock.

0: Disable

1: Enable

(R/W)

**LP\_UART\_RX\_SCLK\_EN** Configures whether or not to enable LP UART RX clock.

0: Disable

1: Enable

(R/W)

**LP\_UART\_TX\_RST\_CORE** Write 1 and then write 0 to reset LP UART TX. (R/W)

**LP\_UART\_RX\_RST\_CORE** Write 1 and then write 0 to reset LP UART RX. (R/W)

Register 37.57. LP\_UART\_STATUS\_REG (0x001C)

|             |    |    |              |    |   |              |   |    |            |  |  |                    |    |    |            |    |    |             |   |   |              |   |   |              |   |  |            |   |   |                    |   |   |            |  |  |
|-------------|----|----|--------------|----|---|--------------|---|----|------------|--|--|--------------------|----|----|------------|----|----|-------------|---|---|--------------|---|---|--------------|---|--|------------|---|---|--------------------|---|---|------------|--|--|
| LP_UART_TXD |    |    | LP_UART_RTSN |    |   | LP_UART_DTRN |   |    | (reserved) |  |  | LP_UART_TXFIFO_CNT |    |    | (reserved) |    |    | LP_UART_RXD |   |   | LP_UART_CTSN |   |   | LP_UART_DSRN |   |  | (reserved) |   |   | LP_UART_RXFIFO_CNT |   |   | (reserved) |  |  |
| 31          | 30 | 29 | 28           | 24 |   |              |   | 23 | 19         |  |  |                    | 18 | 16 | 15         | 14 | 13 | 12          | 8 |   |              |   | 7 | 3            |   |  |            | 2 | 0 |                    |   |   |            |  |  |
| 1           | 1  | 1  | 0            | 0  | 0 | 0            | 0 | 0  | 0          |  |  |                    | 0  | 0  | 0          | 1  | 1  | 0           | 0 | 0 | 0            | 0 | 0 | 0            | 0 |  |            |   | 0 | 0                  | 0 | 0 | Reset      |  |  |

Reset

**LP\_UART\_RXFIFO\_CNT** Represents the number of valid data bytes in RX FIFO. (RO)**LP\_UART\_DSRN** Represents the level of the internal LP UART DSR signal. (RO)**LP\_UART\_CTSN** Represents the level of the internal LP UART CTS signal. (RO)**LP\_UART\_RXD** Represents the level of the internal LP UART RXD signal. (RO)**LP\_UART\_TXFIFO\_CNT** Represents the number of valid data bytes in TX FIFO. (RO)**LP\_UART\_DTRN** Represents the level of the internal LP UART DTR signal. (RO)**LP\_UART\_RTSN** Represents the level of the internal LP UART RTS signal. (RO)**LP\_UART\_TXD** Represents the level of the internal LP UART TXD signal. (RO)

Register 37.58. LP\_UART\_MEM\_TX\_STATUS\_REG (0x0068)

|            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |                       |    |    |    |            |    |   |   |                       |   |   |   |            |   |   |   |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|-----------------------|----|----|----|------------|----|---|---|-----------------------|---|---|---|------------|---|---|---|
| (reserved) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LP_UART_TX_SRAM_RADDR |    |    |    | (reserved) |    |   |   | LP_UART_TX_SRAM_WADDR |   |   |   | (reserved) |   |   |   |
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15                    | 14 | 13 | 12 | 11         | 10 | 9 | 8 | 7                     | 6 | 5 | 4 | 3          | 2 | 1 | 0 |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0x0                   | 0  | 0  | 0  | 0          | 0  | 0 | 0 | 0x0                   | 0 | 0 | 0 | 0          | 0 | 0 | 0 |

Reset

**LP\_UART\_TX\_SRAM\_WADDR** Represents the offset address to write TX FIFO. (RO)**LP\_UART\_TX\_SRAM\_RADDR** Represents the offset address to read TX FIFO. (RO)

### Register 37.59. LP\_UART\_MEM\_RX\_STATUS\_REG (0x006C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                       |    |  |  |            |   |    |    |                       |  |  |  |            |   |   |       |  |  |   |   |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------|----|--|--|------------|---|----|----|-----------------------|--|--|--|------------|---|---|-------|--|--|---|---|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_UART_RX_SRAM_WADDR |    |  |  | (reserved) |   |    |    | LP_UART_RX_SRAM_RADDR |  |  |  | (reserved) |   |   |       |  |  |   |   |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17                    | 16 |  |  |            |   | 12 | 11 |                       |  |  |  | 8          | 7 |   |       |  |  | 3 | 2 |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x10                  |    |  |  | 0          | 0 | 0  | 0  | 0x10                  |  |  |  | 0          | 0 | 0 | Reset |  |  |   |   |  |  |  |  |   |

**LP\_UART\_RX\_SRAM\_RADDR** Represents the offset address to read RX FIFO. (RO)

**LP\_UART\_RX\_SRAM\_WADDR** Represents the offset address to write RX FIFO. (RO)

### Register 37.60. LP\_UART\_FSM\_STATUS\_REG (0x0070)

|            |   |   |   |   |   |   |   |                    |  |  |  |                    |  |  |  |
|------------|---|---|---|---|---|---|---|--------------------|--|--|--|--------------------|--|--|--|
| (reserved) |   |   |   |   |   |   |   | LP_UART_ST_UTX_OUT |  |  |  | LP_UART_ST_URX_OUT |  |  |  |
| 31         |   |   |   |   |   |   |   | 7                  |  |  |  | 3                  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                  |  |  |  | 0                  |  |  |  |
| Reset      |   |   |   |   |   |   |   |                    |  |  |  |                    |  |  |  |

**LP\_UART\_ST\_URX\_OUT** Represents the status of the receiver. (RO)

**LP\_UART\_ST\_UTX\_OUT** Represents the status of the transmitter. (RO)



**Register 37.61. LP\_UART\_AFIFO\_STATUS\_REG (0x0090)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_UART_RX_AFIFO_EMPTY<br>LP_UART_RX_AFIFO_FULL<br>LP_UART_TX_AFIFO_EMPTY<br>LP_UART_TX_AFIFO_FULL |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0 | 1 | 0 | Reset |

**LP\_UART\_TX\_AFIFO\_FULL** Represents whether or not the APB TX asynchronous FIFO is full.

0: Not full

1: Full

(RO)

**LP\_UART\_TX\_AFIFO\_EMPTY** Represents whether or not the APB TX asynchronous FIFO is empty.

0: Not empty

1: Empty

(RO)

**LP\_UART\_RX\_AFIFO\_FULL** Represents whether or not the APB RX asynchronous FIFO is full.

0: Not full

1: Full

(RO)

**LP\_UART\_RX\_AFIFO\_EMPTY** Represents whether or not the APB RX asynchronous FIFO is empty.

0: Not empty

1: Empty

(RO)

**Register 37.62. LP\_UART\_AT\_CMD\_PRECNT\_SYNC\_REG (0x0050)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_PRE_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x901                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_UART\_PRE\_IDLE\_NUM** Configures the idle time before the receiver receives the first AT\_CMD.

Measurement unit: bit time (the time to transmit 1 bit). (R/W)

Register 37.63. LP\_UART\_AT\_CMD\_POSTCNT\_SYNC\_REG (0x0054)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_POST_IDLE_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x901                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**LP\_UART\_POST\_IDLE\_NUM** Configures the interval between the last AT\_CMD and subsequent data.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)

### Register 37.64. LP\_UART\_AT\_CMD\_GAPTOUT\_SYNC\_REG (0x0058)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_RX_GAP_TOUT                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11<br>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_UART\_RX\_GAP\_TOUT** Configures the interval between two AT\_CMD characters.  
Measurement unit: bit time (the time to transmit 1 bit). (R/W)

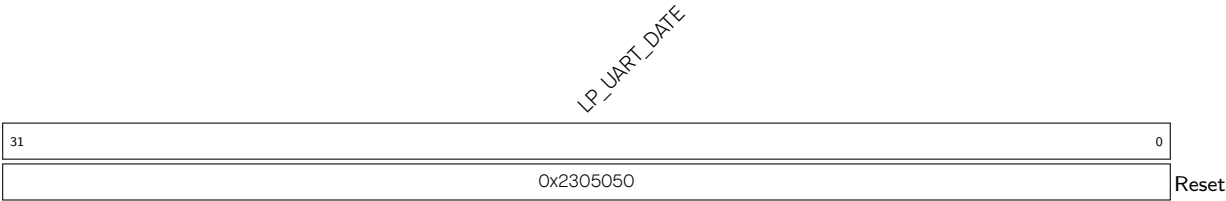
### Register 37.65. LP\_UART\_AT\_CMD\_CHAR\_SYNC\_REG (0x005C)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_UART_CHAR_NUM |  |  |  |  |  |  |  | LP_UART_AT_CMD_CHAR |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15               |  |  |  |  |  |  |  | 7                   |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x3              |  |  |  |  |  |  |  | 0x2b                |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**LP\_UART\_AT\_CMD\_CHAR** Configures the AT\_CMD character. (R/W)

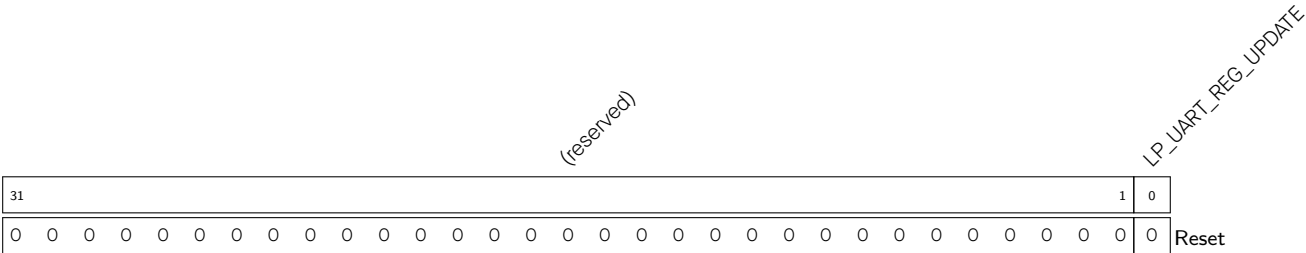
**LP\_UART\_CHAR\_NUM** Configures the number of continuous AT\_CMD characters a receiver can receive. (R/W)

Register 37.66. LP\_UART\_DATE\_REG (0x008C)



LP\_UART\_DATE   Version control register. (R/W)

Register 37.67. LP\_UART\_REG\_UPDATE\_REG (0x0098)

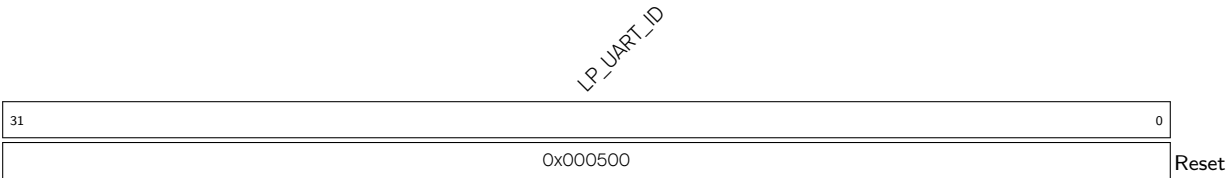


LP\_UART\_REG\_UPDATE   Configures whether or not to synchronize registers.

- 0: Not synchronize
- 1: Synchronize

(R/W/SC)

Register 37.68. LP\_UART\_ID\_REG (0x009C)



LP\_UART\_ID   Configures the LP UART ID. (R/W)

### 37.7.3 UHCI Registers

The addresses in this section are relative to UHCI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 37.69. UHCI\_CONFO\_REG (0x0000)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   |   |   |   |   |  |   |   |       |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|---|---|---|---|---|---|---|--|---|---|-------|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |   |   |   | UHCI_UART_RX_BRK_EOF_EN<br>UHCI_CLK_EN<br>UHCI_ENCODE_CRC_EN<br>UHCI_LEN_EOF_EN<br>UHCI_UART_IDLE_EOF_EN<br>UHCI_CRC_REC_EN<br>UHCI_HEAD_EN<br>UHCI_SEPER_EN<br>UHCI_UART_SEL<br>UHCI_RX_RST<br>UHCI_TX_RST |   |   |   |  |   |   |       |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6   | 5 | 4 |   |  | 2 | 1 | 0     |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 1 | 1 | 0 | 1   | 1 | 1 | 0 |  | 0 | 0 | Reset |  |  |

Reset

**UHCI\_TX\_RST** Write 1 and then write 0 to reset the decoder state machine. (R/W)

**UHCI\_RX\_RST** Write 1 and then write 0 to reset the encoder state machine. (R/W)

**UHCI\_UART0\_CE** Select one UART from UART 0 ~ 4 to connect with UHCI.

0: Select UART0

1: Select UART1

2: Select UART2

3: Select UART3

4: Select UART4

5 ~ 7: No effect, as no UART will connect with UHCI

(R/W)

**UHCI\_UART1\_CE** Configures whether or not to connect UHCI with UART1.

0: Not connect

1: Connect

(R/W)

**UHCI\_SEPER\_EN** Configures whether or not to separate the data frame with a special character.

0: Not separate

1: Separate

(R/W)

**UHCI\_HEAD\_EN** Configures whether or not to encode the data packet with a formatting header.

0: Not use formatting header

1: Use formatting header

(R/W)

Continued on the next page...

**Register 37.69. UHCI\_CONFO\_REG (0x0000)**

Continued from the previous page...

**UHCI\_CRC\_REC\_EN** Configures whether or not to enable the reception of the 16-bit CRC.

0: Disable

1: Enable

(R/W)

**UHCI\_UART\_IDLE\_EOF\_EN** Configures whether or not to stop receiving data when UART is idle.

0: Not stop

1: Stop

(R/W)

**UHCI\_LEN\_EOF\_EN** Configures when the UHCI decoder stops receiving data.

0: Stops after receiving 0xC0

1: Stops when the number of received data bytes reach the specified value. When UHCI\_HEAD\_EN is 1, the specified value is the data length indicated by the UHCI packet header; when UHCI\_HEAD\_EN is 0, the specified value is the configured value.

(R/W)

**UHCI\_ENCODE\_CRC\_EN** Configures whether or not to enable data integrity check by appending a 16 bit CCITT-CRC to the end of the data.

0: Disable

1: Enable

(R/W)

**UHCI\_CLK\_EN** Configures clock gating.

0: Support clock only when the application writes registers.

1: Always force the clock on for registers.

(R/W)

**UHCI\_UART\_RX\_BRK\_EOF\_EN** Configures whether or not to stop UHCI from receiving data after UART has received a NULL frame.

0: Not stop

1: Stop

(R/W)

### Register 37.70. UHCI\_CONF1\_REG (0x0014)

[illegible]

**UHCI\_CHECK\_SUM\_EN** Configures whether or not to enable header checksum validation when UHCI receives a data packet.

0: Disable

1: Enable

(R/W)

**UHCI\_CHECK\_SEQ\_EN** Configures whether or not to enable the sequence number check when UHCI receives a data packet.

0: Disable

1: Enable

(R/W)

**UHCI\_CRC\_DISABLE** Configures whether or not to enable CRC calculation.

0: Disable

1: Enable

Valid only when the Data Integrity Check Present bit in UHCI packet is 1.

(R/W)

**UHCI\_SAVE\_HEAD** Configures whether or not to save the packet header when UHCI receives a data packet.

0: Not save

1: Save

(R/W)

**UHCI\_TX\_CHECK\_SUM\_RE** Configures whether or not to encode the data packet with a checksum.

0: Not use checksum

1: Use checksum

(R/W)

**UHCI\_TX\_ACK\_NUM\_RE** Configures whether or not to encode the data packet with an acknowledgment when a reliable packet is to be transmitted.

0: Not use acknowledgement

1: Use acknowledgement

(R/W)

Continued on the next page...

**Register 37.70. UHCI\_CONF1\_REG (0x0014)**

Continued from the previous page...

**UHCI\_WAIT\_SW\_START** Configures whether or not to put the UHCI encoder state machine to ST\_SW\_WAIT state.

0: No

1: Yes

(R/W)

**UHCI\_SW\_START** Configures whether or not to send data packets when the encoder state machine is in ST\_SW\_WAIT state.

0: Not send

1: Send

(R/W/SC)

### Register 37.71. UHCI\_ESCAPE\_CONF\_REG (0x0020)

[illegible]

**UHCI\_TX\_CO\_ESC\_EN** Configures whether or not to decode character 0xC0 when DMA receives data.

0: Not decode

1: Decode

(R/W)

**UHCI\_TX\_DB\_ESC\_EN** Configures whether or not to decode character 0xDB when DMA receives data.

0: Not decode

1: Decode

(R/W)

**UHCI\_TX\_11\_ESC\_EN** Configures whether or not to decode flow control character 0x11 when DMA receives data.

0: Not decode

1: Decode

(R/W)

|                          |   |
|--------------------------|---|
| <b>UHCI_TX_13_ESC_EN</b> | Configures whether or not to decode flow control character 0x13 when DMA receives data. |
|--------------------------|---|

0: Not decode

1: Decode

(R/W)

**UHCI\_RX\_CO\_ESC\_EN** Configures whether or not to replace 0xC0 by special characters when DMA sends data.

0: Not replace

1: Replace

(R/W)

**UHCI\_RX\_DB\_ESC\_EN** Configures whether or not to replace 0xDB by special characters when DMA sends data.

0: Not replace

1: Replace

(R/W)

Continued on the next page...



**Register 3771. UHCI\_ESCAPE\_CONF\_REG (0x0020)**

Continued from the previous page...

**UHCI\_RX\_11\_ESC\_EN** Configures whether or not to replace flow control character 0x11 by special characters when DMA sends data.

0: Not replace

1: Replace

(R/W)

**UHCI\_RX\_13\_ESC\_EN** Configures whether or not to replace flow control character 0x13 by special characters when DMA sends data.

0: Not replace

1: Replace

(R/W)

**Register 37.72. UHCI\_HUNG\_CONF\_REG (0x0024)**

|            |   |   |   |   |   |   |    |                         |    |   |    |                           |  |  |      |                     |    |    |   |                         |   |  |  |                           |  |  |      |                     |  |  |  |
|------------|---|---|---|---|---|---|----|-------------------------|----|---|----|---------------------------|--|--|------|---------------------|----|----|---|-------------------------|---|--|--|---------------------------|--|--|------|---------------------|--|--|--|
| (reserved) |   |   |   |   |   |   |    | UHCL_RXFIFO_TIMEOUT_ENA |    |   |    | UHCL_RXFIFO_TIMEOUT_SHIFT |  |  |      | UHCL_RXFIFO_TIMEOUT |    |    |   | UHCL_TXFIFO_TIMEOUT_ENA |   |  |  | UHCL_TXFIFO_TIMEOUT_SHIFT |  |  |      | UHCL_TXFIFO_TIMEOUT |  |  |  |
| 31         |   |   |   |   |   |   | 24 | 23                      | 22 |   | 20 | 19                        |  |  |      | 12                  | 11 | 10 |   | 8                       | 7 |  |  |                           |  |  |      | 0                   |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1                       |    | 0 |    |                           |  |  | 0x10 |                     | 1  |    | 0 |                         |   |  |  |                           |  |  | 0x10 | Reset               |  |  |  |

**UHCI\_TXFIFO\_TIMEOUT** Configures the timeout value for DMA data reception.

Measurement unit: ms. (R/W)

**UHCI\_TXFIFO\_TIMEOUT\_SHIFT** Configures the upper limit of the timeout counter for TX FIFO. (R/W)

**UHCI\_TXFIFO\_TIMEOUT\_ENA** Configures whether or not to enable the data reception timeout for TX FIFO.

0: Disable

1: Enable

(R/W)

**UHCI\_RXFIFO\_TIMEOUT** Configures the timeout value for DMA to read data from RAM.

Measurement unit: ms. (R/W)

**UHCI\_RXFIFO\_TIMEOUT\_SHIFT** Configures the upper limit of the timeout counter for RX FIFO. (R/W)

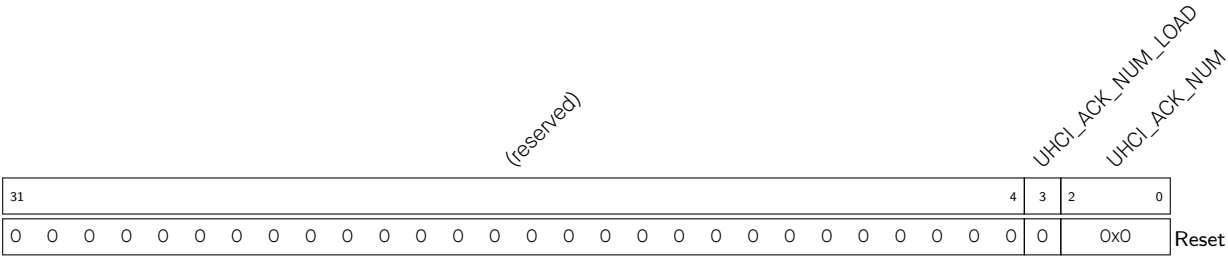
**UHCI\_RXFIFO\_TIMEOUT\_ENA** Configures whether or not to enable the DMA data transmission timeout.

0: Disable

1: Enable

(R/W)

Register 37.73. UHCI\_ACK\_NUM\_REG (0x0028)



**UHCI\_ACK\_NUM** Configures the number of acknowledgements used in software flow control.  
(R/W)

**UHCI\_ACK\_NUM\_LOAD** Configures whether or not load acknowledgements.  
0: Not load  
1: Load  
(WT)

**Register 37.74. UHCI\_QUICK\_SENT\_REG (0x0030)**

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| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | UHCI_ALWAYS_SEND_EN |   |  |  | UHCI_ALWAYS_SEND_NUM |   |   |  | UHCI_SINGLE_SEND_EN |  |  |  | UHCI_SINGLE_SEND_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8 | 7                   | 6 |  |  | 4                    | 3 | 2 |  |                     |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**UHCI\_SINGLE\_SEND\_NUM** Configures the source of data to be transmitted in single\_send mode.

- 0: Q0 register
  - 1: Q1 register
  - 2: Q2 register
  - 3: Q3 register
  - 4: Q4 register
  - 5: Q5 register
  - 6: Q6 register
  - 7: Invalid. No effect
- (R/W)

**UHCI\_SINGLE\_SEND\_EN** Configures whether or not to enable single\_send mode.

- 0: Disable
  - 1: Enable
- (R/W/SC)

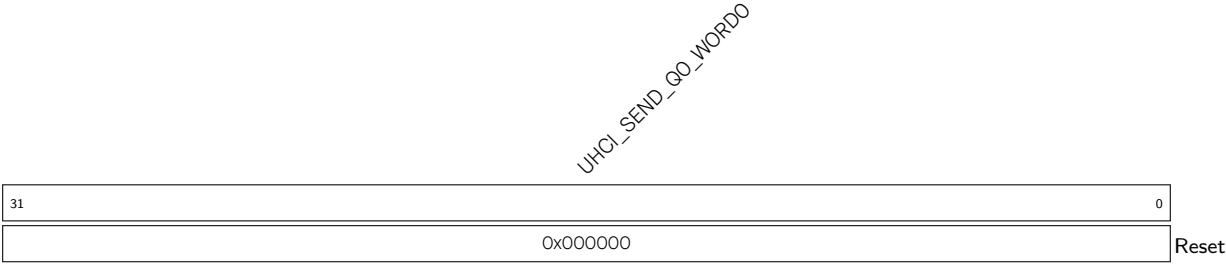
**UHCI\_ALWAYS\_SEND\_NUM** Configures the source of data to be transmitted in always\_send mode.

- 0: Q0 register
  - 1: Q1 register
  - 2: Q2 register
  - 3: Q3 register
  - 4: Q4 register
  - 5: Q5 register
  - 6: Q6 register
  - 7: Invalid. No effect
- (R/W)

**UHCI\_ALWAYS\_SEND\_EN** Configures whether or not to enable always\_send mode.

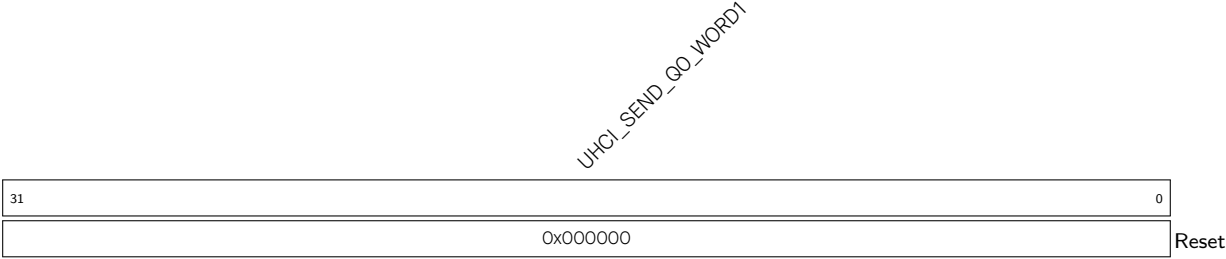
- 0: Disable
  - 1: Enable
- (R/W)

Register 37.75. UHCI\_REG\_Q0\_WORD0\_REG (0x0034)



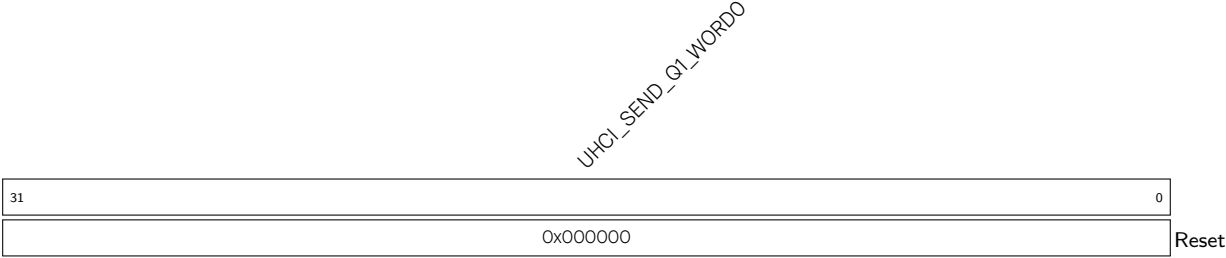
**UHCI\_SEND\_Q0\_WORD0**   Data to be transmitted in Q0 register. (R/W)

Register 37.76. UHCI\_REG\_Q0\_WORD1\_REG (0x0038)



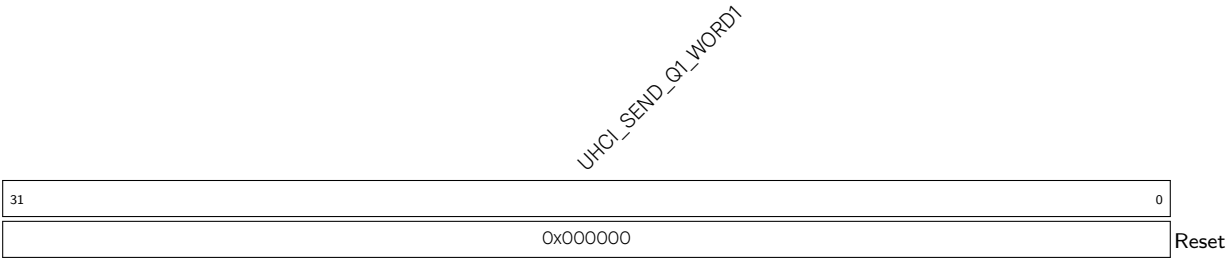
**UHCI\_SEND\_Q0\_WORD1**   Data to be transmitted in Q0 register. (R/W)

Register 37.77. UHCI\_REG\_Q1\_WORD0\_REG (0x003C)



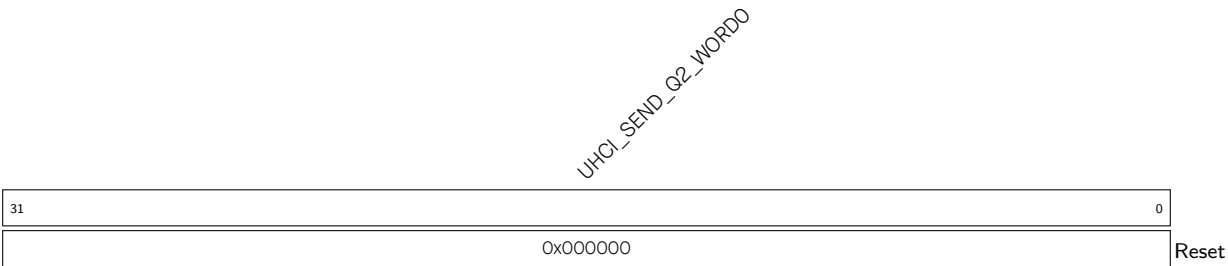
**UHCI\_SEND\_Q1\_WORD0**   Data to be transmitted in Q1 register. (R/W)

Register 37.78. UHCI\_REG\_Q1\_WORD1\_REG (0x0040)



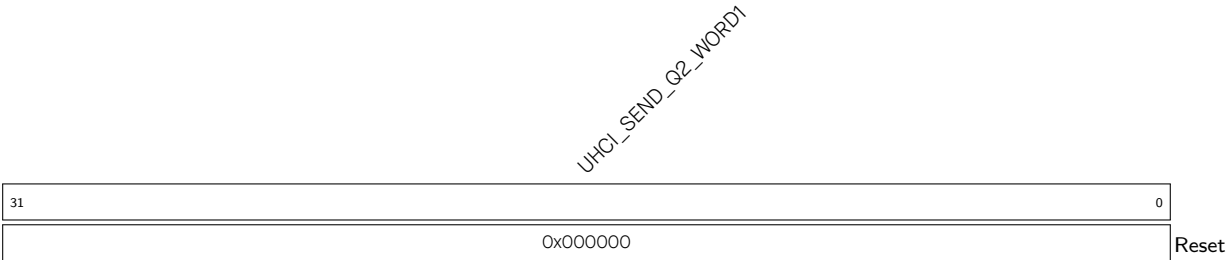
**UHCI\_SEND\_Q1\_WORD1** Data to be transmitted in Q1 register. (R/W)

Register 37.79. UHCI\_REG\_Q2\_WORD0\_REG (0x0044)

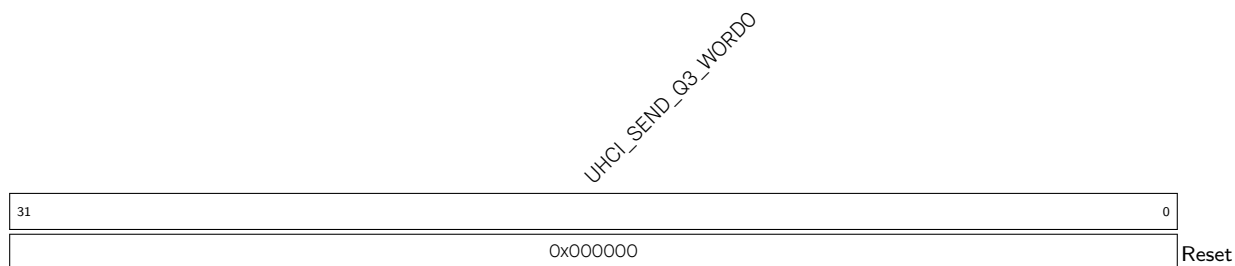


**UHCI\_SEND\_Q2\_WORD0** Data to be transmitted in Q2 register. (R/W)

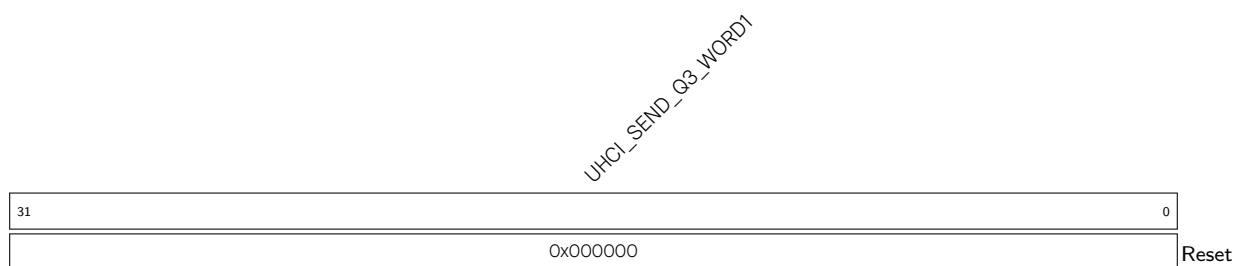
Register 37.80. UHCI\_REG\_Q2\_WORD1\_REG (0x0048)



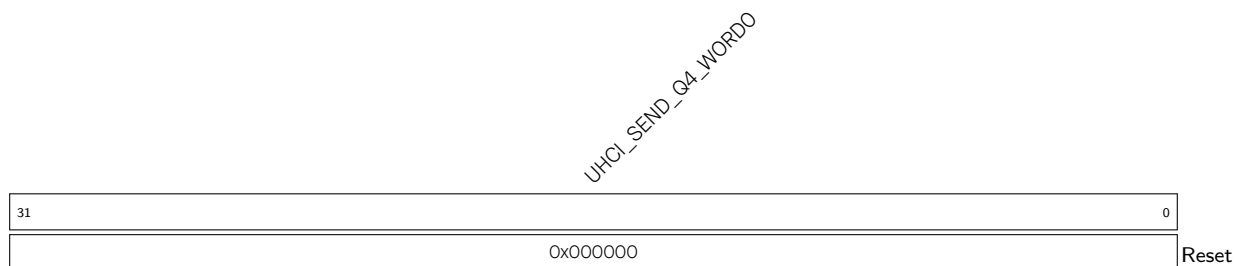
**UHCI\_SEND\_Q2\_WORD1** Data to be transmitted in Q2 register. (R/W)

**Register 37.81. UHCI\_REG\_Q3\_WORD0\_REG (0x004C)**

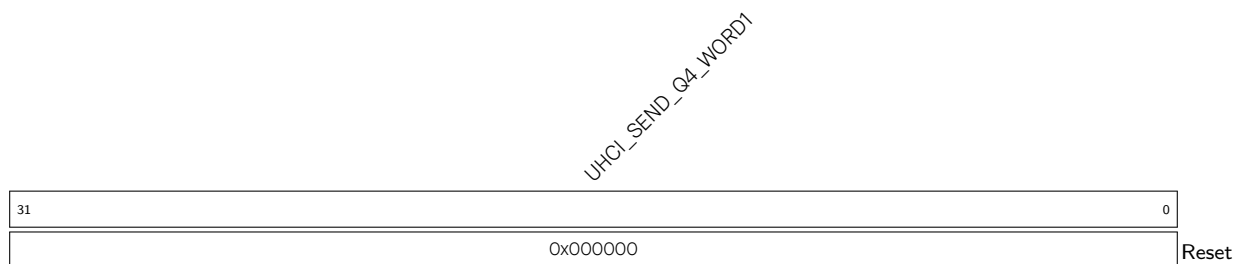
**UHCI\_SEND\_Q3\_WORD0** Data to be transmitted in Q3 register. (R/W)

**Register 37.82. UHCI\_REG\_Q3\_WORD1\_REG (0x0050)**

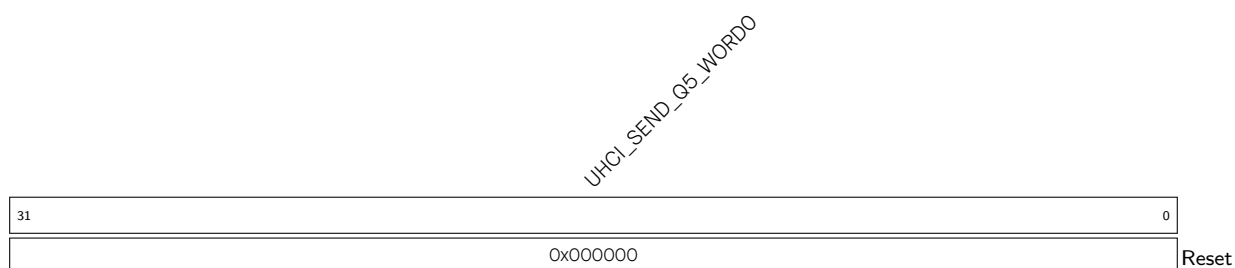
**UHCI\_SEND\_Q3\_WORD1** Data to be transmitted in Q3 register. (R/W)

**Register 37.83. UHCI\_REG\_Q4\_WORD0\_REG (0x0054)**

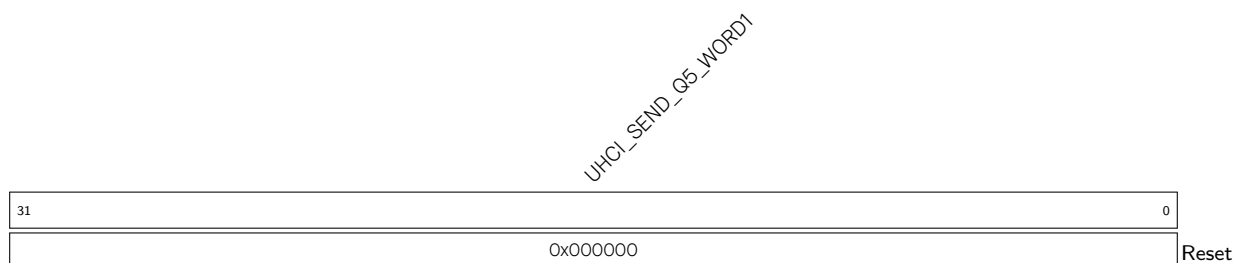
**UHCI\_SEND\_Q4\_WORD0** Data to be transmitted in Q4 register. (R/W)

**Register 37.84. UHCI\_REG\_Q4\_WORD1\_REG (0x0058)**

**UHCI\_SEND\_Q4\_WORD1** Data to be transmitted in Q4 register. (R/W)

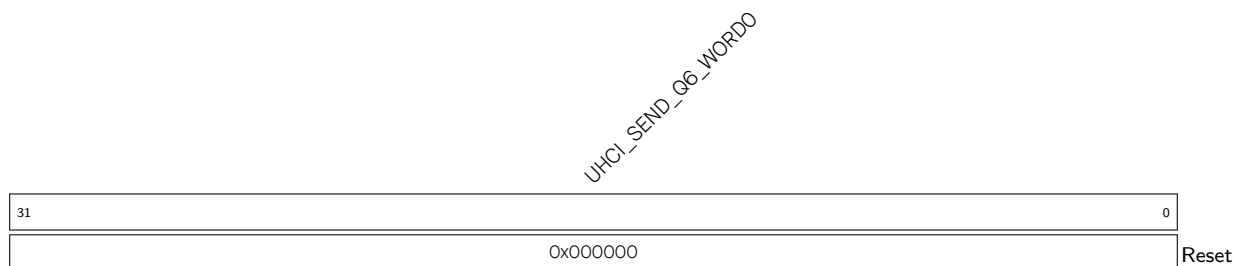
**Register 37.85. UHCI\_REG\_Q5\_WORD0\_REG (0x005C)**

**UHCI\_SEND\_Q5\_WORD0** Data to be transmitted in Q5 register. (R/W)

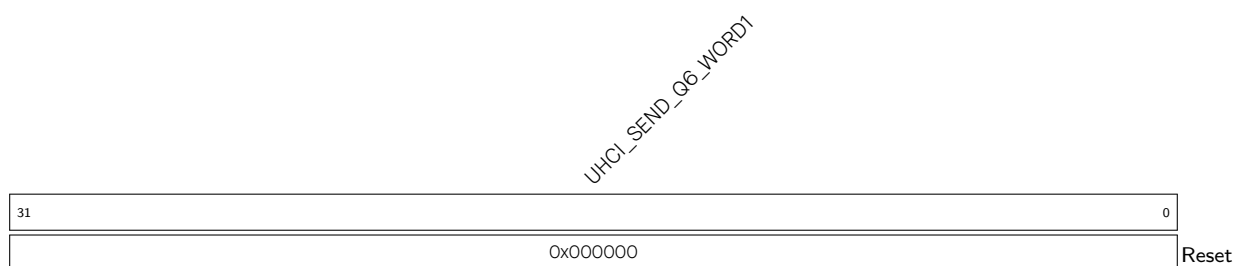
**Register 37.86. UHCI\_REG\_Q5\_WORD1\_REG (0x0060)**

**UHCI\_SEND\_Q5\_WORD1** Data to be transmitted in Q5 register. (R/W)

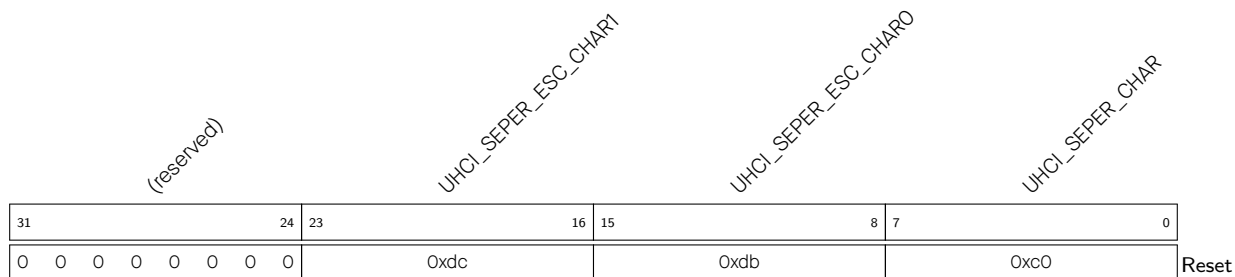


**Register 37.87. UHCI\_REG\_Q6\_WORD0\_REG (0x0064)**

**UHCI\_SEND\_Q6\_WORD0** Data to be transmitted in Q6 register. (R/W)

**Register 37.88. UHCI\_REG\_Q6\_WORD1\_REG (0x0068)**

**UHCI\_SEND\_Q6\_WORD1** Data to be transmitted in Q6 register. (R/W)

**Register 37.89. UHCI\_ESC\_CONFO\_REG (0x006C)**

**UHCI\_SEPER\_CHAR** Configures separators to encode data packets. The default value is 0xc0. (R/W)

**UHCI\_SEPER\_ESC\_CHAR0** Configures the first character of SLIP escape sequence. The default value is 0xdb. (R/W)

**UHCI\_SEPER\_ESC\_CHAR1** Configures the second character of SLIP escape sequence. The default value is 0xdc. (R/W)

**Register 37.90. UHCI\_ESC\_CONF1\_REG (0x0070)**

|            |   |   |   |   |   |   |   |                     |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   | UHCI_ESC_SEQ0_CHAR1 |  |  |  |  |  |  |  | UHCI_ESC_SEQ0_CHAR0 |  |  |  |  |  |  |  | UHCI_ESC_SEQ0 |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   | 24                  |  |  |  |  |  |  |  | 16                  |  |  |  |  |  |  |  | 15            |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0xdd                |  |  |  |  |  |  |  | 0xdb                |  |  |  |  |  |  |  | 0xdb          |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |

**UHCI\_ESC\_SEQ0** Configures the character that needs to be encoded. The default value is 0xDB used as the first character of SLIP escape sequence. (R/W)

**UHCI\_ESC\_SEQ0\_CHAR0** Configures the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

**UHCI\_ESC\_SEQ0\_CHAR1** Configures the second character of SLIP escape sequence. The default value is 0xDD. (R/W)

**Register 37.91. UHCI\_ESC\_CONF2\_REG (0x0074)**

|            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  | 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| 31         |  |  |  |  |  |  |  | 24                  |  |  |  |  |  |  |  | 23                  |  |  |  |  |  |  |  | 16            |  |  |  |  |  |  |  | 15 |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  | 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| 0          |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | 0             |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

**UHCI\_ESC\_SEQ1** Configures a character that need to be encoded. The default value is 0x11 used as a flow control character. (R/W)

**UHCI\_ESC\_SEQ1\_CHAR0** Configures the first character of SLIP escape sequence. The default value is 0xDB. (R/W)

**UHCI\_ESC\_SEQ1\_CHAR1** Configures the second character of SLIP escape sequence. The default value is 0xDE. (R/W)

Register 37.92. UHCI\_ESC\_CONF3\_REG (0x0078)

|            |   |   |   |   |   |   |   |                     |  |  |  |  |  |  |    |                     |  |  |  |  |  |   |  |               |  |  |  |  |   |  |  |       |
|------------|---|---|---|---|---|---|---|---------------------|--|--|--|--|--|--|----|---------------------|--|--|--|--|--|---|--|---------------|--|--|--|--|---|--|--|-------|
| (reserved) |   |   |   |   |   |   |   | UHCI_ESC_SEQ2_CHAR1 |  |  |  |  |  |  |    | UHCI_ESC_SEQ2_CHAR0 |  |  |  |  |  |   |  | UHCI_ESC_SEQ2 |  |  |  |  |   |  |  |       |
| 31         |   |   |   |   |   |   |   | 24                  |  |  |  |  |  |  | 16 |                     |  |  |  |  |  | 8 |  |               |  |  |  |  | 0 |  |  |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0xdf                |  |  |  |  |  |  |    | 0xdb                |  |  |  |  |  |   |  | 0x13          |  |  |  |  |   |  |  | Reset |

- UHCI\_ESC\_SEQ2 Configures the character that needs to be decoded. The default value is 0x13 used as a flow control character. (R/W)
- UHCI\_ESC\_SEQ2\_CHAR0 Configures the first character of SLIP escape sequence. The default value is 0xDB. (R/W)
- UHCI\_ESC\_SEQ2\_CHAR1 Configures the second character of SLIP escape sequence. The default value is 0xDF. (R/W)

Register 37.93. UHCI\_PKT\_THRES\_REG (0x007C)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | UHCL_PKT_THRS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 13            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x80          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

- UHCI\_PKT\_THRS Configures the maximum value of the packet length.  
Measurement unit: byte.  
Valid only when UHCI\_HEAD\_EN is 0. (R/W)

**Register 37.94. UHCI\_INT\_RAW\_REG (0x0004)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UHCI_APP_CTRL1_INT_RAW<br>UHCI_APP_CTRL0_INT_RAW<br>UHCI_OUT_EOF_INT_RAW<br>UHCI_SEND_A_REG_Q_INT_RAW<br>UHCI_SEND_S_REG_Q_INT_RAW<br>UHCI_TX_HUNG_INT_RAW<br>UHCI_RX_HUNG_INT_RAW<br>UHCI_TX_START_INT_RAW<br>UHCI_RX_START_INT_RAW |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2  | 1 | 0 |   |   |   |   |   |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**UHCI\_RX\_START\_INT\_RAW** The raw interrupt status of UHCI\_RX\_START\_INT. (R/WTC/SS)

**UHCI\_TX\_START\_INT\_RAW** The raw interrupt status of UHCI\_TX\_START\_INT. (R/WTC/SS)

**UHCI\_RX\_HUNG\_INT\_RAW** The raw interrupt status of UHCI\_RX\_HUNG\_INT. (R/WTC/SS)

**UHCI\_TX\_HUNG\_INT\_RAW** The raw interrupt status of UHCI\_TX\_HUNG\_INT. (R/WTC/SS)

**UHCI\_SEND\_S\_REG\_Q\_INT\_RAW** The raw interrupt status of UHCI\_SEND\_S\_REG\_Q\_INT.  
(R/WTC/SS)

**UHCI\_SEND\_A\_REG\_Q\_INT\_RAW** The raw interrupt status of UHCI\_SEND\_A\_REG\_Q\_INT.  
(R/WTC/SS)

**UHCI\_OUT\_EOF\_INT\_RAW** The raw interrupt status of UHCI\_OUT\_EOF\_INT. (R/WTC/SS)

**UHCI\_APP\_CTRL0\_INT\_RAW** The raw interrupt status of UHCI\_APP\_CTRL0\_INT. (R/W)

**UHCI\_APP\_CTRL1\_INT\_RAW** The raw interrupt status of UHCI\_APP\_CTRL1\_INT. (R/W)

### Register 37.95. UHCI\_INT\_ST\_REG (0x0008)

[illegible]

**UHCI\_RX\_START\_INT\_ST** The masked interrupt status of UHCI\_RX\_START\_INT. (RO)

|                             |  |
|-----------------------------|--|
| <b>UHCI_TX_START_INT_ST</b> | The masked interrupt status of UHCI_TX_START_INT. (RO) |
|-----------------------------|--|

|                            |   |
|----------------------------|---|
| <b>UHCI_RX_HUNG_INT_ST</b> | The masked interrupt status of UHCI_RX_HUNG_INT. (RO) |
|----------------------------|---|

**UHCI\_TX\_HUNG\_INT\_ST** The masked interrupt status of UHCI\_TX\_HUNG\_INT. (RO)

**UHCI\_SEND\_S\_REG\_Q\_INT\_ST** The masked interrupt status of UHCI\_SEND\_S\_REG\_Q\_INT. (RO)

**UHCI\_SEND\_A\_REG\_Q\_INT\_ST** The masked interrupt status of UHCI\_SEND\_A\_REG\_Q\_INT. (RO)

**UHCI\_OUTLINK\_EOF\_ERR\_INT\_ST** The masked interrupt status of UHCI\_OUTLINK\_EOF\_ERR\_INT.  
(RO)

**UHCI\_APP\_CTRL0\_INT\_ST** The masked interrupt status of UHCI\_APP\_CTRL0\_INT. (RO)

**UHCI\_APP\_CTRL1\_INT\_ST** The masked interrupt status of UHCI\_APP\_CTRL1\_INT. (RO)

**Register 37.96. UHCI\_INT\_ENA\_REG (0x000C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |       |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|-------|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UHCI_APP_CTRL1_INT_ENA<br>UHCI_APP_CTRL0_INT_ENA<br>UHCI_OUTLINK_EOF_ERR_INT_ENA<br>UHCI_SEND_A_REG_Q_INT_ENA<br>UHCI_SEND_S_REG_Q_INT_ENA<br>UHCI_TX_HUNG_INT_ENA<br>UHCI_RX_HUNG_INT_ENA<br>UHCI_TX_START_INT_ENA<br>UHCI_RX_START_INT_ENA |   |   |   |   |   |   |       |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9 | 8 | 7 | 6  | 5 | 4 | 3 | 2 | 1 | 0 | Reset |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 |   |   |   |   |   |       |  |  |

**UHCI\_RX\_START\_INT\_ENA** Write 1 to enable UHCI\_RX\_START\_INT. (R/W)

**UHCI\_TX\_START\_INT\_ENA** Write 1 to enable UHCI\_TX\_START\_INT. (R/W)

**UHCI\_RX\_HUNG\_INT\_ENA** Write 1 to enable UHCI\_RX\_HUNG\_INT. (R/W)

**UHCI\_TX\_HUNG\_INT\_ENA** Write 1 to enable UHCI\_TX\_HUNG\_INT. (R/W)

**UHCI\_SEND\_S\_REG\_Q\_INT\_ENA** Write 1 to enable UHCI\_SEND\_S\_REG\_Q\_INT. (R/W)

**UHCI\_SEND\_A\_REG\_Q\_INT\_ENA** Write 1 to enable UHCI\_SEND\_A\_REG\_Q\_INT. (R/W)

**UHCI\_OUTLINK\_EOF\_ERR\_INT\_ENA** Write 1 to enable UHCI\_OUTLINK\_EOF\_ERR\_INT. (R/W)

**UHCI\_APP\_CTRL0\_INT\_ENA** Write 1 to enable UHCI\_APP\_CTRL0\_INT. (R/W)

**UHCI\_APP\_CTRL1\_INT\_ENA** Write 1 to enable UHCI\_APP\_CTRL1\_INT. (R/W)

**Register 37.97. UHCI\_INT\_CLR\_REG (0x0010)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |       |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|-------|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | UHCL_APP_CTRL1_INT_CLR<br>UHCL_APP_CTRL0_INT_CLR<br>UHCL_OUTLINK_EOF_ERR_INT_CLR<br>UHCL_SEND_A_REG_Q_INT_CLR<br>UHCL_SEND_S_REG_Q_INT_CLR<br>UHCL_TX_HUNG_INT_CLR<br>UHCL_RX_HUNG_INT_CLR<br>UHCL_TX_START_INT_CLR<br>UHCL_RX_START_INT_CLR |   |   |   |   |   |   |       |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9  | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |  |

**UHCI\_RX\_START\_INT\_CLR** Write 1 to clear UHCI\_RX\_START\_INT. (WT)

**UHCI\_TX\_START\_INT\_CLR** Write 1 to clear UHCI\_TX\_START\_INT. (WT)

**UHCI\_RX\_HUNG\_INT\_CLR** Write 1 to clear UHCI\_RX\_HUNG\_INT. (WT)

**UHCI\_TX\_HUNG\_INT\_CLR** Write 1 to clear UHCI\_TX\_HUNG\_INT. (WT)

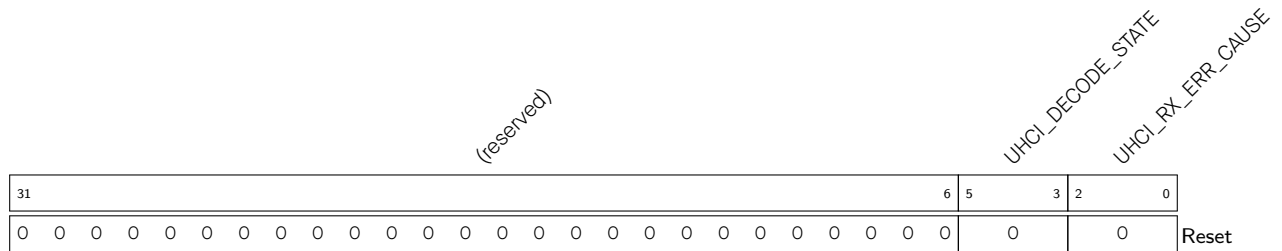
**UHCI\_SEND\_S\_REG\_Q\_INT\_CLR** Write 1 to clear UHCI\_SEND\_S\_REG\_Q\_INT. (WT)

**UHCI\_SEND\_A\_REG\_Q\_INT\_CLR** Write 1 to clear UHCI\_SEND\_A\_REG\_Q\_INT. (WT)

**UHCI\_OUTLINK\_EOF\_ERR\_INT\_CLR** Write 1 to clear UHCI\_OUTLINK\_EOF\_ERR\_INT. (WT)

**UHCI\_APP\_CTRL0\_INT\_CLR** Write 1 to clear UHCI\_APP\_CTRL0\_INT. (WT)

**UHCI\_APP\_CTRL1\_INT\_CLR** Write 1 to clear UHCI\_APP\_CTRL1\_INT. (WT)

**Register 37.98. UHCI\_STATE0\_REG (0x0018)**

**UHCI\_RX\_ERR\_CAUSE** Represents the error type when DMA has received a packet with error.

0: Invalid. No effect

1: Checksum error in the HCI packet

2: Sequence number error in the HCI packet

3: CRC bit error in the HCI packet

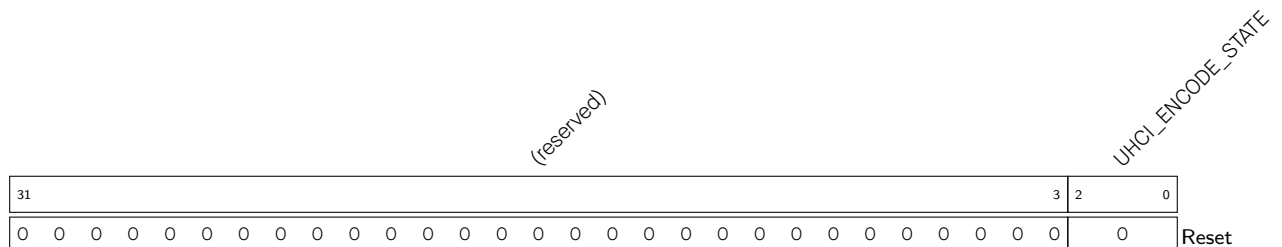
4: 0xC0 is found but the received HCI packet is not complete 5: 0xC0 is not found when the HCI packet has been received

6: CRC check error

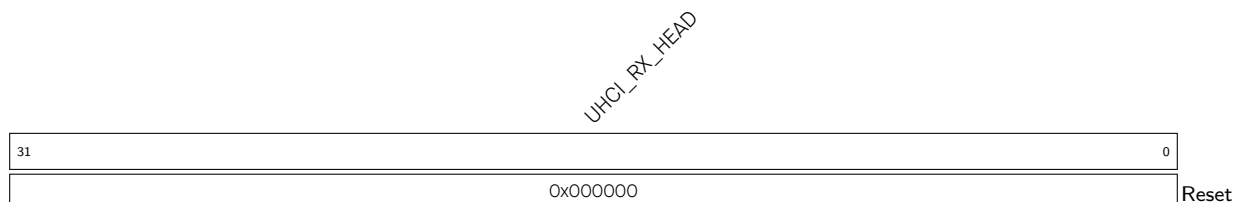
7: Invalid. No effect

(RO)

**UHCI\_DECODE\_STATE** Represents the UHCI decoder status. (RO)

**Register 37.99. UHCI\_STATE1\_REG (0x001C)**

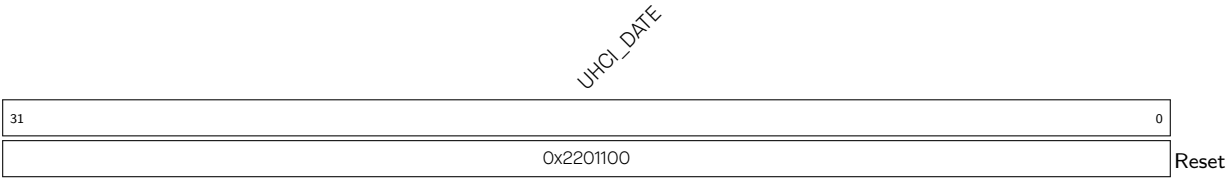
**UHCI\_ENCODE\_STATE** Represents the UHCI encoder status. (RO)

**Register 37.100. UHCI\_RX\_HEAD\_REG (0x002C)**

**UHCI\_RX\_HEAD** Represents the header of the current received packet. (RO)



Register 37.101. UHCI\_DATE\_REG (0x0080)



**UHCI\_DATE** Version control register. (R/W)

## Chapter 38

## SPI Controller (SPI)

### 38.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial interface useful for communication with external peripherals. The ESP32-P4 chip integrates four SPI controllers:

- MSPI controller, including two sub-controllers
  - FLASH MSPI controller
    - \* FLASH MSPI SPI0
    - \* FLASH MSPI SPI1
  - PSRAM MSPI controller
    - \* PSRAM MSPI SPI0
    - \* PSRAM MSPI SPI1
- General Purpose SPI2 (GP-SPI2)
- General Purpose SPI3 (GP-SPI3)
- Low-Power SPI (LP-SPI)

MSPI controller is primarily reserved for internal use to communicate with external flash and PSRAM memory. This chapter mainly focuses on the GP-SPI and LP-SPI. **In this chapter unless otherwise stated, GP-SPI refers to both GP-SPI2 and GP-SPI3.**

### 38.2 Glossary

To better illustrate the functions of GP-SPI and LP-SPI, the following terms are used in this chapter.

|                    |   |
|--------------------|---|
| <b>Master Mode</b> | GP-SPI or LP-SPI acts as an SPI master and initiates SPI transactions.  |
| <b>Slave Mode</b>  | GP-SPI or LP-SPI acts as an SPI slave and exchanges data with its master when its CS is asserted.   |
| <b>MISO</b>        | Master in, slave out, data transmission from a slave to a master.   |
| <b>MOSI</b>        | Master out, slave in, data transmission from a master to a slave.   |
| <b>Transaction</b> | One instance of a master asserting a CS line, transferring data to and from a slave, and de-asserting the CS line. Transactions are atomic, which means they can never be interrupted by another transaction. |

|  |  |
|--|--|
| <b>SPI Transfer</b>                    | The whole process of an SPI master exchanging data with a slave. One SPI transfer consists of one or more SPI transactions.  |
| <b>Single Transfer</b>                 | An SPI transfer that consists of only one transaction.   |
| <b>CPU-Controlled Transfer</b>         | A data transfer that happens between CPU configured buffer <a href="#">SPI_WO_REG~SPI_W15_REG</a> ( <a href="#">LP_SPI_WO_REG~LP_SPI_W15_REG</a> ) and SPI peripherals.                |
| <b>DMA-Controlled Transfer</b>         | A data transfer that happens between DMA and SPI peripherals, controlled by the DMA engine.  |
| <b>Configurable Segmented Transfer</b> | A data transfer controlled by DMA when GP-SPI2 works as a master. Such transfer consists of multiple transactions (segments), and each of transaction can be configured independently. |
| <b>Slave Segmented Transfer</b>        | A data transfer controlled by DMA when GP-SPI works as a slave. Such transfer consists of multiple transactions (segments).  |
| <b>Full-duplex</b>                     | The sending line and receiving line between the master and the slave are independent. Sending data and receiving data happen at the same time.   |
| <b>Half-duplex</b>                     | Only one side, the master or the slave, sends data first, and the other side receives data. Sending data and receiving data can not happen at the same time.                           |
| <b>4-line full-duplex</b>              | 4-line here means: clock line, CS line, and two data lines. The two data lines can be used to send or receive data simultaneously.   |
| <b>4-line half-duplex</b>              | 4-line here means: clock line, CS line, and two data lines. The two data lines can not be used simultaneously.   |
| <b>3-line half-duplex</b>              | 3-line here means: clock line, CS line, and one data line. The data line is used to transmit or receive data.  |
| <b>1-bit SPI</b>                       | In one clock cycle, one bit can be transferred.  |
| <b>(2-bit) Dual SPI</b>                | In one clock cycle, two bits can be transferred.   |
| <b>Dual Output Read</b>                | A data mode of Dual SPI. In one clock cycle, one bit of a command, or one bit of an address, or two bits of data can be transferred.   |
| <b>Dual I/O Read</b>                   | Another data mode of Dual SPI. In one clock cycle, one bit of a command, or two bits of an address, or two bits of data can be transferred.  |
| <b>(4-bit) Quad SPI</b>                | In one clock cycle, four bits can be transferred.  |
| <b>Quad Output Read</b>                | A data mode of Quad SPI. In one clock cycle, one bit of a command, or one bit of an address, or four bits of data can be transferred.  |
| <b>Quad I/O Read</b>                   | Another data mode of Quad SPI. In one clock cycle, one bit of a command, or four bits of an address, or four bits of data can be transferred.  |
| <b>QPI</b>                             | In one clock cycle, four bits of a command, or four bits of an address, or four bits of data can be transferred.   |
| <b>(8-bit) Octal SPI</b>               | In one clock cycle, eight bits can be transferred.   |
| <b>Octal Output Read</b>               | A data mode of Octal SPI. In one clock cycle, one bit of a command, or one bit of an address, or eight bits of data can be transferred.  |

|                       |  |
|-----------------------|--|
| <b>Octal I/O Read</b> | Another data mode of Octal SPI. In one clock cycle, one bit of a command, or eight bits of an address, or eight bits of data can be transferred. |
| <b>OPI</b>            | In one clock cycle, eight bits of a command, or eight bits of an address, or eight bits of data can be transferred.                              |
| <b>SPI2</b>           | The prefix of the signals for GP-SPI2. SPI2 bus signals are routed to GPIO pins via HP GPIO matrix or HP IO MUX.                                 |
| <b>SPI3</b>           | The prefix of the signals for GP-SPI3. SPI3 bus signals are routed to GPIO pins via HP GPIO matrix only.   |
| <b>LP_SPI</b>         | The prefix of the signals for LP-SPI. LP_SPI bus signals are routed to GPIO pins via LP GPIO matrix only.  |

## 38.3 Features

GP-SPI has the following features:

- Works as master or as slave
- Half- and full-duplex communications
- CPU- and DMA-controlled transfers
- Various data modes
  - **GP-SPI2**
    - \* 1-bit SPI mode
    - \* 2-bit Dual SPI mode
    - \* 4-bit Quad SPI mode
    - \* QPI mode
    - \* 8-bit Octal SPI mode (available only when GP-SPI2 works as a master)
    - \* OPI mode (available only when GP-SPI2 works as a master)
  - **GP-SPI3**
    - \* 1-bit SPI mode
    - \* 2-bit Dual SPI mode
    - \* 4-bit Quad SPI mode
    - \* QPI mode
- Configurable module clock frequency
  - Master: up to 80 MHz
  - Slave: up to 60 MHz
- Configurable data length
  - CPU-controlled transfer as master or as slave: 1~64 bytes
  - DMA-controlled single transfer as master: 1~32 KB

- DMA-controlled configurable segmented transfer as master: data length is unlimited
  - DMA-controlled single transfer or segmented transfer as slave: data length is unlimited
- Configurable bit read/write order
- Independent interrupts for CPU-controlled transfer and DMA-controlled transfer
- Configurable clock polarity and phase
- Four SPI clock modes: mode 0~mode 3
- Multiple CS lines as master
  - **GP-SPI2**: CS0~CS5
  - **GP-SPI3**: CS0~CS2
- Able to communicate with SPI devices, such as a sensor, a screen controller, as well as a flash or RAM chip

**LP-SPI is a simplified version of GP-SPI and has a subset of GP-SPI's features:**

- Works as a master or as a slave
- Half- and full-duplex communications
- CPU-controlled transfer
- 1-bit SPI data mode
- Configurable module clock frequency:
  - Master: up to 40 MHz
  - Slave: up to 40 MHz
- Configurable data length:
  - CPU-controlled transfer as master or as slave: 1~64 bytes
- Configurable bit read/write order
- Interrupts for CPU-controlled transfer
- Configurable clock polarity and phase
- Four SPI clock modes: mode 0~mode 3
- One CS line as master: CS0
- Wake-up feature as slave (the only new feature compared with GP-SPI)

## 38.4 Architectural Overview

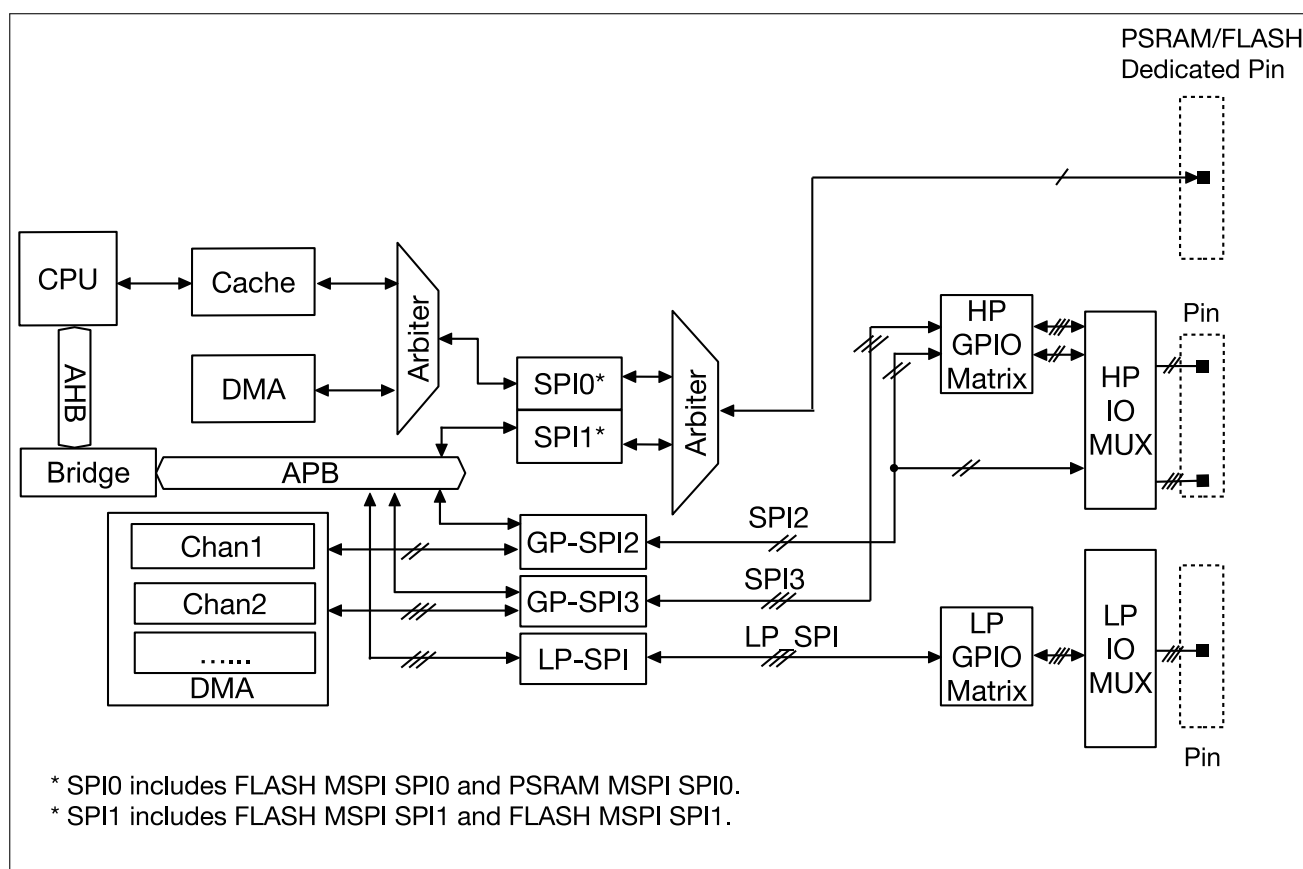


Figure 38.4-1. SPI Module Overview

Figure 38.4-1 shows an overview of this SPI module. GP-SPI2, GP-SPI3, and LP-SPI exchange data with SPI devices by the following ways:

- CPU-controlled transfer:
  - CPU ↔ LP-SPI ↔ SPI devices
  - CPU ↔ GP-SPI2 (GP-SPI3) ↔ SPI devices
- DMA-controlled transfer: DMA ↔ GP-SPI2 (GP-SPI3) ↔ SPI devices

In this chip, “SPI2”, “SPI3”, and “LP\_SPI” are used as prefixes of GP-SPI2, GP-SPI3, and LP-SPI input and output signal buses to illustrate the SPI bus functions.

SPI2 bus signals are routed to GPIO pins via either the HP GPIO matrix or the HP IO MUX, while SPI3 bus signals are routed to GPIO pins via the HP GPIO matrix only. LP\_SPI bus signals are routed via the LP GPIO matrix only. For more information, see Chapter 8 *GPIO Matrix and IO MUX*.

The functionalities of GP-SPI3 are nearly the same as those of GP-SPI2. The functionalities of LP-SPI are a subset of the GP-SPI functionalities. GP-SPI2’s functionalities are described in Section 38.5. The differences among GP-SPI2, GP-SPI3, and LP-SPI are described in Section 38.5.1 and Section 38.10.

## 38.5 Functional Description

### 38.5.1 Data Modes

GP-SPI and LP-SPI can be configured as either a master or a slave to communicate with other SPI devices in the following data modes, see Table 38.5-1. For more information about the data modes used when GP-SPI or LP-SPI works as a master, see Section 38.5.9, and Section 38.5.10 for GP-SPI working as a slave.

**Table 38.5-1. Data Modes Supported by GP-SPI and LP-SPI**

| Data Mode |                   | CMD State | Address State | Data State | GP-SPI2 | GP-SPI3 | LP-SPI |
|-----------|-------------------|-----------|---------------|------------|---------|---------|--------|
| 1-bit SPI |                   | 1-bit     | 1-bit         | 1-bit      | Y       | Y       | Y      |
| Dual SPI  | Dual Output Read  | 1-bit     | 1-bit         | 2-bit      | Y       | Y       | —      |
|           | Dual I/O Read     | 1-bit     | 2-bit         | 2-bit      | Y       | Y       | —      |
| Quad SPI  | Quad Output Read  | 1-bit     | 1-bit         | 4-bit      | Y       | Y       | —      |
|           | Quad I/O Read     | 1-bit     | 4-bit         | 4-bit      | Y       | Y       | —      |
| Octal SPI | Octal Output Read | 1-bit     | 1-bit         | 8-bit      | Y       | —       | —      |
|           | Octal I/O Read    | 1-bit     | 8-bit         | 8-bit      | Y       | —       | —      |
| QPI       |                   | 4-bit     | 4-bit         | 4-bit      | Y       | Y       | —      |
| OPI       |                   | 8-bit     | 8-bit         | 8-bit      | Y       | —       | —      |

### 38.5.2 Introduction to Bus Signals

The functional description of SPI2/SPI3 and LP\_SPI bus signals is shown in Table 38.5-2. Tables 38.5-3, 38.5-4, and 38.5-5 list the signals used in various SPI modes.

**Table 38.5-2. Functional Description of SPI2/SPI3 and LP\_SPI Bus Signals**

| SPI2 Bus Signal | SPI3 Bus Signal | LP-SPI Bus Signal | Function                                       |
|-----------------|-----------------|-------------------|--|
| SPI2CLK         | SPI3_CLK        | LP_SPI_CLK        | Input and output clock as master/slave         |
| SPI2CS0         | SPI3_CS0        | LP_SPI_CS         | Input and output CS signal as master/slave     |
| SPI2CS1~5       | SPI3_CS1~2      | —                 | Output CS signal as master                     |
| SPI2D           | SPI3_D          | LP_SPI_D          | MOSI/SIO0 (serial data input and output, bit0) |
| SPI2Q           | SPI3_Q          | LP_SPI_Q          | MISO/SIO1 (serial data input and output, bit1) |
| SPI2WP          | SPI3_WP         | —                 | SIO2 (serial data input and output, bit2)      |
| SPI2HD          | SPI3_HD         | —                 | SIO3 (serial data input and output, bit3)      |
| SPI2D4~7        | —               | —                 | SIO4~7 (serial data input and output, bit4~7)  |
| SPI2DQS         | —               | —                 | Output data mask signal as master              |

Table 38.5-3. SPI2 Bus Signals Used in Various SPI Modes

| SPI2<br>Bus<br>Signal | Master          |                        |                  |                |                |     |           |     | Slave |           |                  |                |                |     |
|-----------------------|-----------------|------------------------|------------------|----------------|----------------|-----|-----------|-----|-------|-----------|------------------|----------------|----------------|-----|
|                       | FD <sup>1</sup> | 1-bit SPI              |                  | Dual SPI       | Quad SPI       | QPI | Octal SPI | OPI | FD    | 1-bit SPI |                  | Dual SPI       | Quad SPI       | QPI |
|                       |                 | 3-line HD <sup>2</sup> | 4-line HD        |                |                |     |           |     |       | 3-line HD | 4-line HD        |                |                |     |
| SPI2CLK               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   | Y     | Y         | Y                | Y              | Y              | Y   |
| SPI2CS0               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   | Y     | Y         | Y                | Y              | Y              | Y   |
| SPI2CS1               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   |       |           |                  |                |                |     |
| SPI2CS2               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   |       |           |                  |                |                |     |
| SPI2CS3               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   |       |           |                  |                |                |     |
| SPI2CS4               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   |       |           |                  |                |                |     |
| SPI2CS5               | Y               | Y                      | Y                | Y              | Y              | Y   | Y         | Y   |       |           |                  |                |                |     |
| SPI2D                 | Y               | Y                      | (Y) <sup>3</sup> | Y <sup>4</sup> | Y <sup>5</sup> | Y   | Y         | Y   | Y     | Y         | (Y) <sup>6</sup> | Y <sup>7</sup> | Y <sup>8</sup> | Y   |
| SPI2Q                 | Y               |                        | (Y) <sup>3</sup> | Y <sup>4</sup> | Y <sup>5</sup> | Y   | Y         | Y   | Y     |           | (Y) <sup>6</sup> | Y <sup>7</sup> | Y <sup>8</sup> | Y   |
| SPI2WP                |                 |                        |                  |                | Y <sup>5</sup> | Y   | Y         | Y   |       |           |                  |                | Y <sup>8</sup> | Y   |
| SPI2HD                |                 |                        |                  |                | Y <sup>5</sup> | Y   | Y         | Y   |       |           |                  |                | Y <sup>8</sup> | Y   |
| SPI2D4~7              |                 |                        |                  |                |                |     | Y         | Y   |       |           |                  |                |                |     |
| SPI2DQS               |                 |                        |                  |                |                |     | Y         | Y   |       |           |                  |                |                |     |

<sup>1</sup> FD: full-duplex<sup>2</sup> HD: half-duplex<sup>3</sup> Only one of the two signals is used at a time.<sup>4</sup> The two signals are used in parallel.<sup>5</sup> The four signals are used in parallel.<sup>6</sup> Only one of the two signals is used at a time.<sup>7</sup> The two signals are used in parallel.<sup>8</sup> The four signals are used in parallel.



Table 38.5-4. SPI3 Bus Signals Used in Various SPI Modes

| SPI3<br>Bus<br>Signal | Master          |                                     |                  |                |                |     | Slave |                        |                  |                |                |     |
|-----------------------|-----------------|-------------------------------------|------------------|----------------|----------------|-----|-------|------------------------|------------------|----------------|----------------|-----|
|                       | FD <sup>1</sup> | 1-bit SPI<br>3-line HD <sup>2</sup> | 4-line HD        | Dual SPI       | Quad SPI       | QPI | FD    | 1-bit SPI<br>3-line HD | 4-line HD        | Dual SPI       | Quad SPI       | QPI |
| SPI3_CLK              | Y               | Y                                   | Y                | Y              | Y              | Y   | Y     | Y                      | Y                | Y              | Y              | Y   |
| SPI3_CS0              | Y               | Y                                   | Y                | Y              | Y              | Y   | Y     | Y                      | Y                | Y              | Y              | Y   |
| SPI3_CS1              | Y               | Y                                   | Y                | Y              | Y              | Y   |       |                        |                  |                |                |     |
| SPI3_CS2              | Y               | Y                                   | Y                | Y              | Y              | Y   |       |                        |                  |                |                |     |
| SPI3_D                | Y               | Y                                   | (Y) <sup>3</sup> | Y <sup>4</sup> | Y <sup>5</sup> | Y   | Y     | Y                      | (Y) <sup>6</sup> | Y <sup>7</sup> | Y <sup>8</sup> | Y   |
| SPI3_Q                | Y               |                                     | (Y) <sup>3</sup> | Y <sup>4</sup> | Y <sup>5</sup> | Y   | Y     |                        | (Y) <sup>6</sup> | Y <sup>7</sup> | Y <sup>8</sup> | Y   |
| SPI3_WP               |                 |                                     |                  |                | Y <sup>5</sup> | Y   |       |                        |                  |                | Y <sup>8</sup> | Y   |
| SPI3_HD               |                 |                                     |                  |                | Y <sup>5</sup> | Y   |       |                        |                  |                | Y <sup>8</sup> | Y   |

<sup>1</sup> FD: full-duplex<sup>2</sup> HD: half-duplex<sup>3</sup> Only one of the two signals is used at a time.<sup>4</sup> The two signals are used in parallel.<sup>5</sup> The four signals are used in parallel.<sup>6</sup> Only one of the two signals is used at a time.<sup>7</sup> The two signals are used in parallel.<sup>8</sup> The four signals are used in parallel.

Table 38.5-5. LP-SPI Bus Signals Used in Various SPI Modes

| LP_SPI Bus Signal | Master (1-bit SPI) |                        |                  | Slave (1-bit SPI) |           |                  |
|-------------------|--------------------|------------------------|------------------|-------------------|-----------|------------------|
|                   | FD <sup>1</sup>    | 3-line HD <sup>2</sup> | 4-line HD        | FD                | 3-line HD | 4-line HD        |
| LP_SPI_CLK        | Y                  | Y                      | Y                | Y                 | Y         | Y                |
| LP_SPI_CS         | Y                  | Y                      | Y                | Y                 | Y         | Y                |
| LP_SPI_D          | Y                  | Y                      | (Y) <sup>3</sup> | Y                 | Y         | (Y) <sup>3</sup> |
| LP_SPI_Q          | Y                  |                        | (Y) <sup>3</sup> | Y                 |           | (Y) <sup>3</sup> |

<sup>1</sup> FD: full-duplex<sup>2</sup> HD: half-duplex<sup>3</sup> Only one of the two signals is used at a time.

### 38.5.3 Bit Read/Write Order Control

- GP-SPI
  - When operating as a master:
    - \* The bit order of the command, address and data sent by the GP-SPI master is controlled by [SPI\\_WR\\_BIT\\_ORDER](#).
    - \* The bit order of the data received by the master is controlled by [SPI\\_RD\\_BIT\\_ORDER](#).
  - When operating as a slave:
    - \* The bit order of the data sent by the GP-SPI slave is controlled by [SPI\\_WR\\_BIT\\_ORDER](#).
    - \* The bit order of the command, address and data received by the slave is controlled by [SPI\\_RD\\_BIT\\_ORDER](#).
- LP-SPI
  - When operating as a master:
    - \* The bit order of the command, address and data sent by the LP-SPI master is controlled by [LP\\_SPI\\_WR\\_BIT\\_ORDER](#).
    - \* The bit order of the data received by the master is controlled by [LP\\_SPI\\_RD\\_BIT\\_ORDER](#).
  - When operating as a slave:
    - \* The bit order of the data sent by the LP-SPI slave is controlled by [LP\\_SPI\\_WR\\_BIT\\_ORDER](#).
    - \* The bit order of the command, address and data received by the slave is controlled by [LP\\_SPI\\_RD\\_BIT\\_ORDER](#).

Tables [38.5-6](#) and [38.5-7](#) show the functions of [SPI\\_RD/WR\\_BIT\\_ORDER](#) and [LP\\_SPI\\_RD/WR\\_BIT\\_ORDER](#).

Table 38.5-6. Bit Order Control in GP-SPI (Take GP-SPI2 as an Example)

| Bit Mode   | SPI2 Bus Data  | <a href="#">SPI_RD/WR_BIT_ORDER</a> = 0 (MSB) | <a href="#">SPI_RD/WR_BIT_ORDER</a> = 2 (MSB) | <a href="#">SPI_RD/WR_BIT_ORDER</a> = 1 (LSB) | <a href="#">SPI_RD/WR_BIT_ORDER</a> = 3 (LSB) |
|------------|----------------|---|---|---|---|
| 1-bit mode | SPI2D or SPI2Q | B7→B6→B5→B4→B3→B2→B1→B0                       | B7→B6→B5→B4→B3→B2→B1→B0                       | B0→B1→B2→B3→B4→B5→B6→B7                       | B0→B1→B2→B3→B4→B5→B6→B7                       |
| 2-bit mode | SPI2Q          | B7→B5→B3→B1                                   | B6→B4→B2→B0                                   | B1→B3→B5→B7                                   | B0→B2→B4→B6                                   |
|            | SPI2D          | B6→B4→B2→B0                                   | B7→B5→B3→B1                                   | B0→B2→B4→B6                                   | B1→B3→B5→B7                                   |
| 4-bit mode | SPI2HD         | B7→B3   | B4→B0   | B3→B7   | B0→B4   |
|            | SPI2WP         | B6→B2   | B5→B1   | B2→B6   | B1→B5   |
|            | SPI2Q          | B5→B1   | B6→B2   | B1→B5   | B2→B6   |
|            | SPI2D          | B4→B0   | B7→B3   | B0→B4   | B3→B7   |
| 8-bit mode | SPI2D7         | B7  | B7  | B0  | B0  |
|            | SPI2D6         | B6  | B6  | B1  | B1  |
|            | SPI2D5         | B5  | B5  | B2  | B2  |
|            | SPI2D4         | B4  | B4  | B3  | B3  |
|            | SPI2HD         | B3  | B3  | B4  | B4  |
|            | SPI2WP         | B2  | B2  | B5  | B5  |
|            | SPI2Q          | B1  | B1  | B6  | B6  |
|            | SPI2D          | B0  | B0  | B7  | B7  |

Table 38.5-7. Bit Order Control in LP-SPI

| Bit Mode   | LP_SPI Bus Signal    | <a href="#">LP_SPI_RD/WR_BIT_ORDER</a> = 0 (MSB) | <a href="#">LP_SPI_RD/WR_BIT_ORDER</a> = 1 (LSB) |
|------------|----------------------|--|--|
| 1-bit mode | LP_SPI_D or LP_SPI_Q | B7→B6→B5→B4→B3→B2→B1→B0                          | B0→B1→B2→B3→B4→B5→B6→B7                          |

### 38.5.4 Unaligned Byte Transfer

- When operating as a master, GP-SPI sends and receives data in bits. The bit length is equal to `SPI_MS_DATA_BITLEN` + 1, a multiple of 1/2/4/8 in 1/2/4/8-bit mode.
  - When sending data whose length is not an integer multiple of 8 bits, the software needs to fill the last part of the data less than 8 bits into a full 1-byte data.
  - When receiving data whose length is not an integer multiple of 8 bits, the part less than 1 byte is still received as 1 byte.
- When operating as slave, GP-SPI sends and receives data in bits. The bit length is a multiple of 1/2/4/8 in 1/2/4/8-bit mode.
  - When sending data whose length is not an integer multiple of 8 bits, the software needs to fill the last part of the data less than 8 bits into a full 1-byte data.
  - When receiving data whose length is not an integer multiple of 8 bits, the part less than 1 byte is still received as 1 byte. The total bit length received can be read from `SPI_SLV_DATA_BITLEN`. The valid bits in the last 1 byte is indicated by `SPI_SLV_LAST_BYTE_STRB`.

**Note:**

- No matter working as master or slave, GP-SPI sends and receives the data parts less than 1 byte following the same bit order as the other data bits as configured.
- LP-SPI does not support this unaligned byte transfer.

### 38.5.5 Transfer Types

The transfer types supported by GP-SPI working as a master or a slave are shown in Table 38.5-8.

Table 38.5-8. Supported Transfer Types as Master or Slave

| Mode   |             | CPU-Controlled<br>Single Transfer<br>1 | DMA-Controlled<br>Single Transfer | DMA-Controlled<br>Configurable<br>Segmented Transfer<br>2 | DMA-Controlled<br>Slave Segmented<br>Transfer |
|--------|-------------|--|-----------------------------------|---|---|
| Master | Full-Duplex | Y                                      | Y                                 | Y   | —   |
|        | Half-Duplex | Y                                      | Y                                 | Y   | —   |
| Slave  | Full-Duplex | Y                                      | Y                                 | —   | Y   |
|        | Half-Duplex | Y                                      | Y                                 | —   | Y   |

<sup>1</sup> LP-SPI supports only the CPU-controlled single transfer.

<sup>2</sup> GP-SPI3 does not support DMA-controlled configurable segmented transfer.

The following sections provide detailed information about the transfer types listed in the table above.

### 38.5.6 CPU-Controlled Data Transfer

**Note:**

Both GP-SPI and LP-SPI provide 16 x 32-bit data buffers:

- GP-SPI: [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#)
- LP-SPI: [LP\\_SPI\\_W0\\_REG~LP\\_SPI\\_W15\\_REG](#)

The following section illustrates the buffer's structure using GP-SPI data buffer as an example.

Figure 38.5-1 shows the buffer's structure. CPU-controlled transfer indicates the transfer, in which the data to send is from GP-SPI data buffer and the received data is stored to GP-SPI data buffer. In such transfer, every single transaction needs to be triggered by the CPU, after its related registers are configured. For such reason, the CPU-controlled transfer is always single transfer (consisting of only one transaction). CPU-controlled transfer supports full-duplex communication and half-duplex communication.

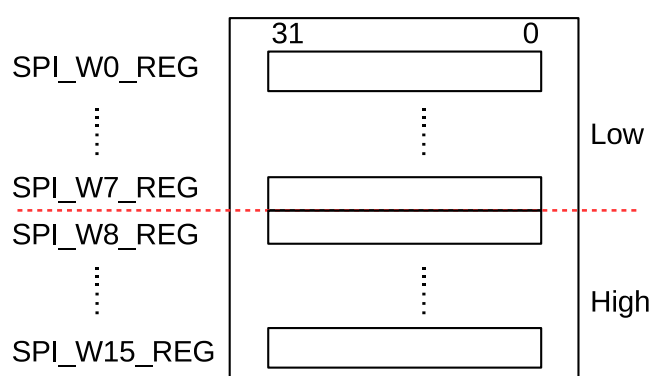


Figure 38.5-1. Data Buffer Used in CPU-Controlled Transfer

### 38.5.6.1 CPU-Controlled Master Transfer

In a CPU-controlled master full-duplex or half-duplex transfer, the RX or TX data is saved to or sent from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#). The bits [SPI\\_USR\\_MOSI\\_HIGHPART](#) and [SPI\\_USR\\_MISO\\_HIGHPART](#) control which buffers are used. See the description below.

- TX data

- When [SPI\\_USR\\_MOSI\\_HIGHPART](#) is cleared, i.e., high part mode is disabled, TX data is read from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#) and the data address is incremented by 1 on each byte transferred. **If the data byte length is larger than 64, the data in [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#) may be sent more than once.**

Take each 256 bytes as a cycle:

- \* The first 64 bytes (Byte 0~Byte 63) are read from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* Byte 64~Byte 255 are read from [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* Byte 256~Byte 319 (the first 64 bytes in another 256 bytes) are read from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#) again, sequentially, same as the behaviors described above.

**For instance:** to send 258 bytes (Byte 0~Byte 257), the data is read from the registers as follows:

- \* The first 64 bytes (Byte 0~Byte 63) are read from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* Byte 64~Byte 255 are read from [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.

- \* The other bytes (*Byte 256* and *Byte 257*) are read from [SPI\\_WO\\_REG\[7:0\]](#) and [SPI\\_WO\\_REG\[15:8\]](#) again, sequentially. The logic is:
  - The address to read data for *Byte 256* is the result of  $(256 \% 64 = 0)$ , i.e., [SPI\\_WO\\_REG\[7:0\]](#).
  - The address to read data for *Byte 257* is the result of  $(257 \% 64 = 1)$ , i.e., [SPI\\_WO\\_REG\[15:8\]](#).
- When [SPI\\_USR\\_MOSI\\_HIGHPART](#) is set, i.e., high part mode is enabled, TX data is read from [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) and the data address is incremented by 1 on each byte transferred. **If the data byte length is larger than 32, the data in [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) may be sent more than once.**

Take each 256 bytes as a cycle:

- \* The first 32 bytes (*Byte 0~Byte 31*) are read from [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 32~Byte 255* are read from [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* *Byte 256~Byte 287* (the first 32 bytes in the another 256 bytes) are read from [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) again, sequentially, same as the behaviors described above.

**For instance:** to send 258 bytes (*Byte 0~Byte 257*), the data is read from the registers as follows:

- \* The first 32 bytes (*Byte 0~Byte 31*) are read from [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 32~Byte 255* are read from [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* The other bytes (*Byte 256* and *Byte 257*) are read from [SPI\\_W8\\_REG\[7:0\]](#) and [SPI\\_W8\\_REG\[15:8\]](#) again, sequentially. The logic is:
  - The address to read data for *Byte 256* is the result of  $(256 \% 32 = 0)$ , i.e., [SPI\\_W8\\_REG\[7:0\]](#).
  - The address to read data for *Byte 257* is the result of  $(257 \% 32 = 1)$ , i.e., [SPI\\_W8\\_REG\[15:8\]](#).

#### • RX data

- When [SPI\\_USR\\_MISO\\_HIGHPART](#) is cleared, i.e., high part mode is disabled, RX data is saved to [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#), and the data address is incremented by 1 on each byte transferred. **If the data byte length is larger than 64, the data in [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) may be overwritten.**

Take each 256 bytes as a cycle:

- \* The first 64 bytes (*Byte 0~Byte 63*) are saved to [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 64~Byte 255* are saved to [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* *Byte 256~Byte 319* (the first 64 bytes in the another 256 bytes) are saved to [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) again, sequentially, same as the behaviors described above.

**For instance:** to receive 258 bytes (*Byte 0~Byte 257*), the data is saved to the registers as follows:

- \* The first 64 bytes (*Byte 0~Byte 63*) are saved to [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 64~Byte 255* are saved to [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.

- \* The other bytes (*Byte 256* and *Byte 257*) are saved to [SPI\\_WO\\_REG\[7:0\]](#) and [SPI\\_WO\\_REG\[15:8\]](#) again, sequentially. The logic is:
  - The address to save *Byte 256* is the result of  $(256 \% 64 = 0)$ , i.e., [SPI\\_WO\\_REG\[7:0\]](#).
  - The address to save *Byte 257* is the result of  $(257 \% 64 = 1)$ , i.e., [SPI\\_WO\\_REG\[15:8\]](#).
- When [SPI\\_USR\\_MISO\\_HIGHPART](#) is set, i.e., high part mode is enabled, the RX data is saved to [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#), and the data address is incremented by 1 on each byte transferred. **If the data byte length is larger than 32, the content of [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) may be overwritten.**

Take each 256 bytes as a cycle:

- \* *Byte 0~Byte 31* are saved to [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 32~Byte 255* are saved to [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* *Byte 256~Byte 287* (the first 32 bytes in the another 256 bytes) are saved to [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) again, sequentially.

**For instance:** to receive 258 bytes (*Byte 0~Byte 257*), the data is saved to the registers as follows:

- \* The first 32 bytes (*Byte 0~Byte 31*) are saved to [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#), sequentially.
- \* *Byte 32~Byte 255* are saved to [SPI\\_W15\\_REG\[31:24\]](#) repeatedly.
- \* The other bytes (*Byte 256* and *Byte 257*) are saved to [SPI\\_W8\\_REG\[7:0\]](#) and [SPI\\_W8\\_REG\[15:8\]](#) again, sequentially. The logic is:
  - The address to save *Byte 256* is the result of  $(256 \% 32 = 0)$ , i.e., [SPI\\_W8\\_REG\[7:0\]](#).
  - The address to save *Byte 257* is the result of  $(257 \% 32 = 1)$ , i.e., [SPI\\_W8\\_REG\[15:8\]](#).

**Note:**

- TX/RX data address mentioned above both are byte-addressable.
  - If high part mode is disabled, Address 0 stands for [SPI\\_WO\\_REG\[7:0\]](#), and Address 1 for [SPI\\_WO\\_REG\[15:8\]](#), and so on.
  - If high part mode is enabled, Address 0 stands for [SPI\\_W8\\_REG\[7:0\]](#), and Address 1 for [SPI\\_W8\\_REG\[15:8\]](#), and so on.

The largest address points to [SPI\\_W15\\_REG\[31:24\]](#).

- To avoid any possible error in TX/RX data, such as TX data being sent more than once or RX data being overwritten, please make sure the registers are configured correctly.
- LP-SPI functions similarly, but uses LP-SPI registers and LP-SPI data buffers, as shown in Section [38.12.3](#).

### 38.5.6.2 CPU-Controlled Slave Transfer

In a CPU-controlled slave full-duplex or half-duplex transfer, the RX or TX data is saved to or sent from [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#), which are byte-addressable.

- In full-duplex communication, the address of [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) starts from 0 and is incremented by 1 on each byte transferred. If the data address is larger than 63, the data in [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) will be overwritten, same as the behaviors described in the master transfer when high part mode is disabled.

- In half-duplex communication, the *ADDR* value in [transmission format](#) is the start address of the RX or TX data, corresponding to the registers [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#). The RX or TX address is incremented by 1 on each byte transferred. If the address is larger than 63 (the highest byte address, i.e., [SPI\\_W15\\_REG\[31:24\]](#)), the data in [SPI\\_W8\\_REG~SPI\\_W15\\_REG](#) will be overwritten, same as the behaviors described in the master transfer when high part mode is enabled.

According to your applications, the registers [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#) can be used as:

- data buffers only
- data buffers and status buffers
- status buffers only

## 38.5.7 DMA-Controlled Data Transfer

### Note:

LP-SPI does not support this transfer. The description below is for GP-SPI only.

DMA-controlled transfer refers to the transfer in which the DMA RX module receives data and the DMA TX module sends data. This transfer is supported both as master and as slave.

A DMA-controlled transfer can be:

- a single transfer, consisting of only one transaction. GP-SPI supports this transfer both as master and as slave.
- a configurable segmented transfer, consisting of several transactions (segments). Only GP-SPI2 supports this transfer when working as a master. For more information, see [Section 38.5.9.5](#).
- a slave segmented transfer, consisting of several transactions (segments). GP-SPI supports this transfer only when working as a slave. For more information, see [Section 38.5.10.3](#).

A DMA-controlled transfer only needs to be triggered once by CPU. When such a transfer is triggered, data is transferred by the DMA engine from or to the DMA-linked memory, without CPU operation.

DMA-controlled transfer supports full-duplex communication, half-duplex communication and functions described in [Section 38.5.9](#) and [Section 38.5.10](#). Meanwhile, the DMA RX module is independent from the DMA TX module, which means that there are four kinds of full-duplex communications:

- Data is received in DMA-controlled mode and sent in DMA-controlled mode.
- Data is received in DMA-controlled mode but sent in CPU-controlled mode.
- Data is received in CPU-controlled mode but sent in DMA-controlled mode.
- Data is received in CPU-controlled mode and sent in CPU-controlled mode.

### 38.5.7.1 DMA Configuration

- Select a DMA channel *n* and configure DMA TX/RX descriptor. See [Chapter 3 GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).



- Set [AXI\\_DMA\\_INLINK\\_START\\_CH \$n\$](#)  or [AXI\\_DMA\\_OUTLINK\\_START\\_CH \$n\$](#)  to start DMA RX or TX engine, respectively.
- Before all the DMA TX buffer is used or the DMA TX engine is reset, if [AXI\\_DMA\\_OUTLINK\\_RESTART\\_CH \$n\$](#)  is set, a new TX buffer will be added to the end of the last TX buffer in use.
- DMA RX buffer is linked in the same way as the DMA TX buffer, by setting [AXI\\_DMA\\_INLINK\\_START\\_CH \$n\$](#)  or [AXI\\_DMA\\_INLINK\\_RESTART\\_CH \$n\$](#) .
- The TX and RX data lengths are determined by the configured DMA TX and RX buffer respectively, both of which are 0~32 KB.
- Initialize DMA inlink and outlink before DMA starts. The bits [SPI\\_DMA\\_RX\\_ENA](#) and [SPI\\_DMA\\_TX\\_ENA](#) in register [SPI\\_DMA\\_CONF\\_REG](#) should be set, otherwise the read/write data will be stored to/sent from the registers [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#).

When GP-SPI operating as master, if [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT\\_ENA](#) is set, then the interrupt [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#) will be triggered when one single transfer or one configurable segmented transfer is finished.

When GP-SPI operating as slave, if [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT\\_ENA](#) is set, then the interrupt [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#) will be triggered when one of the following conditions are met.

**Table 38.5-9. Interrupt Trigger Condition on GP-SPI Data Transfer as Slave**

| Transfer Type            | Control Bit <sup>1</sup> | Control Bit <sup>2</sup> | Condition   |
|--------------------------|--------------------------|--------------------------|---|
| Slave Single Transfer    | 0                        | 0                        | A single transfer is done.  |
|                          | 1                        | 0                        | A single transfer is done. Or the length of the received data is equal to ( <a href="#">SPI_MS_DATA_BITLEN</a> + 1 ).   |
| Slave Segmented Transfer | 0                        | 1                        | <a href="#">CMD7</a> or <a href="#">End_SEG_TRANS</a> is received correctly.  |
|                          | 1                        | 1                        | <a href="#">CMD7</a> or <a href="#">End_SEG_TRANS</a> is received correctly. Or the length of the received data is equal to ( <a href="#">SPI_MS_DATA_BITLEN</a> + 1 ). |

<sup>1</sup> [SPI\\_RX\\_EOF\\_EN](#)

<sup>2</sup> [SPI\\_DMA\\_SLV\\_SEG\\_TRANS\\_EN](#)

### 38.5.7.2 DMA TX/RX Buffer Length Control

It is recommended that the length of the configured DMA TX/RX buffer is equal to the length of actual data transferred.

- If the length of the configured DMA TX buffer is shorter than that of the actual data transferred, the extra data will be the same as the last transferred data. [SPI\\_OUTFIFO\\_EMPTY\\_ERR\\_INT](#) and [AXI\\_DMA\\_OUT\\_EOF\\_CH \$n\$ \\_INT](#) are triggered.
- If the length of the configured DMA TX buffer is longer than that of actual data transferred, the TX buffer is not fully used, and the remaining buffer will be used for the following transaction even if a new TX buffer is linked later. Please keep it in mind. Or save the unused data and reset the DMA.
- If the length of the configured DMA RX buffer is shorter than that of the actual data transferred, the extra data will be lost. [SPI\\_INFIFO\\_FULL\\_ERR\\_INT](#) and [SPI\\_TRANS\\_DONE\\_INT](#) are triggered. But [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH \$n\$ \\_INT](#) is not triggered.

- If the length of the configured DMA RX buffer is longer than that of the actual data transferred, the RX buffer is not fully used, and the remaining buffer is discarded. In the following transaction, a new linked buffer will be used directly.

### 38.5.8 Data Flow Control (Take GP-SPI as an Example)

CPU-controlled and DMA-controlled transfers are supported in GP-SPI both as master and as slave. CPU-controlled transfer means that data is transferred between registers [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) and the SPI device. DMA-controlled transfer means that data is transferred between the configured DMA TX/RX buffer and the SPI device. To select between the two transfer types, configure [SPI\\_DMA\\_RX\\_ENA](#) and [SPI\\_DMA\\_TX\\_ENA](#) before the transfer starts.

#### 38.5.8.1 GP-SPI Functional Blocks

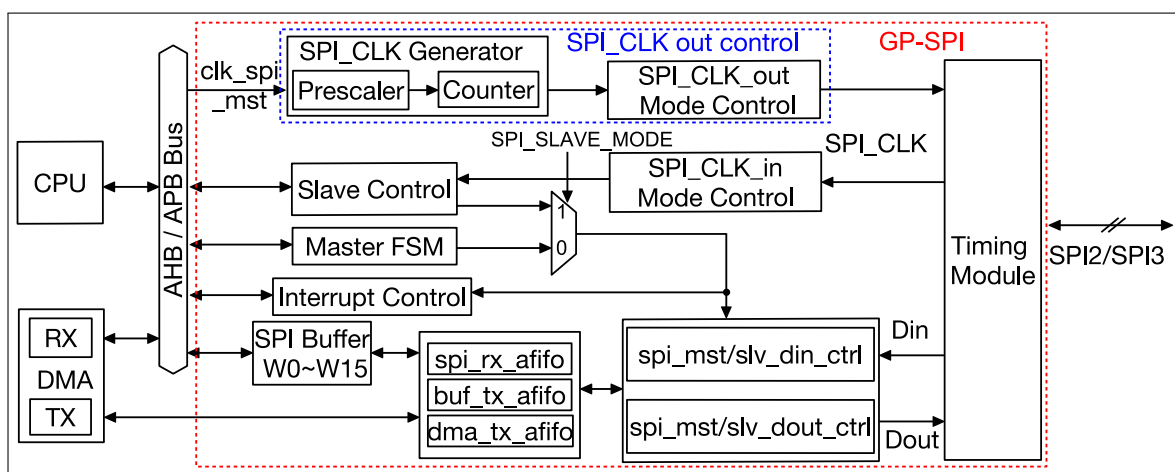


Figure 38.5-2. GP-SPI Functional Blocks

Figure 38.5-2 shows the main functional blocks in GP-SPI, including:

- **Master FSM:** all the features supported in GP-SPI as master are controlled by this state machine together with register configuration.
- **SPI Buffer:** [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#). See Figure 38.5-1. The data in CPU-controlled transfer is prepared in this buffer.
- **Timing Module:** captures data on SPI2/SPI3 bus.
- **spi\_mst/slv\_din\_ctrl** and **spi\_mst/slv\_dout\_ctrl:** converts the TX/RX data into bytes.
- **spi\_rx\_afifo:** stores the received data.
- **buf\_tx\_afifo:** stores the data to send.
- **dma\_tx\_afifo:** stores the data from DMA.
- **clk\_spi\_mst:** this clock is the module clock of GP-SPI and is used in GP-SPI as master to generate SPI\_CLK signal for data transfer and for slaves.
- **SPI\_CLK Generator:** generates SPI\_CLK by dividing clk\_spi\_mst. The divider is determined by [SPI\\_CLKCNT\\_N](#) and [SPI\\_CLKDIV\\_PRE](#).

- SPI\_CLK\_out Mode Control: outputs the SPI\_CLK signal for data transfer and for slaves.
- SPI\_CLK\_in Mode Control: captures the SPI\_CLK signal from SPI master when GP-SPI works as a slave.

### 38.5.8.2 Data Flow Control as Master

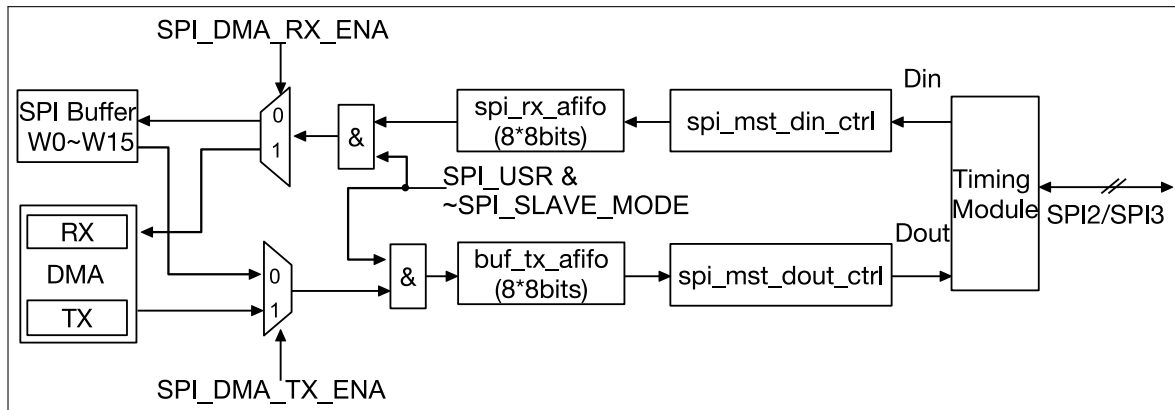


Figure 38.5-3. Data Flow Control in GP-SPI as Master

Figure 38.5-3 shows the data flow of GP-SPI as master. Its control logic is as follows:

- RX data: data bits in SPI2/SPI3 bus is captured by *Timing Module*, converted into bytes by *spi\_mst\_din\_ctrl* module, then buffered in *spi\_rx\_afifo*, and finally stored in corresponding addresses according to the transfer types.
  - CPU-controlled transfer: the data is stored to registers [SPI\\_W0\\_REG ~SPI\\_W15\\_REG](#).
  - DMA-controlled transfer: the data is stored to DMA RX buffer.
- TX data: the TX data is from corresponding addresses according to transfer modes and is saved to *buf\_tx\_afifo*.
  - CPU-controlled transfer: TX data is from [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#).
  - DMA-controlled transfer: TX data is from DMA TX buffer.

The data in *buf\_tx\_afifo* is sent out to *Timing Module* in 1/2/4/(8)-bit modes, controlled by GP-SPI state machine. The *Timing Module* can be used for timing compensation. For more information, see Section [38.8](#).

### 38.5.8.3 Data Flow Control as Slave

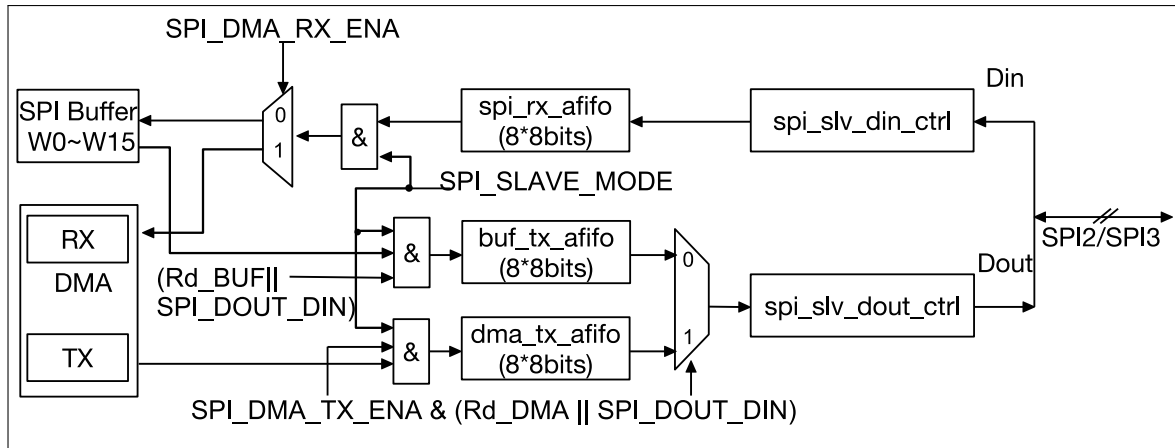


Figure 38.5-4. Data Flow Control in GP-SPI as Slave

Figure 38.5-4 shows the data flow of GP-SPI as slave. Its control logic is as follows:

- In CPU/DMA-controlled full-/half-duplex transfer, when an external SPI master starts the SPI transfer, data on the SPI2/SPI3 bus is captured, converted into bytes by the *spi\_slv\_din\_ctrl* module, and then is stored in *spi\_rx\_afifo*.
  - In CPU-controlled full-duplex transfer, the received data in *spi\_rx\_afifo* will be later stored into registers *SPI\_WO\_REG~SPI\_W15\_REG*, successively.
  - In half-duplex *Wr\_BUF* transfer, when the value of address (*SLV\_ADDR[7:0]*) is received, the received data in *spi\_rx\_afifo* will be stored in the related address of registers *SPI\_WO\_REG~SPI\_W15\_REG*.
  - In DMA-controlled full-duplex transfer or in half-duplex *Wr\_DMA* transfer, the received data in *spi\_rx\_afifo* will be stored in the configured DMA RX buffer.
- In CPU-controlled full-/half-duplex transfer, the data to send is stored in *buf\_tx\_afifo*. In DMA-controlled full-/half-duplex transfer, the data to send is stored in *dma\_tx\_afifo*. Therefore, *Rd\_BUF* transaction controlled by CPU and *Rd\_DMA* transaction controlled by DMA can be done in one slave segmented transfer.
  - In CPU-controlled full-duplex transfer, when *SPI\_SLAVE\_MODE* and *SPI\_DOUTDIN* are set and *SPI\_DMA\_TX\_ENA* is cleared, the data in *SPI\_WO\_REG~SPI\_W15\_REG* will be stored into *buf\_tx\_afifo*.
  - In CPU-controlled half-duplex transfer, when *SPI\_SLAVE\_MODE* is set, *SPI\_DOUTDIN* is cleared, *Rd\_BUF* command and *SLV\_ADDR[7:0]* are received, the data started from the related address of *SPI\_WO\_REG~SPI\_W15\_REG* will be stored into *buf\_tx\_afifo*.
  - In DMA-controlled full-duplex transfer, when *SPI\_SLAVE\_MODE*, *SPI\_DOUTDIN*, and *SPI\_DMA\_TX\_ENA* are set, the data in the configured DMA TX buffer will be stored into *dma\_tx\_afifo*.
  - In DMA-controlled half-duplex transfer, when *SPI\_SLAVE\_MODE* is set, *SPI\_DOUTDIN* is cleared, and *Rd\_DMA* command is received, the data in the configured DMA TX buffer will be stored into *dma\_tx\_afifo*.

The data in *buf\_tx\_afifo* or *dma\_tx\_afifo* is sent out by *splv\_dout\_ctrl* module in 1/2/4(8)-bit modes.

## 38.5.9 GP-SPI as a Master

GP-SPI can be configured as a SPI master by clearing the bit [SPI\\_SLAVE\\_MODE](#) in [SPI\\_SLAVE\\_REG](#). In this operation mode, GP-SPI provides clock signal (the divided clock from GP-SPI module clock) and CS signal.

### 38.5.9.1 State Machine

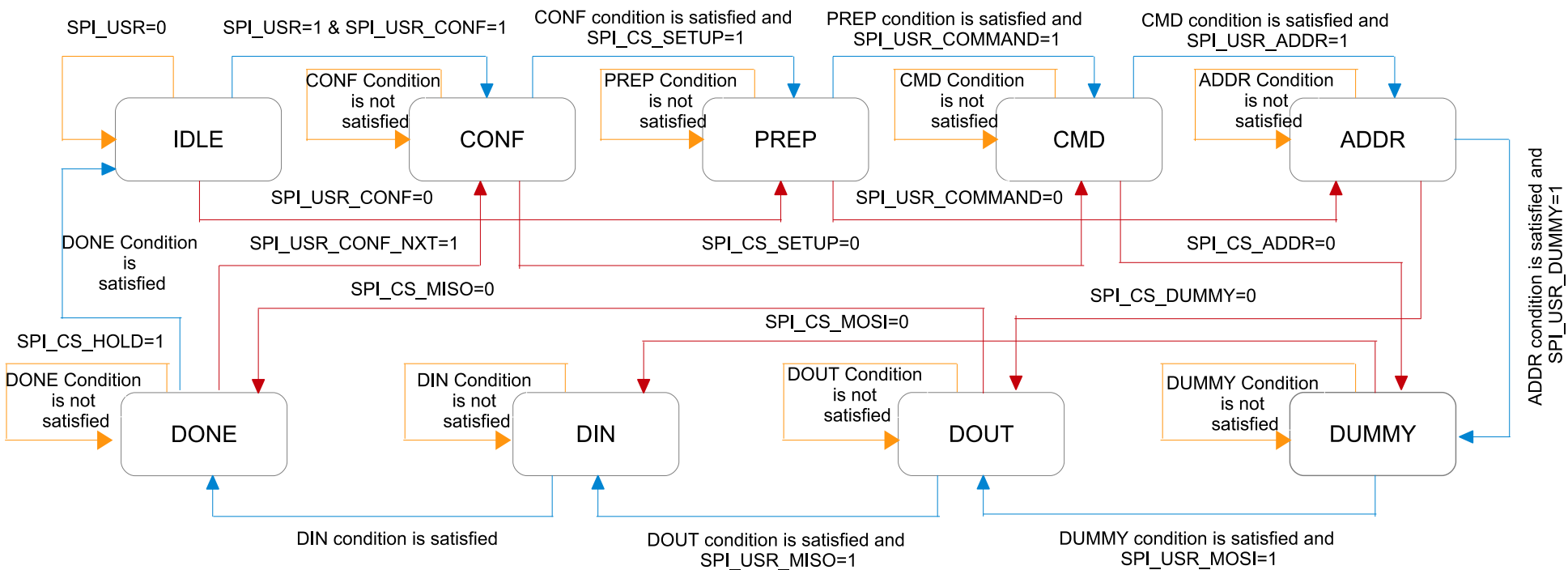
When GP-SPI works as a master, the state machine controls GP-SPI's various states during data transfer, including configuration (CONF), preparation (PREP), command (CMD), address (ADDR), dummy (DUMMY), data out (DOUT), and data in (DIN) states. GP-SPI is mainly used to access 1/2/4/8-bit SPI devices, such as flash and external RAM, thus the naming of GP-SPI states keeps consistent with the sequence naming of flash and external RAM. The meaning of each state is described as follows and Figure [38.5-5](#) shows the workflow of GP-SPI state machine.

1. IDLE: GP-SPI is not active or is operating as a slave.
2. CONF (valid for GP-SPI2 only): only used in DMA-controlled [configurable segmented transfer](#). Set [SPI\\_USR](#) and [SPI\\_USR\\_CONF](#) to enable this state. If this state is not enabled, it means the current transfer is a single transfer.
3. PREP: prepare an SPI transaction and control SPI CS setup time. Set [SPI\\_USR](#) and [SPI\\_CS\\_SETUP](#) to enable this state.
4. CMD: send command sequence. Set [SPI\\_USR](#) and [SPI\\_USR\\_COMMAND](#) to enable this state.
5. ADDR: send address sequence. Set [SPI\\_USR](#) and [SPI\\_USR\\_ADDR](#) to enable this state.
6. DUMMY (wait cycle): send dummy sequence. set [SPI\\_USR](#) and [SPI\\_USR\\_DUMMY](#) to enable this state.
7. DATA: transfer data.
  - DOUT: send data sequence. Set [SPI\\_USR](#) and [SPI\\_USR\\_MOSI](#) to enable this state.
  - DIN: receive data sequence. Set [SPI\\_USR](#) and [SPI\\_USR\\_MISO](#) to enable this state.
8. DONE: control SPI CS hold time. Set [SPI\\_USR](#) to enable this state.

#### Note:

To start this state machine, set [SPI\\_USR](#) first. [SPI\\_MST\\_FD\\_WAIT\\_DMA\\_TX\\_DATA](#) controls when [SPI\\_USR](#) takes effect:

- 0: the configured state takes effect immediately after [SPI\\_USR](#) and other control registers are configured.
- 1: if DOUT state is configured, the [SPI\\_USR](#) and other control registers will take effect, and the state machine will start, only when the data is ready in *buf\_tx\_afifo*.



Legend to state flow:

- —: indicates corresponding state condition is not satisfied; repeats current state.
- —: corresponding registers are set and conditions are satisfied; goes to next state.
- —: state registers are not set; skips one or more following states, depending on the registers of the following states are set or not.

Explanation to the conditions listed in the figure above:

- CONF condition:  $\text{gpc}[17:0] \geq \text{SPI\_CONF\_BITLEN}[17:0]$
- PREP condition:  $\text{gpc}[4:0] \geq \text{SPI\_CS\_SETUP\_TIME}[4:0]$
- CMD condition:  $\text{gpc}[3:0] \geq \text{SPI\_USR\_COMMAND\_BITLEN}[3:0]$
- ADDR condition:  $\text{gpc}[4:0] \geq \text{SPI\_USR\_ADDR\_BITLEN}[4:0]$
- DUMMY condition:  $\text{gpc}[7:0] \geq \text{SPI\_USR\_DUMMY\_CYCLELEN}[7:0]$
- DOUT condition:  $\text{gpc}[17:0] \geq \text{SPI\_MS\_DATA\_BITLEN}[17:0]$
- DIN condition:  $\text{gpc}[17:0] \geq \text{SPI\_MS\_DATA\_BITLEN}[17:0]$
- DONE condition:  $(\text{gpc}[4:0] \geq \text{SPI\_CS\_HOLD\_TIME}[4:0] \parallel \text{SPI\_CS\_HOLD} == 1'b0)$

A counter ( $\text{gpc}[17:0]$ ) is used in the state machine to control the cycle length of each state. The states CONF, PREP, CMD, ADDR, DUMMY, DOUT, and DIN can be enabled or disabled independently. The cycle length of each state can also be configured independently.

### 38.5.9.2 Register Configuration for State and Bit Mode Control

#### Introduction

The registers, related to GP-SPI state control, are listed in Table 38.5-10. Users can enable QPI mode for GP-SPI by setting the bit [SPI\\_QPI\\_MODE](#) in register [SPI\\_USER\\_REG](#).

Table 38.5-10. Registers Used for State Control in 1/2/4/8-bit Modes

| State | Control Registers for 1-bit Mode<br>SPI2/SPI3 Bus                  | Control Registers for 2-bit Mode<br>SPI2/SPI3 Bus                                   | Control Registers for 4-bit Mode<br>SPI2/SPI3 Bus                                   | Control Registers for 8-bit Mode<br>SPI2 Bus                                       |
|-------|--|---|---|--|
| CMD   | SPI_USR_COMMAND_VALUE<br>SPI_USR_COMMAND_BITLEN<br>SPI_USR_COMMAND | SPI_USR_COMMAND_VALUE<br>SPI_USR_COMMAND_BITLEN<br>SPI_FCMD_DUAL<br>SPI_USR_COMMAND | SPI_USR_COMMAND_VALUE<br>SPI_USR_COMMAND_BITLEN<br>SPI_FCMD_QUAD<br>SPI_USR_COMMAND | SPI_USR_COMMAND_VALUE<br>SPI_USR_COMMAND_BITLEN<br>SPI_FCMD_OCT<br>SPI_USR_COMMAND |
| ADDR  | SPI_USR_ADDR_VALUE<br>SPI_USR_ADDR_BITLEN<br>SPI_USR_ADDR          | SPI_USR_ADDR_VALUE<br>SPI_USR_ADDR_BITLEN<br>SPI_USR_ADDR<br>SPI_FADDR_DUAL         | SPI_USR_ADDR_VALUE<br>SPI_USR_ADDR_BITLEN<br>SPI_USR_ADDR<br>SPI_FADDR_QUAD         | SPI_USR_ADDR_VALUE<br>SPI_USR_ADDR_BITLEN<br>SPI_USR_ADDR SPI_FADDR_OCT            |
| DUMMY | SPI_USR_DUMMY_CYCLELEN<br>SPI_USR_DUMMY                            | SPI_USR_DUMMY_CYCLELEN<br>SPI_USR_DUMMY   | SPI_USR_DUMMY_CYCLELEN<br>SPI_USR_DUMMY   | SPI_USR_DUMMY_CYCLELEN<br>SPI_USR_DUMMY  |
| DIN   | SPI_USR_MISO<br>SPI_MS_DATA_BITLEN                                 | SPI_USR_MISO<br>SPI_MS_DATA_BITLEN<br>SPI_FREAD_DUAL                                | SPI_USR_MISO<br>SPI_MS_DATA_BITLEN<br>SPI_FREAD_QUAD                                | SPI_USR_MISO<br>SPI_MS_DATA_BITLEN<br>SPI_FREAD_OCT                                |
| DOUT  | SPI_USR_MOSI<br>SPI_MS_DATA_BITLEN                                 | SPI_USR_MOSI<br>SPI_MS_DATA_BITLEN<br>SPI_FWRITE_DUAL                               | SPI_USR_MOSI<br>SPI_MS_DATA_BITLEN<br>SPI_FWRITE_QUAD                               | SPI_USR_MOSI<br>SPI_MS_DATA_BITLEN<br>SPI_FWRITE_OCT                               |



As shown in Table 38.5-10, the registers in each cell should be configured to set the SPI2/SPI3 bus to corresponding bit mode, i.e., the mode shown in the table header, at a specific state (corresponding to the first column).

### Configuration

For instance, when GP-SPI2 reads data, and

- CMD is in 1-bit mode
- ADDR is in 2-bit mode
- DUMMY lasts for 8 clock cycles
- DIN is in 4-bit mode

The register configuration can be as follows:

1. Configure CMD state related registers.
  - Configure the required command value in [SPI\\_USR\\_COMMAND\\_VALUE](#).
  - Configure command bit length in [SPI\\_USR\\_COMMAND\\_BITLEN](#). [SPI\\_USR\\_COMMAND\\_BITLEN](#) = expected bit length - 1.
  - Set [SPI\\_USR\\_COMMAND](#).
  - Clear [SPI\\_FCMD\\_DUAL](#), [SPI\\_FCMD\\_QUAD](#), and [SPI\\_FCMD\\_OCT](#).
2. Configure ADDR state related registers.
  - Configure the required address value in [SPI\\_USR\\_ADDR\\_VALUE](#).
  - Configure address bit length in [SPI\\_USR\\_ADDR\\_BITLEN](#). [SPI\\_USR\\_ADDR\\_BITLEN](#) = expected bit length - 1.
  - Set [SPI\\_USR\\_ADDR](#) and [SPI\\_FADDR\\_DUAL](#).
  - Clear [SPI\\_FADDR\\_QUAD](#) and [SPI\\_FCMD\\_OCT](#).
3. Configure DUMMY state related registers.
  - Configure DUMMY cycles in [SPI\\_USR\\_DUMMY\\_CYCLELEN](#). [SPI\\_USR\\_DUMMY\\_CYCLELEN](#) = expected clock cycles - 1.
  - Set [SPI\\_USR\\_DUMMY](#).
4. Configure DIN state related registers.
  - Configure read data bit length in [SPI\\_MS\\_DATA\\_BITLEN](#). [SPI\\_MS\\_DATA\\_BITLEN](#) = expected bit length - 1.
  - Set [SPI\\_FREAD\\_QUAD](#) and [SPI\\_USR\\_MISO](#).
  - Clear [SPI\\_FREAD\\_DUAL](#) and [SPI\\_FCMD\\_OCT](#).
  - Configure DMA for DMA-controlled transfer. For CPU controlled transfer, no action is needed.
5. Clear [SPI\\_USR\\_MOSI](#).
6. Set [SPI\\_DMA\\_AFIFO\\_RST](#), [SPI\\_BUF\\_AFIFO\\_RST](#), and [SPI\\_RX\\_AFIFO\\_RST](#) to reset these buffers.
7. Set [SPI\\_USR](#) to start GP-SPI2 transfer.

**Note:**

Updating the configuration when the GP-SPI works as master described in this and subsequent sections requires to set [SPI\\_UPDATE](#) accordingly to synchronize the configuration from AHB\_CLK domain to clk\_spi\_mst domain. For more detailed configuration, see the sections above. No operation is required when the GP-SPI works as slave.

When writing data (DOUT state), [SPI\\_USR\\_MOSI](#) should be configured instead, while [SPI\\_USR\\_MISO](#) should be cleared. The output data bit length is the value of [SPI\\_MS\\_DATA\\_BITLEN](#) + 1. Output data should be configured in GP-SPI2 data buffer ([SPI\\_WO\\_REG](#)~[SPI\\_W15\\_REG](#)) for CPU-controlled transfer, or DMA TX buffer for DMA-controlled transfer.

Pay special attention to the command value in [SPI\\_USR\\_COMMAND\\_VALUE](#) and to address value in [SPI\\_USR\\_ADDR\\_VALUE](#).

The configuration of command value is as follows:

**Table 38.5-11. Sending Sequence of Command Value**

| COMMAND_BITLEN <sup>1</sup> | COMMAND_VALUE <sup>2</sup> | BIT_ORDER <sup>3</sup> | Sending Sequence of Command Value   |
|-----------------------------|----------------------------|------------------------|---|
| 0~7                         | [7:0]                      | 1                      | <a href="#">COMMAND_VALUE</a> [ <a href="#">COMMAND_BITLEN</a> :0] is sent first.   |
|                             |                            | 0                      | <a href="#">COMMAND_VALUE</a> [7:7- <a href="#">COMMAND_BITLEN</a> ] is sent first.   |
| 8~15                        | [15:0]                     | 1                      | <a href="#">COMMAND_VALUE</a> [7:0] is sent first, and then <a href="#">COMMAND_VALUE</a> [ <a href="#">COMMAND_BITLEN</a> :8].     |
|                             |                            | 0                      | <a href="#">COMMAND_VALUE</a> [7:0] is sent first, and then <a href="#">COMMAND_VALUE</a> [15:15- <a href="#">COMMAND_BITLEN</a> ]. |

<sup>1</sup> [SPI\\_USR\\_COMMAND\\_BITLEN](#): this field is used to configure the bit length of the command.

<sup>2</sup> [SPI\\_USR\\_COMMAND\\_VALUE](#): command value is written into this field. For which part of this field is used, see the table above.

<sup>3</sup> [SPI\\_WR\\_BIT\\_ORDER](#): 0: LSB first; 1: MSB first.

The configuration of address value is as follows:

**Table 38.5-12. Sending Sequence of Address Value**

| ADDR_BITLEN <sup>1</sup> | ADDR_VALUE <sup>2</sup> | BIT_ORDER <sup>3</sup> | Sending Sequence of Address Value  |
|--------------------------|-------------------------|------------------------|--|
| 0~7                      | [31:24]                 | 1                      | <a href="#">ADDR_VALUE</a> [ <a href="#">ADDR_BITLEN</a> + 24:24] is sent first.   |
|                          |                         | 0                      | <a href="#">ADDR_VALUE</a> [31:31- <a href="#">ADDR_BITLEN</a> ] is sent first.  |
| 8~15                     | [31:16]                 | 1                      | <a href="#">ADDR_VALUE</a> [31:24] is sent first, and then <a href="#">ADDR_VALUE</a> [ <a href="#">ADDR_BITLEN</a> + 8:16]. |
|                          |                         | 0                      | <a href="#">ADDR_VALUE</a> [31:24] is sent first, and then <a href="#">ADDR_VALUE</a> [23:31- <a href="#">ADDR_BITLEN</a> ]. |
| 16~23                    | [31:8]                  | 1                      | <a href="#">ADDR_VALUE</a> [31:16] is sent first, and then <a href="#">ADDR_VALUE</a> [ <a href="#">ADDR_BITLEN</a> -8:8].   |

|       |        |   |   |
|-------|--------|---|---|
|       |        | 0 | <a href="#">ADDR_VALUE[31:16]</a> is sent first, and then <a href="#">ADDR_VALUE[15:31-ADDR_BITLEN]</a> . |
| 24~31 | [31:0] | 1 | <a href="#">ADDR_VALUE[31:8]</a> is sent first, and then <a href="#">ADDR_VALUE[ADDR_BITLEN-24:0]</a> .   |
|       |        | 0 | <a href="#">ADDR_VALUE[31:8]</a> is sent first, and then <a href="#">ADDR_VALUE[7:31-ADDR_BITLEN]</a> .   |

<sup>1</sup> [SPI\\_USR\\_ADDR\\_BITLEN](#): this field is used to configure the bit length of the address.

<sup>2</sup> [SPI\\_USR\\_ADDR\\_VALUE](#): address value is written into this field. For which part of this field is used, see the table above.

<sup>3</sup> [SPI\\_WR\\_BIT\\_ORDER](#): 0: LSB first; 1: MSB first.

### 38.5.9.3 Full-Duplex Communication (1-bit Mode Only)

#### Introduction

GP-SPI supports SPI full-duplex communication. In this mode, SPI master provides CLK and CS signals, exchanging data with SPI slave in 1-bit mode via MOSI (SPI2D/SPI3\_D, sending) and MISO (SPI2Q/SPI3\_Q, receiving) at the same time. To enable this communication mode, set the bit [SPI\\_DOUTDIN](#) in register [SPI\\_USER\\_REG](#). Figure 38.5-6 illustrates the connection of GP-SPI2 with its slave in full-duplex communication.

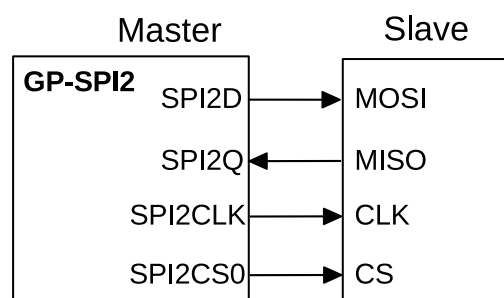


Figure 38.5-6. Full-Duplex Communication Between GP-SPI2 Master and a Slave

In full-duplex communication, the behavior of states CMD, ADDR, DUMMY, DOUT and DIN are configurable. Usually, the states CMD, ADDR and DUMMY are not used in this communication. The bit length of transferred data is configured in [SPI\\_MS\\_DATA\\_BITLEN](#). The actual bit length used in communication equals to ([SPI\\_MS\\_DATA\\_BITLEN](#) + 1).

#### Configuration (Take GP-SPI2 as an example)

To start a data transfer, follow the steps below:

- Configure the IO path via IO MUX or GPIO matrix between GP-SPI2 and an external SPI device.
- Configure AHB clock (AHB\_CLK, see Chapter 9 [Reset and Clock](#)) and module clock (clk\_spi\_mst) for the GP-SPI2 module.
- Set [SPI\\_DOUTDIN](#) and clear [SPI\\_SLAVE\\_MODE](#), to enable master full-duplex communication.
- Configure GP-SPI2 registers listed in Table 38.5-10.
- Configure SPI CS setup time and hold time according to Section 38.6.

- Set the property of SPI2CLK according to Section 38.7.
- Prepare data according to the selected transfer type:
  - In CPU-controlled MOSI transfer, prepare data in registers [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#).
  - In DMA-controlled transfer,
    - \* configure [SPI\\_DMA\\_TX\\_ENA/SPI\\_DMA\\_RX\\_ENA](#),
    - \* configure DMA TX/RX link,
    - \* and start DMA TX/RX engine, as described in Section 38.5.7 and Section 38.5.8.
- Configure interrupts and wait for SPI slave to get ready for transfer.
- Set [SPI\\_DMA\\_AFIFO\\_RST](#), [SPI\\_BUF\\_AFIFO\\_RST](#), and [SPI\\_RX\\_AFIFO\\_RST](#) to reset these buffers.
- Set [SPI\\_USR](#) in register [SPI\\_CMD\\_REG](#) to start the transfer and wait for the configured interrupts.

#### 38.5.9.4 Half-Duplex Communication (1/2/4/(8)-bit Mode)

##### Introduction

In this mode, GP-SPI provides CLK and CS signals. Only one side (SPI master or slave) can send data at a time, while the other side receives the data. To enable this communication mode, clear the bit [SPI\\_DOUTDIN](#) in register [SPI\\_USER\\_REG](#). The standard format of SPI half-duplex communication is CMD + [ADDR +] [DUMMY +] [DOUT or DIN]. The states ADDR, DUMMY, DOUT, and DIN are optional, and can be disabled or enabled independently.

As described in Section 38.5.9.2, the properties of GP-SPI states: CMD, ADDR, DUMMY, DOUT and DIN, such as cycle length, value, and parallel bus bit mode, can be set independently. For the register configuration, see Table 38.5-10.

The detailed properties of half-duplex GP-SPI are as follows:

1. CMD: 0~16 bits, master output, slave input.
2. ADDR: 0~32 bits, master output, slave input.
3. DUMMY: 0~256 SPI2CLK/SPI3\_CLK cycles, master output, slave input.
4. DOUT: 0~512 bits (64 bytes) in CPU-controlled transfer, 0~256 Kbits (32 KB) in DMA-controlled single transfer, and unlimited length in DMA-controlled configurable segmented transfer, master output, slave input.
5. DIN: 0~512 bits (64 bytes) in CPU-controlled transfer, 0~256 Kbits (32 KB) in DMA-controlled single transfer, and unlimited length in DMA-controlled configurable segmented transfer, slave output, master input.

GP-SPI2 also supports Double Transfer Rate (DTR) in 1/2/4/8-bit modes, in which data is sent and received at the rising and the falling edges of SPI clock:

- If [SPI\\_CMD\\_DTR\\_EN](#) is set, the CMD value will be sent in DTR mode; otherwise CMD phase will be in Single Transfer Rate (STR) mode.
- If [SPI\\_ADDR\\_DTR\\_EN](#) is set, the ADDR value will be sent in DTR mode; otherwise ADDR phase will be in STR mode.

- If [SPI\\_DATA\\_DTR\\_EN](#) is set, the input data in state DIN or output data in state DOUT will be sent in DTR mode; otherwise the data will be in STR mode.

The control bits [SPI\\_CMD\\_DTR\\_EN](#), [SPI\\_ADDR\\_DTR\\_EN](#), and [SPI\\_DATA\\_DTR\\_EN](#) can be configured independently, which means CMD in STR mode, ADDR and DOUT or DIN in DTR mode are supported.

GP-SPI2 can only output SPI2DQS signal, but can not receive the signal. Therefore, only flash or external RAM working in fixed dummy mode (dummy cycles in a read sequence is fixed) are supported.

#### Configuration (Take GP-SPI2 as an example)

The register configuration can be as follows:

1. Configure the IO path via HP IO MUX or HP GPIO matrix between GP-SPI2 and an external SPI device.
2. Configure AHB clock (AHB\_CLK) and module clock (clk\_spi\_mst) for the GP-SPI2 module.
3. Clear [SPI\\_DOUTDIN](#) and [SPI\\_SLAVE\\_MODE](#), to enable master half-duplex communication.
4. Configure GP-SPI2 registers listed in Table [38.5-10](#).
5. Configure SPI CS setup time and hold time according to Section [38.6](#).
6. Set the property of SPI2CLK according to Section [38.7](#).
7. Prepare data according to the selected transfer type:
  - In CPU-controlled MOSI transfer, prepare data in registers [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#).
  - In DMA-controlled transfer,
    - configure [SPI\\_DMA\\_TX\\_ENA/SPI\\_DMA\\_RX\\_ENA](#),
    - configure DMA TX/RX link,
    - and start DMA TX/RX engine, as described in Section [38.5.7](#) and Section [38.5.8](#).
8. Configure interrupts and wait for SPI slave to get ready for transfer.
9. Set [SPI\\_DMA\\_AFIFO\\_RST](#), [SPI\\_BUF\\_AFIFO\\_RST](#), and [SPI\\_RX\\_AFIFO\\_RST](#) to reset these buffers.
10. Set [SPI\\_USR](#) in register [SPI\\_CMD\\_REG](#) to start the transfer and wait for the configured interrupts.

#### Application Example (Take GP-SPI2 as an example)

The following example shows how GP-SPI2 accesses flash and external RAM in master half-duplex communication.

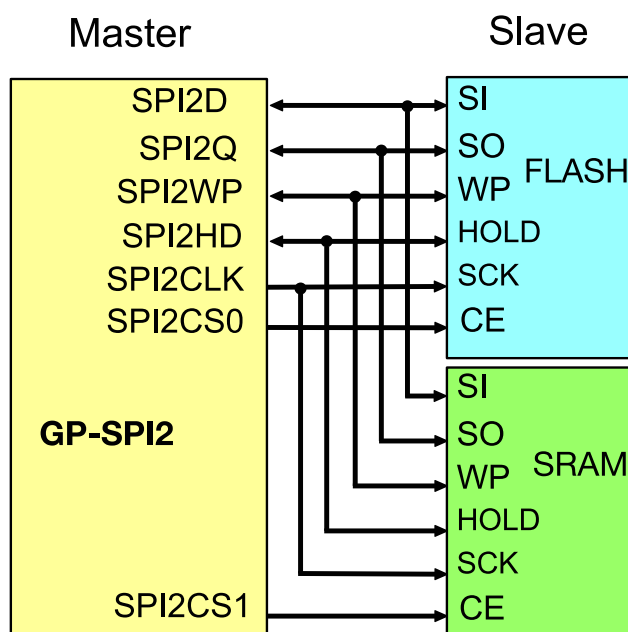


Figure 38.5-7. Connection of GP-SPI2 to Flash and External RAM in 4-bit Mode

Figure 38.5-8 indicates GP-SPI2 Quad I/O Read sequence according to standard flash specification. Other GP-SPI2 command sequences are implemented in accordance with the requirements of SPI slaves.

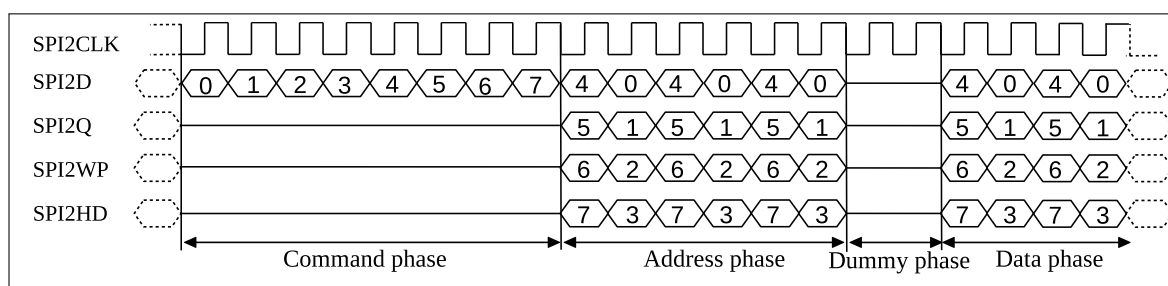


Figure 38.5-8. SPI Quad I/O Read Command Sequence Sent by GP-SPI2 to Flash

### 38.5.9.5 DMA-Controlled Configurable Segmented Transfer

#### Note:

- LP-SPI and GP-SPI3 do not support DMA-controlled configurable segmented transfer.
- Note that there is no separate section on how to configure a single transfer as master, since the CONF state of a configurable segmented transfer can be skipped to implement a single transfer.

#### Introduction

When GP-SPI2 works as a master, it provides a feature named configurable segmented transfer controlled by DMA.

A DMA-controlled transfer as master can be:

- a single transfer, consisting of only one transaction;
- or a configurable segmented transfer, consisting of several transactions (segments).

In a configurable segmented transfer, the registers of each single transaction (segment) are configurable. This feature enables GP-SPI2 to do as many transactions (segments) as configured after such transfer is triggered once by the CPU. Figure 38.5-9 shows how this feature works.

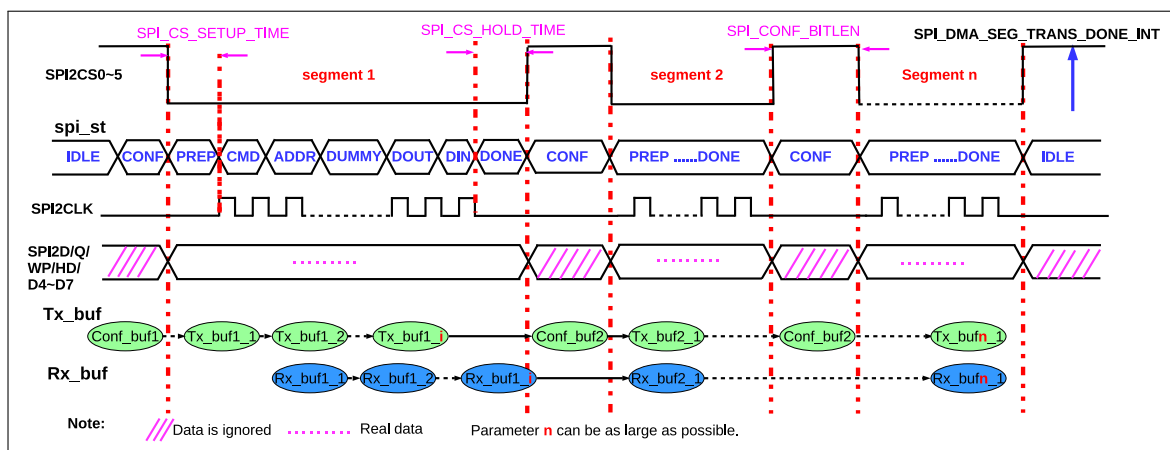


Figure 38.5-9. Configurable Segmented Transfer as Master

As shown in Figure 38.5-9, the registers for one transaction (segment *n*) can be reconfigured by GP-SPI2 hardware according to the content in its Conf\_buf*n* during the CONF state, before this segment starts.

It is recommended to provide separate DMA CONF links and CONF buffers (Conf\_buf*i* in Figure 38.5-9) for each CONF state. A DMA TX link is used to connect all the CONF buffers and TX data buffers (Tx\_buf*i* in Figure 38.5-9) into a chain. Hence, the behavior of the SPI2 bus in each segment can be controlled independently.

For example, in a configurable segmented transfer, its segment *i*, segment *j*, and segment *k* can be configured to full-duplex, half-duplex MISO, and half-duplex MOSI, respectively. *i*, *j*, and *k* represent different segment numbers.

Meanwhile, the state of GP-SPI2, the data length and cycle length of the SPI2 bus, and the behavior of the DMA, can be configured independently for each segment. When this whole DMA-controlled transfer (consisting of several segments) has finished, a GP-SPI2 interrupt, SPI\_DMA\_SEG\_TRANS\_DONE\_INT, is triggered.

### Configuration

1. Configure the IO path via HP IO MUX or HP GPIO matrix between GP-SPI2 and an external SPI device.
2. Configure AHB clock (AHB\_CLK) and module clock (clk\_spi\_mst) for the GP-SPI2 module.
3. Clear SPI\_DOUTDIN and SPI\_SLAVE\_MODE, to enable master half-duplex communication.
4. Configure GP-SPI2 registers listed in Table 38.5-10.
5. Configure SPI CS setup time and hold time according to Section 38.6.
6. Set the property of SPI2CLK according to Section 38.7.
7. Prepare descriptors for DMA CONF buffer and TX data (optional) for each segment. Chain the descriptors of CONF buffer and TX buffers of several segments into one linked list.
8. Similarly, prepare descriptors for RX buffers for each segment and chain them into one linked list.

9. Configure all the needed CONF buffers, TX buffers and RX buffers, respectively for each segment before this DMA-controlled transfer begins.
10. Point [AXI\\_DMA\\_OUTLINK\\_ADDR\\_CH\*n\*](#) to the head address of the CONF and TX buffer descriptor linked list, and then set [AXI\\_DMA\\_OUTLINK\\_START\\_CH\*n\*](#) to start the TX DMA.
11. Clear the bit [SPI\\_RX\\_EOF\\_EN](#) in register [SPI\\_DMA\\_CONF\\_REG](#). Point [AXI\\_DMA\\_INLINK\\_ADDR\\_CH\*n\*](#) to the head address of the CONF and RX buffer descriptor linked list, and then set [AXI\\_DMA\\_INLINK\\_START\\_CH\*n\*](#) to start the RX DMA.
12. Set [SPI\\_USR\\_CONF](#) to enable CONF state.
13. Set [SPI\\_DMA\\_SEG\\_TRANS\\_DONE\\_INT\\_ENA](#) to enable the [SPI\\_DMA\\_SEG\\_TRANS\\_DONE\\_INT](#) interrupt. Configure other interrupts if needed according to Section 38.11.
14. Wait for all the slaves to get ready for transfer.
15. Set [SPI\\_DMA\\_AFIFO\\_RST](#), [SPI\\_BUF\\_AFIFO\\_RST](#), and [SPI\\_RX\\_AFIFO\\_RST](#) to reset these buffers.
16. Set [SPI\\_USR](#) to start this DMA-controlled transfer.
17. Wait for [SPI\\_DMA\\_SEG\\_TRANS\\_DONE\\_INT](#) interrupt, which means this transfer has finished and the data has been stored into corresponding memory.

**Note:**

Prepare the data to send for each segment in its PREP state. Shall ensure that:

$$(SPI\_CS\_SETUP\_TIME + 1) \times T_{SPI\_CLK} \geq 4 \times (T_{AHB\_CLK} + T_{clk\_spi\_mst})$$

### Configuration of CONF Buffer and Magic Value

In a configurable segmented transfer, only registers which change from the last transaction (segment) need to be re-configured to new values in CONF state. The configuration of other registers can be skipped (i.e., kept the same) to save time and chip resources.

The first word in DMA CONF buffer *i*, called SPI\_BIT\_MAP\_WORD, defines whether given GP-SPI2 register is to be updated or not in segment *i*. The relation of SPI\_BIT\_MAP\_WORD and GP-SPI2 registers to update can be seen in Table 38.5-13 Bitmap (BM) Table. If a bit in the BM table is set to 1, its corresponding register value will be updated in this segment. Otherwise, if some registers should be kept from being changed, the related bits should be set to 0.

**Table 38.5-13. BM Table for CONF State**

| BM Bit | Register                        | BM Bit | Register                            |
|--------|---------------------------------|--------|-------------------------------------|
| 0      | <a href="#">SPI_ADDR_REG</a>    | 7      | <a href="#">SPI_MISC_REG</a>        |
| 1      | <a href="#">SPI_CTRL_REG</a>    | 8      | <a href="#">SPI_DIN_MODE_REG</a>    |
| 2      | <a href="#">SPI_CLOCK_REG</a>   | 9      | <a href="#">SPI_DIN_NUM_REG</a>     |
| 3      | <a href="#">SPI_USER_REG</a>    | 10     | <a href="#">SPI_DOUT_MODE_REG</a>   |
| 4      | <a href="#">SPI_USER1_REG</a>   | 11     | <a href="#">SPI_DMA_CONF_REG</a>    |
| 5      | <a href="#">SPI_USER2_REG</a>   | 12     | <a href="#">SPI_DMA_INT_ENA_REG</a> |
| 6      | <a href="#">SPI_MS_DLEN_REG</a> | 13     | <a href="#">SPI_DMA_INT_CLR_REG</a> |



Then new values of all the registers to be modified should be placed right after SPI\_BIT\_MAP\_WORD, in consecutive words in the CONF buffer.

To ensure the correctness of the content in each CONF buffer, the value in SPI\_BIT\_MAP\_WORD[31:28] is used as a “magic value”, and will be compared with SPI\_DMA\_SEG\_MAGIC\_VALUE in register SPI\_SLAVE\_REG. The value of SPI\_DMA\_SEG\_MAGIC\_VALUE should be configured before this DMA-controlled transfer starts, and can not be changed during these segments.

- If SPI\_BIT\_MAP\_WORD[31:28] == SPI\_DMA\_SEG\_MAGIC\_VALUE, this DMA-controlled transfer continues normally. SPI\_DMA\_SEG\_TRANS\_DONE\_INT is triggered at the end of this DMA-controlled transfer.
- If SPI\_BIT\_MAP\_WORD[31:28] != SPI\_DMA\_SEG\_MAGIC\_VALUE, GP-SPI2 state (spi\_st) goes back to IDLE and the transfer is ended immediately. The interrupt SPI\_DMA\_SEG\_TRANS\_DONE\_INT is still triggered, with SPI\_SEG\_MAGIC\_ERR\_INT\_RAW bit set to 1.

### CONF Buffer Configuration Example

Table 38.5-14 and Table 38.5-15 provide an example to show how to configure a CONF buffer for a transaction (segment *i*) in which SPI\_ADDR\_REG, SPI\_CTRL\_REG, SPI\_CLOCK\_REG, SPI\_USER\_REG, and SPI\_USER1\_REG need to be updated.

**Table 38.5-14. An Example of CONF buffer *i* in Segment *i***

| CONF buffer <i>i</i> | Note  |
|----------------------|---|
| SPI_BIT_MAP_WORD     | The first word in this buffer. Its value is 0xA000001F in this example when the SPI_DMA_SEG_MAGIC_VALUE is set to 0xA. As shown in Table 38.5-15, bits 0, 1, 2, 3, and 4 are set, indicating the following registers will be updated. |
| SPI_ADDR_REG         | The second word, stores the new value to SPI_ADDR_REG.  |
| SPI_CTRL_REG         | The third word, stores the new value to SPI_CTRL_REG.   |
| SPI_CLOCK_REG        | The fourth word, stores the new value to SPI_CLOCK_REG.   |
| SPI_USER_REG         | The fifth word, stores the new value to SPI_USER_REG.   |
| SPI_USER1_REG        | The sixth word, stores the new value to SPI_USER1_REG.  |

**Table 38.5-15. BM Bit Value and Register to Be Updated in This Example**

| BM Bit | Value | Register        | BM Bit | Value | Register            |
|--------|-------|-----------------|--------|-------|---------------------|
| 0      | 1     | SPI_ADDR_REG    | 7      | 0     | SPI_MISC_REG        |
| 1      | 1     | SPI_CTRL_REG    | 8      | 0     | SPI_DIN_MODE_REG    |
| 2      | 1     | SPI_CLOCK_REG   | 9      | 0     | SPI_DIN_NUM_REG     |
| 3      | 1     | SPI_USER_REG    | 10     | 0     | SPI_DOUT_MODE_REG   |
| 4      | 1     | SPI_USER1_REG   | 11     | 0     | SPI_DMA_CONF_REG    |
| 5      | 0     | SPI_USER2_REG   | 12     | 0     | SPI_DMA_INT_ENA_REG |
| 6      | 0     | SPI_MS_DLEN_REG | 13     | 0     | SPI_DMA_INT_CLR_REG |

### Notes

In a DMA-controlled configurable segmented transfer, please pay special attention to the following bits:

- **SPI\_USR\_CONF**: set **SPI\_USR\_CONF** before **SPI\_USR** is set, to enable this transfer.
- **SPI\_USR\_CONF\_NEXT**: if segment *i* is not the final transaction of this whole DMA-controlled transfer, its **SPI\_USR\_CONF\_NEXT** bit should be set to 1.
- **SPI\_CONF\_BITLEN**: GP-SPI2 CS setup time and hold time are programmable independently in each segment, see Section 38.6 for detailed configuration. The CS high time in each segment is about:

$$(\text{SPI\_CONF\_BITLEN} + 5) \times T_{\text{AHB\_CLK}}$$

The CS high time in CONF state can be set from 62.5  $\mu\text{s}$ ~3.2768 ms when  $f_{\text{AHB\_CLK}}$  is 80 MHz.

(**SPI\_CONF\_BITLEN** + 5) will overflow from (0x40000 - **SPI\_CONF\_BITLEN** - 5) if **SPI\_CONF\_BITLEN** is larger than 0x3FFFA.

### 38.5.10 GP-SPI Works as a Slave

GP-SPI can be used as a slave to communicate with an SPI master. As a slave, GP-SPI supports 1-bit SPI, 2-bit dual SPI, 4-bit quad SPI, and QPI modes, with specific communication formats. To enable this mode, set **SPI\_SLAVE\_MODE** in register **SPI\_SLAVE\_REG**.

The CS signal must be held low during the transfer, and its falling/rising edges indicate the start/end of a single or segmented transfer. Take CS low-level effective as an example, when GP-SPI is used as a slave, the CS invalid duration (high-level) between each SPI transfer should not be less than  $8 T_{\text{AHB\_CLK}}$  to ensure that each transfer can end normally.

#### 38.5.10.1 Configurable Communication Formats

When GP-SPI works as a slave, SPI full-duplex and half-duplex communications are available. To select from the two communications, configure **SPI\_DOUTDIN** in register **SPI\_USER\_REG**.

Full-duplex communication means that input data and output data are transmitted simultaneously throughout the entire transaction. All bits are treated as input or output data, which means no command, address or dummy states are expected. The interrupt **SPI\_TRANS\_DONE\_INT** is triggered once the transaction ends.

In half-duplex communication, the format is CMD+ADDR+DUMMY+DATA (DIN or DOUT).

- “DIN” means that an SPI master reads data from GP-SPI.
- “DOUT” means that an SPI master writes data to GP-SPI.

The detailed properties of each state are as follows:

##### 1. CMD:

- Indicate the function of SPI slave.
- One byte from master to slave.
- Only the values in Table 38.5-16 and Table 38.5-17 are valid.
- Can be sent in 1-bit SPI mode or 4-bit QPI mode.

##### 2. ADDR:

- The address for **Wr\_BUF** and **Rd\_BUF** commands in CPU-controlled transfer, or placeholder bits in other transfers and can be defined by application.

- One byte from master to slave.
- Can be sent in 1-bit, 2-bit or 4-bit modes according to the command.

### 3. DUMMY:

- Its value is meaningless. SPI slave prepares data in this state.
- Bit mode of SPI2 bus is also meaningless here.
- Last for eight SPI\_CLK cycles.

### 4. DIN or DOUT:

- Data length can be 0~64 bytes in CPU-controlled transfer and unlimited in DMA-controlled transfer.
- Can be sent in 1-bit, 2-bit or 4-bit modes according to the CMD value.

#### Note:

The states of ADDR and DUMMY can never be skipped in any half-duplex communications.

When a half-duplex transaction is complete, the transferred CMD and ADDR values are latched into [SPI\\_SLV\\_LAST\\_COMMAND](#) and [SPI\\_SLV\\_LAST\\_ADDR](#), respectively. [SPI\\_SLV\\_CMD\\_ERR\\_INT\\_RAW](#) will be set if the transferred CMD value is not supported by GP-SPI as slave. [SPI\\_SLV\\_CMD\\_ERR\\_INT\\_RAW](#) can only be cleared by software.

### 38.5.10.2 CMD Values Supported in Half-Duplex Communication

In half-duplex communication, the defined values of CMD determine the transfer types. Unsupported CMD values are disregarded, meanwhile the related transfer is ignored and [SPI\\_SLV\\_CMD\\_ERR\\_INT\\_RAW](#) is set. The transfer format is CMD (8 bits) + ADDR (8 bits) + DUMMY (8 SPI\_CLK cycles) + DATA (unit in bytes). The detailed description of CMD[3:0] is as follows:

- 0x1 (Wr\_BUF): CPU-controlled write operation. Master sends data and GP-SPI receives data. The data is stored in the related address of [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#).
- 0x2 (Rd\_BUF): CPU-controlled read operation. Master receives the data sent by GP-SPI. The data comes from the related address of [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#).
- 0x3 (Wr\_DMA): DMA-controlled write operation. Master sends data and GP-SPI receives data. The data is stored in GP-SPI DMA RX buffer.
- 0x4 (Rd\_DMA): DMA-controlled read operation. Master receives the data sent by GP-SPI. The data comes from GP-SPI DMA TX buffer.
- 0x7 (CMD7): used to generate an [SPI\\_SLV\\_CMD7\\_INT](#) interrupt. It can also generate a [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#) interrupt in a slave segmented transfer when DMA RX link is used. But it will not end GP-SPI's slave segmented transfer.
- 0x8 (CMD8): only used to generate an [SPI\\_SLV\\_CMD8\\_INT](#) interrupt, which will not end GP-SPI's slave segmented transfer.
- 0x9 (CMD9): only used to generate an [SPI\\_SLV\\_CMD9\\_INT](#) interrupt, which will not end GP-SPI's slave segmented transfer.

- 0xA (CMDA): only used to generate an [SPI\\_SLV\\_CMDA\\_INT](#) interrupt, which will not end GP-SPI's slave segmented transfer.

CMD7, CMD8, CMD9, and CMDA commands are reserved for user definition. These commands can be used as handshake signals, as passwords of some specific functions, as trigger signals of some user defined actions, and so on.

1/2/4-bit modes in states of CMD, ADDR, DATA are supported, which are determined by value of CMD[7:4]. The DUMMY state is always in 1-bit mode and lasts for eight SPI\_CLK cycles. The definition of CMD[7:4] is as follows:

- 0x0: CMD, ADDR, and DATA states all are in 1-bit mode.
- 0x1: CMD and ADDR are in 1-bit mode. DATA is in 2-bit mode.
- 0x2: CMD and ADDR are in 1-bit mode. DATA is in 4-bit mode.
- 0x5: CMD is in 1-bit mode. ADDR and DATA are in 2-bit mode.
- 0xA: CMD is in 1-bit mode, ADDR and DATA are in 4-bit mode or in QPI mode.

In addition, if the value of CMD[7:0] is 0x05, 0xA5, 0x06, or 0xDD, DUMMY and DATA states are skipped. The definition of CMD[7:0] is as follows:

- 0x05 (End\_SEG\_TRANS): master sends this command to end slave segmented transfer in SPI mode.
- 0xA5 (End\_SEG\_TRANS): master sends this command to end slave segmented transfer in QPI mode.
- 0x06 (En\_QPI): GP-SPI enters QPI mode when receiving this command and the bit [SPI\\_QPI\\_MODE](#) in register [SPI\\_USER\\_REG](#) is set.
- 0xDD (Ex\_QPI): GP-SPI exits QPI mode when receiving this command and the bit [SPI\\_QPI\\_MODE](#) is cleared.

All the CMD values supported by GP-SPI are listed in Table [38.5-16](#) and Table [38.5-17](#). Note that the DUMMY state is always in 1-bit mode and lasts for eight SPI\_CLK cycles.

**Table 38.5-16. CMD Values Supported in SPI Mode**

| Transfer Type | CMD[7:0] | CMD State  | ADDR State | DATA State |
|---------------|----------|------------|------------|------------|
| Wr_BUF        | 0x01     | 1-bit mode | 1-bit mode | 1-bit mode |
|               | 0x11     | 1-bit mode | 1-bit mode | 2-bit mode |
|               | 0x21     | 1-bit mode | 1-bit mode | 4-bit mode |
|               | 0x51     | 1-bit mode | 2-bit mode | 2-bit mode |
|               | 0xA1     | 1-bit mode | 4-bit mode | 4-bit mode |
| Rd_BUF        | 0x02     | 1-bit mode | 1-bit mode | 1-bit mode |
|               | 0x12     | 1-bit mode | 1-bit mode | 2-bit mode |
|               | 0x22     | 1-bit mode | 1-bit mode | 4-bit mode |
|               | 0x52     | 1-bit mode | 2-bit mode | 2-bit mode |
|               | 0xA2     | 1-bit mode | 4-bit mode | 4-bit mode |
| Wr_DMA        | 0x03     | 1-bit mode | 1-bit mode | 1-bit mode |
|               | 0x13     | 1-bit mode | 1-bit mode | 2-bit mode |
|               | 0x23     | 1-bit mode | 1-bit mode | 4-bit mode |
|               | 0x53     | 1-bit mode | 2-bit mode | 2-bit mode |

Table 38.5-16. CMD Values Supported in SPI Mode

| Transfer Type | CMD[7:0] | CMD State  | ADDR State | DATA State |
|---------------|----------|------------|------------|------------|
|               | 0xA3     | 1-bit mode | 4-bit mode | 4-bit mode |
| Rd_DMA        | 0x04     | 1-bit mode | 1-bit mode | 1-bit mode |
|               | 0x14     | 1-bit mode | 1-bit mode | 2-bit mode |
|               | 0x24     | 1-bit mode | 1-bit mode | 4-bit mode |
|               | 0x54     | 1-bit mode | 2-bit mode | 2-bit mode |
|               | 0xA4     | 1-bit mode | 4-bit mode | 4-bit mode |
| CMD7          | 0x07     | 1-bit mode | 1-bit mode | -          |
|               | 0x17     | 1-bit mode | 1-bit mode | -          |
|               | 0x27     | 1-bit mode | 1-bit mode | -          |
|               | 0x57     | 1-bit mode | 2-bit mode | -          |
|               | 0xA7     | 1-bit mode | 4-bit mode | -          |
| CMD8          | 0x08     | 1-bit mode | 1-bit mode | -          |
|               | 0x18     | 1-bit mode | 1-bit mode | -          |
|               | 0x28     | 1-bit mode | 1-bit mode | -          |
|               | 0x58     | 1-bit mode | 2-bit mode | -          |
|               | 0xA8     | 1-bit mode | 4-bit mode | -          |
| CMD9          | 0x09     | 1-bit mode | 1-bit mode | -          |
|               | 0x19     | 1-bit mode | 1-bit mode | -          |
|               | 0x29     | 1-bit mode | 1-bit mode | -          |
|               | 0x59     | 1-bit mode | 2-bit mode | -          |
|               | 0xA9     | 1-bit mode | 4-bit mode | -          |
| CMDA          | 0x0A     | 1-bit mode | 1-bit mode | -          |
|               | 0x1A     | 1-bit mode | 1-bit mode | -          |
|               | 0x2A     | 1-bit mode | 1-bit mode | -          |
|               | 0x5A     | 1-bit mode | 2-bit mode | -          |
|               | 0xAA     | 1-bit mode | 4-bit mode | -          |
| End_SEG_TRANS | 0x05     | 1-bit mode | -          | -          |
| En_QPI        | 0x06     | 1-bit mode | -          | -          |

Table 38.5-17. CMD Values Supported in QPI Mode

| Transfer Type | CMD[7:0] | CMD State  | ADDR State | DATA State |
|---------------|----------|------------|------------|------------|
| Wr_BUF        | 0xA1     | 4-bit mode | 4-bit mode | 4-bit mode |
| Rd_BUF        | 0xA2     | 4-bit mode | 4-bit mode | 4-bit mode |
| Wr_DMA        | 0xA3     | 4-bit mode | 4-bit mode | 4-bit mode |
| Rd_DMA        | 0xA4     | 4-bit mode | 4-bit mode | 4-bit mode |
| CMD7          | 0xA7     | 4-bit mode | 4-bit mode | -          |
| CMD8          | 0xA8     | 4-bit mode | 4-bit mode | -          |
| CMD9          | 0xA9     | 4-bit mode | 4-bit mode | -          |
| CMDA          | 0xAA     | 4-bit mode | 4-bit mode | -          |
| End_SEG_TRANS | 0xA5     | 4-bit mode | 4-bit mode | -          |
| Ex_QPI        | 0xDD     | 4-bit mode | 4-bit mode | -          |

Master sends 0x06 CMD (En\_QPI) to set GP-SPI slave to QPI mode and all the states of supported transfer will be in 4-bit mode afterwards. If 0xDD CMD (Ex\_QPI) is received, GP-SPI slave will be back to SPI mode.

Other transfer types than these described in Table 38.5-16 and Table 38.5-17 are ignored. But if the CS low-level duration is longer than two APB\_CLK cycles, [SPI\\_TRANS\\_DONE\\_INT](#) will be triggered. For more information on interrupts triggered at the end of transmissions, please refer to Section 38.11.

### 38.5.10.3 Slave Single Transfer and Slave Segmented Transfer

When GP-SPI works as a slave, it supports full-duplex and half-duplex communications controlled by DMA and by CPU. DMA-controlled transfer can be a single transfer, or a slave segmented transfer consisting of several transactions (segments). The CPU-controlled transfer can only be one single transfer, since each CPU-controlled transaction needs to be triggered by CPU.

In a slave segmented transfer, all transfer types listed in Table 38.5-16 and Table 38.5-17 are supported in a single transaction (segment). It means that CPU-controlled transaction and DMA-controlled transaction can be mixed in one slave segmented transfer.

It is recommended that in a slave segmented transfer:

- CPU-controlled transaction is used for handshake communication and short data transfers.
- DMA-controlled transaction is used for large data transfers.

### 38.5.10.4 Configuration of Slave Single Transfer

When operating as slave, GP-SPI supports CPU/DMA-controlled full-duplex/half-duplex single transfers.

The register configuration procedure is as follows (take GP-SPI2 as an example):

1. Configure the IO path via HP IO MUX or HP GPIO matrix between GP-SPI2 and an external SPI device.
2. Configure AHB clock (AHB\_CLK).
3. Set [SPI\\_SLAVE\\_MODE](#) to enable slave mode.
4. Configure [SPI\\_DOUTDIN](#):
  - 1: enable full-duplex communication.
  - 0: enable half-duplex communication.
5. Prepare data:
  - if CPU-controlled transfer is selected and GP-SPI2 is used to send data, then prepare data in registers [SPI\\_W0\\_REG~SPI\\_W15\\_REG](#).
  - if DMA-controlled transfer is selected,
    - configure [SPI\\_DMA\\_TX\\_ENA/SPI\\_DMA\\_RX\\_ENA](#) and [SPI\\_RX\\_EOF\\_EN](#).
    - configure DMA TX/RX link,
    - and start DMA TX/RX engine, as described in Section 38.5.7 and Section 38.5.8.
6. Set [SPI\\_DMA\\_AFIFO\\_RST](#), [SPI\\_BUF\\_AFIFO\\_RST](#), and [SPI\\_RX\\_AFIFO\\_RST](#) to reset these buffers.

7. Clear `SPI_DMA_SLV_SEG_TRANS_EN` in register `SPI_DMA_CONF_REG` to enable slave single transfer.
8. Set `SPI_TRANS_DONE_INT_ENA` in register `SPI_DMA_INT_ENA_REG` and wait for the interrupt `SPI_TRANS_DONE_INT`. In DMA-controlled mode, it is recommended to wait for the interrupt `AXI_DMA_IN_SUC_EOF_CHn_INT` when DMA RX buffer is used, which means that data has been stored in the related memory. Other interrupts described in Section 38.11 are optional.

### 38.5.10.5 Configuration of Slave Segmented Transfer in Half-Duplex

DMA must be used in this mode. The register configuration procedure is as follows (take GP-SPI2 as an example):

1. Configure the IO path via HP IO MUX or HP GPIO matrix between GP-SPI2 and an external SPI device.
2. Configure APB clock (APB\_CLK).
3. Set `SPI_SLAVE_MODE` to enable slave mode.
4. Clear `SPI_DOUTDIN` to enable half-duplex communication.
5. Prepare data in registers `SPI_WO_REG~SPI_W15_REG`, if needed.
6. Set `SPI_DMA_AFIFO_RST`, `SPI_BUF_AFIFO_RST`, and `SPI_RX_AFIFO_RST` to reset these buffers.
7. Set bits `SPI_DMA_RX_ENA` and `SPI_DMA_TX_ENA`. Clear the bit `SPI_RX_EOF_EN`. Configure DMA TX/RX link and start DMA TX/RX engine, as shown in Section 38.5.7 and Section 38.5.8.
8. Set `SPI_DMA_SLV_SEG_TRANS_EN` in register `SPI_DMA_CONF_REG` to enable slave segmented transfer.
9. Set `SPI_DMA_SEG_TRANS_DONE_INT_ENA` in register `SPI_DMA_INT_ENA_REG` and wait for the interrupt `SPI_DMA_SEG_TRANS_DONE_INT`, which means that the segmented transfer has finished and data has been put into the related memory. Other interrupts described in Section 38.11 are optional.

When `End_SEG_TRANS` (0x05 in SPI mode, 0xA5 in QPI mode) is received by GP-SPI, this slave segmented transfer is ended and the interrupt `SPI_DMA_SEG_TRANS_DONE_INT` is triggered.

### 38.5.10.6 Configuration of Slave Segmented Transfer in Full-Duplex

DMA must be used in this mode. In such transfer, the data is transferred from and to the DMA buffer. The interrupt `AXI_DMA_IN_SUC_EOF_CHn_INT` is triggered when the transfer ends.

The register configuration procedure is as follows (take GP-SPI2 as an example):

1. Configure the IO path via HP IO MUX or HP GPIO matrix between GP-SPI2 and an external SPI device.
2. Configure APB clock (APB\_CLK).
3. Set `SPI_SLAVE_MODE` and `SPI_DOUTDIN`, to enable slave full-duplex communication.
4. Set `SPI_DMA_AFIFO_RST`, `SPI_BUF_AFIFO_RST`, and `SPI_RX_AFIFO_RST` to reset these buffers.
5. Set `SPI_DMA_TX_ENA/SPI_DMA_RX_ENA`. Configure DMA TX/RX link and start DMA TX/RX engine, as shown in Section 38.5.7 and Section 38.5.8.
6. Set `SPI_RX_EOF_EN` in register `SPI_DMA_CONF_REG`. Configure `SPI_MS_DATA_BITLEN`[17:0] in register `SPI_MS_DLEN_REG` to the bit length of the received DMA data.
7. Set `SPI_DMA_SLV_SEG_TRANS_EN` in register `SPI_DMA_CONF_REG` to enable slave segmented transfer.

8. Set `AXI_DMA_IN_SUC_EOF_CH $n$ _INT_ENA` and wait for the interrupt `AXI_DMA_IN_SUC_EOF_CH $n$ _INT`.

## 38.6 CS Setup Time and Hold Time Control

SPI bus CS (SPI\_CS) setup time and hold time are very important to meet the timing requirements of various SPI devices (e.g., flash or PSRAM).

CS setup time is the time between the CS falling edge and the first latch edge of SPI bus CLK (SPI\_CLK). The first latch edge for mode 0 and mode 3 is rising edge, and falling edge for mode 2 and mode 4.

CS hold time is the time between the last latch edge of SPI\_CLK and the CS rising edge.

When operating as slave, the CS setup time and hold time should be longer than  $0.5 \times T_{\text{SPI\_CLK}}$ , otherwise the SPI transfer may be incorrect.  $T_{\text{SPI\_CLK}}$  is one cycle of SPI\_CLK.

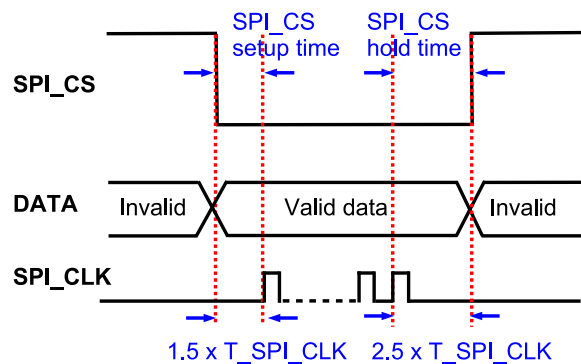
When operating as master, set the CS setup time by specifying `SPI_CS_SETUP` in register `SPI_USER_REG` and `SPI_CS_SETUP_TIME` in register `SPI_USER1_REG`.

- If `SPI_CS_SETUP` is cleared, the SPI CS setup time is  $0.5 \times T_{\text{SPI\_CLK}}$ .
- If `SPI_CS_SETUP` is set, the SPI CS setup time is  $(\text{SPI\_CS\_SETUP\_TIME} + 1.5) \times T_{\text{SPI\_CLK}}$ .

Set the CS hold time by specifying `SPI_CS_HOLD` in register `SPI_USER_REG` and `SPI_CS_HOLD_TIME` in register `SPI_USER1_REG`.

- If `SPI_CS_HOLD` is cleared, the SPI CS hold time is  $0.5 \times T_{\text{SPI\_CLK}}$ .
- If `SPI_CS_HOLD` is set, the SPI CS hold time is  $(\text{SPI\_CS\_HOLD\_TIME} + 1.5) \times T_{\text{SPI\_CLK}}$ .

Figure 38.6-1 and Figure 38.6-2 show the recommended CS timing and register configuration to access external RAM and flash.

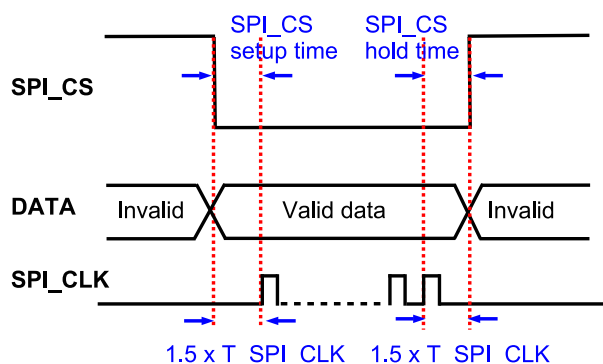


Register Configurations:

```
SPI_CS_SETUP = 1; SPI_CS_SETUP_TIME = 0;
SPI_CS_HOLD = 1; SPI_CS_HOLD_TIME = 1.
```

Figure 38.6-1. Recommended CS Timing and Settings When Accessing External RAM





Register Configurations:

SPI\_CS\_SETUP = 1; SPI\_CS\_SETUP\_TIME = 0;  
SPI\_CS\_HOLD = 1; SPI\_CS\_HOLD\_TIME = 0.

Figure 38.6-2. Recommended CS Timing and Settings When Accessing Flash

## 38.7 GP-SPI Clock Control

GP-SPI has the following clocks:

- `clk_spi_mst`: module clock of GP-SPI, derived from the following clock sources, depending on the configuration of `HP_SYS_CLKRST_GPSPI2/3_CLK_SRC_SEL`:
  - 0: `XTAL_CLK`
  - 1: `RC_FAST_CLK`
  - 2: `SDIO_PLLO_CLK`
  - 3: `APLL_CLK`
  - 4: `SPLL_CLK` (480 MHz)

The divider value is equal to `HP_SYS_CLKRST_GPSPI2/3_MST_CLK_DIV_NUM + 1`.

`HP_SYS_CLKRST_GPSPI2/3_SYS_CLK_EN` is used to enable the selected clock source. `clk_spi_mst` is used in GP-SPI as master to generate `SPI_CLK` signal for data transfer and for slaves.

- `clk_hclk`: module timing compensation clock of GP-SPI, which is a frequency-doubled clock derived from the same source as `clk_spi_mst`. Its clock source is also determined by `HP_SYS_CLKRST_GPSPI2/3_CLK_SRC_SEL`. To use this clock, `HP_SYS_CLKRST_GPSPI2/3_HS_CLK_EN` must be set, and the divider value is equal to `HP_SYS_CLKRST_GPSPI2/3_HS_CLK_DIV_NUM + 1`.
- `SPI_CLK`: this is the output clock when the GP-SPI works as master, or IO input clock when the GP-SPI works as slave.
- `AHB_CLK`: clock for register configuration.

When operating as master, the maximum output clock frequency of GP-SPI is  $f_{\text{clk\_spi\_mst}}$ . To have slower frequencies, the output clock frequency can be divided as follows:

$$f_{\text{SPI\_CLK}} = \frac{f_{\text{clk\_spi\_mst}}}{(\text{SPI\_CLKCNT\_N} + 1)(\text{SPI\_CLKDIV\_PRE} + 1)}$$

The divider is configured by `SPI_CLKCNT_N` and `SPI_CLKDIV_PRE` in register `SPI_CLOCK_REG`. When the bit `SPI_CLK_EQU_SYSCLK` in register `SPI_CLOCK_REG` is set, the output clock frequency of GP-SPI will be  $f_{clk\_spi\_mst}$ . For other integral clock divisions, `SPI_CLK_EQU_SYSCLK` should be cleared.

When operating as slave, the supported input clock frequency ( $f_{SPI\_CLK}$ ) of GP-SPI is:

- If  $f_{AHB\_CLK} \geq 60$  MHz,  $f_{SPI\_CLK} \leq 60$  MHz.
- If  $f_{AHB\_CLK} < 60$  MHz,  $f_{SPI\_CLK} \leq f_{AHB\_CLK}$ .

### 38.7.1 LP-SPI Clock Control

LP-SPI has the following clocks:

- `lp_spi_pclk`: LP-SPI module clock and clock for register configuration. `lp_spi_pclk` is used to generate `LP_SPI_CLK` for data transfer and for slaves when LP-SPI works as master. `LPPERI_CK_EN_LP_SPI` is used to enable this `lp_spi_pclk`.
- `LP_SPI_CLK`: output clock as master.

### 38.7.2 Clock Phase and Polarity

SPI protocol has four clock modes, i.e., modes 0~3. See Figure 38.7-1 and Figure 38.7-2 (excerpted from SPI protocol):

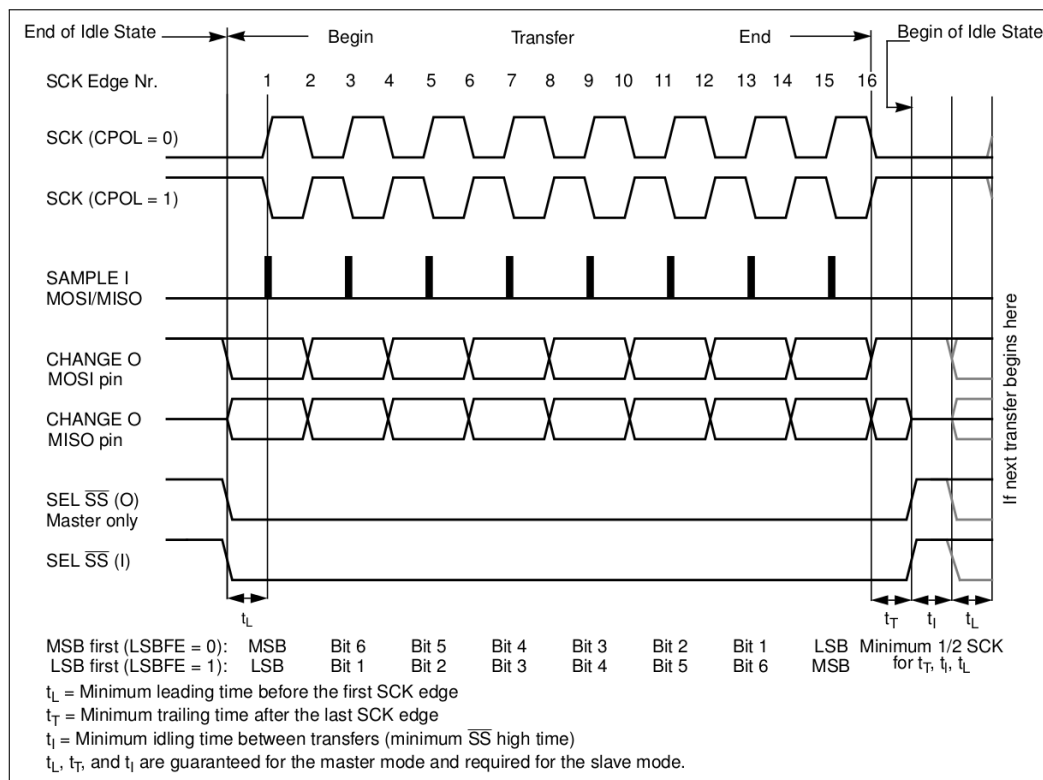


Figure 38.7-1. SPI Clock Mode 0 or 2

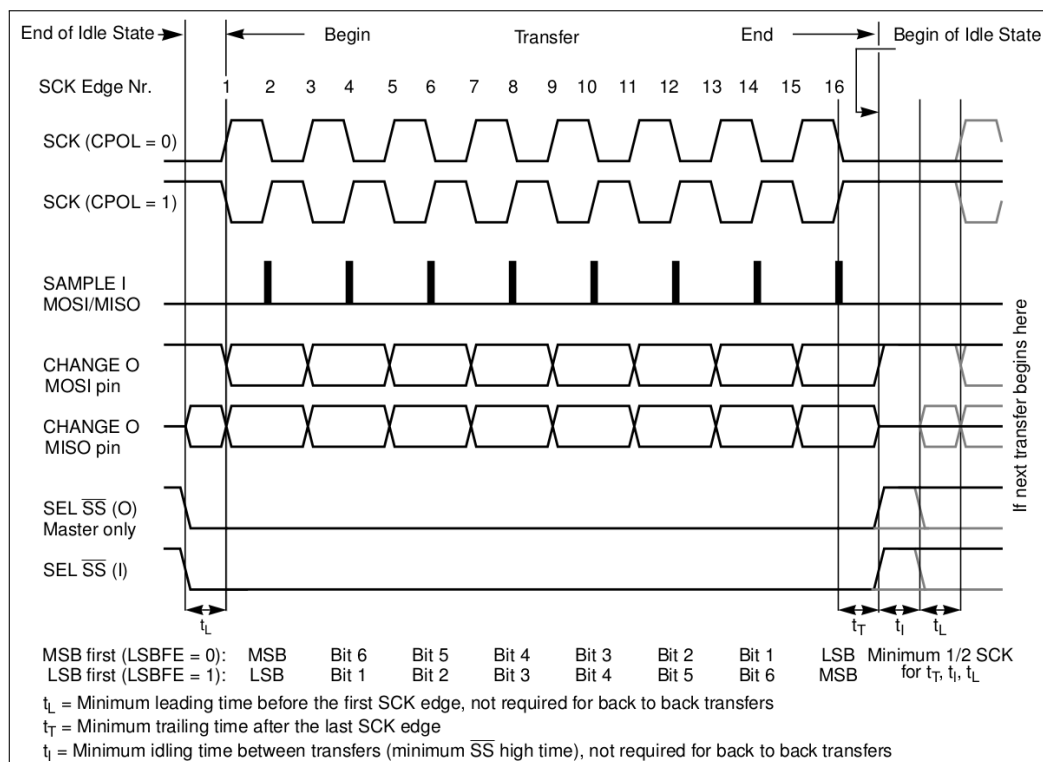


Figure 38.7-2. SPI Clock Mode 1 or 3

1. Mode 0: CPOL = 0, CPHA = 0; SCK is 0 when the SPI is in idle state; data is changed on the falling edge of SCK and sampled on the rising edge. The first data is shifted out before the first falling edge of SCK.
2. Mode 1: CPOL = 0, CPHA = 1; SCK is 0 when the SPI is in idle state; data is changed on the rising edge of SCK and sampled on the falling edge.
3. Mode 2: CPOL = 1, CPHA = 0; SCK is 1 when the SPI is in idle state; data is changed on the rising edge of SCK and sampled on the falling edge. The first data is shifted out before the first rising edge of SCK.
4. Mode 3: CPOL = 1, CPHA = 1; SCK is 1 when the SPI is in idle state; data is changed on the falling edge of SCK and sampled on the rising edge.

### 38.7.3 Clock Control as Master

The four clock modes 0~3 are supported in GP-SPI as master. The polarity and phase of GP-SPI clock are controlled by the bit [SPI\\_CLK\\_IDLE\\_EDGE](#) in register [SPI\\_MISC\\_REG](#) and the bit [SPI\\_CLK\\_OUT\\_EDGE](#) in register [SPI\\_USER\\_REG](#). The register configuration for SPI clock modes 0~3 is provided in Table 38.7-1, and can be changed according to the path delay in the application.

Table 38.7-1. Clock Phase and Polarity Configuration as Master

| Control Bit                       | Mode 0 | Mode 1 | Mode 2 | Mode 3 |
|-----------------------------------|--------|--------|--------|--------|
| <a href="#">SPI_CLK_IDLE_EDGE</a> | 0      | 0      | 1      | 1      |
| <a href="#">SPI_CLK_OUT_EDGE</a>  | 0      | 1      | 1      | 0      |

$\square$  [SPI\\_CLK\\_MODE](#) is used to select the number of rising edges of SPI\_CLK when SPI\_CS raises high to be 0, 1, 2 or SPI\_CLK always on.

**Note:**

When [SPI\\_CLK\\_MODE](#) is configured to 1 or 2, the bit [SPI\\_CS\\_HOLD](#) must be set and the value of [SPI\\_CS\\_HOLD\\_TIME](#) should be larger than 1.

### 38.7.4 Clock Control as Slave

GP-SPI as slave also supports clock modes 0~3. The polarity and phase are configured by the bits [SPI\\_TSCK\\_I\\_EDGE](#) and [SPI\\_RSCK\\_I\\_EDGE](#) in register [SPI\\_USER\\_REG](#). The output edge of data is controlled by [SPI\\_CLK\\_MODE\\_13](#) in register [SPI\\_SLAVE\\_REG](#). The detailed register configuration is shown in Table 38.7-2:

Table 38.7-2. Clock Phase and Polarity Configuration as Slave

| Control Bit                     | Mode 0 | Mode 1 | Mode 2 | Mode 3 |
|---------------------------------|--------|--------|--------|--------|
| <a href="#">SPI_TSCK_I_EDGE</a> | 0      | 1      | 1      | 0      |
| <a href="#">SPI_RSCK_I_EDGE</a> | 0      | 1      | 1      | 0      |
| <a href="#">SPI_CLK_MODE_13</a> | 0      | 1      | 0      | 1      |

## 38.8 GP-SPI Timing Compensation

### Introduction

The I/O lines are mapped via GPIO matrix or IO MUX. But there is no timing adjustment in IO MUX. The input data and output data can be delayed for 1 or 2 IO MUX operating clock cycles at the rising or falling edge in GPIO matrix. For detailed register configuration, see Chapter 8 [GPIO Matrix and IO MUX](#). Timing compensation is supported only by GP-SPI.

Figure 38.8-1 shows the timing compensation control for GP-SPI as master, including the following paths:

- “CLK”: the output path of GP-SPI bus clock. The clock is sent out by [SPI\\_CLK](#) out control module, passes through GPIO matrix or IO MUX and then goes to an external SPI device.
- “IN”: data input path of GP-SPI (see line 3 path in color purple in Figure 38.8-1). The input data from an external SPI device passes through GPIO matrix or IO MUX, then is adjusted by the Timing Module (see Figure 38.5-2) and finally is stored into [spi\\_rx\\_afifo](#).
- “OUT”: data output path of GP-SPI (see line 2 path in color rose-red in Figure 38.8-1). The output data is sent out to the Timing Module, passes through GPIO matrix or IO MUX and is then captured by an external SPI device.

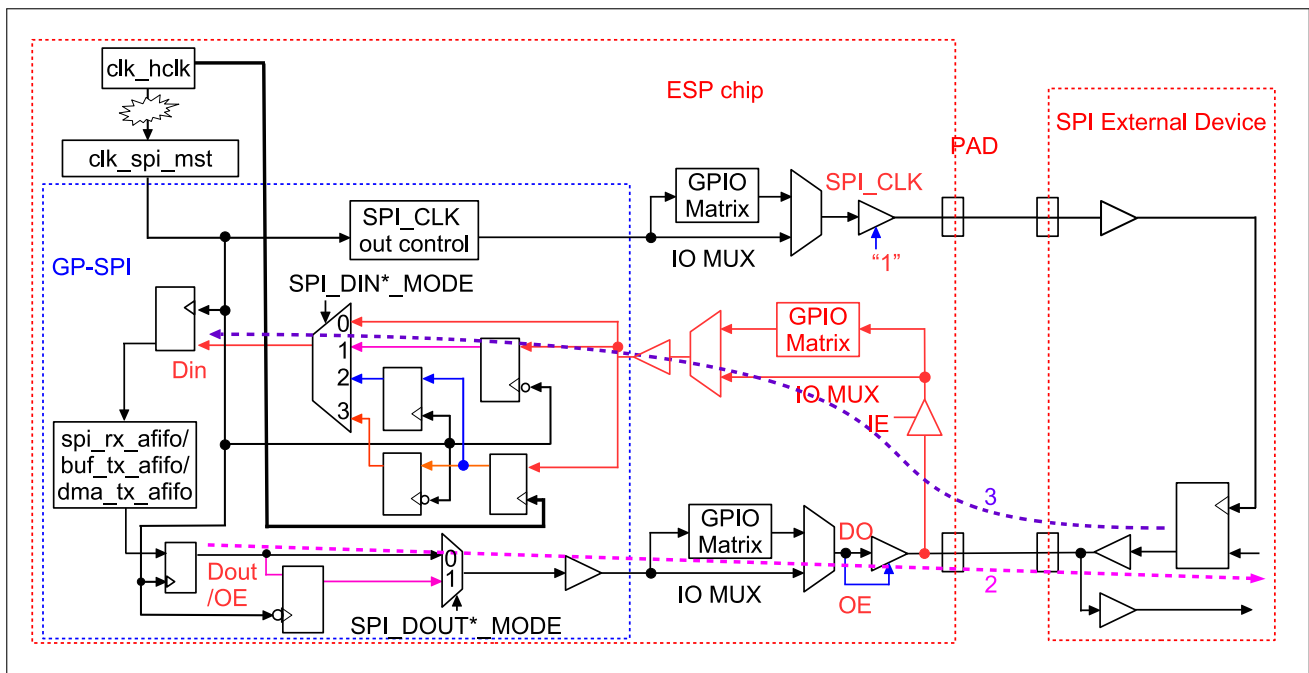


Figure 38.8-1. Timing Compensation Control Diagram in GP-SPI as Master

Every input and output data is passing through the Timing Module and the module can be used to apply delay in units of  $T_{\text{clk\_spi\_mst}}$  (one cycle of `clk_spi_mst`) on rising or falling edge.

### Key Registers

- `SPI_DIN_MODE_REG`: select the latch edge of input data
- `SPI_DIN_NUM_REG`: select the delay cycles of input data
- `SPI_DOUT_MODE_REG`: select the latch edge of output data

### Timing Compensation Example

Figure 38.8-2 shows a timing compensation example in GP-SPI2 as master. Note that DUMMY cycle length is configurable to compensate the delay in I/O lines, so as to enhance the performance of GP-SPI2.

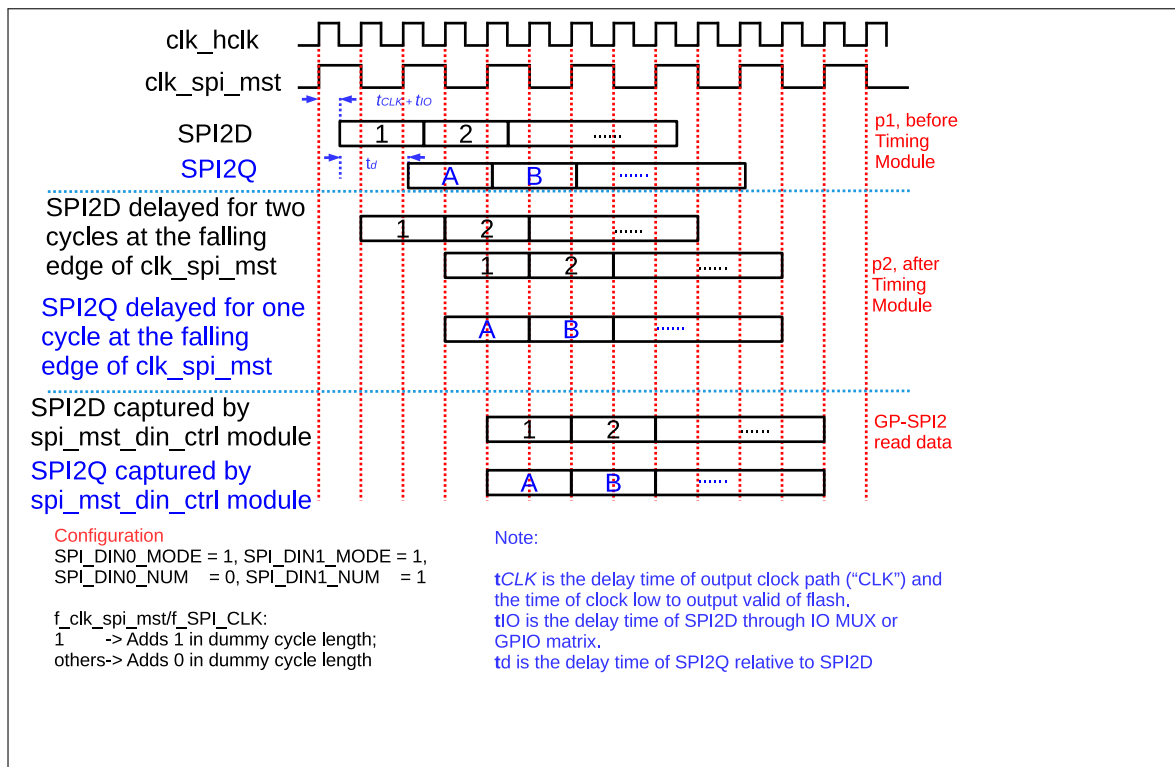


Figure 38.8-2. Timing Compensation Example in GP-SPI2 as Master

In Figure 38.8-2, "p1" is the point of input data of Timing Module, "p2" is the point of output data of Timing Module. Since the input data  $SPI2Q$  is unaligned to  $SPI2D$ , the read data of GP-SPI2 will be wrong without the timing compensation.

To get the correct read data, follow the settings below. Assuming  $f_{clk\_spi\_mst}$  equals to  $f_{SPI\_CLK}$ :

- Delay  $SPI2D$  for two cycles at the falling edge of  $clk\_spi\_mst$ .
- Delay  $SPI2Q$  for one cycle at the falling edge of  $clk\_spi\_mst$ .
- Add one extra dummy cycle.

When GP-SPI works as slave, if the bit `SPI_RSCK_DATA_OUT` in register `SPI_SLAVE_REG` is set to 1, the output data is sent at latch edge, which is half an SPI clock cycle earlier. This can be used for slave mode timing compensation.

## 38.9 LP-SPI Wake-Up

LP-SPI supports wake-up feature when working as a slave. When LP-SPI is in a sleep state (set `LP_SPI_SLEEP_EN` to 1), it can generate a wake\_up signal and trigger PMU to wake up the chip by configuring `LP_SPI_SLV_WK_MODE_SEL` to select the wake up mode. For the detailed wake-up flow, see Chapter 13 *Low-Power Management*.

- When `LP_SPI_SLV_WK_MODE_SEL` = 0, LP-SPI wakes up the chip after detecting the start bit.
- When `LP_SPI_SLV_WK_MODE_SEL` = 1, LP-SPI wakes up the chip after receiving a specific character sequence.

- [LP\\_SPI\\_SLEEP\\_WK\\_DATA\\_SEL](#) selects to monitor the specific character starting from the CMD state or DIN state.
- [LP\\_SPI\\_SLEEP\\_DIS\\_RXFIFO\\_WR\\_EN](#) selects whether to save data before waking up.
- [LP\\_SPI\\_SLV\\_WK\\_CHAR0~LP\\_SPI\\_SLV\\_WK\\_CHAR4](#) define wake up characters. LP-SPI wakes up the chip once it detects the character sequence consisting of CHAR0/CHAR1/CHAR2/CHAR3/CHAR4.
- [LP\\_SPI\\_SLV\\_WK\\_CHAR\\_NUM](#) and [LP\\_SPI\\_SLV\\_WK\\_CHAR\\_MASK](#) configure various character sequences, see Table 38.9-1. LP-SPI also supports fuzzy detection. For example, [LP\\_SPI\\_WK\\_SLV\\_CHAR\\_NUM](#) = 5 and [LP\\_SPI\\_SLV\\_WK\\_MASK](#) = 0x15 (binary 10101), then the character sequence will be \*/CHAR1\*/CHAR3/\*.

Table 38.9-1. LP-SPI Wake-Up Configuration When Working as a Slave

| LP_SPI_WK_SLV_CHAR_NUM | LP_SPI_SLV_WK_MASK | Character Sequence            |
|------------------------|--------------------|-------------------------------|
| 1                      | 0xF                | CHAR4                         |
| 2                      | 0x7                | CHAR3/CHAR4                   |
| 3                      | 0x3                | CHAR2/CHAR3/CHAR4             |
| 4                      | 0x1                | CHAR1/CHAR2/CHAR3/CHAR4       |
| 5                      | 0x0                | CHAR0/CHAR1/CHAR2/CHAR3/CHAR4 |

## 38.10 Differences Among LP-SPI, GP-SPI2, and GP-SPI3

### 38.10.1 Feature Differences

Table 38.10-1 lists the differences among GP-SPI2, GP-SPI3, and LP-SPI on their supported features.

Table 38.10-1. Feature Differences Among GP-SPI2, GP-SPI3, and LP-SPI

| Feature   | GP-SPI2                              | GP-SPI3  | LP-SPI                                |
|---|--------------------------------------|--|---------------------------------------|
| Data modes supported in CMD/ADDR/DOUT/DIN states when working as a master | 1/2/4/8-bit                          | 1/2/4-bit  | 1-bit                                 |
| Data modes supported in CMD/ADDR/DOUT/DIN states when working as a slave  | 1/2/4-bit                            | 1/2/4-bit  | 1-bit                                 |
| DMA-controlled transfers  | Support all DMA-controlled transfers | Not support DMA-controlled configurable segmented transfer | Not support any DMA related transfers |
| I/O mapping   | Via HP GPIO matrix or HP IO MUX      | Via HP GPIO matrix   | Via LP GPIO matrix or LP IO MUX       |
| CS line amount  | 6                                    | 3  | 1                                     |
| Unaligned byte transfer   | Support                              | Support  | Not support                           |
| DTR feature   | Support                              | Not support  | Not support                           |

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Table 38.10-1 – Cont'd from previous page

| Feature                                 | GP-SPI2     | GP-SPI3     | LP-SPI      |
|---|-------------|-------------|-------------|
| Wake-up feature when working as a slave | Not support | Not support | Support     |
| Timing compensation                     | Support     | Support     | Not support |

## 38.10.2 Register Differences

Table 38.10-2 lists the registers and fields that differs in GP-SPI2, GP-SPI3, and LP-SPI.

Table 38.10-2. Register Differences

| Register | Field             | GP-SPI2 | GP-SPI3 | LP-SPI |
|----------|-------------------|---------|---------|--------|
| CMD_REG  | CONF_BITLEN       | Y       | —       | —      |
| USER_REG | OPI_MODE          | Y       | Y       | —      |
|          | FWRITE_DUAL       | Y       | Y       | —      |
|          | FWRITE_DUAD       | Y       | Y       | —      |
|          | FWRITE_OCT        | Y       | —       | —      |
|          | USR_CONF_NEXT     | Y       | —       | —      |
| CTRL_REG | FADDR_DUAL        | Y       | Y       | —      |
|          | FADDR_QUAD        | Y       | Y       | —      |
|          | FADDR_OCT         | Y       | —       | —      |
|          | FCMD_DUAL         | Y       | Y       | —      |
|          | FCMD_QUAD         | Y       | Y       | —      |
|          | FCMD_OCT          | Y       | —       | —      |
|          | FREAD_DUAL        | Y       | Y       | —      |
|          | FREAD_QUAD        | Y       | Y       | —      |
|          | FREAD_OCT         | Y       | —       | —      |
|          | HOLD_POL          | Y       | Y       | —      |
|          | WP_POL            | Y       | Y       | —      |
| MISC_REG | CS1_DIS           | Y       | Y       | —      |
|          | CS2_DIS           | Y       | Y       | —      |
|          | CS3_DIS           | Y       | —       | —      |
|          | CS4_DIS           | Y       | —       | —      |
|          | CS5_DIS           | Y       | —       | —      |
|          | CLK_DATA_DTR_EN   | Y       | —       | —      |
|          | DATA_DTR_EN       | Y       | —       | —      |
|          | ADDR_DTR_EN       | Y       | —       | —      |
|          | DQS_IDLE_EDGE     | Y       | —       | —      |
|          | QUAD_DIN_PIN_SWAP | Y       | —       | —      |

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Table 38.10-2 – cont'd from previous page

| Register        | Field                   | GP-SPI2 | GP-SPI3 | LP-SPI |
|-----------------|-------------------------|---------|---------|--------|
| DMA_CONF_REG    | DMA_OUTFIFO_EMPTY       | Y       | Y       | —      |
|                 | DMA_INFIFO_FULL         | Y       | Y       | —      |
|                 | DMA_SLV_SEG_TRANS_EN    | Y       | Y       | —      |
|                 | SLV_RX_SEG_TRANS_CLR_EN | Y       | Y       | —      |
|                 | SLV_TX_SEG_TRANS_CLR_EN | Y       | Y       | —      |
|                 | RX_EOF_EN               | Y       | Y       | —      |
|                 | DMA_RX_ENA              | Y       | Y       | —      |
|                 | DMA_TX_ENA              | Y       | Y       | —      |
|                 | DMA_AFIFO_RST           | Y       | Y       | —      |
| SLEEP_CONFO_REG | SLV_WK_CHAR0            | —       | —       | Y      |
|                 | SLV_WK_CHAR_NUM         | —       | —       | Y      |
|                 | SLV_WK_CHAR_MASK        | —       | —       | Y      |
|                 | SLV_WK_MODE_SEL         | —       | —       | Y      |
|                 | SLEEP_EN                | —       | —       | Y      |
|                 | SLEEP_DIS_RXFIFO_WR_EN  | —       | —       | Y      |
|                 | SLEEP_WK_DATA_SEL       | —       | —       | Y      |
| SLEEP_CONF1_REG | SLV_WK_CHAR1            | —       | —       | Y      |
|                 | SLV_WK_CHAR2            | —       | —       | Y      |
|                 | SLV_WK_CHAR3            | —       | —       | Y      |
|                 | SLV_WK_CHAR4            | —       | —       | Y      |
| SLAVE_REG       | SLV_RDDMA_BITLEN_EN     | Y       | Y       | —      |
|                 | SLV_WRDMA_BITLEN_EN     | Y       | Y       | —      |
|                 | SLV_LAST_BYTE_STRB      | Y       | Y       | —      |
|                 | DMA_SEG_MAGIC_VALUE     | Y       | —       | —      |
|                 | USR_CONF                | Y       | —       | —      |
|                 | MST_FD_WAIT_DMA_TX_DATA | Y       | Y       | —      |
| DIN_MODE_REG    | DIN4_MODE               | Y       | —       | —      |
|                 | DIN5_MODE               | Y       | —       | —      |
|                 | DIN6_MODE               | Y       | —       | —      |
|                 | DIN7_MODE               | Y       | —       | —      |
| DIN_NUM_REG     | DIN4_NUM                | Y       | —       | —      |
|                 | DIN5_NUM                | Y       | —       | —      |
|                 | DIN6_NUM                | Y       | —       | —      |
|                 | DIN7_NUM                | Y       | —       | —      |
| DOUT_MODE_REG   | DOUT4_MODE              | Y       | —       | —      |
|                 | DOUT5_MODE              | Y       | —       | —      |
|                 | DOUT6_MODE              | Y       | —       | —      |
|                 | DOUT7_MODE              | Y       | —       | —      |
|                 | D_DQS_MODE              | Y       | —       | —      |

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Table 38.10-2 – cont'd from previous page

| Register        | Field                         | GP-SPI2 | GP-SPI3 | LP-SPI |
|-----------------|-------------------------------|---------|---------|--------|
| DMA_INT_ENA_REG | DMA_INFIFO_FULL_ERR_INT_ENA   | Y       | Y       | —      |
|                 | DMA_OUTFIFO_EMPTY_ERR_INT_ENA | Y       | Y       | —      |
|                 | SLV_EX_QPI_INT_ENA            | Y       | Y       | —      |
|                 | SLV_EN_QPI_INT_ENA            | Y       | Y       | —      |
|                 | SLV_CMD7_INT_ENA              | Y       | Y       | —      |
|                 | SLV_CMD8_INT_ENA              | Y       | Y       | —      |
|                 | SLV_CMD9_INT_ENA              | Y       | Y       | —      |
|                 | SLV_CMDA_INT_ENA              | Y       | Y       | —      |
|                 | SLV_RD_DMA_DONE_INT_ENA       | Y       | Y       | —      |
|                 | SLV_WR_DMA_DONE_INT_ENA       | Y       | Y       | —      |
|                 | LP_SPI_WAKEUP_INT_ENA         | —       | —       | Y      |
|                 | DMA_SEG_TRANS_DONE_INT_ENA    | Y       | Y       | —      |
|                 | SPI_SEG_MAGIC_ERR_INT_ENA     | Y       | —       | —      |
| DMA_INT_CLR_REG | DMA_INFIFO_FULL_ERR_INT_CLR   | Y       | Y       | —      |
|                 | DMA_OUTFIFO_EMPTY_ERR_INT_CLR | Y       | Y       | —      |
|                 | SLV_EX_QPI_INT_CLR            | Y       | Y       | —      |
|                 | SLV_EN_QPI_INT_CLR            | Y       | Y       | —      |
|                 | SLV_CMD7_INT_CLR              | Y       | Y       | —      |
|                 | SLV_CMD8_INT_CLR              | Y       | Y       | —      |
|                 | SLV_CMD9_INT_CLR              | Y       | Y       | —      |
|                 | SLV_CMDA_INT_CLR              | Y       | Y       | —      |
|                 | SLV_RD_DMA_DONE_INT_CLR       | Y       | Y       | —      |
|                 | SLV_WR_DMA_DONE_INT_CLR       | Y       | Y       | —      |
|                 | LP_SPI_WAKEUP_INT_CLR         | —       | —       | Y      |
|                 | DMA_SEG_TRANS_DONE_INT_CLR    | Y       | Y       | —      |
|                 | SPI_SEG_MAGIC_ERR_INT_CLR     | Y       | —       | —      |
| DMA_INT_RAW_REG | DMA_INFIFO_FULL_ERR_INT_RAW   | Y       | Y       | —      |
|                 | DMA_OUTFIFO_EMPTY_ERR_INT_RAW | Y       | Y       | —      |
|                 | SLV_EX_QPI_INT_RAW            | Y       | Y       | —      |
|                 | SLV_EN_QPI_INT_RAW            | Y       | Y       | —      |
|                 | SLV_CMD7_INT_RAW              | Y       | Y       | —      |
|                 | SLV_CMD8_INT_RAW              | Y       | Y       | —      |
|                 | SLV_CMD9_INT_RAW              | Y       | Y       | —      |
|                 | SLV_CMDA_INT_RAW              | Y       | Y       | —      |
|                 | SLV_RD_DMA_DONE_INT_RAW       | Y       | Y       | —      |
|                 | SLV_WR_DMA_DONE_INT_RAW       | Y       | Y       | —      |
|                 | LP_SPI_WAKEUP_INT_RAW         | —       | —       | Y      |
|                 | DMA_SEG_TRANS_DONE_INT_RAW    | Y       | Y       | —      |
|                 | SPI_SEG_MAGIC_ERR_INT_RAW     | Y       | —       | —      |

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Table 38.10-2 – cont'd from previous page

| Register        | Field                         | GP-SPI2 | GP-SPI3 | LP-SPI |
|-----------------|-------------------------------|---------|---------|--------|
| DMA_INT_ST_REG  | DMA_INFIFO_FULL_ERR_INT_ST    | Y       | Y       | —      |
|                 | DMA_OUTFIFO_EMPTY_ERR_INT_ST  | Y       | Y       | —      |
|                 | SLV_EX_QPI_INT_ST             | Y       | Y       | —      |
|                 | SLV_EN_QPI_INT_ST             | Y       | Y       | —      |
|                 | SLV_CMD7_INT_ST               | Y       | Y       | —      |
|                 | SLV_CMD8_INT_ST               | Y       | Y       | —      |
|                 | SLV_CMD9_INT_ST               | Y       | Y       | —      |
|                 | SLV_CMDA_INT_ST               | Y       | Y       | —      |
|                 | SLV_RD_DMA_DONE_INT_ST        | Y       | Y       | —      |
|                 | SLV_WR_DMA_DONE_INT_ST        | Y       | Y       | —      |
|                 | LP_SPI_WAKEUP_INT_ST          | —       | —       | Y      |
|                 | DMA_SEG_TRANS_DONE_INT_ST     | Y       | Y       | —      |
|                 | SPI_SEG_MAGIC_ERR_INT_ST      | Y       | —       | —      |
| DMA_INT_SET_REG | DMA_INFIFO_FULL_ERR_INT_SET   | Y       | Y       | —      |
|                 | DMA_OUTFIFO_EMPTY_ERR_INT_SET | Y       | Y       | —      |
|                 | SLV_EX_QPI_INT_SET            | Y       | Y       | —      |
|                 | SLV_EN_QPI_INT_SET            | Y       | Y       | —      |
|                 | SLV_CMD7_INT_SET              | Y       | Y       | —      |
|                 | SLV_CMD8_INT_SET              | Y       | Y       | —      |
|                 | SLV_CMD9_INT_SET              | Y       | Y       | —      |
|                 | SLV_CMDA_INT_SET              | Y       | Y       | —      |
|                 | SLV_RD_DMA_DONE_INT_SET       | Y       | Y       | —      |
|                 | SLV_WR_DMA_DONE_INT_SET       | Y       | Y       | —      |
|                 | LP_SPI_WAKEUP_INT_SET         | —       | —       | Y      |
|                 | DMA_SEG_TRANS_DONE_INT_SET    | Y       | Y       | —      |
|                 | SPI_SEG_MAGIC_ERR_INT_SET     | Y       | —       | —      |

### 38.10.3 Interrupt Differences

Table 38.10-3 lists the interrupts supported in GP-SPI2, GP-SPI3, and LP-SPI.

Table 38.10-3. Interrupt Differences

| Interrupt                                     | GP-SPI2 | GP-SPI3 | LP-SPI |
|---|---------|---------|--------|
| <a href="#">SPI_DMA_INFIFO_FULL_ERR_INT</a>   | Y       | Y       | —      |
| <a href="#">SPI_DMA_OUTFIFO_EMPTY_ERR_INT</a> | Y       | Y       | —      |
| <a href="#">SPI_SLV_EX_QPI_INT</a>            | Y       | Y       | —      |
| <a href="#">SPI_SLV_EN_QPI_INT</a>            | Y       | Y       | —      |
| <a href="#">SPI_SLV_CMD7_INT</a>              | Y       | Y       | —      |
| <a href="#">SPI_SLV_CMD8_INT</a>              | Y       | Y       | —      |
| <a href="#">SPI_SLV_CMD9_INT</a>              | Y       | Y       | —      |
| <a href="#">SPI_SLV_CMDA_INT</a>              | Y       | Y       | —      |

Table 38.10-3. Interrupt Differences

| Interrupt                                       | GP-SPI2 | GP-SPI3 | LP-SPI |
|---|---------|---------|--------|
| <a href="#">SPI_SLV_RD_DMA_DONE_INT</a>         | Y       | Y       | —      |
| <a href="#">SPI_SLV_WR_DMA_DONE_INT</a>         | Y       | Y       | —      |
| <a href="#">SPI_SLV_RD_BUF_DONE_INT</a>         | Y       | Y       | Y      |
| <a href="#">SPI_SLV_WR_BUF_DONE_INT</a>         | Y       | Y       | Y      |
| <a href="#">SPI_TRANS_DONE_INT</a>              | Y       | Y       | Y      |
| <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a>      | Y       | Y       | —      |
| <a href="#">SPI_SEG_MAGIC_ERR_INT</a>           | Y       | —       | —      |
| <a href="#">SPI_MST_RX_AFIFO_WFULL_ERR_INT</a>  | Y       | Y       | Y      |
| <a href="#">SPI_MST_TX_AFIFO_REMPTY_ERR_INT</a> | Y       | Y       | Y      |
| <a href="#">SPI_SLV_CMD_ERR_INT</a>             | Y       | Y       | Y      |
| <a href="#">SPI_APP2_INT</a>                    | Y       | Y       | Y      |
| <a href="#">SPI_APP1_INT</a>                    | Y       | Y       | Y      |
| <a href="#">LP_SPI_WAKEUP_INT</a>               | —       | —       | Y      |

## 38.11 Interrupt

### 38.11.1 Interrupt Description

ESP32-P4 LP-SPI and GP-SPI can generate the following external interrupt signals:

- LP-SPI: `LP_SPI_INTR`
- GP-SPI2: `SPI_INTR_2`
- GP-SPI3: `SPI_INTR_3`

`LP_SPI_INTR` is directly mapped to LP CPU (see [Low-Power CPU](#)), and `SPI_INTR_2/SPI_INTR_3` can be mapped to HP CPU0/1 through the [Interrupt Matrix](#). These interrupt signals are generated by internal interrupt sources of LP-SPI and GP-SPI. Table 38.11-1 lists the internal interrupt sources, interrupt trigger conditions, and generated interrupt signals of LP-SPI and GP-SPI.

Table 38.11-1. Internal Interrupt Sources of LP-SPI and GP-SPI

| Internal Interrupt Source                     | Trigger Condition   | Interrupt Signal                   |
|---|---|------------------------------------|
| <a href="#">SPI_DMA_INFIFO_FULL_ERR_INT</a>   | The length of DMA RX FIFO is shorter than that of actual data transferred               | <code>SPI_INTR_2/SPI_INTR_3</code> |
| <a href="#">SPI_DMA_OUTFIFO_EMPTY_ERR_INT</a> | The length of DMA TX FIFO is shorter than that of actual data transferred               | <code>SPI_INTR_2/SPI_INTR_3</code> |
| <a href="#">SPI_SLV_EX_QPI_INT</a>            | <code>Ex_QPI</code> is received correctly in GP-SPI2 as slave and the SPI transfer ends | <code>SPI_INTR_2/SPI_INTR_3</code> |
| <a href="#">SPI_SLV_EN_QPI_INT</a>            | <code>En_QPI</code> is received correctly in GP-SPI2 as slave and the SPI transfer ends | <code>SPI_INTR_2/SPI_INTR_3</code> |

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Table 38.11-1 – cont'd from previous page

| Internal Interrupt Source      | Trigger Condition   | Interrupt Signal                      |
|--------------------------------|---|---------------------------------------|
| SPI_SLV_CMD7_INT               | CMD7 is received correctly in GP-SPI2 as slave and the SPI transfer ends  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_CMD8_INT               | CMD8 is received correctly in GP-SPI2 as slave and the SPI transfer ends  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_CMD9_INT               | CMD9 is received correctly in GP-SPI2 as slave and the SPI transfer ends  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_CMDA_INT               | CMDA is received correctly in GP-SPI2 as slave and the SPI transfer ends  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_RD_DMA_DONE_INT        | At the end of Rd_DMA transfer as slave  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_WR_DMA_DONE_INT        | At the end of Wr_DMA transfer as slave  | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SLV_RD_BUF_DONE_INT        | At the end of Rd_BUF transfer as slave  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_SLV_WR_BUF_DONE_INT        | At the end of Wr_BUF transfer as slave  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_TRANS_DONE_INT             | At the end of SPI bus transfer in both as master and as slave.  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_DMA_SEG_TRANS_DONE_INT     | At the end of End_SEG_TRANS transfer in GP-SPI slave segmented transfer mode or at the end of configurable segmented transfer as master | SPI_INTR_2/SPI_INTR_3                 |
| SPI_SEG_MAGIC_ERR_INT          | A Magic error occurs in CONF buffer during configurable segmented transfer as master  | SPI_INTR_2                            |
| SPI_MST_RX_AFIFO_WFULL_ERR_INT | RX AFIFO write-full error in GP-SPI as master   | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_MST_TX_AFIFO_EMPTY_ERR_INT | TX AFIFO read-empty error in GP-SPI as master   | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_SLV_CMD_ERR_INT            | A received command value is not supported in GP-SPI as slave  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_APP2_INT                   | Set <a href="#">SPI_APP2_INT_SET</a> (Only used for user defined function)  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |
| SPI_APP1_INT                   | Set <a href="#">SPI_APP1_INT_SET</a> (Only used for user defined function)  | LP_SPI_INTR/SPI_INTR_2/<br>SPI_INTR_3 |

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Table 38.11-1 – cont'd from previous page

| Internal Interrupt Source | Trigger Condition  | Interrupt Signal |
|---------------------------|--|------------------|
| LP_SPI_WAKEUP_INT         | Pre-defined chars are received and wake_up signal is generated | LP_SPI_INTR      |

LP-SPI is a simplified version of GP-SPI, which contains only some GP-SPI interrupt sources. Each interrupt source has a common set of configuration registers, see the *Interrupt Registers* in Section [Register Summary](#).

### 38.11.2 Interrupts Used in Master and in Slave (Take GP-SPI as an Example)

Table 38.11-2 and Table 38.11-3 show the interrupts used in GP-SPI master and slave modes. Set the interrupt enable bit SPI\_\*\_INT\_ENA in [SPI\\_DMA\\_INT\\_ENA\\_REG](#) and wait for the interrupt. When the transfer ends, the related interrupt is triggered and should be cleared by software before the next transfer.

Table 38.11-2. GP-SPI Master Mode Interrupts

| Transfer Type                   | Communication Mode    | Controlled by | Interrupt  |
|---------------------------------|-----------------------|---------------|--|
| Single Transfer                 | Full-duplex           | DMA           | <a href="#">AXI_DMA_IN_SUC_EOF_CH<sub>n</sub>_INT</a> <sup>1</sup> |
|                                 |                       | CPU           | <a href="#">SPI_TRANS_DONE_INT</a> <sup>2</sup>                    |
|                                 | Half-duplex MOSI Mode | DMA           | <a href="#">SPI_TRANS_DONE_INT</a>                                 |
|                                 |                       | CPU           | <a href="#">SPI_TRANS_DONE_INT</a>                                 |
|                                 | Half-duplex MISO Mode | DMA           | <a href="#">AXI_DMA_IN_SUC_EOF_CH<sub>n</sub>_INT</a>              |
|                                 |                       | CPU           | <a href="#">SPI_TRANS_DONE_INT</a>                                 |
| Configurable Segmented Transfer | Full-duplex           | DMA           | <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a> <sup>3</sup>            |
|                                 |                       | CPU           | Not supported  |
|                                 | Half-duplex MOSI Mode | DMA           | <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a>                         |
|                                 |                       | CPU           | Not supported  |
|                                 | Half-duplex MISO      | DMA           | <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a>                         |
|                                 |                       | CPU           | Not supported  |

<sup>1</sup> If [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CH<sub>n</sub>\\_INT](#) is triggered, it means all the RX data of GP-SPI has been stored in the RX buffer, and the TX data has been transferred to the slave.

<sup>2</sup> [SPI\\_TRANS\\_DONE\\_INT](#) is triggered when CS is high, which indicates that master has completed the data exchange in [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) with slave in this mode.

<sup>3</sup> If [SPI\\_DMA\\_SEG\\_TRANS\\_DONE\\_INT](#) is triggered, it means that the whole configurable segmented transfer (consisting of several segments) has finished, i.e., the RX data has been stored in the RX buffer completely and all the TX data has been sent out.

Table 38.11-3. GP-SPI Slave Mode Interrupts

| Transfer Type            | Communication Mode    | Controlled by | Interrupt  |
|--------------------------|-----------------------|---------------|--|
| Single Transfer          | Full-duplex           | DMA           | <a href="#">AXI_DMA_IN_SUC_EOF_CHn_INT</a> <sup>1</sup>  |
|                          |                       | CPU           | <a href="#">SPI_TRANS_DONE_INT</a> <sup>2</sup>          |
|                          | Half-duplex MOSI Mode | DMA (Wr_DMA)  | <a href="#">AXI_DMA_IN_SUC_EOF_CHn_INT</a> <sup>3</sup>  |
|                          |                       | CPU (Wr_BUF)  | <a href="#">SPI_TRANS_DONE_INT</a> <sup>4</sup>          |
|                          | Half-duplex MISO Mode | DMA (Rd_DMA)  | <a href="#">SPI_TRANS_DONE_INT</a> <sup>5</sup>          |
|                          |                       | CPU (Rd_BUF)  | <a href="#">SPI_TRANS_DONE_INT</a> <sup>6</sup>          |
| Slave Segmented Transfer | Full-duplex           | DMA           | <a href="#">AXI_DMA_IN_SUC_EOF_CHn_INT</a> <sup>7</sup>  |
|                          |                       | CPU           | Not supported <sup>8</sup>                               |
|                          | Half-duplex MOSI Mode | DMA (Wr_DMA)  | <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a> <sup>9</sup>  |
|                          |                       | CPU (Wr_BUF)  | Not supported <sup>10</sup>                              |
|                          | Half-duplex MISO Mode | DMA (Rd_DMA)  | <a href="#">SPI_DMA_SEG_TRANS_DONE_INT</a> <sup>11</sup> |
|                          |                       | CPU (Rd_BUF)  | Not supported <sup>12</sup>                              |

<sup>1</sup> If [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#) is triggered, it means all the RX data has been stored in the RX buffer, and the TX data has been sent to the slave.

<sup>2</sup> [SPI\\_TRANS\\_DONE\\_INT](#) is triggered when CS is high, which indicates that master has completed the data exchange in [SPI\\_WO\\_REG~SPI\\_W15\\_REG](#) with slave in this mode.

<sup>3</sup> [SPI\\_SLV\\_WR\\_DMA\\_DONE\\_INT](#) just means that the transmission on the SPI bus is done, but can not ensure that all the push data has been stored in the RX buffer. For this reason, [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#) is recommended.

<sup>4</sup> Or wait for [SPI\\_SLV\\_WR\\_BUF\\_DONE\\_INT](#).

<sup>5</sup> Or wait for [SPI\\_SLV\\_RD\\_DMA\\_DONE\\_INT](#).

<sup>6</sup> Or wait for [SPI\\_SLV\\_RD\\_BUF\\_DONE\\_INT](#).

<sup>7</sup> Slave should set the total read data byte length in [SPI\\_MS\\_DATA\\_BITLEN](#) before the transfer begins. Set [SPI\\_RX\\_EOF\\_EN](#) to 1 before the end of the interrupt program.

<sup>8</sup> Master and slave should define a method to end the segmented transfer, such as via GPIO interrupt.

<sup>9</sup> Master sends End\_SEG\_TRAN to end the segmented transfer or slave sets the total read data byte length in [SPI\\_MS\\_DATA\\_BITLEN](#) and waits for [AXI\\_DMA\\_IN\\_SUC\\_EOF\\_CHn\\_INT](#).

<sup>10</sup> Half-duplex Wr\_BUF single transfer can be used in a slave segmented transfer.

<sup>11</sup> Master sends End\_SEG\_TRAN to end the segmented transfer.

<sup>12</sup> Half-duplex Rd\_BUF single transfer can be used in a slave segmented transfer.

## 38.12 Register Summary

### 38.12.1 GP-SPI2 Register Summary

The addresses in this section are relative to GP-SPI2 base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

The abbreviations given in Column Access are explained in Section [Access Types for Registers](#).

| Name                           | Description | Address | Access |
|--------------------------------|-------------|---------|--------|
| User-defined control registers |             |         |        |

| Name                                       | Description                                 | Address | Access   |
|--|---|---------|----------|
| <a href="#">SPI_CMD_REG</a>                | Command control register                    | 0x0000  | varies   |
| <a href="#">SPI_ADDR_REG</a>               | Address value register                      | 0x0004  | R/W      |
| <a href="#">SPI_USER_REG</a>               | SPI USER control register                   | 0x0010  | varies   |
| <a href="#">SPI_USER1_REG</a>              | SPI USER control register 1                 | 0x0014  | R/W      |
| <a href="#">SPI_USER2_REG</a>              | SPI USER control register 2                 | 0x0018  | R/W      |
| <b>Control and configuration registers</b> |   |         |          |
| <a href="#">SPI_CTRL_REG</a>               | SPI control register                        | 0x0008  | R/W      |
| <a href="#">SPI_MS_DLEN_REG</a>            | SPI data bit length control register        | 0x001C  | R/W      |
| <a href="#">SPI_MISC_REG</a>               | SPI misc register                           | 0x0020  | R/W      |
| <a href="#">SPI_DMA_CONF_REG</a>           | SPI DMA control register                    | 0x0030  | varies   |
| <a href="#">SPI_SLAVE_REG</a>              | SPI slave control register                  | 0x00E0  | varies   |
| <a href="#">SPI_SLAVE1_REG</a>             | SPI slave control register 1                | 0x00E4  | R/W/SS   |
| <b>Clock control registers</b>             |   |         |          |
| <a href="#">SPI_CLOCK_REG</a>              | SPI clock control register                  | 0x000C  | R/W      |
| <a href="#">SPI_CLK_GATE_REG</a>           | SPI module clock and register clock control | 0x00E8  | R/W      |
| <b>Timing registers</b>                    |   |         |          |
| <a href="#">SPI_DIN_MODE_REG</a>           | SPI input delay mode configuration          | 0x0024  | R/W      |
| <a href="#">SPI_DIN_NUM_REG</a>            | SPI input delay number configuration        | 0x0028  | R/W      |
| <a href="#">SPI_DOUT_MODE_REG</a>          | SPI output delay mode configuration         | 0x002C  | R/W      |
| <b>Interrupt registers</b>                 |   |         |          |
| <a href="#">SPI_DMA_INT_ENA_REG</a>        | SPI interrupt enable register               | 0x0034  | R/W      |
| <a href="#">SPI_DMA_INT_CLR_REG</a>        | SPI interrupt clear register                | 0x0038  | WT       |
| <a href="#">SPI_DMA_INT_RAW_REG</a>        | SPI interrupt raw register                  | 0x003C  | R/WTC/SS |
| <a href="#">SPI_DMA_INT_ST_REG</a>         | SPI interrupt status register               | 0x0040  | RO       |
| <a href="#">SPI_DMA_INT_SET_REG</a>        | SPI interrupt software set register         | 0x0044  | WT       |
| <b>CPU-controlled data buffer</b>          |   |         |          |
| <a href="#">SPI_W0_REG</a>                 | SPI CPU-controlled buffer 0                 | 0x0098  | R/W/SS   |
| <a href="#">SPI_W1_REG</a>                 | SPI CPU-controlled buffer 1                 | 0x009C  | R/W/SS   |
| <a href="#">SPI_W2_REG</a>                 | SPI CPU-controlled buffer 2                 | 0x00A0  | R/W/SS   |
| <a href="#">SPI_W3_REG</a>                 | SPI CPU-controlled buffer 3                 | 0x00A4  | R/W/SS   |
| <a href="#">SPI_W4_REG</a>                 | SPI CPU-controlled buffer 4                 | 0x00A8  | R/W/SS   |
| <a href="#">SPI_W5_REG</a>                 | SPI CPU-controlled buffer 5                 | 0x00AC  | R/W/SS   |
| <a href="#">SPI_W6_REG</a>                 | SPI CPU-controlled buffer 6                 | 0x00B0  | R/W/SS   |
| <a href="#">SPI_W7_REG</a>                 | SPI CPU-controlled buffer 7                 | 0x00B4  | R/W/SS   |
| <a href="#">SPI_W8_REG</a>                 | SPI CPU-controlled buffer 8                 | 0x00B8  | R/W/SS   |
| <a href="#">SPI_W9_REG</a>                 | SPI CPU-controlled buffer 9                 | 0x00BC  | R/W/SS   |
| <a href="#">SPI_W10_REG</a>                | SPI CPU-controlled buffer 10                | 0x00C0  | R/W/SS   |
| <a href="#">SPI_W11_REG</a>                | SPI CPU-controlled buffer 11                | 0x00C4  | R/W/SS   |
| <a href="#">SPI_W12_REG</a>                | SPI CPU-controlled buffer 12                | 0x00C8  | R/W/SS   |
| <a href="#">SPI_W13_REG</a>                | SPI CPU-controlled buffer 13                | 0x00CC  | R/W/SS   |
| <a href="#">SPI_W14_REG</a>                | SPI CPU-controlled buffer 14                | 0x00D0  | R/W/SS   |
| <a href="#">SPI_W15_REG</a>                | SPI CPU-controlled buffer 15                | 0x00D4  | R/W/SS   |
| <b>Version register</b>                    |   |         |          |



| Name                         | Description     | Address | Access |
|------------------------------|-----------------|---------|--------|
| <a href="#">SPI_DATE_REG</a> | Version control | 0x00F0  | R/W    |

### 38.12.2 GP-SPI3 Register Summary

The addresses in this section are relative to GP-SPI3 base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column Access are explained in Section [Access Types for Registers](#).

| Name                                       | Description                                 | Address | Access   |
|--|---|---------|----------|
| <b>User-defined control registers</b>      |   |         |          |
| <a href="#">SPI_CMD_REG</a>                | Command control register                    | 0x0000  | varies   |
| <a href="#">SPI_ADDR_REG</a>               | Address value register                      | 0x0004  | R/W      |
| <a href="#">SPI_USER_REG</a>               | SPI USER control register                   | 0x0010  | varies   |
| <a href="#">SPI_USER1_REG</a>              | SPI USER control register 1                 | 0x0014  | R/W      |
| <a href="#">SPI_USER2_REG</a>              | SPI USER control register 2                 | 0x0018  | R/W      |
| <b>Control and configuration registers</b> |   |         |          |
| <a href="#">SPI_CTRL_REG</a>               | SPI control register                        | 0x0008  | R/W      |
| <a href="#">SPI_MS_DLEN_REG</a>            | SPI data bit length control register        | 0x001C  | R/W      |
| <a href="#">SPI_MISC_REG</a>               | SPI misc register                           | 0x0020  | R/W      |
| <a href="#">SPI_DMA_CONF_REG</a>           | SPI DMA control register                    | 0x0030  | varies   |
| <a href="#">SPI_SLAVE_REG</a>              | SPI slave control register                  | 0x00E0  | varies   |
| <a href="#">SPI_SLAVE1_REG</a>             | SPI slave control register 1                | 0x00E4  | R/W/SS   |
| <b>Clock control registers</b>             |   |         |          |
| <a href="#">SPI_CLOCK_REG</a>              | SPI clock control register                  | 0x000C  | R/W      |
| <a href="#">SPI_CLK_GATE_REG</a>           | SPI module clock and register clock control | 0x00E8  | R/W      |
| <b>Timing registers</b>                    |   |         |          |
| <a href="#">SPI_DIN_MODE_REG</a>           | SPI input delay mode configuration          | 0x0024  | R/W      |
| <a href="#">SPI_DIN_NUM_REG</a>            | SPI input delay number configuration        | 0x0028  | R/W      |
| <a href="#">SPI_DOUT_MODE_REG</a>          | SPI output delay mode configuration         | 0x002C  | R/W      |
| <b>Interrupt registers</b>                 |   |         |          |
| <a href="#">SPI_DMA_INT_ENA_REG</a>        | SPI interrupt enable register               | 0x0034  | R/W      |
| <a href="#">SPI_DMA_INT_CLR_REG</a>        | SPI interrupt clear register                | 0x0038  | WT       |
| <a href="#">SPI_DMA_INT_RAW_REG</a>        | SPI interrupt raw register                  | 0x003C  | R/WTC/SS |
| <a href="#">SPI_DMA_INT_ST_REG</a>         | SPI interrupt status register               | 0x0040  | RO       |
| <a href="#">SPI_DMA_INT_SET_REG</a>        | SPI interrupt software set register         | 0x0044  | WT       |
| <b>CPU-controlled data buffer</b>          |   |         |          |
| <a href="#">SPI_W0_REG</a>                 | SPI CPU-controlled buffer 0                 | 0x0098  | R/W/SS   |
| <a href="#">SPI_W1_REG</a>                 | SPI CPU-controlled buffer 1                 | 0x009C  | R/W/SS   |
| <a href="#">SPI_W2_REG</a>                 | SPI CPU-controlled buffer 2                 | 0x00A0  | R/W/SS   |
| <a href="#">SPI_W3_REG</a>                 | SPI CPU-controlled buffer 3                 | 0x00A4  | R/W/SS   |
| <a href="#">SPI_W4_REG</a>                 | SPI CPU-controlled buffer 4                 | 0x00A8  | R/W/SS   |
| <a href="#">SPI_W5_REG</a>                 | SPI CPU-controlled buffer 5                 | 0x00AC  | R/W/SS   |
| <a href="#">SPI_W6_REG</a>                 | SPI CPU-controlled buffer 6                 | 0x00B0  | R/W/SS   |

| Name                         | Description                  | Address | Access |
|------------------------------|------------------------------|---------|--------|
| <a href="#">SPI_W7_REG</a>   | SPI CPU-controlled buffer 7  | 0x00B4  | R/W/SS |
| <a href="#">SPI_W8_REG</a>   | SPI CPU-controlled buffer 8  | 0x00B8  | R/W/SS |
| <a href="#">SPI_W9_REG</a>   | SPI CPU-controlled buffer 9  | 0x00BC  | R/W/SS |
| <a href="#">SPI_W10_REG</a>  | SPI CPU-controlled buffer 10 | 0x00C0  | R/W/SS |
| <a href="#">SPI_W11_REG</a>  | SPI CPU-controlled buffer 11 | 0x00C4  | R/W/SS |
| <a href="#">SPI_W12_REG</a>  | SPI CPU-controlled buffer 12 | 0x00C8  | R/W/SS |
| <a href="#">SPI_W13_REG</a>  | SPI CPU-controlled buffer 13 | 0x00CC  | R/W/SS |
| <a href="#">SPI_W14_REG</a>  | SPI CPU-controlled buffer 14 | 0x00D0  | R/W/SS |
| <a href="#">SPI_W15_REG</a>  | SPI CPU-controlled buffer 15 | 0x00D4  | R/W/SS |
| <b>Version register</b>      |                              |         |        |
| <a href="#">SPI_DATE_REG</a> | Version control              | 0x00F0  | R/W    |

### 38.12.3 LP-SPI Register Summary

The addresses in this section are relative to LP-SPI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column Access are explained in Section *Access Types for Registers*.

| Name                                       | Description                                    | Address | Access |
|--|--|---------|--------|
| <b>User-defined control registers</b>      |  |         |        |
| <a href="#">LP_SPI_CMD_REG</a>             | Command control register                       | 0x0000  | varies |
| <a href="#">LP_SPI_ADDR_REG</a>            | Address value register                         | 0x0004  | R/W    |
| <a href="#">LP_SPI_USER_REG</a>            | LP-SPI USER control register                   | 0x0010  | R/W    |
| <a href="#">LP_SPI_USER1_REG</a>           | LP-SPI USER control register 1                 | 0x0014  | R/W    |
| <a href="#">LP_SPI_USER2_REG</a>           | LP-SPI USER control register 2                 | 0x0018  | R/W    |
| <b>Control and configuration registers</b> |  |         |        |
| <a href="#">LP_SPI_CTRL_REG</a>            | LP-SPI control register                        | 0x0008  | R/W    |
| <a href="#">LP_SPI_MS_DLEN_REG</a>         | LP-SPI data bit length control register        | 0x001C  | R/W    |
| <a href="#">LP_SPI_MISC_REG</a>            | LP-SPI misc register                           | 0x0020  | R/W    |
| <a href="#">LP_SPI_DMA_CONF_REG</a>        | LP-SPI DMA control register                    | 0x0030  | WT     |
| <a href="#">LP_SPI_SLEEP_CONFO_REG</a>     | LP-SPI sleep configure register 0              | 0x0044  | R/W    |
| <a href="#">LP_SPI_SLEEP_CONF1_REG</a>     | LP-SPI sleep configure register 1              | 0x0048  | R/W    |
| <a href="#">LP_SPI_SLAVE_REG</a>           | LP-SPI slave control register                  | 0x00E0  | varies |
| <a href="#">LP_SPI_SLAVE1_REG</a>          | LP-SPI slave control register 1                | 0x00E4  | R/W/SS |
| <b>Clock control registers</b>             |  |         |        |
| <a href="#">LP_SPI_CLOCK_REG</a>           | LP-SPI clock control register                  | 0x000C  | R/W    |
| <a href="#">LP_SPI_CLK_GATE_REG</a>        | LP-SPI module clock and register clock control | 0x00E8  | R/W    |
| <b>Timing registers</b>                    |  |         |        |
| <a href="#">LP_SPI_DIN_MODE_REG</a>        | LP-SPI input delay mode configuration          | 0x0024  | R/W    |
| <a href="#">LP_SPI_DIN_NUM_REG</a>         | LP-SPI input delay number configuration        | 0x0028  | R/W    |
| <a href="#">LP_SPI_DOUT_MODE_REG</a>       | LP-SPI output delay mode configuration         | 0x002C  | R/W    |
| <b>Interrupt registers</b>                 |  |         |        |
| <a href="#">LP_SPI_DMA_INT_ENA_REG</a>     | LP-SPI interrupt enable register               | 0x0034  | R/W    |

| Name                                   | Description                            | Address | Access   |
|--|--|---------|----------|
| <a href="#">LP_SPI_DMA_INT_CLR_REG</a> | LP-SPI interrupt clear register        | 0x0038  | WT       |
| <a href="#">LP_SPI_DMA_INT_RAW_REG</a> | LP-SPI interrupt raw register          | 0x003C  | R/WTC/SS |
| <a href="#">LP_SPI_DMA_INT_ST_REG</a>  | LP-SPI interrupt status register       | 0x0040  | RO       |
| <a href="#">LP_SPI_DMA_INT_SET_REG</a> | LP-SPI interrupt software set register | 0x004C  | WT       |
| <b>CPU-controlled data buffer</b>      |  |         |          |
| <a href="#">LP_SPI_W0_REG</a>          | LP-SPI CPU-controlled buffer 0         | 0x0098  | R/W/SS   |
| <a href="#">LP_SPI_W1_REG</a>          | LP-SPI CPU-controlled buffer 1         | 0x009C  | R/W/SS   |
| <a href="#">LP_SPI_W2_REG</a>          | LP-SPI CPU-controlled buffer 2         | 0x00A0  | R/W/SS   |
| <a href="#">LP_SPI_W3_REG</a>          | LP-SPI CPU-controlled buffer 3         | 0x00A4  | R/W/SS   |
| <a href="#">LP_SPI_W4_REG</a>          | LP-SPI CPU-controlled buffer 4         | 0x00A8  | R/W/SS   |
| <a href="#">LP_SPI_W5_REG</a>          | LP-SPI CPU-controlled buffer 5         | 0x00AC  | R/W/SS   |
| <a href="#">LP_SPI_W6_REG</a>          | LP-SPI CPU-controlled buffer 6         | 0x00B0  | R/W/SS   |
| <a href="#">LP_SPI_W7_REG</a>          | LP-SPI CPU-controlled buffer 7         | 0x00B4  | R/W/SS   |
| <a href="#">LP_SPI_W8_REG</a>          | LP-SPI CPU-controlled buffer 8         | 0x00B8  | R/W/SS   |
| <a href="#">LP_SPI_W9_REG</a>          | LP-SPI CPU-controlled buffer 9         | 0x00BC  | R/W/SS   |
| <a href="#">LP_SPI_W10_REG</a>         | LP-SPI CPU-controlled buffer 10        | 0x00C0  | R/W/SS   |
| <a href="#">LP_SPI_W11_REG</a>         | LP-SPI CPU-controlled buffer 11        | 0x00C4  | R/W/SS   |
| <a href="#">LP_SPI_W12_REG</a>         | LP-SPI CPU-controlled buffer 12        | 0x00C8  | R/W/SS   |
| <a href="#">LP_SPI_W13_REG</a>         | LP-SPI CPU-controlled buffer 13        | 0x00CC  | R/W/SS   |
| <a href="#">LP_SPI_W14_REG</a>         | LP-SPI CPU-controlled buffer 14        | 0x00D0  | R/W/SS   |
| <a href="#">LP_SPI_W15_REG</a>         | LP-SPI CPU-controlled buffer 15        | 0x00D4  | R/W/SS   |
| <b>Version register</b>                |  |         |          |
| <a href="#">LP_SPI_DATE_REG</a>        | Version control                        | 0x00F0  | R/W      |

## 38.13 Register

### 38.13.1 GP-SPI2 Register

The addresses in this section are relative to GP-SPI2 base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 38.1. SPI\_CMD\_REG (0x0000)**

|            |   |   |   |   |   |   |   |                       |    |            |    |   |   |   |   |  |    |                 |  |  |  |  |  |  |  |  |       |  |  |  |   |  |  |  |
|------------|---|---|---|---|---|---|---|-----------------------|----|------------|----|---|---|---|---|--|----|-----------------|--|--|--|--|--|--|--|--|-------|--|--|--|---|--|--|--|
| (reserved) |   |   |   |   |   |   |   | SPI_USR<br>SPI_UPDATE |    | (reserved) |    |   |   |   |   |  |    | SPI_CONF_BITLEN |  |  |  |  |  |  |  |  |       |  |  |  |   |  |  |  |
| 31         |   |   |   |   |   |   |   | 25                    | 24 | 23         | 22 |   |   |   |   |  | 18 | 17              |  |  |  |  |  |  |  |  |       |  |  |  | 0 |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                     | 0  | 0          | 0  | 0 | 0 | 0 | 0 |  |    |                 |  |  |  |  |  |  |  |  | Reset |  |  |  |   |  |  |  |

**SPI\_CONF\_BITLEN** Configures the SPI\_CLK cycles of SPI CONF state.

Measurement unit: SPI\_CLK clock cycle.

Can be configured in CONF state.

(R/W)

**SPI\_UPDATE** Configures whether or not to synchronize SPI registers from APB clock domain into SPI module clock domain.

0: Not synchronize

1: Synchronize

This bit is only used in SPI master transfer.

(WT)

**SPI\_USR** Configures whether or not to enable user-defined command.

0: Not enable

1: Enable

An SPI operation will be triggered when the bit is set. This bit will be cleared once the operation is done. Can not be changed by CONF\_buf.

(R/W/SC)

**Register 38.2. SPI\_ADDR\_REG (0x0004)**

|                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SPI_USR_ADDR_VALUE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SPI\_USR\_ADDR\_VALUE** Configures the address to slave. Can be configured in CONF state.

(R/W)

**Register 38.3. SPI\_USER\_REG (0x0010)**

| SPI_USR_COMMAND<br>SPI_USR_ADDR<br>SPI_USR_DUMMY<br>SPI_USR_MISO<br>SPI_USR_MOSI<br>SPI_USR_DUMMY_IDLE<br>SPI_USR_MOSI_HIGHPART<br>SPI_USR_MISO_HIGHPART<br><br>(reserved) |    |    |    |    |    |    |    |    |   | SPI_SIO<br>(reserved)<br>SPI_USR_CONF_NXT<br>SPI_FWRITE_OCT<br>SPI_FWRITE_QUAD<br>SPI_FWRITE_DUAL<br>(reserved)<br>SPI_CK_OUT_EDGE<br>SPI_RSCK_I_EDGE<br>SPI_CS_SETUP<br>SPI_TSCK_I_HOLD<br>SPI_OPI_MODE<br>SPI_QPI_MODE<br>(reserved)<br>SPI_DOUTDIN |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|---|---|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 |   | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 1  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

Reset

**SPI\_DOUTDIN** Configures whether or not to enable full-duplex communication.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_QPI\_MODE** Configures whether or not to enable QPI mode.

0: Disable

1: Enable

This configuration is applicable when the SPI controller works as master or slave. Can be configured in CONF state.

(R/W/SS/SC)

**SPI\_OPI\_MODE** Configures whether or not to enable OPI mode.

0: Disable. SPI controller works in other modes.

1: Enable. SPI controller works in OPI mode, all phases of which are in 8-bit mode.

This configuration is only applicable when the SPI controller works as master. Can be configured in CONF state.

(R/W)

**SPI\_TSCK\_I\_EDGE** Configures whether or not to change the polarity of TSCK in slave transfer.

0: TSCK = SPI\_CK\_I

1: TSCK = !SPI\_CK\_I

(R/W)

**SPI\_CS\_HOLD** Configures whether or not to keep SPI CS low when SPI is in DONE state.

0: Not keep low

1: Keep low

Can be configured in CONF state.

(R/W)

**SPI\_CS\_SETUP** Configures whether or not to enable SPI CS when SPI is in prepare (PREP) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.3. SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**SPI\_RSCK\_I\_EDGE** Configures whether or not to change the polarity of RSCK in slave transfer.

0: RSCK = !SPI\_CK\_I

1: RSCK = SPI\_CK\_I

(R/W)

**SPI\_CK\_OUT\_EDGE** Configures SPI clock mode together with SPI\_CK\_IDLE\_EDGE. Can be configured in CONF state. For more information, see Section [38.7.3](#).

(R/W)

**SPI\_FWRITE\_DUAL** Configures whether or not to enable the 2-bit mode of read-data phase in write operations.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FWRITE\_QUAD** Configures whether or not to enable the 4-bit mode of read-data phase in write operations.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FWRITE\_OCT** Configures whether or not to enable the 8-bit mode of read-data phase in write operations.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_CONF\_NXT** Configures whether or not to enable the CONF state for the next transaction (segment) in a configurable segmented transfer.

0: This transfer will end after the current transaction (segment) is finished. Or this is not a configurable segmented transfer.

1: This configurable segmented transfer will continue its next transaction (segment).

Can be configured in CONF state.

(R/W)

**SPI\_SIO** Configures whether or not to enable 3-line half-duplex communication, where MOSI and MISO signals share the same pin.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.3. SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**SPI\_USR\_MISO\_HIGHPART** Configures whether or not to enable High-Part mode in read-data phase, i.e., only access to high-part of the buffers: SPI\_W8\_REG ~ SPI\_W15\_REG.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_MOSI\_HIGHPART** Configures whether or not to enable High-Part mode in write-data phase, i.e., only access to high-part of the buffers: SPI\_W8\_REG ~ SPI\_W15\_REG.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_DUMMY\_IDLE** Configures whether or not to disable SPI clock in DUMMY state.

0: Not disable

1: Disable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_MOSI** Configures whether or not to enable the write-data (DOUT) state of an operation.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_MISO** Configures whether or not to enable the read-data (DIN) state of an operation.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_DUMMY** Configures whether or not to enable the DUMMY state of an operation.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_ADDR** Configures whether or not to enable the address (ADDR) state of an operation.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.3. SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**SPI\_USR\_COMMAND** Configures whether or not to enable the command (CMD) state of an operation.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)



**Register 38.4. SPI\_USER1\_REG (0x0014)**

|                     |    |  |  |                  |    |  |  |                   |    |  |  |                          |    |   |   |            |   |   |   |                        |   |       |  |
|---------------------|----|--|--|------------------|----|--|--|-------------------|----|--|--|--------------------------|----|---|---|------------|---|---|---|------------------------|---|-------|--|
| SPI_USR_ADDR_BITLEN |    |  |  | SPI_CS_HOLD_TIME |    |  |  | SPI_CS_SETUP_TIME |    |  |  | SPI_MST_WFULL_ERR_END_EN |    |   |   | (reserved) |   |   |   | SPI_USR_DUMMY_CYCLELEN |   |       |  |
| 31                  | 27 |  |  | 26               | 22 |  |  | 21                | 17 |  |  | 16                       | 15 | 8 |   |            | 7 | 0 |   |                        |   |       |  |
| 23                  |    |  |  | 0x1              |    |  |  | 0                 |    |  |  | 1                        | 0  | 0 | 0 | 0          | 0 | 0 | 0 | 0                      | 7 | Reset |  |

**SPI\_USR\_DUMMY\_CYCLELEN** Configures the length of DUMMY state.

Measurement unit: SPI\_CLK clock cycles.

This value is (the expected cycle number - 1).

Can be configured in CONF state.

(R/W)

**SPI\_MST\_WFULL\_ERR\_END\_EN** Configures whether or not to end the SPI transfer when SPI RX AFIFO wfull error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)

**SPI\_CS\_SETUP\_TIME** Configures the length of prepare (PREP) state.

Measurement unit: SPI\_CLK clock cycles.

This value is equal to the expected cycles - 1. This field is used together with SPI\_CS\_SETUP.

Can be configured in CONF state.

(R/W)

**SPI\_CS\_HOLD\_TIME** Configures the delay cycles of CS pin.

Measurement unit: SPI\_CLK clock cycles.

This field is used together with SPI\_CS\_HOLD.

Can be configured in CONF state.

(R/W)

**SPI\_USR\_ADDR\_BITLEN** Configures the bit length in address state.

This value is (expected bit number - 1).

Can be configured in CONF state.

(R/W)

### Register 38.5. SPI\_USER2\_REG (0x0018)

[illegible]

**SPI\_USR\_COMMAND\_VALUE** Configures the command value.

Can be configured in CONF state.

(R/W)

**SPI\_MST\_EMPTY\_ERR\_END\_EN** Configures whether or not to end the SPI transfer when SPI TX AFIFO read empty error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)

**SPI\_USR\_COMMAND\_BITLEN** Configures the bit length of command state.

This value is (expected bit number - 1).

Can be configured in CONF state.

(R/W)

### Register 38.6. SPI\_CTRL\_REG (0x0008)

[illegible]

**SPI\_DUMMY\_OUT** Configures whether or not to output the SPI2 bus signals in DUMMY state.

0: Not output

1: Output

Can be configured in CONF state.

(R/W)

**SPI\_FADDR\_DUAL** Configures whether or not to enable 2-bit mode during address (ADDR) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FADDR\_QUAD** Configures whether or not to enable 4-bit mode during address (ADDR) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FADDR\_OCT** Configures whether or not to enable 8-bit mode during address (ADDR) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FCMD\_DUAL** Configures whether or not to enable 2-bit mode during command (CMD) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FCMD\_QUAD** Configures whether or not to enable 4-bit mode during command (CMD) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.6. SPI\_CTRL\_REG (0x0008)**

Continued from the previous page...

**SPI\_FCMD\_OCT** Configures whether or not to enable 8-bit mode during command (CMD) state.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FREAD\_DUAL** Configures whether or not to enable the 2-bit mode of read-data (DIN) state in read operations.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FREAD\_QUAD** Configures whether or not to enable the 4-bit mode of read-data (DIN) state in read operations.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_FREAD\_OCT** Configures whether or not to enable the 8-bit mode of read-data (DIN) state in read operations.

0: Disable

1: Enable

Can be configured in CONF state. (R/W)

**SPI\_Q\_POL** Configures MISO line polarity.

0: Low

1: High

Can be configured in CONF state.

(R/W)

**SPI\_D\_POL** Configures MOSI line polarity.

0: Low

1: High

Can be configured in CONF state.

(R/W)

**SPI\_HOLD\_POL** Configures SPI\_HOLD output value when SPI is in idle.

0: Output low

1: Output high

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.6. SPI\_CTRL\_REG (0x0008)****Continued from the previous page...****SPI\_WP\_POL** Configures the output value of write-protect signal when SPI is in idle.

0: Output low

1: Output high

Can be configured in CONF state.

(R/W)

**SPI\_RD\_BIT\_ORDER** Configures the bit order in read-data (MISO) state.

0: MSB first

1: LSB first

2: MSB first

3: LSB first

Can be configured in CONF state. For more information, see Table 38.5-6.

(R/W)

**SPI\_WR\_BIT\_ORDER** Configures the bit order in command (CMD), address (ADDR), and write-data (MOSI) states.

0: MSB first

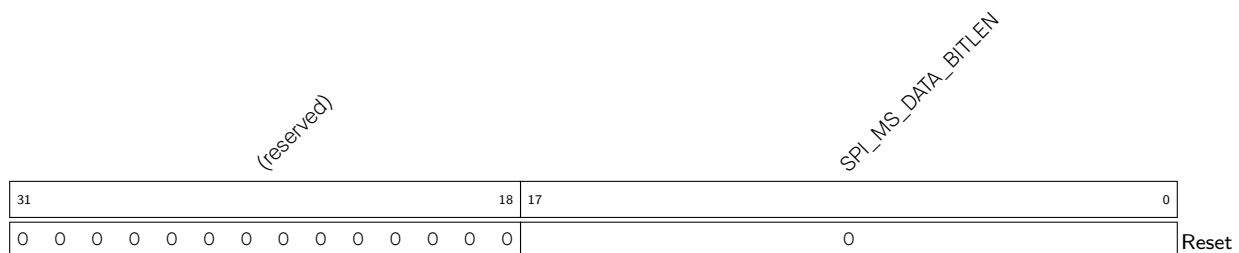
1: LSB first

2: MSB first

3: LSB first

Can be configured in CONF state. For more information, see Table 38.5-6.

(R/W)

**Register 38.7. SPI\_MS\_DLEN\_REG (0x001C)****SPI\_MS\_DATA\_BITLEN** Configures the data bit length of SPI transfer in DMA-controlled master transfer or in CPU-controlled master transfer. Or configures the bit length of SPI RX transfer in DMA-controlled slave transfer.

This value shall be (expected bit\_num - 1).

Can be configured in CONF state.

(R/W)

**Register 38.8. SPI\_MISC\_REG (0x0020)**

|  |    |    |    |   |    |    |    |   |    |    |    |  |    |    |    |   |   |   |   |   |   |   |   |   |
|--|----|----|----|---|----|----|----|---|----|----|----|--|----|----|----|---|---|---|---|---|---|---|---|---|
| SPI_QUAD_DIN_PIN_SWAP<br>SPI_CS_KEEP_ACTIVE<br>SPI_CLK_IDLE_EDGE<br>(reserved) |    |    |    | SPI_DQS_IDLE_EDGE<br>SPI_SLAVE_CS_POL<br>(reserved) |    |    |    | SPI_CMD_DTR_EN<br>SPI_ADDR_DTR_EN<br>SPI_DATA_DTR_EN<br>SPI_CLK_DATA_DTR_EN<br>(reserved) |    |    |    | SPI_MASTER_CS_POL<br><br>SPI_CLK_DIS<br>SPI_CS5_DIS<br>SPI_CS4_DIS<br>SPI_CS3_DIS<br>SPI_CS2_DIS<br>SPI_CS1_DIS<br>SPI_CS0_DIS |    |    |    |   |   |   |   |   |   |   |   |   |
| 31   | 30 | 29 | 28 | 25  | 24 | 23 | 22 | 20  | 19 | 18 | 17 | 16   | 15 | 13 | 12 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| 0  | 0  | 0  | 0  | 0   | 0  | 0  | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

Reset

Reset

**SPI\_CS0\_DIS** Configures whether or not to disable SPI\_CS0 pin.

0: SPI\_CS0 signal is from/to SPI\_CS0 pin.

1: Disable SPI\_CS0 pin.

Can be configured in CONF state.

(R/W)

**SPI\_CS1\_DIS** Configures whether or not to disable SPI\_CS1 pin.

0: SPI\_CS1 signal is from/to SPI\_CS1 pin.

1: Disable SPI\_CS1 pin.

Can be configured in CONF state.

(R/W)

**SPI\_CS2\_DIS** Configures whether or not to disable SPI\_CS2 pin.

0: SPI\_CS2 signal is from/to SPI\_CS2 pin.

1: Disable SPI\_CS2 pin.

Can be configured in CONF state.

(R/W)

**SPI\_CS3\_DIS** Configures whether or not to disable SPI\_CS3 pin.

0: SPI\_CS3 signal is from/to SPI\_CS3 pin.

1: Disable SPI\_CS3 pin.

Can be configured in CONF state.

(R/W)

**SPI\_CS4\_DIS** Configures whether or not to disable SPI\_CS4 pin.

0: SPI\_CS4 signal is from/to SPI\_CS4 pin.

1: Disable SPI\_CS4 pin.

Can be configured in CONF state.

(R/W)

**SPI\_CS5\_DIS** Configures whether or not to disable SPI\_CS5 pin.

0: SPI\_CS5 signal is from/to SPI\_CS5 pin.

1: Disable SPI\_CS5 pin.

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.8. SPI\_MISC\_REG (0x0020)**

Continued from the previous page...

**SPI\_CK\_DIS** Configures whether or not to disable SPI\_CLK output.

0: Enable

1: Disable

Can be configured in CONF state.

(R/W)

**SPI\_MASTER\_CS\_POL** Configures the polarity of SPI\_CS $n$  ( $n = 0\sim5$ ) line in master transfer.

0: SPI\_CS $n$  is low active.

1: SPI\_CS $n$  is high active.

Can be configured in CONF state.

(R/W)

**SPI\_CLK\_DATA\_DTR\_EN** Configures whether or not to enable DTR mode for SPI\_CLK, DATA, and SPI\_DQS when the SPI works as master.

0: Enable DTR mode only for SPI\_DQS

1: Enable DTR mode for SPI\_CLK, DATA, and SPI\_DQS.

This bit should be used with SPI\_DATA\_DTR\_EN, SPI\_ADDR\_DTR\_EN, and SPI\_CMD\_DTR\_EN.

(R/W)

**SPI\_DATA\_DTR\_EN** Configures whether or not to enable DTR mode for SPI\_CLK and DATA in DOUT and DIN states when the SPI works as master in 1/2/4/8-bit mode.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_ADDR\_DTR\_EN** Configures whether or not to enable DTR mode for SPI\_CLK and DATA in ADDR state when the SPI works as master in 1/2/4/8-bit mode.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_CMD\_DTR\_EN** Configures whether or not to enable DTR mode for SPI\_CLK and DATA in CMD state when the SPI works as master in 1/2/4/8-bit mode.

0: Not enable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_SLAVE\_CS\_POL** Configures whether or not to invert SPI slave input CS polarity.

0: Not change

1: Invert

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.8. SPI\_MISC\_REG (0x0020)**

Continued from the previous page...

**SPI\_DQS\_IDLE\_EDGE** Configured the default value of SPI\_DQS.

0: Low

1: High

Can be configured in CONF state.

(R/W)

**SPI\_CK\_IDLE\_EDGE** Configures the level of SPI\_CLK line when GP-SPI2 is in idle.

0: Low

1: High

Can be configured in CONF state.

(R/W)

**SPI\_CS\_KEEP\_ACTIVE** Configures whether or not to keep the SPI\_CS line low.

0: Not keep low

1: Keep low

Can be configured in CONF state.

(R/W)

**SPI\_QUAD\_DIN\_PIN\_SWAP** Configures whether or not to swap SPI Quad input pins.

0: Not swap

1: Swap SPI2D with SPI2Q, and SPI2WP with SPI2HD

Can be configured in CONF state.

(R/W)



**Register 38.9. SPI\_DMA\_CONF\_REG (0x0030)**

|  |    |    |    |    |            |    |   |   |   |   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |       |
|--|----|----|----|----|------------|----|---|---|---|---|----|----|----|----|----|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|-------|
| SPI_DMA_AFIFO_RST<br>SPI_BUF_AFIFO_RST<br>SPI_RX_AFIFO_RST<br>SPI_DMA_TX_ENA<br>SPI_DMA_RX_ENA<br>(reserved) |    |    |    |    | (reserved) |    |   |   |   |   |    |    |    |    |    |   |   |   |   | SPI_RX_EOF_EN<br>SPI_SLV_TX_SEG_TRANS_CLR_EN<br>SPI_SLV_RX_SEG_TRANS_CLR_EN<br>SPI_DMA_SLV_SEG_TRANS_EN<br>(reserved) |   |   |   |   | SPI_DMA_INFIFO_FULL<br>SPI_DMA_OUTFIFO_EMPTY |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26         | 22 |   |   |   |   | 21 | 20 | 19 | 18 | 17 | 2 |   |   |   |   |   |   |   |   |  | 1 | 0 |   |   |   |       |
| 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 1 | 1 | Reset |

Reset

**SPI\_DMA\_OUTFIFO\_EMPTY** Represents whether or not the DMA TX FIFO is ready for sending data.

0: Ready  
1: Not ready  
(RO)

**SPI\_DMA\_INFIFO\_FULL** Represents whether or not the DMA RX FIFO is ready for receiving data.

0: Ready  
1: Not ready  
(RO)

**SPI\_DMA\_SLV\_SEG\_TRANS\_EN** Configures whether or not to enable DMA-controlled segmented transfer in slave half-duplex communication.

0: Disable  
1: Enable  
(R/W)

**SPI\_SLV\_RX\_SEG\_TRANS\_CLR\_EN** In slave segmented transfer, if the size of the DMA RX buffer is smaller than the size of the received data,

1: the data in all the following Wr\_DMA transactions will not be received.  
0: the data in this Wr\_DMA transaction will not be received, but in the following transactions,  
- if the size of DMA RX buffer is not 0, the data in following Wr\_DMA transactions will be received.  
- if the size of DMA RX buffer is 0, the data in following Wr\_DMA transactions will not be received.  
(R/W)

**SPI\_SLV\_TX\_SEG\_TRANS\_CLR\_EN** In slave segmented transfer, if the size of the DMA TX buffer is smaller than the size of the transmitted data,

1: the data in the following transactions will not be updated, i.e. the old data is transmitted repeatedly.  
0: the data in this transaction will not be updated. But in the following transactions,  
- if new data is filled in DMA TX FIFO, new data will be transmitted.  
- if no new data is filled in DMA TX FIFO, no new data will be transmitted.  
(R/W)

Continued on the next page...

**Register 38.9. SPI\_DMA\_CONF\_REG (0x0030)**

Continued from the previous page...

**SPI\_RX\_EOF\_EN** Configures the trigger source of GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW.

0: GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW is set by SPI\_TRANS\_DONE\_INT event in a single transfer, or by an SPI\_DMA\_SEG\_TRANS\_DONE\_INT event in a segmented transfer.

1: In a DAM-controlled transfer, if the bit number of transferred data is equal to (SPI\_MS\_DATA\_BITLEN + 1), then GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW will be set by hardware.  
(R/W)

**SPI\_DMA\_RX\_ENA** Configures whether or not to enable DMA-controlled receive data transfer.

0: Disable

1: Enable

(R/W)

**SPI\_DMA\_TX\_ENA** Configures whether or not to enable DMA-controlled send data transfer.

0: Disable

1: Enable

(R/W)

**SPI\_RX\_AFIFO\_RST** Configures whether or not to reset RX AFIFO (i.e., spi\_rx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to receive data in SPI master and slave transfer.

0: Not reset

1: Reset

(WT)

**SPI\_BUF\_AFIFO\_RST** Configures whether or not to reset BUF TX AFIFO (i.e., buf\_tx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to send data out in SPI slave CPU-controlled transfer and master transfer.

0: Not reset

1: Reset

(WT)

**SPI\_DMA\_AFIFO\_RST** Configures whether or not to reset DMA TX AFIFO (i.e., dma\_tx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to send data out in SPI slave DMA-controlled transfer.

0: Not reset

1: Reset

(WT)

### Register 38.10. SPI\_SLAVE\_REG (0x00E0)

[illegible]

**SPI\_CLK\_MODE** Configures SPI clock mode.

- 0: SPI clock is off when CS becomes inactive.
- 1: SPI clock is delayed one cycle after CS becomes inactive.
- 2: SPI clock is delayed two cycles after CS becomes inactive.
- 3: SPI clock is always on.

Can be configured in CONF state.

(R/W)

**SPI\_CLK\_MODE\_13** Configures clock mode.

- 0: SPI clock mode 1 and mode 3. See Table 38.7-2.
- 1: SPI clock mode 0 and mode 2. See Table 38.7-2.

(R/W)

**SPI\_RSCK\_DATA\_OUT** Configures the edge of output data.

- 0: Output data at TSCK rising edge.  
1: Output data at RSCK rising edge.

(R/W)

**SPI\_SLV\_RDDMA\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Rd\_DMA transfer.

- 0: Not use  
1: Use

(R/W)

**SPI\_SLV\_WRDMA\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Wr DMA transfer.

- 0: Not use  
1: Use

(R/W)

**SPI\_SLV\_RDBUF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Rd\_BUF transfer.

- 0: Not use  
1: Use

(R/W)

Continued on the next page...

**Register 38.10. SPI\_SLAVE\_REG (0x00E0)**

Continued from the previous page...

**SPI\_SLV\_WRBUF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Wr\_BUF transfer.

0: Not use

1: Use

(R/W)

**SPI\_SLV\_LAST\_BYTE\_STRB** Represents the valid bits of the last received data byte in SPI slave full-duplex and half-duplex transfer.

(R/SS)

**SPI\_DMA\_SEG\_MAGIC\_VALUE** Configures the magic value of BM table in DMA-controlled configurable segmented transfer.

(R/W)

**SPI\_SLAVE\_MODE** Configures SPI work mode.

0: Master

1: Slave

(R/W)

**SPI\_SOFT\_RESET** Configures whether or not to reset the SPI clock line, CS line, and data line via software.

0: Not reset

1: Reset

Can be configured in CONF state.

(WT)

**SPI\_USR\_CONF** Configures whether or not to enable the CONF state of current DMA-controlled configurable segmented transfer.

0: No effect, which means the current transfer is not a configurable segmented transfer.

1: Enable, which means a configurable segmented transfer is started.

(R/W)

**SPI\_MST\_FD\_WAIT\_DMA\_TX\_DATA** Configures whether or not to wait DMA TX data gets ready before starting SPI transfer in master full-duplex transfer.

0: Not wait

1: Wait

(R/W)

Register 38.11. SPI\_SLAVE1\_REG (0x00E4)

|                   |    |    |    |    |   |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |       |
|-------------------|----|----|----|----|---|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|-------|
| SPI_SLV_LAST_ADDR |    |    |    |    |   |  |  |  |  | SPI_SLV_LAST_COMMAND |  |  |  |  |  |  |  |  |  | SPI_SLV_DATA_BITLEN |  |  |  |  |  |  |  |  |  |       |
| 31                | 26 | 25 | 18 | 17 | 0 |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |       |
| 0                 |    |    |    |    |   |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  |  |  | Reset |

**SPI\_SLV\_DATA\_BITLEN** Configures the transferred data bit length in SPI slave full-/half-duplex modes.  
(R/W/SS)

**SPI\_SLV\_LAST\_COMMAND** Configures the command value in slave mode.  
(R/W/SS)

**SPI\_SLV\_LAST\_ADDR** Configures the address value in slave mode.  
(R/W/SS)

### Register 38.12. SPI\_CLOCK\_REG (0x000C)

|    |    |    |    |     |    |     |    |     |   |       |
|----|----|----|----|-----|----|-----|----|-----|---|-------|
| 31 | 30 | 22 | 21 | 18  | 17 | 12  | 11 | 6   | 5 | 0     |
| 1  | 0  | 0  | 0  | 0   | 0  | 0   | 0  | 0   | 0 | 0     |
|    |    | 0  |    | 0x3 |    | 0x1 |    | 0x3 |   | Reset |

**SPI\_CLKCNT\_L** Configures clock duty cycles, together with SPI\_CLKCNT\_H and SPI\_CLKCNT\_N.

In master transfer, this field must be equal to SPI\_CLKCNT\_N.

In slave mode, it must be 0.

Can be configured in CONF state.

(R/W)

**SPI\_CLKCNT\_H** Configures the duty cycle of SPI\_CLK (high level) in master transfer.

It's recommended to configure this value to  $\text{floor}((\text{SPI\_CLKCNT\_N} + 1)/2 - 1)$ . `floor()` here is to round a number down, e.g.,  $\text{floor}(2.2) = 2$ .

In slave mode, it must be 0.

Can be configured in CONF state.

(R/W)

**SPI\_CLKCNT\_N** Configures the divider of SPI\_CLK in master transfer.

SPI\_CLK frequency is  $f_{\text{clk\_spi\_mst}} / (\text{SPI\_CLKDIV\_PRE} + 1) / (\text{SPI\_CLKCNT\_N} + 1)$ .

Can be configured in CONF state.

(R/W)

**SPI\_CLKDIV\_PRE** Configures the pre-divider of SPI\_CLK in master transfer.

Can be configured in CONF state.

(R/W)

**SPI\_CLK\_EQU\_SYSCLK** Configures whether or not the SPI\_CLK is equal to clk\_spi\_mst in master transfer.

0: SPI CLK is divided from clk spi mst.

1: SPI\_CLK is equal to clk\_spi\_mst.

Can be configured in CONF state.

(R/W)

Register 38.13. SPI\_CLK\_GATE\_REG (0x00E8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |            |            |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|------------|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   | (reserved) | SPI_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |            |            |   |   |   |   |   |   |   | 3 | 2 | 1 | 0 |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0          | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**SPI\_CLK\_EN** Configures whether or not to enable clock gate.  
0: Disable  
1: Enable  
(R/W)

### Register 38.14. SPI\_DIN\_MODE\_REG (0x0024)

[illegible]

**SPI\_DINO\_MODE** Configures the input mode for SPI2D signal.

- 0: Input without delay
- 1: Input at the (SPI\_DINO\_NUM + 1)th falling edge of clk\_spi\_mst
- 2: Input at the (SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle
- 3: Input at the (SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle
- Can be configured in CONF state.
- (R/W)

**SPI\_DIN1\_MODE** Configures the input mode for SPI2Q signal.

- 0: Input without delay
- 1: Input at the (SPI\_DIN1\_NUM+1)th falling edge of clk\_spi\_mst
- 2: Input at the (SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle
- 3: Input at the (SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle
- Can be configured in CONF state.
- (R/W)

**SPI\_DIN2\_MODE** Configures the input mode for SPI2WP signal.

- 0: Input without delay
- 1: Input at the (SPI\_DIN2\_NUM + 1)th falling edge of clk\_spi\_mst
- 2: Input at the (SPI\_DIN2\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle
- 3: Input at the (SPI\_DIN2\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle
- Can be configured in CONF state.
- (R/W)

Continued on the next page...



**Register 38.14. SPI\_DIN\_MODE\_REG (0x0024)**

Continued from the previous page...

**SPI\_DIN3\_MODE** Configures the input mode for SPI2HD signal.

0: Input without delay

1: Input at the (SPI\_DIN3\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN3\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN3\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

Can be configured in CONF state.

(R/W)

**SPI\_DIN4\_MODE** Configures the input mode for SPI2D4 signal.

0: Input without delay

1: Input at the (SPI\_DIN4\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN4\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN4\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

Can be configured in CONF state.

(R/W)

**SPI\_DIN5\_MODE** Configures the input mode for SPI2D5 signal.

0: Input without delay

1: Input at the (SPI\_DIN5\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN5\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN5\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

Can be configured in CONF state.

(R/W)

**SPI\_DIN6\_MODE** Configures the input mode for SPI2D6 signal.

0: Input without delay

1: Input at the (SPI\_DIN6\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN6\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN6\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.14. SPI\_DIN\_MODE\_REG (0x0024)**

Continued from the previous page...

**SPI\_DIN7\_MODE** Configures the input mode for SPI2D7 signal.

0: Input without delay

1: Input at the (SPI\_DIN7\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN7\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN7\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

Can be configured in CONF state.

(R/W)

**SPI\_TIMING\_HCLK\_ACTIVE** Configures whether or not to enable HCLK (high-frequency clock) in SPI input timing module.

0: Disable

1: Enable

Can be configured in CONF state. (R/W)

**Register 38.15. SPI\_DIN\_NUM\_REG (0x0028)**

| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | SPI_DIN7_NUM |    | SPI_DIN6_NUM |    | SPI_DIN5_NUM |    | SPI_DIN4_NUM |   | SPI_DIN3_NUM |   | SPI_DIN2_NUM |   | SPI_DIN1_NUM |   | SPI_DINO_NUM |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|--------------|----|--------------|----|--------------|----|--------------|---|--------------|---|--------------|---|--------------|---|--------------|---|
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15           | 14 | 13           | 12 | 11           | 10 | 9            | 8 | 7            | 6 | 5            | 4 | 3            | 2 | 1            | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0            | 0  | 0            | 0  | 0            | 0  | 0            | 0 | 0            | 0 | 0            | 0 | Reset        |   |              |   |

Reset

**SPI\_DINO\_NUM** Configures the delays to input signal SPI2D based on the setting of SPI\_DINO\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN1\_NUM** Configures the delays to input signal SPI2Q based on the setting of SPI\_DIN1\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN2\_NUM** Configures the delays to input signal SPI2WP based on the setting of SPI\_DIN2\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN3\_NUM** Configures the delays to input signal SPI2HD based on the setting of SPI\_DIN3\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

Continued on the next page...

**Register 38.15. SPI\_DIN\_NUM\_REG (0x0028)**

Continued from the previous page...

**SPI\_DIN4\_NUM** Configures the delays to input signal SPI2D4 based on the setting of SPI\_DIN4\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN5\_NUM** Configures the delays to input signal SPI2D5 based on the setting of SPI\_DIN5\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN6\_NUM** Configures the delays to input signal SPI2D6 based on the setting of SPI\_DIN6\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

**SPI\_DIN7\_NUM** Configures the delays to input signal SPI2D7 based on the setting of SPI\_DIN7\_MODE.

0: Delayed by 1 clock cycle

1: Delayed by 2 clock cycles

2: Delayed by 3 clock cycles

3: Delayed by 4 clock cycles

Can be configured in CONF state.

(R/W)

### Register 38.16. SPI\_DOUT\_MODE\_REG (0x002C)

[illegible]

**SPI\_DOUT0\_MODE** Configures the output mode for SPI2D signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_DOUT1\_MODE** Configures the output mode for SPI2Q signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_DOUT2\_MODE** Configures the output mode for SPI2WP signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_DOUT3\_MODE** Configures the output mode for SPI2HD signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_DOUT4\_MODE** Configures the output mode for SPI2D4 signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_DOUT5\_MODE** Configures the output mode for SPI2D5 signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI DOUT6 MODE** Configures the output mode for SPI2D6 signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**Register 38.16. SPI\_DOUT\_MODE\_REG (0x002C)**

Continued from the previous page...

**SPI\_DOUT7\_MODE** Configures the output mode for SPI2D7 signal.

0: Output without delay

1: Output with a delay of a SPI module clock cycle at its falling edge

Can be configured in CONF state.

(R/W)

**SPI\_D\_DQS\_MODE** Configures the output mode for output SPI\_DQS signal.

0: Output without delay

1: Output is delayed for a SPI clock cycle at its falling edge.

Can be configured in CONF state.

(R/W)

Register 38.17. SPI\_DMA\_INT\_ENA\_REG (0x0034)

|            |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|-------|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | SPI_APP1_INT_ENA<br>SPI_APP2_INT_ENA<br>SPI_MST_TX_INT_ENA<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_ENA<br>SPI_SLV_CMD_ERR_INT_ENA<br>SPI_SEG_MAGIC_ERR_INT_ENA<br>SPI_DMA_SEG_TRANS_DONE_INT_ENA<br>SPI_TRANS_DONE_INT_ENA<br>SPI_SLV_WR_BUF_DONE_INT_ENA<br>SPI_SLV_RD_BUF_DONE_INT_ENA<br>SPI_SLV_WR_DMA_DONE_INT_ENA<br>SPI_SLV_RD_DMA_DONE_INT_ENA<br>SPI_SLV_CMD9_INT_ENA<br>SPI_SLV_CMD8_INT_ENA<br>SPI_SLV_CMD7_INT_ENA<br>SPI_SLV_EX_QPI_INT_ENA<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_ENA<br>SPI_DMA_INFIFO_FULL_ERR_INT_ENA |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 21   | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_ENA** Write 1 to enable SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(R/W)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_ENA** Write 1 to enable SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/W)

**SPI\_SLV\_EX\_QPI\_INT\_ENA** Write 1 to enable SPI\_SLV\_EX\_QPI\_INT interrupt.  
(R/W)

**SPI\_SLV\_EN\_QPI\_INT\_ENA** Write 1 to enable SPI\_SLV\_EN\_QPI\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD7\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD7\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD8\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD8\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD9\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD9\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMDA\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMDA\_INT interrupt.  
(R/W)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(R/W)

**SPI\_TRANS\_DONE\_INT\_ENA** Write 1 to enable SPI\_TRANS\_DONE\_INT interrupt.  
(R/W)

Continued on the next page...

**Register 38.17. SPI\_DMA\_INT\_ENA\_REG (0x0034)**

Continued from the previous page...

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_ENA** Write 1 to enable SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(R/W)

**SPI\_SEG\_MAGIC\_ERR\_INT\_ENA** Write 1 to enable SPI\_SEG\_MAGIC\_ERR\_INT interrupt.  
(R/W)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(R/W)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(R/W)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/W)

**SPI\_APP2\_INT\_ENA** Write 1 to enable SPI\_APP2\_INT interrupt.  
(R/W)

**SPI\_APP1\_INT\_ENA** Write 1 to enable SPI\_APP1\_INT interrupt.  
(R/W)



(reserved)

SPI\_APP1\_INT\_CLR  
SPI\_APP2\_INT\_CLR  
SPI\_MST\_TX\_CLR  
SPI\_MST\_RX\_AFIFO\_EMPTY\_ERR\_INT\_CLR  
SPI\_SLV\_CMD\_ERR\_INT\_CLR  
SPI\_SLV\_BUF\_ADDRC\_ERR\_INT\_CLR  
SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_CLR  
SPI\_TRANS\_DONE\_INT\_CLR  
SPI\_SLV\_WR\_BUF\_DONE\_INT\_CLR  
SPI\_SLV\_RD\_BUF\_DONE\_INT\_CLR  
SPI\_SLV\_WR\_DMA\_DONE\_INT\_CLR  
SPI\_SLV\_RD\_DMA\_DONE\_INT\_CLR  
SPI\_SLV\_CMD0\_DONE\_INT\_CLR  
SPI\_SLV\_CMD1\_DONE\_INT\_CLR  
SPI\_SLV\_CMD2\_DONE\_INT\_CLR  
SPI\_SLV\_CMD3\_DONE\_INT\_CLR  
SPI\_SLV\_CMD4\_DONE\_INT\_CLR  
SPI\_SLV\_CMD5\_DONE\_INT\_CLR  
SPI\_SLV\_CMD6\_DONE\_INT\_CLR  
SPI\_SLV\_CMD7\_DONE\_INT\_CLR  
SPI\_SLV\_CMD8\_DONE\_INT\_CLR  
SPI\_SLV\_CMD9\_DONE\_INT\_CLR  
SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_CLR  
SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_CLR

**SPI\_TRANS\_DONE\_INT\_CLR** Write 1 to clear SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

PRELIMINARY

**Register 38.18. SPI\_DMA\_INT\_CLR\_REG (0x0038)**

Continued from the previous page...

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_CLR** Write 1 to clear SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(WT)

**SPI\_SEG\_MAGIC\_ERR\_INT\_CLR** Write 1 to clear SPI\_SEG\_MAGIC\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_APP2\_INT\_CLR** Write 1 to clear SPI\_APP2\_INT interrupt.  
(WT)

**SPI\_APP1\_INT\_CLR** Write 1 to clear SPI\_APP1\_INT interrupt.  
(WT)

Register 38.19. SPI\_DMA\_INT\_RAW\_REG (0x003C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SPI_APP1_INT_RAW<br>SPI_APP2_INT_RAW<br>SPI_MST_TX_AFIFO_EMPTY_ERR_INT_RAW<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_RAW<br>SPI_SLV_CMD_ERR_INT_RAW<br>SPI_SEG_MAGIC_ERR_INT_RAW<br>SPI_DMA_SEG_TRANS_DONE_INT_RAW<br>SPI_TRANS_DONE_INT_RAW<br>SPI_SLV_WR_BUF_DONE_INT_RAW<br>SPI_SLV_RD_BUF_DONE_INT_RAW<br>SPI_SLV_WR_DMA_DONE_INT_RAW<br>SPI_SLV_RD_DMA_DONE_INT_RAW<br>SPI_SLV_CMD9_INT_RAW<br>SPI_SLV_CMD8_INT_RAW<br>SPI_SLV_CMD7_INT_RAW<br>SPI_SLV_EN_QPI_INT_RAW<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_RAW<br>SPI_DMA_INFIFO_FULL_ERR_INT_RAW |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_RAW** The raw interrupt status of SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(R/WTC/SS)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_RAW** The raw interrupt status of SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_EX\_QPI\_INT\_RAW** The raw interrupt status of SPI\_SLV\_EX\_QPI\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_EN\_QPI\_INT\_RAW** The raw interrupt status of SPI\_SLV\_EN\_QPI\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD7\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD7\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD8\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD8\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD9\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD9\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMDA\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMDA\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/WTC/SS)

Continued on the next page...

**Register 38.19. SPI\_DMA\_INT\_RAW\_REG (0x003C)**

Continued from the previous page...

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of SPI\_TRANS\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_SEG\_MAGIC\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SEG\_MAGIC\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_SLV\_CMD\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_APP2\_INT\_RAW** The raw interrupt status of SPI\_APP2\_INT interrupt. The value is only controlled by the application.

(R/WTC/SS)

**SPI\_APP1\_INT\_RAW** The raw interrupt status of SPI\_APP1\_INT interrupt. The value is only controlled by the application.

(R/WTC/SS)

Register 38.20. SPI\_DMA\_INT\_ST\_REG (0x0040)

|            |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |    |    |    |    |    |    |    |    |    |    | SPI_APP1_INT_ST<br>SPI_APP2_INT_ST<br>SPI_MST_TX_INT_ST<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_ST<br>SPI_SLV_CMD_AFIFO_WFULL_ERR_INT_ST<br>SPI_SLV_BUF_ERR_INT_ST<br>SPI_SEG_MAGIC_ERR_INT_ST<br>SPI_DMA_SEG_TRANS_ERR_INT_ST<br>SPI_TRANS_DONE_INT_ST<br>SPI_SLV_WR_BUF_DONE_INT_ST<br>SPI_SLV_RD_BUF_DONE_INT_ST<br>SPI_SLV_WR_DMA_DONE_INT_ST<br>SPI_SLV_RD_DMA_DONE_INT_ST<br>SPI_SLV_CMDA_DONE_INT_ST<br>SPI_SLV_CMD9_INT_ST<br>SPI_SLV_CMD8_INT_ST<br>SPI_SLV_EN_QPI_INT_ST<br>SPI_SLV_EX_QPI_INT_ST<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_ST<br>SPI_DMA_INFIFO_FULL_ERR_INT_ST |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10  | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_ST** The interrupt status of SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(RO)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_ST** The interrupt status of SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(RO)

**SPI\_SLV\_EX\_QPI\_INT\_ST** The interrupt status of SPI\_SLV\_EX\_QPI\_INT interrupt.  
(RO)

**SPI\_SLV\_EN\_QPI\_INT\_ST** The interrupt status of SPI\_SLV\_EN\_QPI\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD7\_INT\_ST** The interrupt status of SPI\_SLV\_CMD7\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD8\_INT\_ST** The interrupt status of SPI\_SLV\_CMD8\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD9\_INT\_ST** The interrupt status of SPI\_SLV\_CMD9\_INT interrupt.  
(RO)

**SPI\_SLV\_CMDA\_INT\_ST** The interrupt status of SPI\_SLV\_CMDA\_INT interrupt.  
(RO)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(RO)

Continued on the next page...

**Register 38.20. SPI\_DMA\_INT\_ST\_REG (0x0040)**

Continued from the previous page...

**SPI\_TRANS\_DONE\_INT\_ST** The interrupt status of SPI\_TRANS\_DONE\_INT interrupt.  
(RO)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_ST** The interrupt status of SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(RO)

**SPI\_SEG\_MAGIC\_ERR\_INT\_ST** The interrupt status of SPI\_SEG\_MAGIC\_ERR\_INT interrupt.  
(RO)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ST** The status bit for SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD\_ERR\_INT\_ST** The interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(RO)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(RO)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(RO)

**SPI\_APP2\_INT\_ST** The interrupt status of SPI\_APP2\_INT interrupt.  
(RO)

**SPI\_APP1\_INT\_ST** The interrupt status of SPI\_APP1\_INT interrupt.  
(RO)

### Register 38.21. SPI\_DMA\_INT\_SET\_REG (0x0044)

[illegible]

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_SET** Write 1 to set SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(WT)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_SET** Write 1 to set SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT in-  
terrupt.  
(WT)

**SPI\_SLV\_EX\_QPI\_INT\_SET** Write 1 to set SPI\_SLV\_EX\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_EN\_QPI\_INT\_SET** Write 1 to set SPI\_SLV\_EN\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD7\_INT\_SET** Write 1 to set SPI\_SLV\_CMD7\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD8\_INT\_SET** Write 1 to set SPI\_SLV\_CMD8\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD9\_INT\_SET** Write 1 to set SPI\_SLV\_CMD9\_INT interrupt.  
(WT)

**SPI\_SLV\_CMDA\_INT\_SET** Write 1 to set SPI\_SLV\_CMDA\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(WT)

**SPI\_TRANS\_DONE\_INT\_SET** Write 1 to set SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

Continued on the next page...

**Register 38.21. SPI\_DMA\_INT\_SET\_REG (0x0044)**

Continued from the previous page...

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_SET** Write 1 to set SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(WT)

**SPI\_SEG\_MAGIC\_ERR\_INT\_SET** Write 1 to set SPI\_SEG\_MAGIC\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_APP2\_INT\_SET** Write 1 to set SPI\_APP2\_INT interrupt.  
(WT)

**SPI\_APP1\_INT\_SET** Write 1 to set SPI\_APP1\_INT interrupt.  
(WT)

**Register 38.22. SPI\_W0\_REG (0x0098)**

|          |   |
|----------|---|
| SPI_BUFO |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUFO** 32-bit data buffer 0.  
(R/W/SS)



## SPI\_BUF1

**SPI\_BUF1** 32-bit data buffer 1.  
(R/W/SS)

## SPI\_BUF2

**SPI\_BUF2** 32-bit data buffer 2.  
(R/W/SS)

## SPI\_BUF3

**SPI\_BUF3** 32-bit data buffer 3.  
(R/W/SS)

## SPI\_BUF4

**SPI\_BUF4** 32-bit data buffer 4.  
(R/W/SS)

## Register 38.27. SPI\_W5\_REG (0x00AC)

|          |   |
|----------|---|
| SPI_BUF5 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF5** 32-bit data buffer 5.  
(R/W/SS)

## Register 38.28. SPI\_W6\_REG (0x00B0)

|          |   |
|----------|---|
| SPI_BUF6 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF6** 32-bit data buffer 6.  
(R/W/SS)

## Register 38.29. SPI\_W7\_REG (0x00B4)

|          |   |
|----------|---|
| SPI_BUF7 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF7** 32-bit data buffer 7.  
(R/W/SS)

## Register 38.30. SPI\_W8\_REG (0x00B8)

|          |   |
|----------|---|
| SPI_BUF8 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF8** 32-bit data buffer 8.  
(R/W/SS)

**Register 38.31. SPI\_W9\_REG (0x00BC)**

|                 |   |
|-----------------|---|
| <i>SPI_BUF9</i> |   |
| 31              | 0 |
| 0               |   |
| Reset           |   |

**SPI\_BUF9** 32-bit data buffer 9.  
(R/W/SS)

**Register 38.32. SPI\_W10\_REG (0x00C0)**

|                  |   |
|------------------|---|
| <i>SPI_BUF10</i> |   |
| 31               | 0 |
| 0                |   |
| Reset            |   |

**SPI\_BUF10** 32-bit data buffer 10.  
(R/W/SS)

**Register 38.33. SPI\_W11\_REG (0x00C4)**

|                  |   |
|------------------|---|
| <i>SPI_BUF11</i> |   |
| 31               | 0 |
| 0                |   |
| Reset            |   |

**SPI\_BUF11** 32-bit data buffer 11.  
(R/W/SS)

**Register 38.34. SPI\_W12\_REG (0x00C8)**

|                  |   |
|------------------|---|
| <i>SPI_BUF12</i> |   |
| 31               | 0 |
| 0                |   |
| Reset            |   |

**SPI\_BUF12** 32-bit data buffer 12.  
(R/W/SS)

Register 38.35. SPI\_W13\_REG (0x00CC)

|           |   |
|-----------|---|
| SPI_BUF13 |   |
| 31        | 0 |
| 0         |   |
| Reset     |   |

SPI\_BUF13 32-bit data buffer 13.  
(R/W/SS)

Register 38.36. SPI\_W14\_REG (0x00D0)

|           |   |
|-----------|---|
| SPI_BUF14 |   |
| 31        | 0 |
| 0         |   |
| Reset     |   |

SPI\_BUF14 32-bit data buffer 14.  
(R/W/SS)

Register 38.37. SPI\_W15\_REG (0x00D4)

|           |   |
|-----------|---|
| SPI_BUF15 |   |
| 31        | 0 |
| 0         |   |
| Reset     |   |

SPI\_BUF15 32-bit data buffer 15.  
(R/W/SS)

Register 38.38. SPI\_DATE\_REG (0x00F0)

|            |    |           |   |
|------------|----|-----------|---|
| (reserved) |    | SPI_DATE  |   |
| 31         | 28 | 27        | 0 |
| 0          | 0  | 0         | 0 |
|            |    | 0x2207202 |   |
|            |    | Reset     |   |

SPI\_DATE Version control register.  
(R/W)

38.13.2 GP-SPI3 Register

The addresses in this section are relative to GP-SPI3 base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

Register 38.39. SPI\_CMD\_REG (0x0000)

|            |  |  |  |  |  |  |                       |  |            |  |  |  |  |    |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|--|--|--|--|--|--|-----------------------|--|------------|--|--|--|--|----|----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |  |  |  |  |  |  | SPI_USR<br>SPI_UPDATE |  | (reserved) |  |  |  |  |    |    |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         |  |  |  |  |  |  | 25                    |  |            |  |  |  |  | 24 | 23 | 22 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          |  |  |  |  |  |  | 0                     |  |            |  |  |  |  | 0  | 0  | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | Reset |

**SPI\_UPDATE** Configures whether or not to synchronize SPI registers from APB clock domain into SPI module clock domain.  
0: Not synchronize  
1: Synchronize  
This bit is only used in SPI master transfer.  
(WT)

**SPI\_USR** Configures whether or not to enable user-defined command.  
0: Not enable  
1: Enable  
An SPI operation will be triggered when the bit is set. This bit will be cleared once the operation is done.  
(R/W/SC)

Register 38.40. SPI\_ADDR\_REG (0x0004)

|                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| SPI_USR_ADDR_VALUE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**SPI\_USR\_ADDR\_VALUE** Configures the address to slave.  
(R/W)

Register 38.41. SPI\_USER\_REG (0x0010)

| SPI_USR_COMMAND |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |    |  |   |  |    |  |    | SPI_USR_ADDR |    |  |   |  |    |  |    |  |    |  |    |  |    |  |   |  |   |  |   |  |   |  | SPI_USR_DUMMY |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_USR_MISO |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | SPI_USR_MOSI |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_USR_DUMMY_IDLE |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | SPI_USR_MOSI_HIGHPART |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_USR_MISO_HIGHPART |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_SIO |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_FWRITE_QUAD |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | SPI_FWRITE_DUAL |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | (reserved) |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | SPI_CK_OUT_EDGE |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_RSCK_I_EDGE |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | SPI_CS_SETUP |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_CS_HOLD |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_TSCK_I_EDGE |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_QPI_MODE |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  | (reserved) |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   | SPI_DOUTDIN |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |
|-----------------|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|----|--|---|--|----|--|----|--------------|----|--|---|--|----|--|----|--|----|--|----|--|----|--|---|--|---|--|---|--|---|--|---------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|--------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--------------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|-----------------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-----------------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|---------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-----------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|-----------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|-----------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-----------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|--------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-----------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|------------|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|-------------|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|---|--|
| 31              |  | 30 |  | 29 |  | 28 |  | 27 |  | 26 |  | 25 |  | 24 |  | 23 |  |   |  | 18 |  | 17 |              | 16 |  |   |  | 14 |  | 13 |  | 12 |  | 11 |  | 10 |  | 9 |  | 8 |  | 7 |  | 6 |  | 5             |  | 4 |  | 3 |  | 2 |  | 1 |  | 0 |  |   |  |   |  |   |  |   |  |   |  |   |              |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |              |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |                    |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |                       |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |                       |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |         |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |                 |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |                 |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |            |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |                 |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |                 |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |              |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |             |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |                 |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |              |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |            |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |             |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |   |  |
| 1               |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0 |  | 0  |  | 0  |              | 0  |  | 0 |  | 0  |  | 0  |  | 0  |  | 0  |  | 0  |  | 0 |  | 0 |  | 0 |  | 1 |  | 1             |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |              | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0            |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |                    | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0                     |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |                       | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |         | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |                 | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0               |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |            | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0               |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |                 | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0            |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |             | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |                 | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |              | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0          |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |             | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  | 0 |  |

Reset

**SPI\_DOUTDIN** Configures whether or not to enable full-duplex communication.

0: Disable

1: Enable

(R/W)

**SPI\_QPI\_MODE** Configures whether or not to enable QPI mode.

0: Disable

1: Enable

This configuration is applicable when the SPI controller works as master or slave.

(R/W/SS/SC)

**SPI\_TSCK\_I\_EDGE** Configures whether or not to change the polarity of TSCK in slave transfer.

0: TSCK = SPI\_CK\_I

1: TSCK = !SPI\_CK\_I

(R/W)

**SPI\_CS\_HOLD** Configures whether or not to keep SPI CS low when SPI is in DONE state.

0: Not keep low

1: Keep low

(R/W)

**SPI\_CS\_SETUP** Configures whether or not to enable SPI CS when SPI is in prepare (PREP) state.

0: Disable

1: Enable

(R/W)

**SPI\_RSCK\_I\_EDGE** Configures whether or not to change the polarity of RSCK in slave transfer.

0: RSCK = !SPI\_CK\_I

1: RSCK = SPI\_CK\_I

(R/W)

**SPI\_CK\_OUT\_EDGE** Configures SPI clock mode together with SPI\_CK\_IDLE\_EDGE. For more information, see Section 38.7.3.

(R/W)

Continued on the next page...

**Register 38.41. SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**SPI\_FWRITE\_DUAL** Configures whether or not to enable the 2-bit mode of read-data phase in write operations.

0: Not enable

1: Enable

(R/W)

**SPI\_FWRITE\_QUAD** Configures whether or not to enable the 4-bit mode of read-data phase in write operations.

0: Not enable

1: Enable

(R/W)

**SPI\_SIO** Configures whether or not to enable 3-line half-duplex communication, where MOSI and MISO signals share the same pin.

0: Disable

1: Enable

(R/W)

**SPI\_USR\_MISO\_HIGHPART** Configures whether or not to enable High-Part mode in read-data phase, i.e., only access to high-part of the buffers: SPI\_W8\_REG ~ SPI\_W15\_REG.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_MOSI\_HIGHPART** Configures whether or not to enable High-Part mode in write-data phase, i.e., only access to high-part of the buffers: SPI\_W8\_REG ~ SPI\_W15\_REG.

0: Disable

1: Enable

Can be configured in CONF state.

(R/W)

**SPI\_USR\_DUMMY\_IDLE** Configures whether or not to disable SPI clock in DUMMY state.

0: Not disable

1: Disable

(R/W)

**SPI\_USR\_MOSI** Configures whether or not to enable the write-data (DOUT) state of an operation.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 38.41. SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**SPI\_USR\_MISO** Configures whether or not to enable the read-data (DIN) state of an operation.

0: Disable

1: Enable

(R/W)

**SPI\_USR\_DUMMY** Configures whether or not to enable the DUMMY state of an operation.

0: Disable

1: Enable

(R/W)

**SPI\_USR\_ADDR** Configures whether or not to enable the address (ADDR) state of an operation.

0: Disable

1: Enable

(R/W)

**SPI\_USR\_COMMAND** Configures whether or not to enable the command (CMD) state of an operation.

0: Disable

1: Enable

(R/W)



**Register 38.42. SPI\_USER1\_REG (0x0014)**

|                          |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
|--------------------------|----|-----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|
| SPI_USR_ADDR_BITLEN      |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| SPI_CS_HOLD_TIME         |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| SPI_CS_SETUP_TIME        |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| SPI_MST_WFULL_ERR_END_EN |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| (reserved)               |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| SPI_USR_DUMMY_CYCLELEN   |    |     |    |    |    |    |    |   |   |   |   |   |   |   |   |       |
| 31                       | 27 | 26  | 22 | 21 | 17 | 16 | 15 | 8 | 7 | 0 |   |   |   |   |   |       |
| 23                       |    | 0x1 |    | 0  |    | 1  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 7 | Reset |

**SPI\_USR\_DUMMY\_CYCLELEN** Configures the length of DUMMY state.

Measurement unit: SPI\_CLK clock cycles.

This value is (the expected cycle number - 1).

(R/W)

**SPI\_MST\_WFULL\_ERR\_END\_EN** Configures whether or not to end the SPI transfer when SPI RX AFIFO wfull error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)

**SPI\_CS\_SETUP\_TIME** Configures the length of prepare (PREP) state.

Measurement unit: SPI\_CLK clock cycles.

This value is equal to the expected cycles - 1. This field is used together with SPI\_CS\_SETUP.

(R/W)

**SPI\_CS\_HOLD\_TIME** Configures the delay cycles of CS pin.

Measurement unit: SPI\_CLK clock cycles.

This field is used together with SPI\_CS\_HOLD.

(R/W)

**SPI\_USR\_ADDR\_BITLEN** Configures the bit length in address state.

This value is (expected bit number - 1).

(R/W)

### Register 38.43. SPI\_USER2\_REG (0x0018)

|                        |  |  |  |  |  |  |    |  |  |  |  |  |  |                           |  |  |  |  |  |  |    |  |  |  |  |  |  |            |  |  |  |  |  |  |    |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------------|--|--|--|--|--|--|----|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|----|--|--|--|--|--|--|------------|--|--|--|--|--|--|----|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|
| SPI_USR_COMMAND_BITLEN |  |  |  |  |  |  |    |  |  |  |  |  |  | SPI_MST_EMPTY_ERR_END_EN  |  |  |  |  |  |  |    |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |    |  |  |  |  |  |  | SPI_USR_COMMAND_VALUE |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                     |  |  |  |  |  |  | 28 |  |  |  |  |  |  | 27                        |  |  |  |  |  |  | 26 |  |  |  |  |  |  | 16         |  |  |  |  |  |  | 15 |  |  |  |  |  |  | 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 7                      |  |  |  |  |  |  | 1  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  | 0  |  |  |  |  |  |  | Reset      |  |  |  |  |  |  |    |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |

**SPI\_USR\_COMMAND\_VALUE** Configures the command value.

(R/W)

**SPI\_MST\_EMPTY\_ERR\_END\_EN** Configures whether or not to end the SPI transfer when SPI TX AFIFO read empty error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)

**SPI\_USR\_COMMAND\_BITLEN** Configures the bit length of command state. This value is (expected bit number - 1).

(R/W)

### Register 38.44. SPI\_CTRL\_REG (0x0008)

[illegible]

**SPI\_DUMMY\_OUT** Configures whether or not to output the SPI3 bus signals in DUMMY state.

0: Not output

1: Output

(R/W)

**SPI\_FADDR\_DUAL** Configures whether or not to enable 2-bit mode during address (ADDR) state.

0: Disable

1: Enable

(R/W)

**SPI\_FADDR\_QUAD** Configures whether or not to enable 4-bit mode during address (ADDR) state.

0: Disable

1: Enable

(R/W)

**SPI\_FCMD\_DUAL** Configures whether or not to enable 2-bit mode during command (CMD) state.

0: Disable

1: Enable

(R/W)

**SPI\_FCMD\_QUAD** Configures whether or not to enable 4-bit mode during command (CMD) state.

0: Disable

1: Enable

(R/W)

**SPI\_FREAD\_DUAL** Configures whether or not to enable the 2-bit mode of read-data (DIN) state in read operations.

0: Disable

1: Enable

(R/W)

**SPI\_FREAD\_QUAD** Configures whether or not to enable the 4-bit mode of read-data (DIN) state in read operations.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 38.44. SPI\_CTRL\_REG (0x0008)**

Continued from the previous page...

**SPI\_Q\_POL** Configures MISO line polarity.

0: Low

1: High

(R/W)

**SPI\_D\_POL** Configures MOSI line polarity.

0: Low

1: High

(R/W)

**SPI\_HOLD\_POL** Configures SPI\_HOLD output value when SPI is in idle.

0: Output low

1: Output high

(R/W)

**SPI\_WP\_POL** Configures the output value of write-protect signal when SPI is in idle.

0: Output low

1: Output high

(R/W)

**SPI\_RD\_BIT\_ORDER** Configures the bit order in read-data (MISO) state.

0: MSB first

1: LSB first

2: MSB first

3: LSB first

(R/W)

**SPI\_WR\_BIT\_ORDER** Configures the bit order in command (CMD), address (ADDR), and write-data (MOSI) states.

0: MSB first

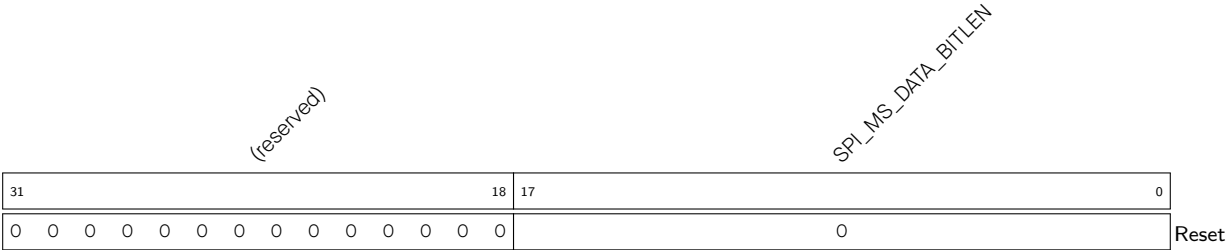
1: LSB first

2: MSB first

3: LSB first

(R/W)

Register 38.45. SPI\_MS\_DLEN\_REG (0x001C)



**SPI\_MS\_DATA\_BITLEN** Configures the data bit length of SPI transfer in CPU-controlled master transfer. Or configures the bit length of SPI RX transfer in DMA-controlled slave transfer. This value shall be (expected bit\_num - 1).  
(R/W)

Register 38.46. SPI\_MISC\_REG (0x0020)

|  |    |    |    |                                |    |    |    |  |   |   |   |   |   |   |   |
|--|----|----|----|--------------------------------|----|----|----|--|---|---|---|---|---|---|---|
| SPI_QUAD_DIN_PIN_SWAP<br>SPI_CS_KEEP_ACTIVE<br>SPI_CLK_IDLE_EDGE<br>(reserved) |    |    |    | SPI_SLAVE_CS_POL<br>(reserved) |    |    |    | SPI_MASTER_CS_POL<br>SPI_CLK_DIS<br>(reserved) |   |   |   | SPI_CS2_DIS<br>SPI_CS1_DIS<br>SPI_CS0_DIS |   |   |   |
| 31   | 30 | 29 | 28 | 24                             | 23 | 22 | 10 | 9  | 7 | 6 | 5 | 3   | 2 | 1 | 0 |
| 0  | 0  | 0  | 0  | 0                              | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0   | 0 | 1 | 0 |

Reset

**SPI\_CS0\_DIS** Configures whether or not to disable SPI\_CS0 pin.

0: SPI\_CS0 signal is from/to SPI\_CS0 pin.

1: Disable SPI\_CS0 pin.

(R/W)

**SPI\_CS1\_DIS** Configures whether or not to disable SPI\_CS1 pin.

0: SPI\_CS1 signal is from/to SPI\_CS1 pin.

1: Disable SPI\_CS1 pin.

(R/W)

**SPI\_CS2\_DIS** Configures whether or not to disable SPI\_CS2 pin.

0: SPI\_CS2 signal is from/to SPI\_CS2 pin.

1: Disable SPI\_CS2 pin.

(R/W)

**SPI\_CLK\_DIS** Configures whether or not to disable SPI\_CLK output.

0: Enable

1: Disable

(R/W)

**SPI\_MASTER\_CS\_POL** Configures the polarity of SPI\_CS $n$  ( $n = 0\sim 2$ ) line in master transfer.

0: SPI\_CS $n$  is low active.

1: SPI\_CS $n$  is high active.

(R/W)

**SPI\_SLAVE\_CS\_POL** Configures whether or not invert SPI slave input CS polarity.

0: Not change

1: Invert

(R/W)

**SPI\_CLK\_IDLE\_EDGE** Configures the level of SPI\_CLK line when GP-SPI3 is in idle.

0: Low

1: High

(R/W)

**SPI\_CS\_KEEP\_ACTIVE** Configures whether or not to keep the SPI\_CS line low.

0: Not keep low

1: Keep low

(R/W)

Continued on the next page...

**Register 38.46. SPI\_MISC\_REG (0x0020)**

Continued from the previous page...

**SPI\_QUAD\_DIN\_PIN\_SWAP** Configures whether or not to swap SPI Quad input pins.

0: Not swap

1: Swap SPI3\_D with SPI3\_Q, and SPI3\_WP with SPI3\_HD

(R/W)

**Register 38.47. SPI\_DMA\_CONF\_REG (0x0030)**

|  |    |    |    |    |   |    |   |   |   |   |    |    |    |    |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |   |   |
|--|----|----|----|----|---|----|---|---|---|---|----|----|----|----|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|--|---|---|
| SPI_DMA_AFIFO_RST<br>SPI_BUF_AFIFO_RST<br>SPI_RX_AFIFO_RST<br>SPI_DMA_TX_ENA<br>SPI_DMA_RX_ENA<br>(reserved) |    |    |    |    | SPI_RX_EOF_EN<br>SPI_SLV_TX_SEG_TRANS_CLR_EN<br>SPI_SLV_RX_SEG_TRANS_CLR_EN<br>SPI_DMA_SLV_SEG_TRANS_EN<br>(reserved) |    |   |   |   |   |    |    |    |    | SPI_DMA_INFIFO_FULL<br>SPI_DMA_OUTFIFO_EMPTY |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |  |   |   |
| 31   | 30 | 29 | 28 | 27 | 26  | 22 |   |   |   |   | 21 | 20 | 19 | 18 | 17   |   |   |   |   |   |   |   |   |   | 2 |   |   |   |   |   |   |   |       |  | 1 | 0 |
| 0  | 0  | 0  | 0  | 0  | 0   | 0  | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | Reset |  |   |   |

Reset

**SPI\_DMA\_OUTFIFO\_EMPTY** Represents whether or not the DMA TX FIFO is ready for sending data.

0: Ready  
1: Not ready  
(RO)

**SPI\_DMA\_INFIFO\_FULL** Represents whether or not the DMA RX FIFO is ready for receiving data.

0: Ready  
1: Not ready  
(RO)

**SPI\_DMA\_SLV\_SEG\_TRANS\_EN** Configures whether or not to enable DMA-controlled segmented transfer in slave half-duplex communication.

0: Disable  
1: Enable  
(R/W)

**SPI\_SLV\_RX\_SEG\_TRANS\_CLR\_EN** In slave segmented transfer, if the size of the DMA RX buffer is smaller than the size of the received data,

1: the data in all the following Wr\_DMA transactions will not be received  
0: the data in this Wr\_DMA transaction will not be received, but in the following transactions,  
- if the size of DMA RX buffer is not 0, the data in following Wr\_DMA transactions will be received.  
- if the size of DMA RX buffer is 0, the data in following Wr\_DMA transactions will not be received.  
(R/W)

**SPI\_SLV\_TX\_SEG\_TRANS\_CLR\_EN** In slave segmented transfer, if the size of the DMA TX buffer is smaller than the size of the transmitted data,

1: the data in the following transactions will not be updated, i.e. the old data is transmitted repeatedly.  
0: the data in this transaction will not be updated. But in the following transactions,  
- if new data is filled in DMA TX FIFO, new data will be transmitted. - if no new data is filled in DMA TX FIFO, no new data will be transmitted.  
(R/W)

Continued on the next page...



**Register 38.47. SPI\_DMA\_CONF\_REG (0x0030)**

Continued from the previous page...

**SPI\_RX\_EOF\_EN** Configures the trigger source of GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW.

0: GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW is set by SPI\_TRANS\_DONE\_INT event in a single transfer, or by an SPI\_DMA\_SEG\_TRANS\_DONE\_INT event in a segmented transfer.

1: In a DAM-controlled transfer, if the bit number of transferred data is equal to (SPI\_MS\_DATA\_BITLEN + 1), then GDMA\_IN\_SUC\_EOF\_CH $n$ \_INT\_RAW will be set by hardware.  
(R/W)

**SPI\_DMA\_RX\_ENA** Configures whether or not to enable DMA-controlled receive data transfer.

0: Disable

1: Enable

(R/W)

**SPI\_DMA\_TX\_ENA** Configures whether or not to enable DMA-controlled send data transfer.

0: Disable

1: Enable

(R/W)

**SPI\_RX\_AFIFO\_RST** Configures whether or not to reset RX AFIFO (i.e., spi\_rx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to receive data in SPI master and slave transfer.

0: Not reset

1: Reset

(WT)

**SPI\_BUF\_AFIFO\_RST** Configures whether or not to reset BUF TX AFIFO (i.e., buf\_tx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to send data out in SPI slave CPU-controlled transfer and master transfer.

0: Not reset

1: Reset

(WT)

**SPI\_DMA\_AFIFO\_RST** Configures whether or not to reset DMA TX AFIFO (i.e., dma\_tx\_afifo in Figure 38.5-3 and Figure 38.5-4), which is used to send data out in SPI slave DMA-controlled transfer.

0: Not reset

1: Reset

(WT)

### Register 38.48. SPI\_SLAVE\_REG (0x00E0)

[illegible]

**SPI\_CLK\_MODE** Configures SPI clock mode.

- 0: SPI clock is off when CS becomes inactive.
- 1: SPI clock is delayed one cycle after CS becomes inactive.
- 2: SPI clock is delayed two cycles after CS becomes inactive.
- 3: SPI clock is always on.

(R/W)

**SPI\_CLK\_MODE\_13** Configures clock mode.

- 0: SPI clock mode 1 and mode 3. See Table 38.7-2.  
1: SPI clock mode 0 and mode 2. See Table 38.7-2.

(R/W)

**SPI\_RSCK\_DATA\_OUT** Configures the edge of output data.

- 0: Output data at TSCK rising edge.  
1: Output data at RSCK rising edge.

(R/W)

**SPI\_SLV\_RDDMA\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Rd\_DMA transfer.

- 0: Not use  
1: Use

(R/W)

**SPI\_SLV\_WRDMA\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Wr\_DMA transfer.

- 0: Not use  
1: Use

(R/W)

**SPI\_SLV\_RDBUF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Rd\_BUF transfer.

- 0: Not use  
1: Use

(R/W)

Continued on the next page...

**Register 38.48. SPI\_SLAVE\_REG (0x00E0)**

Continued from the previous page...

**SPI\_SLV\_WRBUF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Wr\_BUF transfer.

0: Not use

1: Use

(R/W)

**SPI\_SLV\_LAST\_BYTE\_STRB** Represents the valid bits of the last received data byte in SPI slave full-duplex and half-duplex transfer.

(R/SS)

**SPI\_SLAVE\_MODE** Configures SPI work mode.

0: Master

1: Slave

(R/W)

**SPI\_SOFT\_RESET** Configures whether to reset the SPI clock line, CS line, and data line via software.

0: Not reset

1: Reset

(WT)

**SPI\_MST\_FD\_WAIT\_DMA\_TX\_DATA** Configures whether or not to wait DMA TX data gets ready before starting SPI transfer in master full-duplex transfer.

0: Not wait

1: Wait

(R/W)

Register 38.49. SPI\_SLAVE1\_REG (0x00E4)

|                   |    |    |    |    |   |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |       |
|-------------------|----|----|----|----|---|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|-------|
| SPI_SLV_LAST_ADDR |    |    |    |    |   |  |  |  |  | SPI_SLV_LAST_COMMAND |  |  |  |  |  |  |  |  |  | SPI_SLV_DATA_BITLEN |  |  |  |  |  |  |  |  |  |       |
| 31                | 26 | 25 | 18 | 17 | 0 |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |       |
| 0                 |    |    |    |    |   |  |  |  |  | 0                    |  |  |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  |  |  | Reset |

**SPI\_SLV\_DATA\_BITLEN** Configures the transferred data bit length in SPI slave full-/half-duplex modes.  
(R/W/SS)

**SPI\_SLV\_LAST\_COMMAND** Configures the command value in slave mode.  
(R/W/SS)

**SPI\_SLV\_LAST\_ADDR** Configures the address value in slave mode.  
(R/W/SS)

Register 38.50. SPI\_CLOCK\_REG (0x000C)

|                    |    |   |   |            |   |   |    |                |   |    |    |              |   |   |    |              |   |   |   |              |   |   |   |
|--------------------|----|---|---|------------|---|---|----|----------------|---|----|----|--------------|---|---|----|--------------|---|---|---|--------------|---|---|---|
| SPI_CLK_EQU_SYSCLK |    |   |   | (reserved) |   |   |    | SPI_CLKDIV_PRE |   |    |    | SPI_CLKCNT_N |   |   |    | SPI_CLKCNT_H |   |   |   | SPI_CLKCNT_L |   |   |   |
| 31                 | 30 |   |   |            |   |   | 22 | 21             |   | 18 | 17 |              |   |   | 12 | 11           |   |   | 6 | 5            |   |   | 0 |
| 1                  | 0  | 0 | 0 | 0          | 0 | 0 | 0  | 0              | 0 | 0  | 0  | 0            | 0 | 0 | 0  | 0            | 0 | 0 | 0 | 0            | 0 | 0 | 0 |

Reset

**SPI\_CLKCNT\_L** Configures clock duty cycles, together with SPI\_CLKCNT\_H and SPI\_CLKCNT\_N.

In master transfer, this field must be equal to SPI\_CLKCNT\_N.

In slave mode, it must be 0.

Can be configured in CONF state.

(R/W)

**SPI\_CLKCNT\_H** Configures the duty cycle of SPI\_CLK (high level) in master transfer.

It's recommended to configure this value to  $\text{floor}((\text{SPI\_CLKCNT\_N} + 1)/2 - 1)$ . floor() here is to round a number down, e.g., floor(2.2) = 2.

In slave mode, it must be 0.

(R/W)

**SPI\_CLKCNT\_N** Configures the divider of SPI\_CLK in master transfer.

SPI\_CLK frequency is  $f_{\text{clk\_spi\_mst}}/(\text{SPI\_CLKDIV\_PRE} + 1)/(\text{SPI\_CLKCNT\_N} + 1)$ .

(R/W)

**SPI\_CLKDIV\_PRE** Configures the pre-divider of SPI\_CLK in master transfer.

(R/W)

**SPI\_CLK\_EQU\_SYSCLK** Configures whether or not the SPI\_CLK is equal to clk\_spi\_mst in master transfer.

0: SPI\_CLK is divided from clk\_spi\_mst.

1: SPI\_CLK is equal to clk\_spi\_mst.

(R/W)

Register 38.51. SPI\_CLK\_GATE\_REG (0x00E8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |            |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|------------|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   | SPI_CLK_EN |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            | 3 | 2 | 1 | 0          |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0          | 0 | 0 | 0 |

Reset

**SPI\_CLK\_EN** Configures whether or not to enable clock gate.

0: Disable

1: Enable

(R/W)

### Register 38.52. SPI\_DIN\_MODE\_REG (0x0024)

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |                     |    |    |  |  |  |  |            |   |  |   |  |   |   |   |               |       |               |   |               |  |               |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|---------------------|----|----|--|--|--|--|------------|---|--|---|--|---|---|---|---------------|-------|---------------|---|---------------|--|---------------|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SPI_TIMING_HCLK_ACTIVE |                     |    |    |  |  |  |  | (reserved) |   |  |   |  |   |   |   | SPI_DIN3_MODE |       | SPI_DIN2_MODE |   | SPI_DIN1_MODE |  | SPI_DINO_MODE |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                     |                     | 16 | 15 |  |  |  |  |            |   |  | 8 |  | 7 | 6 | 5 | 4             | 3     | 2             | 1 | 0             |  |               |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                      | 0 0 0 0 0 0 0 0 0 0 |    |    |  |  |  |  |            | 0 |  | 0 |  | 0 |   | 0 |               | Reset |               |   |               |  |               |  |

**SPI\_DINO\_MODE** Configures the input mode for SPI3\_D signal.

0: Input without delay

1: Input at the (SPI\_DINO\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

**SPI\_DIN1\_MODE** Configures the input mode for SPI3\_Q signal.

0: Input without delay

1: Input at the (SPI\_DIN1\_NUM+1)th falling edge of clk\_spi\_mst.

2: Input at the (SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

**SPI\_DIN2\_MODE** Configures the input mode for SPI3\_WP signal.

0: Input without delay

1: Input at the (SPI\_DIN2\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN2\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN2\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

**SPI\_DIN3\_MODE** Configures the input mode for SPI3\_HD signal.

0: Input without delay

1: Input at the (SPI\_DIN3\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (SPI\_DIN3\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (SPI\_DIN3\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

Continued on the next page...

**Register 38.52. SPI\_DIN\_MODE\_REG (0x0024)**

Continued from the previous page...

**SPI\_TIMING\_HCLK\_ACTIVE** Configures whether or not to enable HCLK (high-frequency clock) in SPI input timing module.

0: Disable

1: Enable

(R/W)

**Register 38.53. SPI\_DIN\_NUM\_REG (0x0028)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              |   |       |   |              |  |              |  |              |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------|---|-------|---|--------------|--|--------------|--|--------------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SPI_DIN3_NUM |   |       |   | SPI_DIN2_NUM |  | SPI_DIN1_NUM |  | SPI_DINO_NUM |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8 | 7            | 6 | 5     | 4 |              |  |              |  |              |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 0 | Reset |   |              |  |              |  |              |  |

**SPI\_DINO\_NUM** Configures the delays to input signal SPI3\_D based on the setting of SPI\_DINO\_MODE.

- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)

**SPI\_DIN1\_NUM** Configures the delays to input signal SPI3\_Q based on the setting of SPI\_DIN1\_MODE.

- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)

**SPI\_DIN2\_NUM** Configures the delays to input signal SPI3\_WP based on the setting of SPI\_DIN2\_MODE.

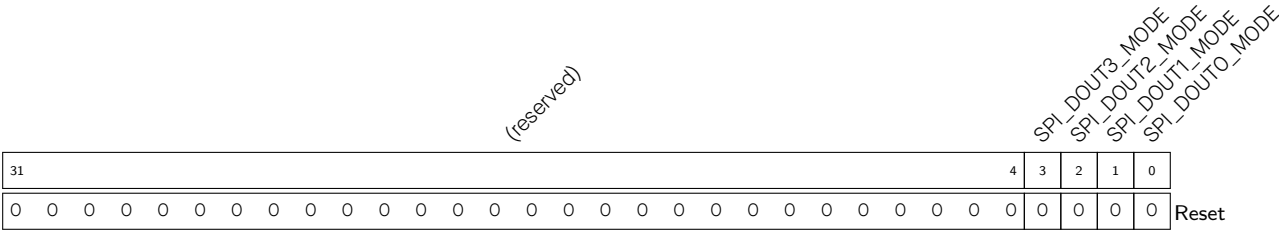
- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)

**SPI\_DIN3\_NUM** Configures the delays to input signal SPI3\_HD based on the setting of SPI\_DIN3\_MODE.

- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)



Register 38.54. SPI\_DOUT\_MODE\_REG (0x002C)



- SPI\_DOUT0\_MODE** Configures the output mode for SPI3\_D signal.  
0: Output without delay  
1: Output with a delay of a SPI module clock cycle at its falling edge  
(R/W)
- SPI\_DOUT1\_MODE** Configures the output mode for SPI3\_Q signal.  
0: Output without delay  
1: Output with a delay of a SPI module clock cycle at its falling edge  
(R/W)
- SPI\_DOUT2\_MODE** Configures the output mode for SPI3\_WP signal.  
0: Output without delay  
1: Output with a delay of a SPI module clock cycle at its falling edge  
(R/W)
- SPI\_DOUT3\_MODE** Configures the output mode for SPI3\_HD signal.  
0: Output without delay  
1: Output with a delay of a SPI module clock cycle at its falling edge  
(R/W)

**Register 38.55. SPI\_DMA\_INT\_ENA\_REG (0x0034)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|-------|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | SPI_APP1_INT_ENA<br>SPI_APP2_INT_ENA<br>SPI_MST_TX_AFIFO_EMPTY_ERR_INT_ENA<br>SPI_MST_RX_AFIFO_WFULL_ERR_INT_ENA<br>SPI_SLV_CMD_ERR_INT_ENA<br>(reserved)<br>SPI_DMA_SEG_TRANS_DONE_INT_ENA<br>SPI_TRANS_DONE_INT_ENA<br>SPI_SLV_WR_BUF_DONE_INT_ENA<br>SPI_SLV_RD_BUF_DONE_INT_ENA<br>SPI_SLV_RD_DMA_DONE_INT_ENA<br>SPI_SLV_WR_DMA_DONE_INT_ENA<br>SPI_SLV_CMD9_INT_ENA<br>SPI_SLV_CMD8_INT_ENA<br>SPI_SLV_CMD7_INT_ENA<br>SPI_SLV_EN_QPI_INT_ENA<br>SPI_SLV_EX_QPI_INT_ENA<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_ENA<br>SPI_DMA_INFIFO_FULL_ERR_INT_ENA |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 21  | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_ENA** Write 1 to enable SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(R/W)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_ENA** Write 1 to enable SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/W)

**SPI\_SLV\_EX\_QPI\_INT\_ENA** Write 1 to enable SPI\_SLV\_EX\_QPI\_INT interrupt.  
(R/W)

**SPI\_SLV\_EN\_QPI\_INT\_ENA** Write 1 to enable SPI\_SLV\_EN\_QPI\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD7\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD7\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD8\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD8\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD9\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD9\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMDA\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMDA\_INT interrupt.  
(R/W)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(R/W)

Continued on the next page...

**Register 38.55. SPI\_DMA\_INT\_ENA\_REG (0x0034)**

Continued from the previous page...

**SPI\_TRANS\_DONE\_INT\_ENA** Write 1 to enable SPI\_TRANS\_DONE\_INT interrupt.  
(R/W)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_ENA** Write 1 to enable SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(R/W)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(R/W)

**SPI\_SLV\_CMD\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(R/W)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(R/W)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/W)

**SPI\_APP2\_INT\_ENA** Write 1 to enable SPI\_APP2\_INT interrupt.  
(R/W)

**SPI\_APP1\_INT\_ENA** Write 1 to enable SPI\_APP1\_INT interrupt.  
(R/W)

## Register 38.56. SPI\_DMA\_INT\_CLR\_REG (0x0038)

|            |   |   |   |   |   |   |   |   |   |   |    |   |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|----|---|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |    | SPI_APP1_INT_CLR<br>SPI_APP2_INT_CLR<br>SPI_MST_TX_INT_CLR<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_CLR<br>SPI_SLV_CMD_ERR_INT_CLR<br>SPI_SLV_BUF_ADDR_ERR_INT_CLR<br>(reserved)<br>SPI_DMA_SEG_TRANS_DONE_INT_CLR<br>SPI_TRANS_DONE_INT_CLR<br>SPI_SLV_WR_BUF_DONE_INT_CLR<br>SPI_SLV_RD_BUF_DONE_INT_CLR<br>SPI_SLV_WR_DMA_DONE_INT_CLR<br>SPI_SLV_RD_DMA_DONE_INT_CLR<br>SPI_SLV_CMD7_INT_CLR<br>SPI_SLV_CMD8_INT_CLR<br>SPI_SLV_CMD9_INT_CLR<br>SPI_SLV_CMDA_INT_CLR<br>SPI_SLV_EN_QPI_INT_CLR<br>SPI_SLV_EX_QPI_INT_CLR<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_CLR<br>SPI_DMA_INFIFO_FULL_ERR_INT_CLR |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   | 21 | 20  | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_CLR** Write 1 to clear SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(WT)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_CLR** Write 1 to clear SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_EX\_QPI\_INT\_CLR** Write 1 to clear SPI\_SLV\_EX\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_EN\_QPI\_INT\_CLR** Write 1 to clear SPI\_SLV\_EN\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD7\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD7\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD8\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD8\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD9\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD9\_INT interrupt.  
(WT)

**SPI\_SLV\_CMDA\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMDA\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(WT)

Continued on the next page...

**Register 38.56. SPI\_DMA\_INT\_CLR\_REG (0x0038)**

Continued from the previous page...

**SPI\_TRANS\_DONE\_INT\_CLR** Write 1 to clear SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_CLR** Write 1 to clear SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_APP2\_INT\_CLR** Write 1 to clear SPI\_APP2\_INT interrupt.  
(WT)

**SPI\_APP1\_INT\_CLR** Write 1 to clear SPI\_APP1\_INT interrupt.  
(WT)

**Register 38.57. SPI\_DMA\_INT\_RAW\_REG (0x003C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|-------|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | SPI_APP1_INT_RAW<br>SPI_APP2_INT_RAW<br>SPI_MST_TX_AFIFO_EMPTY_ERR_INT_RAW<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_RAW<br>SPI_SLV_CMD_ERR_INT_RAW<br>SPI_SLV_BUF_ADDR_ERR_INT_RAW<br>(reserved)<br>SPI_DMA_SEG_TRANS_DONE_INT_RAW<br>SPI_TRANS_DONE_INT_RAW<br>SPI_SLV_WR_BUF_DONE_INT_RAW<br>SPI_SLV_RD_BUF_DONE_INT_RAW<br>SPI_SLV_WR_DMA_DONE_INT_RAW<br>SPI_SLV_RD_DMA_DONE_INT_RAW<br>SPI_SLV_CMD9_INT_RAW<br>SPI_SLV_CMD8_INT_RAW<br>SPI_SLV_CMD7_INT_RAW<br>SPI_SLV_EN_QPI_INT_RAW<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_RAW<br>SPI_DMA_INFIFO_FULL_ERR_INT_RAW |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 21  | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_RAW** The raw interrupt status of SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(R/WTC/SS)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_RAW** The raw interrupt status of SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_EX\_QPI\_INT\_RAW** The raw interrupt status of SPI\_SLV\_EX\_QPI\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_EN\_QPI\_INT\_RAW** The raw interrupt status of SPI\_SLV\_EN\_QPI\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD7\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD7\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD8\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD8\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMD9\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD9\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_CMDA\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMDA\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(R/WTC/SS)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/WTC/SS)

Continued on the next page...

**Register 38.57. SPI\_DMA\_INT\_RAW\_REG (0x003C)**

Continued from the previous page...

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of SPI\_TRANS\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.

(R/WTC/SS)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_SLV\_CMD\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.

(R/WTC/SS)

**SPI\_APP2\_INT\_RAW** The raw interrupt status of SPI\_APP2\_INT interrupt. The value is only controlled by the application.

(R/WTC/SS)

**SPI\_APP1\_INT\_RAW** The raw interrupt status of SPI\_APP1\_INT interrupt. The value is only controlled by the application.

(R/WTC/SS)

Register 38.58. SPI\_DMA\_INT\_ST\_REG (0x0040)

|            |    |    |    |    |    |    |    |    |    |    |    |  |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|----|----|----|----|----|----|----|----|----|----|--|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |    |    |    |    |    |    |    |    |    |    | SPI_APP1_INT_ST<br>SPI_APP2_INT_ST<br>SPI_MST_TX_AFIFO_EMPTY_ERR_INT_ST<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_ST<br>SPI_SLV_CMD_ERR_INT_ST<br>(reserved)<br>SPI_DMA_SEG_TRANS_DONE_INT_ST<br>SPI_SLV_WR_BUF_DONE_INT_ST<br>SPI_SLV_RD_BUF_DONE_INT_ST<br>SPI_SLV_RD_DMA_DONE_INT_ST<br>SPI_SLV_WR_DMA_DONE_INT_ST<br>SPI_SLV_CMDA_INT_ST<br>SPI_SLV_CMD9_INT_ST<br>SPI_SLV_CMD8_INT_ST<br>SPI_SLV_EN_QPI_INT_ST<br>SPI_SLV_EX_QPI_INT_ST<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_ST<br>SPI_DMA_INFIFO_FULL_ERR_INT_ST |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10   | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_ST** The interrupt status of SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(RO)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_ST** The interrupt status of SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(RO)

**SPI\_SLV\_EX\_QPI\_INT\_ST** The interrupt status of SPI\_SLV\_EX\_QPI\_INT interrupt.  
(RO)

**SPI\_SLV\_EN\_QPI\_INT\_ST** The interrupt status of SPI\_SLV\_EN\_QPI\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD7\_INT\_ST** The interrupt status of SPI\_SLV\_CMD7\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD8\_INT\_ST** The interrupt status of SPI\_SLV\_CMD8\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD9\_INT\_ST** The interrupt status of SPI\_SLV\_CMD9\_INT interrupt.  
(RO)

**SPI\_SLV\_CMDA\_INT\_ST** The interrupt status of SPI\_SLV\_CMDA\_INT interrupt.  
(RO)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(RO)

Continued on the next page...



**Register 38.58. SPI\_DMA\_INT\_ST\_REG (0x0040)**

Continued from the previous page...

**SPI\_TRANS\_DONE\_INT\_ST** The interrupt status of SPI\_TRANS\_DONE\_INT interrupt.  
(RO)

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_ST** The interrupt status of SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(RO)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ST** The interrupt status of SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(RO)

**SPI\_SLV\_CMD\_ERR\_INT\_ST** The interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(RO)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(RO)

**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(RO)

**SPI\_APP2\_INT\_ST** The interrupt status of SPI\_APP2\_INT interrupt.  
(RO)

**SPI\_APP1\_INT\_ST** The interrupt status of SPI\_APP1\_INT interrupt.  
(RO)

**Register 38.59. SPI\_DMA\_INT\_SET\_REG (0x0044)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|-------|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | SPI_APP1_INT_SET<br>SPI_APP2_INT_SET<br>SPI_MST_TX_INT_SET<br>SPI_MST_RX_AFIFO_EMPTY_ERR_INT_SET<br>SPI_SLV_CMD_ERR_INT_SET<br>SPI_SLV_BUF_ADDR_ERR_INT_SET<br>(reserved)<br>SPI_DMA_SEG_TRANS_DONE_INT_SET<br>SPI_TRANS_DONE_INT_SET<br>SPI_SLV_WR_BUF_DONE_INT_SET<br>SPI_SLV_RD_BUF_DONE_INT_SET<br>SPI_SLV_WR_DMA_DONE_INT_SET<br>SPI_SLV_RD_DMA_DONE_INT_SET<br>SPI_SLV_CMD8_INT_SET<br>SPI_SLV_CMD9_INT_SET<br>SPI_SLV_CMD7_INT_SET<br>SPI_SLV_EN_QPI_INT_SET<br>SPI_SLV_EX_QPI_INT_SET<br>SPI_DMA_OUTFIFO_EMPTY_ERR_INT_SET<br>SPI_DMA_INFIFO_FULL_ERR_INT_SET |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |       |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 21  | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2     | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |

**SPI\_DMA\_INFIFO\_FULL\_ERR\_INT\_SET** Write 1 to set SPI\_DMA\_INFIFO\_FULL\_ERR\_INT interrupt.  
(WT)

**SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT\_SET** Write 1 to set SPI\_DMA\_OUTFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_SLV\_EX\_QPI\_INT\_SET** Write 1 to set SPI\_SLV\_EX\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_EN\_QPI\_INT\_SET** Write 1 to set SPI\_SLV\_EN\_QPI\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD7\_INT\_SET** Write 1 to set SPI\_SLV\_CMD7\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD8\_INT\_SET** Write 1 to set SPI\_SLV\_CMD8\_INT interrupt.  
(WT)

**SPI\_SLV\_CMD9\_INT\_SET** Write 1 to set SPI\_SLV\_CMD9\_INT interrupt.  
(WT)

**SPI\_SLV\_CMDA\_INT\_SET** Write 1 to set SPI\_SLV\_CMDA\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_DMA\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_RD\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_DMA\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_WR\_DMA\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_RD\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_WR\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(WT)

**SPI\_TRANS\_DONE\_INT\_SET** Write 1 to set SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

Continued on the next page...

**Register 38.59. SPI\_DMA\_INT\_SET\_REG (0x0044)**

Continued from the previous page...

**SPI\_DMA\_SEG\_TRANS\_DONE\_INT\_SET** Write 1 to set SPI\_DMA\_SEG\_TRANS\_DONE\_INT interrupt.  
(WT)

**SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

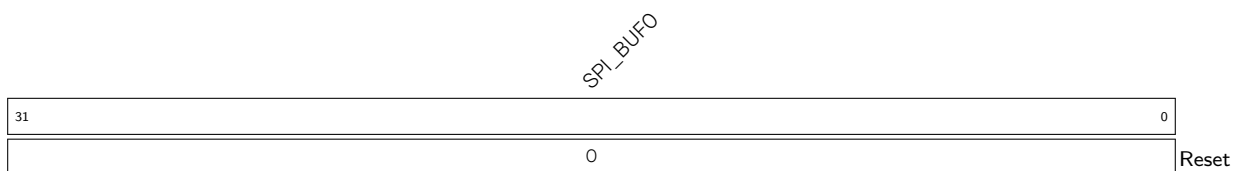
**SPI\_SLV\_CMD\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

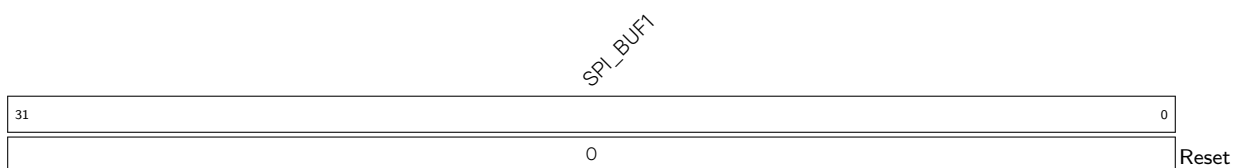
**SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**SPI\_APP2\_INT\_SET** Write 1 to set SPI\_APP2\_INT interrupt.  
(WT)

**SPI\_APP1\_INT\_SET** Write 1 to set SPI\_APP1\_INT interrupt.  
(WT)

**Register 38.60. SPI\_W0\_REG (0x0098)**

**SPI\_BUFO** 32-bit data buffer 0.  
(R/W/SS)

**Register 38.61. SPI\_W1\_REG (0x009C)**

**SPI\_BUF1** 32-bit data buffer 1.  
(R/W/SS)

## Register 38.62. SPI\_W2\_REG (0x00A0)

|          |   |
|----------|---|
| SPI_BUF2 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF2** 32-bit data buffer 2.  
(R/W/SS)

## Register 38.63. SPI\_W3\_REG (0x00A4)

|          |   |
|----------|---|
| SPI_BUF3 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF3** 32-bit data buffer 3.  
(R/W/SS)

## Register 38.64. SPI\_W4\_REG (0x00A8)

|          |   |
|----------|---|
| SPI_BUF4 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF4** 32-bit data buffer 4.  
(R/W/SS)

## Register 38.65. SPI\_W5\_REG (0x00AC)

|          |   |
|----------|---|
| SPI_BUF5 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF5** 32-bit data buffer 5.  
(R/W/SS)

## Register 38.66. SPI\_W6\_REG (0x00B0)

|          |   |
|----------|---|
| SPI_BUF6 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF6** 32-bit data buffer 6.  
(R/W/SS)

## Register 38.67. SPI\_W7\_REG (0x00B4)

|          |   |
|----------|---|
| SPI_BUF7 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF7** 32-bit data buffer 7.  
(R/W/SS)

## Register 38.68. SPI\_W8\_REG (0x00B8)

|          |   |
|----------|---|
| SPI_BUF8 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF8** 32-bit data buffer 8.  
(R/W/SS)

## Register 38.69. SPI\_W9\_REG (0x00BC)

|          |   |
|----------|---|
| SPI_BUF9 |   |
| 31       | 0 |
| 0        |   |
| Reset    |   |

**SPI\_BUF9** 32-bit data buffer 9.  
(R/W/SS)

**Register 38.70. SPI\_W10\_REG (0x00C0)**

|                  |       |
|------------------|-------|
| <i>SPI_BUF10</i> |       |
| 31               | 0     |
| 0                |       |
|                  | Reset |

**SPI\_BUF10** 32-bit data buffer 10.  
(R/W/SS)

**Register 38.71. SPI\_W11\_REG (0x00C4)**

|                  |       |
|------------------|-------|
| <i>SPI_BUF11</i> |       |
| 31               | 0     |
| 0                |       |
|                  | Reset |

**SPI\_BUF11** 32-bit data buffer 11.  
(R/W/SS)

**Register 38.72. SPI\_W12\_REG (0x00C8)**

|                  |       |
|------------------|-------|
| <i>SPI_BUF12</i> |       |
| 31               | 0     |
| 0                |       |
|                  | Reset |

**SPI\_BUF12** 32-bit data buffer 12.  
(R/W/SS)

**Register 38.73. SPI\_W13\_REG (0x00CC)**

|                  |       |
|------------------|-------|
| <i>SPI_BUF13</i> |       |
| 31               | 0     |
| 0                |       |
|                  | Reset |

**SPI\_BUF13** 32-bit data buffer 13.  
(R/W/SS)

## SPI\_BUF14

**SPI\_BUF14** 32-bit data buffer 14.  
(R/W/SS)

## SPI\_BUF15

**SPI\_BUF15** 32-bit data buffer 15.  
(R/W/SS)

(reserved)

**SPI\_DATE** Version control register.  
(R/W)

The addresses in this section are relative to LP-SPI base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

Espressif Systems

**Register 38.77. LP\_SPI\_CMD\_REG (0x0000)**

|            |   |   |   |   |   |   |                             |    |            |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|-----------------------------|----|------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   | LP_SPI_USR<br>LP_SPI_UPDATE |    | (reserved) |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   | 25                          | 24 | 23         | 22 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0  | 0          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

**LP\_SPI\_UPDATE** Configures whether or not to synchronize SPI registers from APB clock domain into SPI module clock domain.

0: Not synchronize

1: Synchronize

This bit is only used in SPI master transfer.

(WT)

**LP\_SPI\_USR** Configures whether or not to enable user-defined command.

0: Not enable

1: Enable

An SPI operation will be triggered when the bit is set. This bit will be cleared once the operation is done.

(R/W/SC)

**Register 38.78. LP\_SPI\_ADDR\_REG (0x0004)**

|                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| LP_SPI_USR_ADDR_VALUE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**LP\_SPI\_USR\_ADDR\_VALUE** Configures the address to slave.

(R/W)



**Register 38.79. LP\_SPI\_USER\_REG (0x0010)**

|                    |    |                 |    |                  |    |                 |    |                 |    |                       |   |                          |   |                          |   |            |    |            |    |            |   |                    |   |                    |   |                 |   |                |   |                    |   |            |   |                |       |  |  |  |  |  |   |
|--------------------|----|-----------------|----|------------------|----|-----------------|----|-----------------|----|-----------------------|---|--------------------------|---|--------------------------|---|------------|----|------------|----|------------|---|--------------------|---|--------------------|---|-----------------|---|----------------|---|--------------------|---|------------|---|----------------|-------|--|--|--|--|--|---|
| LP_SPI_USR_COMMAND |    | LP_SPI_USR_ADDR |    | LP_SPI_USR_DUMMY |    | LP_SPI_USR_MISO |    | LP_SPI_USR_MOSI |    | LP_SPI_USR_DUMMY_IDLE |   | LP_SPI_USR_MOSI_HIGHPART |   | LP_SPI_USR_MISO_HIGHPART |   | (reserved) |    | LP_SPI_SIO |    | (reserved) |   | LP_SPI_CK_OUT_EDGE |   | LP_SPI_RSCK_I_EDGE |   | LP_SPI_CS_SETUP |   | LP_SPI_CS_HOLD |   | LP_SPI_TSCK_I_EDGE |   | (reserved) |   | LP_SPI_DOUTDIN |       |  |  |  |  |  |   |
| 31                 | 30 | 29              | 28 | 27               | 26 | 25              | 24 | 23              | 18 |                       |   |                          |   |                          |   |            | 17 | 16         | 10 |            |   |                    |   |                    |   |                 | 9 | 8              | 7 | 6                  | 5 | 4          | 1 |                |       |  |  |  |  |  | 0 |
| 1                  | 0  | 0               | 0  | 0                | 0  | 0               | 0  | 0               | 0  | 0                     | 0 | 0                        | 0 | 0                        | 0 | 0          | 0  | 0          | 0  | 0          | 0 | 0                  | 0 | 0                  | 1 | 1               | 0 | 0              | 0 | 0                  | 0 | 0          | 0 | 0              | Reset |  |  |  |  |  |   |

**LP\_SPI\_DOUTDIN** Configures whether or not to enable full-duplex communication.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_TSCK\_I\_EDGE** Configures whether or not to change the polarity of TSCK in slave transfer.

0: TSCK = SPI\_CK\_I

1: TSCK = !SPI\_CK\_I

(R/W)

**LP\_SPI\_CS\_HOLD** Configures whether or not to keep SPI CS low when SPI is in DONE state.

0: Not keep low

1: Keep low

(R/W)

**LP\_SPI\_CS\_SETUP** Configures whether or not to enable SPI CS when SPI is in prepare (PREP) state.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_RSCK\_I\_EDGE** Configures whether or not to change the polarity of RSCK in slave transfer.

0: RSCK = !SPI\_CK\_I

1: RSCK = SPI\_CK\_I

(R/W)

**LP\_SPI\_CK\_OUT\_EDGE** Configures SPI clock mode together with LP\_SPI\_CK\_IDLE\_EDGE.

For more information, see Section [38.7.3](#). (R/W)

**LP\_SPI\_SIO** Configures whether or not to enable 3-line half-duplex communication, where MOSI and MISO signals share the same pin.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 38.79. LP\_SPI\_USER\_REG (0x0010)**

Continued from the previous page...

**LP\_SPI\_USR\_MISO\_HIGHPART** Configures whether or not to enable High-Part mode in read-data phase, i.e., only access to high-part of the buffers: LP\_SPI\_W8\_REG ~ LP\_SPI\_W15\_REG.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_MOSI\_HIGHPART** Configures whether or not to enable High-Part mode in write-data phase, i.e., only access to high-part of the buffers: LP\_SPI\_W8\_REG ~ LP\_SPI\_W15\_REG.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_DUMMY\_IDLE** Configures whether or not to disable SPI clock in DUMMY state.

0: Not disable

1: Disable

(R/W)

**LP\_SPI\_USR\_MOSI** Configures whether or not to enable the write-data (DOUT) state of an operation.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_MISO** Configures whether or not to enable the read-data (DIN) state of an operation.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_DUMMY** Configures whether or not to enable the DUMMY state of an operation.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_ADDR** Configures whether or not to enable the address (ADDR) state of an operation.

0: Disable

1: Enable

(R/W)

**LP\_SPI\_USR\_COMMAND** Configures whether or not to enable the command (CMD) state of an operation.

0: Disable

1: Enable

(R/W)

### Register 38.80. LP\_SPI\_USER1\_REG (0x0014)

|                        |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |
|------------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|-----------------------------|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|
| LP_SPI_USR_ADDR_BITLEN |  |  |  |  |  |  |  | LP_SPI_CS_HOLD_TIME |  |  |  |  |  |  |  | LP_SPI_CS_SETUP_TIME |  |  |  |  |  |  |  | LP_SPI_MST_WFULL_ERR_END_EN |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  | LP_SPI_USR_DUMMY_CYCLELEN |  |  |  |  |  |  |  |
| 3127262221171615870    |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |                             |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |
| 23                     |  |  |  |  |  |  |  | 0x1                 |  |  |  |  |  |  |  | 0                    |  |  |  |  |  |  |  | 10000000000000              |  |  |  |  |  |  |  | 7          |  |  |  |  |  |  |  | Reset                     |  |  |  |  |  |  |  |

**LP\_SPI\_USR\_DUMMY\_CYCLELEN** Configures the length of DUMMY state.

Measurement unit: SPI\_CLK clock cycles.

This value is (the expected cycle number - 1). (R/W)

**LP\_SPI\_MST\_WFULL\_ERR\_END\_EN** Configures whether or not to end the LP-SPI transfer when SPI RX AFIFO wfull error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)

**LP\_SPI\_CS\_SETUP\_TIME** Configures the length of prepare (PREP) state.

Measurement unit: SPI\_CLK clock cycles.

This value is equal to the expected cycles - 1. This field is used together with LP\_SPI\_CS\_SETUP.  
(R/W)

**LP\_SPI\_CS\_HOLD\_TIME** Configures the delay cycles of CS pin.

Measurement unit: SPI\_CLK clock cycles.

This field is used together with LP\_SPI\_CS\_HOLD. (R/W)

**LP\_SPI\_USR\_ADDR\_BITLEN** Configures the bit length in address state.

This value is (expected bit number - 1). (R/W)

Register 38.81. LP\_SPI\_USER2\_REG (0x0018)



- LP\_SPI\_USR\_COMMAND\_VALUE

Configures the command value. (R/W)
- LP\_SPI\_MST\_EMPTY\_ERR\_END\_EN

Configures whether or not to end the LP-SPI transfer when SPI TX AFIFO read empty error occurs in master full-/half-duplex transfers.

0: Not end

1: End

(R/W)
- LP\_SPI\_USR\_COMMAND\_BITLEN

Configures the bit length of command state.

This value is (expected bit number - 1).

(R/W)

Register 38.82. LP\_SPI\_CTRL\_REG (0x0008)

|            |    |    |    |    |  |    |    |    |   |            |   |   |   |   |                              |   |   |   |   |            |   |   |   |   |                                |   |   |   |   |       |
|------------|----|----|----|----|--|----|----|----|---|------------|---|---|---|---|------------------------------|---|---|---|---|------------|---|---|---|---|--------------------------------|---|---|---|---|-------|
| (reserved) |    |    |    |    | LP_SPI_WR_BIT_ORDER<br>LP_SPI_RD_BIT_ORDER |    |    |    |   | (reserved) |   |   |   |   | LP_SPI_D_POL<br>LP_SPI_Q_POL |   |   |   |   | (reserved) |   |   |   |   | LP_SPI_DUMMY_OUT<br>(reserved) |   |   |   |   |       |
| 31         | 27 | 26 | 25 | 24 | 20   | 19 | 18 | 17 |   |            |   |   |   | 4 | 3                            | 2 | 0 |   |   |            |   |   |   |   |                                |   |   |   |   |       |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 1          | 1 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | Reset |

**LP\_SPI\_DUMMY\_OUT** Configures whether or not to output the LP\_SPI bus signals in DUMMY state.

0: Not output

1: Output

(R/W)

**LP\_SPI\_Q\_POL** Configures MISO line polarity.

0: Low

1: High

(R/W)

**LP\_SPI\_D\_POL** Configures MOSI line polarity.

0: Low

1: High

(R/W)

**LP\_SPI\_RD\_BIT\_ORDER** Configures the bit order in read-data (MISO) state.

0: MSB first

1: LSB first

(R/W)

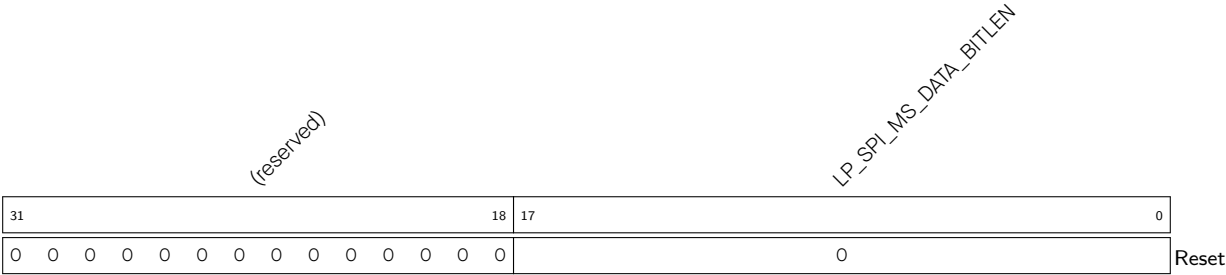
**LP\_SPI\_WR\_BIT\_ORDER** Configures the bit order in command (CMD), address (ADDR), and write-data (MOSI) states.

0: MSB first

1: LSB first

(R/W)

Register 38.83. LP\_SPI\_MS\_DLEN\_REG (0x001C)



**LP\_SPI\_MS\_DATA\_BITLEN** Configures the data bit length of SPI transfer in CPU-controlled master transfer.  
This value shall be (expected bit\_num - 1).  
(R/W)

Register 38.84. LP\_SPI\_MISC\_REG (0x0020)

|            |    |    |    |                       |   |   |   |                     |    |    |   |            |   |   |   |                     |   |   |   |            |   |   |   |                      |   |   |   |               |   |   |   |            |  |  |  |                |  |  |  |
|------------|----|----|----|-----------------------|---|---|---|---------------------|----|----|---|------------|---|---|---|---------------------|---|---|---|------------|---|---|---|----------------------|---|---|---|---------------|---|---|---|------------|--|--|--|----------------|--|--|--|
| (reserved) |    |    |    | LP_SPI_CS_KEEP_ACTIVE |   |   |   | LP_SPI_CK_IDLE_EDGE |    |    |   | (reserved) |   |   |   | LP_SPI_SLAVE_CS_POL |   |   |   | (reserved) |   |   |   | LP_SPI_MASTER_CS_POL |   |   |   | LP_SPI_CK_DIS |   |   |   | (reserved) |  |  |  | LP_SPI_CS0_DIS |  |  |  |
| 31         | 30 | 29 | 28 | 24                    |   |   |   | 23                  | 22 | 10 |   |            |   |   |   |                     |   |   |   | 9          | 7 | 6 | 5 | 1                    |   |   |   | 0             |   |   |   |            |  |  |  |                |  |  |  |
| 0          | 0  | 0  | 0  | 0                     | 0 | 0 | 0 | 0                   | 0  | 0  | 0 | 0          | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0             | 0 | 0 | 0 | Reset      |  |  |  |                |  |  |  |

**LP\_SPI\_CS0\_DIS** Configures whether or not to disable SPI\_CS0 pin.

0: SPI\_CS0 signal is from/to SPI\_CS0 pin.

1: Disable SPI\_CS0 pin.

(R/W)

**LP\_SPI\_CLK\_DIS** Configures whether or not to disable SPI\_CLK output.

0: Enable

1: Disable

(R/W)

**LP\_SPI\_MASTER\_CS\_POL** Configures the polarity of SPI\_CS0 line in master transfer.

0: SPI\_CS0 is low active.

1: SPI\_CS0 is high active.

(R/W)

**LP\_SPI\_SLAVE\_CS\_POL** Configures whether or not invert SPI slave input CS polarity.

0: Not change

1: Invert

(R/W)

**LP\_SPI\_CLK\_IDLE\_EDGE** Configures the level of SPI\_CLK line when LP-SPI is in idle.

0: Low

1: High

(R/W)

**LP\_SPI\_CS\_KEEP\_ACTIVE** Configures whether or not to keep the SPI\_CS line low.

0: Not keep low

1: Keep low

(R/W)

(reserved)  
LP\_SPI\_BUF\_AFIFO\_RST  
LP\_SPI\_RX\_AFIFO\_RST

(reserved)

(WT)

(WT)



### Register 38.86. LP\_SPI\_SLEEP\_CONFO\_REG (0x0044)

Register map for LP\_SPI\_SIV\_WK\_CHAR0:

- Bit 31: (reserved)
- Bits 15-11: LP\_SPI\_SLEEP\_DIS\_RXFIFO\_WR\_EN
- Bits 14-10: LP\_SPI\_SLEEP\_EN
- Bits 9-7: LP\_SPI\_SIV\_WK\_MODE\_SEL
- Bits 6-4: LP\_SPI\_SIV\_WK\_CHAR\_MASK
- Bits 3-1: LP\_SPI\_SIV\_WK\_CHAR\_NUM
- Bit 0: LP\_SPI\_SIV\_WK\_CHAR0

Reset state values: 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0, 0x0, 0x0, 0xa

LP\_SPI\_SLV\_WK\_CHAR0 Configures wake-up character 0.  
(R/W)

**LP\_SPI\_SLV\_WK\_CHAR\_NUM** Configures the amount of the enabled wake-up characters.  
(R/W)

**LP\_SPI\_SLV\_WK\_CHAR\_MASK** Configures the bit map for the characters to be masked.  
 Bit 0 ~ bit 4 correspond to wake-up character 0 ~ character 4, respectively.  
 If the bit value is:

- 0: The corresponding wake-up character is not masked.
- 1: The corresponding wake-up character is masked.

(R/W)

**LP\_SPI\_SLV\_WK\_MODE\_SEL** Configures the wake-up mode.

- 0: Wakes up the chip once the LP-SPI slave detects a start bit.
- 1: Wakes up the chip once the LP-SPI slave detects a specific sequence of characters.

(R/W)

**LP\_SPI\_SLEEP\_EN** Configures whether or not to enable sleep mode.  
0: Not enable  
1: Enable  
(R/W)

**LP\_SPI\_SLEEP\_DIS\_RXFIFO\_WR\_EN** Configures whether or not to store the data before wake-up.

- 0: Store the data
- 1: Not store the data

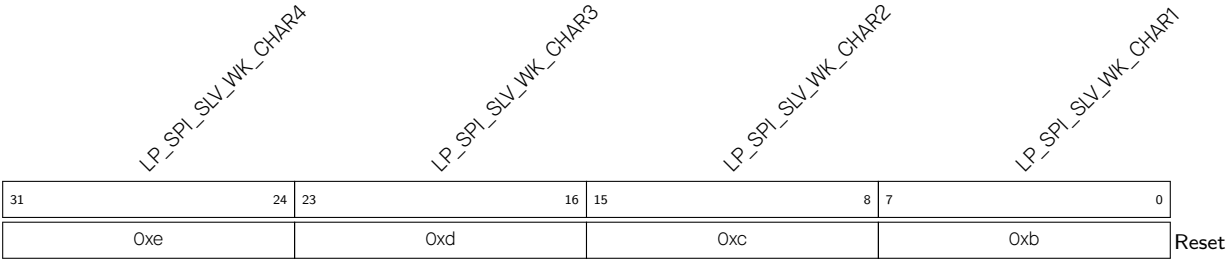
(R/W)

**LP\_SPI\_SLEEP\_WK\_DATA\_SEL** Configures in which states to detect the wake-up characters.

- 0: Only detect wake-up characters from RX data in DATA state.
- 1: Detect wake-up characters from RX data in all states.

(R/W)

Register 38.87. LP\_SPI\_SLEEP\_CONF1\_REG (0x0048)



**LP\_SPI\_SLV\_WK\_CHAR1**   Configures wake-up character 1.  
(R/W)

**LP\_SPI\_SLV\_WK\_CHAR2**   Configures wake-up character 2.  
(R/W)

**LP\_SPI\_SLV\_WK\_CHAR3**   Configures wake-up character 3.  
(R/W)

**LP\_SPI\_SLV\_WK\_CHAR4**   Configures wake-up character 4.  
(R/W)

**Register 38.88. LP\_SPI\_SLAVE\_REG (0x00E0)**

|            |    |    |    |  |   |   |   |   |   |   |   |            |    |    |   |  |   |   |   |            |   |   |       |   |  |  |  |
|------------|----|----|----|--|---|---|---|---|---|---|---|------------|----|----|---|--|---|---|---|------------|---|---|-------|---|--|--|--|
| (reserved) |    |    |    | LP_SPI_SOFT_RESET<br>LP_SPI_SLAVE_MODE |   |   |   |   |   |   |   | (reserved) |    |    |   | LP_SPI_SLV_WRBUF_BITLEN_EN<br>LP_SPI_SLV_RDBUF_BITLEN_EN |   |   |   | (reserved) |   |   |       | LP_SPI_RSCK_DATA_OUT<br>LP_SPI_CLK_MODE_13<br>LP_SPI_CLK_MODE |  |  |  |
| 31         | 28 | 27 | 26 | 25                                     |   |   |   |   |   |   |   | 12         | 11 | 10 | 9 |  | 4 | 3 | 2 | 1          | 0 |   |       |   |  |  |  |
| 0          | 0  | 0  | 0  | 0                                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0  | 0  | 0 | 0  | 0 | 0 | 0 | 0          | 0 | 0 | Reset |   |  |  |  |

**LP\_SPI\_CLK\_MODE** Configures LP-SPI clock mode.

- 0: LP-SPI clock is off when CS becomes inactive.
- 1: LP-SPI clock is delayed one cycle after CS becomes inactive.
- 2: LP-SPI clock is delayed two cycles after CS becomes inactive.
- 3: LP-SPI clock is always on.

(R/W)

**LP\_SPI\_CLK\_MODE\_13** Configures clock mode.

- 0: SPI clock mode 1 and mode 3. See Table [38.7-2](#).
- 1: SPI clock mode 0 and mode 2. See Table [38.7-2](#).

(R/W)

**LP\_SPI\_RSCK\_DATA\_OUT** Configures the edge of output data.

- 0: Output data at TSCK rising edge.
- 1: Output data at RSCK rising edge.

(R/W)

**LP\_SPI\_SLV\_RDBUFF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Rd\_BUF transfer.

- 0: Not use
- 1: Use

(R/W)

**LP\_SPI\_SLV\_WRBUFF\_BITLEN\_EN** Configures whether or not to use SPI\_SLV\_DATA\_BITLEN to store the data bit length of Wr\_BUF transfer.

- 0: Not use
- 1: Use

(R/W)

**LP\_SPI\_SLAVE\_MODE** Configures SPI work mode.

- 0: Master
- 1: Slave

(R/W)

**LP\_SPI\_SOFT\_RESET** Configures whether to reset the SPI clock line, CS line, and data line via software.

- 0: Not reset
- 1: Reset

(WT)

Register 38.89. LP\_SPI\_SLAVE1\_REG (0x00E4)

|                         |    |    |    |    |   |  |  |  |  |
|-------------------------|----|----|----|----|---|--|--|--|--|
| LP_SPI_SLV_LAST_ADDR    |    |    |    |    |   |  |  |  |  |
| LP_SPI_SLV_LAST_COMMAND |    |    |    |    |   |  |  |  |  |
| LP_SPI_SLV_DATA_BITLEN  |    |    |    |    |   |  |  |  |  |
| 31                      | 26 | 25 | 18 | 17 | 0 |  |  |  |  |
| 0                       |    | 0  |    | 0  |   |  |  |  |  |
| Reset                   |    |    |    |    |   |  |  |  |  |

**LP\_SPI\_SLV\_DATA\_BITLEN** Configures the transferred data bit length in SPI slave full-/half-duplex modes.  
(R/W/SS)

**LP\_SPI\_SLV\_LAST\_COMMAND** Configures the command value in slave mode.  
(R/W/SS)

**LP\_SPI\_SLV\_LAST\_ADDR** Configures the address value in slave mode.  
(R/W/SS)

### Register 38.90. LP\_SPI\_CLOCK\_REG (0x000C)

LP\_SPI\_CLK\_CNTL

LP\_SPI\_CLK\_CNTL[31:30]

LP\_SPI\_CLK\_CNTL[21:17]

LP\_SPI\_CLK\_CNTL[12:11]

LP\_SPI\_CLK\_CNTL[6:5]

LP\_SPI\_CLK\_CNTL[0]

(reserved)

|    |    |    |    |    |    |     |    |     |   |     |  |
|----|----|----|----|----|----|-----|----|-----|---|-----|--|
| 31 | 30 | 22 | 21 | 18 | 17 | 12  | 11 | 6   | 5 | 0   |  |
| 1  | 0  | 0  | 0  | 0  | 0  | 0   | 0  | 0   | 0 | 0   |  |
|    |    |    |    | 0  |    | 0x3 |    | 0x1 |   | 0x3 |  |

Reset

**LP\_SPI\_CLKCNT\_L** Configures clock duty cycles, together with LP\_SPI\_CLKCNT\_H and LP\_SPI\_CLKCNT\_N.

In master transfer, this field must be equal to LP\_SPI\_CLKCNT\_N.

In slave mode, it must be 0.

(R/W)

**LP\_SPI\_CLKCNT\_H** Configures the duty cycle of LP\_SPI\_CLK (high level) in master transfer.

It's recommended to configure this value to  $\text{floor}((\text{LP\_SPI\_CLKCNT\_N} + 1)/2 - 1)$ . `floor()` here is to round a number down, e.g.,  $\text{floor}(2.2) = 2$ .

In slave mode, it must be 0.

(R/W)

**LP\_SPI\_CLKCNT\_N** Configures the divider of LP\_SPI\_CLK in master transfer.

LP\_SPI\_CLK frequency is  $f_{lp\_spi\_clk}/(LP\_SPI\_CLKDIV\_PRE + 1)/(LP\_SPI\_CLKCNT\_N + 1)$ .

(R/W)

**LP\_SPI\_CLKDIV\_PRE** Configures the pre-divider of LP\_SPI\_CLK in master transfer.

(R/W)

**LP\_SPI\_CLK\_EQU\_SYSCLK** Configures whether or not the LP\_SPI\_CLK is equal to lp\_spi\_pclk in master transfer.

0: LP\_SPI\_CLK is divided from lp\_spi\_pclk.

1: LP\_SPI\_CLK is equal to lp\_spi\_pclk.

(R/W)

### Register 38.91. LP\_SPI\_CLK\_GATE\_REG (0x00E8)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |            |   |   |   |               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   | (reserved) |   |   |   | LP_SPI_CLK_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3          | 2 | 1 | 0 |            |   |   |   |               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LP\_SPI\_CLK\_EN** Configures whether or not to enable clock gate.

0: Disable

1: Enable

(R/W)

**Register 38.92. LP\_SPI\_DIN\_MODE\_REG (0x0024)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                           |    |    |   |   |   |   |   |            |   |   |   |   |   |   |   |            |   |   |   |            |   |   |   |                  |   |   |   |                  |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------|----|----|---|---|---|---|---|------------|---|---|---|---|---|---|---|------------|---|---|---|------------|---|---|---|------------------|---|---|---|------------------|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_SPI_TIMING_HCLK_ACTIVE |    |    |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   | (reserved) |   |   |   | (reserved) |   |   |   | LP_SPI_DIN1_MODE |   |   |   | LP_SPI_DINO_MODE |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17                        | 16 | 15 |   |   |   |   |   |            |   | 8 | 7 | 6 | 5 | 4 | 3 | 2          | 1 | 0 |   |            |   |   |   |                  |   |   |   |                  |   |   |   |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                         | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_SPI\_DINO\_MODE** Configures the input mode for LP\_SPI\_D signal.

0: Input without delay

1: Input at the (LP\_SPI\_DINO\_NUM + 1)th falling edge of clk\_spi\_mst

2: Input at the (LP\_SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (LP\_SPI\_DINO\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

**LP\_SPI\_DIN1\_MODE** Configures the input mode for LP\_SPI\_Q signal.

0: Input without delay

1: Input at the (LP\_SPI\_DIN1\_NUM+1)th falling edge of clk\_spi\_mst

2: Input at the (LP\_SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst rising edge cycle

3: Input at the (LP\_SPI\_DIN1\_NUM + 1)th rising edge of clk\_hclk plus one clk\_spi\_mst falling edge cycle

(R/W)

**LP\_SPI\_TIMING\_HCLK\_ACTIVE** Configures whether or not to enable HCLK (high-frequency clock) in LP-SPI input timing module.

0: Disable

1: Enable

(R/W)

**Register 38.93. LP\_SPI\_DIN\_NUM\_REG (0x0028)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |   |   |   |            |   |            |   |                 |   |                 |  |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|---|---|---|------------|---|------------|---|-----------------|---|-----------------|--|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |   |   |   | (reserved) |   | (reserved) |   | LP_SPI_DIN1_NUM |   | LP_SPI_DINO_NUM |  |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            | 8 | 7 | 6 | 5          | 4 | 3          | 2 | 1               | 0 |                 |  |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          |   |   |   | 0          |   | 0          |   | 0               |   | 0               |  | Reset |

**LP\_SPI\_DINO\_NUM** Configures the delays to input signal LP\_SPI\_D based on the setting of LP\_SPI\_DINO\_MODE.

- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)

**LP\_SPI\_DIN1\_NUM** Configures the delays to input signal LP\_SPI\_Q based on the setting of LP\_SPI\_DIN1\_MODE.

- 0: Delayed by 1 clock cycle
  - 1: Delayed by 2 clock cycles
  - 2: Delayed by 3 clock cycles
  - 3: Delayed by 4 clock cycles
- (R/W)

**Register 38.94. LP\_SPI\_DOUT\_MODE\_REG (0x002C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |   |            |   |                   |       |                   |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|---|------------|---|-------------------|-------|-------------------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |   | (reserved) |   | LP_SPI_DOUT1_MODE |       | LP_SPI_DOUT0_MODE |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 4          | 3 | 2          | 1 | 0                 |       |                   |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          | 0 | 0          | 0 | 0                 | Reset |                   |  |

**LP\_SPI\_DOUT0\_MODE** Configures the output mode for LP\_SPI\_D signal.

- 0: Output without delay
  - 1: Output with a delay of an LP-SPI module clock cycle at its falling edge
- (R/W)

**LP\_SPI\_DOUT1\_MODE** Configures the output mode for LP\_SPI\_Q signal.

- 0: Output without delay
  - 1: Output with a delay of an LP-SPI module clock cycle at its falling edge
- (R/W)

Register 38.95. LP\_SPI\_DMA\_INT\_ENA\_REG (0x0034)

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |            |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|------------|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   | LP_SPI_APP1_INT_ENA<br>LP_SPI_APP2_INT_ENA<br>LP_SPI_MST_TX_AFIFO_EMPTY_ERR_INT_ENA<br>LP_SPI_MST_RX_AFIFO_WFULL_ERR_INT_ENA<br>LP_SPI_SLV_CMD_ERR_INT_ENA<br>LP_SPI_SLV_BUF_ADDR_ERR_INT_ENA<br>LP_SPI_WAKEUP_INT_ENA<br>(reserved)<br>LP_SPI_TRANS_DONE_INT_ENA<br>LP_SPI_SLV_WR_BUF_DONE_INT_ENA<br>LP_SPI_SLV_RD_BUF_DONE_INT_ENA |   |   |   |   |    |    |    |    |    |    |    | (reserved) |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14         | 13 | 12 | 11 | 10 | 9 |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_SPI\_SLV\_RD\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/W)

**LP\_SPI\_SLV\_WR\_BUF\_DONE\_INT\_ENA** Write 1 to enable SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(R/W)

**LP\_SPI\_TRANS\_DONE\_INT\_ENA** Write 1 to enable SPI\_TRANS\_DONE\_INT interrupt.  
(R/W)

**LP\_SPI\_WAKEUP\_INT\_ENA** Write 1 to enable LP\_SPI\_WAKEUP\_INT interrupt.  
(R/W)

**LP\_SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(R/W)

**LP\_SPI\_SLV\_CMD\_ERR\_INT\_ENA** Write 1 to enable SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(R/W)

**LP\_SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(R/W)

**LP\_SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ENA** Write 1 to enable SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/W)

**LP\_SPI\_APP2\_INT\_ENA** Write 1 to enable SPI\_APP2\_INT interrupt.  
(R/W)

**LP\_SPI\_APP1\_INT\_ENA** Write 1 to enable SPI\_APP1\_INT interrupt.  
(R/W)



Register 38.96. LP\_SPI\_DMA\_INT\_CLR\_REG (0x0038)

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | LP_SPI_APP1_INT_CLR<br>LP_SPI_APP2_INT_CLR<br>LP_SPI_MST_TX_AFIFO_EMPTY_ERR_INT_CLR<br>LP_SPI_MST_RX_AFIFO_WFULL_ERR_INT_CLR<br>LP_SPI_SLV_BUF_ADDR_ERR_INT_CLR<br>LP_SPI_SLV_CMD_ERR_INT_CLR<br>LP_SPI_WAKEUP_INT_CLR<br>(reserved)<br>LP_SPI_TRANS_DONE_INT_CLR<br>LP_SPI_SLV_WR_BUF_DONE_INT_CLR<br>LP_SPI_SLV_RD_BUF_DONE_INT_CLR |    |    |    |    |    |    |    |    |    |    |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10         | 9 |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

**LP\_SPI\_SLV\_RD\_BUF\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_WR\_BUF\_DONE\_INT\_CLR** Write 1 to clear SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_TRANS\_DONE\_INT\_CLR** Write 1 to clear SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_WAKEUP\_INT\_CLR** Write 1 to clear LP\_SPI\_WAKEUP\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_CMD\_ERR\_INT\_CLR** Write 1 to clear SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_CLR** Write 1 to clear SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_APP2\_INT\_CLR** Write 1 to clear SPI\_APP2\_INT interrupt.  
(WT)

**LP\_SPI\_APP1\_INT\_CLR** Write 1 to clear SPI\_APP1\_INT interrupt.  
(WT)

Register 38.97. LP\_SPI\_DMA\_INT\_RAW\_REG (0x003C)

|            |   |   |   |   |   |   |   |   |   |   |    |  |    |    |    |    |    |    |    |    |    |    |   |            |   |   |   |   |   |   |   |   |   |       |  |
|------------|---|---|---|---|---|---|---|---|---|---|----|--|----|----|----|----|----|----|----|----|----|----|---|------------|---|---|---|---|---|---|---|---|---|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |    | LP_SPI_APP1_INT_RAW<br>LP_SPI_APP2_INT_RAW<br>LP_SPI_MST_TX_AFIFO_EMPTY_ERR_INT_RAW<br>LP_SPI_MST_RX_AFIFO_WFULL_ERR_INT_RAW<br>LP_SPI_SLV_CMD_ERR_INT_RAW<br>LP_SPI_SLV_BUF_ADDR_ERR_INT_RAW<br>(reserved)<br>LP_SPI_TRANS_DONE_INT_RAW<br>LP_SPI_SLV_WR_BUF_DONE_INT_RAW<br>LP_SPI_SLV_RD_BUF_DONE_INT_RAW |    |    |    |    |    |    |    |    |    |    |   | (reserved) |   |   |   |   |   |   |   |   |   |       |  |
| 31         |   |   |   |   |   |   |   |   |   |   | 21 | 20   | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 |            |   |   |   |   |   |   |   |   |   | 0     |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |  |

**LP\_SPI\_SLV\_RD\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_SLV\_WR\_BUF\_DONE\_INT\_RAW** The raw interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of SPI\_TRANS\_DONE\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_WAKEUP\_INT\_RAW** The raw interrupt status of LP\_SPI\_LP\_SPI\_WAKEUP\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_SLV\_CMD\_ERR\_INT\_RAW** The raw interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_RAW** The raw interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(R/WTC/SS)

**LP\_SPI\_APP2\_INT\_RAW** The raw interrupt status of SPI\_APP2\_INT interrupt.  
The value is only controlled by the application.  
(R/WTC/SS)

**LP\_SPI\_APP1\_INT\_RAW** The raw interrupt status of SPI\_APP1\_INT interrupt.  
The value is only controlled by the application.  
(R/WTC/SS)

Register 38.98. LP\_SPI\_DMA\_INT\_ST\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_SPI_APP1_INT_ST<br>LP_SPI_APP2_INT_ST<br>LP_SPI_MST_TX_INT_ST<br>LP_SPI_MST_RX_AFIFO_EMPTY_ERR_INT_ST<br>LP_SPI_SLV_CMD_ERR_INT_ST<br>LP_SPI_SLV_BUF_ADDR_ERR_INT_ST<br>LP_SPI_WAKEUP_INT_ST<br>(reserved)<br>LP_SPI_TRANS_DONE_INT_ST<br>LP_SPI_SLV_WR_BUF_DONE_INT_ST<br>LP_SPI_SLV_RD_BUF_DONE_INT_ST |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |   |   |   |   |            |   |   |   |   |   | 9 |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LP\_SPI\_SLV\_RD\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(RO)

**LP\_SPI\_SLV\_WR\_BUF\_DONE\_INT\_ST** The interrupt status of SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(RO)

**LP\_SPI\_TRANS\_DONE\_INT\_ST** The interrupt status of SPI\_TRANS\_DONE\_INT interrupt.  
(RO)

**LP\_SPI\_WAKEUP\_INT\_ST** The interrupt status bit of LP\_SPI\_WAKEUP\_INT interrupt.  
(RO)

**LP\_SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_ST** The interrupt status bit of SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(RO)

**LP\_SPI\_SLV\_CMD\_ERR\_INT\_ST** The interrupt status of SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(RO)

**LP\_SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(RO)

**LP\_SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_ST** The interrupt status of SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(RO)

**LP\_SPI\_APP2\_INT\_ST** The interrupt status of SPI\_APP2\_INT interrupt.  
(RO)

**LP\_SPI\_APP1\_INT\_ST** The interrupt status of SPI\_APP1\_INT interrupt.  
(RO)

Register 38.99. LP\_SPI\_DMA\_INT\_SET\_REG (0x004C)

|            |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |    |            |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|----|------------|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   | LP_SPI_APP1_INT_SET<br>LP_SPI_APP2_INT_SET<br>LP_SPI_MST_TX_AFIFO_EMPTY_ERR_INT_SET<br>LP_SPI_MST_RX_AFIFO_WFULL_ERR_INT_SET<br>LP_SPI_SLV_CMD_ERR_INT_SET<br>LP_SPI_SLV_BUF_ADDR_ERR_INT_SET<br>(reserved)<br>LP_SPI_TRANS_DONE_INT_SET<br>LP_SPI_SLV_WR_BUF_DONE_INT_SET<br>LP_SPI_SLV_RD_BUF_DONE_INT_SET |    |    |    |    |    |    |    |    |    | (reserved) |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |  | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12         | 11 | 10 | 9 |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_SPI\_SLV\_RD\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_RD\_BUF\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_WR\_BUF\_DONE\_INT\_SET** Write 1 to set SPI\_SLV\_WR\_BUF\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_TRANS\_DONE\_INT\_SET** Write 1 to set SPI\_TRANS\_DONE\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_BUF\_ADDR\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_BUF\_ADDR\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_SLV\_CMD\_ERR\_INT\_SET** Write 1 to set SPI\_SLV\_CMD\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_RX\_AFIFO\_WFULL\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT\_SET** Write 1 to set SPI\_MST\_TX\_AFIFO\_EMPTY\_ERR\_INT interrupt.  
(WT)

**LP\_SPI\_APP2\_INT\_SET** Write 1 to set SPI\_APP2\_INT interrupt.  
(WT)

**LP\_SPI\_APP1\_INT\_SET** Write 1 to set SPI\_APP1\_INT interrupt.  
(WT)

**Register 38.100. LP\_SPI\_WO\_REG (0x0098)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF0</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF0** 32-bit data buffer 0.  
(R/W/SS)

**Register 38.101. LP\_SPI\_W1\_REG (0x009C)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF1</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF1** 32-bit data buffer 1.  
(R/W/SS)

**Register 38.102. LP\_SPI\_W2\_REG (0x00A0)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF2</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF2** 32-bit data buffer 2.  
(R/W/SS)

**Register 38.103. LP\_SPI\_W3\_REG (0x00A4)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF3</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF3** 32-bit data buffer 3.  
(R/W/SS)

LP\_SPI\_BUF4

LP\_SPI\_BUF5

LP\_SPI\_BUF6

LP\_SPI\_BUF7

**Register 38.108. LP\_SPI\_W8\_REG (0x00B8)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF8</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF8** 32-bit data buffer 8.  
(R/W/SS)

**Register 38.109. LP\_SPI\_W9\_REG (0x00BC)**

|                    |   |
|--------------------|---|
| <i>LP_SPI_BUF9</i> |   |
| 31                 | 0 |
| 0                  |   |
| Reset              |   |

**LP\_SPI\_BUF9** 32-bit data buffer 9.  
(R/W/SS)

**Register 38.110. LP\_SPI\_W10\_REG (0x00C0)**

|                     |   |
|---------------------|---|
| <i>LP_SPI_BUF10</i> |   |
| 31                  | 0 |
| 0                   |   |
| Reset               |   |

**LP\_SPI\_BUF10** 32-bit data buffer 10.  
(R/W/SS)

**Register 38.111. LP\_SPI\_W11\_REG (0x00C4)**

|                     |   |
|---------------------|---|
| <i>LP_SPI_BUF11</i> |   |
| 31                  | 0 |
| 0                   |   |
| Reset               |   |

**LP\_SPI\_BUF11** 32-bit data buffer 11.  
(R/W/SS)

LP\_SPI\_BUF12

LP\_SPI\_BUF13

LP\_SPI\_BUF14

LP\_SPI\_BUF15



Register 38.116. LP\_SPI\_DATE\_REG (0x00F0)

|            |    |    |   |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|------------|----|----|---|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved) |    |    |   | LP_SPI_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31         | 28 | 27 | 0 |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0          | 0  | 0  | 0 | 0x2009040   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

LP\_SPI\_DATE Version control register.  
(R/W)

## Chapter 39

### I2C Controller (I2C)

The I2C (Inter-Integrated Circuit) bus allows ESP32-P4 to communicate with multiple external devices. These external devices can share one I2C bus. ESP32-P4 has three I2C controllers: two in the main system and one in the low-power system. The two I2C controllers in the main system can act as a master or a slave (referred to as I2C below), while the one in the low-power system can only act as a master (referred to as LP\_I2C below), which can still work when the main system sleeps.

#### 39.1 Overview

The I2C bus has two lines, namely a serial data line (SDA) and a serial clock line (SCL). Both SDA and SCL lines are open-drain. The I2C bus can be connected to a single or multiple master devices and a single or multiple slave devices. However, only one master device can access a slave at a time via the bus.

The master initiates communication by generating a START condition: pulling the SDA line low while SCL is high. Then it issues nine clock pulses via SCL. The first eight pulses are used to transmit a 7-bit address followed by a read/write ( $R/\overline{W}$ ) bit. If the address of an I2C slave matches the 7-bit address transmitted, this matching slave can respond by pulling SDA low on the ninth clock pulse. The master and the slave can send or receive data according to the  $R/\overline{W}$  bit. Whether to terminate the data transfer or not is determined by the logic level of the acknowledge (ACK) bit. During data transfer, SDA changes only when SCL is low. Once the communication has finished, the master sends a STOP condition: pulling SDA up while SCL is high. If a master both reads and writes data in one transfer, then it should send a RSTART condition, a slave address, and a  $R/\overline{W}$  bit before changing its operation. The RSTART condition is used to change the transfer direction and the mode of the devices (master mode or slave mode).

#### 39.2 Features

The I2C controller of ESP32-P4 has the following features:

- Master mode and slave mode
- Communication between multiple masters and slaves
- Standard mode (100 Kbit/s)
- Fast mode (400 Kbit/s)
- 7-bit addressing and 10-bit addressing
- Continuous data transfer achieved by pulling SCL low in slave mode
- Programmable digital noise filtering
- Dual address mode, which uses slave address and slave memory or register address

## 39.3 I2C Architecture

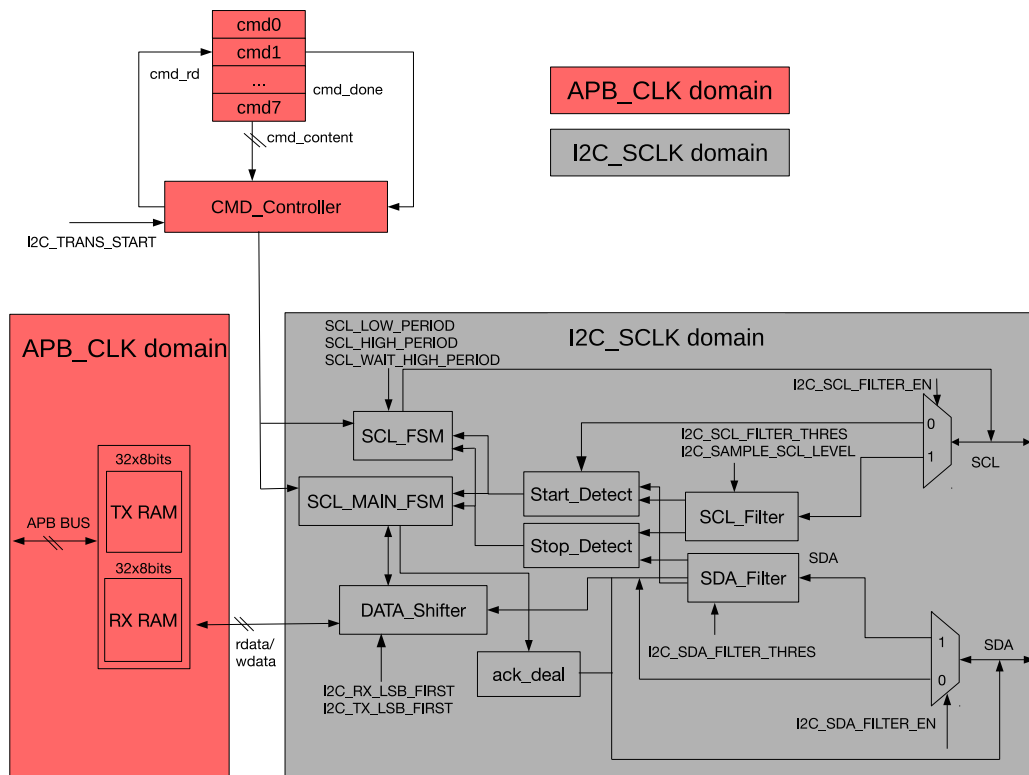


Figure 39.3-1. I2C Master Architecture

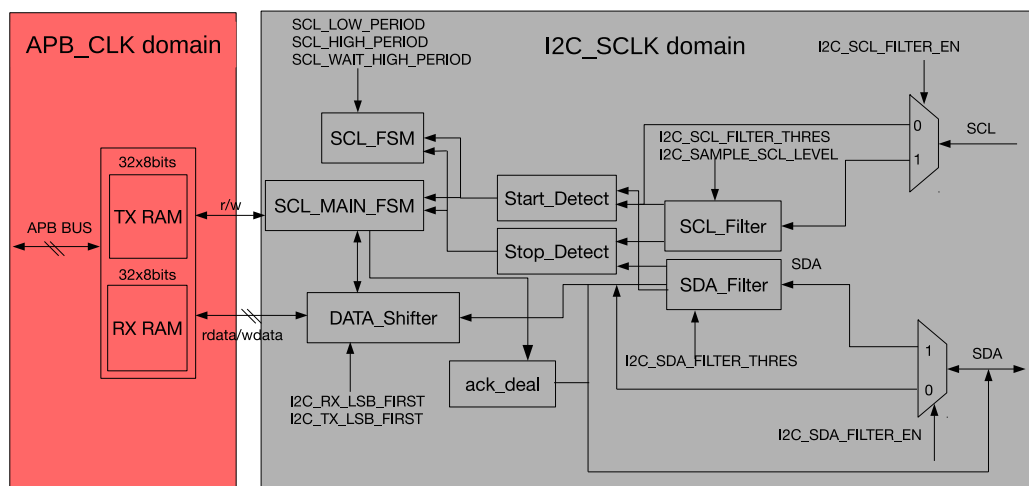


Figure 39.3-2. I2C Slave Architecture

The I2C controller runs either in master mode or slave mode, which is determined by `I2C_MS_MODE`. Figure 39.3-1 shows the architecture of a master, while Figure 39.3-2 shows that of a slave. The I2C controller has the following main parts:

- Transmit and receive memory (TX/RX RAM): store data to be transmitted and data received respectively.
- Command controller (CMD\_Controller): generate (R)START, STOP, WRITE, READ, and END commands

- SCL clock controller (SCL\_FSM): generate the timing sequence conforming to the I2C protocol. Figure 39.3-3 and Table 39.3-1 are the timing diagram and corresponding parameters of the I2C protocol.
- SDA data controller (SCL\_MAIN\_FSM): control the execution of I2C commands and the data sequence of the SDA line. It also controls the ACK\_deal module to generate the ACK bit and detect the level of the ACK bit on the SDA line.
- Serial/parallel data converter (DATA\_Shifter): shift data between serial and parallel form
- Filter for SCL (SCL\_Filter): remove noises on SCL input signals
- Filter for SDA (SDA\_Filter): remove noises on SDA input signals
- ACK bit controller (ack\_deal): generate the ACK bit and detect the level of the ACK bit on the SDA line under the control of SCL\_MAIN\_FSM.

Besides, the I2C controller also has a clock module that generates I2C clocks, and a synchronization module that synchronizes the APB bus and the I2C controller.

The clock module is used to select clock sources, turn on and off clocks, and divide clocks. The synchronization module synchronizes signal transfer between different clock domains.

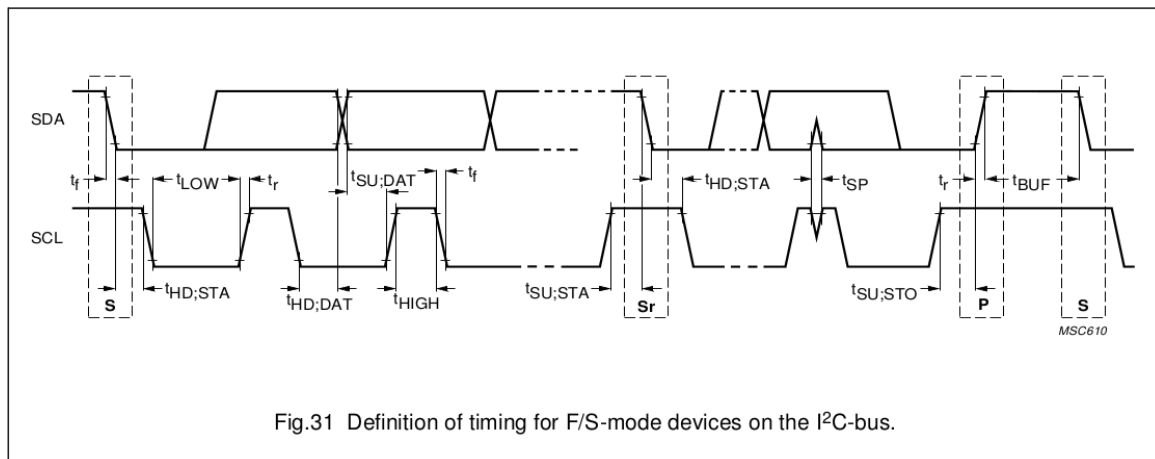


Figure 39.3-3. I2C Protocol Timing (Cited from Fig.31 in [The I2C-bus specification](#) Version 2.1)

| PARAMETER   | SYMBOL              | STANDARD-MODE    |                     | FAST-MODE                             |                    | UNIT |
|---|---------------------|------------------|---------------------|---------------------------------------|--------------------|------|
|   |                     | MIN.             | MAX.                | MIN.                                  | MAX.               |      |
| SCL clock frequency   | f <sub>SCL</sub>    | 0                | 100                 | 0                                     | 400                | kHz  |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated                   | t <sub>HD;STA</sub> | 4.0              | —                   | 0.6                                   | —                  | μs   |
| LOW period of the SCL clock   | t <sub>LOW</sub>    | 4.7              | —                   | 1.3                                   | —                  | μs   |
| HIGH period of the SCL clock  | t <sub>HIGH</sub>   | 4.0              | —                   | 0.6                                   | —                  | μs   |
| Set-up time for a repeated START condition  | t <sub>SU;STA</sub> | 4.7              | —                   | 0.6                                   | —                  | μs   |
| Data hold time:<br>for CBUS compatible masters (see NOTE, Section 10.1.3)<br>for I <sup>2</sup> C-bus devices | t <sub>HD;DAT</sub> | 5.0              | —                   | —                                     | —                  | μs   |
|   |                     | 0 <sup>(2)</sup> | 3.45 <sup>(3)</sup> | 0 <sup>(2)</sup>                      | 0.9 <sup>(3)</sup> | μs   |
| Data set-up time  | t <sub>SU;DAT</sub> | 250              | —                   | 100 <sup>(4)</sup>                    | —                  | ns   |
| Rise time of both SDA and SCL signals   | t <sub>r</sub>      | —                | 1000                | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns   |
| Fall time of both SDA and SCL signals   | t <sub>f</sub>      | —                | 300                 | 20 + 0.1C <sub>b</sub> <sup>(5)</sup> | 300                | ns   |
| Set-up time for STOP condition  | t <sub>SU;STO</sub> | 4.0              | —                   | 0.6                                   | —                  | μs   |
| Bus free time between a STOP and START condition  | t <sub>BUF</sub>    | 4.7              | —                   | 1.3                                   | —                  | μs   |

Table 39.3-1. I2C Timing Parameters (Cited from Table 5 in [The I2C-bus specification](#) Version 2.1)

## 39.4 Functional Description

As mentioned above, one or more masters and one or more slaves can be connected on the I2C bus. The following sections describe the operations of the ESP32-P4 I2C controllers. Note that operations may differ between the I2C controllers in ESP32-P4 and other masters or slaves on the bus. Please refer to datasheets of individual I2C devices for specific information.

### 39.4.1 Clock Configuration

Registers, TX RAM, and RX RAM are configured and accessed in the APB\_CLK clock domain. The main logic of the I2C controller, including SCL\_FSM, SCL\_MAIN\_FSM, SCL\_FILTER, SDA\_FILTER, and DATA\_SHIFTER, are in the I2C\_SCLK clock domain.

You can configure the clock source for I2C\_SCLK of I2C0 in the main system (HP) to FOSC\_20M\_CLK or XTAL\_40M\_CLK via [HP\\_SYS\\_CLKRST\\_I2C0\\_CLK\\_SRC\\_SEL](#) and configure that of I2C1 in the main system via [HP\\_SYS\\_CLKRST\\_I2C1\\_CLK\\_SRC\\_SEL](#). For the clock source for I2C\_SCLK of LP\_I2C in the low-power system (LP), you can configure it to XTAL\_D2\_CLK, LP\_DYN\_FAST\_CLK, or PLL\_LP\_CLK 8 MHz via [LPPERI\\_LP\\_I2C\\_CLK\\_SEL](#).

The steps to configure the clock source for HP I2C0 are as follows:

- Enable the clock source for I2C\_SCLK of I2C0 by configuring [HP\\_SYS\\_CLKRST\\_I2C0\\_CLK\\_EN](#) to 1.
- When [HP\\_SYS\\_CLKRST\\_I2C0\\_SRC\\_SEL](#) is 0, the clock source is XTAL\_40M\_CLK.
- When [HP\\_SYS\\_CLKRST\\_I2C0\\_SRC\\_SEL](#) is 1, the clock source is FOSC\_20M\_CLK.

The steps to configure the clock source for HP I2C1 are as follows:

- Enable the clock source for I2C\_SCLK of I2C1 by configuring [HP\\_SYS\\_CLKRST\\_I2C1\\_CLK\\_EN](#) to 1.

- When `HP_SYS_CLKRST_I2C1_SRC_SEL` is 0, the clock source is `XTAL_40M_CLK`.
- When `HP_SYS_CLKRST_I2C1_SRC_SEL` is 1, the clock source is `FOSC_20M_CLK`.

The steps to configure the clock source for LP\_I2C are as follows:

- Enable the clock source for I2C\_SCLK of LP\_I2C by configuring `LPPERI_CK_EN_LP_I2C` to 1.
- When `LPPERI_LP_I2C_CLK_SEL` is 0, the clock source is `LP_DYN_FAST_CLK`.
- When `LPPERI_LP_I2C_CLK_SEL` is 1, the clock source is `XTAL_D2_CLK`.
- When `LPPERI_LP_I2C_CLK_SEL` is 2, the clock source is `PLL_LP_CLK` 8 MHz.

The clock source then passes through a fractional divider to generate I2C\_SCLK according to the following equation:

$$I2C\_SCLK\_DIV\_NUM + 1 + \frac{I2C\_SCLK\_DIV\_A}{I2C\_SCLK\_DIV\_B}$$

In the equation, `I2C_SCLK_DIV_NUM` represents the integer part of the divisor, `I2C_SCLK_DIV_A` represents the numerator of the fractional part of the divisor, and `I2C_SCLK_DIV_B` represents the denominator of the fractional part of the divisor. Limited by timing parameters, the derived clock I2C\_SCLK should operate at a frequency 20 times larger than SCL's frequency.

For I2C0:

- Configure `I2C_SCLK_DIV_NUM` via `HP_SYS_CLKRST_I2C0_CLK_DIV_NUM`.
- Configure `I2C_SCLK_DIV_A` via `HP_SYS_CLKRST_I2C0_CLK_DIV_NUMERATOR`.
- Configure `I2C_SCLK_DIV_B` via `HP_SYS_CLKRST_I2C0_CLK_DIV_DENOMINATOR`.

For I2C1:

- Configure `I2C_SCLK_DIV_NUM` via `HP_SYS_CLKRST_I2C1_CLK_DIV_NUM`.
- Configure `I2C_SCLK_DIV_A` via `HP_SYS_CLKRST_I2C1_CLK_DIV_NUMERATOR`.
- Configure `I2C_SCLK_DIV_B` via `HP_SYS_CLKRST_I2C1_CLK_DIV_DENOMINATOR`.

### 39.4.2 SCL and SDA Noise Filtering

`SCL_Filter` and `SDA_Filter` modules are identical and are used to filter signal noise on SCL and SDA, respectively. These filters can be enabled or disabled by configuring `I2C_SCL_FILTER_EN` and `I2C_SDA_FILTER_EN`.

Take `SCL_Filter` as an example. When enabled, `SCL_Filter` samples input signals on the SCL line continuously. These input signals are valid only if they remain unchanged for consecutive `I2C_SCL_FILTER_THRES` `I2C_SCLK` clock cycles. Given that only valid input signals can pass through the filter, `SCL_Filter` can remove glitches whose pulse width is shorter than `I2C_SCL_FILTER_THRES` `I2C_SCLK` clock cycles, while `SDA_Filter` can remove glitches whose pulse width is shorter than `I2C_SDA_FILTER_THRES` `I2C_SCLK` clock cycles.

### 39.4.3 SCL Clock Stretching

The I2C controller in slave mode (i.e., slave) can realize the function called clock stretching by holding the SCL line low to suspend data transmission in exchange for more time to process data. This function is enabled

by setting the [I2C\\_SLAVE\\_SCL\\_STRETCH\\_EN](#) bit. The time period to release the SCL line from stretching is configured by setting the [I2C\\_STRETCH\\_PROTECT\\_NUM](#) field, in order to avoid timing sequence errors. The slave can choose to achieve clock stretching by holding the SCL line low when one of the following four events occurs:

1. Address match: The address of the slave matches the address sent by the master via the SDA line, and the  $R/\overline{W}$  bit is 1.
2. RAM being full: RX RAM of the slave is full. Note that when the slave receives less than the FIFO depth, which is 32 bytes in ESP32-P4 I2C, it is not necessary to enable clock stretching; when the slave receives FIFO depth bytes or more, you may interrupt data transmission to wrapped around RAM via the FIFO threshold, or enable clock stretching for more time to process data. When clock stretching is enabled, [I2C\\_RX\\_FULL\\_ACK\\_LEVEL](#) must be cleared, otherwise there will be unpredictable consequences.
3. RAM being empty: The slave is sending data, but its TX RAM is empty.
4. Sending an ACK: If [I2C\\_SLAVE\\_BYTE\\_ACK\\_CTL\\_EN](#) is set, the slave pulls SCL low when sending an ACK bit. At this stage, software validates data and configures [I2C\\_SLAVE\\_BYTE\\_ACK\\_LVL](#) to control the level of the ACK bit. Note that when RX RAM of the slave is full, the level of the ACK bit to be sent is determined by [I2C\\_RX\\_FULL\\_ACK\\_LEVEL](#), instead of [I2C\\_SLAVE\\_BYTE\\_ACK\\_LVL](#). In this case, [I2C\\_RX\\_FULL\\_ACK\\_LEVEL](#) should also be cleared to ensure proper functioning of clock stretching.

When clock stretching occurs, the cause of stretching can be read from the [I2C\\_STRETCH\\_CAUSE](#) bit. Clock stretching can be disabled by setting the [I2C\\_SLAVE\\_SCL\\_STRETCH\\_CLR](#) bit.

### 39.4.4 Generating SCL Pulses in Idle State

Usually, when the I2C bus is idle, the SCL line is held high. The I2C controller in ESP32-P4 can be programmed to generate SCL pulses in an idle state. This function only works when the I2C controller is configured as master. If the [I2C\\_SCL\\_RST\\_SLV\\_EN](#) bit is set, hardware will send [I2C\\_SCL\\_RST\\_SLV\\_NUM](#) SCL pulses, and then automatically clear the [I2C\\_SCL\\_RST\\_SLV\\_EN](#) bit.

### 39.4.5 Synchronization

I2C registers are configured in the APB\_CLK domain, whereas the I2C controller is configured in the asynchronous I2C\_SCLK domain. Therefore, before being used by the I2C controller, register values should be synchronized by first writing configuration registers and then writing 1 to [I2C\\_CONF\\_UPGATE](#). Registers that need synchronization are listed in Table [39.4-1](#).

Table 39.4-1. I2C Synchronous Registers

| Register                     | Field                      | Address |
|------------------------------|----------------------------|---------|
| I2C_CTR_REG                  | I2C_SLV_TX_AUTO_START_EN   | 0x0004  |
|                              | I2C_ADDR_10BIT_RW_CHECK_EN |         |
|                              | I2C_ADDR_BROADCASTING_EN   |         |
|                              | I2C_SDA_FORCE_OUT          |         |
|                              | I2C_SCL_FORCE_OUT          |         |
|                              | I2C_SAMPLE_SCL_LEVEL       |         |
|                              | I2C_RX_FULL_ACK_LEVEL      |         |
|                              | I2C_MS_MODE                |         |
|                              | I2C_TX_LSB_FIRST           |         |
|                              | I2C_RX_LSB_FIRST           |         |
|                              | I2C_ARBITRATION_EN         |         |
| I2C_TO_REG                   | I2C_TIME_OUT_EN            | 0x000C  |
|                              | I2C_TIME_OUT_VALUE         |         |
| I2C_SLAVE_ADDR_REG           | I2C_ADDR_10BIT_EN          | 0x0010  |
|                              | I2C_SLAVE_ADDR             |         |
| I2C_FIFO_CONF_REG            | I2C_FIFO_ADDR_CFG_EN       | 0x0018  |
| I2C_SCL_SP_CONF_REG          | I2C_SDA_PD_EN              | 0x0080  |
|                              | I2C_SCL_PD_EN              |         |
|                              | I2C_SCL_RST_SLV_NUM        |         |
|                              | I2C_SCL_RST_SLV_EN         |         |
| I2C_SCL_STRETCH_CONF_REG     | I2C_SLAVE_BYTE_ACK_CTL_EN  | 0x0084  |
|                              | I2C_SLAVE_BYTE_ACK_LVL     |         |
|                              | I2C_SLAVE_SCL_STRETCH_EN   |         |
|                              | I2C_STRETCH_PROTECT_NUM    |         |
| I2C_SCL_LOW_PERIOD_REG       | I2C_SCL_LOW_PERIOD         | 0x0000  |
| I2C_SCL_HIGH_PERIOD_REG      | I2C_WAIT_HIGH_PERIOD       | 0x0038  |
|                              | I2C_HIGH_PERIOD            |         |
| I2C_SDA_HOLD_REG             | I2C_SDA_HOLD_TIME          | 0x0030  |
| I2C_SDA_SAMPLE_REG           | I2C_SDA_SAMPLE_TIME        | 0x0034  |
| I2C_SCL_START_HOLD_REG       | I2C_SCL_START_HOLD_TIME    | 0x0040  |
| I2C_SCL_RSTART_SETUP_REG     | I2C_SCL_RSTART_SETUP_TIME  | 0x0044  |
| I2C_SCL_STOP_HOLD_REG        | I2C_SCL_STOP_HOLD_TIME     | 0x0048  |
| I2C_SCL_STOP_SETUP_REG       | I2C_SCL_STOP_SETUP_TIME    | 0x004C  |
| I2C_SCL_ST_TIME_OUT_REG      | I2C_SCL_ST_TO_I2C          | 0x0078  |
| I2C_SCL_MAIN_ST_TIME_OUT_REG | I2C_SCL_MAIN_ST_TO_I2C     | 0x007C  |
| I2C_FILTER_CFG_REG           | I2C_SCL_FILTER_EN          | 0x0050  |
|                              | I2C_SCL_FILTER_THRES       |         |
|                              | I2C_SDA_FILTER_EN          |         |
|                              | I2C_SDA_FILTER_THRES       |         |

### 39.4.6 Open-Drain Output

SCL and SDA output drivers must be configured as open-drain. There are two ways to achieve this:



1. Set `I2C_SCL_FORCE_OUT` and `I2C_SDA_FORCE_OUT`, and configure `GPIO_PINn_PAD_DRIVER` for corresponding SCL and SDA pads as open-drain.
2. Clear `I2C_SCL_FORCE_OUT` and `I2C_SDA_FORCE_OUT`.

Because these lines are configured as open-drain, the low-to-high transition time of each line is longer, determined together by the pull-up resistor and line capacitance. The output duty cycle of I2C is limited by the SDA and SCL line's pull-up speed, mainly SCL's speed.

In addition, when `I2C_SCL_FORCE_OUT` and `I2C_SCL_PD_EN` are set to 1, SCL can be forced low; when `I2C_SDA_FORCE_OUT` and `I2C_SDA_PD_EN` are set to 1, SDA can be forced low.

### 39.4.7 Timing Parameter Configuration

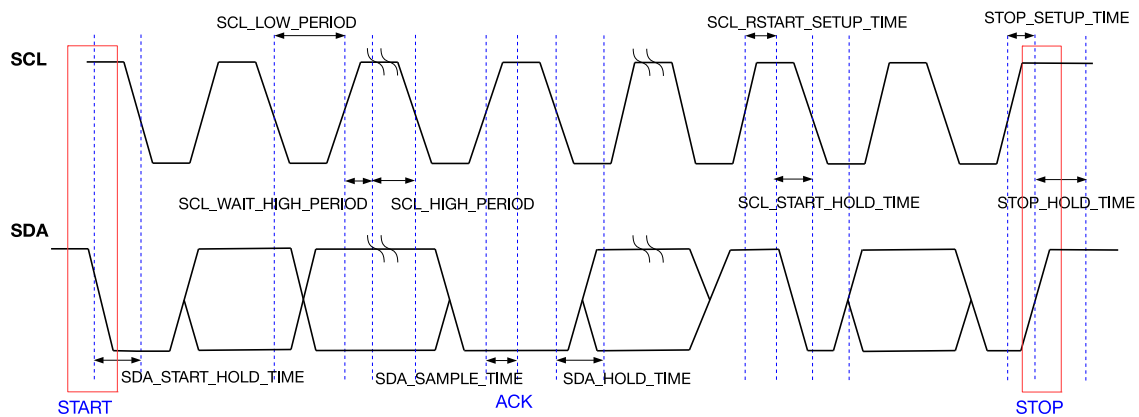


Figure 39.4-1. I2C Timing Diagram

Figure 39.4-1 shows the timing diagram of an I2C master. This figure also specifies registers used to configure the START bit, STOP bit, data hold time, data sample time, waiting time on the rising SCL edge, etc. Timing parameters are calculated as follows in `I2C_SCLK` clock cycles:

1.  $t_{LOW} = (I2C\_SCL\_LOW\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
2.  $t_{HIGH} = (I2C\_SCL\_HIGH\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
3.  $t_{SU:STA} = (I2C\_SCL\_RSTART\_SETUP\_TIME + 1) \cdot T_{I2C\_SCLK}$
4.  $t_{HD:STA} = (I2C\_SCL\_START\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
5.  $t_r = (I2C\_SCL\_WAIT\_HIGH\_PERIOD + 1) \cdot T_{I2C\_SCLK}$
6.  $t_{SU:STO} = (I2C\_SCL\_STOP\_SETUP\_TIME + 1) \cdot T_{I2C\_SCLK}$
7.  $t_{BUF} = (I2C\_SCL\_STOP\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
8.  $t_{HD:DAT} = (I2C\_SDA\_HOLD\_TIME + 1) \cdot T_{I2C\_SCLK}$
9.  $t_{SU:DAT} = (I2C\_SCL\_LOW\_PERIOD - I2C\_SDA\_HOLD\_TIME) \cdot T_{I2C\_SCLK}$

Timing registers below are divided into two groups, depending on the mode in which these registers are active:

- Master mode only:

1. **I2C\_SCL\_START\_HOLD\_TIME**: Specifies the interval between the moment SDA is pulled low and the moment SCL is pulled low when the master generates a START condition. This interval is (**I2C\_SCL\_START\_HOLD\_TIME** + 1) in I2C\_SCLK cycles. This register is active only when the I2C controller works in master mode.
2. **I2C\_SCL\_LOW\_PERIOD**: Specifies the low period of SCL. This period lasts (**I2C\_SCL\_LOW\_PERIOD** + 1) in I2C\_SCLK cycles. This register is active only when the I2C controller works in master mode.

However, this period could be extended in the following scenarios:

- SCL is pulled low by peripheral devices when I2C acts as a master.
  - SCL is pulled low by an END command executed by the I2C controller.
  - SCL is pulled low by clock stretching when I2C acts as a slave.
3. **I2C\_SCL\_WAIT\_HIGH\_PERIOD**: Specifies the time for SCL to switch from low to high in I2C\_SCLK cycles. Please make sure that SCL can be pulled high within this time period. Otherwise, the high period of SCL may be incorrect. This register is active only when the I2C controller works in master mode.
  4. **I2C\_SCL\_HIGH\_PERIOD**: Specifies the high period of SCL in I2C\_SCLK cycles. This register is active only when the I2C controller works in master mode. When SCL goes high within (**I2C\_SCL\_WAIT\_HIGH\_PERIOD** + 1) in I2C\_SCLK cycles, its frequency is:

$$f_{scl} = \frac{f_{I2C\_SCLK}}{I2C\_SCL\_LOW\_PERIOD + I2C\_SCL\_HIGH\_PERIOD + I2C\_SCL\_WAIT\_HIGH\_PERIOD + 3 + I2C\_SCL\_FILTER\_THRES}$$

where 3 represents the amount of clock cycles required to synchronize the SCL. If the SCL filtering function is turned on, the delay caused by **I2C\_SCL\_FILTER\_THRES** needs to be added. As the SCL low-to-high transition time represented by **I2C\_SCL\_WAIT\_HIGH\_PERIOD** + 1 module clock can be affected by the pull-up resistor, IO drive capability, SCL line capacitance, etc., deviation may occur between the actual frequency of the test and the theoretical frequency. At this point, deviations can be reduced by adjusting the value of **I2C\_SCL\_WAIT\_HIGH\_PERIOD**.

- Master mode and slave mode:

1. **I2C\_SDA\_SAMPLE\_TIME**: Specifies the interval between the rising edge of SCL and the level sampling time of SDA. It is advised to set a value in the middle of SCL's high period, so as to correctly sample the level of SCL. This register is active both in master mode and slave mode.
2. **I2C\_SDA\_HOLD\_TIME**: Specifies the interval between changing the SDA output level and the falling edge of SCL. This register is active both in master mode and slave mode.

Timing parameters limits corresponding register configuration.

1.  $\frac{f_{I2C\_SCLK}}{f_{SCL}} > 20$
2.  $3 \times f_{I2C\_SCLK} \leq (I2C\_SDA\_HOLD\_TIME - 4) \times f_{APB\_CLK}$
3.  $I2C\_SDA\_HOLD\_TIME + I2C\_SCL\_START\_HOLD\_TIME > SDA\_FILTER\_THRES + 3$
4.  $I2C\_SCL\_WAIT\_HIGH\_PERIOD < I2C\_SDA\_SAMPLE\_TIME < I2C\_SCL\_HIGH\_PERIOD$
5.  $I2C\_SDA\_SAMPLE\_TIME < I2C\_SCL\_WAIT\_HIGH\_PERIOD + I2C\_SCL\_START\_HOLD\_TIME + I2C\_SCL\_RSTART\_SETUP\_TIME$
6.  $I2C\_STRETCH\_PROTECT\_NUM + I2C\_SDA\_HOLD\_TIME > I2C\_SCL\_LOW\_PERIOD$

### 39.4.8 Timeout Control

The I2C controller has three types of timeout control, namely timeout control for SCL\_FSM, for SCL\_MAIN\_FSM, and for the SCL line. The first two are always enabled, while the third is configurable.

When SCL\_FSM remains unchanged for more than  $2^{I2C\_SCL\_ST\_TO\_I2C}$  clock cycles, an `I2C_SCL_ST_TO_INT` interrupt is triggered, and then SCL\_FSM goes to idle state. The value of `I2C_SCL_ST_TO_I2C` should be less than or equal to 22, which means SCL\_FSM could remain unchanged for  $2^{22}$  I2C\_SCLK clock cycles at most before the interrupt is generated.

When SCL\_MAIN\_FSM remains unchanged for more than  $2^{I2C\_SCL\_MAIN\_ST\_TO\_I2C}$  I2C\_SCLK clock cycles, an `I2C_SCL_MAIN_ST_TO_INT` interrupt is triggered, and then SCL\_MAIN\_FSM goes to idle state. The value of `I2C_SCL_MAIN_ST_TO_I2C` should be less than or equal to 22, which means SCL\_MAIN\_FSM could remain unchanged for  $2^{22}$  clock cycles at most before the interrupt is generated.

Timeout control for SCL is enabled by setting `I2C_TIME_OUT_EN`. When the level of SCL remains unchanged for more than  $2^{I2C\_TIME\_OUT\_VALUE}$  clock cycles, an `I2C_TIME_OUT_INT` interrupt is triggered, and then the I2C bus goes to idle state.

### 39.4.9 Command Configuration

When the I2C controller works in master mode, CMD\_Controller reads commands from 8 sequential command registers and controls SCL\_FSM and SCL\_MAIN\_FSM accordingly.

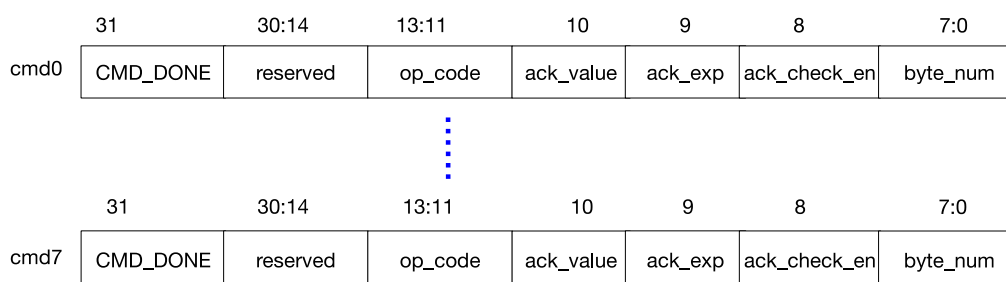


Figure 39.4-2. Structure of I2C Command Registers

Command registers, whose structure is illustrated in Figure 39.4-2, are active only when the I2C controller works in master mode. Fields of command registers are:

1. **CMD\_DONE**: Indicates that a command has been executed. After each command has been executed, the CMD\_DONE bit in the corresponding command register is set to 1 by hardware. By reading this bit, the software can tell if the command has been executed. When writing new commands, this bit must be cleared by software.
2. **op\_code**: Indicates the command. The I2C controller supports five commands:
  - **WRITE**: `op_code` = 1. The I2C controller sends a slave address, a register address (only in dual address mode), and data to the slave.
  - **STOP**: `op_code` = 2. The I2C controller sends a STOP bit defined by the I2C protocol. This code also indicates that the command sequence has been executed, and the CMD\_Controller stops reading commands. After restarted by software, the CMD\_Controller resumes reading commands from command register 0.

- READ: op\_code = 3. The I2C controller reads data from the slave.
  - END: op\_code = 4. The I2C controller pulls the SCL line down and suspends I2C communication. This code also indicates that the command sequence has been completed, and the CMD\_Controller stops executing commands. Once the software refreshes data in command registers and the RAM, the CMD\_Controller can be restarted to execute commands from command register 0 again.
  - RSTART: op\_code = 6. The I2C controller sends a START bit or a RSTART bit defined by the I2C protocol.
3. ack\_value: Used to configure the level of the ACK bit sent by the I2C controller during a read operation. This bit is ignored in RSTART, STOP, END, and WRITE conditions.
  4. ack\_exp: Used to configure the level of the ACK bit expected by the I2C controller during a write operation. This bit is ignored during RSTART, STOP, END, and READ conditions.
  5. ack\_check\_en: Used to enable the I2C controller during a write operation to check whether the ACK level sent by the slave matches ack\_exp in the command. If this bit is set and the level received does not match ack\_exp in the WRITE command, the master will generate an I2C\_NACK\_INT interrupt and a STOP condition for data transfer. If this bit is cleared, the controller will not check the ACK level sent by the slave. This bit is ignored during RSTART, STOP, END, and READ conditions.
  6. byte\_num: Specifies the length of data (in bytes) to be read or written. It can range from 1 to 255 bytes. This bit is ignored during RSTART, STOP, and END conditions.

Each command sequence is executed starting from command register 0 and terminated by a STOP or an END. Therefore, there must be a STOP or an END command in the eight command registers.

A complete data transfer on the I2C bus should be initiated by a START and terminated by a STOP. The transfer process may be completed using multiple sequences, separated by END commands. Each sequence may differ in the direction of data transfer, clock frequency, slave addresses, data length, etc. This allows efficient use of available peripheral RAM and also achieves more flexible I2C communication.

### 39.4.10 TX/RX RAM Data Storage

Both TX RAM and RX RAM are  $32 \times 8$  bits and can be accessed in FIFO or non-FIFO mode. If [I2C\\_NONFIFO\\_EN](#) bit is cleared, both RAMs are accessed in FIFO mode; if [I2C\\_NONFIFO\\_EN](#) bit is set, both RAMs are accessed in non-FIFO mode.

TX RAM stores data that the I2C controller needs to send. During communication, when the I2C controller needs to send data (except acknowledgment bits), it reads data from TX RAM and sends them sequentially via SDA. When the I2C controller works in master mode, all data must be stored in TX RAM in the order they need to be sent to slaves. The data stored in TX RAM include slave addresses, read/write bits, register addresses (only in dual address mode) and data to be sent. When the I2C controller works in slave mode, TX RAM only stores data to be sent.

TX RAM can be read and written by the CPU. The CPU writes to TX RAM either in FIFO mode or in non-FIFO mode (direct address). In FIFO mode, the CPU writes to TX RAM via the fixed address [I2C\\_DATA\\_REG](#), with addresses for writing in TX RAM incremented automatically by hardware. In non-FIFO mode, the CPU accesses TX RAM directly via address fields ([I2C Base Address](#) + 0x100) ~ ([I2C Base Address](#) + 0x17C). Each byte in TX RAM occupies an entire word in the address space. Therefore, the address of the first byte is [I2C Base](#)

[Address](#) + 0x100, the second byte is [I2C Base Address](#) + 0x104, the third byte is [I2C Base Address](#) + 0x108, and so on. The CPU can only read TX RAM via direct addresses. Bytes written to the TX RAM can be read back by the CPU, via the direct addresses. Addresses for reading TX RAM are the same as addresses for writing TX RAM.

RX RAM stores data the I2C controller receives during communication. When the I2C controller works in slave mode, neither slave addresses sent by the master nor register addresses (only in dual address mode) will be stored in RX RAM. Values of RX RAM can be read by software after I2C communication is completed.

RX RAM can only be read by the CPU. The CPU reads RX RAM either in FIFO mode or in non-FIFO mode (direct address). In FIFO mode, the CPU reads RX RAM via the fixed address [I2C\\_DATA\\_REG](#), with addresses for reading RX RAM incremented automatically by hardware. In non-FIFO mode, the CPU accesses TX RAM directly via address fields ([I2C Base Address](#) + 0x180) ~ ([I2C Base Address](#) + 0x1FC). Each byte in RX RAM occupies an entire word in the address space. Therefore, the address of the first byte is [I2C Base Address](#) + 0x180, the second byte is [I2C Base Address](#) + 0x184, the third byte is [I2C Base Address](#) + 0x188 and so on.

In FIFO mode, the TX RAM of a master may wrap around to send data larger than the FIFO depth. Set [I2C\\_FIFO\\_PRT\\_EN](#). If the size of data to be sent is smaller than [I2C\\_TXFIFO\\_WM\\_THRHD](#) (master), an [I2C\\_TXFIFO\\_WM\\_INT](#) (master) interrupt is generated. After receiving the interrupt, the software continues writing to [I2C\\_DATA\\_REG](#) (master). Please ensure that software writes to or refreshes TX RAM before the master sends data, otherwise it may result in unpredictable consequences.

In FIFO mode, the RX RAM of a slave may also wrap around to receive data larger than the FIFO depth. Set [I2C\\_FIFO\\_PRT\\_EN](#) and clear [I2C\\_RX\\_FULL\\_ACK\\_LEVEL](#). If data already received (to be overwritten) is larger than [I2C\\_RXFIFO\\_WM\\_THRHD](#) (slave), an [I2C\\_RXFIFO\\_WM\\_INT](#) (slave) interrupt is generated. After receiving the interrupt, the software continues reading from [I2C\\_DATA\\_REG](#) (slave).

### 39.4.11 Data Conversion

DATA\_Shifter is used for serial/parallel conversion, converting byte data in TX RAM to an outgoing serial bitstream or an incoming serial bitstream to byte data in RX RAM. [I2C\\_RX\\_LSB\\_FIRST](#) and [I2C\\_TX\\_LSB\\_FIRST](#) can be used to select LSB- or MSB-first storage and transmission of data.

### 39.4.12 Addressing Mode

The ESP32-P4 I2C controller supports 7-bit and 10-bit addressing. 10-bit addressing can be mixed with 7-bit addressing. Besides, the ESP32-P4 I2C controller also supports dual address mode.

Define the slave address as SLV\_ADDR. In 7-bit addressing mode, the slave address is SLV\_ADDR[6:0]; in 10-bit addressing mode, the slave address is SLV\_ADDR[9:0].

In 7-bit addressing mode, the master only needs to send one byte of the address, which comprises SLV\_ADDR[6:0] and a  $R/\overline{W}$  bit. In the 7-bit addressing mode, there is a special case called general call addressing (broadcast). It is enabled by setting [I2C\\_ADDR\\_BROADCASTING\\_EN](#) in a slave. When the slave receives the general call address (0x00) from the master and the  $R/\overline{W}$  bit followed is 0, it responds to the master regardless of its own address.

In 10-bit addressing mode, the master needs to send two bytes of address. The first byte is slave\_addr\_first\_7bits followed by a  $R/\overline{W}$  bit, and slave\_addr\_first\_7bits should be configured as (0x78 | SLV\_ADDR[9:8]). The second byte is slave\_addr\_second\_byte, which should be configured as SLV\_ADDR[7:0].

The slave can enable 10-bit addressing by configuring [I2C\\_ADDR\\_10BIT\\_EN](#). [I2C\\_SLAVE\\_ADDR](#) is used to configure I2C slave address. Specifically, [I2C\\_SLAVE\\_ADDR\[14:7\]](#) should be configured as [SLV\\_ADDR\[7:0\]](#), and [I2C\\_SLAVE\\_ADDR\[6:0\]](#) should be configured as  $(0x78 \mid \text{SLV\_ADDR}[9:8])$ . Since a 10-bit slave address has one more byte than a 7-bit address, `byte_num` of the WRITE command and the number of bytes in the RAM increase by one. Please refer to [Programming Example](#) for detailed descriptions.

When working in slave mode, the I2C controller supports dual address mode, where the first address is the address of an I2C slave, and the second one is the slave's memory address. When using dual address mode, RAM must be accessed in non-FIFO mode. Dual address mode is enabled by setting [I2C\\_FIFO\\_ADDR\\_CFG\\_EN](#). When the slave address received by the slave is inconsistent with the internally configured slave address, the [I2C\\_SLAVE\\_ADDR\\_UNMATCH](#) interrupt will be generated.

### 39.4.13 $R/\overline{W}$ Bit Check in 10-bit Addressing Mode

In 10-bit addressing mode, when [I2C\\_ADDR\\_10BIT\\_RW\\_CHECK\\_EN](#) is set to 1, the I2C controller performs a check on the first byte, which consists of `slave_addr_first_7bits` and a  $R/\overline{W}$  bit. When the  $R/\overline{W}$  bit does not indicate a WRITE operation, i.e., not in line with the I2C protocol, the data transfer ends. If the check feature is not enabled, when the  $R/\overline{W}$  bit does not indicate a WRITE, the data transfer still continues, but transfer failure may occur.

### 39.4.14 To Start the I2C Controller

To start the I2C controller in master mode, after configuring the controller to master mode and command registers, write 1 to [I2C\\_TRANS\\_START](#) in order to let the master start to parse and execute command sequences. The master always executes a command sequence starting from the command register 0 to a STOP or an END. To execute another command sequence starting from command register 0, refresh commands by writing 1 again to [I2C\\_TRANS\\_START](#).

There are two ways to start the I2C controller in slave mode:

- Set [I2C\\_SLV\\_TX\\_AUTO\\_START\\_EN](#), and the slave starts automatic transfer upon an address match;
- Clear [I2C\\_SLV\\_TX\\_AUTO\\_START\\_EN](#), and always set [I2C\\_TRANS\\_START](#) before accepting any transfer.

## 39.5 Functional Differences Between LP\_I2C and I2C

LP\_I2C can be used as a master to communicate with external devices when the main system sleeps. LP\_I2C includes all the functions of the ESP32-P4 I2C<sub>master</sub>, but doesn't include any functions of ESP32-P4 I2C<sub>slave</sub>. It does not contain any registers related to the I2C<sub>slave</sub>. For detailed register list, see [39.8.2 LP\\_I2C Register Summary](#).

The design differences between LP\_I2C and I2C master are as follows:

- The size of TX/RX RAM in LP\_I2C is 16\*8 bit, which means the TX/RX FIFO depth is 16 bytes.
- The clock source of APB\_CLK in LP\_I2C is CLK\_AON\_FAST. The clock source for I2C\_SCLK is configured via [LPPERI\\_LP\\_I2C\\_CLK\\_SEL](#). The corresponding bits are:
  - 0: CLK\_ROOT\_FAST
  - 1: CLK\_XTALD2

– 2: PLL\_F8M\_CLK

Configuring [LPPERI\\_CK\\_EN\\_LP\\_I2C](#) to 1 enables the clock source of I2C\_SCLK. Adjust the timing registers accordingly when the clock frequency changes.

See the programming examples of ESP32-P4 I2C<sub>slave</sub> in [39.6](#) for that of LP\_I2C.

## 39.6 Programming Example

This section provides programming examples for typical communication scenarios. ESP32-P4 has two I2C controllers. For the convenience of description, I2C masters and slaves in all subsequent figures are ESP32-P4 I2C controllers. I2C master is referred to as I2C<sub>master</sub>, and I2C slave is referred to as I2C<sub>slave</sub>.

### 39.6.1 I2C<sub>master</sub> Writes to I2C<sub>slave</sub> with a 7-bit Address in One Command Sequence

#### 39.6.1.1 Introduction

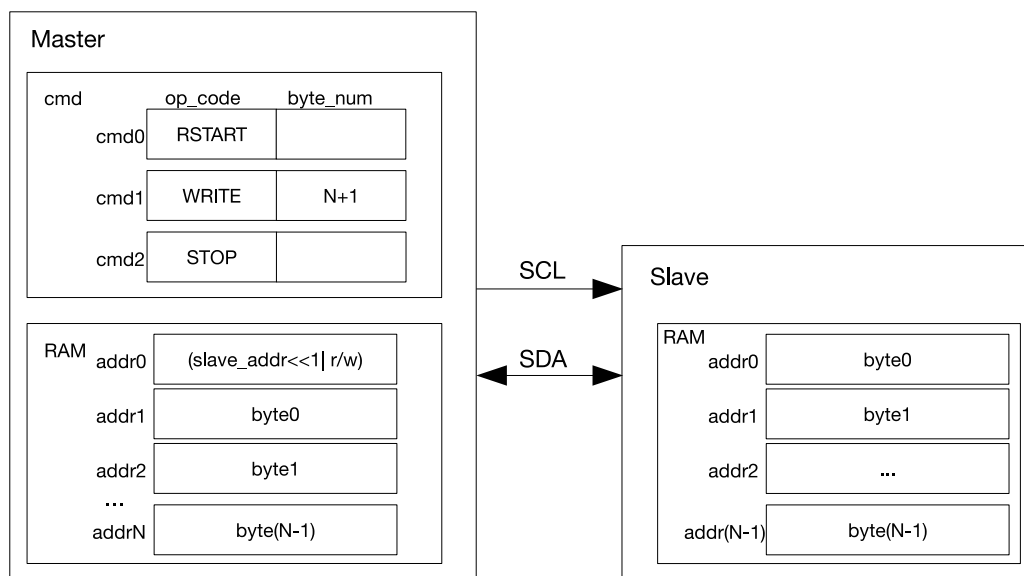


Figure 39.6-1. I2C<sub>master</sub> Writing to I2C<sub>slave</sub> with a 7-bit Address

Figure [39.6-1](#) shows how I2C<sub>master</sub> writes N bytes of data to I2C<sub>slave</sub> registers or RAM using 7-bit addressing. As shown in figure [39.6-1](#), the first byte in the RAM of I2C<sub>master</sub> is a 7-bit I2C<sub>slave</sub> address followed by a  $R/\overline{W}$  bit. When the  $R/\overline{W}$  bit is 0, it indicates a WRITE operation. The remaining bytes are used to store data ready for transfer. The cmd box contains related command sequences.

After the command sequence is configured and data in RAM is ready, I2C<sub>master</sub> enables the controller and initiates data transfer by setting the [I2C\\_TRANS\\_START](#) bit. The controller has four steps to take:

1. Wait for SCL to go high, to avoid SCL being used by other masters or slaves.
2. Execute a RSTART command by sending a START bit.
3. Execute a WRITE command by taking N+1 bytes from the RAM in order and sending them to I2C<sub>slave</sub> in the same order. The first byte is the address of I2C<sub>slave</sub>.



4. Execute a STOP command. Once the I2C<sub>master</sub> transfers a STOP bit, an I2C\_TRANS\_COMPLETE\_INT interrupt is generated.

### 39.6.1.2 Configuration Example

1. Configure the timing parameter registers of I2C<sub>master</sub> and I2C<sub>slave</sub> according to Section 39.4.7.
2. Set I2C\_MS\_MODE (master) to 1, and I2C\_MS\_MODE (slave) to 0.
3. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
4. Configure command registers of I2C<sub>master</sub>.

| Command register      | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|-----------------------|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master) | RSTART  | —         | —       | —            | —        |
| I2C_COMMAND1 (master) | WRITE   | ack_value | ack_exp | 1            | N+1      |
| I2C_COMMAND2 (master) | STOP    | —         | —       | —            | —        |

5. Write the address of I2C<sub>slave</sub> and data to be sent to TX RAM of I2C<sub>master</sub> in either FIFO mode or non-FIFO mode according to Section 39.4.10.
6. Write the address of I2C<sub>slave</sub> to I2C\_SLAVE\_ADDR (slave) in I2C\_SLAVE\_ADDR\_REG (slave) register.
7. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C\_TRANS\_START (master) and I2C\_TRANS\_START (slave) to start transfer.
9. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in I2C\_SLAVE\_ADDR (slave). When ack\_check\_en (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When ack\_check\_en (master) is 0, I2C<sub>master</sub> does not check the ACK value and take I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches ack\_exp (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.
  - Not match: If the received ACK value does not match ack\_exp, I2C<sub>master</sub> generates an I2C\_NACK\_INT (master) interrupt and stops data transfer.
10. I2C<sub>master</sub> sends data, and determines whether to check ACK value according to ack\_check\_en (master).
11. If data to be sent (N) is larger than TX FIFO depth, TX RAM of I2C<sub>master</sub> may wrap around in FIFO mode. For details, please refer to Section 39.4.10.
12. If data to be received (N) is larger than RX FIFO depth, RX RAM of I2C<sub>slave</sub> may wrap around in FIFO mode. For details, please refer to Section 39.4.10.

If data to be received (N) is larger than RX FIFO depth, the other way is to enable clock stretching by setting the I2C\_SLAVE\_SCL\_STRETCH\_EN (slave), and clearing I2C\_RX\_FULL\_ACK\_LEVEL. When RX RAM is full, an I2C\_SLAVE\_STRETCH\_INT (slave) interrupt is generated. In this way, I2C<sub>slave</sub> can hold SCL low, in exchange for more time to read data. After the software has finished reading, you can set I2C\_SLAVE\_STRETCH\_INT\_CLR (slave) to 1 to clear interrupt, and set I2C\_SLAVE\_SCL\_STRETCH\_CLR (slave) to release the SCL line.



13. After data transfer completes, I2C<sub>master</sub> executes the STOP command, and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.

39.6.2 I2C<sub>master</sub> Writes to I2C<sub>slave</sub> with a 10-bit Address in One Command Sequence

39.6.2.1 Introduction

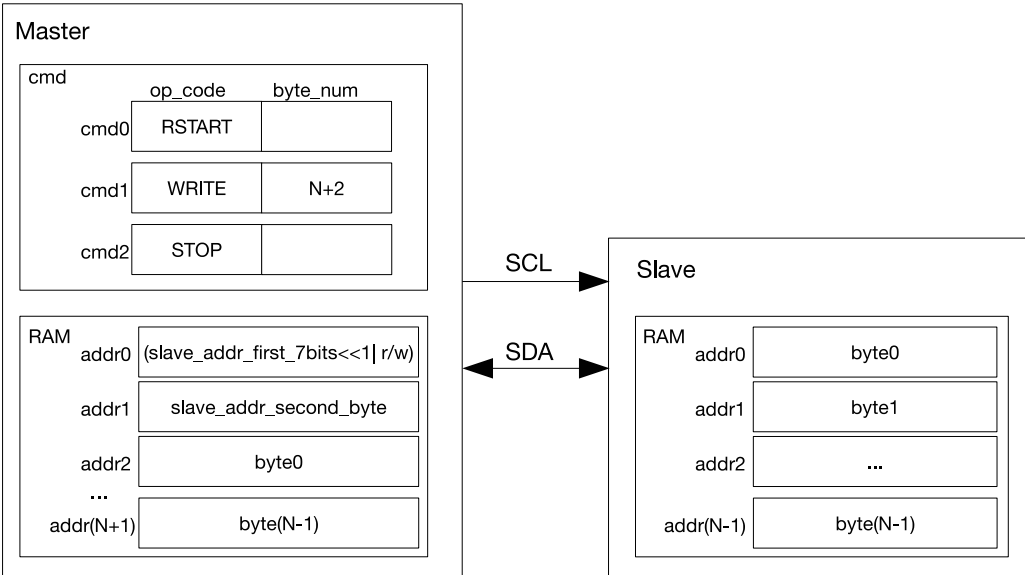


Figure 39.6-2. I2C<sub>master</sub> Writing to a Slave with a 10-bit Address

Figure 39.6-2 shows how I2C<sub>master</sub> writes N bytes of data using 10-bit addressing to an I2C slave. The configuration and transfer process is similar to what is described in 39.6.1, except that a 10-bit I2C<sub>slave</sub> address is formed from two bytes. Since a 10-bit I2C<sub>slave</sub> address has one more byte than a 7-bit I2C<sub>slave</sub> address, byte\_num and length of data in TX RAM increase by 1 accordingly.

39.6.2.2 Configuration Example

1. Set I2C\_MS\_MODE (master) to 1, and I2C\_MS\_MODE (slave) to 0.
2. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
3. Configure command registers of I2C<sub>master</sub>.

| Command registers     | op_code | ack_value | ack_exp | ack_check_er | byte_num |
|-----------------------|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master) | RSTART  | —         | —       | —            | —        |
| I2C_COMMAND1 (master) | WRITE   | ack_value | ack_exp | 1            | N+2      |
| I2C_COMMAND2 (master) | STOP    | —         | —       | —            | —        |

4. Configure I2C\_SLAVE\_ADDR (slave) in I2C\_SLAVE\_ADDR\_REG (slave) as I2C<sub>slave</sub>'s 10-bit address, and set I2C\_ADDR\_10BIT\_EN (slave) to 1 to enable 10-bit addressing.

5. Write the address of I2C<sub>slave</sub> and data to be sent to TX RAM of I2C<sub>master</sub>. The first byte of the address of I2C<sub>slave</sub> comprises ((0x78 | I2C\_SLAVE\_ADDR[9:8])«1) and a  $R/\overline{W}$  bit. The second byte of the address of I2C<sub>slave</sub> is I2C\_SLAVE\_ADDR[7:0]. These two bytes are followed by data to be sent in FIFO or non-FIFO mode.
6. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
7. Write 1 to I2C\_TRANS\_START (master) and I2C\_TRANS\_START (slave) to start transfer.
8. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in I2C\_SLAVE\_ADDR (slave). When ack\_check\_en (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When ack\_check\_en (master) is 0, I2C<sub>master</sub> does not check the ACK value and take I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches ack\_exp (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.
  - Not match: If the received ACK value does not match ack\_exp, I2C<sub>master</sub> generates an I2C\_NACK\_INT (master) interrupt and stops data transfer.
9. I2C<sub>master</sub> sends data, and determines whether to check ACK value according to ack\_check\_en (master).
10. If data to be sent is larger than TX FIFO depth, TX RAM of I2C<sub>master</sub> may wrap around in FIFO mode. For details, please refer to Section 39.4.10.
11. If data to be received is larger than RX FIFO depth, RX RAM of I2C<sub>slave</sub> may wrap around in FIFO mode. For details, please refer to Section 39.4.10.
 

If data to be received is larger than RX FIFO depth, the other way is to enable clock stretching by setting I2C\_SLAVE\_SCL\_STRETCH\_EN (slave), and clearing I2C\_RX\_FULL\_ACK\_LEVEL to 0. When RX RAM is full, an I2C\_SLAVE\_STRETCH\_INT (slave) interrupt is generated. In this way, I2C<sub>slave</sub> can hold SCL low, in exchange for more time to read data. After the software has finished reading, you can set I2C\_SLAVE\_STRETCH\_INT\_CLR (slave) to 1 to clear interrupt, and set I2C\_SLAVE\_SCL\_STRETCH\_CLR (slave) to release the SCL line.
12. After data transfer completes, I2C<sub>master</sub> executes the STOP command, and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.

### 39.6.3 I2C<sub>master</sub> Writes to I2C<sub>slave</sub> with Two 7-bit Addresses in One Command Sequence

### 39.6.3.1 Introduction

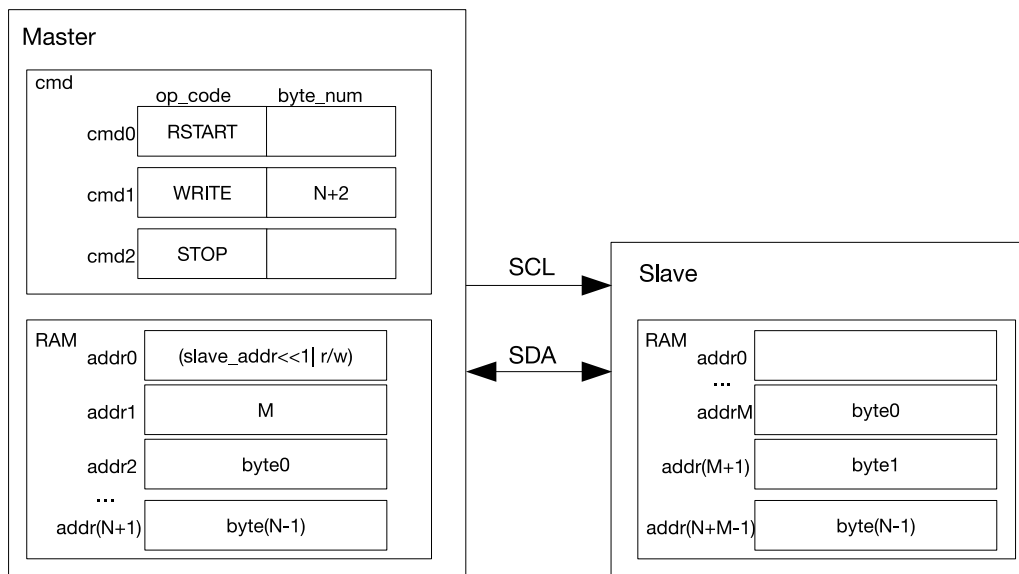


Figure 39.6-3. I2C<sub>master</sub> Writing to I2C<sub>slave</sub> with Two 7-bit Addresses

Figure 39.6-3 shows how I2C<sub>master</sub> writes N bytes of data to I2C<sub>slave</sub> registers or RAM using 7-bit double addressing. The configuration and transfer process is similar to what is described in Section 39.6.1, except that in 7-bit dual address mode I2C<sub>master</sub> sends two 7-bit addresses. The first address is the address of an I2C slave, and the second one is I2C<sub>slave</sub>'s memory address (i.e., addrM in Figure 39.6-3). When using double addressing, RAM must be accessed in non-FIFO mode. The I2C slave puts received byte0 ~ byte (N-1) into its RAM in an order starting from addrM. The RAM is overwritten every 32 bytes.

### 39.6.3.2 Configuration Example

1. Set I2C\_MS\_MODE (master) to 1, and I2C\_MS\_MODE (slave) to 0.
2. Set I2C\_FIFO\_ADDR\_CFG\_EN (slave) to 1 to enable dual address mode.
3. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
4. Configure command registers of I2C<sub>master</sub>.

| Command registers     | op_code | ack_value | ack_exp | ack_check_er | byte_num |
|-----------------------|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master) | RSTART  | —         | —       | —            | —        |
| I2C_COMMAND1 (master) | WRITE   | ack_value | ack_exp | 1            | N+2      |
| I2C_COMMAND2 (master) | STOP    | —         | —       | —            | —        |

5. Write the address of I2C<sub>slave</sub> and data to be sent to TX RAM of I2C<sub>master</sub> in FIFO or non-FIFO mode.
6. Write the address of I2C<sub>slave</sub> to I2C\_SLAVE\_ADDR (slave) in I2C\_SLAVE\_ADDR\_REG (slave) register.
7. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C\_TRANS\_START (master) and I2C\_TRANS\_START (slave) to start transfer.

9. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in [I2C\\_SLAVE\\_ADDR](#) (slave). When `ack_check_en` (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When `ack_check_en` (master) is 0, I2C<sub>master</sub> does not check ACK value and take I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches `ack_exp` (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.
  - Not match: If the received ACK value does not match `ack_exp`, I2C<sub>master</sub> generates an `I2C_NACK_INT` (master) interrupt and stops data transfer.
10. I2C<sub>slave</sub> receives the RX RAM address sent by I2C<sub>master</sub> and adds the offset.
11. I2C<sub>master</sub> sends data, and determines whether to check ACK value according to `ack_check_en` (master).
12. If data to be sent is larger than TX FIFO depth, TX RAM of I2C<sub>master</sub> may wrap around in FIFO mode. For details, please refer to Section [39.4.10](#).
13. If data to be received is larger than RX FIFO depth, you may enable clock stretching by setting [I2C\\_SLAVE\\_SCL\\_STRETCH\\_EN](#) (slave), and clearing [I2C\\_RX\\_FULL\\_ACK\\_LEVEL](#) to 0. When RX RAM is full, an [I2C\\_SLAVE\\_STRETCH\\_INT](#) (slave) interrupt is generated. In this way, I2C<sub>slave</sub> can hold SCL low, in exchange for more time to read data. After the software has finished reading, you can set [I2C\\_SLAVE\\_STRETCH\\_INT\\_CLR](#) (slave) to 1 to clear interrupt, and set [I2C\\_SLAVE\\_SCL\\_STRETCH\\_CLR](#) (slave) to release the SCL line.
14. After data transfer completes, I2C<sub>master</sub> executes the STOP command, and generates an `I2C_TRANS_COMPLETE_INT` (master) interrupt.

#### 39.6.4 I2C<sub>master</sub> Writes to I2C<sub>slave</sub> with a 7-bit Address in Multiple Command Sequences

### 39.6.4.1 Introduction

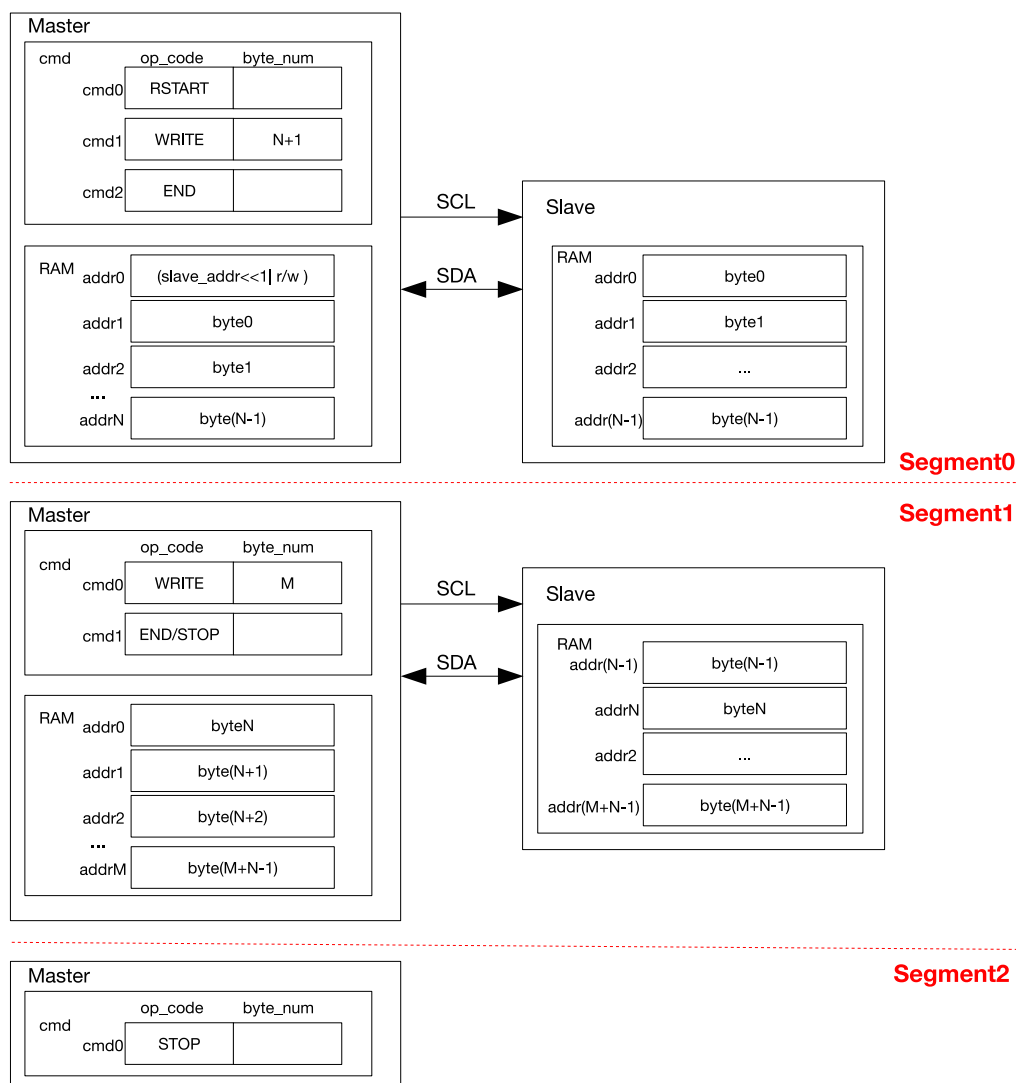


Figure 39.6-4. I2C<sub>master</sub> Writing to I2C<sub>slave</sub> with a 7-bit Address in Multiple Sequences

Given that the I2C Controller RAM holds only the size of TX/RX FIFO depth, when data are too large to be processed, it is advised to transmit them in multiple command sequences. At the end of every command sequence is an END command. When the controller executes this END command, SCL will be pulled low, and the software can refresh command sequence registers and the RAM for the next transfer.

Figure 39.6-4 shows how I2C<sub>master</sub> writes to an I2C slave in two or three segments as an example. For the first segment, the CMD\_Controller registers are configured as shown in Segment0. Once data in I2C<sub>master</sub>'s RAM is ready and I2C\_TRANS\_START is set, I2C<sub>master</sub> initiates data transfer. After executing the END command, I2C<sub>master</sub> turns off the SCL clock and pulls SCL low to reserve the bus. Meanwhile, the controller generates an I2C\_END\_DETECT\_INT interrupt.

For the second segment, after detecting the I2C\_END\_DETECT\_INT interrupt, the software refreshes the CMD\_Controller registers, reloads the RAM, and clears this interrupt, as shown in Segment1. If cmd1 in the second segment is a STOP, then data is transmitted to I2C<sub>slave</sub> in two segments. I2C<sub>master</sub> resumes data transfer after I2C\_TRANS\_START is set, and terminates the transfer by sending a STOP bit.

For the third segment, after the second data transfer finishes and an I2C\_END\_DETECT\_INT is detected, the

CMD\_Controller registers of I2C<sub>master</sub> are configured as shown in Segment2. Once [I2C\\_TRANS\\_START](#) is set, I2C<sub>master</sub> generates a STOP bit and terminates the transfer.

Note that other I2C<sub>master</sub>s will not transact on the bus between two segments. The bus is only released after a STOP command is sent. The I2C controller can be reset by setting [I2C\\_FSM\\_RST](#) field at any time. This field will later be cleared automatically by hardware.

### 39.6.4.2 Configuration Example

1. Set [I2C\\_MS\\_MODE](#) (master) to 1, and [I2C\\_MS\\_MODE](#) (slave) to 0.
2. Write 1 to [I2C\\_CONF\\_UPGATE](#) (master) and [I2C\\_CONF\\_UPGATE](#) (slave) to synchronize registers.
3. Configure command registers of I2C<sub>master</sub>.

| Command registers                     | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|---------------------------------------|---------|-----------|---------|--------------|----------|
| <a href="#">I2C_COMMAND0</a> (master) | RSTART  | —         | —       | —            | —        |
| <a href="#">I2C_COMMAND1</a> (master) | WRITE   | ack_value | ack_exp | 1            | N+1      |
| <a href="#">I2C_COMMAND2</a> (master) | END     | —         | —       | —            | —        |

4. Write the address of I2C<sub>slave</sub> and data to be sent to TX RAM of I2C<sub>master</sub> in either FIFO mode or non-FIFO mode according to Section [39.4.10](#).
5. Write the address of I2C<sub>slave</sub> to [I2C\\_SLAVE\\_ADDR](#) (slave) in [I2C\\_SLAVE\\_ADDR\\_REG](#) (slave) register
6. Write 1 to [I2C\\_CONF\\_UPGATE](#) (master) and [I2C\\_CONF\\_UPGATE](#) (slave) to synchronize registers.
7. Write 1 to [I2C\\_TRANS\\_START](#) (master) and [I2C\\_TRANS\\_START](#) (slave) to start transfer.
8. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in [I2C\\_SLAVE\\_ADDR](#) (slave). When [ack\\_check\\_en](#) (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When [ack\\_check\\_en](#) (master) is 0, I2C<sub>master</sub> does not check ACK value and take I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches [ack\\_exp](#) (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.
  - Not match: If the received ACK value does not match [ack\\_exp](#), I2C<sub>master</sub> generates an [I2C\\_NACK\\_INT](#) (master) interrupt and stops data transfer.
9. I2C<sub>master</sub> sends data, and checks ACK value or not according to [ack\\_check\\_en](#) (master).
10. After the [I2C\\_END\\_DETECT\\_INT](#) (master) interrupt is generated, set [I2C\\_END\\_DETECT\\_INT\\_CLR](#) (master) to 1 to clear this interrupt.
11. Update I2C<sub>master</sub>'s command registers.

| Command registers                     | op_code  | ack_value | ack_exp | ack_check_en | byte_num |
|---------------------------------------|----------|-----------|---------|--------------|----------|
| <a href="#">I2C_COMMAND0</a> (master) | WRITE    | ack_value | ack_exp | 1            | M        |
| <a href="#">I2C_COMMAND1</a> (master) | END/STOP | —         | —       | —            | —        |

- 12. Write M bytes of data to be sent to TX RAM of I2C<sub>master</sub> in FIFO or non-FIFO mode.
- 13. Write 1 to I2C\_TRANS\_START (master) bit to start the transfer and repeat step 9.
- 14. If the command is a STOP, I2C stops the transfer and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.
- 15. If the command is an END, repeat step 10.
- 16. Update I2C<sub>master</sub>'s command registers.

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_er | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND1 (master)                      | STOP    | —         | —       | —            | —        |

- 17. Write 1 to I2C\_TRANS\_START (master) bit to start transfer.
- 18. I2C<sub>master</sub> executes the STOP command and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.

### 39.6.5 I2C<sub>master</sub> Reads I2C<sub>slave</sub> with a 7-bit Address in One Command Sequence

#### 39.6.5.1 Introduction

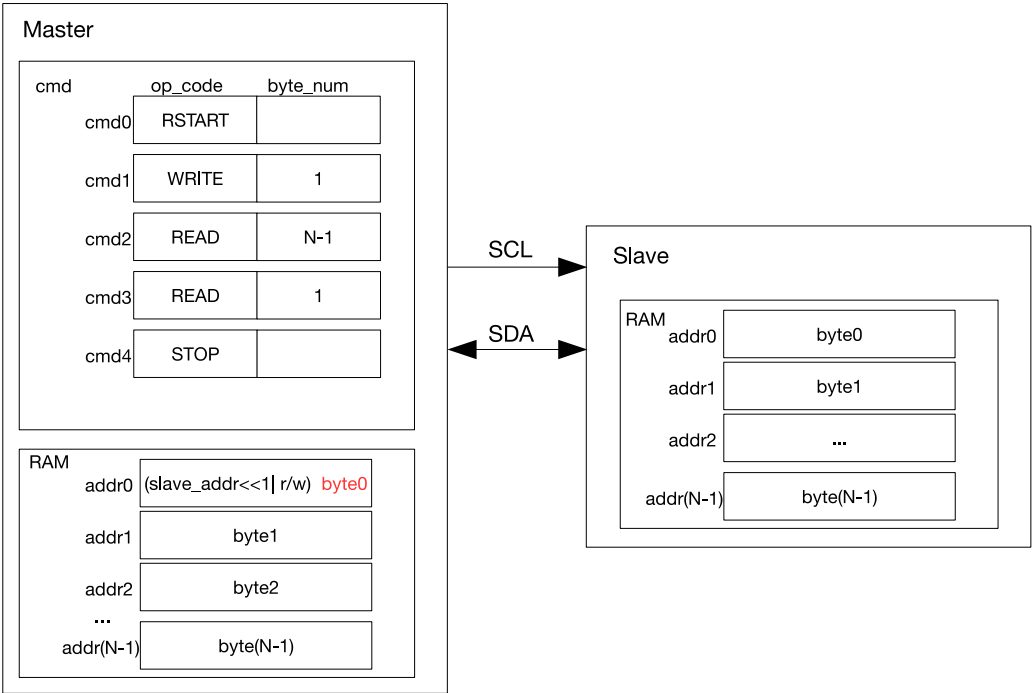


Figure 39.6-5. I2C<sub>master</sub> Reading I2C<sub>slave</sub> with a 7-bit Address

Figure 39.6-5 shows how I2C<sub>master</sub> reads N bytes of data from an I2C slave using 7-bit addressing. cmd1 is a WRITE command, and when this command is executed I2C<sub>master</sub> sends the address of I2C<sub>slave</sub>. The byte sent comprises a 7-bit I2C<sub>slave</sub> address and a  $R/\overline{W}$  bit. When the  $R/\overline{W}$  bit is 1, it indicates a READ operation. If the

address of an I2C slave matches the sent address, this matching slave starts sending data to I2C<sub>master</sub>.

I2C<sub>master</sub> generates acknowledgments according to `ack_value` defined in the READ command upon receiving a byte.

As illustrated in Figure 39.6-5, I2C<sub>master</sub> executes two READ commands: it generates ACKs for (N-1) bytes of data in cmd2, and a NACK for the last byte of data in cmd 3. This configuration may be changed as required.

I2C<sub>master</sub> writes received data into the controller RAM from `addr0`, whose original content (the address of I2C<sub>slave</sub> and a  $R/\overline{W}$  bit) is overwritten by `byte0` marked red in Figure 39.6-5.

### 39.6.5.2 Configuration Example

1. Set `I2C_MS_MODE` (master) to 1, and `I2C_MS_MODE` (slave) to 0.
2. We recommend setting `I2C_SLAVE_SCL_STRETCH_EN` (slave) to 1, so that SCL can be held low for more processing time when I2C<sub>slave</sub> needs to send data. If this bit is not set, the software should write data to be sent to I2C<sub>slave</sub>'s TX RAM before I2C<sub>master</sub> initiates the transfer. The configuration below is applicable to the scenario where `I2C_SLAVE_SCL_STRETCH_EN` (slave) is 1.
3. Write 1 to `I2C_CONF_UPGATE` (master) and `I2C_CONF_UPGATE` (slave) to synchronize registers.
4. Configure command registers of I2C<sub>master</sub>.

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| <code>I2C_COMMAND0</code> (master)         | RSTART  | —         | —       | —            | —        |
| <code>I2C_COMMAND1</code> (master)         | WRITE   | 0         | 0       | 1            | 1        |
| <code>I2C_COMMAND2</code> (master)         | READ    | 0         | 0       | 1            | N-1      |
| <code>I2C_COMMAND3</code> (master)         | READ    | 1         | 0       | 1            | 1        |
| <code>I2C_COMMAND4</code> (master)         | STOP    | —         | —       | —            | —        |

5. Write the address of I2C<sub>slave</sub> to TX RAM of I2C<sub>master</sub> in either FIFO mode or non-FIFO mode according to Section 39.4.10.
6. Write the address of I2C<sub>slave</sub> to `I2C_SLAVE_ADDR` (slave) in `I2C_SLAVE_ADDR_REG` (slave) register.
7. Write 1 to `I2C_CONF_UPGATE` (master) and `I2C_CONF_UPGATE` (slave) to synchronize registers.
8. Write 1 to `I2C_TRANS_START` (master) bit to start I2C<sub>master</sub>'s transfer.
9. Start I2C<sub>slave</sub>'s transfer according to Section 39.4.14.
10. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in `I2C_SLAVE_ADDR` (slave). When `ack_check_en` (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When `ack_check_en` (master) is 0, I2C<sub>master</sub> does not check ACK value and take I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches `ack_exp` (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.



- Not match: If the received ACK value does not match `ack_exp`, `I2Cmaster` generates an `I2C_NACK_INT` (master) interrupt and stops data transfer.
11. After `I2C_SLAVE_STRETCH_INT` (slave) is generated, the `I2C_STRETCH_CAUSE` bit is 0. The address of `I2Cslave` matches the address sent over SDA, and `I2Cslave` needs to send data.
  12. Write data to be sent to TX RAM of `I2Cslave` in either FIFO mode or non-FIFO mode according to Section 39.4.10.
  13. Set `I2C_SLAVE_SCL_STRETCH_CLR` (slave) to 1 to release SCL.
  14. `I2Cslave` sends data, and `I2Cmaster` checks ACK value or not according to `ack_check_en` (master) in the READ command.
  15. If data to be read by `I2Cmaster` is larger than the TX FIFO depth of `I2Cslave`, an `I2C_SLAVE_STRETCH_INT` (slave) interrupt will be generated when TX RAM of `I2Cslave` becomes empty. In this way, `I2Cslave` can hold SCL low, so that software has more time to pad data in TX RAM of `I2Cslave` and read data in RX RAM of `I2Cmaster`. After software has finished reading, you can set `I2C_SLAVE_STRETCH_INT_CLR` (slave) to 1 to clear interrupt, and set `I2C_SLAVE_SCL_STRETCH_CLR` (slave) to release the SCL line.
  16. After `I2Cmaster` has received the last byte of data, set `ack_value` (master) to 1. `I2Cslave` will stop the transfer once receiving the `I2C_NACK_INT` interrupt.
  17. After data transfer completes, `I2Cmaster` executes the STOP command, and generates an `I2C_TRANS_COMPLETE_INT` (master) interrupt.

### 39.6.6 `I2Cmaster` Reads `I2Cslave` with a 10-bit Address in One Command Sequence

39.6.6.1 Introduction

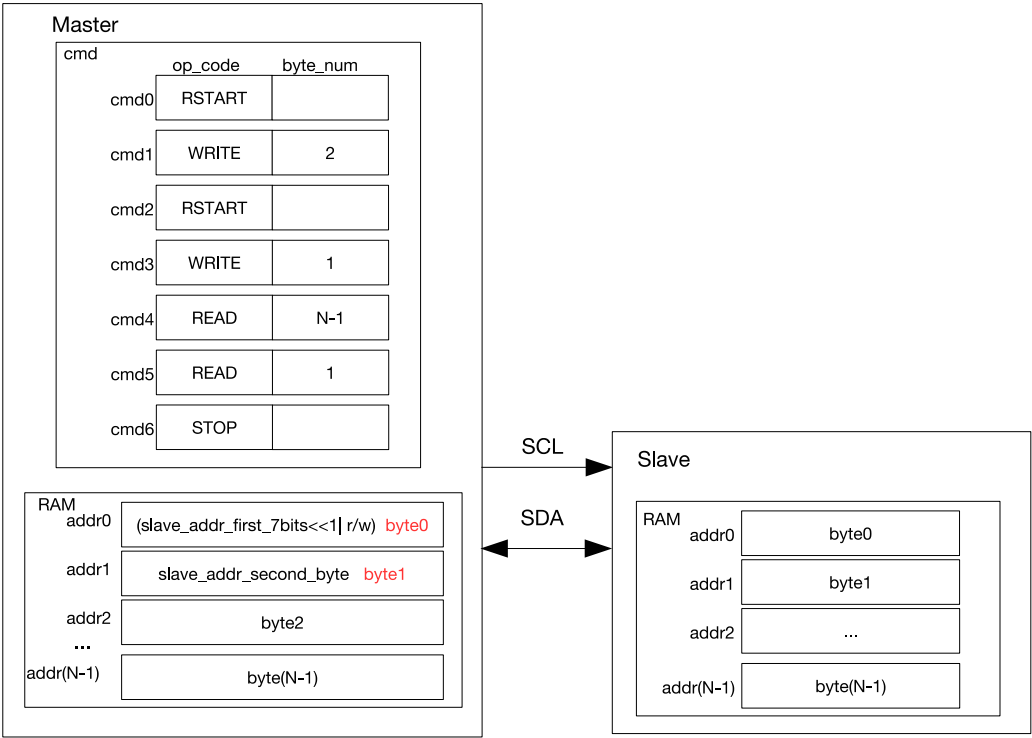


Figure 39.6-6. I2C<sub>master</sub> Reading I2C<sub>slave</sub> with a 10-bit Address

Figure 39.6-6 shows how I2C<sub>master</sub> reads data from an I2C slave using 10-bit addressing. Unlike 7-bit addressing, in 10-bit addressing the WRITE command of the I2C<sub>master</sub> is formed from two bytes, and correspondingly TX RAM of this master stores a 10-bit address of two bytes. The  $R/\overline{W}$  bit in the first byte is 0, which indicates a WRITE operation. After a RSTART condition, I2C<sub>master</sub> sends the first byte of address again to read data from I2C<sub>slave</sub>, but the  $R/\overline{W}$  bit is 1, which indicates a READ operation. The two address bytes can be configured as described in Section 39.6.2.

39.6.6.2 Configuration Example

1. Set `I2C_MS_MODE` (master) to 1, and `I2C_MS_MODE` (slave) to 0.
2. We recommend setting `I2C_SLAVE_SCL_STRETCH_EN` (slave) to 1, so that SCL can be held low for more processing time when I2C<sub>slave</sub> needs to send data. If this bit is not set, the software should write data to be sent to I2C<sub>slave</sub>'s TX RAM before I2C<sub>master</sub> initiates the transfer. The configuration below is applicable to a scenario where `I2C_SLAVE_SCL_STRETCH_EN` (slave) is 1.
3. Write 1 to `I2C_CONF_UPGATE` (master) and `I2C_CONF_UPGATE` (slave) to synchronize registers.
4. Configure command registers of I2C<sub>master</sub>.

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_er | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master)                      | RSTART  | —         | —       | —            | —        |
| I2C_COMMAND1 (master)                      | WRITE   | 0         | 0       | 1            | 2        |

|                                       |        |   |   |   |     |
|---------------------------------------|--------|---|---|---|-----|
| <a href="#">I2C_COMMAND2</a> (master) | RSTART | — | — | — | —   |
| <a href="#">I2C_COMMAND3</a> (master) | WRITE  | 0 | 0 | 1 | 1   |
| <a href="#">I2C_COMMAND4</a> (master) | READ   | 0 | 0 | 1 | N-1 |
| <a href="#">I2C_COMMAND5</a> (master) | READ   | 1 | 0 | 1 | 1   |
| <a href="#">I2C_COMMAND6</a> (master) | STOP   | — | — | — | —   |

- Configure [I2C\\_SLAVE\\_ADDR](#) (slave) in [I2C\\_SLAVE\\_ADDR\\_REG](#) (slave) as  $I2C_{\text{slave}}$ 's 10-bit address, and set [I2C\\_ADDR\\_10BIT\\_EN](#) (slave) to 1 to enable 10-bit addressing.
- Write the address of  $I2C_{\text{slave}}$  and data to be sent to TX RAM of  $I2C_{\text{master}}$  in either FIFO or non-FIFO mode. The first byte of address comprises  $((0x78 | I2C\_SLAVE\_ADDR[9:8]) \ll 1)$  and a  $R/\overline{W}$  bit, which is 1 and indicates a WRITE operation. The second byte of address is [I2C\\_SLAVE\\_ADDR](#)[7:0]. The third byte is  $((0x78 | I2C\_SLAVE\_ADDR[9:8]) \ll 1)$  and a  $R/\overline{W}$  bit, which is 1 and indicates a READ operation.
- Write 1 to [I2C\\_CONF\\_UPGATE](#) (master) and [I2C\\_CONF\\_UPGATE](#) (slave) to synchronize registers.
- Write 1 to [I2C\\_TRANS\\_START](#) (master) to start  $I2C_{\text{master}}$ 's transfer.
- Start  $I2C_{\text{slave}}$ 's transfer according to Section 39.4.14.
- $I2C_{\text{slave}}$  compares the slave address sent by  $I2C_{\text{master}}$  with its own address in [I2C\\_SLAVE\\_ADDR](#) (slave). When [ack\\_check\\_en](#) (master) in  $I2C_{\text{master}}$ 's WRITE command is 1,  $I2C_{\text{master}}$  checks ACK value each time it sends a byte. When [ack\\_check\\_en](#) (master) is 0,  $I2C_{\text{master}}$  does not check ACK value and take  $I2C_{\text{slave}}$  as a matching slave by default.
  - Match: If the received ACK value matches [ack\\_exp](#) (master) (the expected ACK value),  $I2C_{\text{master}}$  continues data transfer.
  - Not match: If the received ACK value does not match [ack\\_exp](#),  $I2C_{\text{master}}$  generates an [I2C\\_NACK\\_INT](#) (master) interrupt and stops data transfer.
- $I2C_{\text{master}}$  sends a RSTART and the third byte in TX RAM, which is  $((0x78 | I2C\_SLAVE\_ADDR[9:8]) \ll 1)$  and a  $R/\overline{W}$  bit that indicates READ.
- $I2C_{\text{slave}}$  repeats step 10. If its address matches the address sent by  $I2C_{\text{master}}$ ,  $I2C_{\text{slave}}$  proceed on to the next steps.
- After [I2C\\_SLAVE\\_STRETCH\\_INT](#) (slave) is generated, the [I2C\\_STRETCH\\_CAUSE](#) bit is 0. The address of  $I2C_{\text{slave}}$  matches the address sent over SDA, and  $I2C_{\text{slave}}$  needs to send data.
- Write data to be sent to TX RAM of  $I2C_{\text{slave}}$  in either FIFO mode or non-FIFO mode according to Section 39.4.10.
- Set [I2C\\_SLAVE\\_SCL\\_STRETCH\\_CLR](#) (slave) to 1 to release SCL.
- $I2C_{\text{slave}}$  sends data, and  $I2C_{\text{master}}$  checks ACK value or not according to [ack\\_check\\_en](#) (master) in the READ command.

17. If data to be read by I2C<sub>master</sub> is larger than the TX FIFO depth of I2C<sub>slave</sub>, an [I2C\\_SLAVE\\_STRETCH\\_INT](#) (slave) interrupt will be generated when TX RAM of I2C<sub>slave</sub> becomes empty. In this way, I2C<sub>slave</sub> can hold SCL low, so that software has more time to pad data in TX RAM of I2C<sub>slave</sub> and read data in RX RAM of I2C<sub>master</sub>. After the software has finished reading, you can set [I2C\\_SLAVE\\_STRETCH\\_INT\\_CLR](#) (slave) to 1 to clear interrupt, and set [I2C\\_SLAVE\\_SCL\\_STRETCH\\_CLR](#) (slave) to release the SCL line.
18. After I2C<sub>master</sub> has received the last byte of data, set ack\_value (master) to 1. I2C<sub>slave</sub> will stop transfer once receiving the I2C\_NACK\_INT interrupt.
19. After data transfer completes, I2C<sub>master</sub> executes the STOP command, and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.

## 39.6.7 I2C<sub>master</sub> Reads I2C<sub>slave</sub> with Two 7-bit Addresses in One Command Sequence

### 39.6.7.1 Introduction

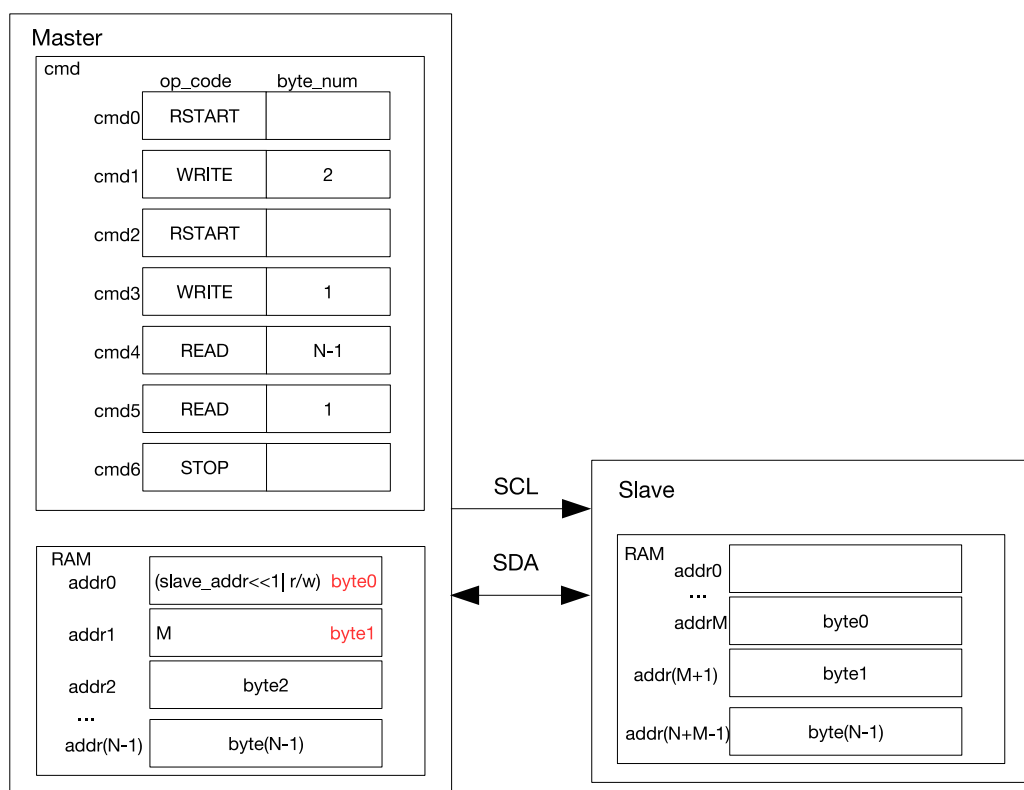


Figure 39.6-7. I2C<sub>master</sub> Reading N Bytes of Data from addrM of I2C<sub>slave</sub> with a 7-bit Address

Figure 39.6-7 shows how I2C<sub>master</sub> reads data from specified addresses in an I2C slave. I2C<sub>master</sub> sends two bytes of addresses: the first byte is a 7-bit I2C<sub>slave</sub> address followed by a  $R/\overline{W}$  bit, which is 0 and indicates a WRITE; the second byte is I2C<sub>slave</sub>'s memory address. After a RSTART condition, I2C<sub>master</sub> sends the first byte of address again, but the  $R/\overline{W}$  bit is 1 which indicates a READ. Then, I2C<sub>master</sub> reads data starting from addrM.

### 39.6.7.2 Configuration Example

1. Set `I2C_MS_MODE` (master) to 1, and `I2C_MS_MODE` (slave) to 0.
2. We recommend setting `I2C_SLAVE_SCL_STRETCH_EN` (slave) to 1, so that SCL can be held low for more processing time when `I2Cslave` needs to send data. If this bit is not set, the software should write data to be sent to `I2Cslave`'s TX RAM before `I2Cmaster` initiates the transfer. The configuration below is applicable to the scenario where `I2C_SLAVE_SCL_STRETCH_EN` (slave) is 1.
3. Set `I2C_FIFO_ADDR_CFG_EN` (slave) to 1 to enable dual address mode.
4. Write 1 to `I2C_CONF_UPGATE` (master) and `I2C_CONF_UPGATE` (slave) to synchronize registers.
5. Configure command registers of `I2Cmaster`.

| Command registers of <code>I2C<sub>master</sub></code> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| <code>I2C_COMMAND0</code> (master)                     | RSTART  | —         | —       | —            | —        |
| <code>I2C_COMMAND1</code> (master)                     | WRITE   | 0         | 0       | 1            | 2        |
| <code>I2C_COMMAND2</code> (master)                     | RSTART  | —         | —       | —            | —        |
| <code>I2C_COMMAND3</code> (master)                     | WRITE   | 0         | 0       | 1            | 1        |
| <code>I2C_COMMAND4</code> (master)                     | READ    | 0         | 0       | 1            | N-1      |
| <code>I2C_COMMAND5</code> (master)                     | READ    | 1         | 0       | 1            | 1        |
| <code>I2C_COMMAND6</code> (master)                     | STOP    | —         | —       | —            | —        |

6. Configure `I2C_SLAVE_ADDR` (slave) in `I2C_SLAVE_ADDR_REG` (slave) register as `I2Cslave`'s 7-bit address, and set `I2C_ADDR_10BIT_EN` (slave) to 0 to enable 7-bit addressing.
7. Write the address of `I2Cslave` and data to be sent to TX RAM of `I2Cmaster` in either FIFO or non-FIFO mode according to Section 39.4.10. The first byte of address comprises ( `I2C_SLAVE_ADDR[6:0]` )«1) and a  $R/\overline{W}$  bit, which is 0 and indicates a WRITE. The second byte of the address is memory address M of `I2Cslave`. The third byte is ( `I2C_SLAVE_ADDR[6:0]` )«1) and a  $R/\overline{W}$  bit, which is 1 and indicates a READ.
8. Write 1 to `I2C_CONF_UPGATE` (master) and `I2C_CONF_UPGATE` (slave) to synchronize registers.
9. Write 1 to `I2C_TRANS_START` (master) to start `I2Cmaster`'s transfer.
10. Start `I2Cslave`'s transfer according to Section 39.4.14.
11. `I2Cslave` compares the slave address sent by `I2Cmaster` with its own address in `I2C_SLAVE_ADDR` (slave). When `ack_check_en` (master) in `I2Cmaster`'s WRITE command is 1, `I2Cmaster` checks ACK value each time it sends a byte. When `ack_check_en` (master) is 0, `I2Cmaster` does not check ACK value and takes `I2Cslave` as a matching slave by default.
  - Match: If the received ACK value matches `ack_exp` (master) (the expected ACK value), `I2Cmaster` continues data transfer.

- Not match: If the received ACK value does not match `ack_exp`, `I2C_master` generates an `I2C_NACK_INT` (master) interrupt and stops data transfer.
12. `I2C_slave` receives memory address sent by `I2C_master` and adds the offset.
  13. `I2C_master` sends a RSTART and the third byte in TX RAM, which is  $((0x78 \mid I2C\_SLAVE\_ADDR[9:8]) \ll 1)$  and a R bit.
  14. `I2C_slave` repeats step 11. If its address matches the address sent by `I2C_master`, `I2C_slave` proceed on to the next steps.
  15. After `I2C_SLAVE_STRETCH_INT` (slave) is generated, the `I2C_STRETCH_CAUSE` bit is 0. The address of `I2C_slave` matches the address sent over SDA, and `I2C_slave` needs to send data.
  16. Write data to be sent to TX RAM of `I2C_slave` in either FIFO mode or non-FIFO mode according to Section 39.4.10.
  17. Set `I2C_SLAVE_SCL_STRETCH_CLR` (slave) to 1 to release SCL.
  18. `I2C_slave` sends data, and `I2C_master` checks ACK value or not according to `ack_check_en` (master) in the READ command.
  19. If data to be read by `I2C_master` is larger than the TX FIFO depth of `I2C_slave`, an `I2C_SLAVE_STRETCH_INT` (slave) interrupt will be generated when TX RAM of `I2C_slave` becomes empty. In this way, `I2C_slave` can hold SCL low, so that software has more time to pad data in TX RAM of `I2C_slave` and read data in RX RAM of `I2C_master`. After software has finished reading, you can set `I2C_SLAVE_STRETCH_INT_CLR` (slave) to 1 to clear interrupt, and set `I2C_SLAVE_SCL_STRETCH_CLR` (slave) to release the SCL line.
  20. After `I2C_master` has received the last byte of data, set `ack_value` (master) to 1. `I2C_slave` will stop transfer once receiving the `I2C_NACK_INT` interrupt.
  21. After data transfer completes, `I2C_master` executes the STOP command, and generates an `I2C_TRANS_COMPLETE_INT` (master) interrupt.

### 39.6.8 `I2C_master` Reads `I2C_slave` with a 7-bit Address in Multiple Command Sequences

## 39.6.8.1 Introduction

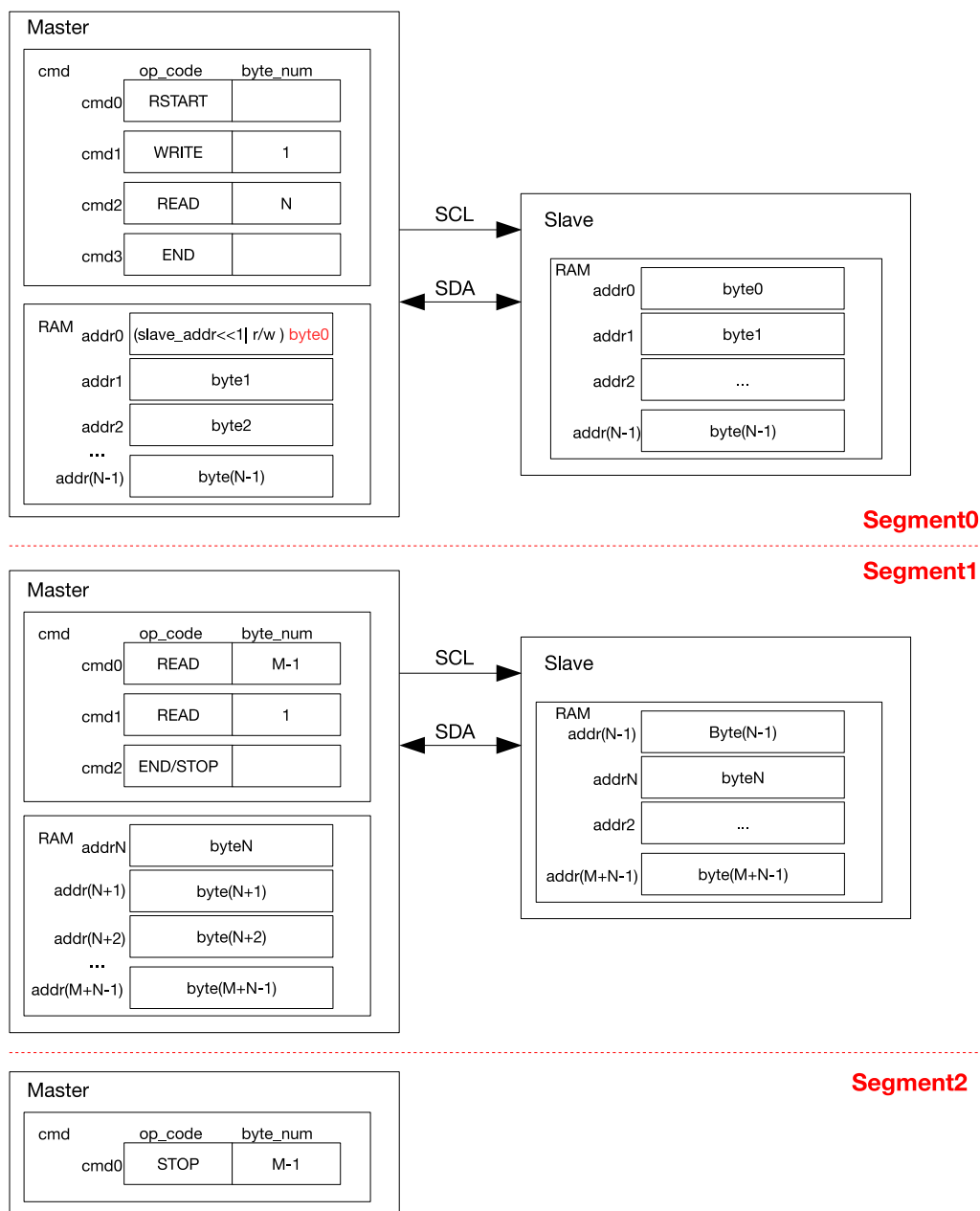
Figure 39.6-8. I2C<sub>master</sub> Reading I2C<sub>slave</sub> with a 7-bit Address in Segments

Figure 39.6-8 shows how I2C<sub>master</sub> reads (N+M) bytes of data from an I2C slave in two/three segments separated by END commands. Configuration procedures are described as follows:

1. The procedures for Segment0 is similar to 39.6-5, except that the last command is an END.
2. Prepare data in the TX RAM of I2C<sub>slave</sub>, and set I2C\_TRANS\_START to start data transfer. After executing the END command, I2C<sub>master</sub> refreshes command registers and the RAM as shown in Segment1, and clears the corresponding I2C\_END\_DETECT\_INT interrupt. If cmd2 in Segment1 is a STOP, then data is read from I2C<sub>slave</sub> in two segments. I2C<sub>master</sub> resumes data transfer by setting I2C\_TRANS\_START and terminates the transfer by sending a STOP bit.
3. If cmd2 in Segment1 is an END, then data is read from I2C<sub>slave</sub> in three segments. After the second data

transfer finishes and an I2C\_END\_DETECT\_INT interrupt is detected, the cmd box is configured as shown in Segment2. Once I2C\_TRANS\_START is set, I2C<sub>master</sub> terminates the transfer by sending a STOP bit.

### 39.6.8.2 Configuration Example

1. Set I2C\_MS\_MODE (master) to 1, and I2C\_MS\_MODE (slave) to 0.
2. We recommend setting I2C\_SLAVE\_SCL\_STRETCH\_EN (slave) to 1, so that SCL can be held low for more processing time when I2C<sub>slave</sub> needs to send data. If this bit is not set, the software should write data to be sent to I2C<sub>slave</sub>'s TX RAM before I2C<sub>master</sub> initiates the transfer. The configuration below is applicable to a scenario where I2C\_SLAVE\_SCL\_STRETCH\_EN (slave) is 1.
3. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
4. Configure command registers of I2C<sub>master</sub>.

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master)                      | RSTART  | —         | —       | —            | —        |
| I2C_COMMAND1 (master)                      | WRITE   | 0         | 0       | 1            | 1        |
| I2C_COMMAND2 (master)                      | READ    | 0         | 0       | 1            | N        |
| I2C_COMMAND3 (master)                      | END     | —         | —       | —            | —        |

5. Write the address of I2C<sub>slave</sub> to TX RAM of I2C<sub>master</sub> in FIFO or non-FIFO mode.
6. Write the address of I2C<sub>slave</sub> to I2C\_SLAVE\_ADDR (slave) in I2C\_SLAVE\_ADDR\_REG (slave) register.
7. Write 1 to I2C\_CONF\_UPGATE (master) and I2C\_CONF\_UPGATE (slave) to synchronize registers.
8. Write 1 to I2C\_TRANS\_START (master) to start I2C<sub>master</sub>'s transfer.
9. Start I2C<sub>slave</sub>'s transfer according to Section 39.4.14.
10. I2C<sub>slave</sub> compares the slave address sent by I2C<sub>master</sub> with its own address in I2C\_SLAVE\_ADDR (slave). When ack\_check\_en (master) in I2C<sub>master</sub>'s WRITE command is 1, I2C<sub>master</sub> checks ACK value each time it sends a byte. When ack\_check\_en (master) is 0, I2C<sub>master</sub> does not check the ACK value and takes I2C<sub>slave</sub> as a matching slave by default.
  - Match: If the received ACK value matches ack\_exp (master) (the expected ACK value), I2C<sub>master</sub> continues data transfer.
  - Not match: If the received ACK value does not match ack\_exp, I2C<sub>master</sub> generates an I2C\_NACK\_INT (master) interrupt and stops data transfer.
11. After I2C\_SLAVE\_STRETCH\_INT (slave) is generated, the I2C\_STRETCH\_CAUSE bit is 0. The address of I2C<sub>slave</sub> matches the address sent over SDA, and I2C<sub>slave</sub> needs to send data.
12. Write data to be sent to TX RAM of I2C<sub>slave</sub> in either FIFO mode or non-FIFO mode according to Section 39.4.10.
13. Set I2C\_SLAVE\_SCL\_STRETCH\_CLR (slave) to 1 to release SCL.



14. I2C<sub>slave</sub> sends data, and I2C<sub>master</sub> checks ACK value or not according to ack\_check\_en (master) in the READ command.
15. If data to be read by I2C<sub>master</sub> in one READ command (N or M) is larger than the TX FIFO depth of I2C<sub>slave</sub>, an I2C\_SLAVE\_STRETCH\_INT (slave) interrupt will be generated when TX RAM of I2C<sub>slave</sub> becomes empty. In this way, I2C<sub>slave</sub> can hold SCL low so that software has more time to pad data in TX RAM of I2C<sub>slave</sub> and read data in RX RAM of I2C<sub>master</sub>. After the software has finished reading, you can set I2C\_SLAVE\_STRETCH\_INT\_CLR (slave) to 1 to clear interrupt, and set I2C\_SLAVE\_SCL\_STRETCH\_CLR (slave) to release the SCL line.
16. Once finishing reading data in the first READ command, I2C<sub>master</sub> executes the END command and triggers an I2C\_END\_DETECT\_INT (master) interrupt, which is cleared by setting I2C\_END\_DETECT\_INT\_CLR (master) to 1.
17. Update I2C<sub>master</sub>'s command registers using one of the following two methods:

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master)                      | READ    | ack_value | ack_exp | 1            | M        |
| I2C_COMMAND1 (master)                      | END     | —         | —       | —            | —        |

Or

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND0 (master)                      | READ    | 0         | 0       | 1            | M-1      |
| I2C_COMMAND0 (master)                      | READ    | 1         | 0       | 1            | 1        |
| I2C_COMMAND1 (master)                      | STOP    | —         | —       | —            | —        |

18. Write M bytes of data to be sent to TX RAM of I2C<sub>slave</sub>. If M is larger than the TX FIFO depth, then repeat step 12 in FIFO or non-FIFO mode.
19. Write 1 to I2C\_TRANS\_START (master) bit to start the transfer and repeat step 14.
20. If the last command is a STOP, then set ack\_value (master) to 1 after I2C<sub>master</sub> has received the last byte of data. I2C<sub>slave</sub> stops transfer upon the I2C\_NACK\_INT interrupt. I2C<sub>master</sub> executes the STOP command to stop the transfer and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.
21. If the last command is an END, then repeat step 16 and proceed on to the next steps.
22. Update I2C<sub>master</sub>'s command registers.

| Command registers of I2C <sub>master</sub> | op_code | ack_value | ack_exp | ack_check_en | byte_num |
|--|---------|-----------|---------|--------------|----------|
| I2C_COMMAND1 (master)                      | STOP    | —         | —       | —            | —        |

23. Write 1 to I2C\_TRANS\_START (master) bit to start transfer.

24. I2C<sub>master</sub> executes the STOP command to stop transfer, and generates an I2C\_TRANS\_COMPLETE\_INT (master) interrupt.

## 39.7 Interrupts

ESP32-P4's I2C<sub>n</sub> can generate the I2C<sub>n</sub>\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#). There are several internal interrupt sources from I2C<sub>n</sub> that can generate the above interrupt signal(s) as follows:

- I2C\_SLAVE\_STRETCH\_INT: Triggered when one of the four stretching events occurs in slave mode.
- I2C\_DET\_START\_INT: Triggered when the master or the slave detects a START signal.
- I2C\_SCL\_MAIN\_ST\_TO\_INT: Triggered when the main state machine SCL\_MAIN\_FSM remains unchanged for over [I2C\\_SCL\\_MAIN\\_ST\\_TO\\_I2C\[23:0\]](#) clock cycles.
- I2C\_SCL\_ST\_TO\_INT: Triggered when the state machine SCL\_FSM remains unchanged for over [I2C\\_SCL\\_ST\\_TO\\_I2C\[23:0\]](#) clock cycles.
- I2C\_RXFIFO\_UDF\_INT: Triggered when the I2C controller reads RX FIFO via the APB bus, but RX FIFO is empty.
- I2C\_TXFIFO\_OVF\_INT: Triggered when the I2C controller writes TX FIFO via the APB bus, but TX FIFO is full.
- I2C\_NACK\_INT: Triggered when the ACK value received by the master is not as expected, or when the ACK value received by the slave is 1.
- I2C\_TRANS\_START\_INT: Triggered when the I2C controller sends a START bit.
- I2C\_TIME\_OUT\_INT: Triggered when SCL stays high or low for more than  $2^{I2C\_TIME\_OUT\_VALUE}$  clock cycles during data transfer.
- I2C\_TRANS\_COMPLETE\_INT: Triggered when the I2C controller detects a STOP bit.
- I2C\_MST\_TXFIFO\_UDF\_INT: Triggered when TX FIFO of the master underflows.
- I2C\_ARBITRATION\_LOST\_INT: Triggered when the SDA's output value does not match its input value while the master's SCL is high.
- I2C\_BYTE\_TRANS\_DONE\_INT: Triggered when the I2C controller sends or receives a byte.
- I2C\_END\_DETECT\_INT: Triggered when op\_code of the master indicates an END command and an END condition is detected.
- I2C\_RXFIFO\_OVF\_INT: Triggered when RX FIFO of the I2C controller overflows.
- I2C\_TXFIFO\_WM\_INT: I2C TX FIFO watermark interrupt. Triggered when [I2C\\_FIFO\\_PRT\\_EN](#) is 1 and the pointers of TX FIFO are less than [I2C\\_TXFIFO\\_WM\\_THRHD\[4:0\]](#).
- I2C\_RXFIFO\_WM\_INT: I2C RX FIFO watermark interrupt. Triggered when [I2C\\_FIFO\\_PRT\\_EN](#) is 1 and the pointers of RX FIFO are greater than [I2C\\_RXFIFO\\_WM\\_THRHD\[4:0\]](#).
- I2C\_SLAVE\_ADDR\_UNMATCH\_INT: Triggered when the received slave address is inconsistent with the internally configured slave address in slave mode.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [39.8.1 I2C Register Summary](#).

## 39.8 Register Summary

### 39.8.1 I2C Register Summary

The addresses in this section are relative to the I2C Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description  | Address | Access   |
|--|--|---------|----------|
| <b>Timing registers</b>                      |  |         |          |
| <a href="#">I2C_SCL_LOW_PERIOD_REG</a>       | Configures the low level width of the SCL Clock  | 0x0000  | R/W      |
| <a href="#">I2C_SDA_HOLD_REG</a>             | Configures the hold time after a negative SCL edge   | 0x0030  | R/W      |
| <a href="#">I2C_SDA_SAMPLE_REG</a>           | Configures the sample time after a positive SCL edge   | 0x0034  | R/W      |
| <a href="#">I2C_SCL_HIGH_PERIOD_REG</a>      | Configures the high level width of SCL   | 0x0038  | R/W      |
| <a href="#">I2C_SCL_START_HOLD_REG</a>       | Configures the delay between the SDA and SCL negative edge for a start condition                         | 0x0040  | R/W      |
| <a href="#">I2C_SCL_RSTART_SETUP_REG</a>     | Configures the delay between the positive edge of SCL and the negative edge of SDA                       | 0x0044  | R/W      |
| <a href="#">I2C_SCL_STOP_HOLD_REG</a>        | Configures the delay after the SCL clock edge for a stop condition                                       | 0x0048  | R/W      |
| <a href="#">I2C_SCL_STOP_SETUP_REG</a>       | Configures the delay between the SDA and SCL rising edge for a stop condition Measurement unit: i2c_sclk | 0x004C  | R/W      |
| <a href="#">I2C_SCL_ST_TIME_OUT_REG</a>      | SCL status time out register   | 0x0078  | R/W      |
| <a href="#">I2C_SCL_MAIN_ST_TIME_OUT_REG</a> | SCL main status time out register  | 0x007C  | R/W      |
| <b>Configuration registers</b>               |  |         |          |
| <a href="#">I2C_CTR_REG</a>                  | Transmission setting   | 0x0004  | varies   |
| <a href="#">I2C_TO_REG</a>                   | Setting time out control for receiving data  | 0x000C  | R/W      |
| <a href="#">I2C_SLAVE_ADDR_REG</a>           | Local slave address setting  | 0x0010  | R/W      |
| <a href="#">I2C_FIFO_CONF_REG</a>            | FIFO configuration register  | 0x0018  | R/W      |
| <a href="#">I2C_FILTER_CFG_REG</a>           | SCL and SDA filter configuration register  | 0x0050  | R/W      |
| <a href="#">I2C_SCL_SP_CONF_REG</a>          | Power configuration register   | 0x0080  | varies   |
| <a href="#">I2C_SCL_STRETCH_CONF_REG</a>     | Set SCL stretch of I2C slave   | 0x0084  | varies   |
| <b>Status registers</b>                      |  |         |          |
| <a href="#">I2C_SR_REG</a>                   | Describe I2C work status   | 0x0008  | RO       |
| <a href="#">I2C_FIFO_ST_REG</a>              | FIFO status register   | 0x0014  | RO       |
| <a href="#">I2C_DATA_REG</a>                 | Rx FIFO read data  | 0x001C  | HRO      |
| <b>Interrupt registers</b>                   |  |         |          |
| <a href="#">I2C_INT_RAW_REG</a>              | Raw interrupt status   | 0x0020  | R/SS/WTC |
| <a href="#">I2C_INT_CLR_REG</a>              | Interrupt clear bits   | 0x0024  | WT       |
| <a href="#">I2C_INT_ENA_REG</a>              | Interrupt enable bits  | 0x0028  | R/W      |

| Name                                      | Description                                 | Address | Access |
|---|---|---------|--------|
| <a href="#">I2C_INT_STATUS_REG</a>        | Status of captured I2C communication events | 0x002C  | RO     |
| <b>Command registers</b>                  |   |         |        |
| <a href="#">I2C_COMDO_REG</a>             | I2C command register 0                      | 0x0058  | varies |
| <a href="#">I2C_COMD1_REG</a>             | I2C command register 1                      | 0x005C  | varies |
| <a href="#">I2C_COMD2_REG</a>             | I2C command register 2                      | 0x0060  | varies |
| <a href="#">I2C_COMD3_REG</a>             | I2C command register 3                      | 0x0064  | varies |
| <a href="#">I2C_COMD4_REG</a>             | I2C command register 4                      | 0x0068  | varies |
| <a href="#">I2C_COMD5_REG</a>             | I2C command register 5                      | 0x006C  | varies |
| <a href="#">I2C_COMD6_REG</a>             | I2C command register 6                      | 0x0070  | varies |
| <a href="#">I2C_COMD7_REG</a>             | I2C command register 7                      | 0x0074  | varies |
| <b>Version register</b>                   |   |         |        |
| <a href="#">I2C_DATE_REG</a>              | Version register                            | 0x00F8  | R/W    |
| <b>Address register</b>                   |   |         |        |
| <a href="#">I2C_TXFIFO_START_ADDR_REG</a> | I2C TX FIFO base address register           | 0x0100  | HRO    |
| <a href="#">I2C_RXFIFO_START_ADDR_REG</a> | I2C RX FIFO base address register           | 0x0180  | HRO    |

## 39.8.2 LP\_I2C Register Summary

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <b>Timing Registers</b>                         |  |         |        |
| <a href="#">LP_I2C_SCL_LOW_PERIOD_REG</a>       | Configures the low level width of the SCL Clock                                    | 0x0000  | R/W    |
| <a href="#">LP_I2C_SDA_HOLD_REG</a>             | Configures the hold time after a negative SCL edge                                 | 0x0030  | R/W    |
| <a href="#">LP_I2C_SDA_SAMPLE_REG</a>           | Configures the sample time after a positive SCL edge                               | 0x0034  | R/W    |
| <a href="#">LP_I2C_SCL_HIGH_PERIOD_REG</a>      | Configures the high level width of SCL   | 0x0038  | R/W    |
| <a href="#">LP_I2C_SCL_START_HOLD_REG</a>       | Configures the delay between the SDA and SCL negative edge for a start condition   | 0x0040  | R/W    |
| <a href="#">LP_I2C_SCL_RSTART_SETUP_REG</a>     | Configures the delay between the positive edge of SCL and the negative edge of SDA | 0x0044  | R/W    |
| <a href="#">LP_I2C_SCL_STOP_HOLD_REG</a>        | Configures the delay after the SCL clock edge for a stop condition                 | 0x0048  | R/W    |
| <a href="#">LP_I2C_SCL_STOP_SETUP_REG</a>       | Configures the delay between the SDA and SCL positive edge for a stop condition    | 0x004C  | R/W    |
| <a href="#">LP_I2C_SCL_ST_TIME_OUT_REG</a>      | SCL status time out register   | 0x0078  | R/W    |
| <a href="#">LP_I2C_SCL_MAIN_ST_TIME_OUT_REG</a> | SCL main status time out register  | 0x007C  | R/W    |
| <b>Configuration Registers</b>                  |  |         |        |
| <a href="#">LP_I2C_CTR_REG</a>                  | Transmission setting   | 0x0004  | varies |
| <a href="#">LP_I2C_TO_REG</a>                   | Setting time out control for receiving data  | 0x000C  | R/W    |
| <a href="#">LP_I2C_FIFO_CONF_REG</a>            | FIFO configuration register  | 0x0018  | R/W    |
| <a href="#">LP_I2C_FILTER_CFG_REG</a>           | SCL and SDA filter configuration register  | 0x0050  | R/W    |
| <a href="#">LP_I2C_SCL_SP_CONF_REG</a>          | Power configuration register   | 0x0080  | varies |

| Name   | Description                                 | Address | Access  |
|--|---|---------|---------|
| <b>Status Registers</b>                      |   |         |         |
| <a href="#">LP_I2C_SR_REG</a>                | Describe I2C work status                    | 0x0008  | RO      |
| <a href="#">LP_I2C_FIFO_ST_REG</a>           | FIFO status register                        | 0x0014  | RO      |
| <a href="#">LP_I2C_DATA_REG</a>              | Rx FIFO read data                           | 0x001C  | RO      |
| <b>Interrupt Registers</b>                   |   |         |         |
| <a href="#">LP_I2C_INT_RAW_REG</a>           | Raw interrupt status                        | 0x0020  | R/SS/WT |
| <a href="#">LP_I2C_INT_CLR_REG</a>           | Interrupt clear bits                        | 0x0024  | WT      |
| <a href="#">LP_I2C_INT_ENA_REG</a>           | Interrupt enable bits                       | 0x0028  | R/W     |
| <a href="#">LP_I2C_INT_STATUS_REG</a>        | Status of captured I2C communication events | 0x002C  | RO      |
| <b>Command Registers</b>                     |   |         |         |
| <a href="#">LP_I2C_COMD0_REG</a>             | I2C command register 0                      | 0x0058  | varies  |
| <a href="#">LP_I2C_COMD1_REG</a>             | I2C command register 1                      | 0x005C  | varies  |
| <a href="#">LP_I2C_COMD2_REG</a>             | I2C command register 2                      | 0x0060  | varies  |
| <a href="#">LP_I2C_COMD3_REG</a>             | I2C command register 3                      | 0x0064  | varies  |
| <a href="#">LP_I2C_COMD4_REG</a>             | I2C command register 4                      | 0x0068  | varies  |
| <a href="#">LP_I2C_COMD5_REG</a>             | I2C command register 5                      | 0x006C  | varies  |
| <a href="#">LP_I2C_COMD6_REG</a>             | I2C command register 6                      | 0x0070  | varies  |
| <a href="#">LP_I2C_COMD7_REG</a>             | I2C command register 7                      | 0x0074  | varies  |
| <b>Version Register</b>                      |   |         |         |
| <a href="#">LP_I2C_DATE_REG</a>              | Version register                            | 0x00F8  | R/W     |
| <b>Address Registers</b>                     |   |         |         |
| <a href="#">LP_I2C_TXFIFO_START_ADDR_REG</a> | I2C TXFIFO base address register            | 0x0100  | HRO     |
| <a href="#">LP_I2C_RXFIFO_START_ADDR_REG</a> | I2C RXFIFO base address register            | 0x0180  | HRO     |

## 39.9 Registers

### 39.9.1 I2C Registers

The addresses in this section are relative to the I2C Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 39.1. I2C\_SCL\_LOW\_PERIOD\_REG (0x0000)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SCL_LOW_PERIOD |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                  | 8 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                  |   |   |  |  |  |  |  | Reset |  |

**I2C\_SCL\_LOW\_PERIOD** Configures the low level width of the SCL Clock in master mode.  
Measurement unit: I2C\_SCLK clock cycles  
(R/W)

Register 39.2. I2C\_SDA\_HOLD\_REG (0x0030)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SDA_HOLD_TIME |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                 |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                 |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**I2C\_SDA\_HOLD\_TIME** Configures the time to hold the data after the falling edge of SCL.  
Measurement unit: I2C\_SCLK clock cycles  
(R/W)

**Register 39.3. I2C\_SDA\_SAMPLE\_REG (0x0034)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**I2C\_SDA\_SAMPLE\_TIME** Configures the time for sampling SDA.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**Register 39.4. I2C\_SCL\_HIGH\_PERIOD\_REG (0x0038)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SCL_WAIT_HIGH_PERIOD |  |  |  |  |  |  |  | I2C_SCL_HIGH_PERIOD |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                       |  |  |  |  |  |  |  | 15                  |  |  |  |  |  |  |  | 9     |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                        |  |  |  |  |  |  |  | 0                   |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**I2C\_SCL\_HIGH\_PERIOD** Configures for how long SCL remains high in master mode.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

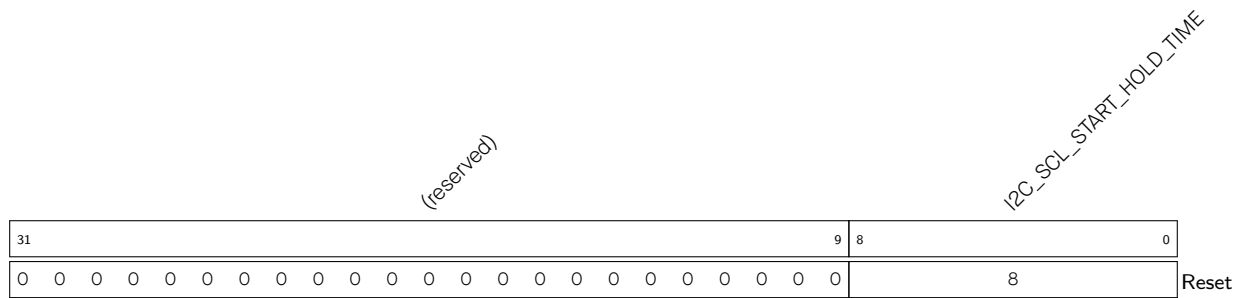
**I2C\_SCL\_WAIT\_HIGH\_PERIOD** Configures the SCL\_FSM's waiting period for SCL high level in master mode.

Measurement unit: I2C\_SCLK clock cycles

(R/W)



### Register 39.5. I2C\_SCL\_START\_HOLD\_REG (0x0040)

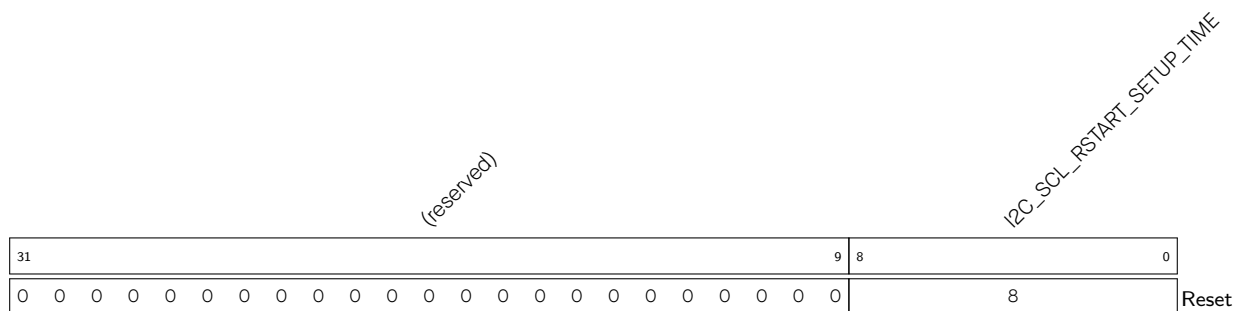


**I2C\_SCL\_START\_HOLD\_TIME** Configures the time between the falling edge of SDA and the falling edge of SCL for a START condition.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

### Register 39.6. I2C\_SCL\_RSTART\_SETUP\_REG (0x0044)

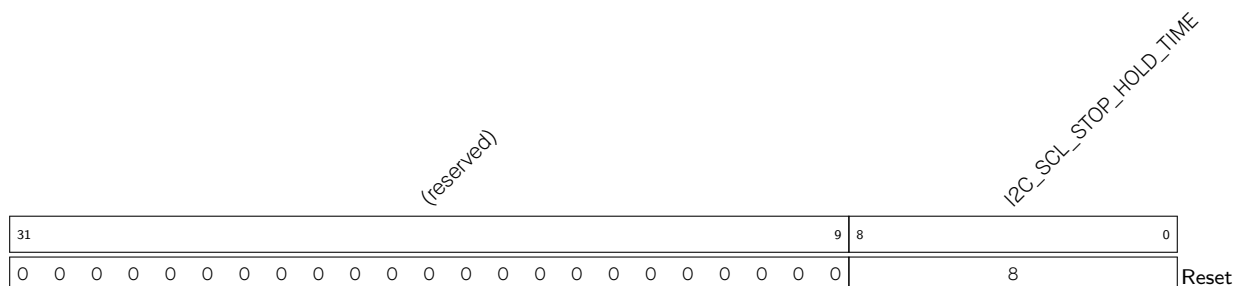


**I2C\_SCL\_RSTART\_SETUP\_TIME** Configures the time between the positive edge of SCL and the negative edge of SDA for a RESTART condition.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

### Register 39.7. I2C\_SCL\_STOP\_HOLD\_REG (0x0048)



**I2C\_SCL\_STOP\_HOLD\_TIME** Configures the delay after the STOP condition.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**Register 39.8. I2C\_SCL\_STOP\_SETUP\_REG (0x004C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SCL_STOP_SETUP_TIME |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**I2C\_SCL\_STOP\_SETUP\_TIME** Configures the time between the rising edge of SCL and the rising edge of SDA.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**Register 39.9. I2C\_SCL\_ST\_TIME\_OUT\_REG (0x0078)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |   |   |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|---|---|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SCL_ST_TO_I2C |   |   |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5                 | 4 | 0 |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x10              |   |   |  | Reset |  |

**I2C\_SCL\_ST\_TO\_I2C** Configures the threshold value of SCL\_FSM state unchanged period. It should be no more than 23.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**Register 39.10. I2C\_SCL\_MAIN\_ST\_TIME\_OUT\_REG (0x007C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SCL_MAIN_ST_TO_I2C |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5                      | 4 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x10                   |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**I2C\_SCL\_MAIN\_ST\_TO\_I2C** Configures the threshold value of SCL\_MAIN\_FSM state unchanged period. It should be no more than 23.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**Register 39.11. I2C\_CTR\_REG (0x0004)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|---|---|---|---|---|---|-------|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2C_ADDR_BROADCASTING_EN<br>I2C_ADDR_10BIT_RW_CHECK_EN<br>I2C_SLV_TX_AUTO_START_EN<br>I2C_CONF_UPGATE<br>I2C_FSM_RST<br>I2C_ARBITRATION_EN<br>I2C_CLK_EN<br>I2C_RX_LSB_FIRST<br>I2C_TX_LSB_FIRST<br>I2C_TRANS_START<br>I2C_MS_MODE<br>I2C_RX_FULL_ACK_LEVEL<br>I2C_SAMPLE_SCL_LEVEL<br>I2C_SCL_FORCE_OUT<br>I2C_SDA_FORCE_OUT |    |    |    |    |    |   |   |   |   |   |   |       |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15  | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1   | 0  | 0  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 0 | 0 | Reset |   |   |   |

**I2C\_SDA\_FORCE\_OUT** Configures the SDA output mode.

0: Open drain output

1: Direct output

(R/W)

**I2C\_SCL\_FORCE\_OUT** Configures the SCL output mode.

0: Open drain output

1: Direct output

(R/W)

**I2C\_SAMPLE\_SCL\_LEVEL** Configures the sample mode for SDA.

0: Sample SDA data on the SCL high level

1: Sample SDA data on the SCL low level

(R/W)

**I2C\_RX\_FULL\_ACK\_LEVEL** Configures the ACK value that needs to be sent by the master when the received RX RAM has reached the threshold.

(R/W)

**I2C\_MS\_MODE** Configures the module as an I2C Master or Slave.

0: Slave

1: Master

(R/W)

**I2C\_TRANS\_START** Configures whether the slave starts sending the data in TX FIFO.

0: No effect

1: Start

(WT)

**I2C\_TX\_LSB\_FIRST** Configures to control the sending order for data needing to be sent.

0: send data from the most significant bit

1: send data from the least significant bit

(R/W)

**I2C\_RX\_LSB\_FIRST** Configures to control the storage order for received data.

0: receive data from the most significant bit

1: receive data from the least significant bit

(R/W)

Continued on the next page...

**Register 39.11. I2C\_CTR\_REG (0x0004)**

Continued from the previous page...

**I2C\_CLK\_EN** Configures whether to gate clock signal for registers.

0: Support clock only when registers are read or written to by software

1: Force clock on for registers

(R/W)

**I2C\_ARBITRATION\_EN** Configures to enable I2C bus arbitration detection.

0: No effect

1: Enable

(R/W)

**I2C\_FSM\_RST** Configures to reset the SCL\_FSM.

0: No effect

1: Reset (WT)

**I2C\_CONF\_UPGATE** Configures this bit for synchronization.

0: No effect

1: Synchronize (WT)

**I2C\_SLV\_TX\_AUTO\_START\_EN** Configures to enable slave to send data automatically

0: Disable

1: Enable

(R/W)

**I2C\_ADDR\_10BIT\_RW\_CHECK\_EN** Configures to check if the R/W bit of 10-bit addressing consists with I2C protocol.

0: Not check

1: Check (R/W)

**I2C\_ADDR\_BROADCASTING\_EN** Configures to support the 7-bit general call function.

0: Not support

1: Support

(R/W)

Register 39.12. I2C\_TO\_REG (0x000C)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |      |                    |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|------|--------------------|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_TIME_OUT_EN |      | I2C_TIME_OUT_VALUE |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6               | 5    | 4                  | 0     |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0               | 0x10 |                    | Reset |  |

**I2C\_TIME\_OUT\_VALUE** Configures the timeout threshold period for SCL stuck at high or low level.

The actual period is  $2^{(I2C\_TIME\_OUT\_VALUE)}$ .

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**I2C\_TIME\_OUT\_EN** Configures to enable time out control.

0: No effect

1: Enable

(R/W)

Register 39.13. I2C\_SLAVE\_ADDR\_REG (0x0010)

|                   |    |   |   |   |   |   |   |   |   |   |   |   |   |   |    |            |   |  |  |  |  |  |  |  |  |  |  |  |  |   |       |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|----|------------|---|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| I2C_ADDR_10BIT_EN |    |   |   |   |   |   |   |   |   |   |   |   |   |   |    | (reserved) |   |  |  |  |  |  |  |  |  |  |  |  |  |   |       | I2C_SLAVE_ADDR |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   | 15 | 14         |   |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0          | 0 |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**I2C\_SLAVE\_ADDR** Configure the slave address of I2C Slave.

(R/W)

**I2C\_ADDR\_10BIT\_EN** Configures to enable the slave 10-bit addressing mode in master mode.

0: No effect

1: Enable

(R/W)

**Register 39.14. I2C\_FIFO\_CONF\_REG (0x0018)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                 |    |    |    |                 |    |     |  |                 |  |     |   |                      |  |       |  |                |   |  |  |                     |  |  |  |                     |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|----|----|----|-----------------|----|-----|--|-----------------|--|-----|---|----------------------|--|-------|--|----------------|---|--|--|---------------------|--|--|--|---------------------|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_FIFO_PRT_EN |    |    |    | I2C_TX_FIFO_RST |    |     |  | I2C_RX_FIFO_RST |  |     |   | I2C_FIFO_ADDR_CFG_EN |  |       |  | I2C_NONFIFO_EN |   |  |  | I2C_TXFIFO_WM_THRHD |  |  |  | I2C_RXFIFO_WM_THRHD |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15              | 14 | 13 | 12 | 11              | 10 | 9   |  |                 |  |     | 5 | 4                    |  |       |  |                | 0 |  |  |                     |  |  |  |                     |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1               | 0  | 0  | 0  | 0               | 0  | 0x4 |  |                 |  | 0xb |   |                      |  | Reset |  |                |   |  |  |                     |  |  |  |                     |  |  |  |

Reset

**I2C\_RXFIFO\_WM\_THRHD** Configures the watermark threshold of RX FIFO in non-FIFO access mode. When I2C\_FIFO\_PRT\_EN is 1 and RX FIFO counter is bigger than I2C\_RXFIFO\_WM\_THRHD[4:0], I2C\_RXFIFO\_WM\_INT\_RAW bit will be valid. (R/W)

**I2C\_TXFIFO\_WM\_THRHD** Configures the watermark threshold of TX FIFO in non-FIFO access mode. When I2C\_FIFO\_PRT\_EN is 1 and TC FIFO counter is bigger than I2C\_TXFIFO\_WM\_THRHD[4:0], I2C\_TXFIFO\_WM\_INT\_RAW bit will be valid. (R/W)

**I2C\_NONFIFO\_EN** Configures to enable APB non-FIFO access. (R/W)

**I2C\_FIFO\_ADDR\_CFG\_EN** Configures the slave to enable dual address mode. When this mode is enabled, the byte received after the I2C address byte represents the offset address in the I2C Slave RAM.  
 0: Disable  
 1: Enable  
 (R/W)

**I2C\_RX\_FIFO\_RST** Configures to reset RX FIFO.  
 0: No effect  
 1: Reset (R/W)

**I2C\_TX\_FIFO\_RST** Configures to reset TX FIFO.  
 0: No effect  
 1: Reset (R/W)

**I2C\_FIFO\_PRT\_EN** Configures to enable FIFO pointer in non-FIFO access mode. This bit controls the valid bits and the TX/RX FIFO overflow, underflow, full and empty interrupts.  
 0: No effect  
 1: Enable  
 (R/W)

Register 39.15. I2C\_FILTER\_CFG\_REG (0x0050)

|    |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |   |  |   |   |   |       |  |
|----|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|---|--|---|---|---|-------|--|
|    |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  | I2C_SDA_FILTER_EN<br>I2C_SCL_FILTER_EN |   | I2C_SDA_FILTER_THRES<br>I2C_SCL_FILTER_THRES |   |   |   |       |  |
| 31 |  |  |  |  |  |  |  |  |  | 10         |  |  |  |  |  |  |  |  |  | 9                                      | 8 | 7  | 4 |   | 3 | 0     |  |
| 0  |  |  |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  |  |  | 1                                      | 1 | 0  |   | 0 |   | Reset |  |

**I2C\_SCL\_FILTER\_THRES** Configures the threshold pulse width to be filtered on SCL. When a pulse on the SCL input has smaller width than this register value, the I2C controller will ignore that pulse. Measurement unit: I2C\_SCLK clock cycles  
(R/W)

**I2C\_SDA\_FILTER\_THRES** Configures the threshold pulse width to be filtered on SDA. When a pulse on the SDA input has smaller width than this register value, the I2C controller will ignore that pulse. Measurement unit: I2C\_SCLK clock cycles  
(R/W)

**I2C\_SCL\_FILTER\_EN** Configures to enable the filter function for SCL.  
0: No effect  
1: Enable  
(R/W)

**I2C\_SDA\_FILTER\_EN** Configures to enable the filter function for SDA.  
0: No effect  
1: Enable  
(R/W)

**Register 39.16. I2C\_SCL\_SP\_CONF\_REG (0x0080)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |               |   |               |   |                     |  |                    |       |   |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------|---|---------------|---|---------------------|--|--------------------|-------|---|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SDA_PD_EN |   | I2C_SCL_PD_EN |   | I2C_SCL_RST_SLV_NUM |  | I2C_SCL_RST_SLV_EN |       |   |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8             | 7 | 6             | 5 | 1                   |  |                    |       | 0 |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0             | 0 | 0             |   |                     |  | 0                  | Reset |   |

**I2C\_SCL\_RST\_SLV\_EN** Configures to send out SCL pulses when I2C master is IDLE. The number of pulses equals to I2C\_SCL\_RST\_SLV\_NUM[4:0].

0: Invalid

1: Send out SCL pulses

(R/W/SC)

**I2C\_SCL\_RST\_SLV\_NUM** Configure the pulses of SCL generated in I2C master mode.

Valid when I2C\_SCL\_RST\_SLV\_EN is 1.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**I2C\_SCL\_PD\_EN** Configures to power down the I2C output SCL line.

0: Not power down.

1: Not work and power down.

Valid only when I2C\_SCL\_FORCE\_OUT is 1. (R/W)

**I2C\_SDA\_PD\_EN** Configures to power down the I2C output SDA line.

0: Not power down.

1: Not work and power down.

Valid only when I2C\_SDA\_FORCE\_OUT is 1. (R/W)



Register 39.17. I2C\_SCL\_STRETCH\_CONF\_REG (0x0084)

|                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |   |   |                         |  |  |  |  |  |  |  |       |  |
|-------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|---|---|-------------------------|--|--|--|--|--|--|--|-------|--|
| (reserved)                          |  |  |  |  |  |  |  |  |  |  |  |  |  | I2C_SLAVE_BYTE_ACK_LVL<br>I2C_SLAVE_BYTE_ACK_CTL_EN<br>I2C_SLAVE_SCL_STRETCH_CLR<br>I2C_SLAVE_SCL_STRETCH_EN |    |    |    |    |   |   | I2C_STRETCH_PROTECT_NUM |  |  |  |  |  |  |  |       |  |
| 31                                  |  |  |  |  |  |  |  |  |  |  |  |  |  | 14   | 13 | 12 | 11 | 10 | 9 | 0 |                         |  |  |  |  |  |  |  |       |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  |   |   |                         |  |  |  |  |  |  |  | Reset |  |

**I2C\_STRETCH\_PROTECT\_NUM** Configures the time period to release the SCL line from stretching to avoid timing violation. Usually it should be larger than the SDA setup time.

Measurement unit: I2C\_SCLK clock cycles

(R/W)

**I2C\_SLAVE\_SCL\_STRETCH\_EN** Configures to enable slave SCL stretch function. The SCL output line will be stretched low when I2C\_SLAVE\_SCL\_STRETCH\_EN is 1 and a stretch event happens. The stretch cause can be seen in I2C\_STRETCH\_CAUSE.

0: Disable

1: Enable

(R/W)

**I2C\_SLAVE\_SCL\_STRETCH\_CLR** Configures to clear the I2C slave SCL stretch function.

0: No effect

1: Clear

(WT)

**I2C\_SLAVE\_BYTE\_ACK\_CTL\_EN** Configures to enable the function for the slave to control ACK level.

0: Disable

1: Enable

(R/W)

**I2C\_SLAVE\_BYTE\_ACK\_LVL** Configures the ACK level when slave controlling ACK level function is enabled.

0: Low level

1: High level

(R/W)

**Register 39.18. I2C\_SR\_REG (0x0008)**

|            |    |                    |    |            |    |                         |    |                |     |            |    |                   |   |                |   |            |   |                     |   |              |   |              |   |            |   |              |   |              |       |
|------------|----|--------------------|----|------------|----|-------------------------|----|----------------|-----|------------|----|-------------------|---|----------------|---|------------|---|---------------------|---|--------------|---|--------------|---|------------|---|--------------|---|--------------|-------|
| (reserved) |    | I2C_SCL_STATE_LAST |    | (reserved) |    | I2C_SCL_MAIN_STATE_LAST |    | I2C_TXFIFO_CNT |     | (reserved) |    | I2C_STRETCH_CAUSE |   | I2C_RXFIFO_CNT |   | (reserved) |   | I2C_SLAVE_ADDRESSED |   | I2C_BUS_BUSY |   | I2C_ARB_LOST |   | (reserved) |   | I2C_SLAVE_RW |   | I2C_RESP_REC |       |
| 31         | 30 | 28                 | 27 | 26         | 24 | 23                      | 18 | 17             | 16  | 15         | 14 | 13                | 8 | 7              | 6 | 5          | 4 | 3                   | 2 | 1            | 0 |              |   |            |   |              |   |              |       |
| 0          | 0  | 0                  | 0  | 0          | 0  | 0                       | 0  | 0              | 0x3 | 0          | 0  | 0                 | 0 | 0              | 0 | 0          | 0 | 0                   | 0 | 0            | 0 | 0            | 0 | 0          | 0 | 0            | 0 | 0            | Reset |

**I2C\_RESP\_REC** Represents the received ACK value in master mode or slave mode.

- 0: ACK
- 1: NACK. (RO)

**I2C\_SLAVE\_RW** Represents the transfer direction in slave mode.

- 0: Master writes to slave. 1: Master reads from slave
- (RO)

**I2C\_ARB\_LOST** Represents whether the I2C controller loses control of SCL line.

- 0: No arbitration lost
- 1: Arbitration lost
- (RO)

**I2C\_BUS\_BUSY** Represents the I2C bus state.

- 0: The I2C bus is in an idle state.
- 1: The I2C bus is busy transferring data
- (RO)

**I2C\_SLAVE\_ADDRESSED** Represents whether the address sent by the master is equal to the address of the slave.

Valid only when the module is configured as an I2C Slave.

- 0: Not equal
- 1: Equal
- (RO)

**I2C\_RXFIFO\_CNT** Represents the number of data bytes received in RAM. (RO)

**I2C\_STRETCH\_CAUSE** Represents the cause of SCL clocking stretching in slave mode.

- 0: Stretching SCL low when the master starts to read data.
- 1: Stretching SCL low when I2C TX FIFO is empty in slave mode.
- 2: Stretching SCL low when I2C RX FIFO is full in slave mode.
- 3: Invalid
- (RO)

**I2C\_TXFIFO\_CNT** Represents the number of data bytes to be sent. (RO)

Continued on the next page...

**Register 39.18. I2C\_SR\_REG (0x0008)**

Continued from the previous page...

**I2C\_SCL\_MAIN\_STATE\_LAST** Represents the states of the I2C module state machine.

- 0: Idle
- 1: Address shift
- 2: ACK address
- 3: Rx data
- 4: Tx data
- 5: Send ACK
- 6: Wait ACK
- 7: Invalid
- (RO)

**I2C\_SCL\_STATE\_LAST** Represents the states of the state machine used to produce SCL.

- 0: Idle
- 1: Start
- 2: Negative edge
- 3: Low
- 4: Positive edge
- 5: High
- 6: Stop
- 7: Invalid
- (RO)

**Register 39.19. I2C\_FIFO\_ST\_REG (0x0014)**

|            |    |    |                    |  |  |   |            |    |    |                  |  |   |  |                  |    |    |  |                  |  |   |    |                  |  |   |  |  |   |   |  |  |  |       |   |
|------------|----|----|--------------------|--|--|---|------------|----|----|------------------|--|---|--|------------------|----|----|--|------------------|--|---|----|------------------|--|---|--|--|---|---|--|--|--|-------|---|
| (reserved) |    |    | I2C_SLAVE_RW_POINT |  |  |   | (reserved) |    |    | I2C_TXFIFO_WADDR |  |   |  | I2C_TXFIFO_RADDR |    |    |  | I2C_RXFIFO_WADDR |  |   |    | I2C_RXFIFO_RADDR |  |   |  |  |   |   |  |  |  |       |   |
| 31         | 30 | 29 |                    |  |  |   | 22         | 21 | 20 | 19               |  |   |  |                  | 15 | 14 |  |                  |  |   | 10 | 9                |  |   |  |  | 5 | 4 |  |  |  |       | 0 |
| 0          | 0  | 0  |                    |  |  | 0 | 0          | 0  |    |                  |  | 0 |  |                  |    | 0  |  |                  |  | 0 |    |                  |  | 0 |  |  |   |   |  |  |  | Reset |   |

Reset

**I2C\_RXFIFO\_RADDR** Represents the offset address of the APB reading from RX FIFO. (RO)**I2C\_RXFIFO\_WADDR** Represents the offset address of the I2C module receiving data and writing to RX FIFO. (RO)**I2C\_TXFIFO\_RADDR** Represents the offset address of the I2C module reading from TX FIFO. (RO)**I2C\_TXFIFO\_WADDR** Represents the offset address of the APB bus writing to TX FIFO. (RO)**I2C\_SLAVE\_RW\_POINT** Represents the offset address in the I2C Slave RAM addressed by I2C Master when in I2C slave mode. (RO)

**Register 39.20. I2C\_DATA\_REG (0x001C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2C_FIFO_RDATA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8              | 7 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**I2C\_FIFO\_RDATA** Represents the value of RX FIFO read data. (RO)

**Register 39.21. I2C\_INT\_RAW\_REG (0x0020)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|---|-------|---|---|---|---|---|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2C_SLAVE_ADDR_UNMATCH_INT_RAW<br>I2C_GENERAL_CALL_INT_RAW<br>I2C_SLAVE_STRETCH_INT_RAW<br>I2C_DET_START_INT_RAW<br>I2C_SCL_MAIN_ST_TO_INT_RAW<br>I2C_SCL_ST_TO_INT_RAW<br>I2C_RXFIFO_UDF_INT_RAW<br>I2C_TXFIFO_UDF_INT_RAW<br>I2C_NACK_INT_RAW<br>I2C_TRANS_START_INT_RAW<br>I2C_TRANS_OUT_INT_RAW<br>I2C_MST_TXFIFO_COMPLETE_INT_RAW<br>I2C_BYTE_ARBTRATION_LOST_INT_RAW<br>I2C_END_DETECT_INT_RAW<br>I2C_RXFIFO_OVF_INT_RAW<br>I2C_TXFIFO_WM_INT_RAW |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 19  | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 0 | Reset |   |   |   |   |   |   |   |   |  |

**I2C\_RXFIFO\_WM\_INT\_RAW** The raw interrupt status of I2C\_RXFIFO\_WM\_INT interrupt. (R/SS/WTC)

**I2C\_TXFIFO\_WM\_INT\_RAW** The raw interrupt status of I2C\_TXFIFO\_WM\_INT interrupt. (R/SS/WTC)

**I2C\_RXFIFO\_OVF\_INT\_RAW** The raw interrupt status of I2C\_RXFIFO\_OVF\_INT interrupt. (R/SS/WTC)

**I2C\_END\_DETECT\_INT\_RAW** The raw interrupt status of the I2C\_END\_DETECT\_INT interrupt. (R/SS/WTC)

**I2C\_BYTE\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of the I2C\_END\_DETECT\_INT interrupt. (R/SS/WTC)

**I2C\_ARBITRATION\_LOST\_INT\_RAW** The raw interrupt status of the I2C\_ARBITRATION\_LOST\_INT interrupt. (R/SS/WTC)

**I2C\_MST\_TXFIFO\_UDF\_INT\_RAW** The raw interrupt status of I2C\_TRANS\_COMPLETE\_INT interrupt. (R/SS/WTC)

**I2C\_TRANS\_COMPLETE\_INT\_RAW** The raw interrupt status of the I2C\_TRANS\_COMPLETE\_INT interrupt. (R/SS/WTC)

Continued on the next page...

**Register 39.21. I2C\_INT\_RAW\_REG (0x0020)**

Continued from the previous page...

**I2C\_TIME\_OUT\_INT\_RAW** The raw interrupt status of the I2C\_TIME\_OUT\_INT interrupt. (R/SS/WTC)

**I2C\_TRANS\_START\_INT\_RAW** The raw interrupt status of the I2C\_TRANS\_START\_INT interrupt.  
(R/SS/WTC)

**I2C\_NACK\_INT\_RAW** The raw interrupt status of I2C\_SLAVE\_STRETCH\_INT interrupt. (R/SS/WTC)

**I2C\_TXFIFO\_OVF\_INT\_RAW** The raw interrupt status of I2C\_TXFIFO\_OVF\_INT interrupt. (R/SS/WTC)

**I2C\_RXFIFO\_UDF\_INT\_RAW** The raw interrupt status of I2C\_RXFIFO\_UDF\_INT interrupt.  
(R/SS/WTC)

**I2C\_SCL\_ST\_TO\_INT\_RAW** The raw interrupt status of I2C\_SCL\_ST\_TO\_INT interrupt. (R/SS/WTC)

**I2C\_SCL\_MAIN\_ST\_TO\_INT\_RAW** The raw interrupt status of I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt.  
(R/SS/WTC)

**I2C\_DET\_START\_INT\_RAW** The raw interrupt status of I2C\_DET\_START\_INT interrupt. (R/SS/WTC)

**I2C\_SLAVE\_STRETCH\_INT\_RAW** The raw interrupt status of I2C\_SLAVE\_STRETCH\_INT interrupt.  
(R/SS/WTC)

**I2C\_GENERAL\_CALL\_INT\_RAW** The raw interrupt status of I2C\_GENARAL\_CALL\_INT interrupt.  
(R/SS/WTC)

**I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_RAW** The raw interrupt status of  
I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_RAW interrupt. (R/SS/WTC)

### Register 39.22. I2C\_INT\_CLR\_REG (0x0024)

[illegible]

**I2C\_RXFIFO\_WM\_INT\_CLR** Write 1 to clear I2C\_RXFIFO\_WM\_INT interrupt. (WT)

**I2C\_TXFIFO\_WM\_INT\_CLR** Write 1 to clear I2C\_TXFIFO\_WM\_INT interrupt. (WT)

**I2C\_RXFIFO\_OVF\_INT\_CLR** Write 1 to clear I2C\_RXFIFO\_OVF\_INT interrupt. (WT)

**I2C\_END\_DETECT\_INT\_CLR** Write 1 to clear the I2C\_END\_DETECT\_INT interrupt. (WT)

**I2C\_BYTE\_TRANS\_DONE\_INT\_CLR** Write 1 to clear the I2C\_BYTE\_TRANS\_DONE\_INT interrupt.  
(WT)

**I2C\_ARBITRATION\_LOST\_INT\_CLR** Write 1 to clear the I2C\_ARBITRATION\_LOST\_INT interrupt. (WT)

**I2C\_MST\_TXFIFO\_UDF\_INT\_CLR** Write 1 to clear I2C\_MST\_TXFIFO\_UDF\_INT interrupt. (WT)

**I2C\_TRANS\_COMPLETE\_INT\_CLR** Write 1 to clear the I2C\_TRANS\_COMPLETE\_INT interrupt. (WT)

**I2C\_TIME\_OUT\_INT\_CLR** Write 1 to clear the I2C\_TIME\_OUT\_INT interrupt. (WT)

**I2C\_TRANS\_START\_INT\_CLR** Write 1 to clear the I2C\_TRANS\_START\_INT interrupt. (WT)

**I2C\_NACK\_INT\_CLR** Write 1 to clear I2C\_NACK\_INT interrupt. (WT)

**I2C\_TXFIFO\_OVF\_INT\_CLR** Write 1 to clear I2C\_TXFIFO\_OVF\_INT interrupt. (WT)

**I2C\_RXFIFO\_UDF\_INT\_CLR** Write 1 to clear I2C\_RXFIFO\_UDF\_INT interrupt. (WT)

**I2C\_SCL\_ST\_TO\_INT\_CLR** Write 1 to clear I2C\_SCL\_ST\_TO\_INT interrupt. (WT)

**I2C\_SCL\_MAIN\_ST\_TO\_INT\_CLR** Write 1 to clear I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (WT)

**I2C\_DET\_START\_INT\_CLR** Write 1 to clear I2C\_DET\_START\_INT interrupt. (WT)

**I2C\_SLAVE\_STRETCH\_INT\_CLR** Write 1 to clear I2C\_SLAVE\_STRETCH\_INT interrupt. (WT)

**I2C GENERAL CALL INT CLR** Write 1 to clear I2C GENARAL CALL INT interrupt. (WT)

**I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_CLR** Write 1 to clear I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_RAW interrupt. (WT)

## Register 39.23. I2C\_INT\_ENA\_REG (0x0028)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|----|----|----|---|-------|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2C_SLAVE_ADDR_UNMATCH_INT_ENA<br>I2C_GENERAL_CALL_INT_ENA<br>I2C_SLAVE_STRETCH_INT_ENA<br>I2C_DET_START_INT_ENA<br>I2C_SCL_MAIN_ST_TO_INT_ENA<br>I2C_SCL_ST_TO_INT_ENA<br>I2C_RXFIFO_UDF_INT_ENA<br>I2C_TXFIFO_OVF_INT_ENA<br>I2C_NACK_INT_ENA<br>I2C_TRANS_START_INT_ENA<br>I2C_TIME_OUT_INT_ENA<br>I2C_TRANS_COMPLETE_INT_ENA<br>I2C_MST_TXFIFO_UDF_INT_ENA<br>I2C_ARBITRATION_LOST_INT_ENA<br>I2C_BYTE_TRANS_DONE_INT_ENA<br>I2C_END_DETECT_INT_ENA<br>I2C_RXFIFO_OVF_INT_ENA<br>I2C_RXFIFO_WM_INT_ENA |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 19   | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | Reset |   |   |   |   |   |   |   |   |

**I2C\_RXFIFO\_WM\_INT\_ENA** Write 1 to enable I2C\_RXFIFO\_WM\_INT interrupt. (R/W)

**I2C\_TXFIFO\_WM\_INT\_ENA** Write 1 to enable I2C\_TXFIFO\_WM\_INT interrupt. (R/W)

**I2C\_RXFIFO\_OVF\_INT\_ENA** Write 1 to enable I2C\_RXFIFO\_OVF\_INT interrupt. (R/W)

**I2C\_END\_DETECT\_INT\_ENA** Write 1 to enable the I2C\_END\_DETECT\_INT interrupt. (R/W)

**I2C\_BYTE\_TRANS\_DONE\_INT\_ENA** Write 1 to enable the I2C\_END\_DETECT\_INT interrupt. (R/W)

**I2C\_ARBITRATION\_LOST\_INT\_ENA** Write 1 to enable the I2C\_ARBITRATION\_LOST\_INT interrupt. (R/W)

**I2C\_MST\_TXFIFO\_UDF\_INT\_ENA** Write 1 to enable I2C\_TRANS\_COMPLETE\_INT interrupt. (R/W)

**I2C\_TRANS\_COMPLETE\_INT\_ENA** Write 1 to enable the I2C\_TRANS\_COMPLETE\_INT interrupt. (R/W)

**I2C\_TIME\_OUT\_INT\_ENA** Write 1 to enable the I2C\_TIME\_OUT\_INT interrupt. (R/W)

**I2C\_TRANS\_START\_INT\_ENA** Write 1 to enable the I2C\_TRANS\_START\_INT interrupt. (R/W)

**I2C\_NACK\_INT\_ENA** Write 1 to enable I2C\_SLAVE\_STRETCH\_INT interrupt. (R/W)

**I2C\_TXFIFO\_OVF\_INT\_ENA** Write 1 to enable I2C\_TXFIFO\_OVF\_INT interrupt. (R/W)

**I2C\_RXFIFO\_UDF\_INT\_ENA** Write 1 to enable I2C\_RXFIFO\_UDF\_INT interrupt. (R/W)

**I2C\_SCL\_ST\_TO\_INT\_ENA** Write 1 to enable I2C\_SCL\_ST\_TO\_INT interrupt. (R/W)

**I2C\_SCL\_MAIN\_ST\_TO\_INT\_ENA** Write 1 to enable I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (R/W)

**I2C\_DET\_START\_INT\_ENA** Write 1 to enable I2C\_DET\_START\_INT interrupt. (R/W)

**I2C\_SLAVE\_STRETCH\_INT\_ENA** Write 1 to enable I2C\_SLAVE\_STRETCH\_INT interrupt. (R/W)

**I2C\_GENERAL\_CALL\_INT\_ENA** Write 1 to enable I2C\_GENARAL\_CALL\_INT interrupt. (R/W)

**I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_ENA** Write 1 to enable I2C\_SLAVE\_ADDR\_UNMATCH\_INT interrupt. (R/W)

**Register 39.24. I2C\_INT\_STATUS\_REG (0x002C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|---|-------|---|---|---|---|---|---|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2C_SLAVE_ADDR_UNMATCH_INT_ST<br>I2C_GENERAL_CALL_INT_ST<br>I2C_SLAVE_STRETCH_INT_ST<br>I2C_DET_START_INT_ST<br>I2C_SCL_MAIN_ST_TO_INT_ST<br>I2C_SCL_ST_TO_INT_ST<br>I2C_RXFIFO_UDF_INT_ST<br>I2C_TXFIFO_UDF_INT_ST<br>I2C_NACK_INT_ST<br>I2C_TRANS_START_INT_ST<br>I2C_TIME_OUT_INT_ST<br>I2C_TRANS_COMPLETE_INT_ST<br>I2C_MST_TXFIFO_UDF_INT_ST<br>I2C_ARBTRATION_LOST_INT_ST<br>I2C_BYTE_TRANS_DONE_INT_ST<br>I2C_END_DETECT_INT_ST<br>I2C_RXFIFO_OVF_INT_ST<br>I2C_TXFIFO_WM_INT_ST<br>I2C_RXFIFO_WM_INT_ST |    |    |    |    |    |    |    |    |    |   |       |   |   |   |   |   |   |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 19  | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8     | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | Reset |   |   |   |   |   |   |   |   |  |  |

**I2C\_RXFIFO\_WM\_INT\_ST** The masked interrupt status of I2C\_RXFIFO\_WM\_INT interrupt. (RO)

**I2C\_TXFIFO\_WM\_INT\_ST** The masked interrupt status of I2C\_TXFIFO\_WM\_INT interrupt. (RO)

**I2C\_RXFIFO\_OVF\_INT\_ST** The masked interrupt status of I2C\_RXFIFO\_OVF\_INT interrupt. (RO)

**I2C\_END\_DETECT\_INT\_ST** The masked interrupt status of the I2C\_END\_DETECT\_INT interrupt. (RO)

**I2C\_BYTE\_TRANS\_DONE\_INT\_ST** The masked interrupt status of the I2C\_END\_DETECT\_INT interrupt. (RO)

**I2C\_ARBTRATION\_LOST\_INT\_ST** The masked interrupt status of the I2C\_ARBTRATION\_LOST\_INT interrupt. (RO)

**I2C\_MST\_TXFIFO\_UDF\_INT\_ST** The masked interrupt status of I2C\_TRANS\_COMPLETE\_INT interrupt. (RO)

**I2C\_TRANS\_COMPLETE\_INT\_ST** The masked interrupt status of the I2C\_TRANS\_COMPLETE\_INT interrupt. (RO)

**I2C\_TIME\_OUT\_INT\_ST** The masked interrupt status of the I2C\_TIME\_OUT\_INT interrupt. (RO)

**I2C\_TRANS\_START\_INT\_ST** The masked interrupt status of the I2C\_TRANS\_START\_INT interrupt. (RO)

**I2C\_NACK\_INT\_ST** The masked interrupt status of I2C\_SLAVE\_STRETCH\_INT interrupt. (RO)

**I2C\_TXFIFO\_OVF\_INT\_ST** The masked interrupt status of I2C\_TXFIFO\_OVF\_INT interrupt. (RO)

Continued on the next page...



**Register 39.24. I2C\_INT\_STATUS\_REG (0x002C)**

Continued from the previous page...

**I2C\_RXFIFO\_UDF\_INT\_ST** The masked interrupt status of I2C\_RXFIFO\_UDF\_INT interrupt. (RO)

**I2C\_SCL\_ST\_TO\_INT\_ST** The masked interrupt status of I2C\_SCL\_ST\_TO\_INT interrupt. (RO)

**I2C\_SCL\_MAIN\_ST\_TO\_INT\_ST** The masked interrupt status of I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (RO)

**I2C\_DET\_START\_INT\_ST** The masked interrupt status of I2C\_DET\_START\_INT interrupt. (RO)

**I2C\_SLAVE\_STRETCH\_INT\_ST** The masked interrupt status of I2C\_SLAVE\_STRETCH\_INT interrupt. (RO)

**I2C\_GENERAL\_CALL\_INT\_ST** The masked interrupt status of I2C\_GENERAL\_CALL\_INT interrupt. (RO)

**I2C\_SLAVE\_ADDR\_UNMATCH\_INT\_ST** The masked interrupt status of I2C\_SLAVE\_ADDR\_UNMATCH\_INT interrupt. (RO)

**Register 39.25. I2C\_COMDO\_REG (0x0058)**

|                          |    |   |   |   |   |   |   |   |   |   |   |   |   |    |    |                     |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|--------------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---------------------|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|
| <i>I2C_COMMAND0_DONE</i> |    |   |   |   |   |   |   |   |   |   |   |   |   |    |    | <i>I2C_COMMAND0</i> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| 31                       | 30 |   |   |   |   |   |   |   |   |   |   |   |   | 14 | 13 | 0                   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| 0                        | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0                   |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |

Reset

**I2C\_COMMAND0** Configures command 0.

It consists of three parts:

op\_code is the command

1: WRITE

2: STOP

3: READ

4: END

6: RSTART

Byte\_num represents the number of bytes that need to be sent or received.

ack\_check\_en, ack\_exp, and ack are used to control the ACK bit. See I2C cmd structure [39.4-2](#) for more information.

(R/W)

**I2C\_COMMAND0\_DONE** Represents whether command 0 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

**Register 39.26. I2C\_COMD1\_REG (0x005C)**

|                          |    |   |   |   |   |   |   |   |   |   |   |   |   |    |    |                     |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
|--------------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---------------------|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|
| <i>I2C_COMMAND1_DONE</i> |    |   |   |   |   |   |   |   |   |   |   |   |   |    |    | <i>I2C_COMMAND1</i> |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| 31                       | 30 |   |   |   |   |   |   |   |   |   |   |   |   | 14 | 13 | 0                   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |
| 0                        | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0                   |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |

Reset

**I2C\_COMMAND1** Configures command 1.

See details in I2C\_CMD0\_REG[13:0]. (R/W)

**I2C\_COMMAND1\_DONE** Represents whether command 1 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

I2C\_COMMAND2\_DONE

(reserved)

I2C\_COMMAND2

Reset

(R/W/SS)

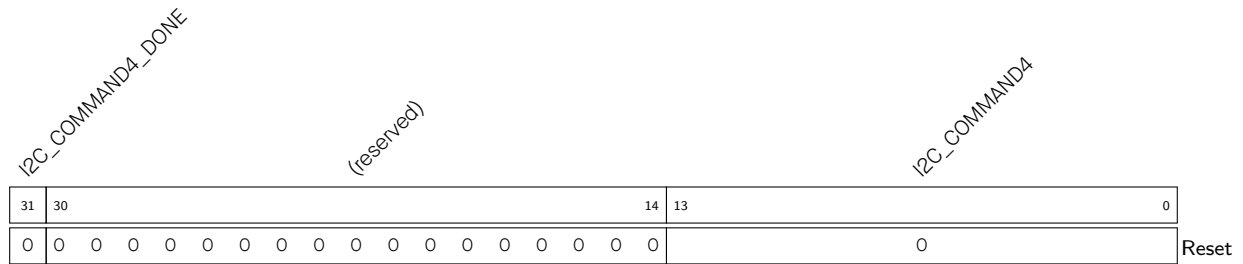
I2C\_COMMAND3\_DONE

(reserved)

I2C\_COMMAND3

Reset

(R/W/SS)

**Register 39.29. I2C\_COMD4\_REG (0x0068)**

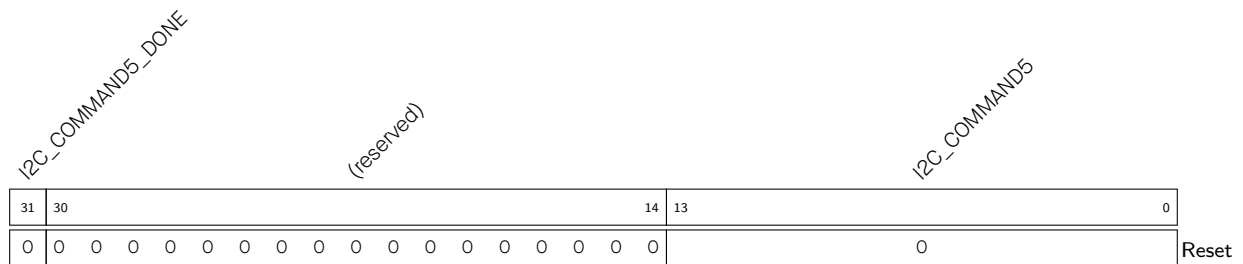
**I2C\_COMMAND4** Configures command 4. See details in I2C\_CMD0\_REG[13:0]. (R/W)

**I2C\_COMMAND4\_DONE** Represents whether command 4 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

**Register 39.30. I2C\_COMD5\_REG (0x006C)**

**I2C\_COMMAND5** Configures command 5. See details in I2C\_CMD0\_REG[13:0]. (R/W)

**I2C\_COMMAND5\_DONE** Represents whether command 5 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

I2C\_COMMAND6\_DONE

(reserved)

I2C\_COMMAND6

Reset

(R/W/SS)

I2C\_COMMAND7\_DONE

(reserved)

I2C\_COMMAND7

Reset

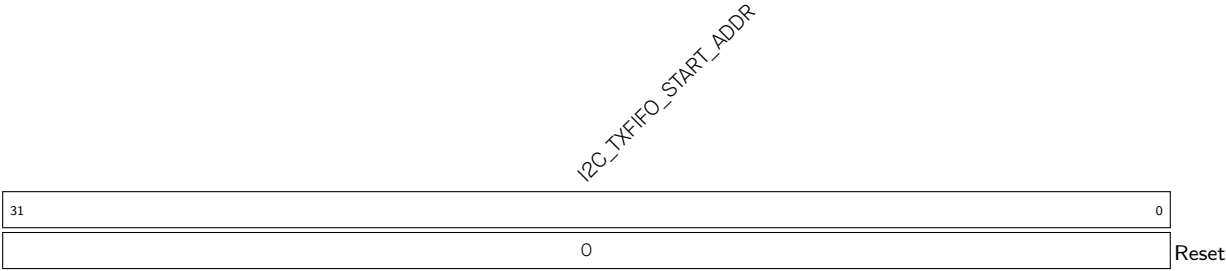
(R/W/SS)

## I2C\_DATE

Reset

PRELIMINARY

Register 39.34. I2C\_TXFIFO\_START\_ADDR\_REG (0x0100)



I2C\_TXFIFO\_START\_ADDR Represents the I2C TX FIFO first address. (HRO)

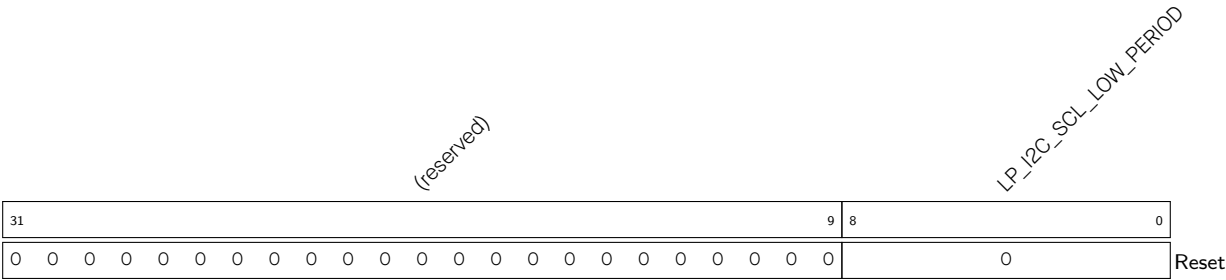
Register 39.35. I2C\_RXFIFO\_START\_ADDR\_REG (0x0180)



I2C\_RXFIFO\_START\_ADDR Represents the I2C RX FIFO first address. (HRO)

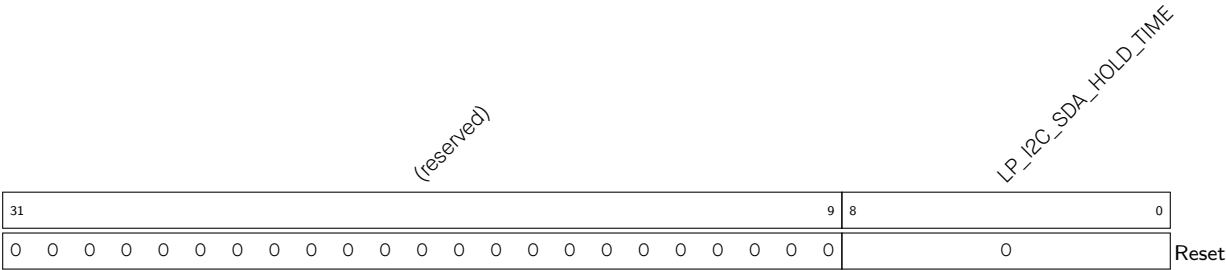
39.9.2 LP\_I2C Registers

Register 39.36. LP\_I2C\_SCL\_LOW\_PERIOD\_REG (0x0000)



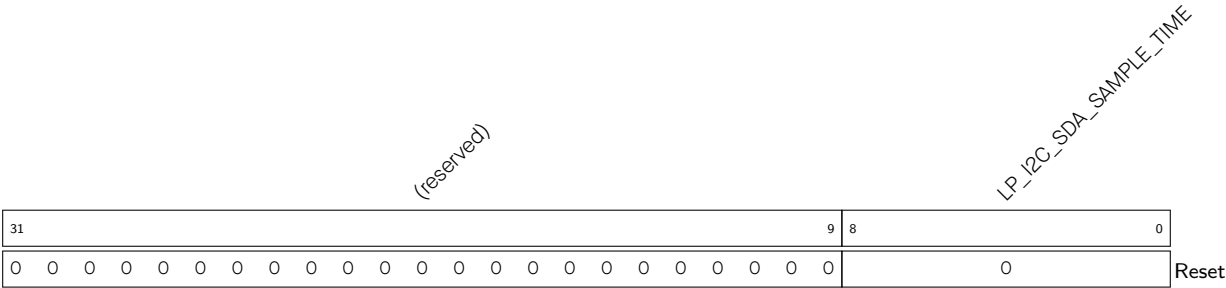
LP\_I2C\_SCL\_LOW\_PERIOD Configures the low level width of the SCL Clock in master mode.  
Measurement unit: i2c\_sclk  
(R/W)

Register 39.37. LP\_I2C\_SDA\_HOLD\_REG (0x0030)



**LP\_I2C\_SDA\_HOLD\_TIME** Configures the time to hold the data after the falling edge of SCL.  
Measurement unit: i2c\_sclk  
(R/W)

Register 39.38. LP\_I2C\_SDA\_SAMPLE\_REG (0x0034)



**LP\_I2C\_SDA\_SAMPLE\_TIME** Configures the time for sampling SDA.  
Measurement unit: i2c\_sclk  
(R/W)

**Register 39.39. LP\_I2C\_SCL\_HIGH\_PERIOD\_REG (0x0038)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                             |  |  |  |  |  |   |   |                        |  |  |  |   |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|-----------------------------|--|--|--|--|--|---|---|------------------------|--|--|--|---|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | LP_I2C_SCL_WAIT_HIGH_PERIOD |  |  |  |  |  |   |   | LP_I2C_SCL_HIGH_PERIOD |  |  |  |   |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                          |  |  |  |  |  |   | 9 | 8                      |  |  |  |   |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                           |  |  |  |  |  | 0 |   |                        |  |  |  | 0 |  |  |   |

Reset

**LP\_I2C\_SCL\_HIGH\_PERIOD** Configures for how long SCL remains high in master mode.

Measurement unit: i2c\_sclk

(R/W)

**LP\_I2C\_SCL\_WAIT\_HIGH\_PERIOD** Configures the SCL\_FSM's waiting period for SCL high level in master mode.

Measurement unit: i2c\_sclk

(R/W)

**Register 39.40. LP\_I2C\_SCL\_START\_HOLD\_REG (0x0040)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_I2C_SCL_START_HOLD_TIME |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                          |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                          |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

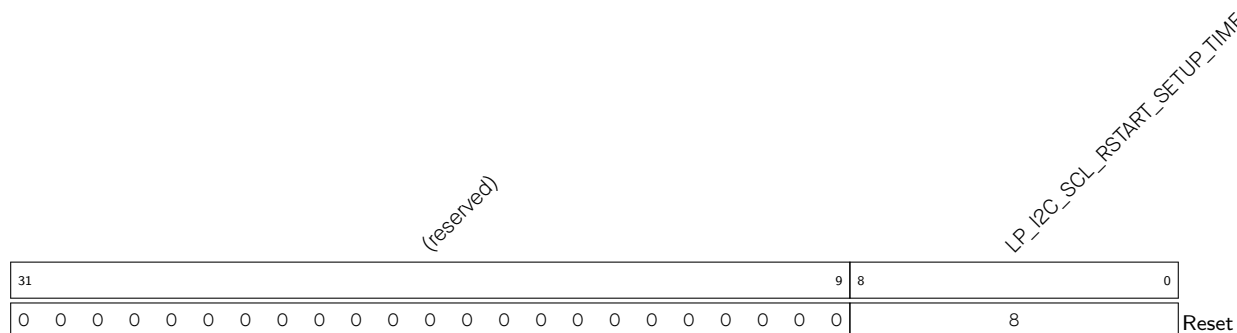
Reset

**LP\_I2C\_SCL\_START\_HOLD\_TIME** Configures the time between the falling edge of SDA and the falling edge of SCL for a START condition.

Measurement unit: i2c\_sclk

(R/W)

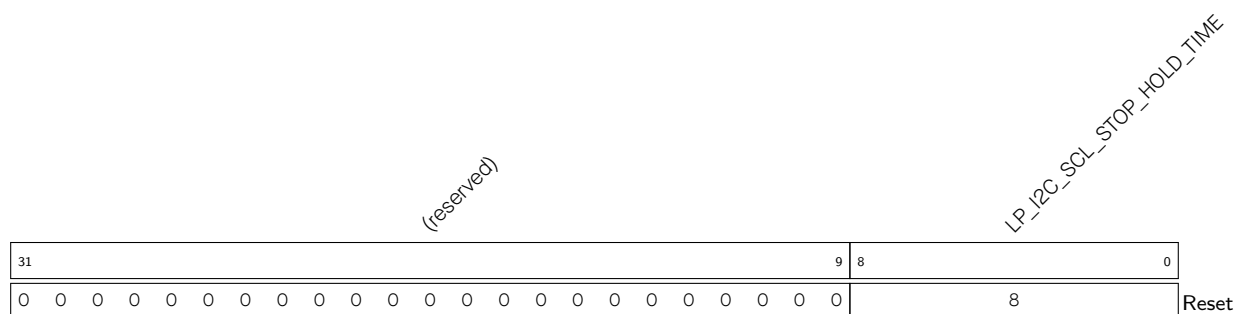


**Register 39.41. LP\_I2C\_SCL\_RSTART\_SETUP\_REG (0x0044)**

**LP\_I2C\_SCL\_RSTART\_SETUP\_TIME** Configures the time between the positive edge of SCL and the negative edge of SDA for a RESTART condition.

Measurement unit: i2c\_sclk

(R/W)

**Register 39.42. LP\_I2C\_SCL\_STOP\_HOLD\_REG (0x0048)**

**LP\_I2C\_SCL\_STOP\_HOLD\_TIME** Configures the delay after the STOP condition.

Measurement unit: i2c\_sclk

(R/W)

**Register 39.43. LP\_I2C\_SCL\_STOP\_SETUP\_REG (0x004C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_I2C_SCL_STOP_SETUP_TIME |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 9                          | 8 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                          |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**LP\_I2C\_SCL\_STOP\_SETUP\_TIME** Configures the time between the rising edge of SCL and the rising edge of SDA.

Measurement unit: i2c\_sclk

(R/W)

**Register 39.44. LP\_I2C\_SCL\_ST\_TIME\_OUT\_REG (0x0078)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_I2C_SCL_ST_TO_I2C |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5                    | 4 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x10                 |   |   |  |  |  |  |  | Reset |  |

**LP\_I2C\_SCL\_ST\_TO\_I2C** Configures the threshold value of SCL\_FSM state unchanged period. It should be no more than 23.

Measurement unit: i2c\_sclk

(R/W)

**Register 39.45. LP\_I2C\_SCL\_MAIN\_ST\_TIME\_OUT\_REG (0x007C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_I2C\_SCL\_MAIN\_ST\_TO\_I2C** Configures the threshold value of SCL\_MAIN\_FSM state unchanged period. It should be no more than 23.

Measurement unit: i2c\_sclk

(R/W)

Register 39.46. LP\_I2C\_CTR\_REG (0x0004)

|            |   |   |   |   |   |   |   |   |   |   |   |   |    |    |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|----|----|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | LP_I2C_CONF_UPGATE<br>LP_I2C_FSM_RST<br>LP_I2C_ARBITRATION_EN<br>LP_I2C_CLK_EN<br>LP_I2C_RX_LSB_FIRST<br>LP_I2C_TX_LSB_FIRST<br>(reserved)<br>LP_I2C_TRANS_START<br>LP_I2C_RX_FULL_ACK_LEVEL<br>(reserved)<br>LP_I2C_SAMPLE_SCL_LEVEL |    |    |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 12  | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_I2C\_SAMPLE\_SCL\_LEVEL** Configures the sample mode for SDA.

1: Sample SDA data on the SCL low level.

0: Sample SDA data on the SCL high level.

(R/W)

**LP\_I2C\_RX\_FULL\_ACK\_LEVEL** Configures the ACK value that needs to be sent by master when the rx\_fifo\_cnt has reached the threshold. (R/W)

**LP\_I2C\_TRANS\_START** Configures to start sending the data in txfifo for slave.

0: No effect

1: Start

(WT)

**LP\_I2C\_TX\_LSB\_FIRST** Configures to control the sending order for data to be sent.

1: send data from the least significant bit

0: send data from the most significant bit

(R/W)

**LP\_I2C\_RX\_LSB\_FIRST** Configures to control the storage order for received data.

1: receive data from the least significant bit

0: receive data from the most significant bit

(R/W)

**LP\_I2C\_CLK\_EN** Configures whether to gate clock signal for registers.

0: Support clock only when registers are read or written to by software

1: Force clock on for registers.

(R/W)

**LP\_I2C\_ARBITRATION\_EN** Configures to enable I2C bus arbitration detection.

0: No effect

1: Enable

(R/W)

**LP\_I2C\_FSM\_RST** Configures to reset the SCL\_FSM.

0: No effect

1: Reset

(WT)

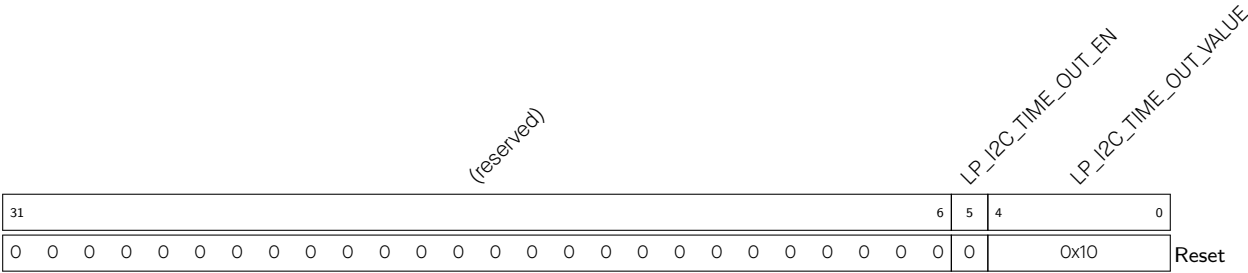
**LP\_I2C\_CONF\_UPGATE** Configures this bit for synchronization.

0: No effect

1: Synchronize

(WT)

Register 39.47. LP\_I2C\_TO\_REG (0x000C)



**LP\_I2C\_TIME\_OUT\_VALUE** Configures the timeout threshold period for SCL sticking at high or low level. The actual period is 2^(reg\_time\_out\_value).  
Measurement unit: i2c\_sclk.  
(R/W)

**LP\_I2C\_TIME\_OUT\_EN** Configures to enable time out control.  
0: No effect  
1: Enable  
(R/W)

Register 39.48. LP\_I2C\_FIFO\_CONF\_REG (0x0018)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |    |    |    |                    |    |     |   |                    |  |   |     |            |   |   |       |                   |  |  |   |                        |  |  |  |            |  |  |  |                        |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|----|----|----|--------------------|----|-----|---|--------------------|--|---|-----|------------|---|---|-------|-------------------|--|--|---|------------------------|--|--|--|------------|--|--|--|------------------------|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_I2C_FIFO_PRT_EN |    |    |    | LP_I2C_TX_FIFO_RST |    |     |   | LP_I2C_RX_FIFO_RST |  |   |     | (reserved) |   |   |       | LP_I2C_NONFIFO_EN |  |  |   | LP_I2C_TXFIFO_WM_THRHD |  |  |  | (reserved) |  |  |  | LP_I2C_RXFIFO_WM_THRHD |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                 | 14 | 13 | 12 | 11                 | 10 | 9   | 8 |                    |  |   |     | 5          | 4 | 3 |       |                   |  |  | 0 |                        |  |  |  |            |  |  |  |                        |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1                  | 0  | 0  | 0  | 0                  | 0  | 0x2 |   |                    |  | 0 | 0x6 |            |   |   | Reset |                   |  |  |   |                        |  |  |  |            |  |  |  |                        |  |  |  |

Reset

**LP\_I2C\_RXFIFO\_WM\_THRHD** Configures the water mark threshold of RXFIFO in nonfifo access mode. When LP\_I2C\_FIFO\_PRT\_EN is 1 and rx FIFO counter is bigger than LP\_I2C\_RXFIFO\_WM\_THRHD[4:0], LP\_I2C\_RXFIFO\_WM\_INT\_RAW bit will be valid. (R/W)

**LP\_I2C\_TXFIFO\_WM\_THRHD** Configures the water mark threshold of TXFIFO in nonfifo access mode. When LP\_I2C\_FIFO\_PRT\_EN is 1 and rx FIFO counter is bigger than LP\_I2C\_TXFIFO\_WM\_THRHD[4:0], LP\_I2C\_TXFIFO\_WM\_INT\_RAW bit will be valid. (R/W)

**LP\_I2C\_NONFIFO\_EN** Configures to enable APB nonfifo access. (R/W)

**LP\_I2C\_RX\_FIFO\_RST** Configures to reset RXFIFO.

0: No effect

1: Reset

(R/W)

**LP\_I2C\_TX\_FIFO\_RST** Configures to reset TXFIFO. 0: No effect

1: Reset

(R/W)

**LP\_I2C\_FIFO\_PRT\_EN** Configures to enable FIFO pointer in non-fifo access mode. This bit controls the valid bits and the TX/RX FIFO overflow, underflow, full and empty interrupts.

0: No effect

1: Enable

(R/W)

Register 39.49. LP\_I2C\_FILTER\_CFG\_REG (0x0050)

|            |   |   |   |   |   |   |   |   |   |                      |    |                      |   |                         |   |                         |   |
|------------|---|---|---|---|---|---|---|---|---|----------------------|----|----------------------|---|-------------------------|---|-------------------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   | LP_I2C_SDA_FILTER_EN |    | LP_I2C_SCL_FILTER_EN |   | LP_I2C_SDA_FILTER_THRES |   | LP_I2C_SCL_FILTER_THRES |   |
| 31         |   |   |   |   |   |   |   |   |   |                      | 10 | 9                    | 8 | 7                       | 4 | 3                       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0  | 0                    | 0 | 0                       | 0 | 0                       | 0 |
|            |   |   |   |   |   |   |   |   |   |                      |    | 1                    | 1 | 0                       |   | 0                       |   |

Reset

**LP\_I2C\_SCL\_FILTER\_THRES** Configures the threshold pulse width to be filtered on SCL. When a pulse on the SCL input has smaller width than this value, the I2C controller will ignore that pulse.

Measurement unit: i2c\_sclk

(R/W)

**LP\_I2C\_SDA\_FILTER\_THRES** Configures the threshold pulse width to be filtered on SDA. When a pulse on the SDA input has smaller width than this value, the I2C controller will ignore that pulse.

Measurement unit: i2c\_sclk

(R/W)

**LP\_I2C\_SCL\_FILTER\_EN** Configures to enable the filter function for SCL.

0: No effect

1: Enable

(R/W)

**LP\_I2C\_SDA\_FILTER\_EN** Configures to enable the filter function for SDA.

0: No effect

1: Enable

(R/W)

Register 39.50. LP\_I2C\_SCL\_SP\_CONF\_REG (0x0080)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |          |   |          |   |                        |   |   |   |                       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | reserved |   | reserved |   | LP_I2C_SCL_RST_SLV_NUM |   |   |   | LP_I2C_SCL_RST_SLV_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8        | 7 | 6        | 5 | 1                      |   |   |   | 0                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0        | 0 | 0        | 0 | 0                      | 0 | 0 | 0 | 0                     | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**LP\_I2C\_SCL\_RST\_SLV\_EN** Configures to send out SCL pulses when I2C master is IDLE. The number of pulses equals to LP\_I2C\_SCL\_RST\_SLV\_NUM[4:0]. (R/W/SC)

**LP\_I2C\_SCL\_RST\_SLV\_NUM** Configure the pulses of SCL generated in I2C master mode.

Valid when LP\_I2C\_SCL\_RST\_SLV\_EN is 1.

Measurement unit: i2c\_sclk

(R/W)

Register 39.51. LP\_I2C\_SR\_REG (0x0008)

|            |    |                       |    |            |    |                            |    |            |    |                   |    |            |   |                   |   |            |   |                 |   |                 |   |            |   |                 |  |
|------------|----|-----------------------|----|------------|----|----------------------------|----|------------|----|-------------------|----|------------|---|-------------------|---|------------|---|-----------------|---|-----------------|---|------------|---|-----------------|--|
| (reserved) |    | LP_I2C_SCL_STATE_LAST |    | (reserved) |    | LP_I2C_SCL_MAIN_STATE_LAST |    | (reserved) |    | LP_I2C_TXFIFO_CNT |    | (reserved) |   | LP_I2C_RXFIFO_CNT |   | (reserved) |   | LP_I2C_BUS_BUSY |   | LP_I2C_ARB_LOST |   | (reserved) |   | LP_I2C_RESP_REC |  |
| 31         | 30 | 28                    | 27 | 26         | 24 | 23                         | 22 | 18         | 17 | 13                | 12 | 8          | 7 | 5                 | 4 | 3          | 2 | 1               | 0 |                 |   |            |   |                 |  |
| 0          | 0  | 0                     | 0  | 0          | 0  | 0                          | 0  | 0          | 0  | 0                 | 0  | 0          | 0 | 0                 | 0 | 0          | 0 | 0               | 0 | 0               | 0 | 0          | 0 | 0               |  |
| Reset      |    |                       |    |            |    |                            |    |            |    |                   |    |            |   |                   |   |            |   |                 |   |                 |   |            |   |                 |  |

**LP\_I2C\_RESP\_REC** Represents the received ACK value in master mode or slave mode.

0: ACK

1: NACK

(RO)

**LP\_I2C\_ARB\_LOST** Represents whether the I2C controller loses control of SCL line.

0: No arbitration lost

1: Arbitration lost

(RO)

**LP\_I2C\_BUS\_BUSY** Represents the I2C bus state.

1: The I2C bus is busy transferring data

0: The I2C bus is in idle state

(RO)

**LP\_I2C\_RXFIFO\_CNT** Represents the number of data bytes received in RAM. (RO)

**LP\_I2C\_TXFIFO\_CNT** Represents the number of data bytes to be sent. (RO)

**LP\_I2C\_SCL\_MAIN\_STATE\_LAST** Represents the states of the I2C module state machine.

0: Idle

1: Address shift

2: ACK address

3: Rx data

4: Tx data

5: Send ACK

6: Wait ACK

(RO)

**LP\_I2C\_SCL\_STATE\_LAST** Represents the states of the state machine used to produce SCL.

0: Idle

1: Start

2: Negative edge

3: Low

4: Positive edge

5: High

6: Stop

(RO)

Register 39.52. LP\_I2C\_FIFO\_ST\_REG (0x0014)

Register map diagram showing bit fields for the I2C module. The register is 32 bits wide. Bit 31 is reserved. Bits 19-18 are LP\_I2C\_TXFIFO\_WADDR. Bits 15-14 are reserved. Bits 13-10 are LP\_I2C\_TXFIFO\_RADDR. Bit 9 is reserved. Bits 8-5 are LP\_I2C\_RXFIFO\_WADDR. Bit 4 is reserved. Bits 3-0 are LP\_I2C\_RXFIFO\_RADDR. Below the register map, a row of bits 0-31 is shown, with bits 0-3 labeled 'Reset'.

**LP\_I2C\_RXFIFO\_RADDR** Represents the offset address of the APB reading from RXFIFO (RO)

**LP\_I2C\_RXFIFO\_WADDR** Represents the offset address of i2c module receiving data and writing to RXFIFO. (RO)

**LP\_I2C\_TXFIFO\_RADDR** Represents the offset address of i2c module reading from TXFIFO. (RO)

**LP\_I2C\_TXFIFO\_WADDR** Represents the offset address of APB bus writing to TXFIFO. (RO)

### Register 39.53. LP\_I2C\_DATA\_REG (0x001C)

[illegible]

**LP\_I2C\_FIFO\_RDATA** Represents the value of RXFIFO read data. (RO)



Register 39.54. LP\_I2C\_INT\_RAW\_REG (0x0020)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_I2C_DET_START_INT_RAW<br>LP_I2C_SCL_MAIN_ST_TO_INT_RAW<br>LP_I2C_SCL_ST_TO_INT_RAW<br>LP_I2C_RXFIFO_UDF_INT_RAW<br>LP_I2C_NACK_INT_RAW<br>LP_I2C_TRANS_START_INT_RAW<br>LP_I2C_TIME_OUT_INT_RAW<br>LP_I2C_TRANS_COMPLETE_INT_RAW<br>LP_I2C_ARBTRATION_LOST_INT_RAW<br>LP_I2C_BYTE_TRANS_DONE_INT_RAW<br>LP_I2C_END_DETECT_INT_RAW<br>LP_I2C_RXFIFO_OVF_INT_RAW<br>LP_I2C_RXFIFO_WM_INT_RAW |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Reset |

**LP\_I2C\_RXFIFO\_WM\_INT\_RAW** The raw interrupt status of LP\_I2C\_RXFIFO\_WM\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_TXFIFO\_WM\_INT\_RAW** The raw interrupt status of LP\_I2C\_TXFIFO\_WM\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_RXFIFO\_OVF\_INT\_RAW** The raw interrupt status of LP\_I2C\_RXFIFO\_OVF\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_END\_DETECT\_INT\_RAW** The raw interrupt status of the LP\_I2C\_END\_DETECT\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_BYTE\_TRANS\_DONE\_INT\_RAW** The raw interrupt status of the LP\_I2C\_END\_DETECT\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_ARBTRATION\_LOST\_INT\_RAW** The raw interrupt status of the LP\_I2C\_ARBTRATION\_LOST\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_MST\_TXFIFO\_UDF\_INT\_RAW** The raw interrupt status of LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_TRANS\_COMPLETE\_INT\_RAW** The raw interrupt status of the LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_TIME\_OUT\_INT\_RAW** The raw interrupt status of the LP\_I2C\_TIME\_OUT\_INT interrupt. (R/SS/WTC)

Continued on the next page...

**Register 39.54. LP\_I2C\_INT\_RAW\_REG (0x0020)**

Continued from the previous page...

**LP\_I2C\_TRANS\_START\_INT\_RAW** The raw interrupt status of the LP\_I2C\_TRANS\_START\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_NACK\_INT\_RAW** The raw interrupt status of LP\_I2C\_SLAVE\_STRETCH\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_TXFIFO\_OVF\_INT\_RAW** The raw interrupt status of LP\_I2C\_TXFIFO\_OVF\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_RXFIFO\_UDF\_INT\_RAW** The raw interrupt status of LP\_I2C\_RXFIFO\_UDF\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_SCL\_ST\_TO\_INT\_RAW** The raw interrupt status of LP\_I2C\_SCL\_ST\_TO\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT\_RAW** The raw interrupt status of LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (R/SS/WTC)

**LP\_I2C\_DET\_START\_INT\_RAW** The raw interrupt status of LP\_I2C\_DET\_START\_INT interrupt. (R/SS/WTC)

Register 39.55. LP\_I2C\_INT\_CLR\_REG (0x0024)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_I2C_DET_START_INT_CLR<br>LP_I2C_SCL_MAIN_ST_TO_INT_CLR<br>LP_I2C_SCL_ST_TO_INT_CLR<br>LP_I2C_RXFIFO_UDF_INT_CLR<br>LP_I2C_TXFIFO_OVF_INT_CLR<br>LP_I2C_NACK_INT_CLR<br>LP_I2C_TRANS_START_INT_CLR<br>LP_I2C_TIME_OUT_INT_CLR<br>LP_I2C_TRANS_COMPLETE_INT_CLR<br>LP_I2C_MST_TXFIFO_UDF_INT_CLR<br>LP_I2C_ARBITRATION_LOST_INT_CLR<br>LP_I2C_BYTE_TRANS_DONE_INT_CLR<br>LP_I2C_END_DETECT_INT_CLR<br>LP_I2C_RXFIFO_WM_INT_CLR<br>LP_I2C_TXFIFO_WM_INT_CLR |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

**LP\_I2C\_RXFIFO\_WM\_INT\_CLR** Write 1 to clear LP\_I2C\_RXFIFO\_WM\_INT interrupt. (WT)

**LP\_I2C\_TXFIFO\_WM\_INT\_CLR** Write 1 to clear LP\_I2C\_TXFIFO\_WM\_INT interrupt. (WT)

**LP\_I2C\_RXFIFO\_OVF\_INT\_CLR** Write 1 to clear LP\_I2C\_RXFIFO\_OVF\_INT interrupt. (WT)

**LP\_I2C\_END\_DETECT\_INT\_CLR** Write 1 to clear the LP\_I2C\_END\_DETECT\_INT interrupt. (WT)

**LP\_I2C\_BYTE\_TRANS\_DONE\_INT\_CLR** Write 1 to clear the LP\_I2C\_END\_DETECT\_INT interrupt. (WT)

**LP\_I2C\_ARBITRATION\_LOST\_INT\_CLR** Write 1 to clear the LP\_I2C\_ARBITRATION\_LOST\_INT interrupt. (WT)

**LP\_I2C\_MST\_TXFIFO\_UDF\_INT\_CLR** Write 1 to clear LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (WT)

**LP\_I2C\_TRANS\_COMPLETE\_INT\_CLR** Write 1 to clear the LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (WT)

**LP\_I2C\_TIME\_OUT\_INT\_CLR** Write 1 to clear the LP\_I2C\_TIME\_OUT\_INT interrupt. (WT)

**LP\_I2C\_TRANS\_START\_INT\_CLR** Write 1 to clear the LP\_I2C\_TRANS\_START\_INT interrupt. (WT)

**LP\_I2C\_NACK\_INT\_CLR** Write 1 to clear LP\_I2C\_SLAVE\_STRETCH\_INT interrupt. (WT)

**LP\_I2C\_TXFIFO\_OVF\_INT\_CLR** Write 1 to clear LP\_I2C\_TXFIFO\_OVF\_INT interrupt. (WT)

**LP\_I2C\_RXFIFO\_UDF\_INT\_CLR** Write 1 to clear LP\_I2C\_RXFIFO\_UDF\_INT interrupt. (WT)

**LP\_I2C\_SCL\_ST\_TO\_INT\_CLR** Write 1 to clear LP\_I2C\_SCL\_ST\_TO\_INT interrupt. (WT)

**LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT\_CLR** Write 1 to clear LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (WT)

**LP\_I2C\_DET\_START\_INT\_CLR** Write 1 to clear LP\_I2C\_DET\_START\_INT interrupt. (WT)

## Register 39.56. LP\_I2C\_INT\_ENA\_REG (0x0028)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|---|---|---|-------|---|---|---|---|---|---|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_I2C_DET_START_INT_ENA<br>LP_I2C_SCL_MAIN_ST_TO_INT_ENA<br>LP_I2C_SCL_ST_TO_INT_ENA<br>LP_I2C_RXFIFO_UDF_INT_ENA<br>LP_I2C_TXFIFO_OVF_INT_ENA<br>LP_I2C_NACK_INT_ENA<br>LP_I2C_TRANS_START_INT_ENA<br>LP_I2C_TRANS_OUT_INT_ENA<br>LP_I2C_MST_TXFIFO_UDF_INT_ENA<br>LP_I2C_TRANS_COMPLETE_INT_ENA<br>LP_I2C_BYTE_TRANS_DONE_INT_ENA<br>LP_I2C_END_DETECT_INT_ENA<br>LP_I2C_RXFIFO_WM_INT_ENA<br>LP_I2C_TXFIFO_WM_INT_ENA |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6     | 5 | 4 | 3 | 2 | 1 | 0 |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | Reset |   |   |   |   |   |   |  |  |

**LP\_I2C\_RXFIFO\_WM\_INT\_ENA** Write 1 to enable LP\_I2C\_RXFIFO\_WM\_INT interrupt. (R/W)

**LP\_I2C\_TXFIFO\_WM\_INT\_ENA** Write 1 to enable LP\_I2C\_TXFIFO\_WM\_INT interrupt. (R/W)

**LP\_I2C\_RXFIFO\_OVF\_INT\_ENA** Write 1 to enable LP\_I2C\_RXFIFO\_OVF\_INT interrupt. (R/W)

**LP\_I2C\_END\_DETECT\_INT\_ENA** Write 1 to enable the LP\_I2C\_END\_DETECT\_INT interrupt. (R/W)

**LP\_I2C\_BYTE\_TRANS\_DONE\_INT\_ENA** Write 1 to enable the LP\_I2C\_END\_DETECT\_INT interrupt. (R/W)

**LP\_I2C\_ARBITRATION\_LOST\_INT\_ENA** Write 1 to enable the LP\_I2C\_ARBITRATION\_LOST\_INT interrupt. (R/W)

**LP\_I2C\_MST\_TXFIFO\_UDF\_INT\_ENA** Write 1 to enable LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (R/W)

**LP\_I2C\_TRANS\_COMPLETE\_INT\_ENA** Write 1 to enable the LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (R/W)

**LP\_I2C\_TIME\_OUT\_INT\_ENA** Write 1 to enable the LP\_I2C\_TIME\_OUT\_INT interrupt. (R/W)

**LP\_I2C\_TRANS\_START\_INT\_ENA** Write 1 to enable the LP\_I2C\_TRANS\_START\_INT interrupt. (R/W)

**LP\_I2C\_NACK\_INT\_ENA** Write 1 to enable LP\_I2C\_SLAVE\_STRETCH\_INT interrupt. (R/W)

**LP\_I2C\_TXFIFO\_OVF\_INT\_ENA** Write 1 to enable LP\_I2C\_TXFIFO\_OVF\_INT interrupt. (R/W)

**LP\_I2C\_RXFIFO\_UDF\_INT\_ENA** Write 1 to enable LP\_I2C\_RXFIFO\_UDF\_INT interrupt. (R/W)

**LP\_I2C\_SCL\_ST\_TO\_INT\_ENA** Write 1 to enable LP\_I2C\_SCL\_ST\_TO\_INT interrupt. (R/W)

**LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT\_ENA** Write 1 to enable LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (R/W)

**LP\_I2C\_DET\_START\_INT\_ENA** Write 1 to enable LP\_I2C\_DET\_START\_INT interrupt. (R/W)

Register 39.57. LP\_I2C\_INT\_STATUS\_REG (0x002C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LP_I2C_DET_START_INT_ST<br>LP_I2C_SCL_MAIN_ST_TO_INT_ST<br>LP_I2C_SCL_ST_TO_INT_ST<br>LP_I2C_RXFIFO_UDF_INT_ST<br>LP_I2C_TXFIFO_UDF_INT_ST<br>LP_I2C_NACK_INT_ST<br>LP_I2C_TRANS_START_INT_ST<br>LP_I2C_TIME_OUT_INT_ST<br>LP_I2C_TRANS_COMPLETE_INT_ST<br>LP_I2C_ARBTRATION_LOST_INT_ST<br>LP_I2C_BYTE_TRANS_DONE_INT_ST<br>LP_I2C_END_DETECT_INT_ST<br>LP_I2C_RXFIFO_OVF_INT_ST<br>LP_I2C_TXFIFO_WM_INT_ST |    |    |    |    |    |    |   |   |   |   |   |   |   |   |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1     | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |

**LP\_I2C\_RXFIFO\_WM\_INT\_ST** The masked interrupt status of LP\_I2C\_RXFIFO\_WM\_INT interrupt. (RO)

**LP\_I2C\_TXFIFO\_WM\_INT\_ST** The masked interrupt status of LP\_I2C\_TXFIFO\_WM\_INT interrupt. (RO)

**LP\_I2C\_RXFIFO\_OVF\_INT\_ST** The masked interrupt status of LP\_I2C\_RXFIFO\_OVF\_INT interrupt. (RO)

**LP\_I2C\_END\_DETECT\_INT\_ST** The masked interrupt status of the LP\_I2C\_END\_DETECT\_INT interrupt. (RO)

**LP\_I2C\_BYTE\_TRANS\_DONE\_INT\_ST** The masked interrupt status of the LP\_I2C\_END\_DETECT\_INT interrupt. (RO)

**LP\_I2C\_ARBTRATION\_LOST\_INT\_ST** The masked interrupt status of the LP\_I2C\_ARBTRATION\_LOST\_INT interrupt. (RO)

**LP\_I2C\_MST\_TXFIFO\_UDF\_INT\_ST** The masked interrupt status of LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (RO)

**LP\_I2C\_TRANS\_COMPLETE\_INT\_ST** The masked interrupt status of the LP\_I2C\_TRANS\_COMPLETE\_INT interrupt. (RO)

**LP\_I2C\_TIME\_OUT\_INT\_ST** The masked interrupt status of the LP\_I2C\_TIME\_OUT\_INT interrupt. (RO)

**LP\_I2C\_TRANS\_START\_INT\_ST** The masked interrupt status of the LP\_I2C\_TRANS\_START\_INT interrupt. (RO)

Continued on the next page...

**Register 39.57. LP\_I2C\_INT\_STATUS\_REG (0x002C)**

Continued from the previous page...

**LP\_I2C\_NACK\_INT\_ST** The masked interrupt status of LP\_I2C\_SLAVE\_STRETCH\_INT interrupt. (RO)

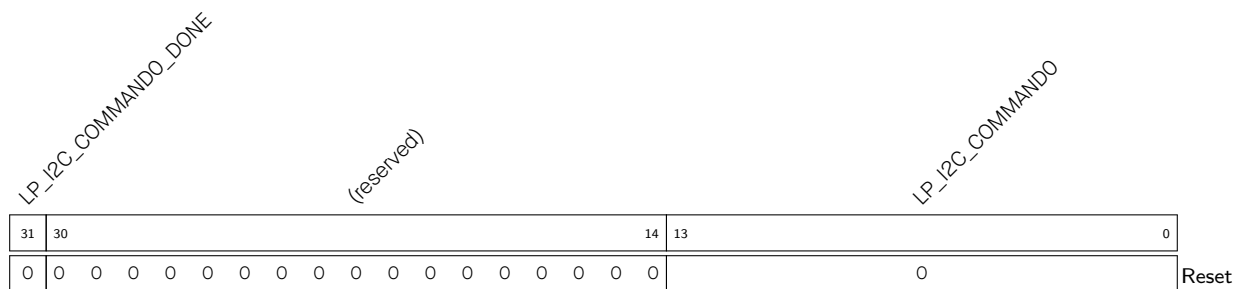
**LP\_I2C\_TXFIFO\_OVF\_INT\_ST** The masked interrupt status of LP\_I2C\_TXFIFO\_OVF\_INT interrupt. (RO)

**LP\_I2C\_RXFIFO\_UDF\_INT\_ST** The masked interrupt status of LP\_I2C\_RXFIFO\_UDF\_INT interrupt. (RO)

**LP\_I2C\_SCL\_ST\_TO\_INT\_ST** The masked interrupt status of LP\_I2C\_SCL\_ST\_TO\_INT interrupt. (RO)

**LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT\_ST** The masked interrupt status of LP\_I2C\_SCL\_MAIN\_ST\_TO\_INT interrupt. (RO)

**LP\_I2C\_DET\_START\_INT\_ST** The masked interrupt status of LP\_I2C\_DET\_START\_INT interrupt. (RO)

**Register 39.58. LP\_I2C\_CMD0\_REG (0x0058)**

**LP\_I2C\_COMMAND0** Configures command 0.

It consists of three parts:

op\_code is the command

1: WRITE

2: STOP

3: READ

4: END

6: RSTART

Byte\_num represents the number of bytes that need to be sent or received.

ack\_check\_en, ack\_exp and ack are used to control the ACK bit. See I2C cmd structure [39.4-2](#) for more information. (R/W)

**LP\_I2C\_COMMAND0\_DONE** Represents whether command 0 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

LP\_I2C\_COMMAND1\_DONE

(reserved)

LP\_I2C\_COMMAND1

Reset

(R/W/SS)

LP\_I2C\_COMMAND2\_DONE

(reserved)

LP\_I2C\_COMMAND2

Reset

(R/W/SS)

LP\_I2C\_COMMAND3\_DONE

(reserved)

LP\_I2C\_COMMAND3

Reset

(R/W/SS)

LP\_I2C\_COMMAND4\_DONE

(reserved)

LP\_I2C\_COMMAND4

Reset

(R/W/SS)



Register 39.63. LP\_I2C\_COMMD5\_REG (0x006C)

|    |    |    |    |   |
|----|----|----|----|---|
| 31 | 30 | 14 | 13 | 0 |
| 0  | 0  | 0  | 0  | 0 |

LP\_I2C\_COMMAND5\_DONE (reserved) LP\_I2C\_COMMAND5

Reset

**LP\_I2C\_COMMAND5** Configures command 5. See details in I2C\_CMD0\_REG[13:0]. (R/W)

**LP\_I2C\_COMMAND5\_DONE** Represents whether command 5 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

### Register 39.64. LP\_I2C\_COMD6\_REG (0x0070)

|    |    |    |    |   |
|----|----|----|----|---|
| 31 | 30 | 14 | 13 | 0 |
| 0  | 0  | 0  | 0  | 0 |

LP\_I2C\_COMMAND6\_DONE (reserved) LP\_I2C\_COMMAND6 Reset

**LP\_I2C\_COMMAND6** Configures command 6. See details in I2C\_CMD0\_REG[13:0]. (R/W)

**LP\_I2C\_COMMAND6\_DONE** Represents whether command 6 is done in I2C Master mode.

0: Not done

1: Done

(R/W/SS)

LP\_I2C\_COMMAND7\_DONE

(reserved)

LP\_I2C\_COMMAND7

Reset

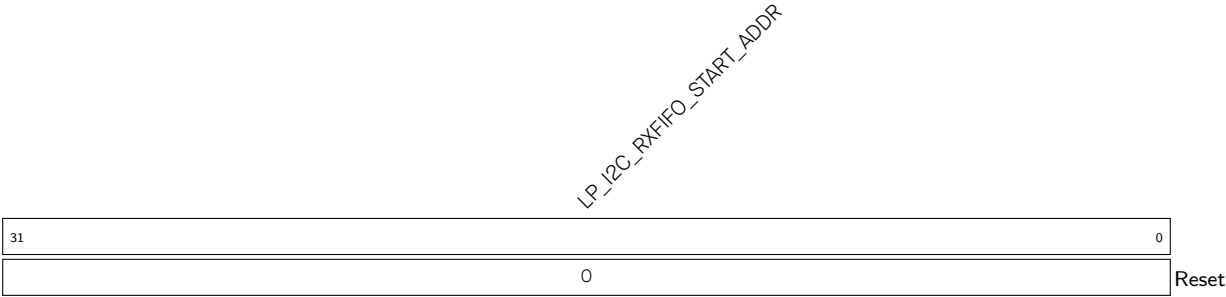
LP\_I2C\_DATE

Reset

LP\_I2C\_TXFIFO\_START\_ADDR

Reset

Register 39.68. LP\_I2C\_RXFIFO\_START\_ADDR\_REG (0x0180)



LP\_I2C\_RXFIFO\_START\_ADDR Represents the I2C rxfifo first address. (HRO)

## Chapter 40

### Analog I2C Controller

#### 40.1 Introduction

The Analog I2C Controller contains two I2C masters dedicated to configuring and communicating with certain analog circuit modules. Those modules can adjust their operating states by configuring their internal registers to better suit the current application scenario of the chip. For example, the Analog I2C Controller can configure an analog sensor to add a uniform offset to the ADC sampling values, thereby extending the sampling voltage range. Each configurable analog module has an I2C slave internally, which is assigned with an independent address. The Analog I2C Controller supports the configuration of the following analog modules:

- CPU\_PLL: This mainly includes the configuration register for CPLL\_CLK, with a slave address of 0x67. For more information on CPLL\_CLK, refer to Chapter [9 Reset and Clock](#).
- SYS\_PLL: This mainly includes the configuration register for SPLL\_CLK, with a slave address of 0x66. For more information on SPLL\_CLK, refer to Chapter [9 Reset and Clock](#).
- MSPI: This mainly includes the configuration register for MPLL\_CLK, with a slave address of 0x63. For more information on MPLL\_CLK, refer to Chapter [9 Reset and Clock](#).
- PLLA: This mainly includes the configuration register for APLL\_CLK, with a slave address of 0x6f. For more information on APLL\_CLK, refer to Chapter [9 Reset and Clock](#).
- ANA\_SENSOR: This mainly includes the configuration register for analog sensors (such as [Temperature Sensor \(TSENS\)](#) and [ADC Controller \(ADC\)](#)), with a slave address of 0x69.
- BIAS: This mainly includes the voltage detection configuration register, with a slave address of 0x6a. For more information, refer to Chapter [21 Brown-out Detector](#).

#### 40.2 Feature List

The Analog I2C Controller has the following features:

- Master mode only
- 7-bit addressing
- Adjustable transmission rate
- Communication in the sleep modes supported by the Low-Power CPU
- Dual master operation mode

## 40.3 Architectural Overview

The figure below shows the architecture of the Analog I2C Controller.

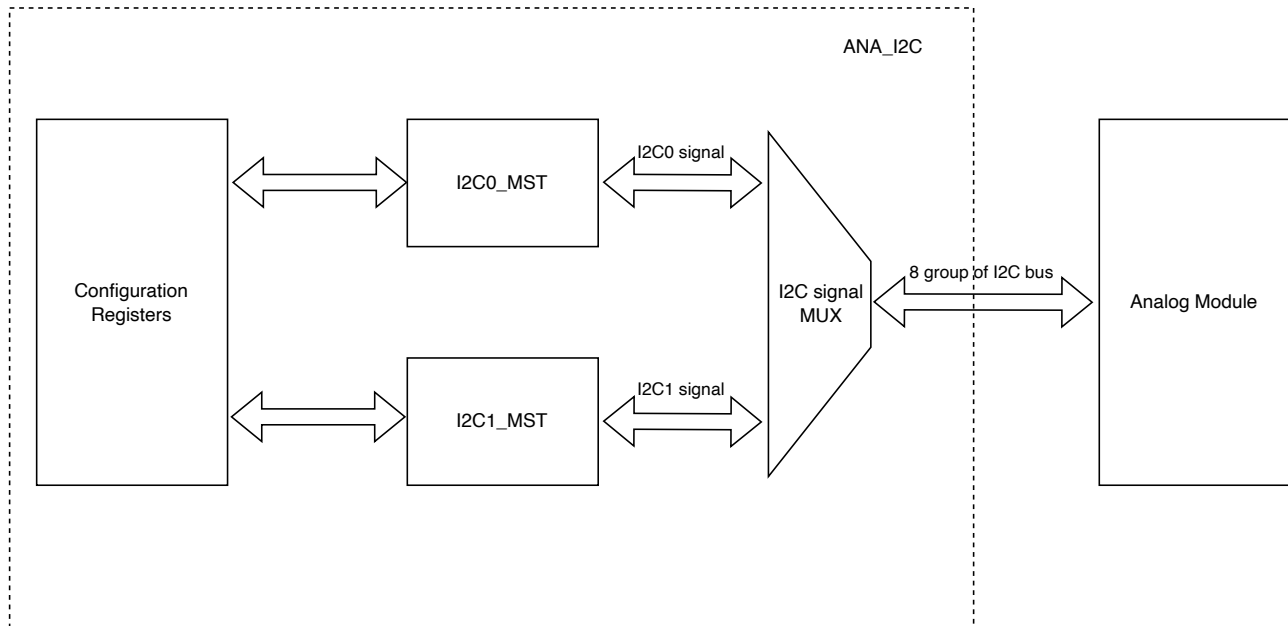


Figure 40.3-1. Analog I2C Controller Architecture

- **Configuration Registers:** A register module interfacing with the software, providing relevant configurations for the operation of the I2C master. This module controls the transmission address, data, etc., and monitors this transmission process by reading the status registers of I2C0/1\_MST.
- **I2C0/1\_MST:** Two I2C masters that can independently configure analog modules in parallel. The I2C signals they generate will be selected by a subsequent MUX and output to the analog modules.
- **I2C signal MUX:** A module that determines which analog master, I2C0\_MST or I2C1\_MST, configures a particular analog module.

## 40.4 Functional Description

### Transmission Rate Adjustment

The transmission rate and signal phase of the I2C signal can be configured by [ANA\\_I2C\\_MST\\_I2Cx\\_SDA\\_SIDE\\_GUARD](#) and [ANA\\_I2C\\_MST\\_I2Cx\\_SCL\\_PULSE\\_DUR](#). The relationship between the register values and the waveform is shown in the following figure.

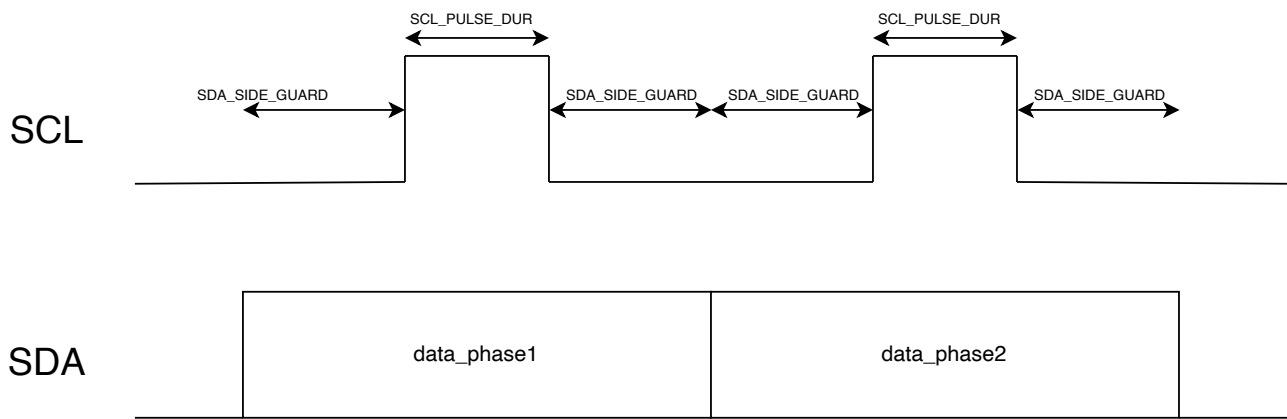


Figure 40.4-1. Signal Phase

### Operation in Sleep Modes

In chip sleep modes, the operation of the Analog I2C Controller can be driven by the Low-Power CPU (see Chapter 2 [Low-Power CPU](#)).

### Dual Master Operation Mode

The module integrates two independent master modules, each with its own set of configurations. The two masters can operate independently, configuring different analog modules, thereby improving operational efficiency.

## 40.5 Programming Procedures

The following is the process for configuring analog modules using the Analog I2C Controller.

- Write 1 to `LPPERI_CK_EN_LP_I2CMST` to enable the clock of the Controller.
- Configure `ANA_I2C_MST_ANA_CONF2` to select the module for communication.
- Configure `ANA_I2C_MST_I2Cx_SDA_SIDE_GUARD` and `ANA_I2C_MST_I2Cx_SCL_PULSE_DUR` to determine the transmission rate and signal phase of the I2C signal.
- Configure `ANA_I2C_MST_I2Cx_CTRL` to select relevant information for the current communication.
- Read `ANA_I2C_MST_I2Cx_BUSY`. A low state indicates the end of the current communication for I2Cx.

## 40.6 Register Summary

The addresses in this section are relative to Analog I2C Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                       | Description  | Address | Access |
|--|--|---------|--------|
| <b>Configuration Registers</b>             |  |         |        |
| <a href="#">ANA_I2C_MST_I2CO_CTRL_REG</a>  | I2C0 transmission configuration register                       | 0x0000  | varies |
| <a href="#">ANA_I2C_MST_I2C1_CTRL_REG</a>  | I2C1 transmission configuration register                       | 0x0004  | varies |
| <a href="#">ANA_I2C_MST_ANA_CONF2_REG</a>  | I2C master selection register                                  | 0x0020  | varies |
| <a href="#">ANA_I2C_MST_I2CO_CTRL1_REG</a> | I2C0 transmission rate and signal phase configuration register | 0x0024  | R/W    |
| <a href="#">ANA_I2C_MST_I2C1_CTRL1_REG</a> | I2C1 transmission rate and signal phase configuration register | 0x0028  | R/W    |
| <a href="#">ANA_I2C_MST_DATE_REG</a>       | Version control register                                       | 0x0038  | R/W    |

## 40.7 Registers

The addresses in this section are relative to Analog I2C Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program registers that contain reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 40.1. ANA\_I2C\_MST\_I2CO\_CTRL\_REG (0x0000)

|            |   |   |   |   |   |    |                       |         |  |  |  |  |  |                       |  |  |  |  |       |   |
|------------|---|---|---|---|---|----|-----------------------|---------|--|--|--|--|--|-----------------------|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |    | ANA_I2C_MST_I2CO_BUSY |         |  |  |  |  |  | ANA_I2C_MST_I2CO_CTRL |  |  |  |  |       |   |
| 31         |   |   |   |   |   | 26 | 25                    | 24      |  |  |  |  |  |                       |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0  | 0                     | 0x00000 |  |  |  |  |  |                       |  |  |  |  | Reset |   |

**ANA\_I2C\_MST\_I2CO\_CTRL** Configures the transmission information for I2CO.

- Bit[0:7]: Configures the slave address
- Bit[8:15]: Configures the slave register address
- Bit[16:23]: Configures the transmitted data
- Bit[24]: Configures the read or write operation
- 0: Write
- 1: Read

Once this register is configured, the I2CO master will generate I2C read or write signals.

(R/W)

**ANA\_I2C\_MST\_I2CO\_BUSY** Represents whether I2CO is currently transferring data.

- 0: I2CO is not transferring data
- 1: I2CO is transferring data

(RO)



Register 40.2. ANA\_I2C\_MST\_I2C1\_CTRL\_REG (0x0004)

|            |    |   |   |   |   |                       |         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |   |       |  |  |  |  |  |  |  |  |
|------------|----|---|---|---|---|-----------------------|---------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|---|-------|--|--|--|--|--|--|--|--|
| (reserved) |    |   |   |   |   | ANA_I2C_MST_I2C1_BUSY |         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ANA_I2C_MST_I2C1_CTRL |  |  |  |  |  |   |       |  |  |  |  |  |  |  |  |
| 31         | 26 |   |   |   |   | 25                    | 24      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  | 0 |       |  |  |  |  |  |  |  |  |
| 0          | 0  | 0 | 0 | 0 | 0 | 0                     | 0x00000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |   | Reset |  |  |  |  |  |  |  |  |

**ANA\_I2C\_MST\_I2C1\_CTRL** Configures the transmission information for I2C1. Its subfields have the same meaning with [ANA\\_I2C\\_MST\\_I2CO\\_CTRL](#). (R/W)

**ANA\_I2C\_MST\_I2C1\_BUSY** Represents whether I2C1 is currently transferring data

0: I2C1 is not transferring data

1: I2C1 is transferring data

(RO)

Register 40.3. ANA\_I2C\_MST\_ANA\_CONF2\_REG (0x0020)

|          |    |  |  |  |  |        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                       |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|----------|----|--|--|--|--|--------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|-----------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| reserved |    |  |  |  |  |        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | ANA_I2C_MST_ANA_CONF2 |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31       | 24 |  |  |  |  |        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 23 |                       |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x0      |    |  |  |  |  | 0x0000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                       |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**ANA\_I2C\_MST\_ANA\_CONF2** Configures which I2C master the following analog modules uses. If the corresponding bit is set to 1, I2C0 master is used for communication; if set to 0, I2C1 master is used. Since the slave address has already been defined, erroneous communication will not be caused.

Bit5: SYS\_PLL

Bit6: SDIO\_PLL

Bit7: ANA\_SENSOR

Bit8: PLLA

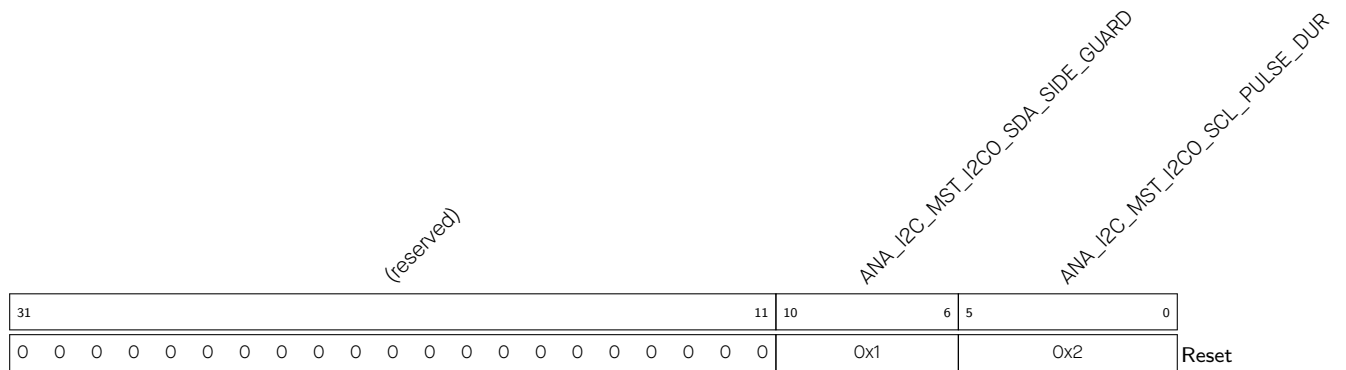
Bit9: MSPI

Bit10: DIG\_REG

Bit11: CPU\_PLL

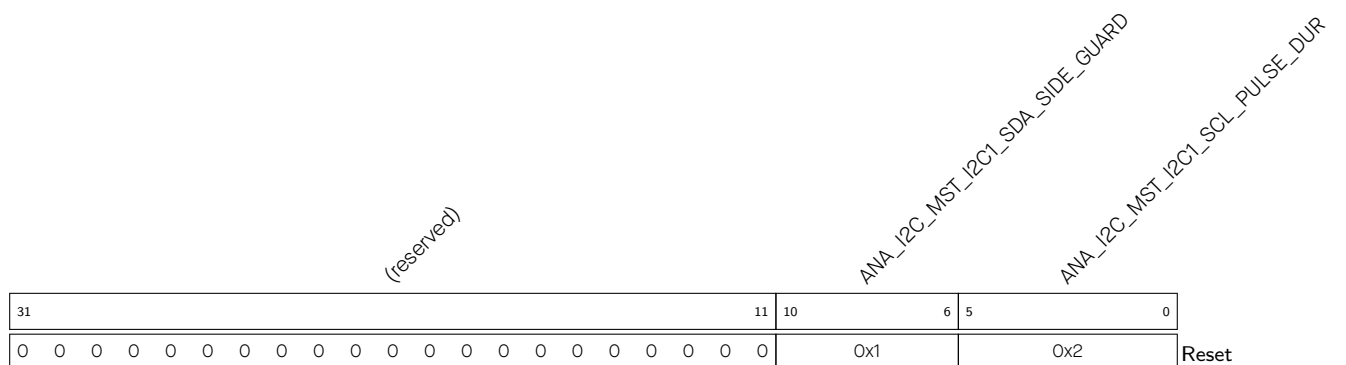
Bit12: BIAS

(R/W)

**Register 40.4. ANA\_I2C\_MST\_I2CO\_CTRL1\_REG (0x0024)**

**ANA\_I2C\_MST\_I2CO\_SCL\_PULSE\_DUR** Configures the duration of the high-level period of the SCL driven by I2CO. The duration is measured by the counter operating on the LP\_FAST\_CLK clock. (R/W)

**ANA\_I2C\_MST\_I2CO\_SDA\_SIDE\_GUARD** Configures the duration of the low-level period of the SCL driven by I2CO. The duration is measured by the counter operating on the LP\_FAST\_CLK clock. (R/W)

**Register 40.5. ANA\_I2C\_MST\_I2C1\_CTRL1\_REG (0x0028)**

**ANA\_I2C\_MST\_I2C1\_SCL\_PULSE\_DUR** Configures the duration of the high-level period of the SCL driven by I2C1. The duration is measured by the counter operating on the LP\_FAST\_CLK clock. (R/W)

**ANA\_I2C\_MST\_I2C1\_SDA\_SIDE\_GUARD** Configures the duration of the low-level period of the SCL driven by I2C1. The duration is measured by the counter operating on the LP\_FAST\_CLK clock. (R/W)

Register 40.6. ANA\_I2C\_MST\_DATE\_REG (0x0038)

|            |    |    |    |                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|----|----|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |    |    | ANA_I2C_MST_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 29 | 28 | 27 | 0                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0  | 0  | 0  | 0x2201300        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

ANA\_I2C\_MST\_DATE Version control register. (R/W)

# Chapter 41

## I2S Controller (I2S)

### 41.1 Overview

ESP32-P4 has three built-in I2S interfaces (i.e., I2S0, I2S1, and I2S2), which provide flexible communication interfaces for streaming digital data in multimedia applications, especially digital audio applications.

The I2S standard bus defines three signals, namely, a bit clock signal (BCK), a channel/word select signal (WS), and a serial data signal (SD). A basic I2S data bus has one master and one slave. The roles remain unchanged throughout the communication. The I2S module on ESP32-P4 provides separate transmit (TX) and receive (RX) units for high performance.

**Note:**

The information provided in this chapter applies to I2S0, I2S1, and I2S2. Unless otherwise indicated, I2S or I2S<sub>n</sub> in this chapter refer to I2S0, I2S1, and I2S2.

### 41.2 Terminology

To better illustrate the functionality of I2S, the following terms are used in this chapter.

|                                       |  |
|---------------------------------------|--|
| <b>Master mode</b>                    | As a master, I2S <sub>n</sub> drives BCK/WS signals and transmits data to or receives data from a slave.   |
| <b>Slave mode</b>                     | As a slave, I2S <sub>n</sub> is driven by BCK/WS signals and receives data from or transmits data to a master.   |
| <b>Full-duplex</b>                    | There are two separate data lines. The transmitted and received data is carried simultaneously.  |
| <b>Half-duplex</b>                    | Only one side, the master or the slave, transmits data first, and the other side receives data. Data transmission and reception cannot occur simultaneously.   |
| <b>A-law and <math>\mu</math>-law</b> | A-law and $\mu$ -law are compression/decompression algorithms in digital pulse code modulated (PCM) non-uniform quantization, which can effectively improve the signal-to-quantization noise ratio.  |
| <b>TDM RX mode</b>                    | In this mode, pulse code modulated (PCM) data is received utilizing time division multiplexing (TDM). The signal lines include BCK, WS, and SD. Data from 16 channels at most can be received. TDM Philips standard, TDM MSB alignment standard, and TDM PCM standard are supported in this mode, depending on user configuration. |

|  |   |
|--|---|
| <b>PDM RX mode</b>                     | In this mode, pulse density modulation (PDM) data is received. Used signals include WS and DATA. PDM standard is supported in this mode by user configuration.  |
| <b>TDM TX mode</b>                     | In this mode, pulse code modulated (PCM) data is sent in a way of time division multiplexing (TDM). The signal lines include BCK, WS, and DATA. Data up to 16 channels can be sent. TDM Philips standard, TDM MSB alignment standard, and TDM PCM standard are supported in this mode, depending on user configuration.                     |
| <b>PDM TX mode</b>                     | In this mode, pulse density modulation (PDM) data is sent. The signal lines include WS and DATA. PDM standard is supported in this mode by user configuration.  |
| <b>PCM-to-PDM Data</b>                 |   |
| <b>Format Converter (for I2S only)</b> | A data format converter that converts PCM data into PDM data (hereinafter referred to as PCM-to-PDM converter), which can be enabled in PDM TX master mode. When the converter is enabled, I2S fetches pulse code modulated (PCM) data from storage via GDMA, converts it to pulse density modulation (PDM) data, and then transmits it.    |
| <b>PDM-to-PCM Data</b>                 |   |
| <b>Format Converter (for I2S only)</b> | A data format converter that converts PDM data into PCM data (hereinafter referred to as PDM-to-PCM converter), which can be enabled in PDM RX master or slave mode. When the converter is enabled, I2S receives pulse density modulation (PDM) data, converts it into pulse code modulated (PCM) data, and stores it into memory via GDMA. |

## 41.3 Features

The I2S module has the following features:

- Master mode and slave mode
- Full-duplex and half-duplex communications
- Separate TX and RX units that can work independently or simultaneously
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- Various TX/RX modes supported:
  - TDM TX mode, up to 16 channels supported
  - TDM RX mode, up to 16 channels supported

- PDM TX mode
  - \* Raw PDM data transmission
  - \* PCM-to-PDM data format conversion (for I2S<sub>0</sub> only), up to 2 channels supported
- PDM RX mode
  - \* Raw PDM data reception
  - \* PDM-to-PCM data format conversion (for I2S<sub>0</sub> only), up to 8 channels supported
- Configurable APLL clock with frequencies up to 240 MHz
- Configurable high-precision sample clock with a variety of sampling frequencies supported (refer to the note below for more details)
- 8/16/24/32-bit data width
- Synchronous counter in TX mode
- ETM feature
- Direct Memory Access (GDMA-AHB only)
- Standard I2S interface interrupts

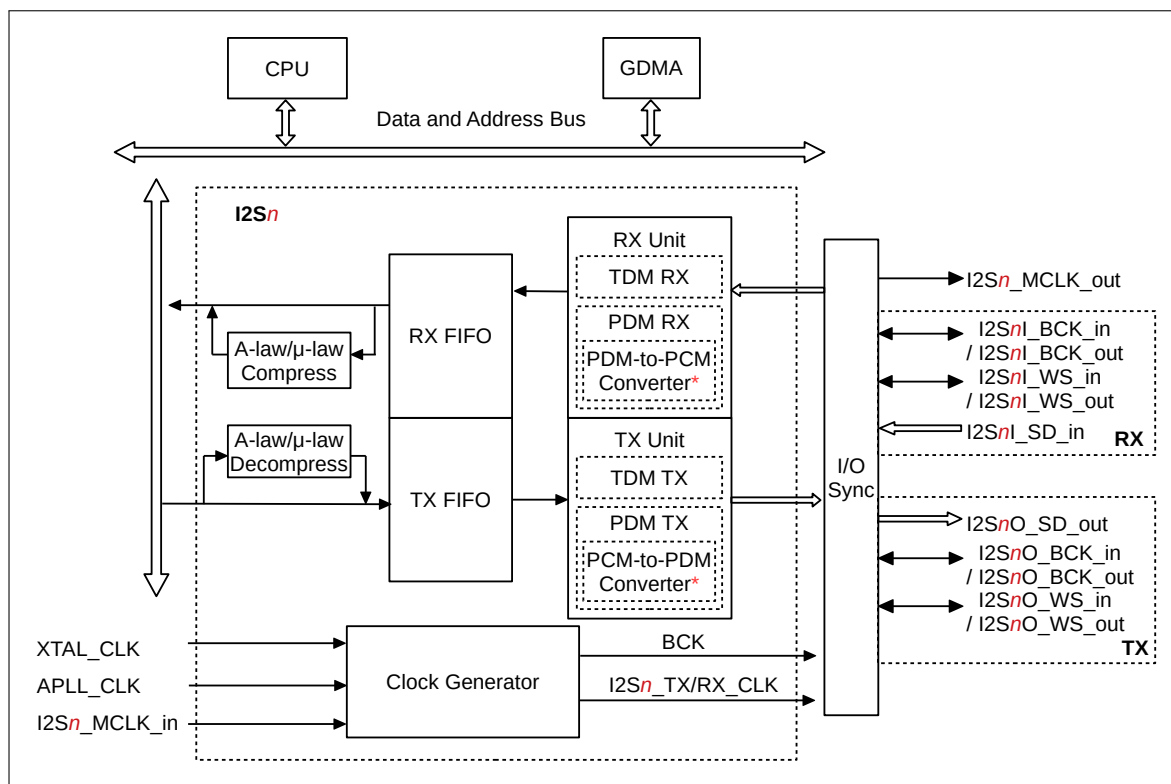
**Note:**

In slave mode, to ensure the sampling accuracy, the module clock frequency must be greater than or equal to 8 times the BCK clock frequency. Therefore, the maximum sampling frequency of I2S<sub>n</sub> is limited by the data bit width and the number of channels. For example, since the clock source frequency is up to 240 MHz, the module clock can be configured up to 120 MHz, and the BCK clock can be configured up to 15 MHz. Therefore, when transmitting dual-channel 32-bit width data, I2S<sub>n</sub> supports sample frequencies up to 234.375 kHz, e.g., 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 128 kHz, and 192 kHz. Please refer to Section 41.6 *I2S TX/RX Clock* for detailed information.

## 41.4 System Architecture

Figure 41.4-1 shows the structure of the ESP32-P4 I2S<sub>n</sub> module, consisting of:

- Transmit control unit (TX Unit)
- Receive control unit (RX Unit)
- Input and output timing unit (I/O Sync)
- Clock divider (Clock Generator)
- 64 x 32-bit TX FIFO
- 64 x 32-bit RX FIFO
- Compress/Decompress units



Note: The PDM-to-PCM converter and PCM-to-PDM converter are only supported by I2S0.

Figure 41.4-1. ESP32-P4 I2S System Diagram

The I2Sn module supports direct memory access (DMA) to internal memory. For more information, see Chapter 3 [GDMA Controller \(GDMA-AHB, GDMA-AXI\)](#).

Both the TX unit and the RX unit have a three-line interface that uses a bit clock line (BCK), a word select line (WS), and a serial data line (SD). The SD line of the TX unit is used for data output and the SD line of the RX unit for data input. The BCK and WS signal lines of the TX and RX units are used for data output in master mode, and the BCK and WS signal lines of the TX and RX units are used for data input in slave mode.

The signal bus of the I2Sn module is shown at the right part of Figure 41.4-1. The naming of these signals in RX and TX units follows the pattern of I2SnA\_B\_C such as I2SnI\_BCK\_in.

- “A” indicates that the signal belongs to the I2Sn TX or RX unit, which includes:
  - “I”: Signal input to/output from the RX unit
  - “O”: Signal input to/output from the TX unit
- “B” represents the signal function, which includes:
  - BCK
  - WS
  - SD
- “C” represents the signal direction, which includes:
  - “in”: Input signal into the I2Sn module
  - “out”: Output signal from the I2Sn module

Table 41.4-1 provides a detailed description of I2S signals.

**Table 41.4-1. I2S<sub>n</sub> Signal Description**

| Signal                        | Direction | Function  |
|-------------------------------|-----------|---|
| I2S <sub>n</sub> I_BCK_in     | Input     | In I2S <sub>n</sub> slave mode, inputs BCK signal for RX unit.                              |
| I2S <sub>n</sub> I_BCK_out    | Output    | In I2S <sub>n</sub> master mode, outputs BCK signal for RX unit.                            |
| I2S <sub>n</sub> I_WS_in      | Input     | In I2S <sub>n</sub> slave mode, inputs WS signal for RX unit.                               |
| I2S <sub>n</sub> I_WS_out     | Output    | In I2S <sub>n</sub> master mode, outputs WS signal for RX unit.                             |
| I2S <sub>n</sub> I_Data_in    | Input     | Works as the serial input data bus for I2S <sub>n</sub> RX unit.                            |
| I2S <sub>n</sub> O_Data_out   | Output    | Works as the serial output data bus for I2S <sub>n</sub> TX unit.                           |
| I2S <sub>n</sub> O_BCK_in     | Input     | In I2S <sub>n</sub> slave mode, inputs BCK signal for TX unit.                              |
| I2S <sub>n</sub> O_BCK_out    | Output    | In I2S <sub>n</sub> master mode, outputs BCK signal for TX unit.                            |
| I2S <sub>n</sub> O_WS_in      | Input     | In I2S <sub>n</sub> slave mode, inputs WS signal for TX unit.                               |
| I2S <sub>n</sub> O_WS_out     | Output    | In I2S <sub>n</sub> master mode, outputs WS signal for TX unit.                             |
| I2S <sub>n</sub> _MCLK_in     | Input     | In I2S <sub>n</sub> slave mode, works as a clock source from the external master.           |
| I2S <sub>n</sub> _MCLK_out    | Output    | In I2S <sub>n</sub> master mode, works as a clock source for the external slave.            |
| I2S <sub>n</sub> OI_Data1_in  | Input     | When the PDM-to-PCM converter is enabled, works as the serial input data line for RX unit.  |
| I2S <sub>n</sub> OI_Data2_in  | Input     | When the PDM-to-PCM converter is enabled, works as the serial input data line for RX unit.  |
| I2S <sub>n</sub> OI_Data3_in  | Input     | When the PDM-to-PCM converter is enabled, works as the serial input data line for RX unit.  |
| I2S <sub>n</sub> OO_Data1_out | Output    | When the PCM-to-PDM converter is enabled, works as the serial output data line for TX unit. |

\* Any required signals of I2S<sub>n</sub> must be mapped to the chip's pins via HP GPIO matrix, see Chapter 8 [GPIO Matrix and IO MUX](#).

## 41.5 Supported Audio Standards

ESP32-P4 I2S<sub>n</sub> supports multiple audio standards, including TDM Philips standard, TDM MSB alignment standard, TDM PCM standard, and PDM standard.

Select the needed standard by configuring the following bits:

- [I2S\\_TX/RX\\_TDM\\_EN](#)
  - 0: Disable TDM mode
  - 1: Enable TDM mode
- [I2S\\_TX/RX\\_PDM\\_EN](#)
  - 0: Disable PDM mode
  - 1: Enable PDM mode
- [I2S\\_TX/RX\\_MSB\\_SHIFT](#)
  - 0: WS and SD signals change simultaneously, i.e., enable MSB alignment standard



- 1: WS signal changes one BCK clock cycle earlier than SD signal, i.e., enable Philips standard or select PCM standard

**Note:**

`I2S_TX/RX_TDM_EN` and `I2S_TX/RX_PDM_EN` must not be configured to 1 or 0 at the same time, otherwise ESP32-P4 I2S<sub>n</sub> will transmit data incorrectly in a mode that is neither TDM nor PDM.

### 41.5.1 TDM Philips Standard

Philips specifications require that WS signal changes one BCK clock cycle earlier than SD signal on BCK falling edge, which means that WS signal is valid from one clock cycle before transmitting the first bit of channel data and changes one clock before the end of channel data transfer. SD signal line transmits the most significant bit of audio data first.

Compared with the Philips standard, TDM Philips standard supports multiple channels. See Figure 41.5-1.

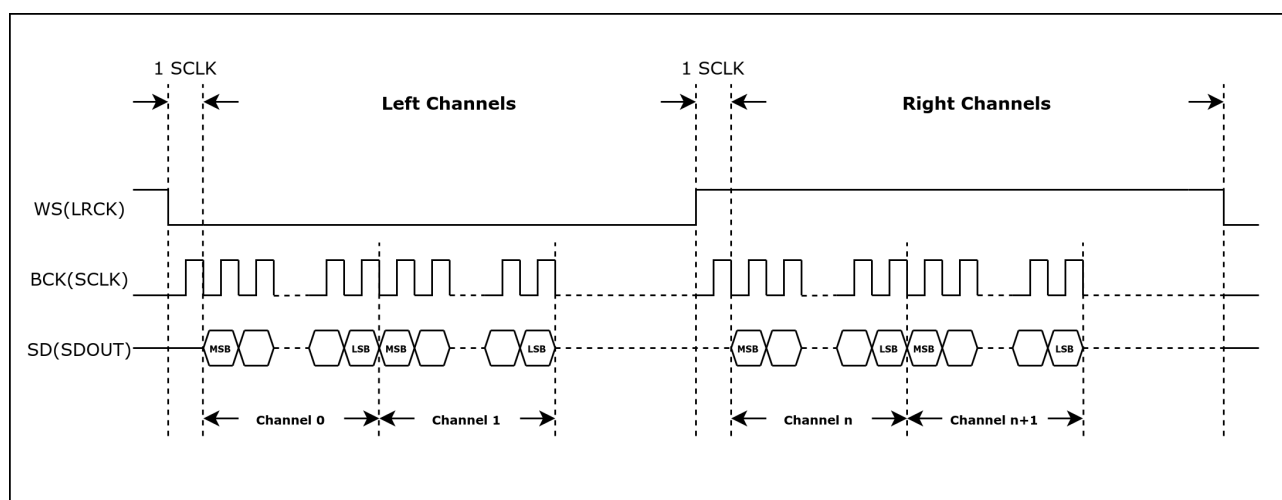


Figure 41.5-1. TDM Philips Standard Timing Diagram

### 41.5.2 TDM MSB Alignment Standard

MSB alignment specifications require that WS and SD signals change simultaneously on the falling edge of BCK. The WS signal is valid until the end of the channel data transfer. The SD signal line transmits the most significant bit of audio data first.

Compared with MSB alignment standard, TDM MSB alignment standard supports multiple channels. See Figure 41.5-2.

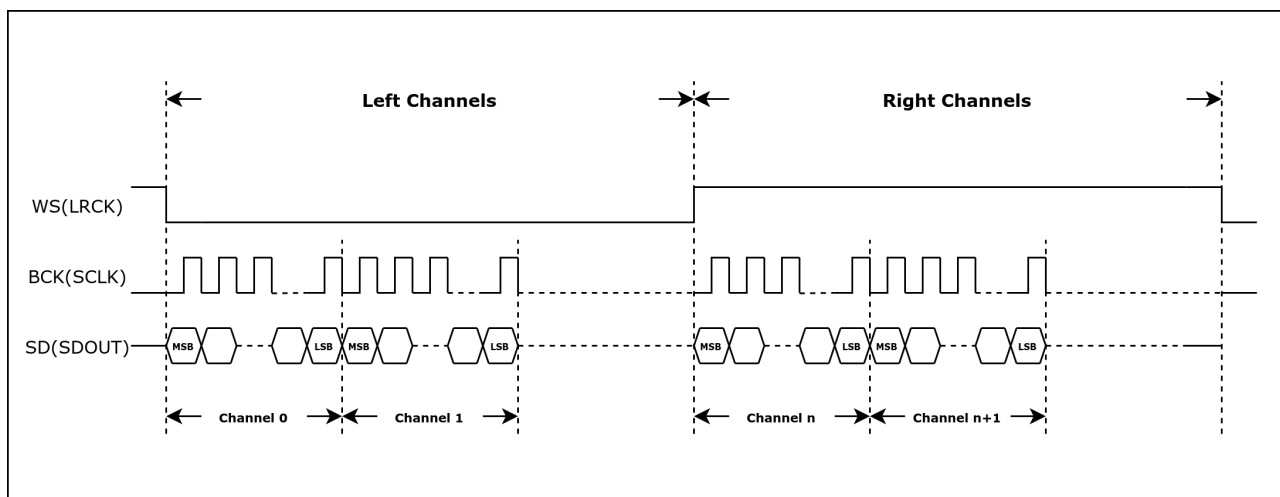


Figure 41.5-2. TDM MSB Alignment Standard Timing Diagram

### 41.5.3 TDM PCM Standard

Short frame synchronization under the PCM standard requires that the WS signal changes one BCK clock cycle earlier than the SD signal on the falling edge of BCK, which means that the WS signal becomes valid one clock cycle before transferring the first bit of channel data and remains unchanged in this BCK clock cycle. SD signal line first transmits the most significant bit of audio data.

Compared with PCM standard, TDM PCM standard supports multiple channels. See Figure 41.5-3.

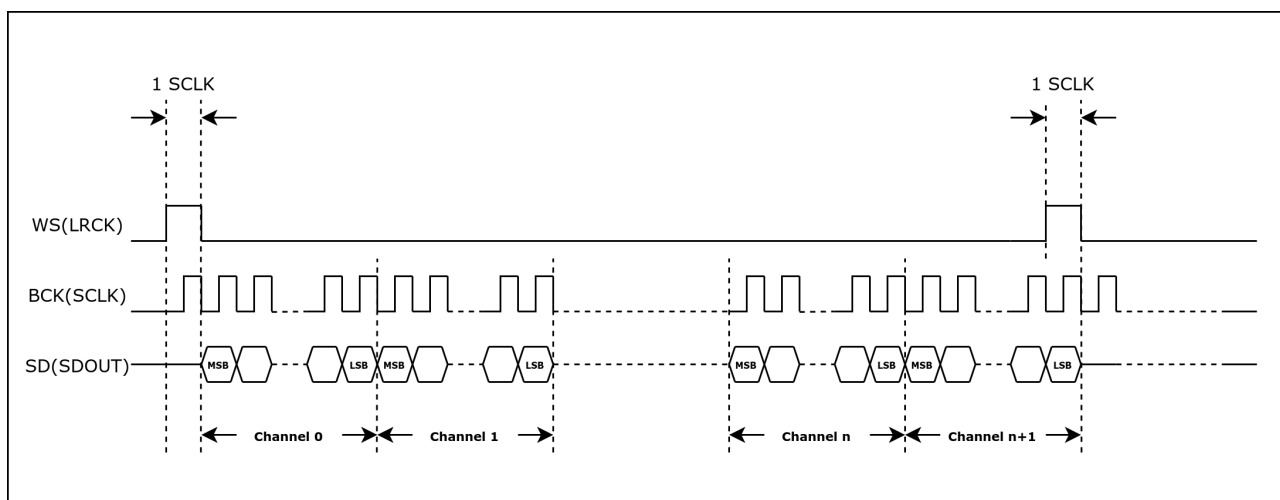


Figure 41.5-3. TDM PCM Standard Timing Diagram

### 41.5.4 PDM Standard

Under PDM standard, WS signal changes continuously during data transmission. The low-level and high-level of this signal indicates the left channel and right channel respectively. WS and SD signals change simultaneously. See Figure 41.5-4.

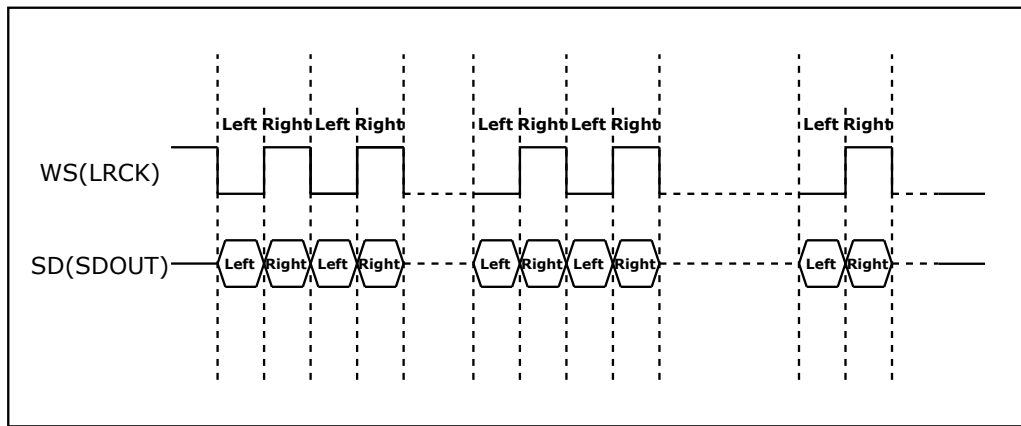


Figure 41.5-4. PDM Standard Timing Diagram

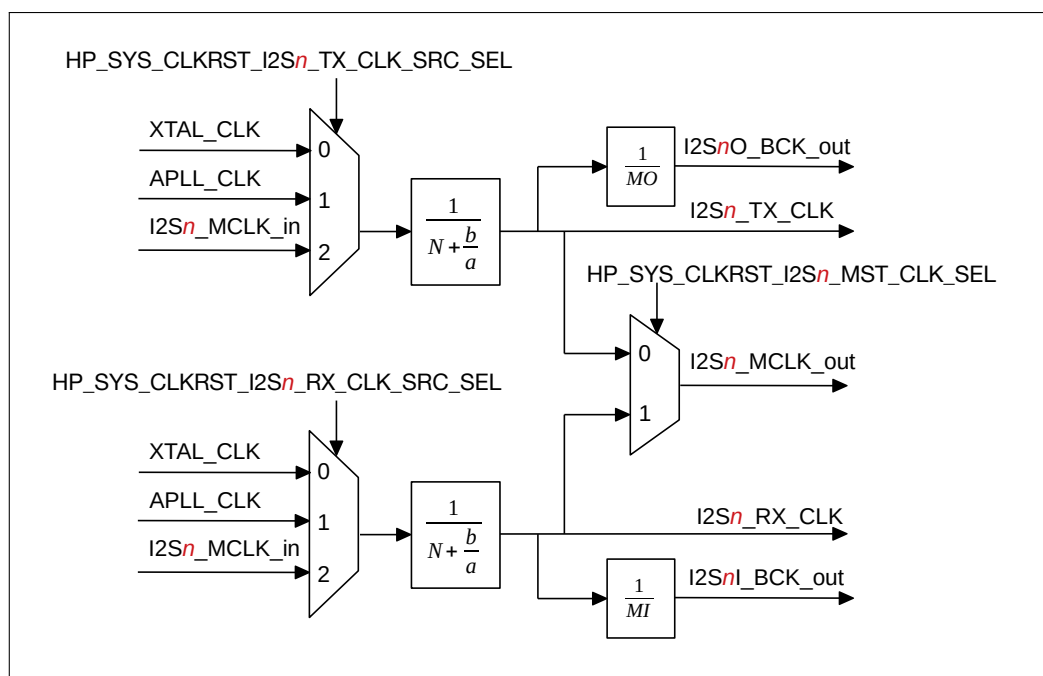
## 41.6 I2S TX/RX Clock

I2S<sub>n</sub>\_TX/RX\_CLK is the master clock of I2S<sub>n</sub> TX/RX unit, divided from:

- 40 MHz XTAL\_CLK
- APLL\_CLK with adjustable frequency
- I2S<sub>n</sub>\_MCLK\_in (external input clock)

The serial clock (BCK) of the I2S<sub>n</sub> TX/RX unit is divided from I2S<sub>n</sub>\_TX/RX\_CLK, as shown in Figure 41.6-1.

HP\_SYS\_CLKRST\_I2S<sub>n</sub>\_TX/RX\_CLK\_SRC\_SEL is used to select clock source for TX/RX unit, and HP\_SYS\_CLKRST\_I2S<sub>n</sub>\_TX/RX\_CLK\_EN to enable or disable the clock source.

Figure 41.6-1. I2S<sub>n</sub> Clock Generator

The following formula shows the relation between I2S<sub>n</sub>\_TX/RX\_CLK frequency  $f_{\text{I2S}_n\text{TX/RX\_CLK}}$  and the divider

clock source frequency  $f_{I2Sn\_CLK\_S}$ :

$$f_{I2Sn\_TX/RX\_CLK} = \frac{f_{I2Sn\_CLK\_S}}{N + \frac{b}{a}}$$

N is an integer value between 2 and 256. The value of N is mapped to that of `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_N` as follows:

- When `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_N` = 0, N = 256;
- When `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_N` = 1, N = 2;
- When `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_N` has any other value, N = `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_N`.

The values of “a” and “b” in fractional divider depend only on x, y, z, and yn1. The corresponding formulas are as follows:

- When  $b \leq \frac{a}{2}$ ,  $yn1 = 0$ ,  $x = \text{floor}(\lceil \frac{a}{b} \rceil) - 1$ ,  $y = a \% b$ ,  $z = b$ ;
- When  $b > \frac{a}{2}$ ,  $yn1 = 1$ ,  $x = \text{floor}(\lceil \frac{a}{a-b} \rceil) - 1$ ,  $y = a \% (a - b)$ ,  $z = a - b$ .

The values of x, y, z, and yn1 are configured in `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_X`, `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_Y`, `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_Z`, and `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_YN1`.

To configure the integer divider, clear `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_X` and `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_Z`, then set `HP_SYS_CLKRST_I2Sn_TX/RX_DIV_Y` to 1.

**Note:**

Using fractional divider may introduce some clock jitter.

In master TX mode, the serial clock BCK for I2Sn TX unit is `I2SnO_BCK_out` divided from `I2Sn_TX_CLK` which is:

$$f_{I2SnO\_BCK\_out} = \frac{f_{I2Sn\_TX\_CLK}}{MO}$$

“MO” is an integer value:

$$MO = I2Sn\_TX\_BCK\_DIV\_NUM + 1$$

**Note:**

Note that `I2Sn_TX_BCK_DIV_NUM` must not be configured as 1.

In master RX mode, the serial clock BCK for I2Sn RX unit is `I2SnI_BCK_out` divided from `I2Sn_RX_CLK`, which is:

$$f_{I2SnI\_BCK\_out} = \frac{f_{I2Sn\_RX\_CLK}}{MI}$$

“MI” is an integer value:

$$MI = I2Sn\_RX\_BCK\_DIV\_NUM + 1$$

**Note:**

- `I2S_RX_BCK_DIV_NUM` must not be configured as 1.
- In I2S slave mode, make sure  $f_{I2S\_TX/RX\_CLK} \geq 8 * f_{BCK}$ . The I2S<sub>n</sub> module can output I2S<sub>n</sub>\_MCLK\_out as the master clock for peripherals.

## 41.7 I2S Reset

The units and FIFOs in the I2S<sub>n</sub> module are reset by the following bits.

- I2S<sub>n</sub> TX/RX units: Reset by the bits `I2S_TX_RESET` and `I2S_RX_RESET`;
- I2S<sub>n</sub> TX/RX FIFO: Reset by the bits `I2S_TX_FIFO_RESET` and `I2S_RX_FIFO_RESET`.

**Note:**

The I2S<sub>n</sub> module clock must be configured first before the module and FIFO are reset.

## 41.8 I2S Master/Slave Mode

The ESP32-P4 I2S<sub>n</sub> module can operate as a master or a slave in half-duplex and full-duplex communications, depending on the configuration of `I2S_RX_SLAVE_MOD` and `I2S_TX_SLAVE_MOD`.

- `I2S_TX_SLAVE_MOD`
  - 0: Master TX mode
  - 1: Slave TX mode
- `I2S_RX_SLAVE_MOD`
  - 0: Master RX mode
  - 1: Slave RX mode

### 41.8.1 Master/Slave TX Mode

- I2S<sub>n</sub> works as a master transmitter:
  - Set `I2S_TX_START` to start transmitting data. When this bit is set, the TX unit keeps driving the clock signal and serial data.
  - If `I2S_TX_STOP_EN` is set and all the data in FIFO is transmitted, the master stops transmitting data and clock signals.
  - If `I2S_TX_STOP_EN` is cleared and all the data in FIFO is transmitted, meanwhile no new data is filled into FIFO, the TX unit keeps transmitting the last data frame and clock signal.
  - Master stops transmitting data when the bit `I2S_TX_START` is cleared.
- I2S<sub>n</sub> works as a slave transmitter:
  - Set `I2S_TX_START`. Wait for the master BCK clock to enable a transmit operation.

- If [I2S\\_TX\\_STOP\\_EN](#) is set and all the data in FIFO is transmitted, then the slave keeps transmitting zeros, till the master stops providing BCK signal.
- If [I2S\\_TX\\_STOP\\_EN](#) is cleared and all the data in FIFO is transmitted, meanwhile no new data is filled into FIFO, the TX unit keeps transmitting the last data frame.
- If [I2S\\_TX\\_START](#) is cleared, slave keeps transmitting zeros till the master stops providing BCK clock signal.

## 41.8.2 Master/Slave RX Mode

- I2Sn works as a master receiver:
  - Set [I2S\\_RX\\_START](#) to start receiving data. When this bit is set, the RX unit keeps outputting clock signal and sampling input data.
  - Configure [I2S\\_RX\\_STOP\\_MODE](#) to control the suspension of data reception:
    - \* 0: The RX unit only suspends data reception when [I2S\\_RX\\_START](#) is cleared.
    - \* 1: The RX unit suspends data reception when [I2S\\_RX\\_START](#) is cleared or the number of received bytes is greater than the value configured in [I2S\\_RX\\_EOF\\_NUM\\_REG](#). When [I2S\\_RX\\_START](#) is not cleared, data reception can be restarted by setting [I2S\\_RX\\_RESET](#) to 1.
    - \* 2: The RX unit suspends data reception when [I2S\\_RX\\_START](#) is cleared or GDMA RX FIFO is full. When [I2S\\_RX\\_START](#) is not cleared and the GDMA RX FIFO is no longer full, data reception can be restarted by setting [I2S\\_RX\\_RESET](#) to 1.
  - RX unit stops receiving data when the bit [I2S\\_RX\\_START](#) is cleared.
- I2Sn works as a slave receiver:
  - Set [I2S\\_RX\\_START](#). Wait for the master BCK signal to start receiving data.
  - Configure [I2S\\_RX\\_STOP\\_MODE](#) to control data reception suspension:
    - \* 0: The RX unit only suspends data reception when [I2S\\_RX\\_START](#) is cleared.
    - \* 1: The RX unit suspends data reception when the number of received bytes is greater than the value configured in [I2S\\_RX\\_EOF\\_NUM\\_REG](#). When [I2S\\_RX\\_START](#) is not cleared, data reception can be restarted by setting [I2S\\_RX\\_RESET](#) to 1.
    - \* 2: The RX unit suspends data reception when [I2S\\_RX\\_START](#) is cleared or GDMA RX FIFO is full. When [I2S\\_RX\\_START](#) is not cleared and the GDMA RX FIFO is no longer full, data reception can be restarted by setting [I2S\\_RX\\_RESET](#) to 1.
  - The RX unit stops receiving data when the bit [I2S\\_RX\\_START](#) is cleared.

## 41.9 Transmitting Data

### Note:

Updating the configuration described in this and subsequent sections requires to set [I2S\\_TX\\_UPDATE](#) accordingly to synchronize registers from APB clock domain to TX clock domain. For more detailed configurations, see Section [41.13.1](#).

In TX mode, I2S<sub>n</sub> first reads data through GDMA and transmits these data out via output signals according to the configured data mode and channel mode.

### 41.9.1 Data Format Control

Data format is controlled in the following phases:

- Phase I: Read data from memory and write it to TX FIFO;
- Phase II: Read the TX data from TX FIFO and convert the data according to the output data mode;
- Phase III: Clock out the TX data serially.

#### 41.9.1.1 Bit Width Control of Channel Valid Data

The bit width of the valid data in each channel is determined by [I2S\\_TX\\_BITS\\_MOD](#) and [I2S\\_TX\\_24\\_FILL\\_EN](#). For details, see the table below.

Table 41.9-1. Bit Width of Channel Valid Data

| Channel Valid Data Width | I2S_TX_BITS_MOD | I2S_TX_24_FILL_EN |
|--------------------------|-----------------|-------------------|
| 32                       | 31              | x <sup>*</sup>    |
|                          | 23              | 1                 |
| 24                       | 23              | 0                 |
| 16                       | 15              | x                 |
| 8                        | 7               | x                 |

\* "x" represents that this value is ignored.

#### 41.9.1.2 Endian Control of Channel Valid Data

When I2S<sub>n</sub> reads data through GDMA, the data endian under various data width is controlled by [I2S\\_TX\\_BIG\\_ENDIAN](#). Table 41.9-2 shows how [I2S\\_TX\\_BIG\\_ENDIAN](#) controls the reading of the data with different valid data widths of the channel.

Table 41.9-2. Endian of Channel Valid Data

| Channel Valid Data Width | Original Data    | Endian of Processed Data | I2S_TX_BIG_ENDIAN |
|--------------------------|------------------|--------------------------|-------------------|
| 32                       | {B3, B2, B1, B0} | {B3, B2, B1, B0}         | 0                 |
|                          |                  | {B0, B1, B2, B3}         | 1                 |
| 24                       | {B2, B1, B0}     | {B2, B1, B0}             | 0                 |
|                          |                  | {B0, B1, B2}             | 1                 |
| 16                       | {B1, B0}         | {B1, B0}                 | 0                 |
|                          |                  | {B0, B1}                 | 1                 |
| 8                        | {B0}             | {B0}                     | x                 |

**Note:**

B0, B1, B2, B3 each represents an 8-bit data, and the symbol {} indicates that the bytes are combined together. For

example, {B3, B2, B1, B0} represents a 32-bit data, wherein B0 represents bit 0-7, B1 represents bit 8-15, B2 represents bit 16-23, and B3 represents bit 24-31.

### 41.9.1.3 A-law/ $\mu$ -law Compression and Decompression

ESP32-P4 I2S<sub>n</sub> compresses/decompresses the valid data into 32-bit by A-law or by  $\mu$ -law. If the bit width of valid data is smaller than 32, zeros are filled to the extra high bits of the data to be compressed/decompressed by default.

**Note:**

Extra high bits here mean the bits[31: channel valid data width] of the data to be compressed/decompressed.

Configure [I2S\\_TX\\_PCM\\_BYPASS](#):

- 0: Compress or decompress the data
- 1: Do not compress or decompress the data

Configure [I2S\\_TX\\_PCM\\_CONF](#):

- 0: Decompress the data using A-law
- 1: Compress the data using A-law
- 2: Decompress the data using  $\mu$ -law
- 3: Compress the data using  $\mu$ -law

At this point, the first phase of data format control is completed.

### 41.9.1.4 Bit Width Control of Channel TX Data

The TX data width in each channel is determined by [I2S\\_TX\\_TDM\\_CHAN\\_BITS](#).

- If TX data width in each channel is larger than the valid data width, zeros will be filled to these extra bits.  
Configure [I2S\\_TX\\_LEFT\\_ALIGN](#):

- 0: The valid data is at the lower bits of TX data. Zeros are filled into higher bits of TX data;
- 1: The valid data is at the higher bits of TX data. Zeros are filled into lower bits of TX data.

- If the TX data width in each channel is smaller than the valid data width, only the lower bits of valid data are sent out, and the higher bits are discarded.

At this point, the second phase of data format control is completed.

### 41.9.1.5 Bit Order Control of Channel Data

The data bit order in each channel is controlled by [I2S\\_TX\\_BIT\\_ORDER](#):

- 0: Not reverse the valid data bit order;
- 1: Reverse the valid data bit order.

At this point, the data format control is completed. The data after format control will be sent sequentially from high to low. Figure [41.9-1](#) shows the complete process of TX data format control.



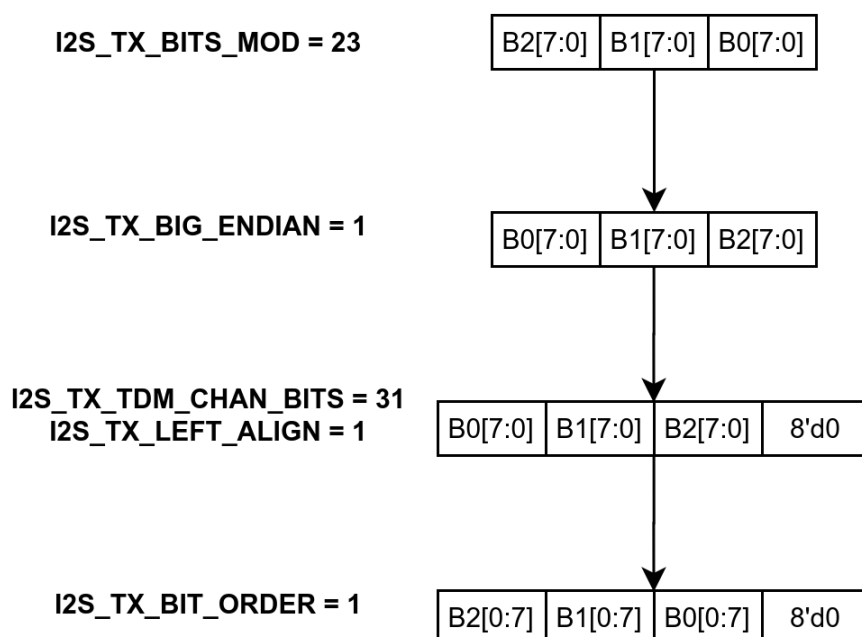


Figure 41.9-1. TX Data Format Control

## 41.9.2 Channel Mode Control

ESP32-P4 I2S<sub>n</sub> supports both TDM TX mode and PDM TX mode. Set [I2S\\_TX\\_TDM\\_EN](#) to enable TDM TX mode, or set [I2S\\_TX\\_PDM\\_EN](#) to enable PDM TX mode.

**Note:**

[I2S\\_TX\\_TDM\\_EN](#) and [I2S\\_TX\\_PDM\\_EN](#) must not be cleared or set simultaneously.

### 41.9.2.1 TDM TX Mode

In TDM TX mode, I2S<sub>n</sub> supports up to 16 channels to transmit data. The total number of TX channels in use is controlled by [I2S\\_TX\\_TDM\\_TOT\\_CHAN\\_NUM](#). For example, If [I2S\\_TX\\_TDM\\_TOT\\_CHAN\\_NUM](#) is set to 5, six channels in total (channel 0 ~ 5) will be used to transmit data. See Figure 41.9-2.

In these TX channels, if [I2S\\_TX\\_TDM\\_CHAN<sub>n</sub>\\_EN](#) is set to:

- 1: This channel transmits the channel data out;
- 0: The TX data to be sent by this channel is controlled by [I2S\\_TX\\_CHAN\\_EQUAL](#):
  - 1: The data of the previous channel is sent out;
  - 0: The data stored in [I2S\\_SINGLE\\_DATA](#) is sent out.

**Note:**

Most stereo I2S<sub>n</sub> codecs can be controlled by setting the I2S<sub>n</sub> module into 2-channel mode under TDM standard.

In TDM TX master mode, WS signal is controlled by [I2S\\_TX\\_WS\\_IDLE\\_POL](#) and [I2S\\_TX\\_TDM\\_WS\\_WIDTH](#):

- [I2S\\_TX\\_WS\\_IDLE\\_POL](#): The default level of WS signal;
- [I2S\\_TX\\_TDM\\_WS\\_WIDTH](#): The cycles the WS default level lasts for when transmitting all channel data.

[I2S\\_TX\\_HALF\\_SAMPLE\\_BITS](#) x 2 is equal to the BCK cycles in one WS period.

### TDM Channel Configuration Example

In this example, the register configuration is as follows:

- [I2S\\_TX\\_TDM\\_CHAN\\_NUM](#) = 5, i.e., channel 0 ~ 5 are used to transmit data.
- [I2S\\_TX\\_CHAN\\_EQUAL](#) = 1, i.e., data of the previous channel will be transmitted if the bit [I2S\\_TX\\_TDM\\_CHAN \$n\$ \\_EN](#) ( $n$  = 0 ~ 5) is cleared.
- [I2S\\_TX\\_TDM\\_CHAN0/2/5\\_EN](#) = 1, i.e., these channels transmit their channel data out.
- [I2S\\_TX\\_TDM\\_CHAN1/3/4\\_EN](#) = 0, i.e., these channels transmit the previous channel's data out.

Once the configuration is done, data is transmitted as follows.

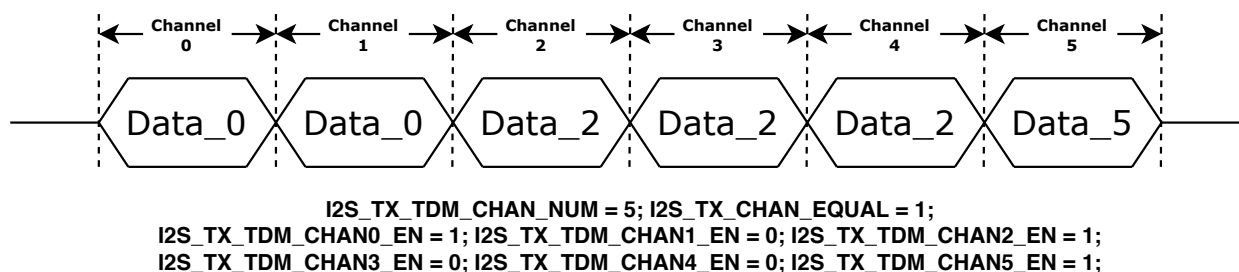


Figure 41.9-2. TDM Channel Control

### 41.9.2.2 PDM TX Mode

In PDM TX mode, [I2S \$n\$](#)  supports both PDM raw data transmission and PCM-to-PDM data format conversion (the latter only supported by [I2S0](#)).

In PDM TX mode, fetching data through GDMA is controlled by [I2S\\_TX\\_MONO](#) and [I2S\\_TX\\_MONO\\_FST\\_VLD](#). See Table 41.9-3. Configure the two bits according to the data stored in memory, be it the single-channel or dual-channel data.

Table 41.9-3. Data-Fetching Control in PDM Mode

| Data-Fetching Control Option   | Mode        | <a href="#">I2S_TX_MONO</a> | <a href="#">I2S_TX_MONO_FST_VLD</a> |
|--|-------------|-----------------------------|-------------------------------------|
| Post data-fetching request to GDMA at any edge of WS signal                    | Stereo mode | 0                           | x                                   |
| Post data-fetching request to GDMA only at the second half period of WS signal | Mono mode   | 1                           | 0                                   |
| Post data-fetching request to GDMA only at the first half period of WS signal  | Mono mode   | 1                           | 1                                   |

When [I2S \$n\$](#)  is in PDM TX master mode, the default level of WS signal is controlled by [I2S\\_TX\\_WS\\_IDLE\\_POL](#), and the WS signal frequency is half of the BCK signal frequency. The configuration of WS signal is similar to that of BCK signal. Please refer to Section 41.6 and Figure 41.6.

When **transmitting raw PDM data**, the I2S<sub>n</sub> channel mode is controlled by [I2S\\_TX\\_CHAN\\_MOD](#) and [I2S\\_TX\\_WS\\_IDLE\\_POL](#). See the table below.

**Table 41.9-4. I2S<sub>n</sub> Channel Control for Raw PDM Data**

| Channel Control Option | Left Channel                                | Right Channel                   | Mode Control Field <sup>1</sup> | Channel Select Bit <sup>2</sup> |
|------------------------|---|---------------------------------|---------------------------------|---------------------------------|
| Stereo mode            | Transmit the left channel data              | Transmit the right channel data | 0                               | x                               |
| Mono mode              | Transmit the left channel data              | Transmit the left channel data  | 1                               | 0                               |
|                        | Transmit the right channel data             | Transmit the right channel data | 1                               | 1                               |
|                        | Transmit the right channel data             | Transmit the right channel data | 2                               | 0                               |
|                        | Transmit the left channel data              | Transmit the left channel data  | 2                               | 1                               |
|                        | Transmit the value of "single" <sup>3</sup> | Transmit the right channel data | 3                               | 0                               |
|                        | Transmit the left channel data              | Transmit the value of "single"  | 3                               | 1                               |
|                        | Transmit the left channel data              | Transmit the value of "single"  | 4                               | 0                               |
|                        | Transmit the value of "single"              | Transmit the right channel data | 4                               | 1                               |

<sup>1</sup> [I2S\\_TX\\_CHAN\\_MOD](#)

<sup>2</sup> [I2S\\_TX\\_WS\\_IDLE\\_POL](#)

<sup>3</sup> The "single" value is equal to the value of [I2S\\_SINGLE\\_DATA](#).

If the **PCM-to-PDM converter is enabled** for I2S<sub>0</sub>, the PCM data through GDMA is converted to PDM data and then output in PDM signal format. Configure [I2S\\_PCM2PDM\\_CONV\\_EN](#) to enable the converter. The register configuration for the PCM-to-PDM converter is as follows:

- Configure 1-line PDM output format or 1-/2-line DAC output mode as the table below:

**Table 41.9-5. I2S<sub>0</sub> PCM-to-PDM Data Output**

| Channel Output Format                 | <a href="#">I2S_TX_PDM_DAC_MODE_EN</a> | <a href="#">I2S_TX_PDM_DAC_2OUT_EN</a> |
|---------------------------------------|--|--|
| 1-line PDM output format <sup>1</sup> | 0                                      | x                                      |
| 1-line DAC output format <sup>2</sup> | 1                                      | 0                                      |
| 2-line DAC output format              | 1                                      | 1                                      |

**Note:**

- In PDM output format, SD data of two channels is sent out in one WS period.
- In DAC output format, SD data of one channel is sent out in one WS period.
- 1-line PDM/DAC output format uses I2S<sub>n</sub>O\_Data\_out as the data output line.
- 2-line DAC output format uses I2S<sub>n</sub>O\_Data\_out and I2S<sub>n</sub>O\_Data1\_out as data output lines.
- In terms of application, the PDM output format is targeted at applications that require clock signals and can decode PDM format codecs, while the DAC output format is targeted at applications that do not rely on clock signals, do not have PDM format codecs, and can recover analog waveforms directly through low-pass filtering.

- Configure sampling frequency and upsampling rate as below:

When the I2S<sup>0</sup> PCM-to-PDM converter is enabled, PDM clock frequency is equal to BCK frequency. The relation of sampling frequency ( $f_{\text{Sampling}}$ , the sampling frequency of PCM data) and BCK frequency (the sampling frequency of PDM data) is as follows:

$$f_{\text{Sampling}} = \frac{f_{\text{BCK}}}{\text{OSR}}$$

Upsampling rate (OSR) is related to `I2S_TX_PDM_SINC_OSR2` as follows:

$$\text{OSR} = \text{I2S\_TX\_PDM\_SINC\_OSR2} \times 64$$

Sampling frequency  $f_{\text{Sampling}}$  is related to `I2S_TX_PDM_FS` as follows:

$$f_{\text{Sampling}} = \text{I2S\_TX\_PDM\_FS} \times 100$$

Configure the registers according to the needed sampling frequency, upsampling rate, and PDM clock frequency.

### PDM Channel Configuration Example

In this example of I2S<sup>0</sup>, the register configuration is as follows.

- `I2S_PCM2PDM_CONV_EN` = 0, i.e., transmit the raw PDM data.
- `I2S_TX_MONO` = 0, i.e., data is fetched from memory via GDMA in both the high and low levels of WS.
- `I2S_TX_CHAN_MOD` = 2, i.e., mono mode is selected.
- `I2S_TX_WS_IDLE_POL` = 1, i.e., both the left and right channels transmit the left channel data, and the right channel data will be discarded.

Once the configuration is done, assume that the data in memory **after data format control** is:

|      |       |      |       |     |      |       |
|------|-------|------|-------|-----|------|-------|
| Left | Right | Left | Right | ... | Left | Right |
|------|-------|------|-------|-----|------|-------|

#### Note:

1. The data above refers to the processed data after data format control instead of the original data.
2. “Left” and “Right” represent channel data, and their bit widths are channel valid data width. Please refer to Section 41.9.1.

Then the channel data is transmitted after channel mode control as follows.

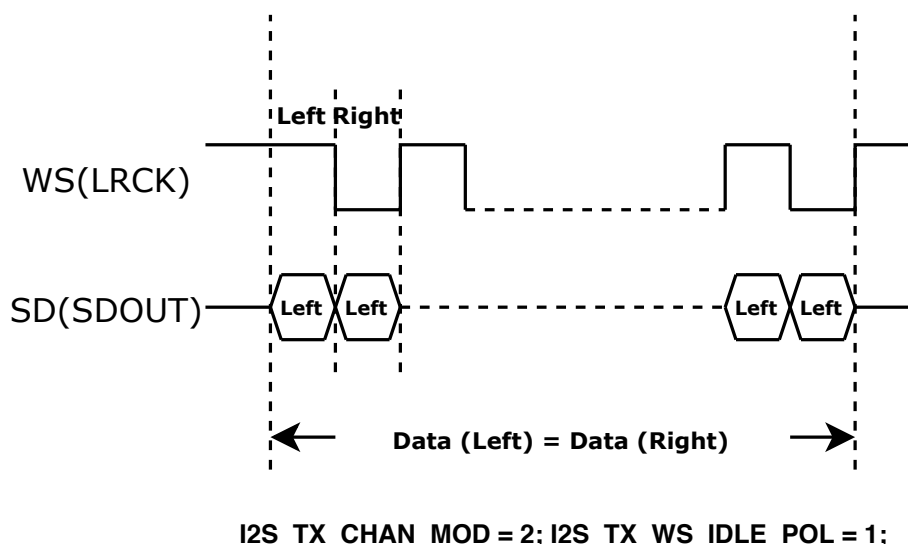


Figure 41.9-3. PDM Channel Control Example

### 41.9.3 Synchronous Counter

ESP32-P4 I2S<sub>n</sub> TX unit contains synchronous counters to reflect the current I2S<sub>n</sub> data transmission status. The counters can be used to detect I2S<sub>n</sub> transmit data errors or to synchronize data when multiple devices are using I2S<sub>n</sub> for data transmission.

ESP32-P4 I2S<sub>n</sub> contains two types of synchronous counters:

- [I2S\\_TX\\_FIFO\\_CNT](#)
  - Each time the I2S<sub>n</sub> TX FIFO reads data, the counter is incremented by 1.
  - The counter can be reset by setting [I2S\\_TX\\_FIFO\\_CNT\\_RST](#).
  - The counter is 31-bit wide and is automatically reset to zero on overflow.
- [I2S\\_TX\\_BCK\\_CNT](#)
  - Each time I2S<sub>n</sub> TX transmits a BCK cycle, the counter is incremented by 1.
  - The counter can be reset by setting [I2S\\_TX\\_BCK\\_CNT\\_RST](#).
  - The counter is 31-bit wide and is automatically reset to zero on overflow.

**Note:**

- Each time the I2S<sub>n</sub> TX FIFO transmits data, a channel data is sent. Therefore, when I2S<sub>n</sub> transmits the data correctly,  $I2S\_TX\_BCK\_CNT = I2S\_TX\_FIFO\_CNT \times \text{the bit width of channel TX data}$  (see Section 41.9.1.4).
- When the I2S<sub>n</sub> TX unit transmits the data, there is some delay between fetching data from the FIFO and transmitting it to the line, so the value of [I2S\\_TX\\_BCK\\_CNT](#) might be a little different from that of [I2S\\_TX\\_FIFO\\_CNT](#).

#### Application scenarios

##### 1. I2S TX synchronization for multiple devices

When multiple devices transmit data through the I2S TX at the same time, desynchronization may occur after a long period of time due to small frequency differences in the clock sources. In this case, read the

`I2S_TX_FIFO_CNT` value of each device to determine the location of the audio data being sent to perform synchronization.

## 2. I2S TX stability check

When the device is in an application scenario with high GDMA usage, there may be numbers missing in I2S TX occasionally due to multiplexing arbitration. In this case, check the ratio of `I2S_TX_BCK_CNT` to `I2S_TX_FIFO_CNT` to confirm the stability of the device when running I2S TX.

## 41.10 Receiving Data

In RX mode, I2S<sub>n</sub> first reads data from the peripheral interface and then stores the data in memory via GDMA according to the configured channel mode and data mode.

### 41.10.1 Channel Mode Control

ESP32-P4 I2S<sub>n</sub> supports both TDM RX mode and PDM RX mode. Set `I2S_RX_TDM_EN` to enable TDM RX mode, or set `I2S_RX_PDM_EN` to enable PDM RX mode.

**Note:**

`I2S_RX_TDM_EN` and `I2S_RX_PDM_EN` must not be cleared or set simultaneously.

#### 41.10.1.1 TDM RX Mode

In TDM RX mode, I2S<sub>n</sub> supports up to 16 channels to input data. The total number of RX channels in use is controlled by `I2S_RX_TDM_TOT_CHAN_NUM`. For example, if `I2S_RX_TDM_TOT_CHAN_NUM` is set to 5, channel 0 ~ 5 will be used to receive data.

In these RX channels, if `I2S_RX_TDM_CHANn_EN` is set to:

- 1: The channel data is valid and will be stored into RX FIFO;
- 0: The channel data is invalid and will not be stored into RX FIFO.

In TDM master mode, WS signal is controlled by `I2S_RX_WS_IDLE_POL` and `I2S_RX_TDM_WS_WIDTH`.

- `I2S_RX_WS_IDLE_POL`: The default level of WS signal;
- `I2S_RX_TDM_WS_WIDTH`: The cycles the WS default level lasts for when receiving all channel data.

`I2S_RX_HALF_SAMPLE_BITS` x 2 is equal to the BCK cycles in one WS period.

#### 41.10.1.2 PDM RX Mode

In PDM RX mode, I2S<sub>n</sub> supports both PDM raw data reception and PDM-to-PCM data format conversion (the latter only supported by I2S<sub>0</sub>).

In PDM RX mode, I2S<sub>n</sub> converts the serial data from channels to the data to be entered into memory.

In PDM RX master mode, the default level of the WS signal is controlled by `I2S_RX_WS_IDLE_POL`. WS frequency is half of the BCK frequency. The configuration of the BCK signal is similar to that of WS signal as described in Section 41.6. Note, in PDM RX mode, the value of `I2S_RX_HALF_SAMPLE_BITS` must be same as that of `I2S_RX_BITS_MOD`.

When the **PDM-to-PCM converter is enabled** for I2S0, the received PDM data is converted to PCM data and controlled according to the data mode. Configure [I2S\\_RX\\_PDM2PCM\\_EN](#) to enable this converter. The register configuration for PDM-to-PCM converter is as follows:

- Configure sampling frequency and downsampling rate.

When I2S0 PDM-to-PCM converter is enabled, PDM clock frequency is:

- in master mode: PDM clock frequency is equal to BCK frequency.
- in slave mode: PDM clock is provided by external device.

The sampling frequency ( $f_{\text{Sampling}}$ ) is related to PDM clock frequency as follows:

$$f_{\text{Sampling}} = \frac{f_{\text{PDM}}}{\text{DSR}}$$

Downsampling rate (DSR) is related to [I2S\\_RX\\_PDM\\_SINC\\_DSR\\_16\\_EN](#) as follows:

$$\text{DSR} = \text{I2S\_RX\_PDM\_SINC\_DSR\_16\_EN} \times 64$$

Configure the registers according to needed master/slave mode, sampling frequency, and downsampling rate.

- Configure valid channels.

When the PDM-to-PCM converter is enabled, input signals from eight channels are supported at most. See Table 41.10-1 for the register configuration and related channels.

**Table 41.10-1. PDM-to-PCM Data Input**

| Input Data Signal | Channel       | Enable Register                         |
|-------------------|---------------|---|
| I2S0I_Data_in     | Left channel  | <a href="#">I2S_RX_TDM_PDM_CHAN0_EN</a> |
|                   | Right channel | <a href="#">I2S_RX_TDM_PDM_CHAN1_EN</a> |
| I2S0I1_Data_in    | Left channel  | <a href="#">I2S_RX_TDM_PDM_CHAN2_EN</a> |
|                   | Right channel | <a href="#">I2S_RX_TDM_PDM_CHAN3_EN</a> |
| I2S0I2_Data_in    | Left channel  | <a href="#">I2S_RX_TDM_PDM_CHAN4_EN</a> |
|                   | Right channel | <a href="#">I2S_RX_TDM_PDM_CHAN5_EN</a> |
| I2S0I3_Data_in    | Left channel  | <a href="#">I2S_RX_TDM_PDM_CHAN6_EN</a> |
|                   | Right channel | <a href="#">I2S_RX_TDM_PDM_CHAN7_EN</a> |

## 41.10.2 Data Format Control

The data format of I2S<sub>n</sub> is controlled in the following phases:

- Phase I: Serial input data is converted into the data to be saved to RX FIFO;
- Phase II: The data is read from RX FIFO and converted according to the input data mode.

### 41.10.2.1 Bit Order Control of Channel Data

The channel data will be stored as the data to be input in order from high to low. The data bit order in each channel is controlled by [I2S\\_RX\\_BIT\\_ORDER](#):

- 0: The bit order of the data to be input is not reversed;
- 1: The bit order of the data to be input is reversed.

At this point, the first phase of data format control is completed. The data to be input after bit order control is stored in the RX FIFO.

#### 41.10.2.2 Bit Width Control of Channel Storage (Valid) Data

The storage data width in each channel is controlled by [I2S\\_RX\\_BITS\\_MOD](#) and [I2S\\_RX\\_24\\_FILL\\_EN](#). See the table below.

Table 41.10-2. Channel Storage Data Width

| Channel Storage Data Width | <a href="#">I2S_RX_BITS_MOD</a> | <a href="#">I2S_RX_24_FILL_EN</a> |
|----------------------------|---------------------------------|-----------------------------------|
| 32                         | 31                              | x                                 |
|                            | 23                              | 1                                 |
| 24                         | 23                              | 0                                 |
| 16                         | 15                              | x                                 |
| 8                          | 7                               | x                                 |

#### 41.10.2.3 Bit Width Control of Channel RX Data

The RX data width in each channel is determined by [I2S\\_RX\\_TDM\\_CHAN\\_BITS](#).

- If the storage data width in each channel is smaller than the received (RX) data width, then only the bits within the storage data width is saved into memory. Configure [I2S\\_RX\\_LEFT\\_ALIGN](#) to:
  - 0: Only the lower bits of the received data within the storage data width is stored to memory;
  - 1: Only the higher bits of the received data within the storage data width is stored to memory.
- If the received data width is smaller than the storage data width in each channel, the higher bits of the received data will be filled with zeros and then the data is saved to memory.

#### 41.10.2.4 Endian Control of Channel Storage Data

The received data is then converted into storage data (to be stored to memory) after some processing, such as discarding extra bits or filling zeros in missing bits. The endian of the storage data is controlled by [I2S\\_RX\\_BIG\\_ENDIAN](#) under various data width. See the table below.

Table 41.10-3. Channel Storage Data Endian

| Channel Storage Data Width | Original Data    | Endian of Processed Data | <a href="#">I2S_RX_BIG_ENDIAN</a> |
|----------------------------|------------------|--------------------------|-----------------------------------|
| 32                         | {B3, B2, B1, B0} | {B3, B2, B1, B0}         | 0                                 |
|                            |                  | {B0, B1, B2, B3}         | 1                                 |
| 24                         | {B2, B1, B0}     | {B2, B1, B0}             | 0                                 |
|                            |                  | {B0, B1, B2}             | 1                                 |
| 16                         | {B1, B0}         | {B1, B0}                 | 0                                 |
|                            |                  | {B0, B1}                 | 1                                 |
| 8                          | {B0}             | {B0}                     | x                                 |



### 41.10.2.5 A-law/ $\mu$ -law Compression and Decompression

ESP32-P4 I2S<sub>n</sub> compresses/decompresses the storage data in 32-bit by A-law or by  $\mu$ -law. By default, zeros are filled into high bits.

Configure [I2S\\_RX\\_PCM\\_BYPASS](#):

- 0: Compress or decompress the data
- 1: Do not compress or decompress the data

Configure [I2S\\_RX\\_PCM\\_CONF](#):

- 0: Decompress the data using A-law
- 1: Compress the data using A-law
- 2: Decompress the data using  $\mu$ -law
- 3: Compress the data using  $\mu$ -law

At this point, the data format control is completed. Data then is stored into memory via GDMA.

## 41.11 Event Task Matrix Feature

ESP32-P4 I2S<sub>n</sub> supports the Event Task Matrix (ETM) function, which allows I2S<sub>n</sub>'s ETM tasks to be triggered by any peripherals' ETM events, or I2S<sub>n</sub>'s ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to I2S<sub>n</sub>. For more information, please refer to [Chapter 12 Event Task Matrix \(ETM\)](#).

I2S<sub>n</sub> can receive the following ETM tasks:

- I2S<sub>n</sub>\_TASK\_START\_TX: Enables I2S<sub>n</sub> TX for data transfer.
- I2S<sub>n</sub>\_TASK\_START\_RX: Enables I2S<sub>n</sub> RX for data transfer.
- I2S<sub>n</sub>\_TASK\_STOP\_TX: Stops I2S<sub>n</sub> TX data transfer.
- I2S<sub>n</sub>\_TASK\_STOP\_RX: Stops I2S<sub>n</sub> RX data transfer.

I2S<sub>n</sub> can generate the following ETM events:

- I2S<sub>n</sub>\_EVT\_TX\_DONE: Indicates that I2S<sub>n</sub> TX has completed data transmission.
- I2S<sub>n</sub>\_EVT\_RX\_DONE: Indicates that I2S<sub>n</sub> RX has completed data reception.
- I2S<sub>n</sub>\_EVT\_X\_WORDS\_SENT: Indicates that the word number sent by I2S<sub>n</sub> TX is equal to or larger than the value set by [I2S\\_ETM\\_TX\\_SEND\\_WORD\\_NUM](#).
- I2S<sub>n</sub>\_EVT\_X\_WORDS\_RECEIVED: Indicates that the word number received by I2S<sub>n</sub> RX is equal to or larger than the value set by [I2S\\_ETM\\_RX\\_RECEIVE\\_WORD\\_NUM](#).

In practical applications, I2S<sub>n</sub>'s ETM events can trigger its own ETM tasks. For example, the I2S<sub>n</sub>\_EVT\_X\_WORDS\_SENT event can trigger the I2S<sub>n</sub>\_TASK\_STOP\_TX task, and in this way stop the I2S<sub>n</sub> operation through ETM.

## 41.12 I2S Interrupts

ESP32-P4's I2S $n$  can generate the I2S $n$ \_INTR interrupt signal that will be sent to the [Interrupt Matrix](#). There are several internal interrupt sources from I2S $n$  that can generate the above interrupt signal(s) as follows:

- I2S $n$ \_TX\_HUNG\_INT: Triggered when data transmission is timed out. For example, if the I2S $n$  module is configured as TX slave mode, but the master does not provide BCK or WS signals for a long time (specified in [I2S\\_LC\\_HUNG\\_CONF\\_REG](#)), this interrupt will be triggered.
- I2S $n$ \_RX\_HUNG\_INT: Triggered when the data reception is timed out. For example, if the I2S $n$  module is configured as RX slave mode, but the master does not transmit data for a long time (specified in [I2S\\_LC\\_HUNG\\_CONF\\_REG](#)), this interrupt will be triggered.
- I2S $n$ \_TX\_DONE\_INT: Triggered when data transmission is completed.
- I2S $n$ \_RX\_DONE\_INT: Triggered when the data reception is completed.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [41.14 Register Summary](#).

## 41.13 Software Configuration Process

### 41.13.1 Configure I2S as TX Mode

Follow the steps below to configure I2S $n$  as TX mode via software:

1. Configure the clock as described in Section [41.6](#).
2. Configure signal pins according to Table [41.4-1](#).
3. Select the mode needed by configuring [I2S\\_TX\\_SLAVE\\_MOD](#).
  - 0: Master TX mode
  - 1: Slave TX mode
4. Set needed TX data mode and TX channel mode as described in Section [41.9](#), and then set [I2S\\_TX\\_UPDATE](#).
5. Reset TX unit and TX FIFO as described in Section [41.7](#).
6. Enable corresponding interrupts. See Section [41.12](#).
7. Configure GDMA outlink.
8. Set [I2S\\_TX\\_STOP\\_EN](#) if needed. For more information, please refer to Section [41.8.1](#).
9. Start transmitting data:
  - In master mode, wait till I2S $n$  slave gets ready, then set [I2S\\_TX\\_START](#) to start transmitting data;

- In slave mode, set [I2S\\_TX\\_START](#). When the I2S<sub>n</sub> master supplies BCK and WS signals, I2S<sub>n</sub> slave starts transmitting data.
10. Wait for the interrupt signals set in Step 6, or check whether the transfer is completed by querying [I2S\\_TX\\_IDLE](#):
    - 0: Transmitter is working;
    - 1: Transmitter is in idle state.
  11. Clear [I2S\\_TX\\_START](#) to stop data transfer.

### 41.13.2 Configure I2S as RX Mode

Follow the steps below to configure I2S<sub>n</sub> as RX mode via software:

1. Configure the clock as described in Section 41.6.
2. Configure signal pins according to Table 41.4-1.
3. Select the mode needed by configuring [I2S\\_RX\\_SLAVE\\_MOD](#).
  - 0: Master RX mode
  - 1: Slave RX mode
4. Set needed RX data mode and RX channel mode as described in Section 41.10, and then set [I2S\\_RX\\_UPDATE](#).
5. Reset the RX unit and its FIFO according to Section 41.7.
6. Enable the corresponding interrupts. See Section 41.12.
7. Configure GDMA inlink and set the length of RX data by configuring [I2S\\_RX\\_EOF\\_NUM\\_REG](#).
8. Start receiving data:
  - In master mode, when the slave is ready, set [I2S\\_RX\\_START](#) to start receiving data.
  - In slave mode, set [I2S\\_RX\\_START](#) to start receiving data when BCK and WS signals are received from the master.
9. The received data is then stored to the specified memory address according to the configuration of GDMA. Then the corresponding interrupt set in step 6 is generated.

## 41.14 Register Summary

The addresses in this section are relative to I2S<sub>n</sub> base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description  | Address | Access   |
|---|--|---------|----------|
| <b>Interrupt registers</b>                    |  |         |          |
| <a href="#">I2S_INT_RAW_REG</a>               | I2S interrupt raw register   | 0x000C  | R/SS/WTC |
| <a href="#">I2S_INT_ST_REG</a>                | I2S interrupt status register  | 0x0010  | RO       |
| <a href="#">I2S_INT_ENA_REG</a>               | I2S interrupt enable register  | 0x0014  | R/W      |
| <a href="#">I2S_INT_CLR_REG</a>               | I2S interrupt clear register   | 0x0018  | WT       |
| <b>RX control and configuration registers</b> |  |         |          |
| <a href="#">I2S_RX_CONF_REG</a>               | I2S RX configuration register  | 0x0020  | varies   |
| <a href="#">I2S_RX_CONF1_REG</a>              | I2S RX configuration register 1  | 0x0028  | R/W      |
| <a href="#">I2S_RX_PDM2PCM_CONF_REG</a>       | I2S RX PDM-to-PCM configuration register                               | 0x0048  | R/W      |
| <a href="#">I2S_RX_TDM_CTRL_REG</a>           | I2S TX TDM mode control register                                       | 0x0050  | R/W      |
| <a href="#">I2S_RXEOF_NUM_REG</a>             | I2S RX data number control register                                    | 0x0064  | R/W      |
| <b>TX control and configuration registers</b> |  |         |          |
| <a href="#">I2S_TX_CONF_REG</a>               | I2S TX configuration register  | 0x0024  | varies   |
| <a href="#">I2S_TX_CONF1_REG</a>              | I2S TX configuration register 1  | 0x002C  | R/W      |
| <a href="#">I2S_TX_PCM2PDM_CONF_REG</a>       | I2S TX PCM-to-PDM configuration register (for I2S <sub>0</sub> only)   | 0x0040  | R/W      |
| <a href="#">I2S_TX_PCM2PDM_CONF1_REG</a>      | I2S TX PCM-to-PDM configuration register (for I2S <sub>0</sub> only)   | 0x0044  | R/W      |
| <a href="#">I2S_TX_TDM_CTRL_REG</a>           | I2S TX TDM mode control register                                       | 0x0054  | R/W      |
| <b>RX clock and timing register</b>           |  |         |          |
| <a href="#">I2S_RX_TIMING_REG</a>             | I2S RX timing control register (some fields for I2S <sub>0</sub> only) | 0x0058  | R/W      |
| <b>TX clock and timing register</b>           |  |         |          |
| <a href="#">I2S_TX_TIMING_REG</a>             | I2S TX timing control register (some fields for I2S <sub>0</sub> only) | 0x005C  | R/W      |
| <b>Control and configuration registers</b>    |  |         |          |
| <a href="#">I2S_LC_HUNG_CONF_REG</a>          | I2S timeout configuration register                                     | 0x0060  | R/W      |
| <a href="#">I2S_CONF_SIGLE_DATA_REG</a>       | I2S single data register   | 0x0068  | R/W      |
| <b>TX status register</b>                     |  |         |          |
| <a href="#">I2S_STATE_REG</a>                 | I2S TX status register   | 0x006C  | RO       |
| <b>ETM register</b>                           |  |         |          |
| <a href="#">I2S_ETM_CONF_REG</a>              | I2S ETM configuration register   | 0x0070  | R/W      |
| <b>Sync counter registers</b>                 |  |         |          |
| <a href="#">I2S_FIFO_CNT_REG</a>              | I2S sync counter register  | 0x0074  | varies   |
| <a href="#">I2S_BCK_CNT_REG</a>               | I2S sync counter register  | 0x0078  | varies   |
| <b>Clock registers</b>                        |  |         |          |
| <a href="#">I2S_CLK_GATE_REG</a>              | Clock gate register  | 0x007C  | R/W      |

| Name                         | Description              | Address | Access |
|------------------------------|--------------------------|---------|--------|
| Version register             |                          |         |        |
| <a href="#">I2S_DATE_REG</a> | Version control register | 0x0080  | R/W    |

## 41.15 Registers

The addresses in this section are relative to I2S<sub>n</sub> base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 41.1. I2S\_INT\_RAW\_REG (0x000C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2S_TX_HUNG_INT_RAW<br>I2S_RX_HUNG_INT_RAW<br>I2S_TX_DONE_INT_RAW<br>I2S_RX_DONE_INT_RAW |   |   |   |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 |       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**I2S\_RX\_DONE\_INT\_RAW** The raw interrupt status of the [I2S\\_RX\\_DONE\\_INT](#) interrupt. (R/SS/WTC)

**I2S\_TX\_DONE\_INT\_RAW** The raw interrupt status of the [I2S\\_TX\\_DONE\\_INT](#) interrupt.  
(R/SS/WTC)

**I2S\_RX\_HUNG\_INT\_RAW** The raw interrupt status of the [I2S\\_RX\\_HUNG\\_INT](#) interrupt. (R/SS/WTC)

**I2S\_TX\_HUNG\_INT\_RAW** The raw interrupt status of the [I2S\\_TX\\_HUNG\\_INT](#) interrupt. (R/SS/WTC)

Register 41.2. I2S\_INT\_ST\_REG (0x0010)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2S_TX_HUNG_INT_ST<br>I2S_RX_HUNG_INT_ST<br>I2S_TX_DONE_INT_ST<br>I2S_RX_DONE_INT_ST |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 4  | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 |   |       |

**I2S\_RX\_DONE\_INT\_ST** The masked interrupt status of the [I2S\\_RX\\_DONE\\_INT](#) interrupt. (RO)

**I2S\_TX\_DONE\_INT\_ST** The masked interrupt status of the [I2S\\_TX\\_DONE\\_INT](#) interrupt. (RO)

**I2S\_RX\_HUNG\_INT\_ST** The masked interrupt status of the [I2S\\_RX\\_HUNG\\_INT](#) interrupt. (RO)

**I2S\_TX\_HUNG\_INT\_ST** The masked interrupt status of the [I2S\\_TX\\_HUNG\\_INT](#) interrupt. (RO)

Register 41.3. I2S\_INT\_ENA\_REG (0x0014)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2S_TX_HUNG_INT_ENA<br>I2S_RX_HUNG_INT_ENA<br>I2S_TX_DONE_INT_ENA<br>I2S_RX_DONE_INT_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**I2S\_RX\_DONE\_INT\_ENA** Write 1 to enable the [I2S\\_RX\\_DONE\\_INT](#) interrupt. (R/W)

**I2S\_TX\_DONE\_INT\_ENA** Write 1 to enable the [I2S\\_TX\\_DONE\\_INT](#) interrupt. (R/W)

**I2S\_RX\_HUNG\_INT\_ENA** Write 1 to enable the [I2S\\_RX\\_HUNG\\_INT](#) interrupt. (R/W)

**I2S\_TX\_HUNG\_INT\_ENA** Write 1 to enable the [I2S\\_TX\\_HUNG\\_INT](#) interrupt. (R/W)

Register 41.4. I2S\_INT\_CLR\_REG (0x0018)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2S-TX_HUNG_INT_CLR<br>I2S-RX_HUNG_INT_CLR<br>I2S-TX_DONE_INT_CLR<br>I2S-RX_DONE_INT_CLR |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | Reset |

**I2S\_RX\_DONE\_INT\_CLR** Write 1 to clear the [I2S\\_RX\\_DONE\\_INT](#) interrupt. (WT)

**I2S\_TX\_DONE\_INT\_CLR** Write 1 to clear the [I2S\\_TX\\_DONE\\_INT](#) interrupt. (WT)

**I2S\_RX\_HUNG\_INT\_CLR** Write 1 to clear the [I2S\\_RX\\_HUNG\\_INT](#) interrupt. (WT)

**I2S\_TX\_HUNG\_INT\_CLR** Write 1 to clear the [I2S\\_TX\\_HUNG\\_INT](#) interrupt. (WT)

### Register 41.5. I2S\_RX\_CONF\_REG (0x0020)

[illegible]

**I2S\_RX\_RESET** Configures whether to reset RX unit.

0: No effect

1: Reset

(WT)

**I2S\_RX\_FIFO\_RESET** Configures whether to reset RX FIFO.

0: No effect

1: Reset

(WT)

**I2S\_RX\_START** Configures whether to start receiving data.

0: No effect

1: Start

(R/W/SC)

**I2S\_RX\_SLAVE\_MOD** Configures whether to enable slave RX mode.

0: Enable master mode

## 1: Enable slave mode

(R/W)

**I2S\_RX\_STOP\_MODE** Configures when I2S RX stop data reception.

0: Only stops when I2S\_RX\_START is cleared

1: Stops when `I2S_RX_START` is cleared or the number of received bytes is greater than the value configured in `I2S_RX_EOF_NUM_REG`

2: Stops when `I2S_RX_START` is cleared or GDMA RX FIFO is full

(R/W)

**I2S\_RX\_MONO** Configures whether to enable RX unit in mono mode.

0: Disable

1: Enable

(R/W)

**I2S\_RX\_BIG\_ENDIAN** Configures I2S RX byte endian.

0: Low address data is saved to low address

1: Low address data is saved to high address

(R/W)

Continued on the next page...



**Register 41.5. I2S\_RX\_CONF\_REG (0x0020)**

Continued from the previous page...

**I2S\_RX\_UPDATE** Configures whether to update I2S RX registers from APB clock domain to I2S RX clock domain. This bit will be cleared by hardware after the register update is done.

0: No effect

1: Update

(R/W/SC)

**I2S\_RX\_MONO\_FST\_VLD** Configures the valid data channel in I2S RX mono mode.

0: The second channel data valid

1: The first channel data valid

(R/W)

**I2S\_RX\_PCM\_CONF** Configures I2S RX compress/decompress mode.

0 (atol): A-law decompress

1 (ltoa): A-law compress

2 (utol):  $\mu$ -law decompress

3 (ltou):  $\mu$ -law compress

(R/W)

**I2S\_RX\_PCM\_BYPASS** Configures whether to bypass the Compress/Decompress units for received data.

0: No effect

1: Bypass

(R/W)

**I2S\_RX\_MSB\_SHIFT** Configures the timing between the WS signal and the MSB of data.

0: Align at the rising edge

1: The WS signal changes one BCK clock earlier

(R/W)

**I2S\_RX\_LEFT\_ALIGN** Configures I2S RX alignment mode.

0: Right alignment mode

1: Left alignment mode

(R/W)

Continued on the next page...

**Register 41.5. I2S\_RX\_CONF\_REG (0x0020)**

Continued from the previous page...

**I2S\_RX\_24\_FILL\_EN** Configures the bit number that the 24-bit channel data is stored to.

0: Store 24-bit channel data to 24 bits

1: Store 24-bit channel data to 32 bits (Extra bits are filled with zeros)

(R/W)

**I2S\_RX\_WS\_IDLE\_POL** Configures the relationship between WS level and which channel data to receive.

0: WS remains low when receiving left channel data and high when receiving right channel data

1: WS remains high when receiving left channel data and low when receiving right channel data

(R/W)

**I2S\_RX\_BIT\_ORDER** Configures whether to reverse the bit order of the I2S RX data to be received.

0: Not reverse

1: Reverse

(R/W)

**I2S\_RX\_TDM\_EN** Configures whether to enable I2S TDM RX mode.

0: Disable

1: Enable

(R/W)

**I2S\_RX\_PDM\_EN** Configures whether to enable I2S PDM RX mode.

0: Disable

1: Enable

(R/W)

**I2S\_RX\_BCK\_DIV\_NUM** Configures the divider of BCK in RX mode. Note this divider must not be configured to 1. (R/W)

Register 41.6. I2S\_RX\_CONF1\_REG (0x0028)

|                      |    |     |    |    |    |     |   |                         |   |   |   |   |     |  |  |                 |       |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |
|----------------------|----|-----|----|----|----|-----|---|-------------------------|---|---|---|---|-----|--|--|-----------------|-------|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|
| I2S_RX_TDM_CHAN_BITS |    |     |    |    |    |     |   | I2S_RX_HALF_SAMPLE_BITS |   |   |   |   |     |  |  | I2S_RX_BITS_MOD |       |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  | I2S_RX_TDM_WS_WIDTH |  |  |  |  |  |  |  |
| 31                   | 27 | 26  | 19 | 18 | 14 | 13  | 9 | 8                       | 0 |   |   |   |     |  |  |                 |       |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |
| 0xf                  |    | 0xf |    |    |    | 0xf |   | 0                       | 0 | 0 | 0 | 0 | 0x0 |  |  |                 | Reset |  |  |  |  |  |  |            |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |

**I2S\_RX\_TDM\_WS\_WIDTH** Configures the width of I2S<sub>nl</sub>\_WS\_out (WS default level) at idle level in TDM mode. Width of I2S<sub>nl</sub>\_WS\_out at idle level in TDM mode = (I2S\_RX\_TDM\_WS\_WIDTH[8:0] + 1) x T\_BCK. (R/W)

**I2S\_RX\_BITS\_MOD** Configures the valid data bit length of I2S RX channel.

- 7: All the valid channel data is in 8-bit mode
  - 15: All the valid channel data is in 16-bit mode
  - 23: All the valid channel data is in 24-bit mode
  - 31: All the valid channel data is in 32-bit mode
  - Other values are invalid.
- (R/W)

**I2S\_RX\_HALF\_SAMPLE\_BITS** Configures I2S RX sample bits. BCK cycles in one WS period = I2S\_RX\_HALF\_SAMPLE\_BITS x 2. (R/W)

**I2S\_RX\_TDM\_CHAN\_BITS** Configures RX bit number for each channel in TDM mode. Bit number expected = I2S\_RX\_TDM\_CHAN\_BITS + 1. (R/W)

### Register 41.7. I2S\_RX\_PDM2PCM\_CONF\_REG (for I2S0 only) (0x0048)

[illegible]

**I2S\_RX\_PDM2PCM\_EN** Configures whether to enable the PDM-to-PCM converter in RX mode.

0: Disable

1: Enable

(R/W)

**I2S\_RX\_PDM\_SINC\_DSR\_16\_EN** Configures the downsampling rate of PDM RX filter group 1 module.

0: 64

1: 128

(R/W)

**I2S\_RX\_PDM2PCM\_AMPLIFY\_NUM** Configures the PDM-to-PCM RX amplify number. PCM data will be multiplied by this value before outputting.

(R/W)

**I2S\_RX\_PDM\_HP\_BYPASS** Configures whether PDM-to-PCM RX bypasses the HP filter.

0: Not bypass

1: Bypass

(R/W)

### Register 41.8. I2S\_RX\_TDM\_CTRL\_REG (0x0050)

[illegible]

**I2S\_RX\_TDM\_PDM\_CHAN $n$ \_EN ( $n$ : 0-7)** Configures whether to enable the valid data input of I2S RX TDM or PDM channel  $n$ .

0: Disable. Channel *n* only inputs 0

1: Enable

(R/W)

**I2S\_RX\_TDM\_CHAN $n$ \_EN** ( $n$ : 8-15) Configures whether to enable the valid data input of I2S RX TDM channel  $n$ .

0: Disable. Channel *n* only inputs 0

1: Enable

(R/W)

**I2S\_RX\_TDM\_TOT\_CHAN\_NUM** Configures the total number of channels in use in I2S RX TDM mode. Total channel number in use = I2S\_RX\_TDM\_TOT\_CHAN\_NUM + 1. (R/W)

### Register 41.9. I2S\_RXEOF\_NUM\_REG (0x0064)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2S_RX_EOF_NUM |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x40           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Reset                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**I2S\_RX\_EOF\_NUM** Configures the bit length of RX data. Bit length of RX data = (I2S\_RX\_BITS\_MOD + 1) x (I2S\_RX\_EOF\_NUM + 1). Once the received data reaches such bit length, an **AHB\_DMA\_IN\_SUC\_EOF\_CHn\_INT** interrupt is triggered in the configured GDMA RX channel. (R/W)

**Register 41.10. I2S\_TX\_CONF\_REG (0x0024)**

| (reserved) |    | I2S_SIG_LOOPBACK |    |    |    | I2S_TX_CHAN_MOD |    |    |    | I2S_TX_BCK_DIV_NUM |    |    |    | I2S_TX_PDM_EN |     | I2S_TX_TDM_EN |   | I2S_TX_BIT_ORDER |   | I2S_TX_WS_IDLE_POL |   | I2S_TX_24_FILL_EN |   | I2S_TX_LEFT_ALIGN |   | I2S_TX_BCK_MSB_SHIFT |       | I2S_TX_PCM_BYPASS |  | I2S_TX_PCM_CONF |  | I2S_TX_MONO_FST_VLD |  | I2S_TX_UPDATE |  | I2S_TX_BIG_ENDIAN |  | I2S_TX_MONO |  | I2S_TX_CHAN_EQUAL |  | I2S_TX_STOP_EN |  | I2S_TX_SLAVE_MOD |  | I2S_TX_FIFO_RESET |  |
|------------|----|------------------|----|----|----|-----------------|----|----|----|--------------------|----|----|----|---------------|-----|---------------|---|------------------|---|--------------------|---|-------------------|---|-------------------|---|----------------------|-------|-------------------|--|-----------------|--|---------------------|--|---------------|--|-------------------|--|-------------|--|-------------------|--|----------------|--|------------------|--|-------------------|--|
| 31         | 30 | 29               | 27 | 26 | 21 | 20              | 19 | 18 | 17 | 16                 | 15 | 14 | 13 | 12            | 11  | 10            | 9 | 8                | 7 | 6                  | 5 | 4                 | 3 | 2                 | 1 | 0                    |       |                   |  |                 |  |                     |  |               |  |                   |  |             |  |                   |  |                |  |                  |  |                   |  |
| 0          | 0  | 0                |    | 6  |    | 0               | 0  | 0  | 0  | 0                  | 1  | 1  | 1  | 1             | 0x0 | 1             | 0 | 0                | 0 | 0                  | 0 | 1                 | 0 | 0                 | 0 | 0                    | Reset |                   |  |                 |  |                     |  |               |  |                   |  |             |  |                   |  |                |  |                  |  |                   |  |

**I2S\_TX\_RESET** Configures whether to reset TX unit.

0: No effect

1: Reset

(WT)

**I2S\_TX\_FIFO\_RESET** Configures whether to reset TX FIFO.

0: No effect

1: Reset

(WT)

**I2S\_TX\_START** Configures whether to start transmitting data.

0: No effect

1: Start

(R/W/SC)

**I2S\_TX\_SLAVE\_MOD** Configures whether to enable slave TX mode.

0: Enable master mode

1: Enable slave mode

(R/W)

**I2S\_TX\_STOP\_EN** Configures whether to stop outputting the BCK signal and the WS signal when TX FIFO is empty.

0: No effect

1: Stop

(R/W)

**I2S\_TX\_CHAN\_EQUAL** Configures whether to equalize left channel data and right channel data in I2S TX mono mode or TDM mode.

0: The I2S\_SINGLE\_DATA is invalid channel data in I2S TX mono mode or TDM mode

1: The left channel data is equal to right channel data in I2S TX mono mode or TDM mode

(R/W)

**I2S\_TX\_MONO** Configures whether to enable TX unit in mono mode.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 41.10. I2S\_TX\_CONF\_REG (0x0024)**

Continued from the previous page...

**I2S\_TX\_BIG\_ENDIAN** Configures I2S TX byte endian.

0: Low address with low address value

1: Low address value to high address

(R/W)

**I2S\_TX\_UPDATE** Configures whether to update I2S TX registers from APB clock domain to I2S TX clock domain.

0: No effect

1: Update

This bit will be cleared by hardware after update register done.

(R/W/SC)

**I2S\_TX\_MONO\_FST\_VLD** Configures the valid data channel in I2S TX mono mode.

0: The second channel data valid

1: The first channel data valid

(R/W)

**I2S\_TX\_PCM\_CONF** Configures the I2S TX compress/decompress mode.

0 (atol): A-law decompress

1 (ltoa): A-law compress

2 (utol):  $\mu$ -law decompress

3 (ltou):  $\mu$ -law compress

(R/W)

**I2S\_TX\_PCM\_BYPASS** Configures whether to bypass Compress/Decompress units for transmitted data.

0: No effect

1: Bypass

(R/W)

**I2S\_TX\_MSB\_SHIFT** Configures the timing between the WS signal and the MSB of data.

0: Align at the rising edge

1: WS signal changes one BCK clock earlier

(R/W)

**I2S\_TX\_BCK\_NO\_DLY** Configures the source of the BCK rising and falling edges in master mode.

0: Rising and falling edges are constructed based on the BCK input from I2S<sub>n</sub>O\_BCK\_in

1: Rising and falling edges are constructed by dividing the clock of I2S<sub>n</sub> TX

(R/W)

**I2S\_TX\_LEFT\_ALIGN** Configures I2S TX alignment mode.

0: Right alignment mode

1: Left alignment mode

(R/W)

Continued on the next page...

**Register 41.10. I2S\_TX\_CONF\_REG (0x0024)**

Continued from the previous page...

**I2S\_TX\_24\_FILL\_EN** Configures the bit number that the 24 channel bits are stored to.

0: Store 24-bit channel data to 24 bits

1: Store 24-bit channel data to 32 bits (Extra bits are filled with zeros)

(R/W)

**I2S\_TX\_WS\_IDLE\_POL** Configures the relationship between WS and which channel data to transmit.

0: WS remains low when transmitting left channel data and high when transmitting right channel data

1: WS remains high when transmitting left channel data and low when transmitting right channel data

(R/W)

**I2S\_TX\_BIT\_ORDER** Configures whether to reverse the bit order of valid data to be sent by the I2S TX.

0: Not reverse

1: Reverse

(R/W)

**I2S\_TX\_TDM\_EN** Configures whether to enable I2S TDM TX mode.

0: Disable

1: Enable

(R/W)

**I2S\_TX\_PDM\_EN** Configures whether to enable I2S PDM TX mode.

0: Disable

1: Enable

(R/W)

**I2S\_TX\_BCK\_DIV\_NUM** Configures the divider of BCK in TX mode. Note this divider must not be configured to 1. (R/W)

**I2S\_TX\_CHAN\_MOD** Configures I2S TX channel mode. For more information, see Table [41.9-4](#).

(R/W)

**I2S\_SIG\_LOOPBACK** Configures whether to enable TX unit and RX unit sharing the same WS and BCK signals.

0: Disable

1: Enable

(R/W)



### Register 41.11. I2S\_TX\_CONF1\_REG (0x002C)

|                      |  |    |  |  |  |                         |  |    |  |  |  |                 |  |    |  |  |  |            |  |   |  |  |  |                     |  |   |  |  |  |       |
|----------------------|--|----|--|--|--|-------------------------|--|----|--|--|--|-----------------|--|----|--|--|--|------------|--|---|--|--|--|---------------------|--|---|--|--|--|-------|
| I2S_TX_TDM_CHAN_BITS |  |    |  |  |  | I2S_TX_HALF_SAMPLE_BITS |  |    |  |  |  | I2S_TX_BITS_MOD |  |    |  |  |  | (reserved) |  |   |  |  |  | I2S_TX_TDM_WS_WIDTH |  |   |  |  |  |       |
| 31                   |  | 27 |  |  |  | 26                      |  | 19 |  |  |  | 18              |  | 14 |  |  |  | 13         |  | 9 |  |  |  | 8                   |  | 0 |  |  |  |       |
| 0xf                  |  |    |  |  |  | 0xf                     |  |    |  |  |  | 0xf             |  |    |  |  |  | 0 0 0 0 0  |  |   |  |  |  | 0x0                 |  |   |  |  |  | Reset |

**I2S\_TX\_TDM\_WS\_WIDTH** Configures the width of I2S<sub>TX</sub> WS\_out (WS default level) at idle level in TDM mode. The width of I2S<sub>TX</sub> WS\_out at idle level in TDM mode = (I2S\_TX\_TDM\_WS\_WIDTH[8:0] + 1) x T\_BCK. (R/W)

**I2S\_TX\_BITS\_MOD** Configures the valid data bit length of I2S TX channel.

- 7: All the valid channel data is in 8-bit mode  
15: All the valid channel data is in 16-bit mode  
23: All the valid channel data is in 24-bit mode  
31: All the valid channel data is in 32-bit mode  
Other values are invalid.  
(R/W)

**I2S\_TX\_HALF\_SAMPLE\_BITS** Configures I2S TX sample bits. BCK cycles in one WS period = I2S\_TX\_HALF\_SAMPLE\_BITS x 2. (R/W)

**I2S\_TX\_TDM\_CHAN\_BITS** Configures TX bit number for each channel in TDM mode. Bit number expected = I2S\_TX\_TDM\_CHAN\_BITS + 1. (R/W)

**Register 41.12. I2S\_TX\_PCM2PDM\_CONF\_REG (for I2S0 only) (0x0040)**

|            |    |   |   |   |   |    |                     |    |    |    |                        |     |     |     |                        |    |    |    |            |     |  |  |  |  |   |                      |  |   |  |  |  |  |            |  |
|------------|----|---|---|---|---|----|---------------------|----|----|----|------------------------|-----|-----|-----|------------------------|----|----|----|------------|-----|--|--|--|--|---|----------------------|--|---|--|--|--|--|------------|--|
| (reserved) |    |   |   |   |   |    | I2S_PCM2PDM_CONV_EN |    |    |    | I2S_TX_PDM_DAC_MODE_EN |     |     |     | I2S_TX_PDM_DAC_2OUT_EN |    |    |    | (reserved) |     |  |  |  |  |   | I2S_TX_PDM_SINC_OSR2 |  |   |  |  |  |  | (reserved) |  |
| 31         | 26 |   |   |   |   | 25 | 24                  | 23 | 22 | 21 | 20                     | 19  | 18  | 17  | 16                     | 15 | 14 | 13 | 12         | 5   |  |  |  |  | 4 | 1                    |  | 0 |  |  |  |  |            |  |
| 0          | 0  | 0 | 0 | 0 | 0 | 0  | 0                   | 0  | 1  | 0  | 0x1                    | 0x1 | 0x1 | 0x1 | 0x0                    |    |    |    |            | 0x2 |  |  |  |  | 0 | Reset                |  |   |  |  |  |  |            |  |

**I2S\_TX\_PDM\_SINC\_OSR2** Configures I2S TX PDM OSR value. (R/W)

**I2S\_TX\_PDM\_DAC\_2OUT\_EN** Configures whether to enable I2S TX PDM DAC mode.

0: Enable 1-line DAC output mode

1: Enable 2-line DAC output mode

Only valid when I2S\_TX\_PDM\_DAC\_MODE\_EN is set.

(R/W)

**I2S\_TX\_PDM\_DAC\_MODE\_EN** Configures whether to enable 1-line PDM output mode or DAC output mode.

0: Enable 1-line PDM output mode

1: Enable DAC output mode

(R/W)

**I2S\_PCM2PDM\_CONV\_EN** Configures whether to enable the I2S TX PCM-to-PDM converter.

0: Disable

1: Enable

(R/W)

**Register 41.13. I2S\_TX\_PCM2PDM\_CONF1\_REG (0x0044)**

|            |  |  |  |  |  |  |            |  |  |  |  |  |  |            |  |      |  |            |  |  |  |               |  |  |  |  |  |  |  |       |  |  |  |
|------------|--|--|--|--|--|--|------------|--|--|--|--|--|--|------------|--|------|--|------------|--|--|--|---------------|--|--|--|--|--|--|--|-------|--|--|--|
| (reserved) |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  | (reserved) |  |      |  | (reserved) |  |  |  | I2S_TX_PDM_FP |  |  |  |  |  |  |  |       |  |  |  |
| 3126       |  |  |  |  |  |  | 3126       |  |  |  |  |  |  | 2523       |  | 2220 |  | 90         |  |  |  |               |  |  |  |  |  |  |  |       |  |  |  |
| 0000000    |  |  |  |  |  |  | 0000000    |  |  |  |  |  |  | 7          |  | 7    |  | 960        |  |  |  |               |  |  |  |  |  |  |  | Reset |  |  |  |

**I2S\_TX\_PDM\_FS** Configures I2S PDM TX upsampling parameter. (R/W)

**Register 41.14. I2S\_TX\_TDM\_CTRL\_REG (0x0054)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  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0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  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| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**I2S\_TX\_TDM\_CHAN $n$ \_EN ( $n$ : 0-15)** Configures whether to enable the valid data output of I2S TX TDM channel  $n$ .

0: Channel TX data is controlled by [I2S\\_TX\\_CHAN\\_EQUAL](#) and [I2S\\_SINGLE\\_DATA](#). See Section [41.9.2.1](#)

1: Enable

(R/W)

**I2S\_TX\_TDM\_TOT\_CHAN\_NUM** Configures the total number of channels in use in I2S TX TDM mode.

Total channel number in use = I2S\_TX\_TDM\_TOT\_CHAN\_NUM + 1. (R/W)

**I2S\_TX\_TDM\_SKIP\_MSK\_EN** Configures the data to be sent in GDMA TX buffer.

0: Data stored in GDMA TX buffer is used by enabled channels and will not be read by channels that are not enabled.

1: Data stored in GDMA TX buffer is read by all channels and will be skipped by channels that are not enabled.

(R/W)

Register 41.15. I2S\_RX\_TIMING\_REG (0x0058)

|            |    |                  |    |            |     |                 |    |            |    |                   |     |            |    |                  |    |            |     |                  |    |            |    |                  |     |            |   |                  |   |            |     |                 |   |
|------------|----|------------------|----|------------|-----|-----------------|----|------------|----|-------------------|-----|------------|----|------------------|----|------------|-----|------------------|----|------------|----|------------------|-----|------------|---|------------------|---|------------|-----|-----------------|---|
| (reserved) |    | I2S_RX_BCK_IN_DM |    | (reserved) |     | I2S_RX_WS_IN_DM |    | (reserved) |    | I2S_RX_BCK_OUT_DM |     | (reserved) |    | I2S_RX_WS_OUT_DM |    | (reserved) |     | I2S_RX_SD3_IN_DM |    | (reserved) |    | I2S_RX_SD2_IN_DM |     | (reserved) |   | I2S_RX_SD1_IN_DM |   | (reserved) |     | I2S_RX_SD_IN_DM |   |
| 31         | 30 | 29               | 28 | 27         | 26  | 25              | 24 | 23         | 22 | 21                | 20  | 19         | 18 | 17               | 16 | 15         | 14  | 13               | 12 | 11         | 10 | 9                | 8   | 7          | 6 | 5                | 4 | 3          | 2   | 1               | 0 |
| 0          | 0  | 0x0              | 0  | 0          | 0x0 | 0               | 0  | 0x0        | 0  | 0                 | 0x0 | 0          | 0  | 0x0              | 0  | 0          | 0x0 | 0                | 0  | 0x0        | 0  | 0                | 0x0 | 0          | 0 | 0x0              | 0 | 0          | 0x0 | 0               | 0 |

Reset

**I2S\_RX\_SD\_IN\_DM** Configures the delay mode of I2S RX SD input signal.

0: Bypass

1: Delay by rising edge

2: Delay by falling edge

3: Reserved

(R/W)

**I2S\_RX\_SD1\_IN\_DM (for I2S0 only)** Configures the delay mode of I2S RX SD1 input signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_SD2\_IN\_DM (for I2S0 only)** Configures the delay mode of I2S RX SD2 input signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_SD3\_IN\_DM (for I2S0 only)** Configures the delay mode of I2S RX SD3 input signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_WS\_OUT\_DM** Configures the delay mode of I2S RX WS output signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_BCK\_OUT\_DM** Configures the delay mode of I2S RX BCK output signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_WS\_IN\_DM** Configures the delay mode of I2S RX WS input signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**I2S\_RX\_BCK\_IN\_DM** Configures the delay mode of I2S RX BCK input signal. For detailed configuration values, please refer to [I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

Register 41.16. I2S\_TX\_TIMING\_REG (0x005C)

|            |    |                  |    |            |    |                 |    |            |    |                   |    |            |    |                  |    |            |   |   |   |   |   |   |   |   |   |                   |   |            |   |                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|----|------------------|----|------------|----|-----------------|----|------------|----|-------------------|----|------------|----|------------------|----|------------|---|---|---|---|---|---|---|---|---|-------------------|---|------------|---|------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |    | I2S_TX_BCK_IN_DM |    | (reserved) |    | I2S_TX_WS_IN_DM |    | (reserved) |    | I2S_TX_BCK_OUT_DM |    | (reserved) |    | I2S_TX_WS_OUT_DM |    | (reserved) |   |   |   |   |   |   |   |   |   | I2S_TX_SD1_OUT_DM |   | (reserved) |   | I2S_TX_SD_OUT_DM |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         | 30 | 29               | 28 | 27         | 26 | 25              | 24 | 23         | 22 | 21                | 20 | 19         | 18 | 17               | 16 | 15         |   |   |   |   |   |   |   |   |   |                   | 6 | 5          | 4 | 3                | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0  | 0x0              |    | 0          | 0  | 0x0             |    | 0          | 0  | 0x0               |    | 0          | 0  | 0x0              |    | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                 | 0 | 0          | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**I2S\_TX\_SD\_OUT\_DM** Configures the delay mode of I2S TX SD output signal.

- 0: Bypass
  - 1: Delay by rising edge
  - 2: Delay by falling edge
  - 3: Reserved
- (R/W)

**I2S\_TX\_SD1\_OUT\_DM (for I2S0 only)** Configures the delay mode of I2S TX SD1 output signal. For detailed configuration values, please refer to [I2S\\_TX\\_SD\\_OUT\\_DM](#). (R/W)

**I2S\_TX\_WS\_OUT\_DM** Configures the delay mode of I2S TX WS output signal. For detailed configuration values, please refer to [I2S\\_TX\\_SD\\_OUT\\_DM](#). (R/W)

**I2S\_TX\_BCK\_OUT\_DM** Configures the delay mode of I2S TX BCK output signal. For detailed configuration values, please refer to [I2S\\_TX\\_SD\\_OUT\\_DM](#). (R/W)

**I2S\_TX\_WS\_IN\_DM** Configures the delay mode of I2S TX WS input signal. For detailed configuration values, please refer to [I2S\\_TX\\_SD\\_OUT\\_DM](#). (R/W)

**I2S\_TX\_BCK\_IN\_DM** Configures the delay mode of I2S TX BCK input signal. For detailed configuration values, please refer to [I2S\\_TX\\_SD\\_OUT\\_DM](#). (R/W)

**Register 41.17. I2S\_LC\_HUNG\_CONF\_REG (0x0060)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |   |  |      |                           |    |  |       |                     |   |   |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|---|--|------|---------------------------|----|--|-------|---------------------|---|---|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | I2S_LC_FIFO_TIMEOUT_ENA |   |  |      | I2S_LC_FIFO_TIMEOUT_SHIFT |    |  |       | I2S_LC_FIFO_TIMEOUT |   |   |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 12                      |   |  |      | 11                        | 10 |  | 8     |                     | 7 | 0 |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1                       | 0 |  | 0x10 |                           |    |  | Reset |                     |   |   |  |  |  |

**I2S\_LC\_FIFO\_TIMEOUT** Configures FIFO timeout threshold. The FIFO hung counter is incremented by one each time I2S is in an error state and the tick counter reaches its threshold. [I2S\\_TX\\_HUNG\\_INT](#) or [I2S\\_RX\\_HUNG\\_INT](#) interrupt will be triggered when FIFO hung counter is equal to the FIFO timeout threshold. (R/W)

**I2S\_LC\_FIFO\_TIMEOUT\_SHIFT** Configures tick counter threshold. The tick counter is incremented by one each time I2S is in an error state and it is on the rising edge in each system clock (APB). The tick counter is reset when counter value  $\geq 88000/2^{I2S\_LC\_FIFO\_TIMEOUT\_SHIFT}$ . (R/W)

**I2S\_LC\_FIFO\_TIMEOUT\_ENA** Configures whether to enable FIFO timeout.

0: Disable

1: Enable

(R/W)

**Register 41.18. I2S\_CONF\_SIGLE\_DATA\_REG (0x0068)**

|                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| I2S_SINGLE_DATA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
|                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 | Reset |

**I2S\_SINGLE\_DATA** Configures constant channel data to be sent out. (R/W)

Register 41.19. I2S\_STATE\_REG (0x006C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | I2S_TX_IDLE |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1           | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1           | Reset |

**I2S\_TX\_IDLE** Represents the TX unit state.

- 0: I2S TX unit is working
- 1: I2S TX unit is in idle state

(RO)

Register 41.20. I2S\_ETM\_CONF\_REG (0x0070)

|            |   |   |   |   |   |   |   |   |   |   |   |                             |      |  |  |  |  |  |    |   |      |  |  |                          |  |  |  |   |       |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|-----------------------------|------|--|--|--|--|--|----|---|------|--|--|--------------------------|--|--|--|---|-------|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | I2S_ETM_RX_RECEIVE_WORD_NUM |      |  |  |  |  |  |    |   |      |  |  | I2S_ETM_TX_SEND_WORD_NUM |  |  |  |   |       |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 20                          | 19   |  |  |  |  |  | 10 | 9 |      |  |  |                          |  |  |  | 0 |       |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                           | 0x40 |  |  |  |  |  |    |   | 0x40 |  |  |                          |  |  |  |   | Reset |  |  |  |  |  |  |

**I2S\_ETM\_TX\_SEND\_WORD\_NUM** Configures the threshold of triggering ETM [I2S\\_TX\\_X\\_WORDS\\_SENT](#) event. When transmitting word number of I2S\_ETM\_TX\_SEND\_WORD\_NUM [9:0], I2S will trigger the corresponding ETM event. (R/W)

**I2S\_ETM\_RX\_RECEIVE\_WORD\_NUM** Configures the threshold of triggering [ETM I2S\\_RX\\_X\\_WORDS\\_RECEIVED](#) event. When receiving word number of I2S\_ETM\_RX\_RECEIVE\_WORD\_NUM [9:0], I2S will trigger the corresponding ETM event. (R/W)

### Register 41.21. I2S\_FIFO\_CNT\_REG (0x0074)

|    |          |   |
|----|----------|---|
| 31 | 30       | 0 |
| 0  | 0x000000 |   |

Reset

**I2S\_TX\_FIFO\_CNT** Configures the TX FIFO counter value. (RO)

**I2S\_TX\_FIFO\_CNT\_RST** Configure whether to reset the TX FIFO counter.

0: No effect

1: Reset

(WT)

### Register 41.22. I2S\_BCK\_CNT\_REG (0x0078)

Diagram illustrating the I2S\_TX\_BCK\_CNT register structure. The register is 32 bits wide. Bit 31 is labeled I2S\_TX\_BCK\_CNT\_RST. Bits 30 to 0 are labeled I2S\_TX\_BCK\_CNT. The reset value is 0x000000.

**I2S\_TX\_BCK\_CNT** Configures the TX BCK counter value. (RO)

**I2S\_TX\_BCK\_CNT\_RST** Configures whether to reset TC BCK counter.

0: No effect

1: Reset

(WT)

### Register 41.23. I2S\_CLK\_GATE\_REG (0x007C)

Register 0x00000000 (I2S\_CLK\_EN) bit field diagram. The register is 32 bits wide. Bit 31 is labeled 'reserved'. Bit 0 is labeled 'I2S\_CLK\_EN'. The register is reset to 0.

**I2S\_CLK\_EN** Configures whether to enable clock gate.

0: Disable

1: Enable

(R/W)



Register 41.24. I2S\_DATE\_REG (0x0080)

|            |   |    |    |           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|---|----|----|-----------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |   |    |    | I2S_DATE  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |   | 28 | 27 |           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0  | 0  | 0x2303240 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

I2S\_DATE Version control register. (R/W)

## Chapter 42

### LP I2S Controller

#### 42.1 Introduction

ESP32-P4 has a built-in LP I2S interface, which provides a data reception communication interface for [Voice Activity Detection \(VAD\)](#) and some digital audio applications in low power mode.

The I2S standard bus defines three signals, namely, a bit clock signal (BCK), a channel/word select signal (WS), and a serial data signal (SD). A basic I2S data bus has one master and one slave. The roles remain unchanged throughout the communication.

The LP I2S module on ESP32-P4 provides an independent RX unit, which supports receiving data when the chip is running with the lowest power consumption. Compared to HP I2S, i.e., I2S<sub>O</sub>, I2S<sub>1</sub>, and I2S<sub>2</sub>, LP I2S does not support DMA access. Instead, it uses a separate internal memory to store data.

**Note:**

For I2S-related terminology, refer to the Section [41.2 Terminology](#) in Chapter [41 I2S Controller \(I2S\)](#).

#### 42.2 Feature List

The LP I2S module has the following features:

- RX master mode and slave mode
- A variety of audio standards supported:
  - TDM Philips standard
  - TDM MSB alignment standard
  - TDM PCM standard
  - PDM standard
- Various RX modes supported:
  - TDM RX mode, up to 2 channels supported
  - PDM RX mode
    - \* Raw PDM data reception
    - \* PDM-to-PCM data format conversion, up to 2 channels supported
- Configurable sample clock with a variety of sampling frequencies supported
- 16-bit data communication

- Standard LP I2S interface interrupts

## 42.3 Architectural Overview

Figure 42.3-1 shows the structure of the ESP32-P4 LP I2S module, consisting of:

- Receive control unit (RX Unit)
- Input and output timing unit (I/O Sync)
- Clock divider (Clock Generator)
- 64 x 32-bit RX FIFO
- 256 x 32-bit LP I2S Memory
- Communication interface for Voice Activity Detection (VAD)

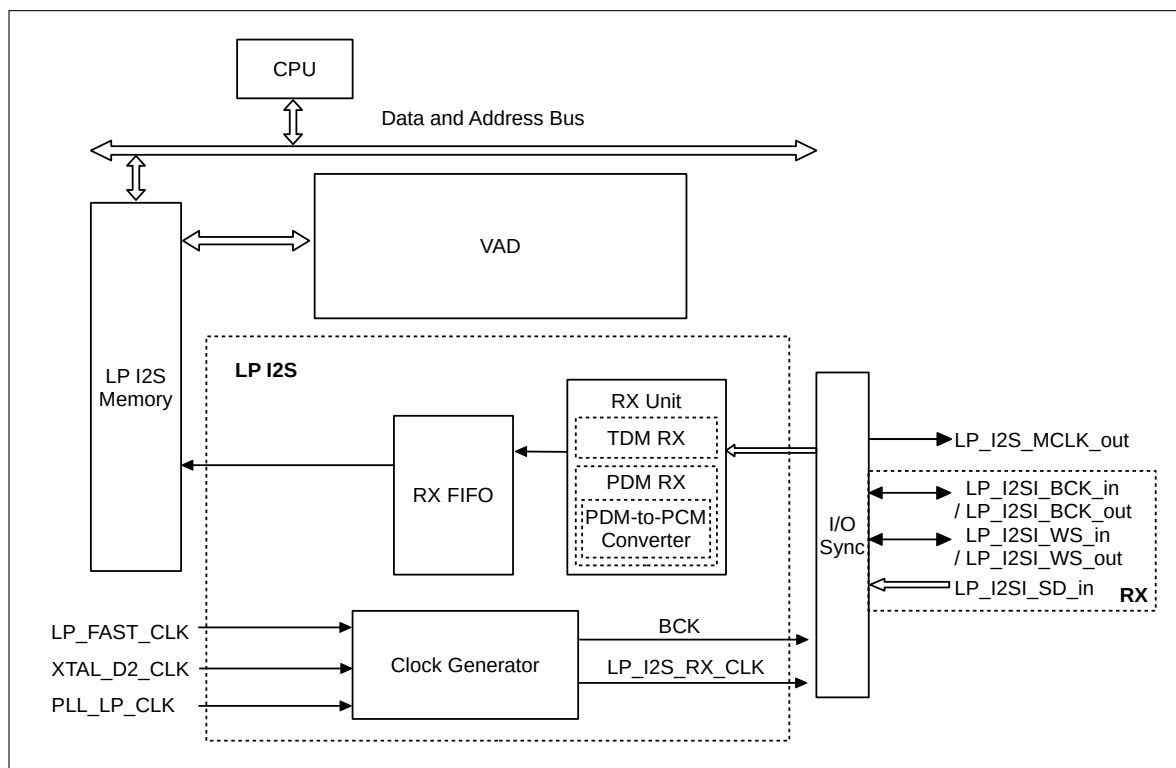


Figure 42.3-1. ESP32-P4 LP I2S Architecture

The RX unit have a three-line interface that uses a bit clock line (BCK), a word select line (WS), and a serial data line (SD). The SD line of the RX unit is dedicated for data input. BCK and WS signal lines for the RX unit can be configured as master output mode or slave input mode.

The signal bus of the LP I2S module is shown at the right part of Figure 42.3-1. The naming of these signals in RX units follows the pattern of LP\_I2SA\_B\_C, for example, LP\_I2SI\_BCK\_in.

- “A” is fixed to “I”, indicating that signals are input to the RX unit
- “B” represents the signal function, which includes:
  - BCK

- WS
- SD
- “C” represents the signal direction, which includes:
  - “in”: Input signal into the LP I2S module
  - “out”: Output signal from the LP I2S module

Table 42.3-1 provides a detailed description of LP I2S signals.

**Table 42.3-1. LP I2S Signal Description**

| Signal <sup>*</sup> | Direction | Function  |
|---------------------|-----------|---|
| LP_I2SI_BCK_in      | Input     | In LP I2S slave mode, inputs BCK signal for RX unit   |
| LP_I2SI_BCK_out     | Output    | In LP I2S master mode, outputs BCK signal for RX unit |
| LP_I2SI_WS_in       | Input     | In LP I2S slave mode, inputs WS signal for RX unit    |
| LP_I2SI_WS_out      | Output    | In LP I2S master mode, outputs WS signal for RX unit  |
| LP_I2SI_SD_in       | Input     | Serial input data bus for LP I2S RX unit              |
| LP_I2S_MCLK_out     | Output    | LP I2S master clock output                            |

<sup>\*</sup> Any required signals of LP I2S must be mapped to the chip's pins via LP GPIO matrix. See Chapter 8 [GPIO Matrix and IO MUX](#).

## 42.4 Supported Audio Standards

ESP32-P4 I2S supports multiple audio standards, including TDM Philips standard, TDM MSB alignment standard, TDM PCM standard, and PDM standard.

Select the needed standard by configuring the following bits:

- [LP\\_I2S\\_RX\\_TDM\\_EN](#)
  - 0: Disable TDM mode
  - 1: Enable TDM mode
- [LP\\_I2S\\_RX\\_PDM\\_EN](#)
  - 0: Disable PDM mode
  - 1: Enable PDM mode
- [LP\\_I2S\\_RX\\_MSB\\_SHIFT](#)
  - 0: WS and SD signals change simultaneously, i.e., enable MSB alignment standard
  - 1: WS signal changes one BCK clock cycle earlier than SD signal, i.e., enable Philips standard or select PCM standard

**Note:**

[LP\\_I2S\\_RX\\_TDM\\_EN](#) and [LP\\_I2S\\_RX\\_PDM\\_EN](#) must not be configured to 1 or 0 at the same time, otherwise LP I2S will transmit data incorrectly in a mode that is neither TDM nor PDM.

### 42.4.1 TDM Philips Standard

Philips standards require that WS signal changes one BCK clock cycle earlier than SD signal on BCK falling edge, which means that WS signal is valid from one clock cycle before transmitting the first bit of channel data and changes one clock before the end of channel data transfer. SD signal line transmits the most significant bit of audio data first.

Compared with the basic Philips standard, TDM Philips standard supports multiple channels. See Figure 42.4-1.

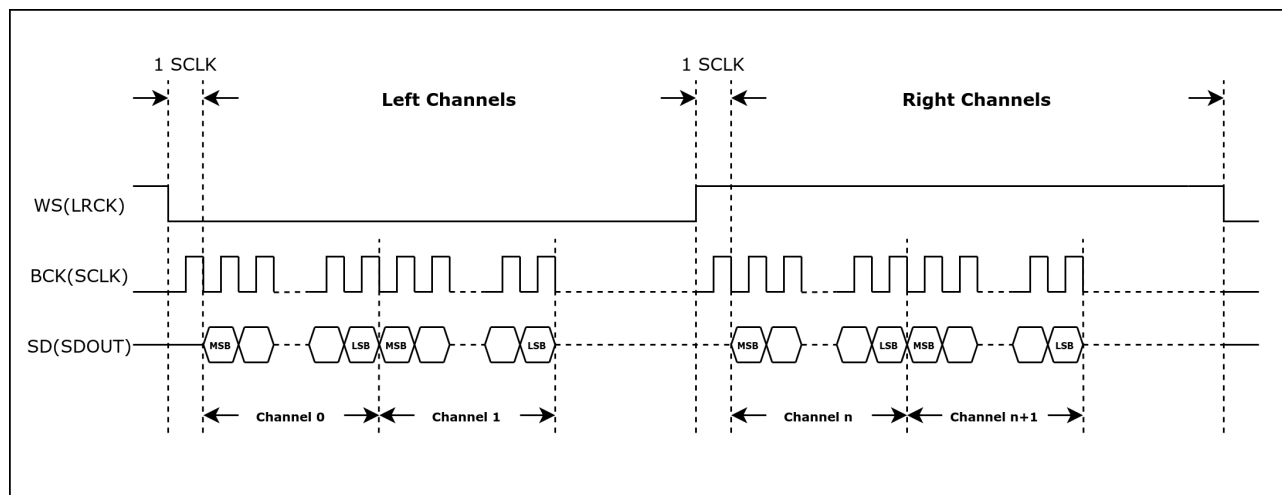


Figure 42.4-1. TDM Philips Standard Timing Diagram

### 42.4.2 TDM MSB Alignment Standard

MSB alignment standards require that WS and SD signals change simultaneously on the falling edge of BCK. The WS signal is valid until the end of the channel data transfer. The SD signal line transmits the most significant bit of audio data first.

Compared with the basic MSB alignment standard, TDM MSB alignment standard supports multiple channels. See Figure 42.4-2.

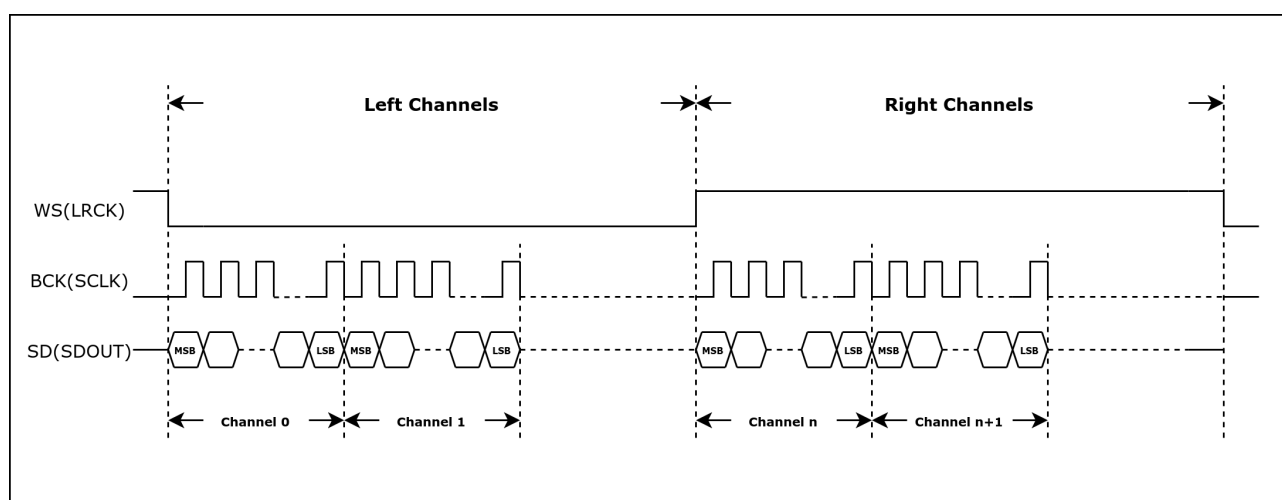


Figure 42.4-2. TDM MSB Alignment Standard Timing Diagram

### 42.4.3 TDM PCM Standard

Short frame synchronization under the PCM standards requires that the WS signal changes one BCK clock cycle earlier than the SD signal on the falling edge of BCK, which means that the WS signal becomes valid one clock cycle before transferring the first bit of channel data and remains unchanged in this BCK clock cycle. SD signal line first transmits the most significant bit of audio data.

Compared with the basic PCM standard, TDM PCM standard supports multiple channels. See Figure 42.4-3.

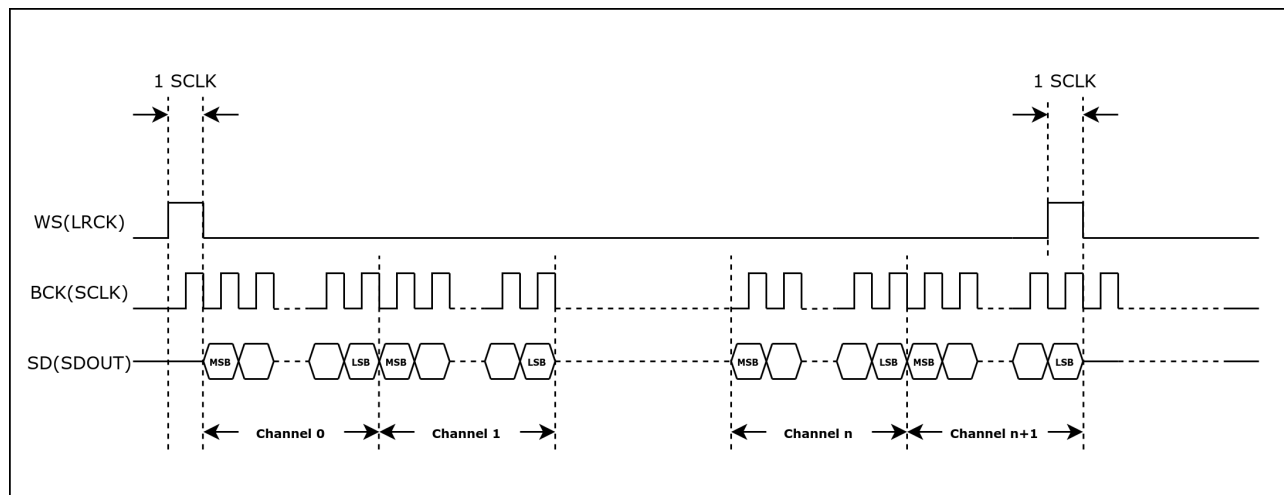


Figure 42.4-3. TDM PCM Standard Timing Diagram

### 42.4.4 PDM Standard

Under PDM standard, WS signal changes continuously during data transmission. The low-level and high-level of this signal indicates the left channel and right channel respectively. WS and SD signals change simultaneously on the falling edge of BCK. See Figure 42.4-4.

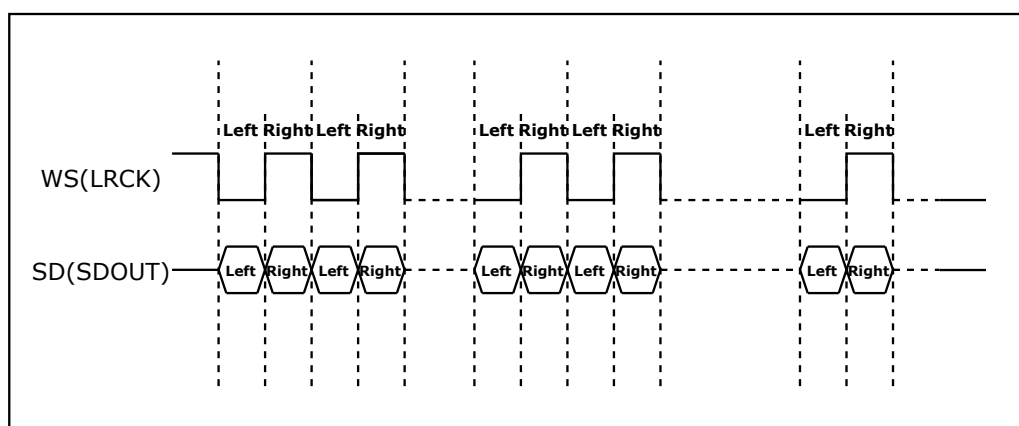


Figure 42.4-4. PDM Standard Timing Diagram

## 42.5 RX Clock

LP\_I2S\_RX\_CLK is the master clock of LP I2S RX unit, divided from:

- Up to 40 MHz LP\_FAST\_CLK with configurable clock source
- 20 MHz XTAL\_D2\_CLK
- 8 MHz PLL\_LP\_CLK

The serial clock (BCK) of the LP I2S RX unit is divided from LP\_I2S\_RX\_CLK, as shown in Figure 42.5-1.

[LPPERI\\_LP\\_I2S\\_RX\\_CLK\\_SEL](#) is used to select clock source for the LP I2S RX unit, and [LPPERI\\_CK\\_EN\\_LP\\_I2S\\_RX](#) to enable or disable the clock source.

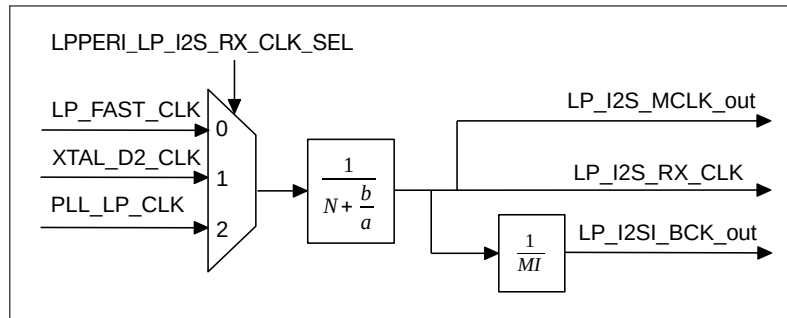


Figure 42.5-1. LP I2S Clock Generator

The following formula shows the relation between LP\_I2S\_RX\_CLK frequency  $f_{LP\_I2S\_RX\_CLK}$  and the divider clock source frequency  $f_{LP\_I2S\_CLK\_S}$ :

$$f_{LP\_I2S\_RX\_CLK} = \frac{f_{LP\_I2S\_CLK\_S}}{N + \frac{b}{a}}$$

N is an integer value between 2 and 256. The value of N is mapped to that of [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_N](#) as follows:

- When [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_N](#) = 0, N = 256;
- When [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_N](#) = 1, N = 2;
- When [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_N](#) has any other value, N = [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_NUM](#).

The values of “a” and “b” in fractional divider depend only on x, y, z, and yn1. The corresponding formulas are as follows:

- When  $b \leq \frac{a}{2}$ ,  $yn1 = 0$ ,  $x = \text{floor}(\lceil \frac{a}{b} \rceil) - 1$ ,  $y = a \% b$ ,  $z = b$ ;
- When  $b > \frac{a}{2}$ ,  $yn1 = 1$ ,  $x = \text{floor}(\lceil \frac{a}{a-b} \rceil) - 1$ ,  $y = a \% (a - b)$ ,  $z = a - b$ .

The values of x, y, z, and yn1 are configured by [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_X](#), [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_Y](#), [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_Z](#) and [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_YN1](#).

To configure the integer divider, clear [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_X](#) and [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_Z](#), then set [LPPERI\\_LP\\_I2S\\_RX\\_CLKM\\_DIV\\_Y](#) to 1.

**Note:**

Using fractional divider may introduce some clock jitter.

In master RX mode, the serial clock BCK for LP I2S RX unit is LP\_I2SI\_BCK\_out divided from LP\_I2S\_RX\_CLK, which is:

$$f_{LP\_I2S\_BCK\_out} = \frac{f_{LP\_I2S\_RX\_CLK}}{MI}$$

“MI” is an integer value:

$$MI = LP\_I2S\_RX\_BCK\_DIV\_NUM + 1$$

**Note:**

`LP_I2S_RX_BCK_DIV_NUM` must not be configured as 1.

In LP I2S slave mode, make sure  $f_{LP\_I2S\_RX\_CLK} \geq 8 \times f_{BCK}$  to ensure the sampling accuracy. The LP I2S module can output `LP_I2S_MCLK_out` as the master clock for peripherals.

Since in slave mode, the module clock frequency must be greater than or equal to 8 times the BCK clock frequency, the maximum sampling frequency of LP I2S is limited by the data bit width and the number of channels. For example, since the clock source frequency is up to 40 MHz, the module clock can be configured up to 20 MHz, and the BCK clock can be configured up to 5 MHz. Therefore, when transmitting dual-channel 16-bit width data, LP I2S supports sample frequencies up to 78.125 kHz, e.g., 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz. For detailed information, please refer to Section [42.5 RX Clock](#).

In addition to the clock frequency limitation, LP I2S uses LP I2S internal memory for data storage instead of DMA. Therefore, users need to read data from the LP I2S internal memory in a timely manner. The reading rate may limit the sample frequencies that LP I2S supports. For detailed information, please refer to Section [42.8.3 Internal Memory](#).

## 42.6 Reset

The units and FIFOs in the LP I2S module are reset by the following bits.

- LP I2S RX units: Reset by the bit `LP_I2S_RX_RESET`;
- LP I2S RX FIFO: Reset by the bits `LP_I2S_RX_FIFO_RESET`.

**Note:**

The LP I2S module clock must be configured first before the units and FIFO are reset.

## 42.7 Master/Slave RX Mode

The LP I2S supports receiving data either as a master or as a slave in RX mode.

- LP I2S works as a master receiver:
  - Set `LP_I2S_RX_START` to start receiving data. When this bit is set, the RX unit keeps outputting clock signal and sampling input data.
  - Configure `LP_I2S_RX_STOP_MODE` to control the suspension of data reception:
    - \* 0: The RX unit only suspends data reception when `LP_I2S_RX_START` is cleared.
    - \* 1: The RX unit suspends data reception when `LP_I2S_RX_START` is cleared or the number of received bytes is greater than the value configured in `LP_I2S_RX_EOF_NUM_REG`. After data



reception is suspended, if `LP_I2S_RX_START` is not cleared, data reception can be restarted by setting `LP_I2S_RX_RESET` to 1.

- RX unit stops receiving data when the bit `LP_I2S_RX_START` is cleared.
- LP I2S works as a slave receiver:
  - Set `LP_I2S_RX_START`. Wait for the master BCK signal to start receiving data.
  - Configure `LP_I2S_RX_STOP_MODE` to control data reception suspension:
    - \* 0: The RX unit only suspends data reception when `LP_I2S_RX_START` is cleared.
    - \* 1: The RX unit suspends data reception when `LP_I2S_RX_START` is cleared or the number of received bytes is greater than the value configured in `LP_I2S_RX_EOF_NUM_REG`. After data reception is suspended, if `LP_I2S_RX_START` is not cleared, data reception can be restarted by setting `LP_I2S_RX_RESET` to 1.
  - The RX unit stops receiving data when the bit `LP_I2S_RX_START` is cleared.

## 42.8 Receiving Data

In RX mode, LP I2S first reads data from the peripheral interface and then stores the data in the LP I2S memory according to the configured channel mode and data mode.

### 42.8.1 Channel Mode Control

ESP32-P4 LP I2S supports both TDM RX mode and PDM RX mode. Set `LP_I2S_RX_TDM_EN` to enable TDM RX mode, or set `LP_I2S_RX_PDM_EN` to enable PDM RX mode.

**Note:**

`LP_I2S_RX_TDM_EN` and `LP_I2S_RX_PDM_EN` must not be cleared or set simultaneously.

#### 42.8.1.1 TDM RX Mode

In TDM RX mode, LP I2S supports up to 2 channels to input data. The total number of RX channels in use is controlled by `LP_I2S_RX_TDM_TOT_CHAN_NUM`. For example, if `LP_I2S_RX_TDM_TOT_CHAN_NUM` is set to 1, channel 0 ~ 1 will be used to receive data.

In these RX channels, if `LP_I2S_RX_TDM_PDM_CHANn_EN` is set to:

- 0: The channel data is invalid and will not be stored into RX FIFO;
- 1: The channel data is valid and will be stored into RX FIFO.

In TDM master mode, WS signal is controlled by `LP_I2S_RX_WS_IDLE_POL` and `LP_I2S_RX_TDM_WS_WIDTH`.

- `LP_I2S_RX_WS_IDLE_POL`: The default level of WS signal;
- `LP_I2S_RX_TDM_WS_WIDTH`: The cycles the WS default level lasts for when receiving all channel data.

`LP_I2S_RX_HALF_SAMPLE_BITS` x 2 is equal to the BCK cycles in one WS period.

### 42.8.1.2 PDM RX Mode

In PDM RX mode, LP I2S converts the serial data from channels to the data to be entered into memory. LP I2S supports both PDM raw data reception and PDM-to-PCM data format conversion.

In PDM RX master mode, the default level of the WS signal is controlled by [LP\\_I2S\\_RX\\_WS\\_IDLE\\_POL](#). WS frequency is half of the BCK frequency. The configuration of the BCK signal is similar to that of WS signal as described in Section 42.5. Note, in PDM RX mode, the value of [LP\\_I2S\\_RX\\_HALF\\_SAMPLE\\_BITS](#) must be same as that of [LP\\_I2S\\_RX\\_BITS\\_MOD](#).

When the PDM-to-PCM converter is enabled for LP I2S, the received PDM data is converted to PCM data and controlled according to the data mode. Configure [LP\\_I2S\\_RX\\_PDM2PCM\\_EN](#) to enable this converter. The register configuration for PDM-to-PCM converter is as follows:

- Configure sampling frequency and downsampling rate.

When LP I2S PDM-to-PCM converter is enabled, PDM clock frequency is:

- in master mode: PDM clock frequency is equal to BCK frequency.
- in slave mode: PDM clock is provided by external device.

The sampling frequency ( $f_{\text{Sampling}}$ ) is related to PDM clock frequency as follows:

$$f_{\text{Sampling}} = \frac{f_{\text{PDM}}}{\text{DSR}}$$

Downsampling rate (DSR) is related to [LP\\_I2S\\_RX\\_PDM\\_SINC\\_DSR\\_16\\_EN](#) as follows:

$$\text{DSR} = \text{LP\_I2S\_RX\_PDM\_SINC\_DSR\_16\_EN} \times 64$$

Configure the registers according to needed master/slave mode, sampling frequency, and downsampling rate.

- Configure valid channels.

When the PDM-to-PCM converter is enabled, input signals from eight channels are supported at most. See Table 42.8-1 for the register configuration and related channels.

Table 42.8-1. PDM-to-PCM Data Input

| Input Data Signal | Channel       | Enable Register                            |
|-------------------|---------------|--|
| LP_I2SI_SD_in     | Left channel  | <a href="#">LP_I2S_RX_TDM_PDM_CHANO_EN</a> |
|                   | Right channel | <a href="#">LP_I2S_RX_TDM_PDM_CHAN1_EN</a> |

## 42.8.2 Data Format Control

The data format of LP I2S is controlled in the following phases:

- Phase I: Serial input data is converted into the data to be saved to RX FIFO;
- Phase II: The data is read from RX FIFO and converted according to the input data mode.

### 42.8.2.1 Bit Order Control of Channel Data

The channel data will be stored as the data to be input in order from high to low. The data bit order in each channel is controlled by [LP\\_I2S\\_RX\\_BIT\\_ORDER](#):

- 0: The bit order of the data to be input is not reversed;
- 1: The bit order of the data to be input is reversed.

At this point, the first phase of data format control is completed.

#### 42.8.2.2 Bit Width Control of Channel RX Data

The storage data width in each channel is controlled by [LP\\_I2S\\_RX\\_BITS\\_MOD](#). For ESP32-P4 LP I2S, the value of [LP\\_I2S\\_RX\\_BITS\\_MOD](#) is fixed as 15. The corresponding channel storage data width is 16 bit.

#### 42.8.2.3 Bit Width Control of Channel RX Data

The RX data width in each channel is determined by [LP\\_I2S\\_RX\\_TDM\\_CHAN\\_BITS](#).

- If the storage data width in each channel is smaller than the received (RX) data width, then only the bits within the storage data width is saved into memory. Configure [LP\\_I2S\\_RX\\_LEFT\\_ALIGN](#) to:
  - 0: Only the lower bits of the received data within the storage data width is stored to memory;
  - 1: Only the higher bits of the received data within the storage data width is stored to memory.
- If the received data width is smaller than the storage data width in each channel, the higher bits of the received data will be filled with zeros and then the data is saved to memory.

#### 42.8.2.4 Endian Control of Channel Storage Data

The received data is then converted into storage data (to be stored to memory) after some processing, such as discarding extra bits or filling zeros in missing bits. The endian of the storage data is controlled by [LP\\_I2S\\_RX\\_BIG\\_ENDIAN](#) (the data bit width is fixed as 16). See the table below.

Table 42.8-2. Channel Storage Data Endian

| Original Data | Endian of Processed Data | <a href="#">LP_I2S_RX_BIG_ENDIAN</a> |
|---------------|--------------------------|--------------------------------------|
| {B1, B0}      | {B1, B0}                 | 0                                    |
|               | {B0, B1}                 | 1                                    |

At this point, the data format control is completed. Data then is stored into memory.

### 42.8.3 Internal Memory

All data after format control is stored in the LP I2S internal memory, which is a 16-bit wide circular buffer that supports RX unit write operations and system read operations. The LP I2S internal memory includes a pair of hardware-maintained read and write pointers to manage write and read operations.

1. When LP I2S writes data:

- If the memory is full: Overwrites the oldest data and increments the write and read pointers by 1 (the value of the read pointer is the value of the write pointer plus one at this point).
- If the memory is not full: Writes the data and increments the write pointer by 1. The read pointer remains unchanged.

2. When the system reads from the LP I2S memory:

- If the memory is empty: The read and write pointers remain unchanged (the value of the read pointer equals to the value of the write pointer at this point).
- If the memory is not empty: Increments the read pointer by 1. The write pointer remains unchanged.

**Note:**

- The incremental operation for the read and write pointers is in a circular manner, i.e., when the value of the read or write pointer reaches the boundary of the memory, the incremental operation resets the value of the pointer to zero.
- Within the LP I2S internal memory architecture, the system always reads the oldest data in the memory.

## 42.9 Interrupts

ESP32-P4's LP I2S can generate the LP\_I2S\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#). There are several internal interrupt sources from LP I2S that can generate the above interrupt signals as follows:

- LP\_I2S\_RX\_HUNG\_INT: Triggered when the data reception is timed out. For example, if the LP I2S module is configured as RX slave mode, but the master does not transmit data for a long time (specified in [LP\\_I2S\\_LC\\_HUNG\\_CONF\\_REG](#)), this interrupt will be triggered.
- LP\_I2S\_RX\_DONE\_INT: Triggered when the data reception is completed.
- LP\_I2S\_RX\_FIFOMEM\_UDF\_INT: Triggered when the LP I2S memory is read empty.
- LP\_I2S\_RX\_MEM\_THRESHOLD\_INT: Triggered when the data in LP I2S memory is larger than the value configured in [LP\\_I2S\\_RX\\_MEM\\_THRESHOLD](#).

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [42.10 Register Summary](#).

## 42.10 Register Summary

The addresses in this section are relative to LP I2S base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

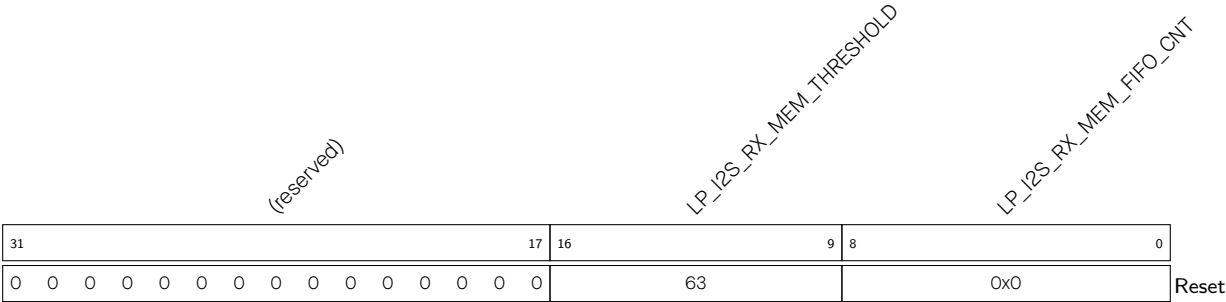
| Name  | Description                               | Address | Access    |
|---|---|---------|-----------|
| <b>RX control and configuration registers</b> |   |         |           |
| <a href="#">LP_I2S_RX_MEM_CONF_REG</a>        | LP I2S memory configuration register      | 0x0008  | varies    |
| <a href="#">LP_I2S_RX_CONF_REG</a>            | LP I2S RX configuration register          | 0x0020  | varies    |
| <a href="#">LP_I2S_RX_CONF1_REG</a>           | LP I2S RX configuration register 1        | 0x0028  | R/W       |
| <a href="#">LP_I2S_RX_TDM_CTRL_REG</a>        | LP I2S RX TDM mode configuration register | 0x0050  | R/W       |
| <a href="#">LP_I2S_RXEOF_NUM_REG</a>          | LP I2S RX data number control register    | 0x0064  | R/W       |
| <a href="#">LP_I2S_RX_PDM_CONF_REG</a>        | LP I2S RX PDM mode configuration register | 0x0070  | R/W       |
| <b>Interrupt registers</b>                    |   |         |           |
| <a href="#">LP_I2S_INT_RAW_REG</a>            | LP I2S interrupt raw register             | 0x000C  | RO/WTC/SS |
| <a href="#">LP_I2S_INT_ST_REG</a>             | LP I2S interrupt status register          | 0x0010  | RO        |
| <a href="#">LP_I2S_INT_ENA_REG</a>            | LP I2S interrupt enable register          | 0x0014  | R/W       |
| <a href="#">LP_I2S_INT_CLR_REG</a>            | LP I2S interrupt clear register           | 0x0018  | WT        |
| <b>RX clock and timing register</b>           |   |         |           |
| <a href="#">LP_I2S_RX_TIMING_REG</a>          | LP I2S RX timing control register         | 0x0058  | R/W       |
| <b>Control and configuration registers</b>    |   |         |           |
| <a href="#">LP_I2S_LC_HUNG_CONF_REG</a>       | LP I2S timeout configuration register     | 0x0060  | R/W       |
| <a href="#">LP_I2S_CONF_SIGLE_DATA_REG</a>    | LP I2S single data register               | 0x0068  | R/W       |
| <b>Clock register</b>                         |   |         |           |
| <a href="#">LP_I2S_CLK_GATE_REG</a>           | Clock gate register                       | 0x00F8  | R/W       |
| <b>Version register</b>                       |   |         |           |
| <a href="#">LP_I2S_DATE_REG</a>               | Version control register                  | 0x00FC  | R/W       |

## 42.11 Registers

The addresses in this section are relative to LP I2S base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

Register 42.1. LP\_I2S\_RX\_MEM\_CONF\_REG (0x0008)



- LP\_I2S\_RX\_MEM\_FIFO\_CNT Configures the number of data in the RX memory. (RO)
- LP\_I2S\_RX\_MEM\_THRESHOLD Configures the RX memory threshold. LP I2S RX memory triggers an interrupt when the data in the memory exceeds (not including equals) this threshold. (R/W)

## Register 42.2. LP\_I2S\_RX\_CONF\_REG (0x0020)

|            |  |  |  |  |  |  |  |  |  |  |  |                  |  |  |  |                  |  |  |  |                     |  |  |  |            |    |    |    |                       |    |    |    |            |   |    |   |                        |   |   |   |                  |   |   |   |            |       |   |   |                      |   |   |   |                |  |  |  |                         |  |  |  |                     |  |  |  |                 |  |  |  |                      |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|------------------|--|--|--|------------------|--|--|--|---------------------|--|--|--|------------|----|----|----|-----------------------|----|----|----|------------|---|----|---|------------------------|---|---|---|------------------|---|---|---|------------|-------|---|---|----------------------|---|---|---|----------------|--|--|--|-------------------------|--|--|--|---------------------|--|--|--|-----------------|--|--|--|----------------------|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  | LP_I2S_RX_PDM_EN |  |  |  | LP_I2S_RX_TDM_EN |  |  |  | LP_I2S_RX_BIT_ORDER |  |  |  | (reserved) |    |    |    | LP_I2S_RX_WS_IDLE_POL |    |    |    | (reserved) |   |    |   | LP_I2S_RX_MONO_FST_VLD |   |   |   | LP_I2S_RX_UPDATE |   |   |   | (reserved) |       |   |   | LP_I2S_RX_BIG_ENDIAN |   |   |   | LP_I2S_RX_MONO |  |  |  | LP_I2S_RX_FIFOMEM_RESET |  |  |  | LP_I2S_RX_SLAVE_MOD |  |  |  | LP_I2S_RX_START |  |  |  | LP_I2S_RX_FIFO_RESET |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  | 21               |  |  |  |                  |  |  |  |                     |  |  |  | 20         | 19 | 18 | 17 | 16                    | 15 | 14 | 13 | 12         |   | 10 | 9 | 8                      | 7 | 6 | 5 | 4                | 3 | 2 | 1 | 0          | Reset |   |   |                      |   |   |   |                |  |  |  |                         |  |  |  |                     |  |  |  |                 |  |  |  |                      |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  | 0                |  |  |  |                  |  |  |  |                     |  |  |  | 0          | 0  | 0  | 0  | 0                     | 1  | 0  | 1  |            | 0 | 1  | 1 | 0                      | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0          | 0     | 0 | 0 | 0                    | 0 | 0 | 0 |                |  |  |  |                         |  |  |  |                     |  |  |  |                 |  |  |  |                      |  |  |  |

Reset

**LP\_I2S\_RX\_RESET** Configures whether to reset RX.

0: No effect

1: Reset

(WT)

**LP\_I2S\_RX\_FIFO\_RESET** Configures whether to reset RX FIFO.

0: No effect

1: Reset

(WT)

**LP\_I2S\_RX\_START** Configures whether to start receiving data.

0: No effect

1: Start

(R/W)

Continued on the next page...

**Register 42.2. LP\_I2S\_RX\_CONF\_REG (0x0020)**

Continued from the previous page...

**LP\_I2S\_RX\_SLAVE\_MOD** Configures whether to enable slave RX mode.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_RX\_FIFOMEM\_RESET** Configures whether to reset RX Sync FIFO memory.

0: No effect

1: Reset

(WT)

**LP\_I2S\_RX\_MONO** Configures whether to enable RX unit in mono mode.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_RX\_BIG\_ENDIAN** Configures LP I2S RX byte endian.

0: Low address data is saved to low address

1: Low address data is saved to high address

(R/W)

**LP\_I2S\_RX\_UPDATE** Configures whether to update LP I2S RX registers from APB clock domain to LP I2S RX clock domain. This bit will be cleared by hardware after the register update is done.

0: No effect

1: Update

(R/W/SC)

**LP\_I2S\_RX\_MONO\_FST\_VLD** Configures which channel data value is valid in LP I2S RX mono mode.

0: The second channel data value is valid

1: The first channel data value is valid

(R/W)

**LP\_I2S\_RX\_STOP\_MODE** Configures when LP I2S RX stops data reception.

0: Only stops when [LP\\_I2S\\_RX\\_START](#) is cleared

1: Stops when [LP\\_I2S\\_RX\\_START](#) is cleared or the number of received bytes is greater than the value configured in [LP\\_I2S\\_RX\\_EOF\\_NUM\\_REG](#)

Other values: Invalid

(R/W)

**LP\_I2S\_RX\_LEFT\_ALIGN** Configures the RX alignment mode

0: Right alignment

1: Left alignment

(R/W)

Continued on the next page...



**Register 42.2. LP\_I2S\_RX\_CONF\_REG (0x0020)**

Continued from the previous page...

**LP\_I2S\_RX\_WS\_IDLE\_POL** Configures the relationship between WS level and which channel data to receive.

0: WS remains low when receiving left channel data and high when receiving right channel data

1: WS remains high when receiving left channel data and low when receiving right channel data

(R/W)

**LP\_I2S\_RX\_BIT\_ORDER** Configures whether to reverse the bit order of the LP I2S RX data to be received.

0: Not reverse

1: Reverse

(R/W)

**LP\_I2S\_RX\_TDM\_EN** Configures whether to enable LP I2S TDM RX mode.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_RX\_PDM\_EN** Configures whether to enable LP I2S PDM RX mode.

0: Disable

1: Enable

(R/W)

Register 42.3. LP\_I2S\_RX\_CONF1\_REG (0x0028)

|            |    |                     |    |                         |    |                            |    |                    |    |                       |   |                        |       |
|------------|----|---------------------|----|-------------------------|----|----------------------------|----|--------------------|----|-----------------------|---|------------------------|-------|
| (reserved) |    | LP_I2S_RX_MSB_SHIFT |    | LP_I2S_RX_TDM_CHAN_BITS |    | LP_I2S_RX_HALF_SAMPLE_BITS |    | LP_I2S_RX_BITS_MOD |    | LP_I2S_RX_BCK_DIV_NUM |   | LP_I2S_RX_TDM_WS_WIDTH |       |
| 31         | 30 | 29                  | 28 | 24                      | 23 | 18                         | 17 | 13                 | 12 | 7                     | 6 |                        | 0     |
| 0          | 0  | 1                   |    | 0xf                     |    | 0xf                        |    | 0xf                |    | 6                     |   | 0x0                    | Reset |

**LP\_I2S\_RX\_TDM\_WS\_WIDTH** Configures the width of LP\_I2SI\_WS\_out (WS default level) at idle level in TDM mode. Width of LP\_I2SI\_WS\_out at idle level in TDM mode = (LP\_I2S\_RX\_TDM\_WS\_WIDTH[6:0] + 1) x T\_BCK. (R/W)

**LP\_I2S\_RX\_BCK\_DIV\_NUM** Configures the divider of BCK in RX mode. Note this divider must not be configured to 1. (R/W)

**LP\_I2S\_RX\_BITS\_MOD** Configures the valid data bit length of LP I2S RX channel. Since the LP I2S only supports 16-bit mode, this field must be configured to 15. LP I2S cannot function properly if this field is configured to any other value. (R/W)

**LP\_I2S\_RX\_HALF\_SAMPLE\_BITS** Configures LP I2S RX sample bits. BCK cycles in one WS period = I2S\_RX\_HALF\_SAMPLE\_BITS x 2. (R/W)

**LP\_I2S\_RX\_TDM\_CHAN\_BITS** Configures RX bit number for each channel in TDM mode. Bit number expected = LP\_I2S\_RX\_TDM\_CHAN\_BITS + 1. (R/W)

**LP\_I2S\_RX\_MSB\_SHIFT** Configures the timing between the WS signal and the MSB of data.

0: Align at the rising edge

1: The WS signal changes one BCK clock earlier

(R/W)

#### Register 42.4. LP\_I2S\_RX\_TDM\_CTRL\_REG (0x0050)

Diagram illustrating the structure of the LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM register (32 bits total):

- Bits 31 to 16: (reserved)
- Bits 15 to 0: LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM
  - Bits 15 to 1: LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM
  - Bit 0: LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM

Reset values: 0x0 for bits 15 to 1, and 1 for bit 0.

**LP\_I2S\_RX\_TDM\_PDM\_CHAN0\_EN** Configures whether to enable the valid data input of LP I2S RX TDM or PDM channel 0.

0: Disable. Channel 0 only inputs 0

1: Enable

(R/W)

**LP\_I2S\_RX\_TDM\_PDM\_CHAN1\_EN** Configures whether to enable the valid data input of LP I2S RX TDM or PDM channel 1.

0: Disable. Channel 1 only inputs 0

1: Enable

(R/W)

**LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM** Configures the total channel number of LP I2S RX TDM mode.

Total channel number in use = LP\_I2S\_RX\_TDM\_TOT\_CHAN\_NUM + 1. (R/W)

### Register 42.5. LP\_I2S\_RXEOF\_NUM\_REG (0x0064)

|   |  |                   |   |
|---|--|-------------------|---|
| 31  |  | 11                | 0 |
| (reserved)                                  |  | LP_I2S_RX_EOF_NUM |   |
| 0 |  | 0x40              |   |
| Reset                                       |  |                   |   |

**LP\_I2S\_RX\_EOF\_NUM** Configures the bit length of RX data. Bit length of RX data = (LP\_I2S\_RX\_BITS\_MOD[4:0] + 1) x (LP\_I2S\_RX\_EOF\_NUM[11:0] + 1). Valid when **LP\_I2S\_RX\_STOP\_MODE** is set to 1. (R/W)

Register 42.6. LP\_I2S\_RX\_PDM\_CONF\_REG (0x0070)

|            |    |    |    |            |    |                         |    |                               |    |                              |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|----|----|------------|----|-------------------------|----|-------------------------------|----|------------------------------|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |    |    | (reserved) |    | LP_I2S_RX_PDM_HP_BYPASS |    | LP_I2S_RX_PDM2PCM_AMPLIFY_NUM |    | LP_I2S_RX_PDM_SINC_DSR_16_EN |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 29 | 28 | 26 | 25         | 24 | 21                      | 20 | 19                            | 18 |                              |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0x7        |    |    |    | 0x6        |    | 0                       |    | 0x1                           |    | 0                            | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LP\_I2S\_RX\_PDM2PCM\_EN** Configures whether to enable the PDM-to-PCM converter in RX mode.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_RX\_PDM\_SINC\_DSR\_16\_EN** Configures the downsampling rate of PDM RX filter group 1 module.

0: 64

1: 128

(R/W)

**LP\_I2S\_RX\_PDM2PCM\_AMPLIFY\_NUM** Configures the PDM-to-PCM RX amplification coefficient.

PCM data will be multiplied by this value before outputting. (R/W)

**LP\_I2S\_RX\_PDM\_HP\_BYPASS** Configures whether PDM-to-PCM RX bypasses the HP filter.

0: Not bypass

1: Bypass

(R/W)

### Register 42.7. LP\_I2S\_INT\_RAW\_REG (0x000C)

[illegible]

**LP\_I2S\_RX\_DONE\_INT\_RAW** The raw interrupt status of the **LP\_I2S\_RX\_DONE\_INT** interrupt.  
(R/SS/WTC)

**LP\_I2S\_RX\_HUNG\_INT\_RAW** The raw interrupt status of the **LP\_I2S\_RX\_DONE\_INT** interrupt.  
(R/SS/WTC)

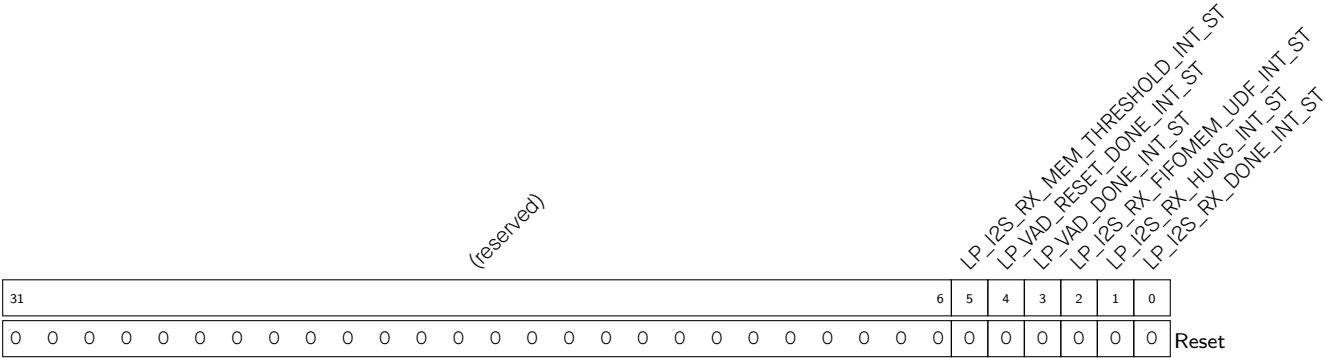
LP\_I2S\_RX\_FIFOMEM\_UDF\_INT\_RAW The raw interrupt status of the LP\_I2S\_RX\_FIFOMEM\_UDF\_INT interrupt. (R/SS/WTC)

**LP\_I2S\_VAD\_DONE\_INT\_RAW** The raw interrupt status of the [LP\\_I2S\\_VAD\\_DONE\\_INT](#) interrupt.  
(R/SS/WTC)

LP\_I2S\_VAD\_RESET\_DONE\_INT\_RAW The raw interrupt status of the LP\_I2S\_VAD\_RESET\_DONE\_INT interrupt. (R/SS/WTC)

**LP\_I2S\_RX\_MEM\_THRESHOLD\_INT\_RAW** The raw interrupt status of the [LP\\_I2S\\_RX\\_MEM\\_THRESHOLD\\_INT](#) interrupt. (R/SS/WTC)

Register 42.8. LP\_I2S\_INT\_ST\_REG (0x0010)



- LP\_I2S\_RX\_DONE\_INT\_ST

The masked interrupt status of the [LP\\_I2S\\_RX\\_DONE\\_INT](#) interrupt. (RO)
- LP\_I2S\_RX\_HUNG\_INT\_ST

The masked interrupt status of the [LP\\_I2S\\_RX\\_DONE\\_INT](#) interrupt. (RO)
- LP\_I2S\_RX\_FIFOMEM\_UDF\_INT\_ST

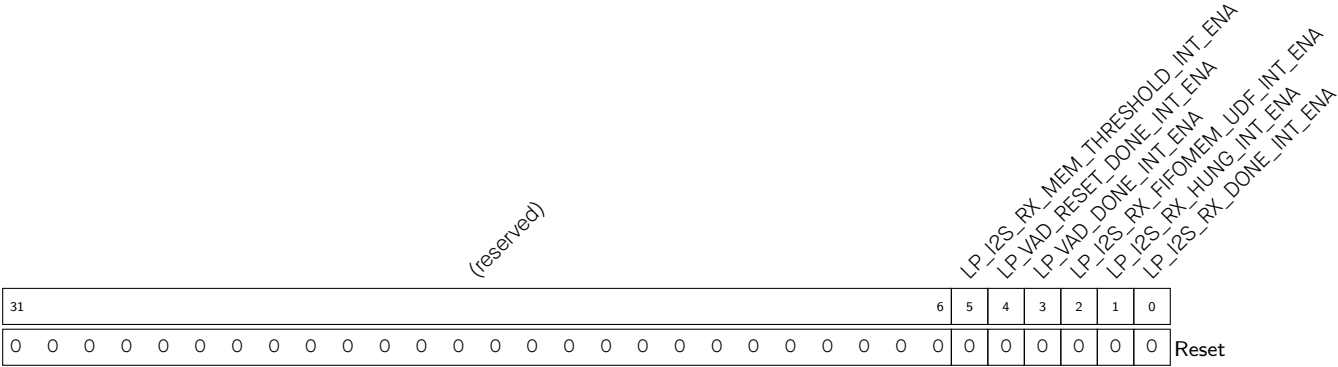
The masked interrupt status of the [LP\\_I2S\\_RX\\_FIFOMEM\\_UDF\\_INT](#) interrupt. (RO)
- LP\_I2S\_VAD\_DONE\_INT\_ST

The masked interrupt status of the [LP\\_I2S\\_VAD\\_DONE\\_INT](#) interrupt. (RO)
- LP\_I2S\_VAD\_RESET\_DONE\_INT\_ST

The masked interrupt status of the [LP\\_I2S\\_VAD\\_RESET\\_DONE\\_INT](#) interrupt. (RO)
- LP\_I2S\_RX\_MEM\_THRESHOLD\_INT\_ST

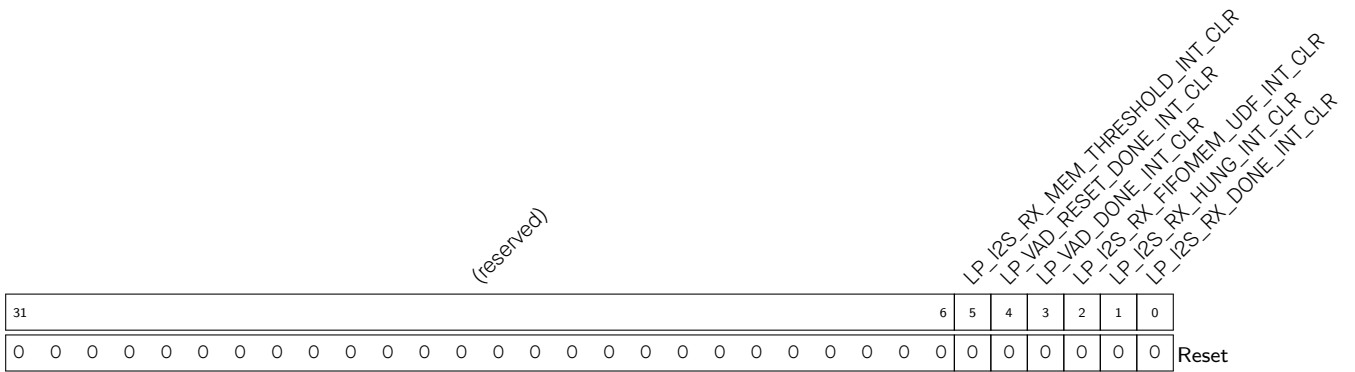
The masked interrupt status of the [LP\\_I2S\\_RX\\_MEM\\_THRESHOLD\\_INT](#) interrupt. (RO)

Register 42.9. LP\_I2S\_INT\_ENA\_REG (0x0014)



- LP\_I2S\_RX\_DONE\_INT\_ENA Write 1 to enable the LP\_I2S\_RX\_DONE\_INT interrupt. (R/W)
- LP\_I2S\_RX\_HUNG\_INT\_ENA Write 1 to enable the LP\_I2S\_RX\_DONE\_INT interrupt. (R/W)
- LP\_I2S\_RX\_FIFOEM\_UDF\_INT\_ENA Write 1 to enable the LP\_I2S\_RX\_FIFOEM\_UDF\_INT interrupt. (R/W)
- LP\_I2S\_VAD\_DONE\_INT\_ENA Write 1 to enable the LP\_I2S\_VAD\_DONE\_INT interrupt. (R/W)
- LP\_I2S\_VAD\_RESET\_DONE\_INT\_ENA Write 1 to enable the LP\_I2S\_VAD\_RESET\_DONE\_INT interrupt. (R/W)
- LP\_I2S\_RX\_MEM\_THRESHOLD\_INT\_ENA Write 1 to enable the LP\_I2S\_RX\_MEM\_THRESHOLD\_INT interrupt. (R/W)

### Register 42.10. LP\_I2S\_INT\_CLR\_REG (0x0018)



**LP\_I2S\_RX\_DONE\_INT\_CLR** Write 1 to clear the **LP\_I2S\_RX\_DONE\_INT** interrupt. (WT)

**LP\_I2S\_RX\_HUNG\_INT\_CLR** Write 1 to clear the **LP\_I2S\_RX\_DONE\_INT** interrupt. (WT)

LP\_I2S\_RX\_FIFOMEM\_UDF\_INT\_CLR Write 1 to clear the LP\_I2S\_RX\_FIFOMEM\_UDF\_INT interrupt.  
(WT)

**LP\_VAD\_DONE\_INT\_CLR** Write 1 to clear the **LP\_I2S\_VAD\_DONE\_INT** interrupt. (WT)

**LP\_VAD\_RESET\_DONE\_INT\_CLR** Write 1 to clear the [LP\\_I2S\\_VAD\\_RESET\\_DONE\\_INT](#) interrupt. (WT)

**LP\_I2S\_RX\_MEM\_THRESHOLD\_INT\_CLR** Write 1 to clear the [LP\\_I2S\\_RX\\_MEM\\_THRESHOLD\\_INT](#) interrupt. (WT)



**Register 42.11. LP\_I2S\_RX\_TIMING\_REG (0x0058)**

|            |    |                     |    |            |    |                    |    |            |    |                      |    |            |    |                     |    |            |   |   |   |   |   |   |   |   |   |                    |   |   |   |   |     |       |
|------------|----|---------------------|----|------------|----|--------------------|----|------------|----|----------------------|----|------------|----|---------------------|----|------------|---|---|---|---|---|---|---|---|---|--------------------|---|---|---|---|-----|-------|
| (reserved) |    | LP_I2S_RX_BCK_IN_DM |    | (reserved) |    | LP_I2S_RX_WS_IN_DM |    | (reserved) |    | LP_I2S_RX_BCK_OUT_DM |    | (reserved) |    | LP_I2S_RX_WS_OUT_DM |    | (reserved) |   |   |   |   |   |   |   |   |   | LP_I2S_RX_SD_IN_DM |   |   |   |   |     |       |
| 31         | 30 | 29                  | 28 | 27         | 26 | 25                 | 24 | 23         | 22 | 21                   | 20 | 19         | 18 | 17                  | 16 | 15         |   |   |   |   |   |   |   |   |   | 2                  | 1 | 0 |   |   |     |       |
| 0          | 0  | 0x0                 |    | 0          | 0  | 0x0                |    | 0          | 0  | 0x0                  |    | 0          | 0  | 0x0                 |    | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                  | 0 | 0 | 0 | 0 | 0x0 | Reset |

Reset

**LP\_I2S\_RX\_SD\_IN\_DM** Configures the delay mode of LP I2S RX SD input signal.

0: Bypass

1: Delay by positive edge

2: Delay by negative edge

3: Invalid

(R/W)

**LP\_I2S\_RX\_WS\_OUT\_DM** Configures the delay mode of LP I2S RX WS output signal. For detailed configuration values, please refer to [LP\\_I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**LP\_I2S\_RX\_BCK\_OUT\_DM** Configures the delay mode of LP I2S RX BCK output signal. For detailed configuration values, please refer to [LP\\_I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**LP\_I2S\_RX\_WS\_IN\_DM** Configures the delay mode of LP I2S RX WS input signal. For detailed configuration values, please refer to [LP\\_I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

**LP\_I2S\_RX\_BCK\_IN\_DM** Configures the delay mode of LP I2S RX BCK input signal. For detailed configuration values, please refer to [LP\\_I2S\\_RX\\_SD\\_IN\\_DM](#). (R/W)

Register 42.12. LP\_I2S\_LC\_HUNG\_CONF\_REG (0x0060)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                            |      |                              |       |                        |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----------------------------|------|------------------------------|-------|------------------------|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | LP_I2S_LC_FIFO_TIMEOUT_ENA |      | LP_I2S_LC_FIFO_TIMEOUT_SHIFT |       | LP_I2S_LC_FIFO_TIMEOUT |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 12 | 11                         | 10   | 8                            | 7     |                        |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1  | 0                          | 0x10 |                              | Reset |                        |  |   |

Reset

**LP\_I2S\_LC\_FIFO\_TIMEOUT** Configures FIFO timeout threshold. The FIFO hung counter is incremented by one each time LP I2S is in an error state and the tick counter reaches its threshold. [LP\\_I2S\\_RX\\_HUNG\\_INT](#) interrupt will be triggered when FIFO hung counter is equal to the FIFO timeout threshold. (R/W)

**LP\_I2S\_LC\_FIFO\_TIMEOUT\_SHIFT** Configures tick counter threshold. The tick counter is incremented by one each time LP I2S is in an error state and it is on the rising edge in each system clock (APB). The tick counter is reset when counter value  $\geq 88000/2^{LP\_I2S\_LC\_FIFO\_TIMEOUT\_SHIFT}$ . (R/W)

**LP\_I2S\_LC\_FIFO\_TIMEOUT\_ENA** The enable bit for FIFO timeout. Configures whether to enable FIFO timeout.  
 0: Disable  
 1: Enable  
 (R/W)

Register 42.13. LP\_I2S\_CONF\_SIGLE\_DATA\_REG (0x0068)

|                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|--------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| LP_I2S_SINGLE_DATA |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

Reset

Reset

**LP\_I2S\_SINGLE\_DATA** Configures the constant channel data to be sent out. (R/W)

#### Register 42.14. LP\_I2S\_CLK\_GATE\_REG (0x00F8)

Diagram of the LP\_I2S\_RX\_LP\_I2S\_CG\_FORCE\_ON register (32 bits):

- Bits 31-1: (reserved)
- Bit 0: Reset

**LP\_I2S\_CLK\_EN** Configures whether to enable clock gate.

0: Disable

1: Enable

(R/W)

**LP\_I2S\_VAD\_CG\_FORCE\_ON** Configures whether to force the VAD clock gate on.

0: No effect

1: Force on

(R/W)

**LP\_I2S\_RX\_MEM\_CG\_FORCE\_ON** Configures whether to force the LP I2S RX memory clock gate on.

0: No effect

1: Force on

(R/W)

**LP\_I2S\_RX\_LP\_I2S\_CG\_FORCE\_ON** Configures whether to force the LP I2S RX register clock gate on.

0: No effect

1: Force on

(R/W)

### Register 42.15. LP\_I2S\_DATE\_REG (0x00FC)

|    |    |    |           |
|----|----|----|-----------|
| 31 | 28 | 27 | 0         |
| 0  | 0  | 0  | 0         |
|    |    |    | 0x2305040 |
|    |    |    | Reset     |

**LP\_I2S\_DATE** Version control register. (R/W)

## Chapter 43

### Pulse Count Controller (PCNT)

The pulse count controller (PCNT) is designed to count input pulses.

#### 43.1 Introduction

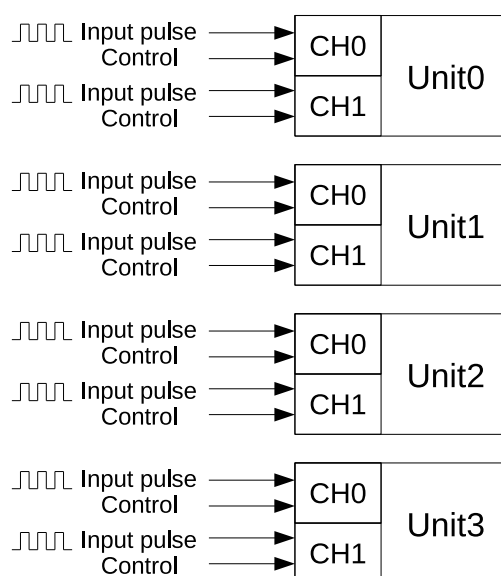


Figure 43.1-1. PCNT Overview

As shown in Figure 43.1-1, PCNT has four independent pulse counters called units, which have their groups of registers. Each unit includes two channels (ch0 and ch1) and a 16-bit signed counter. Each channel has an input pulse signal and an input signal filtering module. The 16-bit signed counter can be configured for incremental or decremental counting. The clock for PCNT module is APB\_CLK.

#### 43.2 Feature List

A PCNT has the following features:

- Four independent pulse counters (units) that count from 1 to 65535
- Each unit consists of two independent channels sharing one pulse counter
- All channels have input pulse signals (e.g., sig\_ch0\_un) with their corresponding control signals (e.g., ctrl\_ch0\_un)
- Independently filter glitches of input pulse signals (sig\_ch0\_un and sig\_ch1\_un) and control signals (ctrl\_ch0\_un and ctrl\_ch1\_un) on each unit

- Each channel has the following parameters:
  - Selection between counting on rising or falling edges of the input pulse signal
  - Configuration to Increment, Decrement, or Disable counter mode for control signal's high and low states
- Maximum frequency of pulses:  $\frac{f_{APB\_CLK}}{2}$

### 43.3 Architectural Overview

Each unit of PCNT includes two channels (ch0 and ch1) and the functionality of the two channels is identical. The remainder of the chapter will take channel 0 (ch0) as example and  $n$  denotes the number of a unit from 0 ~ 3. Each channel of PCNT has two input signals:

- One input pulse signal (e.g., sig\_ch0\_un, the input pulse signal for ch0 of unit  $n$  ch0)
- One control signal (e.g., ctrl\_ch0\_un, the control signal for ch0 of unit  $n$  ch0)

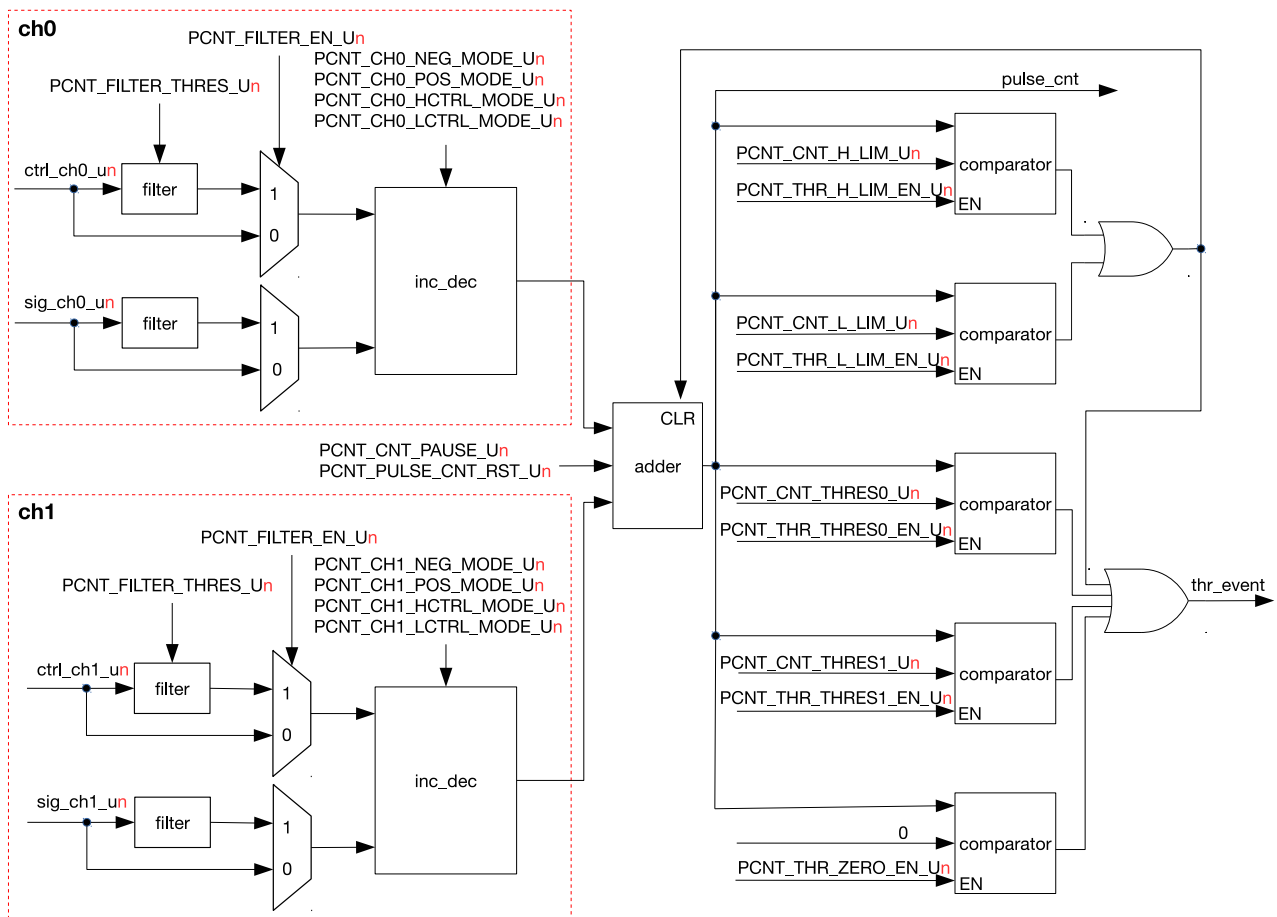


Figure 43.3-1. PCNT Architectural Overview

Figure 43.3-1 shows PCNT's architecture. As stated above, ctrl\_ch0\_un is the control signal for ch0 of unit  $n$ . Its high and low states can be assigned in different counter modes and used for pulse counting of the channel's input pulse signal sig\_ch0\_un on falling or rising edges.

## 43.4 Functional Description

The available counter modes of PCNT are as follows:

- Increment mode: When a channel detects an active edge of sig\_ch0\_un (can be configured by software), the counter value pulse\_cnt increases by 1. Upon reaching PCNT\_CNT\_H\_LIM\_Un, pulse\_cnt is cleared. If PCNT\_CNT\_PAUSE\_Un is set to 1, then pulse\_cnt freezes.
- Decrement mode: When a channel detects an active edge of sig\_ch0\_un (can be configured by software), the counter value pulse\_cnt decreases by 1. Upon reaching PCNT\_CNT\_L\_LIM\_Un, pulse\_cnt is cleared. If PCNT\_CNT\_PAUSE\_Un is set to 1, then pulse\_cnt freezes.
- Disable mode: Counting is disabled, and the counter value pulse\_cnt freezes.

Table 43.4-1 to Table 43.4-4 provide information on how to configure the counter mode for channel 0.

**Table 43.4-1. Counter Mode. Rising edge of Input Pulse Signal. Control Signal in Low State**

| PCNT_CHO_POS_MODE_Un | PCNT_CHO_LCTRL_MODE_Un | Counter Mode |
|----------------------|------------------------|--------------|
| 1                    | 0                      | Increment    |
|                      | 1                      | Decrement    |
|                      | Others                 | Disable      |
| 2                    | 0                      | Decrement    |
|                      | 1                      | Increment    |
|                      | Others                 | Disable      |
| Others               | N/A                    | Disable      |

**Table 43.4-2. Counter Mode. Rising edge of Input Pulse Signal. Control Signal in High State**

| PCNT_CHO_POS_MODE_Un | PCNT_CHO_HCTRL_MODE_Un | Counter Mode |
|----------------------|------------------------|--------------|
| 1                    | 0                      | Increment    |
|                      | 1                      | Decrement    |
|                      | Others                 | Disable      |
| 2                    | 0                      | Decrement    |
|                      | 1                      | Increment    |
|                      | Others                 | Disable      |
| Others               | N/A                    | Disable      |

**Table 43.4-3. Counter Mode. Falling Edge of Input Pulse Signal. Control Signal in Low State**

| PCNT_CHO_NEG_MODE_Un | PCNT_CHO_LCTRL_MODE_Un | Counter Mode |
|----------------------|------------------------|--------------|
| 1                    | 0                      | Increment    |
|                      | 1                      | Decrement    |
|                      | Others                 | Disable      |
| 2                    | 0                      | Decrement    |
|                      | 1                      | Increment    |
|                      | Others                 | Disable      |
| Others               | N/A                    | Disable      |

**Table 43.4-4. Counter Mode. Falling Edge of Input Pulse Signal. Control Signal in High State**

| <a href="#">PCNT_CHO_NEG_MODE_Un</a> | <a href="#">PCNT_CHO_HCTRL_MODE_Un</a> | Counter Mode |
|--------------------------------------|--|--------------|
| 1                                    | 0                                      | Increment    |
|                                      | 1                                      | Decrement    |
|                                      | Others                                 | Disable      |
| 2                                    | 0                                      | Decrement    |
|                                      | 1                                      | Increment    |
|                                      | Others                                 | Disable      |
| Others                               | N/A                                    | Disable      |

Each unit has one filter for all its control and input pulse signals. A filter can be enabled by setting the bit [PCNT\\_FILTER\\_EN\\_Un](#). The filter monitors the signals and ignores all the noise, i.e., the glitches with pulse widths shorter than [PCNT\\_FILTER\\_THRES\\_Un](#) APB clock cycles in length.

As shown on Figure 43.3-1, each unit has two channels which process different input pulse signals and increase or decrease values via their respective inc\_dec modules, then the two channels send these values to the counter module which has a 16-bit wide signed register. This counter can be suspended by setting [PCNT\\_CNT\\_PAUSE\\_Un](#), and cleared by setting [PCNT\\_PULSE\\_CNT\\_RST\\_Un](#).

The PCNT has five watchpoints that share one interrupt. The interrupt can be enabled or disabled by interrupt enable signals of each individual watchpoint.

- Maximum count value: When pulse\_cnt reaches [PCNT\\_CNT\\_H\\_LIM\\_Un](#), a high limit interrupt is triggered and [PCNT\\_CNT\\_THR\\_H\\_LIM\\_LAT\\_Un](#) is high.
- Minimum count value: When pulse\_cnt reaches [PCNT\\_CNT\\_L\\_LIM\\_Un](#), a low limit interrupt is triggered and [PCNT\\_CNT\\_THR\\_L\\_LIM\\_LAT\\_Un](#) is high.
- Two threshold values: When pulse\_cnt equals either [PCNT\\_CNT\\_THRES0\\_Un](#) or [PCNT\\_CNT\\_THRES1\\_Un](#), an interrupt is triggered and either [PCNT\\_CNT\\_THR\\_THRES0\\_LAT\\_Un](#) or [PCNT\\_CNT\\_THR\\_THRES1\\_LAT\\_Un](#) is high respectively.
- Zero: When pulse\_cnt is 0, an interrupt is triggered and [PCNT\\_CNT\\_THR\\_ZERO\\_LAT\\_Un](#) is valid.

If [PCNT\\_CNT\\_H\\_LIM\\_Un](#) and/or [PCNT\\_CNT\\_L\\_LIM\\_Un](#) are reconfigured by software when PCNT is working, the new configuration will take effect after pulse\_cnt counts to any of the above five watchpoints; If [PCNT\\_CNT\\_THRES0\\_Un](#) and/or [PCNT\\_CNT\\_THRES1\\_Un](#) are reconfigured by software, the new configuration will take effect immediately.

## 43.5 Interrupts

ESP32-P4's PCNT can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- [PCNT\\_INT](#)

There are several internal interrupt sources from PCNT that can generate the above interrupt signal. The interrupt sources from PCNT are listed with their trigger conditions and the resulted interrupt signal in Table 43.5-1.

Table 43.5-1. PCNT's Internal Interrupt Sources

| Internal Interrupt Source | Trigger Condition                      | Interrupt Signal |
|---------------------------|--|------------------|
| PCNT_CNT_THR_EVENT_U0_INT | reaching the watchpoint in PCNT unit 0 | PCNT_INT         |
| PCNT_CNT_THR_EVENT_U1_INT | reaching the watchpoint in PCNT unit 1 | PCNT_INT         |
| PCNT_CNT_THR_EVENT_U2_INT | reaching the watchpoint in PCNT unit 2 | PCNT_INT         |
| PCNT_CNT_THR_EVENT_U3_INT | reaching the watchpoint in PCNT unit 3 | PCNT_INT         |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 *Interrupt Matrix* > Section 11.2 *Interrupt Terminology in ESP32-P4*.

## 43.6 Programming Procedures

In each unit, channel 0 and channel 1 can be configured to work independently or together. The three subsections below provide details of channel 0 incrementing independently, channel 0 decrementing independently, and channel 0 and channel 1 incrementing together. For other working modes not elaborated in this section (e.g., channel 1 incrementing/decrementing independently, or one channel incrementing while the other decrementing), reference can be made to these three subsections.

### 43.6.1 Channel 0 Incrementing Independently

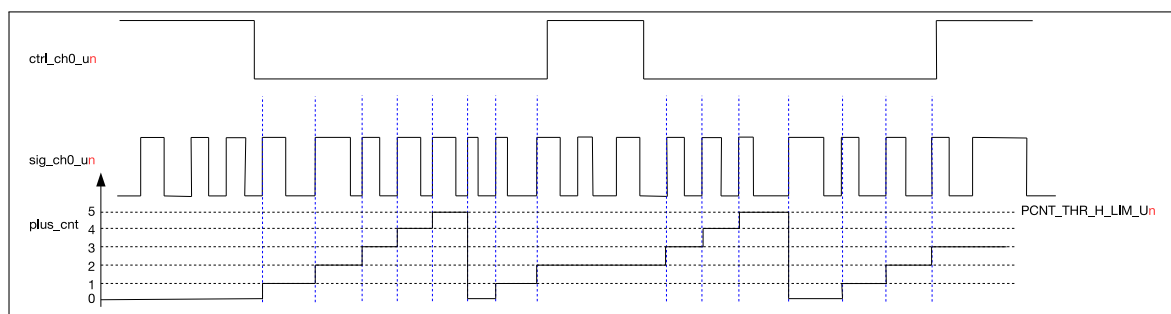


Figure 43.6-1. Channel 0 Up Counting Diagram

Figure 43.6-1 illustrates how channel 0 is configured to increment independently on the rising edge of sig\_ch0\_un while channel 1 is disabled (see Subsection 43.4 for how to disable channel 1). The configuration of channel 0 is shown below.

- **PCNT\_CHO\_LCTRL\_MODE\_Un=0**: When ctrl\_ch0\_un is low, the counter mode specified for the low state turns on, in this case it is Increment mode.
- **PCNT\_CHO\_HCTRL\_MODE\_Un=2**: When ctrl\_ch0\_un is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
- **PCNT\_CHO\_POS\_MODE\_Un=1**: The counter increments on the rising edge of sig\_ch0\_un.



- `PCNT_CHO_NEG_MODE_Un=0`: The counter idles on the falling edge of `sig_ch0_un`.
- `PCNT_CNT_H_LIM_Un=5`: When `pulse_cnt` counts up to `PCNT_CNT_H_LIM_Un`, it is cleared.

### 43.6.2 Channel 0 Decrementing Independently

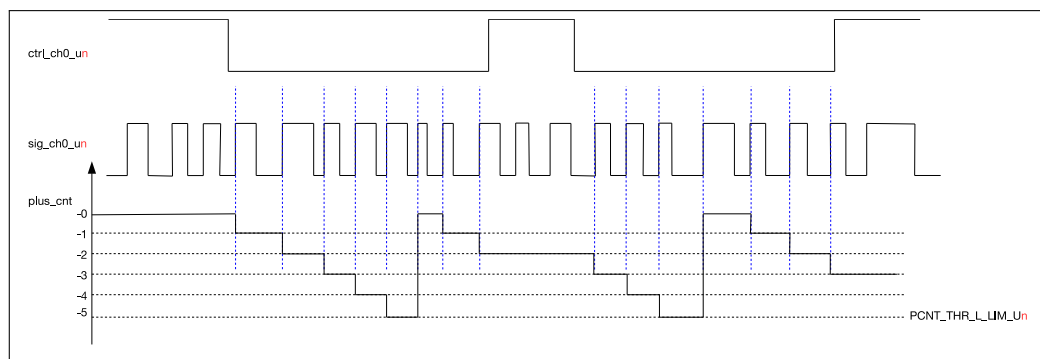


Figure 43.6-2. Channel 0 Down Counting Diagram

Figure 43.6-2 illustrates how channel 0 is configured to decrement independently on the rising edge of `sig_ch0_un` while channel 1 is disabled. The configuration of channel 0 in this case differs from that in Figure 43.6-1 in the following aspects:

- `PCNT_CHO_POS_MODE_Un=2`: the counter decrements on the rising edge of `sig_ch0_un`.
- `PCNT_CNT_L_LIM_Un=-5`: when `pulse_cnt` counts down to `PCNT_CNT_L_LIM_Un`, it is cleared.

### 43.6.3 Channel 0 and Channel 1 Incrementing Together

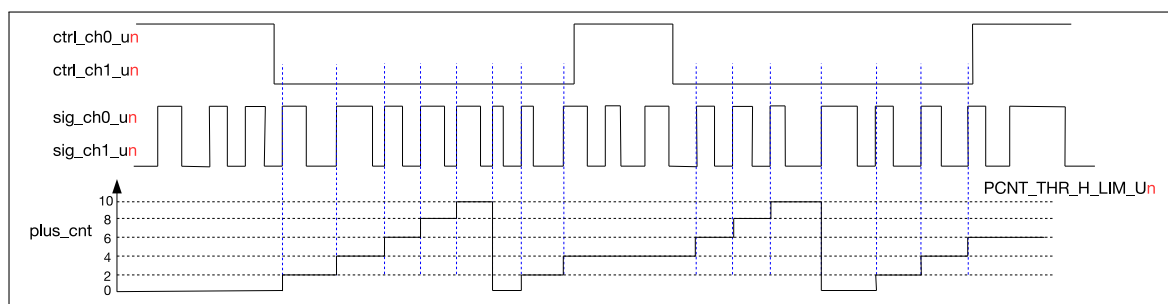


Figure 43.6-3. Two Channels Up Counting Diagram

Figure 43.6-3 illustrates how channel 0 and channel 1 are configured to increment on the rising edge of `sig_ch0_un` and `sig_ch1_un` respectively at the same time. It can be seen in Figure 43.6-3 that control signal `ctr_ch0_un` and `ctr_ch1_un` have the same waveform, so as input pulse signal `sig_ch0_un` and `sig_ch1_un`. The configuration procedure is shown below.

- For channel 0:
  - `PCNT_CHO_LCTRL_MODE_Un=0`: When `ctr_ch0_un` is low, the counter mode specified for the low state turns on, in this case it is Increment mode.

- `PCNT_CHO_HCTRL_MODE_Un`=2: When `ctrl_ch0_un` is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
- `PCNT_CHO_POS_MODE_Un`=1: The counter increments on the rising edge of `sig_ch0_un`.
- `PCNT_CHO_NEG_MODE_Un`=0: The counter idles on the falling edge of `sig_ch0_un`.
- For channel 1:
  - `PCNT_CH1_LCTRL_MODE_Un`=0: When `ctrl_ch1_un` is low, the counter mode specified for the low state turns on, in this case it is Increment mode.
  - `PCNT_CH1_HCTRL_MODE_Un`=2: When `ctrl_ch1_un` is high, the counter mode specified for the low state turns on, in this case it is Disable mode.
  - `PCNT_CH1_POS_MODE_Un`=1: The counter increments on the rising edge of `sig_ch1_un`.
  - `PCNT_CH1_NEG_MODE_Un`=0: The counter idles on the falling edge of `sig_ch1_un`.
- `PCNT_CNT_H_LIM_Un`=10: When `pulse_cnt` counts up to `PCNT_CNT_H_LIM_Un`, it is cleared.

## 43.7 Register Summary

The addresses in this section are relative to **Pulse Count Controller** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                               | Description                         | Address | Access |
|------------------------------------|-------------------------------------|---------|--------|
| <b>Configuration Register</b>      |                                     |         |        |
| <a href="#">PCNT_U0_CONFO_REG</a>  | Configuration register 0 for unit 0 | 0x0000  | R/W    |
| <a href="#">PCNT_U0_CONF1_REG</a>  | Configuration register 1 for unit 0 | 0x0004  | R/W    |
| <a href="#">PCNT_U0_CONF2_REG</a>  | Configuration register 2 for unit 0 | 0x0008  | R/W    |
| <a href="#">PCNT_U1_CONFO_REG</a>  | Configuration register 0 for unit 1 | 0x000C  | R/W    |
| <a href="#">PCNT_U1_CONF1_REG</a>  | Configuration register 1 for unit 1 | 0x0010  | R/W    |
| <a href="#">PCNT_U1_CONF2_REG</a>  | Configuration register 2 for unit 1 | 0x0014  | R/W    |
| <a href="#">PCNT_U2_CONFO_REG</a>  | Configuration register 0 for unit 2 | 0x0018  | R/W    |
| <a href="#">PCNT_U2_CONF1_REG</a>  | Configuration register 1 for unit 2 | 0x001C  | R/W    |
| <a href="#">PCNT_U2_CONF2_REG</a>  | Configuration register 2 for unit 2 | 0x0020  | R/W    |
| <a href="#">PCNT_U3_CONFO_REG</a>  | Configuration register 0 for unit 3 | 0x0024  | R/W    |
| <a href="#">PCNT_U3_CONF1_REG</a>  | Configuration register 1 for unit 3 | 0x0028  | R/W    |
| <a href="#">PCNT_U3_CONF2_REG</a>  | Configuration register 2 for unit 3 | 0x002C  | R/W    |
| <a href="#">PCNT_CTRL_REG</a>      | Control register for all counters   | 0x0060  | R/W    |
| <b>Status Register</b>             |                                     |         |        |
| <a href="#">PCNT_U0_CNT_REG</a>    | Counter value for unit 0            | 0x0030  | RO     |
| <a href="#">PCNT_U1_CNT_REG</a>    | Counter value for unit 1            | 0x0034  | RO     |
| <a href="#">PCNT_U2_CNT_REG</a>    | Counter value for unit 2            | 0x0038  | RO     |
| <a href="#">PCNT_U3_CNT_REG</a>    | Counter value for unit 3            | 0x003C  | RO     |
| <a href="#">PCNT_U0_STATUS_REG</a> | PNCT UNIT0 status register          | 0x0050  | RO     |
| <a href="#">PCNT_U1_STATUS_REG</a> | PNCT UNIT1 status register          | 0x0054  | RO     |
| <a href="#">PCNT_U2_STATUS_REG</a> | PNCT UNIT2 status register          | 0x0058  | RO     |
| <a href="#">PCNT_U3_STATUS_REG</a> | PNCT UNIT3 status register          | 0x005C  | RO     |
| <b>Interrupt Register</b>          |                                     |         |        |
| <a href="#">PCNT_INT_RAW_REG</a>   | Interrupt raw status register       | 0x0040  | RO     |
| <a href="#">PCNT_INT_ST_REG</a>    | Interrupt status register           | 0x0044  | RO     |
| <a href="#">PCNT_INT_ENA_REG</a>   | Interrupt enable register           | 0x0048  | R/W    |
| <a href="#">PCNT_INT_CLR_REG</a>   | Interrupt clear register            | 0x004C  | WO     |
| <b>Version Register</b>            |                                     |         |        |
| <a href="#">PCNT_DATE_REG</a>      | PCNT version control register       | 0x00FC  | R/W    |

## 43.8 Registers

The addresses in this section are relative to **Pulse Count Controller** base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 43.1. PCNT\_UN\_CONF0\_REG (*n*: 0-3) (0x0000+0xC\**n*)**

|                        |    |    |    |     |    |    |    |     |    |    |    |     |    |    |    |     |    |    |    |    |    |   |  |   |  |  |  |                        |  |  |  |   |  |  |  |   |  |  |   |   |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------------|----|----|----|-----|----|----|----|-----|----|----|----|-----|----|----|----|-----|----|----|----|----|----|---|--|---|--|--|--|------------------------|--|--|--|---|--|--|--|---|--|--|---|---|--|--|--|------|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| PCNT_CH1_LCTRL_MODE_U0 |    |    |    |     |    |    |    |     |    |    |    |     |    |    |    |     |    |    |    |    |    |   |  |   |  |  |  | PCNT_CH1_HCTRL_MODE_U0 |  |  |  |   |  |  |  |   |  |  |   |   |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH1_POS_MODE_U0 |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH1_NEG_MODE_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH0_LCTRL_MODE_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH0_HCTRL_MODE_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH0_POS_MODE_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_CH0_NEG_MODE_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_THR_THRES0_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_THR_THRES1_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_THR_L_LIM_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_THR_H_LIM_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_THR_ZERO_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_FILTER_EN_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_FILTER_THRES_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                     | 30 | 29 | 28 | 27  | 26 | 25 | 24 | 23  | 22 | 21 | 20 | 19  | 18 | 17 | 16 | 15  | 14 | 13 | 12 | 11 | 10 | 9 |  |   |  |  |  |                        |  |  |  |   |  |  |  |   |  |  | 0 |   |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x0                    |    |    |    | 0x0 |    |    |    | 0x0 |    |    |    | 0x0 |    |    |    | 0x0 |    |    |    | 0  |    |   |  | 0 |  |  |  | 1                      |  |  |  | 1 |  |  |  | 1 |  |  |   | 1 |  |  |  | 0x10 |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**PCNT\_FILTER\_THRES\_U*n*** Configures the maximum threshold for the filter. Any pulses with width less than this will be ignored when the filter is enabled.

Measurement unit: APB\_CLK cycles.

(R/W)

**PCNT\_FILTER\_EN\_U*n*** This is the enable bit for unit *n*'s input filter. (R/W)

**PCNT\_THR\_ZERO\_EN\_U*n*** This is the enable bit for unit *n*'s zero comparator. (R/W)

**PCNT\_THR\_H\_LIM\_EN\_U*n*** This is the enable bit for unit *n*'s thr\_h\_lim comparator. Configures it to enable the high limit interrupt. (R/W)

**PCNT\_THR\_L\_LIM\_EN\_U*n*** This is the enable bit for unit *n*'s thr\_l\_lim comparator. Configures it to enable the low limit interrupt. (R/W)

**PCNT\_THR\_THRES0\_EN\_U*n*** This is the enable bit for unit *n*'s thres0 comparator. (R/W)

**PCNT\_THR\_THRES1\_EN\_U*n*** This is the enable bit for unit *n*'s thres1 comparator. (R/W)

**PCNT\_CH0\_NEG\_MODE\_U*n*** Configures the behavior when the signal input of channel 0 detects a falling edge.

- 1: Increment the counter
- 2: Decrement the counter
- 0, 3: No effect

(R/W)

**PCNT\_CH0\_POS\_MODE\_U*n*** Configures the behavior when the signal input of channel 0 detects a rising edge.

- 1: Increment the counter
- 2: Decrement the counter
- 0, 3: No effect

(R/W)

**PCNT\_CH0\_HCTRL\_MODE\_U*n*** Configures how the CH*n*\_POS\_MODE/CH*n*\_NEG\_MODE settings will be modified when the control signal is high.

- 0: No modification
- 1: Invert behavior (increase → decrease, decrease → increase)
- 2, 3: Inhibit counter modification

(R/W)

Continued on the next page...

**Register 43.1. PCNT\_UN\_CONFO\_REG (*n*: 0-3) (0x0000+0xC\**n*)**

Continued from the previous page...

**PCNT\_CHO\_LCTRL\_MODE\_UN** Configures how the CH*n*\_POS\_MODE/CH*n*\_NEG\_MODE settings will be modified when the control signal is low.

0: No modification

1: Invert behavior (increase → decrease, decrease → increase)

2, 3: Inhibit counter modification

(R/W)

**PCNT\_CH1\_NEG\_MODE\_UN** Configures the behavior when the signal input of channel 1 detects a falling edge.

1: Increment the counter

2: Decrement the counter

0, 3: No effect

(R/W)

**PCNT\_CH1\_POS\_MODE\_UN** Configures the behavior when the signal input of channel 1 detects a rising edge.

1: Increment the counter

2: Decrement the counter

0, 3: No effect

(R/W)

**PCNT\_CH1\_HCTRL\_MODE\_UN** Configures how the CH*n*\_POS\_MODE/CH*n*\_NEG\_MODE settings will be modified when the control signal is high.

0: No modification

1: Invert behavior (increase → decrease, decrease → increase)

2, 3: Inhibit counter modification

(R/W)

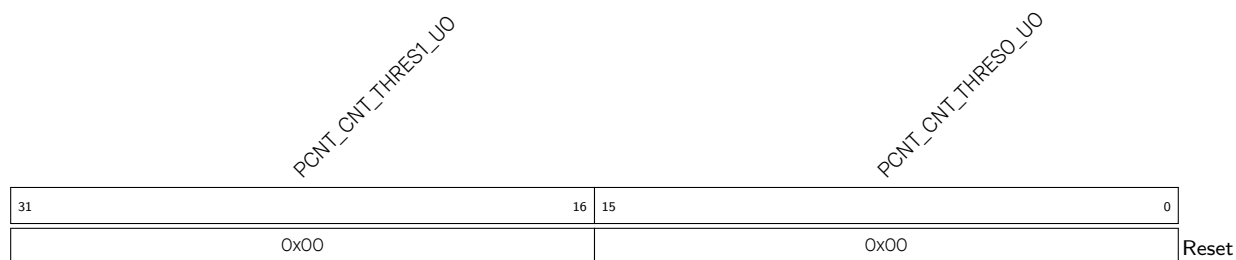
**PCNT\_CH1\_LCTRL\_MODE\_UN** Configures how the CH*n*\_POS\_MODE/CH*n*\_NEG\_MODE settings will be modified when the control signal is low.

0: No modification

1: Invert behavior (increase → decrease, decrease → increase)

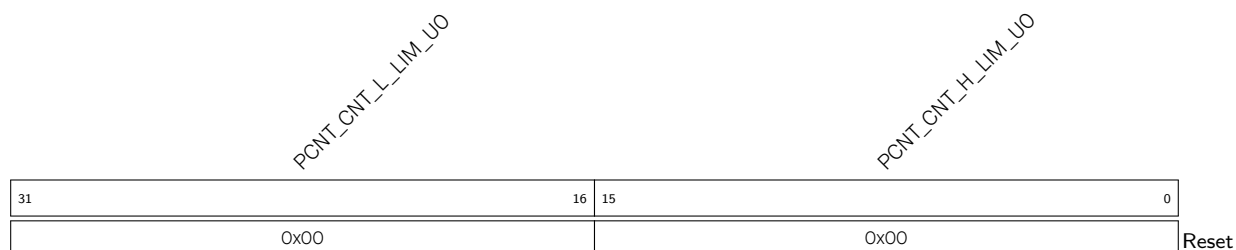
2, 3: Inhibit counter modification

(R/W)

**Register 43.2. PCNT\_UN\_CONF1\_REG (*n*: 0-3) (0x0004+0xC\**n*)**

**PCNT\_CNT\_THRES0\_UN** Configures the thres0 value for unit *n*. (R/W)

**PCNT\_CNT\_THRES1\_UN** Configures the thres1 value for unit *n*. (R/W)

**Register 43.3. PCNT\_UN\_CONF2\_REG (*n*: 0-3) (0x0008+0xC\**n*)**

**PCNT\_CNT\_H\_LIM\_UN** Configures the thr\_h\_lim value for unit *n*. When pulse\_cnt reaches this value, the counter will be cleared to 0. (R/W)

**PCNT\_CNT\_L\_LIM\_UN** Configures the thr\_l\_lim value for unit *n*. When pulse\_cnt reaches this value, the counter will be cleared to 0.(R/W)

Register 43.4. PCNT\_CTRL\_REG (0x0060)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |    |    |   |   |   |   |   |            |   |   |   |   |   |   |   |  |   |   |   |   |   |       |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|----|----|---|---|---|---|---|------------|---|---|---|---|---|---|---|--|---|---|---|---|---|-------|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PCNT_CLK_EN |    |    |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   | PCNT_CNT_PAUSE_U3<br>PCNT_PULSE_CNT_RST_U3<br>PCNT_CNT_PAUSE_U2<br>PCNT_PULSE_CNT_RST_U2<br>PCNT_CNT_PAUSE_U1<br>PCNT_PULSE_CNT_RST_U1<br>PCNT_CNT_PAUSE_U0<br>PCNT_PULSE_CNT_RST_U0 |   |   |   |   |   |       |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17          | 16 | 15 |   |   |   |   |   |            |   |   | 8 | 7 | 6 | 5 | 4 | 3  | 2 | 1 | 0 |   |   |       |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0           | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0  | 1 | 0 | 1 | 0 | 1 | Reset |  |  |  |  |  |

Reset

**PCNT\_PULSE\_CNT\_RST\_U $n$**  Write 1 to clear unit  $n$ 's counter.

0: No effect

1: Clear

(R/W)

**PCNT\_CNT\_PAUSE\_U $n$**  Write 1 to freeze unit  $n$ 's counter.

0: No effect

1: Freeze

(R/W)

**PCNT\_CLK\_EN** Configures whether or not to enable the registers clock gate of PCNT module.

0: the clock for registers is enabled when registers are read and written

1: the clock for registers is always on

(R/W)

Register 43.5. PCNT\_U $n$ \_CNT\_REG ( $n$ : 0-3) (0x0030+0x4\* $n$ )

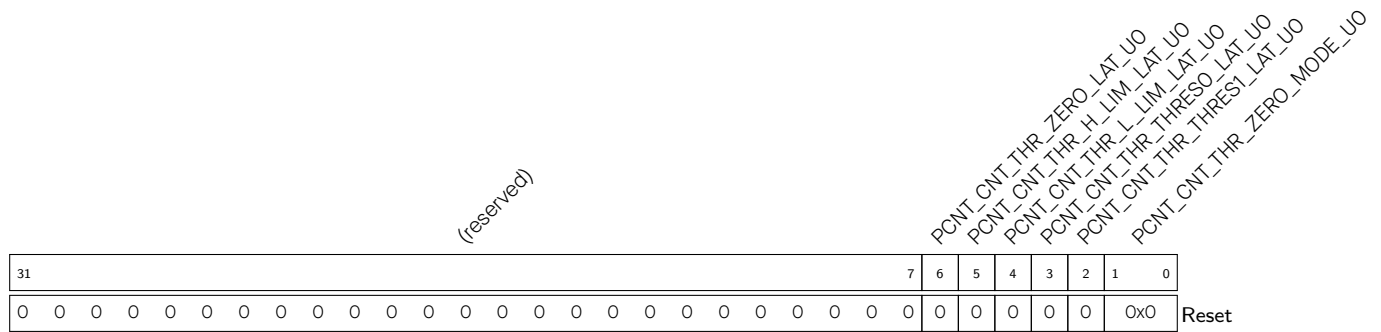
|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PCNT_PULSE_CNT_U0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**PCNT\_PULSE\_CNT\_U $n$**  Represents the current pulse count value for unit  $n$ . (RO)



## Register 43.6. PCNT\_UN\_STATUS\_REG (n: 0-3) (0x0050+0x4\*n)



**PCNT\_CNT\_THR\_ZERO\_MODE\_UN** Represents the pulse counter status of PCNT\_UN corresponding to 0.

- 0: pulse counter decreases from positive to 0
  - 1: pulse counter increases from negative to 0
  - 2: pulse counter is negative
  - 3: pulse counter is positive
- (RO)

**PCNT\_CNT\_THR\_THRES1\_LAT\_UN** Represents whether the current value of PCNT\_UN equals to thres1 when thres1 comparator is enabled.

- 0: others
  - 1: the current pulse counter equals to thres1 and thres1 event is valid
- (RO)

**PCNT\_CNT\_THR\_THRES0\_LAT\_UN** Represents whether the current value of PCNT\_UN equals to thres0 when thres0 comparator is enabled.

- 0: others
  - 1: the current pulse counter equals to thres0 and thres0 event is valid
- (RO)

**PCNT\_CNT\_THR\_L\_LIM\_LAT\_UN** Represents whether the current value of PCNT\_UN is equal to the low limit threshold when the low limit comparator is enabled.

- 0: others
  - 1: the current pulse counter equals to thr\_l\_lim and low limit event is valid.
- (RO)

**PCNT\_CNT\_THR\_H\_LIM\_LAT\_UN** Represents whether the current value of PCNT\_UN is equal to the high limit threshold when the high limit comparator is enabled.

- 0: others
  - 1: the current pulse counter equals to thr\_h\_lim and high limit event is valid.
- (RO)

**PCNT\_CNT\_THR\_ZERO\_LAT\_UN** Represents whether the current value of PCNT\_UN is 0 when the over-zero comparator is enabled.

- 0: others
  - 1: the current pulse counter equals to 0 and zero threshold event is valid.
- (RO)

## Register 43.7. PCNT\_INT\_RAW\_REG (0x0040)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PCNT_CNT_THR_EVENT_U3_INT_RAW<br>PCNT_CNT_THR_EVENT_U2_INT_RAW<br>PCNT_CNT_THR_EVENT_U1_INT_RAW<br>PCNT_CNT_THR_EVENT_U0_INT_RAW |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | Reset |

**PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT\_RAW** The raw interrupt status of the PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT interrupt. (RO)

## Register 43.8. PCNT\_INT\_ST\_REG (0x0044)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PCNT_CNT_THR_EVENT_U3_INT_ST<br>PCNT_CNT_THR_EVENT_U2_INT_ST<br>PCNT_CNT_THR_EVENT_U1_INT_ST<br>PCNT_CNT_THR_EVENT_U0_INT_ST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

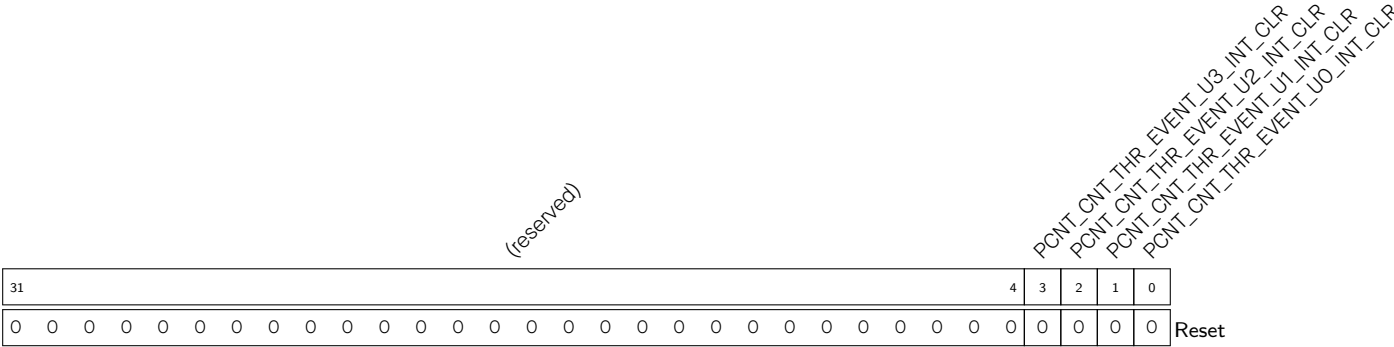
**PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT\_ST** The masked interrupt status of the PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT interrupt. (RO)

## Register 43.9. PCNT\_INT\_ENA\_REG (0x0048)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PCNT_CNT_THR_EVENT_U3_INT_ENA<br>PCNT_CNT_THR_EVENT_U2_INT_ENA<br>PCNT_CNT_THR_EVENT_U1_INT_ENA<br>PCNT_CNT_THR_EVENT_U0_INT_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4  | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

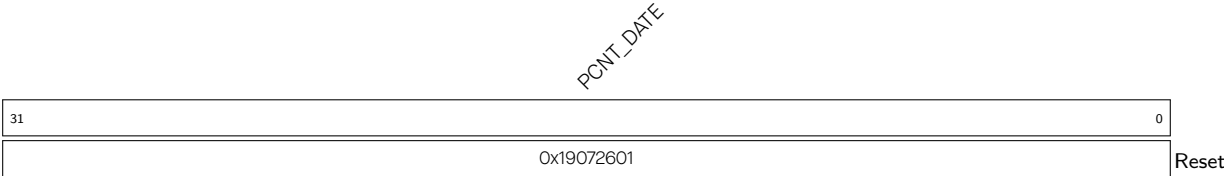
**PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT\_ENA** Write 1 to enable the PCNT\_CNT\_THR\_EVENT\_U $n$ \_INT interrupt. (R/W)

Register 43.10. PCNT\_INT\_CLR\_REG (0x004C)



PCNT\_CNT\_THR\_EVENT\_U<sub>*n*</sub>\_INT\_CLR Write 1 to clear the PCNT\_CNT\_THR\_EVENT\_U<sub>*n*</sub>\_INT interrupt. (WO)

Register 43.11. PCNT\_DATE\_REG (0x00FC)



PCNT\_DATE Version control register. (R/W)

## Chapter 44

# USB 2.0 High-Speed OTG

## 44.1 Overview

The ESP32-P4 chip features a USB 2.0 High-Speed On-The-Go peripheral (OTG\_HS) with an integrated transceiver. This OTG\_HS complies with the USB 2.0 specification, OTG Revision 1.3, and OTG Revision 2.0 specifications. The interface supports USB 2.0 High-Speed mode (480 Mbit/s), Full-Speed mode (12 Mbit/s), and Low-Speed mode (1.5 Mbit/s).

- When OTG\_HS operates in High-Speed or Full-Speed modes, it can be configured as either a Host or a Device.
- When OTG\_HS operates in Low-Speed mode, it can only be configured as a Host.

## 44.2 Glossary

The following abbreviations and terms are used in this chapter.

|                                |  |
|--------------------------------|--|
| <b>Host</b>                    | The host computer system where the USB Host Controller is installed. This includes the host hardware platform (CPU, bus, etc.) and the operating system in use.  |
| <b>Device</b>                  | A logical or physical entity that performs a function. The actual entity described depends on the context of the reference. At the lowest level, device may refer to a single hardware component, as in a memory device. At a higher level, it may refer to a collection of hardware components that perform a particular function, such as a USB interface device. At an even higher level, device may refer to the function performed by an entity attached to the USB; for example, a data/FAX modem device. When used as a non-specific reference, a USB device is either a hub or a function. |
| <b>High-speed</b>              | USB operation at 480 Mbit/s.   |
| <b>Full-speed</b>              | USB operation at 12 Mbit/s.  |
| <b>Low-speed</b>               | USB operation at 1.5 Mbit/s.   |
| <b>Endpoint</b>                | A uniquely addressable portion of a USB device that is the source or sink of information in a communication flow between the host and device.  |
| <b>Scatter/Gather DMA mode</b> | Accesses discontinuous memory areas via DMA.   |
| <b>Buffer DMA mode</b>         | Accesses contiguous memory areas via DMA.  |
| <b>Slave mode</b>              | Accesses memory area through the CPU.  |
| <b>RX FIFO</b>                 | Stores the received data.  |

|                          |  |
|--------------------------|--|
| <b>TX FIFO</b>           | Stores the data to be transmitted.                                       |
| <b>Periodic FIFO</b>     | Stores Isochronous transfer data and Interrupt transfer data to be sent. |
| <b>Non-periodic FIFO</b> | Stores Control transfer data and Bulk transfer data to be sent.          |

## 44.3 Features

### 44.3.1 General Features

- USB 2.0 specification, OTG Revision 1.3 and OTG Revision 2.0 specifications
- High-Speed, Full-Speed, and Low-Speed data rates
- As a host and a device in High-Speed mode and Full-Speed mode
- Dynamic FIFO (DFIFO) sizing, each device EP/host channel can dynamically allocate a maximum of 4 KB FIFO.
- Multiple modes of memory access
  - Scatter/Gather DMA mode
  - Buffer DMA mode
  - Slave Mode
- Integrated UTMI High-Speed transceiver

### 44.3.2 Device Mode Features

- Endpoint 0 always present, bi-directional, consisting of EPO IN and EPO OUT
- 15 additional endpoints 1~15, configurable as IN or OUT
- Maximum of eight IN endpoints concurrently active at any time, including EPO IN
- All OUT endpoints share a single RX FIFO
- Each IN endpoint has a dedicated TX FIFO

### 44.3.3 Host Mode Features

- 16 host channels
- RX FIFO: shared by all periodic and non-periodic transactions
- Two TX FIFO:
  - One shared by all non-periodic transactions
  - One shared by all periodic transactions
- All of the above FIFOs share a 4 KB RAM.
- The size of each FIFO is configurable, with a maximum of 4 KB.

## 44.4 Functional Description

### 44.4.1 Controller Core and Interfaces

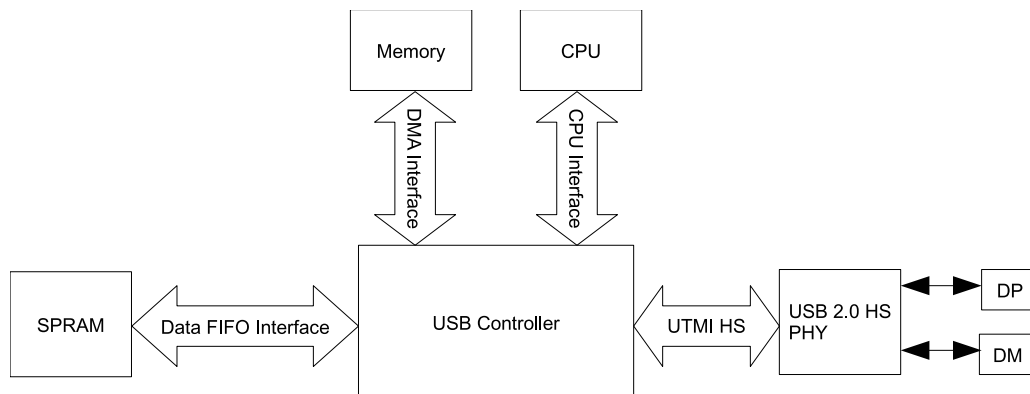


Figure 44.4-1. OTG\_HS System Architecture

OTG\_HS uses the same controller core as OTG\_FS, i.e., USB Controller Core. The controller core has the following interfaces, see Figure 44.4-1:

- **CPU Interface**

Provides the CPU with read/write access to the controller core's various registers and FIFOs. This interface is internally implemented as an AHB slave interface. The way to access the FIFOs through the CPU interface is called Slave mode.

- **DMA Interface**

Provides the controller core's internal DMA with read/write access to system memory, e.g., fetching and writing data payloads in DMA mode. This interface is internally implemented as an AHB master interface.

- **USB 2.0 Interface (USB 2.0 HS PHY)**

This interface is used to connect the controller core to a USB 2.0 UTMI serial transceiver. With this serial transceiver, OTG\_HS is able to support High-Speed data rate and Full-Speed data rate.

- **Data FIFO Interface**

The multiple FIFOs used by the controller core are not actually located within the controller core itself, but on the Single-Port RAM (SPRAM). FIFOs are dynamically sized, thus are allocated at run-time in the SPRAM. When the CPU, DMA, or the controller core attempts to read/write to FIFOs, those accesses are routed through the data FIFO RAM interface.

### 44.4.2 Memory Layout

Figure 44.4-2 illustrates the memory layout of the registers which are used to configure and control the USB Controller Core.

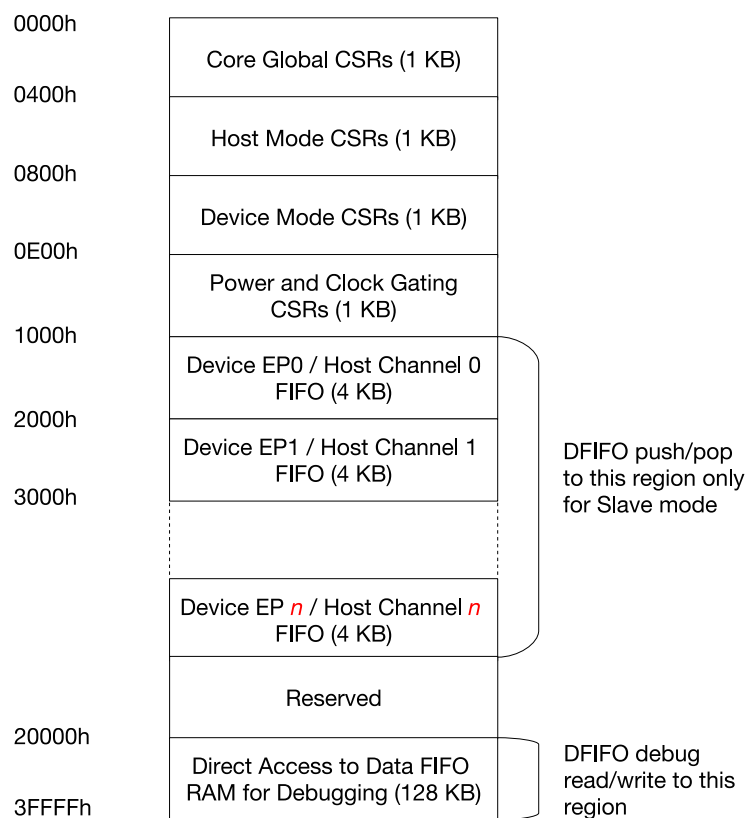


Figure 44.4-2. OTG\_HS Register Layout

#### 44.4.2.1 Control & Status Registers (CSRs)

- **Core Global CSRs**

These registers are responsible for the configuration/control/status of the global features of OTG\_HS, i.e., features which are common to both Host and Device modes. These features include OTG control and system-level interrupts. Software can access these registers whilst in Host or Device modes.

- **Host Mode CSRs**

These registers are responsible for the configuration/control/status in Host mode, thus should only be accessed in Host mode. Each channel has its own set of registers within the Host mode CSRs.

- **Device Mode CSRs**

These registers are responsible for the configuration/control/status in Device mode, thus should only be accessed in Device mode. Each endpoint has its own set of registers within the Device mode CSRs.

- **Power and Clock Gating Register**

A single register controls power-down and gates various clocks.

#### 44.4.2.2 FIFO Access

The OTG\_HS makes use of multiple FIFOs to buffer the data payloads to be transmitted or to buffer the received data payloads. The number and type of FIFOs are dependent on Host or Device mode, and the number of channels or endpoints used, see Section 44.4.3. There are two ways to access the FIFOs: DMA mode and Slave mode. In Slave mode, the CPU will need to access these FIFOs by reading and writing to either the DFIFO push/pop regions or the DFIFO read/write debug region. FIFO access is governed by the

following rules:

- Read access to any address in any one of the 4 KB push/pop regions will result in a pop from the shared RX FIFO.
- Write access to a particular 4 KB push/pop region will result in a push to the corresponding endpoint or channel's TX FIFO given that the endpoint is an IN endpoint, or the channel is an OUT channel.
  - In Device mode, data is pushed to the corresponding IN endpoint's dedicated TX FIFO.
  - In Host mode, data is pushed to the non-periodic TX FIFO or the periodic TX FIFO depending on whether the channel is a non-periodic channel, or a periodic channel.
- Access to the 128 KB read/write region will result in direct read/write instead of a push/pop. This is generally used for debugging purposes only.

Note that pushing and popping data to and from the FIFOs by the CPU is only required in Slave mode. In DMA mode, the internal DMA will handle all pushing/popping of data to and from the TX and RX FIFOs.

### 44.4.3 FIFO and Queue Organization

The FIFOs in OTG\_HS are primarily used to hold data packet payloads, i.e., the data field of USB Data packets. TX FIFOs are used to store data payloads that will be transmitted by OUT transactions in Host mode or IN transactions in Device mode. RX FIFOs are used to store received data payloads of IN transactions in Host mode or OUT transactions in Device mode. In addition to storing data payloads, RX FIFOs also store a **status entry** for each data payload. Each status entry contains information about a data payload such as channel number, byte count, and validity status. In Slave mode, status entries are also used to indicate various channel events.

The portion of SPRAM that can be used for FIFO allocation has a depth of 1024 and a width of 35 bits (32 data bits plus 3 control bits). The multiple FIFOs used by each channel (in Host mode) or endpoint (in Device mode) are allocated into the SPRAM and can be dynamically sized.

#### 44.4.3.1 Host Mode FIFOs and Queues

The following FIFOs are used in Host mode, see Figure [44.4-3](#):



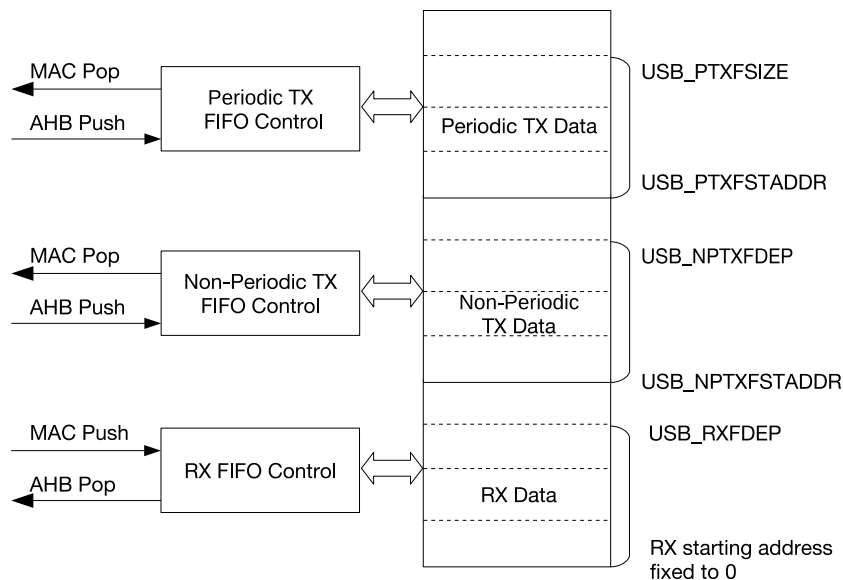


Figure 44.4-3. Host Mode FIFOs

- **Non-periodic TX FIFO:** Stores data payloads of bulk and control OUT transactions for all channels.
- **Periodic TX FIFO:** Stores data payloads of interrupt or isochronous OUT transactions for all channels.
- **RX FIFO:** Stores data payloads of all IN transactions, and status entries that are used to indicate size of data payloads and transaction/channel events such as transfer complete or channel halted.

In addition to FIFOs, Host mode also contains two request queues used to queue up the various transaction request from the multiple channels. Each entry in a request queue holds the IN/OUT channel number along with other information to perform the transaction, such as transaction type. Request queues are also used to queue other types of requests such as a channel halt request.

Unlike FIFOs, request queues are fixed in size and cannot be accessed directly by software. Rather, once a channel is enabled, requests will be automatically written to the request queue by the Host core. The order in which the requests are written into the queue determines the sequence of transactions on the USB.

Host mode contains the following request queues:

- **Non-periodic request queue:** Request queue for all non-periodic Bulk and Control channels. The queue has a depth of four entries.
- **Periodic request queue:** Request queue for all periodic Interrupt and Isochronous channels. The queue has a depth of four entries.

When scheduling transactions, hardware will execute all requests on the periodic request queue first before executing requests on the non-periodic request queue.

#### 44.4.3.2 Device Mode FIFOs

The following FIFOs are used in Device mode, see Figure 44.4-4:

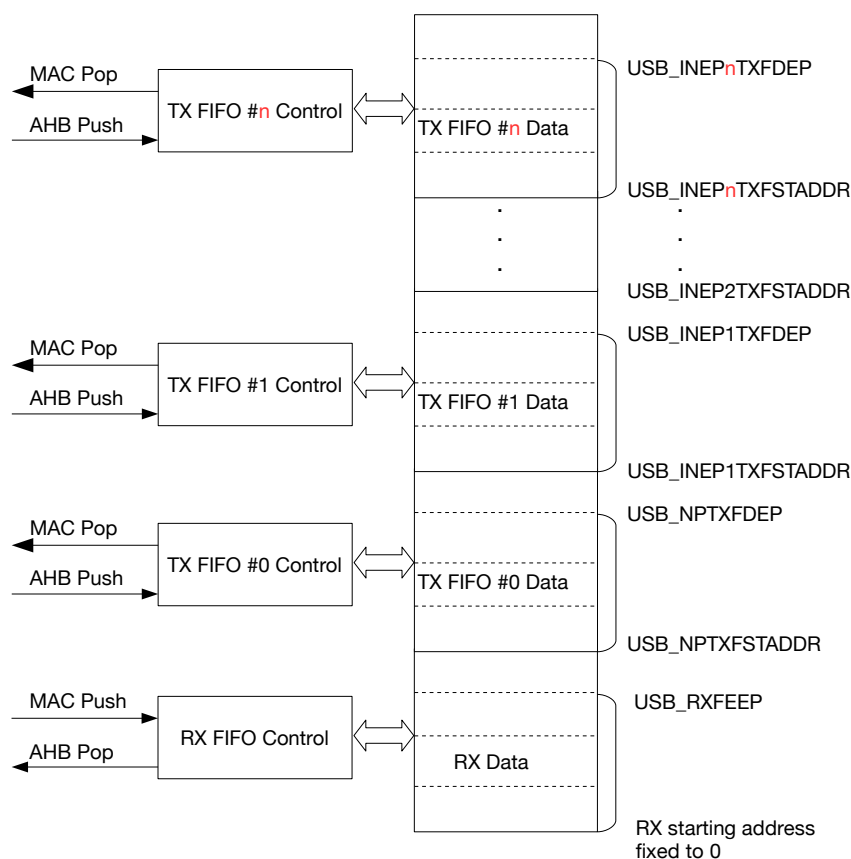


Figure 44.4-4. Device Mode FIFOs

- **RX FIFO:** Stores data payloads received in Data packet, and status entries used to indicate size of those data payloads.
- **Dedicated TX FIFO:** Each active IN endpoint will have a dedicated TX FIFO used to store all IN data payloads of that endpoint, regardless of the transaction type, both periodic and non-periodic IN transactions.

Due to the dedicated FIFOs, Device mode does not use any request queues. Instead, the order of IN transactions are determined by the Host.

#### 44.4.4 Interrupt Hierarchy

OTG\_HS provides a single interrupt line which can be routed via the interrupt matrix to one of the CPUs. The interrupt signal can be unmasked by setting USB\_GLBLINTRMSK. The OTG\_HS interrupt is an OR of all bits in the USB\_GINTSTS\_REG register, and the bits in USB\_GINTSTS\_REG can be unmasked by setting the corresponding bits in the USB\_GINTMSK\_REG register. USB\_GINTSTS\_REG contains system level interrupts, and also specific bits for Host or Device mode interrupts, and OTG specific interrupts. OTG\_HS interrupt sources are organized as Figure 44.4-5 shows.

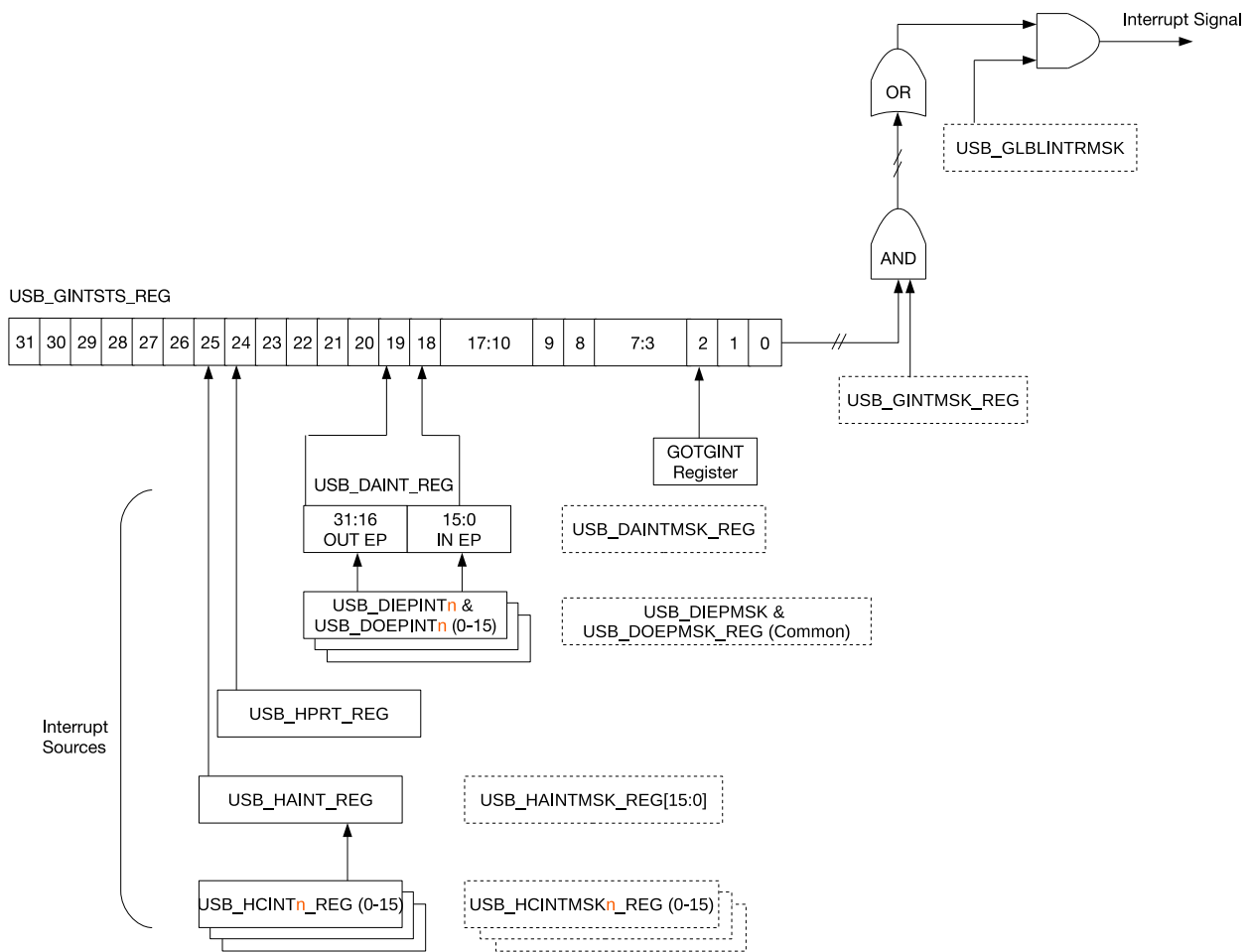


Figure 44.4-5. OTG\_HS Interrupt Hierarchy

The following bits of the USB\_GINTSTS\_REG register indicate an interrupt source lower in the hierarchy:

- **USB\_PRTINT** indicates that the Host port has a pending interrupt. The USB\_HPRT\_REG register indicates the interrupt source.
- **USB\_HCHINT** indicates that one or more Host channels have a pending interrupt. Read the USB\_HAINT\_REG register to determine which channel(s) have a pending interrupt, then read the pending channel's USB\_HCINT<sub>n</sub>\_REG register to determine the interrupt source.
- **USB\_OEPINT** indicates that one or more OUT endpoints have a pending interrupt. Read the USB\_DAJNT\_REG register to determine which OUT endpoint(s) have a pending interrupt, then read the USB\_DOEPINT<sub>n</sub>\_REG register to determine the interrupt source.
- **USB\_IEPINT** indicates that one or more IN endpoints have a pending interrupt. Read the USB\_DAJNT\_REG register to determine which IN endpoint(s) are pending, then read the pending IN endpoint's USB\_DIEPINT<sub>n</sub>\_REG register to determine the interrupt source.
- **USB\_OTGINT** indicates an On-The-Go event has triggered an interrupt. Read the USB\_GOTGINT\_REG register to determine which OTG event(s) triggered the interrupt.

## 44.4.5 DMA Modes and Slave Mode

USB OTG supports three ways to access memory: Slave mode, Buffer DMA mode, and Scatter/Gather DMA mode.

### 44.4.5.1 Slave Mode

In Slave mode, all data payloads must be pushed/popped to and from the FIFOs by the CPU.

- When transmitting a packet using IN endpoints or OUT channels, the data payload must be pushed into the corresponding endpoint or channel's TX FIFO.
- When receiving a packet, the packet's status entry must first be popped off the RX FIFO by reading USB\_GRXSTSP\_REG. The status entry should be used to determine the length of the packet's payload in bytes. The corresponding number of bytes must then be manually popped off the RX FIFO by reading from the RX FIFO's memory region.

### 44.4.5.2 Buffer DMA Mode

Buffer mode is similar to Slave mode but utilizes the internal DMA to push and pop data payloads to the FIFOs.

- When transmitting a packet using IN endpoints or OUT channels, the data payload's address in memory should be written to the USB\_HCDMA $n$ \_REG (in Host mode) or USB\_DIEPDMA $n$ \_REG (in Device mode) registers. When the endpoint or channel is enabled, the internal DMA will push the data payload from memory into the TX FIFO of the channel or endpoint.
- When receiving a packet using OUT endpoints or IN channels, the address of an empty buffer in memory should be written to the USB\_HCDMA $n$ \_REG (in Host mode) or USB\_DOEPDMA $n$ \_REG (in Device mode) registers. When the endpoint or channel is enabled, the internal DMA will pop the data payload from RX FIFO into the buffer.

### 44.4.5.3 Scatter/Gather DMA Mode

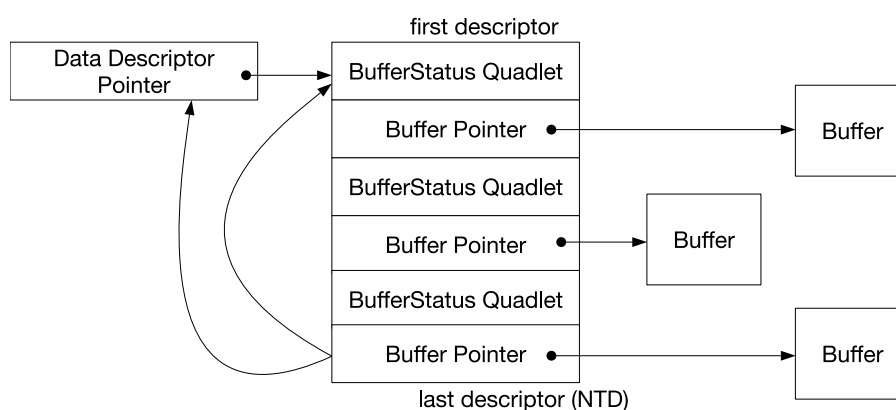


Figure 44.4-6. Scatter/Gather DMA Descriptor List

In Scatter/Gather DMA mode, buffers containing data payloads can be scattered throughout memory. Each endpoint or channel will have a contiguous DMA descriptor list, where each descriptor contains a 32-bit

pointer to the data payload or buffer and a 32-bit buffer descriptor (BufferStatus Quadlet). The data payloads and buffers can correspond to a single transaction (i.e., < 1 MPS bytes) or an entire transfer (> 1 MPS bytes). MPS: maximum packet size. The list is implemented as a ring buffer meaning that the DMA will return to the first entry when it encounters the last entry on the list.

- When transmitting a transfer/transaction using IN endpoints or OUT channels, the DMA will gather the data payloads from the multiple buffers and push them into a TX FIFO.
- When receiving a transfer/transaction using OUT endpoints or IN channels, the DMA will pop the received data payloads from the RX FIFO and scatter them to the multiple buffers pointed to by the DMA list entries.

## 44.4.6 Transaction and Transfer Level Operation

In either Host or Device mode, communication can operate either at the transaction level or the transfer level.

### 44.4.6.1 Transaction and Transfer Level Operation in DMA Mode

When operating at the transfer level in DMA Host mode, software is interrupted only when a channel has been halted. Channels are halted when their programmed transfer size has completed successfully, has received a STALL, or if there are excessive transaction errors, e.g., 3 consecutive transaction errors. In DMA Device mode, all errors are handled by the controller core itself.

When operating at the transaction level in DMA mode, the transfer size is set to the size of one data packet, either a maximum packet size or a short packet size.

### 44.4.6.2 Transaction and Transfer Level Operation in Slave Mode

When operating at the transaction level in Slave Mode, transfers are handled one transaction at a time. Each data payload should correspond to a single data packet, and software must determine whether a retry of the transaction is necessary based on the handshake response received on the USB, e.g., ACK or NAK.

The following table describes transaction level operation in Slave mode for both IN and OUT transactions.

Table 44.4-1. IN and OUT Transactions in Slave Mode

| Host Mode        | Device Mode |
|------------------|-------------|
| OUT Transactions |             |

| Host Mode   | Device Mode  |
|---|--|
| <ol style="list-style-type: none"> <li>1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_HCTSIZ<sub>n</sub>_REG register, enables the channel, then copies the packet's data payload into the TX FIFO.</li> <li>2. When the last DWORD of the data payload has been pushed, the controller core will automatically write a request into the appropriate request queue.</li> <li>3. If the transaction is successful, the USB_XFERCOMPL interrupt will be generated. If the transaction is unsuccessful, an error interrupt, e.g., USB_H_NACK<sub>n</sub> will occur.</li> </ol> | <ol style="list-style-type: none"> <li>1. Software specifies the expected size of the data packet (1 MPS) and the number of data packets (1 data packet) in the USB_DOEPSIZ<sub>n</sub>_REG register. Once the endpoint is enabled, it will wait for the host to transmit a packet to it.</li> <li>2. The received packet will be pushed into the RX FIFO along with a packet status entry.</li> <li>3. If the transaction is unsuccessful, e.g., due to a full RX FIFO, the endpoint will automatically NAK the incoming packet.</li> </ol> |
| IN Transactions   |  |
| <ol style="list-style-type: none"> <li>1. Software specifies the expected size of the data packet and the number of packets (1 data packet) in the USB_HCTSIZ<sub>n</sub>_REG register, then enables the channel.</li> <li>2. The controller core will automatically write a request into the appropriate request queue.</li> <li>3. If the transaction is successful, the received data along with a status entry should be written to the RX FIFO. If the transaction is unsuccessful, an error interrupt, e.g., USB_H_NACK<sub>n</sub> will occur.</li> </ol>  | <ol style="list-style-type: none"> <li>1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_DIEPTSIZ<sub>n</sub>_REG register. Once the endpoint is enabled, it will wait for the host to read the packet.</li> <li>2. When the packet has been transmitted, the USB_XFERCOMPL interrupt will be generated.</li> </ol>  |

When operating at the transfer level in Slave mode, one or more transaction-level operations can be pipelined thus being analogous to transfer level operation in DMA mode. Within pipelined transactions, multiple packets of the same transfer can be read/written from the FIFOs in single instance, thus preventing the need for interrupting the software on a per-packet basis.

Operating on a transfer level in Slave mode is similar to operating on the transaction-level, except the transfer size and packet count for each transfer in the USB\_HCTSIZ<sub>n</sub>\_REG or USB\_DOEPSIZ<sub>n</sub>\_REG register will need to be set to reflect the entire transfer. After the channel or endpoint is enabled, multiple data packets worth of payloads should be written to or read from the TX or RX FIFOs respectively (given that there is enough space or enough data).

### 44.4.7 OTG

Internal ID/VBUS is left floating in OTG\_HS, thus SRP/HNP is not supported. But OTG\_HS still supports Dual-Role-Devices (DRD), i.e, it can be used both as a host and a device. Software can force setting this

controller to work as host or device by configuring ForceDevMode or ForceHstMode in register USB\_GUSBCFG, regardless of the value of ID pin.

## 44.5 Registers

The catalog and comprehensive specifications of USB OTG registers are subject to a Non-Disclosure Agreement (NDA) as mandated by the IP provider. To obtain support information for a particular register, please contact Espressif Technical Support Team via [Technical Inquires](#).

## Chapter 45

# USB 2.0 Full-Speed OTG

## 45.1 Overview

The ESP32-P4 features a USB 2.0 Full-Speed On-The-Go peripheral (henceforth referred to as OTG\_FS) along with integrated transceivers. This OTG\_FS conforms to USB 2.0 specification, OTG Revision 1.3, and OTG Revision 2.0 specifications, OTG\_FS can operate as either a USB Host or Device and supports 12 Mbit/s full-speed (FS) and 1.5 Mbit/s low-speed (LS) data rates of the USB 2.0 specification. The Host Negotiation Protocol (HNP) and the Session Request Protocol (SRP) are also supported.

## 45.2 Glossary

The following abbreviations and terms are used in this chapter.

|  |  |
|--|--|
| <b>Host</b>                            | The host computer system where the USB Host Controller is installed. This includes the host hardware platform (CPU, bus, etc.) and the operating system in use.  |
| <b>Device</b>                          | A logical or physical entity that performs a function. The actual entity described depends on the context of the reference. At the lowest level, device may refer to a single hardware component, as in a memory device. At a higher level, it may refer to a collection of hardware components that perform a particular function, such as a USB interface device. At an even higher level, device may refer to the function performed by an entity attached to the USB; for example, a data/FAX modem device. When used as a non-specific reference, a USB device is either a hub or a function. |
| <b>Full-speed</b>                      | USB operation at 12 Mbit/s.  |
| <b>Low-speed</b>                       | USB operation at 1.5 Mbit/s.   |
| <b>Host Negotiation Protocol (HNP)</b> | Allows the host function to be transferred between two directly connected OTG devices and eliminates the need for a user to switch the cable connections in order to allow a change in control of communications between the devices.  |
| <b>Session Request Protocol (SRP)</b>  | Allows a B-device to request the A-device to turn on the power supply to the USB interface (VBUS) and start a session.   |
| <b>Endpoint</b>                        | A uniquely addressable portion of a USB device that is the source or sink of information in a communication flow between the host and device.  |
| <b>Scatter/Gather DMA mode</b>         | Accesses discontinuous memory areas via DMA.   |



|                          |  |
|--------------------------|--|
| <b>Buffer DMA mode</b>   | Accesses contiguous memory areas via DMA.                                |
| <b>Slave mode</b>        | Accesses memory area through the CPU.                                    |
| <b>RX FIFO</b>           | Stores the received data.  |
| <b>TX FIFO</b>           | Stores the data to be transmitted.                                       |
| <b>Periodic FIFO</b>     | Stores Isochronous transfer data and Interrupt transfer data to be sent. |
| <b>Non-periodic FIFO</b> | Stores Control transfer data and Bulk transfer data to be sent.          |

## 45.3 Features

### 45.3.1 General Features

- USB 2.0 specification, OTG Revision 1.3 and OTG Revision 2.0 specifications
- USB 2.0 full-speed and low-speed data rates
- HNP and SRP as A-device or B-device
- Dynamic FIFO (DFIFO) sizing, maximum to 1 KB
- Multiple modes of memory access
  - Scatter/Gather DMA mode
  - Buffer DMA mode
  - Slave mode
- Two integrated transceivers

### 45.3.2 Device Mode Features

- Endpoint 0 always present, bi-directional, consisting of EPO IN and EPO OUT
- Six additional endpoints 1~6, configurable as IN or OUT
- Maximum of five IN endpoints concurrently active at any time, including EPO IN
- All OUT endpoints share a single RX FIFO
- Each IN endpoint has a dedicated TX FIFO

### 45.3.3 Host Mode Features

- Eight host channels
- RX FIFO: shared by all periodic and non-periodic transactions
- Two TX FIFO:
  - One shared by all non-periodic transactions
  - One shared by all periodic transactions
- All of the above FIFOs share a 1 KB RAM.
- The size of each FIFO is configurable, with a maximum of 1 KB.

## 45.4 Functional Description

### 45.4.1 Controller Core and Interfaces

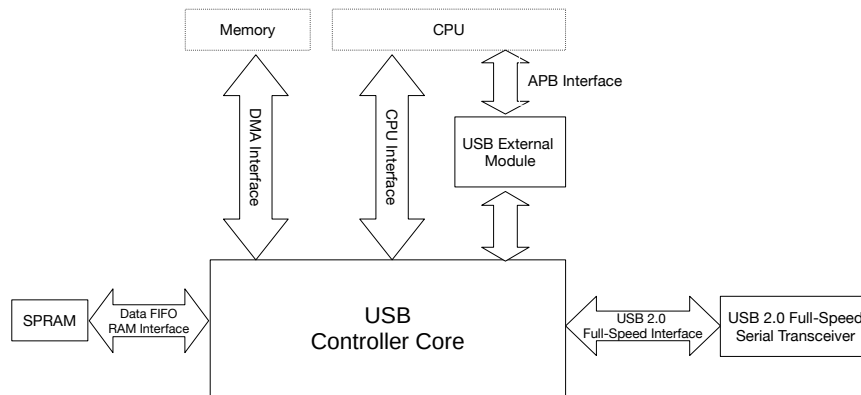


Figure 45.4-1. OTG\_FS System Architecture

The core part of the OTG\_FS peripheral is the USB Controller Core. The controller core has the following interfaces, see Figure 45.4-1:

- **CPU Interface**

Provides the CPU with read/write access to the controller core's various registers and FIFOs. This interface is internally implemented as an AHB slave interface. The way to access the FIFOs through the CPU interface is called Slave mode.

- **APB Interface**

Allows the CPU to control the USB controller core via the USB external controller.

- **DMA Interface**

Provides the controller core's internal DMA with read/write access to system memory, e.g., fetching and writing data payloads in DMA mode. This interface is internally implemented as an AHB master interface.

- **USB 2.0 Full-Speed Interface**

ESP32-P4 has two full-speed transceivers. This interface is used to connect the controller core to one of USB 2.0 full-speed serial transceivers. Aside from USB OTG, ESP32-P4 also includes a USB Serial/JTAG controller, see Chapter 46 [USB Serial/JTAG Controller \(USB\\_SERIAL\\_JTAG\)](#). These two USB controllers can utilize the integrated internal transceivers by time-division multiplexing. In the following sections, GPIO24 and GPIO25 are referred to as FS\_PHY1, while GPIO26 and GPIO27 as FS\_PHY2.

By default FS\_PHY1 connects to USB Serial/JTAG controller and FS\_PHY2 to OTG\_FS. The connection is configurable via eFuse settings:

- 0: FS\_PHY1 is connected to USB Serial/JTAG controller, while FS\_PHY2 to OTG\_FS.
- 1: FS\_PHY2 is connected to USB Serial/JTAG controller, while FS\_PHY1 to OTG\_FS.

- **USB External Controller**

The USB External Controller is primarily used to control the routing of the USB 2.0 full-speed serial interface to the internal registers, thus allowing the CPU to perform query operations, etc. The External Controller can also enable a power saving mode by gating the controller core's clock, i.e., AHB clock, or

powering down the connected SPRAM clock. Note that this power saving mode is different from the power savings via SRP.

- **Data FIFO RAM Interface**

The multiple FIFOs used by the controller core are not actually located within the controller core itself, but on the Single-Port RAM (SPRAM). FIFOs are dynamically sized, thus are allocated at run-time in the SPRAM. When the CPU, DMA, or the controller core attempts to read/write to FIFOs, those accesses are routed through the data FIFO RAM interface.

## 45.4.2 Memory Layout

Figure 45.4-2 illustrates the memory layout of the registers which are used to configure and control the USB Controller Core. Note that USB External Controller uses a separate set of registers called wrap registers.

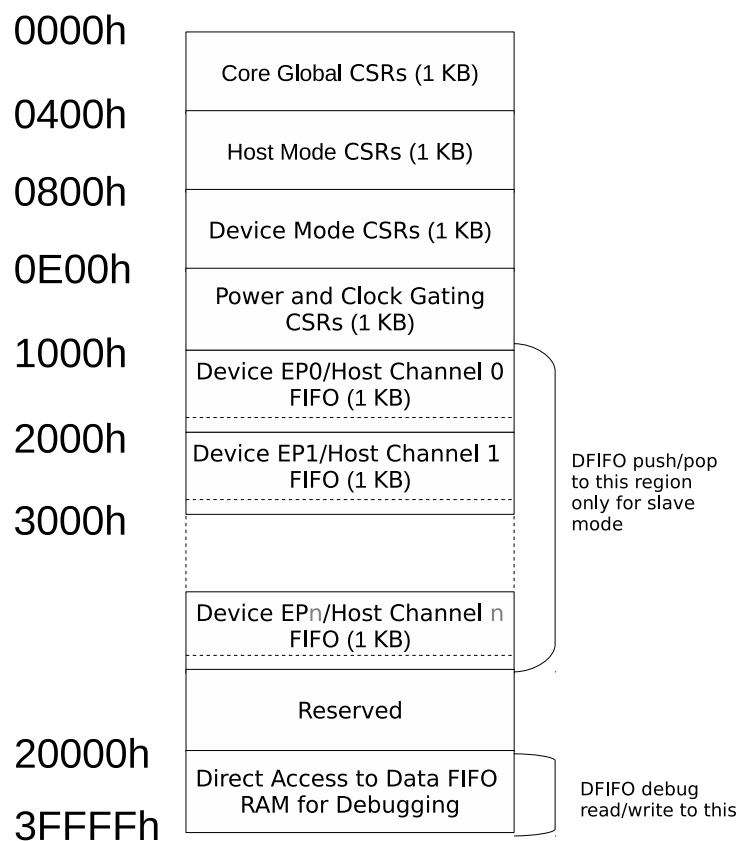


Figure 45.4-2. OTG\_FS Register Layout

### 45.4.2.1 Control & Status Registers (CSRs)

- **Core Global CSRs**

These registers are responsible for the configuration/control/status of the global features of OTG\_FS, i.e., features which are common to both Host and Device modes. These features include:

- OTG control (HNP, SRP, and A/B-device detection);
- USB configuration (Host or Device mode selection and PHY selection);
- and system-level interrupts.

Software can access these registers whilst in Host or Device modes.

- **Host Mode CSRs**

These registers are responsible for the configuration/control/status in Host mode, thus should only be accessed in Host mode. Each channel has its own set of registers within the Host mode CSRs.

- **Device Mode CSRs**

These registers are responsible for the configuration/control/status in Device mode, thus should only be accessed in Device mode. Each endpoint has its own set of registers within the Device mode CSRs.

- **Power and Clock Gating Register**

A single register controls power-down and gates various clocks.

#### 45.4.2.2 FIFO Access

The OTG\_FS makes use of multiple FIFOs to buffer the data payloads to be transmitted or to buffer the received data payloads. The number and type of FIFOs are dependent on Host or Device mode, and the number of channels or endpoints used, see Section 45.4.3. There are two ways to access the FIFOs: DMA mode and Slave mode. In Slave mode, the CPU accesses these FIFOs by reading and writing to either the DFIFO push/pop regions or the DFIFO read/write debug region. FIFO access is governed by the following rules:

- Read access to any address in any one of the 1 KB push/pop regions will result in a pop from the shared RX FIFO.
- Write access to a particular 1 KB push/pop region will result in a push to the corresponding endpoint or channel's TX FIFO given that the endpoint is an IN endpoint, or the channel is an OUT channel.
  - In Device mode, data is pushed to the corresponding IN endpoint's dedicated TX FIFO.
  - In Host mode, data is pushed to the non-periodic TX FIFO or the periodic TX FIFO depending on whether the channel is a non-periodic channel, or a periodic channel.
- Access to the 128 KB read/write region will result in direct read/write instead of a push/pop. This is generally used for debugging purposes only.

Note that pushing and popping data to and from the FIFOs by the CPU is only required in Slave mode. In DMA mode, the internal DMA will handle all pushing/popping of data to and from the TX and RX FIFOs.

#### 45.4.3 FIFO and Queue Organization

The FIFOs in OTG\_FS are primarily used to hold data packet payloads, i.e., the data field of USB Data packets. TX FIFOs are used to store data payloads that will be transmitted by OUT transactions in Host mode or IN transactions in Device mode. RX FIFOs are used to store received data payloads of IN transactions in Host mode or OUT transactions in Device mode. In addition to storing data payloads, RX FIFOs also store a **status entry** for each data payload. Each status entry contains information about a data payload such as channel number, byte count, and validity status. In Slave mode, status entries are also used to indicate various channel events.

The portion of SPRAM that can be used for FIFO allocation has a depth of 256 and a width of 35 bits (32 data bits plus 3 control bits). The multiple FIFOs used by each channel in Host mode or endpoint in Device mode are allocated into the SPRAM and can be dynamically sized.

### 45.4.3.1 Host Mode FIFOs and Queues

The following FIFOs are used in Host mode, see Figure 45.4-3:

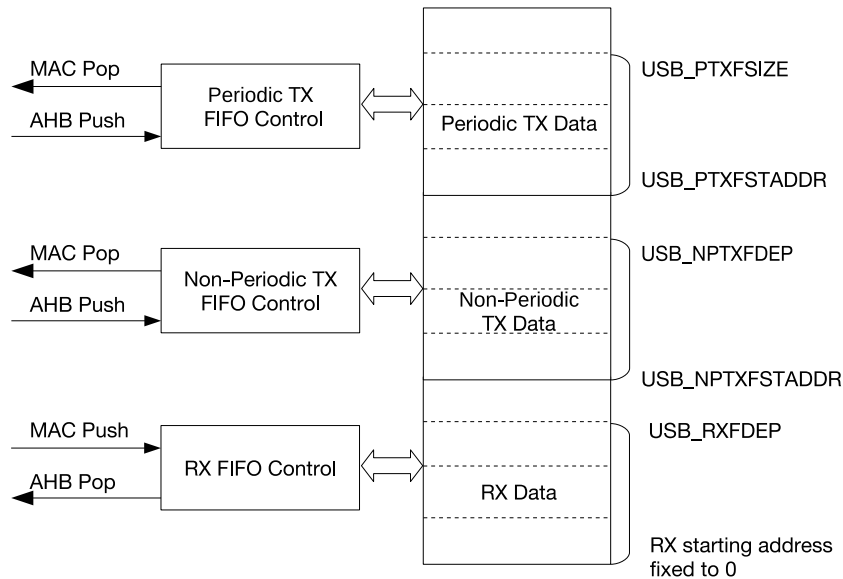


Figure 45.4-3. Host Mode FIFOs

- **Non-periodic TX FIFO:** Stores data payloads of Bulk and Control OUT transactions for all channels.
- **Periodic TX FIFO:** Stores data payloads of Interrupt or Isochronous OUT transactions for all channels.
- **RX FIFO:** Stores data payloads of all IN transactions, and status entries that are used to indicate size of data payloads and transaction/channel events such as transfer complete or channel halted.

In addition to FIFOs, Host mode also contains two request queues used to queue up the various transaction request from the multiple channels. Each entry in a request queue holds the IN/OUT channel number along with other information to perform the transaction, such as transaction type. Request queues are also used to queue other types of requests such as a channel halt request.

Unlike FIFOs, request queues are fixed in size and cannot be accessed directly by software. Rather, once a channel is enabled, requests will be automatically written to the request queue by the Host core. The order in which the requests are written into the queue determines the sequence of transactions on the USB.

Host mode contains the following request queues:

- **Non-periodic request queue:** Request queue for all non-periodic Bulk and Control channels. The queue has a depth of four entries.
- **Periodic request queue:** Request queue for all periodic Interrupt and Isochronous channels. The queue has a depth of eight entries.

When scheduling transactions, hardware will execute all requests on the periodic request queue first before executing requests on the non-periodic request queue.

### 45.4.3.2 Device Mode FIFOs

The following FIFOs are used in Device mode, see Figure 45.4-4:

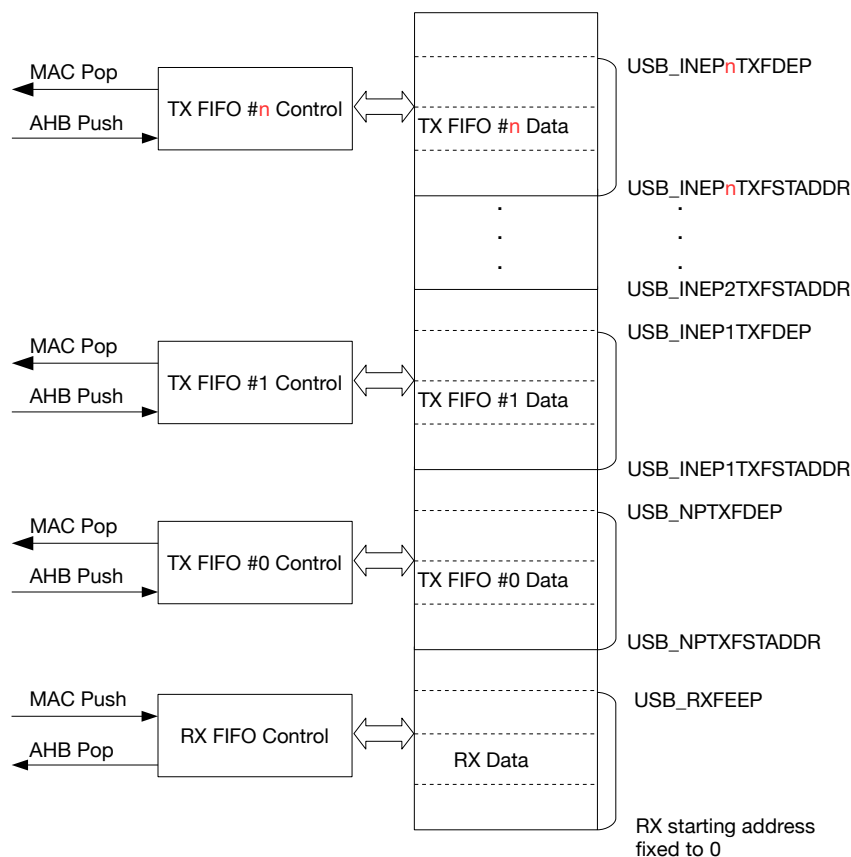


Figure 45.4-4. Device Mode FIFOs

- **RX FIFO:** Stores data payloads received in Data packet, and status entries used to indicate size of those data payloads.
- **Dedicated TX FIFO:** Each active IN endpoint will have a dedicated TX FIFO used to store all IN data payloads of that endpoint, regardless of the transaction type, both periodic and non-periodic IN transactions.

Due to the dedicated FIFOs, Device mode does not use any request queues. Instead, the order of IN transactions are determined by the Host.

#### 45.4.4 Interrupt Hierarchy

OTG\_FS provides a single interrupt line which can be routed via the interrupt matrix to one of the CPUs. The interrupt signal can be unmasked by setting USB\_GLBLINTRMSK. The OTG\_FS interrupt is an OR of all bits in the USB\_GINTSTS\_REG register, and the bits in USB\_GINTSTS\_REG can be unmasked by setting the corresponding bits in the USB\_GINTMSK\_REG register. USB\_GINTSTS\_REG contains system level interrupts, and also specific bits for Host or Device mode interrupts, and OTG specific interrupts. OTG\_FS interrupt sources are organized as Figure 45.4-5 shows.

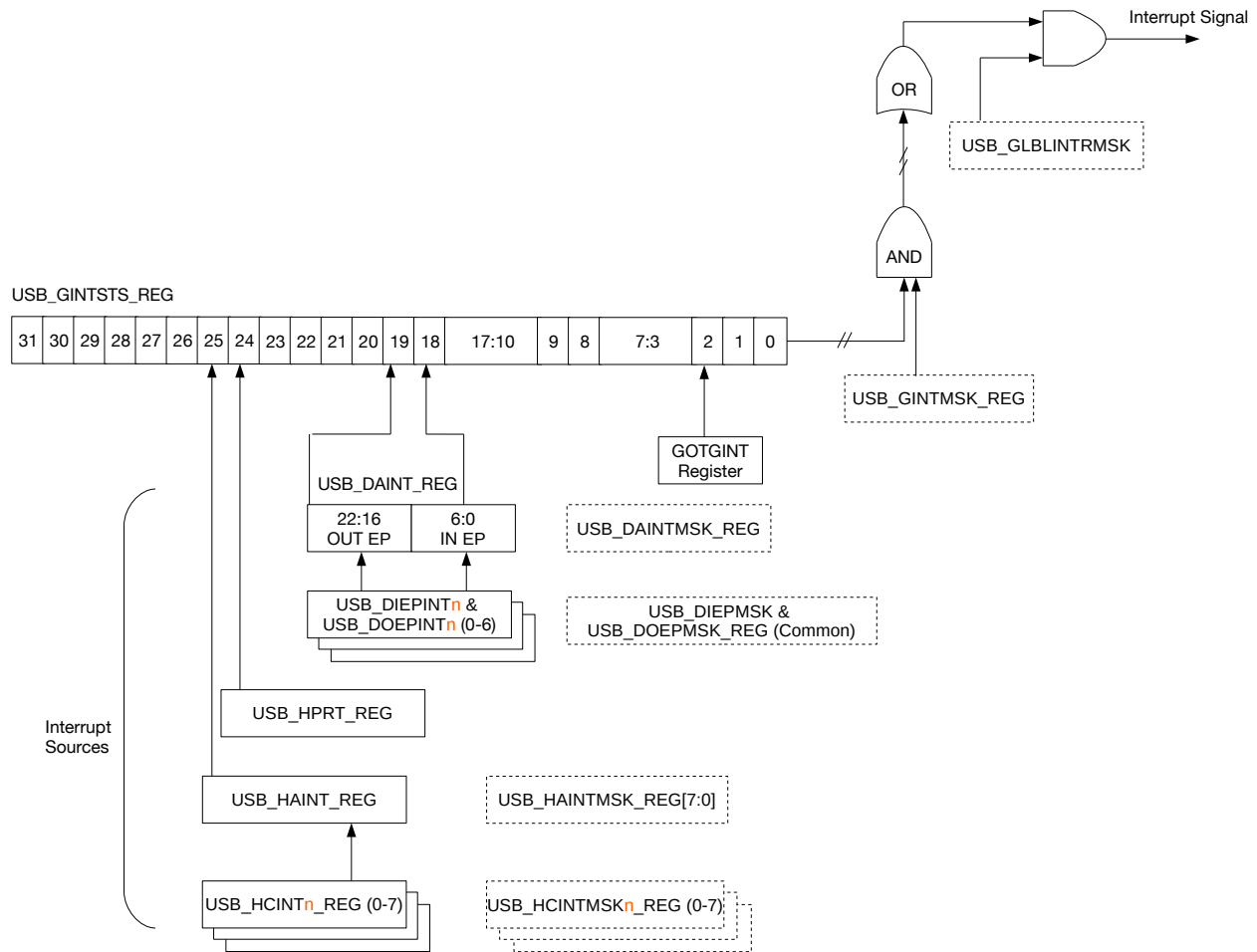


Figure 45.4-5. OTG\_FS Interrupt Hierarchy

The following bits of the **USB\_GINTSTS\_REG** register indicate an interrupt source lower in the hierarchy:

- **USB\_PRTINT** indicates that the Host port has a pending interrupt. The **USB\_HPRT\_REG** register indicates the interrupt source.
- **USB\_HCHINT** indicates that one or more Host channels have a pending interrupt. Read the **USB\_HAINT\_REG** register to determine which channel(s) have a pending interrupt, then read the pending channel's **USB\_HCINT<sub>n</sub>\_REG** register to determine the interrupt source.
- **USB\_OEPINT** indicates that one or more OUT endpoints have a pending interrupt. Read the **USB\_DAINTEG** register to determine which OUT endpoint(s) have a pending interrupt, then read the **USB\_DOEPINT<sub>n</sub>\_REG** register to determine the interrupt source.
- **USB\_IEPINT** indicates that one or more IN endpoints have a pending interrupt. Read the **USB\_DAINTEG** register to determine which IN endpoint(s) are pending, then read the pending IN endpoint's **USB\_DIEPINT<sub>n</sub>\_REG** register to determine the interrupt source.
- **USB\_OTGINT** indicates an On-The-Go event has triggered an interrupt. Read the **USB\_GOTGINT\_REG** register to determine which OTG event(s) triggered the interrupt.

## 45.4.5 Slave Mode and DMA Modes

OTG\_FS supports three ways to access memory: Slave mode, Buffer DMA mode, and Scatter/Gather DMA mode.

### 45.4.5.1 Slave Mode

In Slave mode, all data payloads must be pushed/popped to and from the FIFOs by the CPU.

- When transmitting a packet using IN endpoints or OUT channels, the data payload must be pushed into the corresponding endpoint or channel's TX FIFO.
- When receiving a packet, the packet's status entry must first be popped off the RX FIFO by reading USB\_GRXSTSP\_REG. The status entry should be used to determine the length of the packet's payload (in bytes). The corresponding number of bytes must then be manually popped off the RX FIFO by CPU reading from the RX FIFO's memory region.

### 45.4.5.2 Buffer DMA Mode

Buffer DMA mode is similar to Slave mode but utilizes the internal DMA to push and pop data payloads to the FIFOs.

- When transmitting a packet using IN endpoints or OUT channels, the data payload's address in memory should be written to USB\_HCDMA $n$ \_REG in Host mode or USB\_DIEPDMA $n$ \_REG in Device mode. When the endpoint or channel is enabled, the internal DMA will push the data payload from memory into the TX FIFO of the channel or endpoint.
- When receiving a packet using OUT endpoints or IN channels, the address of an empty buffer in memory should be written to USB\_HCDMA $n$ \_REG in Host mode or USB\_DOEPDMA $n$ \_REG in Device mode. When the endpoint or channel is enabled, the internal DMA will pop the data payload from RX FIFO into the buffer.

### 45.4.5.3 Scatter/Gather DMA Mode

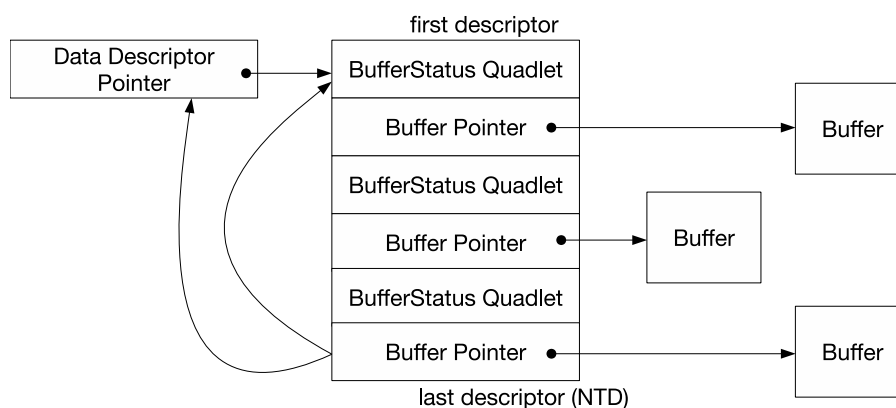


Figure 45.4-6. Scatter/Gather DMA Descriptor List

In Scatter/Gather DMA mode, buffers containing data payloads can be scattered throughout memory. Each endpoint or channel will have a contiguous DMA descriptor list, where each descriptor contains a 32-bit



pointer to the data payload or buffer and a 32-bit buffer descriptor (BufferStatus Quadlet). The data payloads and buffers can correspond to a single transaction (i.e., < 1 MPS bytes) or an entire transfer (> 1 MPS bytes). MPS: maximum packet size. The list is implemented as a ring buffer meaning that the DMA will return to the first entry when it encounters the last entry on the list.

- When transmitting a transfer/transaction using IN endpoints or OUT channels, the DMA will gather the data payloads from the multiple buffers and push them into a TX FIFO.
- When receiving a transfer/transaction using OUT endpoints or IN channels, the DMA will pop the received data payloads from the RX FIFO and scatter them to the multiple buffers pointed to by the DMA list entries.

## 45.4.6 Transaction and Transfer Level Operation

In either Host or Device mode, communication can operate either at the transaction level or the transfer level.

### 45.4.6.1 Transaction and Transfer Level Operation in DMA Mode

When operating at the transaction level in DMA mode, the transfer size is set to the size of one data packet, either a maximum packet size or a short packet size.

When operating at the transfer level in DMA Host mode, software is interrupted only when a channel has been halted. Channels are halted when their programmed transfer size has completed successfully, has received a STALL, or if there are excessive transaction errors, e.g., 3 consecutive transaction errors. In DMA Device mode, all errors are handled by the controller core itself.

### 45.4.6.2 Transaction and Transfer Level Operation in Slave Mode

When operating at the transaction level in Slave Mode, transfers are handled one transaction at a time. Each data payload should correspond to a single data packet, and software must determine whether a retry of the transaction is necessary based on the handshake response received on the USB, e.g., ACK or NAK.

The following table describes transaction level operation in Slave mode for both IN and OUT transactions.

Table 45.4-1. IN and OUT Transactions in Slave Mode

| Host Mode        | Device Mode |
|------------------|-------------|
| OUT Transactions |             |

| Host Mode  | Device Mode   |
|--|---|
| <ol style="list-style-type: none"> <li>1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_HCTSIZ<sub>n</sub>_REG register, enables the channel, then copies the packet's data payload into the TX FIFO.</li> <li>2. When the last DWORD of the data payload has been pushed, the controller core will automatically write a request into the appropriate request queue.</li> <li>3. If the transaction is successful, the USB_XFERCOMPL interrupt will be generated. If the transaction is unsuccessful, an error interrupt, e.g. USB_H_NACK<sub>n</sub> will occur.</li> </ol> | <ol style="list-style-type: none"> <li>1. Software specifies the expected size of the data packet (1 MPS) and the number of data packets (1 data packet) in the USB_DOEPSIZ<sub>n</sub>_REG. Once the endpoint is enabled, it will wait for the host to transmit a packet to it.</li> <li>2. The received packet will be pushed into the RX FIFO along with a packet status entry.</li> <li>3. If the transaction is unsuccessful, e.g., due to a full RX FIFO, the endpoint will automatically NAK the incoming packet.</li> </ol> |
| IN Transactions  |   |
| <ol style="list-style-type: none"> <li>1. Software specifies the expected size of the data packet and the number of packets (1 data packet) in the USB_HCTSIZ<sub>n</sub>_REG register, then enables the channel.</li> <li>2. The controller core will automatically write a request into the appropriate request queue.</li> <li>3. If the transaction is successful, the received data along with a status entry should be written to the RX FIFO. If the transaction is unsuccessful, an error interrupt, e.g., USB_H_NACK<sub>n</sub> will occur.</li> </ol>   | <ol style="list-style-type: none"> <li>1. Software specifies the size of the data packet and the number of data packets (1 data packet) in the USB_DIEPTSIZ<sub>n</sub>_REG register. Once the endpoint is enabled, it will wait for the host to read the packet.</li> <li>2. When the packet has been transmitted, the USB_XFERCOMPL interrupt will be generated.</li> </ol>   |

When operating at the transfer level in Slave mode, one or more transaction-level operations can be pipelined thus being analogous to transfer level operation in DMA mode. Within pipelined transactions, multiple packets of the same transfer can be read/written from the FIFOs in single instance, thus preventing the need for interrupting the software on a per-packet basis.

Operating on a transfer level in Slave mode is similar to operating on the transaction-level, except the transfer size and packet count for each transfer in the USB\_HCTSIZ<sub>n</sub>\_REG or USB\_DOEPSIZ<sub>n</sub>\_REG register will need to be set to reflect the entire transfer. After the channel or endpoint is enabled, multiple data packets worth of payloads should be written to or read from the TX or RX FIFOs respectively (given that there is enough space or enough data).

## 45.5 OTG

USB OTG allows OTG devices to act in the USB Host role or the USB Device role. Thus, OTG devices will typically have a Mini-AB or Micro-AB receptacle so that it can receive an A-plug or B-plug. OTG devices will

become either an A-device or a B-device depending on whether an A-plug or a B-plug is connected.

- A-device defaults to the Host role (A-Host) whilst B-device defaults to the Device role (B-Peripheral).
- A-device and B-device may exchange roles by using the Host Negotiation Protocol (HNP), thus becoming A-peripheral and B-Host.
- A-device can turn off Vbus to save power. B-device can then wake up the A-device by requesting it to turn on Vbus and start a new session. This mechanism is called session request protocol (SRP).
- A-device always powers Vbus even if it is an A-peripheral.

OTG devices are able to determine whether they are connected to an A plug or a B plug using the ID pin of the plugs. The ID pin in A-plugs are pulled to ground whilst B-plugs have the ID pin left floating.

### 45.5.1 OTG Interface

The OTG\_FS supports both the Session Request Protocol (SRP) and Host Negotiation Protocol (HNP) of the OTG Revision 1.3 specification. The OTG\_FS controller core interfaces with the internal transceiver using the UTMI+ OTG interface. The UTMI+ OTG interface allows the controller core to manipulate the transceiver for OTG purposes, e.g., enabling/disabling pull-ups and pull-downs in HNP, and also allows the transceiver to indicate OTG related events. If an external transceiver is used instead, the UTMI+ OTG interface signals will be routed to the ESP32-P4's GPIOs instead through GPIO Matrix. Please refer to Chapter [8 GPIO Matrix and IO MUX](#). The UTMI+ OTG interface signals are described in Table 45.5-1.

**Table 45.5-1. UTMI+ OTG Interface**

| Signal Name          | I/O | Description  |
|----------------------|-----|--|
| usb_otg_iddig_in     | I   | Mini A/B Plug Indicator. Indicates whether the connected plug is mini-A or mini-B. Valid only when usb_otg_idpullup is sampled asserted.<br>0: Mini-A connected<br>1: Mini-B connected   |
| usb_otg_avalid_in    | I   | A-Peripheral Session Valid. Indicates if the voltage Vbus is at a valid level for an A-peripheral session. The comparator thresholds are:<br>0: Vbus < 0.8 V<br>1: Vbus = 0.2 V to 2.0 V |
| usb_otg_bvalid_in    | I   | B-Peripheral Session Valid. Indicates if the voltage Vbus is at a valid level for a B-peripheral session. The comparator thresholds are:<br>0: Vbus < 0.8 V<br>1: Vbus = 0.8 V to 4 V    |
| usb_otg_vbusvalid_in | I   | Vbus Valid. Indicates if the voltage Vbus is valid for A/B-device/peripheral operation. The comparator thresholds are:<br>0: Vbus < 4.4 V<br>1: Vbus > 4.75 V                            |
| usb_srp_sessend_in   | I   | B-device Session End. Indicates if the voltage Vbus is below the B-device Session End threshold. The comparator thresholds are:<br>0: Vbus > 0.8 V<br>1: Vbus < 0.2 V                    |

| Signal Name         | I/O | Description  |
|---------------------|-----|--|
| usb_otg_idpullup    | O   | Analog ID input Sample Enable. Enables sampling the analog ID line.<br>0: ID pin sampling disabled<br>1: ID pin sampling enabled   |
| usb_otg_dppulldown  | O   | D+ Pull-down Resistor Enable. Enables the 15 k $\Omega$ pull-down resistor on the D+ line.   |
| usb_otg_dmpulldown  | O   | D- Pull-down Resistor Enable. Enables the 15 k $\Omega$ pull-down resistor on the D- line.   |
| usb_otg_drvvbus     | O   | Drive Vbus. Enables driving Vbus to 5 V.<br>0: Do not drive Vbus<br>1: Drive Vbus  |
| usb_srp_chrgvbus    | O   | Vbus Input Charge Enable. Directs the PHY to charge Vbus.<br>0: Do not charge Vbus through a resistor<br>1: Charge Vbus through a resistor (must be active for at least 30 ms)               |
| usb_srp_dischrgvbus | O   | Vbus Input Discharge Enable. Directs the PHY to discharge Vbus.<br>0: Do not discharge Vbus through a resistor.<br>1: Discharge Vbus through a resistor (must be active for at least 50 ms). |

## 45.5.2 ID Pin Detection

Bit USB\_CONIDSTS in register USB\_GOTGCTL\_REG indicates whether the OTG controller is an A-device (1'b0) or a B-device (1'b1). The USB\_CONIDSTSCHNG interrupt will trigger whenever there is a change to USB\_CONIDSTS, i.e., when a plug is connected or disconnected.

## 45.5.3 Session Request Protocol (SRP)

### 45.5.3.1 A-Device SRP

Figure 45.5-1 illustrates the flow of SRP when the OTG\_FS is acting as an A-device, i.e., default host and the device that powers Vbus.

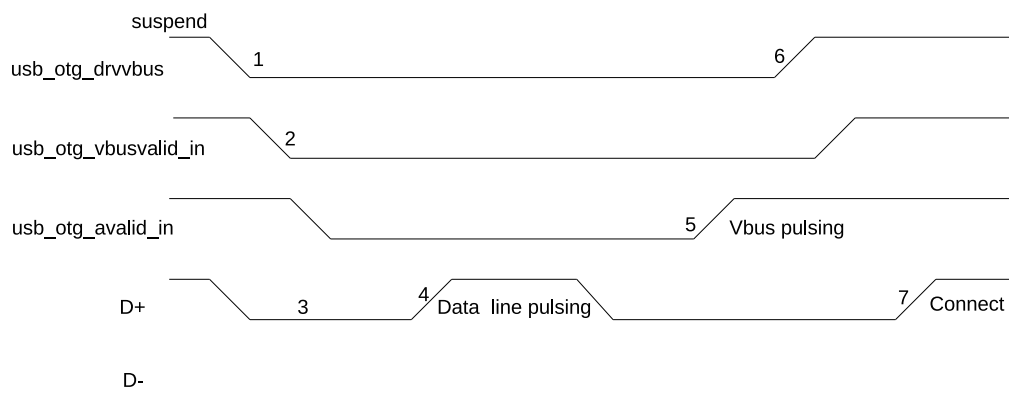


Figure 45.5-1. A-Device SRP

1. To save power, the application suspends and turns off port power when the bus is idle by writing to the Port Suspend (USB\_PRTSUSP to 1'b0) and Port Power (USB\_P RTPWR to 1'b0) bits in the Host Port Control and Status register.

2. PHY indicates port power off by deasserting the `usb_otg_vbusvalid_in` signal.
3. The A-device must detect SEO for at least 2 ms to start SRP when Vbus power is off.
4. To initiate SRP, the B-device turns on its data line pull-up resistor for 5 to 10 ms. The OTG\_FS core detects data-line pulsing.
5. The device drives Vbus above the A-device session valid (2.0 V minimum) for Vbus pulsing. The OTG\_FS core interrupts the application on detecting SRP. The Session Request Detected bit (`USB_SESSREQINT`) is set in Global Interrupt Status register.
6. The application must service the Session Request Detected interrupt and turn on the Port Power bit by writing the Port Power bit in the Host Port Control and Status register. The PHY indicates port power-on by asserting `usb_otg_vbusvalid_in` signal.
7. When the USB is powered, the B-Device connects, completing the SRP process.

### 45.5.3.2 B-Device SRP

Figure 45.5-2 illustrates the flow of SRP when the OTG\_FS is acting as a B-device, i.e., does not power Vbus.

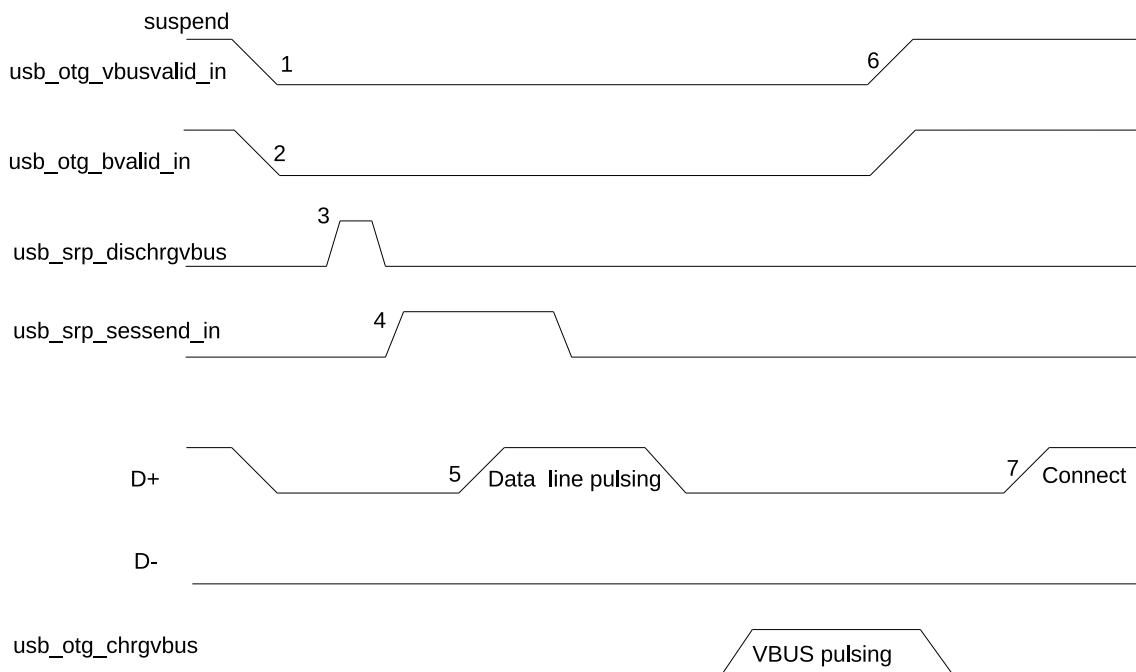


Figure 45.5-2. B-Device SRP

1. To save power, the host (A-device) suspends and turns off port power when the bus is idle. PHY indicates port power off by deasserting the `usb_otg_vbusvalid_in` signal. The OTG\_FS core sets the Early Suspend bit (`USB_ERLYSUSP`) in the Core Interrupt register after detecting 3 ms of bus idleness. Following this, the OTG\_FS core sets the USB Suspend bit (`USB_USBSUSP`) in the Core Interrupt register. PHY indicates the end of the B-device session by deasserting the `usb_otg_bvalid_in` signal.
2. The OTG\_FS core asserts the `usb_otg_dischrgvbus` signal to indicate to the PHY to speed up Vbus discharge.
3. PHY indicates the session's end by asserting the `usb_otg_sessend_in` signal. This is the initial condition

for SRP. The OTG\_FS core requires 2 ms of SEO before initiating SRP. For a USB 2.0 full-speed serial transceiver, the application must wait until Vbus discharges to 0.2 V after USB\_BSESVDL is deasserted.

4. The application waits for 1.5 seconds (TB\_SEO\_SRP time) before initiating SRP by writing the Session Request bit (USB\_SESREQ) in the OTG Control and Status register. The OTG\_FS core performs data-line pulsing followed by Vbus pulsing.
5. The host (A-device) detects SRP from either the data-line or Vbus pulsing, and turns on Vbus. The PHY indicates Vbus power-on by asserting `usb_otg_vbusvalid_in`.
6. The OTG\_FS core performs Vbus pulsing by asserting `usb_srp_chrgvbus`. The host (A-device) starts a new session by turning on Vbus, indicating SRP success. The OTG\_FS core interrupts the application by setting the Session Request Success Status Change bit (USB\_SESREQSC) in the OTG Interrupt Status register. The application reads the Session Request Success bit in the OTG Control and Status register.
7. When the USB is powered, the OTG\_FS core connects, completing the SRP process.

## 45.5.4 Host Negotiation Protocol (HNP)

### 45.5.4.1 A-Device HNP

Figure 45.5-3 illustrates the flow of HNP when the OTG\_FS is acting as an A-device.

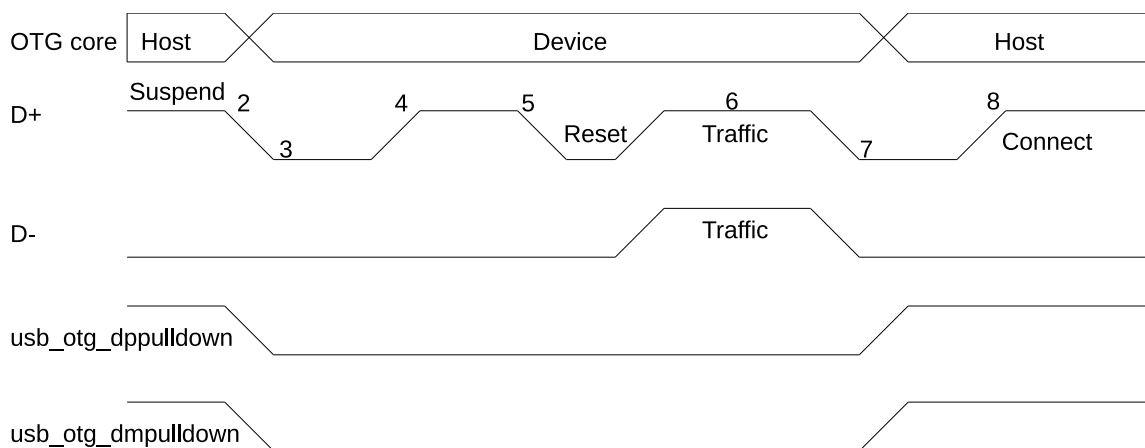


Figure 45.5-3. A-Device HNP

1. The OTG\_FS core sends the B-device a SetFeature `b_hnp_enable` descriptor to enable HNP support. The B-device's ACK response indicates that the B-device supports HNP. The application must set Host Set HNP Enable bit (USB\_HSTSETHNPEN) in the OTG Control and Status register to indicate to the OTG\_FS core that the B-device supports HNP.
2. When it has finished using the bus, the application suspends by writing the Port Suspend bit (USB\_PRTSUSP) in the Host Port Control and Status register.
3. When the B-device observes a USB suspend, it disconnects, indicating the initial condition for HNP. The B-device initiates HNP only when it must switch to the host role; otherwise, the bus continues to be suspended. The OTG\_FS core sets the Host Negotiation Detected interrupt (USB\_HSTNEGDET) in the OTG Interrupt Status register, indicating the start of HNP. The OTG\_FS core deasserts the `usb_otg_dppulldown` and `usb_otg_dmpulldown` signals to indicate a device role. The PHY enables the D+ pull-up resistor, thus indicating a connection for the B-device. The application must read the Current

Mode bit (USB\_CURMOD\_INT) in the OTG Control and Status register to determine Device mode operation.

4. The B-device detects the connection, issues a USB reset, and enumerates the OTG\_FS core for data traffic.
5. The B-device continues the host role, initiating traffic, and suspends the bus when done. The OTG\_FS core sets the Early Suspend bit (USB\_ERLYSUSP) in the Core Interrupt register after detecting 3 ms of bus idleness. Following this, the OTG\_FS core sets the USB Suspend bit (USB\_USBSUSP) in the Core Interrupt register.
6. In Negotiated mode, the OTG\_FS core detects the suspend, disconnects, and switches back to the host role. The OTG\_FS core asserts the usb\_otg\_dppulldown and usb\_otg\_dmpulldown signals to indicate its assumption of the host role.
7. The OTG\_FS core sets the Connector ID Status Change bit (USB\_CONIDSTS) in the OTG Interrupt Status register. The application must read the connector ID status in the OTG Control and Status register to determine the OTG\_FS core's operation as an A-device. This indicates the completion of HNP to the application. The application must read the Current Mode bit (USB\_CURMOD\_INT) in the OTG Control and Status register to determine Host mode operation.
8. The B-device connects, completing the HNP process.

#### 45.5.4.2 B-Device HNP

Figure 45.5-4 illustrates the flow of HNP when the OTG\_FS is acting as a B-device.

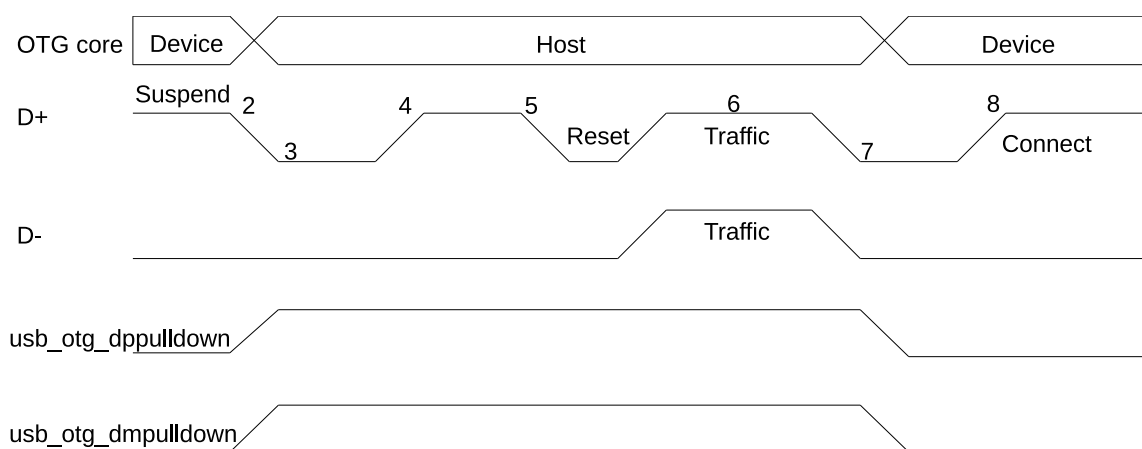


Figure 45.5-4. B-Device HNP

1. The A-device sends the SetFeature b\_hnp\_enable descriptor to enable HNP support. The OTG\_FS core's ACK response indicates that it supports HNP. The application must set the Device HNP Enable bit (USB\_DEVHNPEN) in the OTG Control and Status register to indicate HNP support. The application sets the HNP Request bit (USB\_DEVHNPEN) in the OTG Control and Status register to indicate to the OTG\_FS core to initiate HNP.
2. When A-device has finished using the bus, it suspends the bus.
  - (a) The OTG\_FS core sets the Early Suspend bit (USB\_ERLYSUSP) in the Core Interrupt register after 3 ms of bus idleness. Following this, the OTG\_FS core sets the USB Suspend bit (USB\_USBSUSP) in

- the Core Interrupt register. The OTG\_FS core disconnects and the A-device detects SEO on the bus, indicating HNP.
- (b) The OTG\_FS core asserts the `usb_otg_dppulldown` and `usb_otg_dmpulldown` signals to indicate its assumption of the host role.
  - (c) The A-device responds by activating its D+ pull-up resistor within 3 ms of detecting SEO. The OTG\_FS core detects this as a connect.
  - (d) The OTG\_FS core sets the Host Negotiation Success Status Change interrupt in the OTG Interrupt Status register (`USB_CONIDSTS`), indicating the HNP status. The application must read the Host Negotiation Success bit (`USB_HSTNEGSCS`) in the OTG Control and Status register to determine host negotiation success. The application must read the Current Mode bit (`USB_CURMOD_INT`) in the Core Interrupt register to determine Host mode operation.
3. Program the `USB_PRT_PWR` bit to 1'b1. This drives Vbus on the USB.
  4. Wait for the `USB_PRTCONNDT` interrupt. This indicates that a device is connected to the port.
  5. The application sets the reset bit (`USB_PRT_RST`) and the OTG\_FS core issues a USB reset and enumerates the A-device for data traffic.
  6. Wait for the `USB_PRTENCHNG` interrupt.
  7. The OTG\_FS core continues the host role of initiating traffic, and when done, suspends the bus by writing the Port Suspend bit (`USB_PRT_SUSP`) in the Host Port Control and Status register.
  8. In Negotiated mode, when the A-device detects a suspend, it disconnects and switches back to the host role. The OTG\_FS core deasserts the `usb_otg_dppulldown` and `usb_otg_dmpulldown` signals to indicate the assumption of the device role.
  9. The application must read the Current Mode bit (`USB_CURMOD_INT`) in the Core Interrupt register to determine the Host mode operation.
  10. The OTG\_FS core connects, completing the HNP process.

## 45.6 Registers

The catalog and comprehensive specifications of USB OTG registers are subject to a Non-Disclosure Agreement (NDA) as mandated by the IP provider. To obtain support information for a particular register, please contact Espressif Technical Support Team via [Technical Inquires](#).



## Chapter 46

### USB Serial/JTAG Controller (USB\_SERIAL\_JTAG)

ESP32-P4 contains a USB Serial/JTAG Controller. This unit can be used to program the SoC's flash, read program output, as well as attach a debugger to the running program. All of these are possible for any computer with a USB host (hereafter referred to as 'host') without any active external components.

#### 46.1 Overview

While programming and debugging an ESP32-P4 project using the UART and JTAG functionality is certainly possible, it has a few downsides. First of all, both UART and JTAG take up IO pins and as such, fewer pins are left usable for controlling external signals in software. Additionally, an external chip or adapter is needed for both UART and JTAG to interface with a host computer, which means it will be necessary to integrate these two functionalities in the form of external chips or debugging adapters.

In order to alleviate these issues, ESP32-P4 provides a USB Serial/JTAG Controller, which integrates the functionality of both a USB-to-serial converter as well as a USB-to-JTAG adapter. As this device directly interfaces with an external USB host using only the two data lines required by USB 2.0, only two pins are required to be dedicated to this functionality for debugging ESP32-P4.

#### 46.2 Features

The USB Serial/JTAG controller has the following features:

- USB Full-speed device; Hardwired for CDC-ACM (Communication Device Class - Abstract Control Model) and JTAG adapter functionality
- CDC-ACM:
  - Integrates CDC-ACM adherent serial port emulation (plug-and-play on most modern OSes)
  - Supports host controllable chip reset and entry into download mode
- JTAG adapter functionality:
  - Allows fast communication with CPU debugging core using a compact representation of JTAG instructions
- A control endpoint, a dummy interrupt endpoint, two bulk input endpoints, and two bulk output endpoints; Up to 64-byte data payload size
- Internal PHY: very few or no external components needed to connect to a host computer

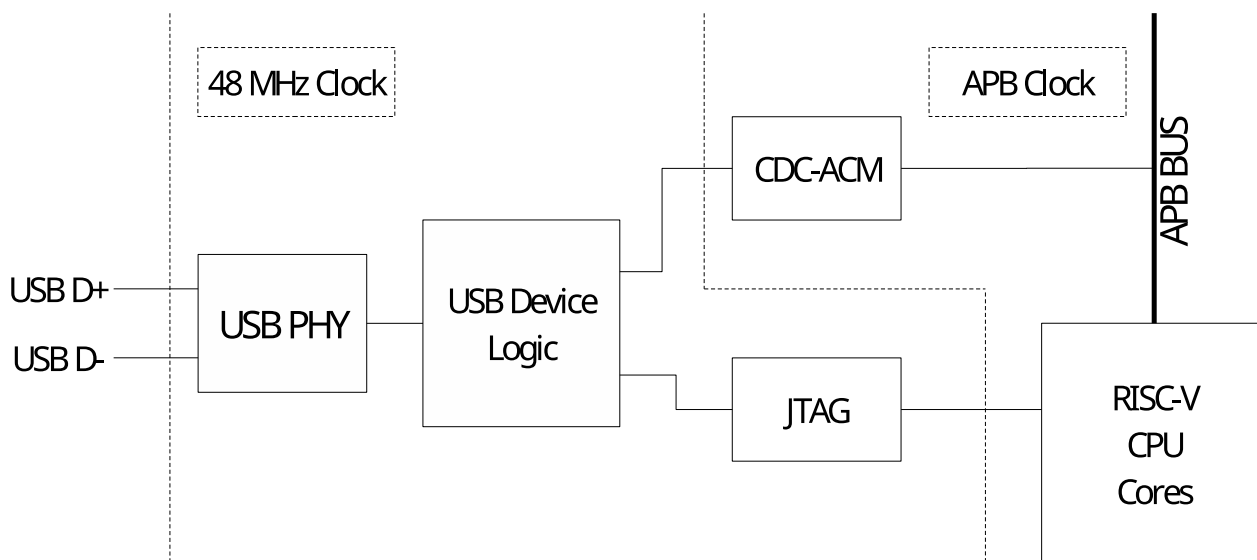


Figure 46.2-1. USB Serial/JTAG High Level Diagram

As shown in Figure 46.2-1, the USB Serial/JTAG controller consists of a USB PHY, a USB device interface, a JTAG command processor, a response capture unit, and the CDC-ACM registers. The PHY and device interface are clocked from a 48 MHz clock derived from the baseband PLL (BBPLL); the software-accessible side of the CDC-ACM block is clocked from APB\_CLK. The JTAG command processor is connected to the JTAG debugging unit of the main processor; the CDC-ACM registers are connected to the APB bus and as such can be read from and written to by software running on the main CPU.

Note that while the USB Serial/JTAG device supports USB 2.0 standard, it only supports Full-speed (12 Mbps) mode but not other modes that the USB 2.0 standard introduced, e.g., the High-speed (480 Mbps) mode.

Figure 46.2-2 shows the internal details of the USB Serial/JTAG controller on the USB side. The USB Serial/JTAG controller consists of a USB 2.0 Full-speed device. It contains a control endpoint, a dummy interrupt endpoint, two bulk input endpoints, and two bulk output endpoints. Together, these form a USB composite device, which consists of a CDC-ACM USB class device as well as a vendor-specific device implementing the JTAG interface. On the SoC side, the JTAG interface is directly connected to the RISC-V CPU's debugging interface, allowing debugging of programs running on that core. Meanwhile, the CDC-ACM device is exposed as a set of registers, allowing a program on the CPU to read and write from it. Additionally, the ROM startup code of the SoC contains code that allows the user to reprogram attached flash memory using this interface.

**Note:**

To get specific information about what endpoint numbers are used for what functionality, please parse the relevant USB descriptors as returned by the device. This guarantees compatibility with other devices with the same functionality but a different implementation.

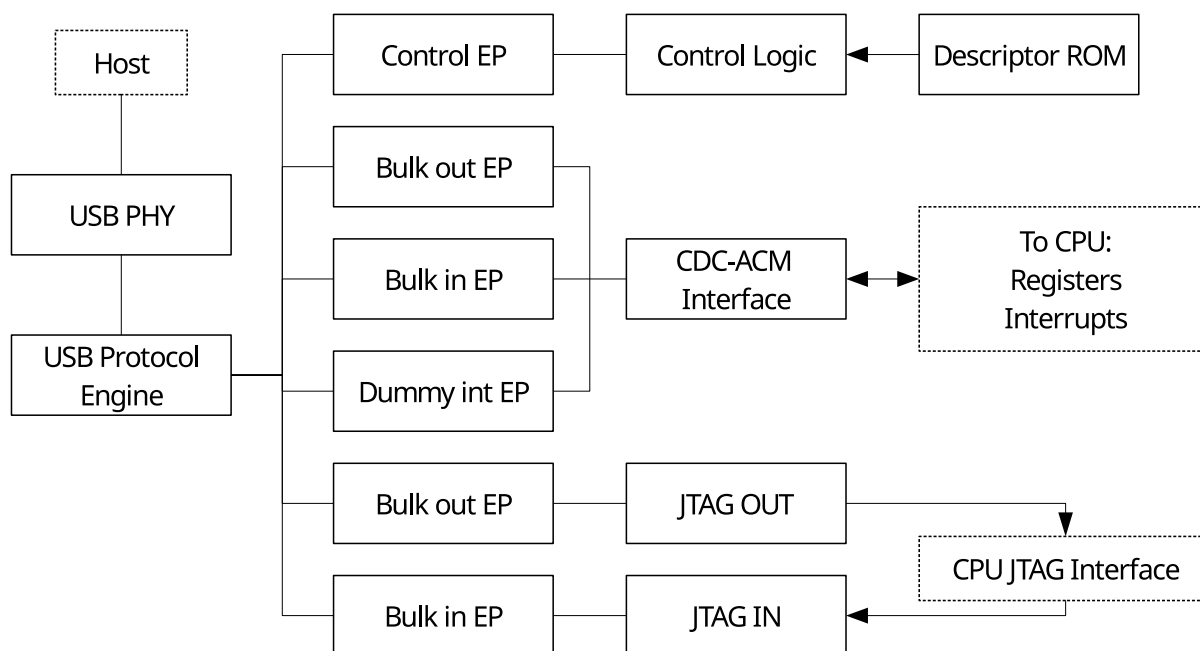


Figure 46.2-2. USB Serial/JTAG Block Diagram

## 46.3 Functional Description

The USB Serial/JTAG controller interfaces with a USB host processor on one side, and with the CPU debugging hardware as well as the software that communicates through the CDC-ACM port on the other side.

### 46.3.1 CDC-ACM USB Interface Functional Description

The CDC-ACM interface adheres to the standard USB CDC-ACM class for serial port emulation. It contains a dummy interrupt endpoint (which will never send any events, as they are not implemented nor needed) and a Bulk IN as well as a Bulk OUT endpoint for the host's received and sent serial data respectively. These endpoints can handle 64-bytes packet at a time, allowing high throughput. As CDC-ACM is a standard USB device class, a host generally can function without any special installation procedures. That is to say, when the USB debugging device is properly connected to a host, the operating system should show a new serial port moments later.

The CDC-ACM interface accepts the following standard CDC-ACM control requests:

Table 46.3-1. Standard CDC-ACM Control Requests

| Command                | Action  |
|------------------------|---|
| SEND_BREAK             | Accepted but ignored (dummy)  |
| SET_LINE_CODING        | Accepted, value sent is readable in software  |
| GET_LINE_CODING        | By default, returns 9600 baud, no parity, 8 data bits, 1 stop bit (Can be changed through software) |
| SET_CONTROL_LINE_STATE | Set the state of the RTS/DTR lines. See Table <a href="#">46.3-2</a>                                |

Aside from general-purpose communication, the CDC-ACM interface can also be used to reset ESP32-P4 and optionally make it enter download mode to flash new firmware. This can be realized by setting the RTS and DTR lines on the virtual serial port.

**Table 46.3-2. CDC-ACM Settings with RTS and DTR**

| RTS | DTR | Action                   |
|-----|-----|--------------------------|
| 0   | 0   | Clear download mode flag |
| 0   | 1   | Set download mode flag   |
| 1   | 0   | Reset ESP32-P4           |
| 1   | 1   | No action                |

Note that if the download mode flag is set when ESP32-P4 is reset, ESP32-P4 will reboot into download mode. When this flag is cleared and the chip is reset, ESP32-P4 will boot from flash. For specific sequences, please refer to Section 46.4. All these functions can also be disabled by programming various eFuses. Please refer to Chapter 7 *eFuse Controller* for more details.

### 46.3.2 CDC-ACM Firmware Interface Functional Description

The CPU can interact with the USB Serial/JTAG controller as the module is connected to the internal APB bus of ESP32-P4. This is mainly used to read and write data from and to the virtual serial port on the attached host.

USB CDC-ACM serial data is sent to and received from the host in packets of 0 to 64 bytes in size. When enough CDC-ACM data has accumulated in the host, the host sends a packet to the CDC-ACM receive endpoint, and the USB Serial/JTAG controller accepts this packet if it has a free buffer. Conversely, the host checks periodically if the USB Serial/JTAG controller has a packet ready to be sent to the host, and if so, receives this packet.

Firmware can get notified of new data from the host in one of the following two ways. First of all, the [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_EP\\_DATA\\_AVAIL](#) bit will remain set as long as there still is unread host data in the buffer. Secondly, the availability of data will trigger the [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#) interrupt. When data is available, it can be read by firmware through repeatedly reading bytes from [USB\\_SERIAL\\_JTAG\\_EP1\\_REG](#). The amount of bytes to read can be determined by checking the [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_EP\\_DATA\\_AVAIL](#) bit after reading each byte to see if there is more data to read. After all data is read, the USB device is automatically readied to receive a new data packet from the host.

When the firmware has data to send, it can put the data in the send buffer and trigger a flush to allow the host to receive the data in a USB packet. In order to do so, there needs to be space available in the send buffer. Firmware can check this by reading [USB\\_REG\\_SERIAL\\_IN\\_EP\\_DATA\\_FREE](#). A 1 in this register field indicates there is still free room in the buffer, and firmware can fill the buffer by writing bytes to the [USB\\_SERIAL\\_JTAG\\_EP1\\_REG](#) register. Writing the buffer does not immediately trigger sending data to the host until the buffer is flushed. After the flush, the entire buffer will be ready to be received by the USB host at once. A flush can be triggered in two ways: 1) after the 64th byte is written to the buffer, the USB hardware will automatically flush the buffer to the host; or 2) firmware can trigger a flush by writing 1 to [USB\\_REG\\_SERIAL\\_WR\\_DONE](#).

Regardless of how a flush is triggered, the send buffer will be unavailable for firmware to write into until it has

been fully read by the host. As soon as the send buffer has been fully read, the [USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#) interrupt will be triggered, indicating that the send buffer can receive another 64 bytes.

It is possible to handle some out-of-band serial requests in software, specifically, the host setting DTR and RTS and changing the line state. If the CDC-ACM interface receives a [SET\\_LINE\\_CODING](#) request, the peripheral can be configured to trigger a [USB\\_SERIAL\\_JTAG\\_SET\\_LINE\\_CODE\\_INT](#) interrupt, at which point the line coding can be read from the [USB\\_SERIAL\\_JTAG\\_SET\\_LINE\\_CODE\\_WO\\_REG](#) register. Similarly, [SET\\_CONTROL\\_LINE\\_STATE](#) requests will trigger [USB\\_SERIAL\\_JTAG\\_RTS\\_CHG\\_INT](#) and [USB\\_SERIAL\\_JTAG\\_DTR\\_CHG\\_INT](#) interrupts if they change the state of these lines. Software can then read the specific state through the [USB\\_SERIAL\\_JTAG\\_RTS](#) and [USB\\_SERIAL\\_JTAG\\_DTR](#) bits. Note that as described earlier, certain RTS/DTR sequences lead to hardware reset of ESP32-P4. Software can disable hardware recognition of these DTR/RTS sequences by setting the [USB\\_SERIAL\\_JTAG\\_USB\\_UART\\_CHIP\\_RST\\_DIS](#) bit, allowing software to interpret these signals freely.

Finally, the host can read the current line state using [GET\\_LINE\\_CODING](#). This event sends back the data in the [USB\\_SERIAL\\_JTAG\\_GET\\_LINE\\_CODE\\_WO\\_REG](#) register and triggers a [USB\\_SERIAL\\_JTAG\\_GET\\_LINE\\_CODE\\_INT](#) interrupt.

### 46.3.3 USB-to-JTAG Interface: JTAG Command Processor

The USB-to-JTAG interface uses a vendor-specific class for its implementation. It consists of two endpoints, one to receive commands and another to send responses. Additionally, some less time-sensitive commands can be given as control requests.

Commands from the host to the JTAG interface are interpreted by the JTAG command processor. Internally, the JTAG command processor implements a full four-wire JTAG bus, consisting of the TCK, TMS and TDI output lines to the RISC-V CPU, as well as the TDO line signalling back from the CPU to the JTAG response capture unit. These signals adhere to the IEEE 1149.1 JTAG standards. Additionally, there is an SRST line to reset ESP32-P4.

Optionally, software can set [USB\\_SERIAL\\_JTAG\\_USB\\_JTAG\\_BRIDGE\\_EN](#) in order to redirect these signals to the GPIO matrix instead, where they can be routed to IO pads on ESP32-P4. This also allows external devices to be debugged via the USB Serial/JTAG peripheral.

The JTAG command processor parses each received nibble (4-bit value) as a command. As USB data is received in 8-bit bytes, this means each byte contains two commands. The USB command processor will execute high-nibble first and low-nibble second. The commands are used to control the TCK, TMS, TDI, and SRST lines of the internal JTAG bus, as well as to signal the JTAG response capture unit the state of the TDO line (which is driven by the CPU debugging logic) that needs to be captured.

In the internal JTAG bus, TCK, TMS, TDI, and TDO are connected directly to the JTAG debugging logic of the RISC-V CPU. SRST is connected to the reset logic of the digital circuitry in ESP32-P4 and a high level on this line will cause a digital system reset. Note that the USB Serial/JTAG controller itself is not affected by SRST.

A nibble can contain the following commands:

**Table 46.3-3. Commands of a Nibble**

| bit       | 3 | 2   | 1   | 0    |
|-----------|---|-----|-----|------|
| CMD_CLK   | 0 | cap | tms | tdi  |
| CMD_RST   | 1 | 0   | 0   | srst |
| CMD_FLUSH | 1 | 0   | 1   | 0    |
| CMD_RSV   | 1 | 0   | 1   | 1    |
| CMD_REP   | 1 | 1   | R1  | R0   |

- CMD\_CLK will set the TDI and TMS as the indicated values and emit one clock pulse on TCK. If the CAP bit is 1, it will instruct the JTAG response capture unit to capture the state of the TDO line. This instruction forms the basis of JTAG communication.
- CMD\_RST will set the state of the SRST line as the indicated value. This can be used to reset ESP32-P4.
- CMD\_FLUSH will instruct the JTAG response capture unit to flush the buffer of all bits it collected so the host is able to read them. Note that in some cases, a JTAG transaction will end in an odd number of commands and as such an odd number of nibbles. In this case, it is allowed to repeat the CMD\_FLUSH command to get an even number of nibbles fitting an integer number of bytes.
- CMD\_RSV is reserved in the current implementation. This command will be ignored when received by ESP32-P4.
- CMD\_REP repeats the last (non-CMD\_REP) command for a certain number of times. The purpose is to compress command streams which repeat the CMD\_CLK instruction for multiple times. A command such as CMD\_CLK can be followed by multiple CMD\_REP commands. The number of repetitions done by one CMD\_REP can be expressed as  $repetition\_count = (R1 \times 2 + R0) \times (4^{cmd\_rep\_count})$ , where *cmd\_rep\_count* indicates the number of the CMD\_REP instruction that went directly before it. Note that the CMD\_REP command is only intended to repeat a CMD\_CLK command. Specifically, using it on a CMD\_FLUSH command may lead to an unresponsive USB device, and a USB reset will be required to recover it.

#### 46.3.4 USB-to-JTAG Interface: CMD\_REP Usage Example

Here is a list of commands as an illustration of the usage of CMD\_REP. Note that each command is a nibble, and in this example, the bitwise command stream would be 0x0D 0x5E 0xCF.

1. 0x0 (CMD\_CLK: cap=0, tdi=0, tms=0)
2. 0xD (CMD\_REP: R1=0, R0=1)
3. 0x5 (CMD\_CLK: cap=1, tdi=0, tms=1)
4. 0xE (CMD\_REP: R1=1, R0=0)
5. 0xC (CMD\_REP: R1=0, R0=0)
6. 0xF (CMD\_REP: R1=1, R0=1)

The following shows what happens at every step:

1. TCK is clocked with the TDI and TMS lines set to 0. No data is captured.
2. TCK is clocked another  $(0 \times 2 + 1) \times (4^0) = 1$  time with the same settings as step 1.

3. TCK is clocked with the TDI line set to 0 and TMS set to 1. Data on the TDO line is captured.
4. TCK is clocked another  $(1 \times 2 + 0) \times (4^0) = 2$  times with the same settings as step 3.
5. Nothing happens:  $(0 \times 2 + 0) \times (4^1) = 0$ . Note that this increases cmd\_rep\_count in the next step.
6. TCK is clocked another  $(1 \times 2 + 1) \times (4^2) = 48$  times with the same settings as step 3.

In other words, this example stream has the same net effect as that of executing command 1 twice, then repeating command 3 for 51 times.

### 46.3.5 USB-to-JTAG Interface: Response Capture Unit

The response capture unit reads the TDO line of the internal JTAG bus and captures its value when the command parser executes a CMD\_CLK with cap=1. It puts this bit into an internal shift register, and writes a byte into the USB buffer when 8 bits have been collected. Of these 8 bits, the least significant one is the one that is read from TDO the earliest.

As soon as either 64 bytes (512 bits) have been collected or a CMD\_FLUSH command is executed, the response capture unit will make the buffer available for the host to receive. Note that the interface to the USB logic is double-buffered. Therefore, as long as the USB throughput is sufficient, the response capture unit can always receive more data. That is to say, while one of the buffers is waiting to be sent to the host, the other can receive more data. When the host has received data from its buffer and the response capture unit flushes its buffer, the two buffers exchange position.

This also means that a command stream can cause at most 128 bytes of capture data generated (less if there are flush commands in the stream) without the host acting to receive the generated data. If more data is generated anyway, the command stream will pause and the device will not accept more commands until the generated capture data is read out.

Note that in general, the logic of the response capture unit tries not to send zero-byte responses. For instance, sending a series of CMD\_FLUSH commands will not cause a series of 0-byte USB responses to be sent. However, in the current implementation, some zero-0 responses may be generated in extraordinary circumstances. It is recommended to ignore these responses.

### 46.3.6 USB-to-JTAG Interface: Control Transfer Requests

Aside from the command processor and the response capture unit, the USB-to-JTAG interface also understands some control requests, as documented in the table below:

**Table 46.3-4. USB-to-JTAG Control Requests**

| bmRequestType | bRequest             | wValue    | wIndex    | wLength | Data            |
|---------------|----------------------|-----------|-----------|---------|-----------------|
| 01000000b     | 0 (VEND_JTAG_SETDIV) | [divider] | interface | 0       | None            |
| 01000000b     | 1 (VEND_JTAG_SETIO)  | [iobits]  | interface | 0       | None            |
| 11000000b     | 2 (VEND_JTAG_GETTDO) | 0         | interface | 1       | [iostate]       |
| 10000000b     | 6 (GET_DESCRIPTOR)   | 0x2000    | 0         | 256     | [jtag cap desc] |

- VEND\_JTAG\_SETDIV sets the divider used. This directly affects the duration of a TCK clock pulse. The TCK clock pulses are derived from a base clock of 48 MHz, which is divided down using an internal

divider. This control request allows the host to set this divider. Note that on startup, the divider is set to 2, which means the TCK clock rate will generally be 24 MHz.

- `VEND_JTAG_SETIO` can bypass the JTAG command processor to set the internal TDI, TDO, TMS, and SRST lines to given values. These values are encoded in the `wValue` field in the format of 11'b0, `srst`, `trst`, `tck`, `tms`, `tdi`.
- `VEND_JTAG_GETTDO` can bypass the JTAG response capture unit to read the internal TDO signal directly. This request returns one byte of data, of which the least significant bit represents the status of the TDO line.
- `GET_DESCRIPTOR` is a standard USB request. However, it can also be used with a vendor-specific `wValue` of 0x2000 to get the JTAG capabilities descriptor. This returns a certain amount of bytes representing the following fixed structure, which describes the capabilities of the USB-to-JTAG adapter (as shown in Table 46.3-5). This structure allows host software to automatically support future revisions of the hardware without the need for an update.

The JTAG capability descriptors of ESP32-P4 are as follows. Note that all 16-bit values are little-endian.

**Table 46.3-5. JTAG Capability Descriptors**

| Byte  | Value | Description   |
|-------|-------|---|
| 0     | 1     | JTAG protocol capability structure version  |
| 1     | 10    | Total length of JTAG protocol capabilities  |
| 2     | 1     | Type of this struct: 1 for speed capability struct  |
| 3     | 8     | Length of this speed capabilities struct  |
| 4 ~ 5 | 4800  | JTAG base clock speed in 10 kHz increments. Note that the maximum TCK speed is half of this value |
| 6 ~ 7 | 1     | Minimum divider value settable by the <code>VEND_JTAG_SETDIV</code> request                       |
| 8 ~ 9 | 255   | Maximum divider value settable by the <code>VEND_JTAG_SETDIV</code> request                       |

## 46.4 Recommended Operation

Little setup is needed for using the USB Serial/JTAG device. The USB-to-JTAG hardware itself does not need any setup aside from the standard USB initialization that the host operating system already does. Apart from that, the CDC-ACM emulation on the host side is also plug-and-play.

On the firmware side, very little initialization is needed either. The USB hardware is self-initialized and after boot-up, if a host is connected and listening on the CDC-ACM interface, data can be exchanged as described above without any specific setup except for the situation when the firmware optionally sets up an interrupt service handler.

One thing to note is that there may be situations where either the host is not attached or the CDC-ACM virtual port is not opened. In such cases, the packets that are flushed to the host will never be picked up and the send buffer will never be empty. It is important to detect these situations and implement timeout, as this is the only way to reliably detect whether the port on the host side is closed or not.

Another thing to note is that the USB device is dependent on the BBPLL for the 48 MHz USB PHY clock. If this PLL is disabled, the USB communication will cease to function.



One scenario where this happens is Deep-sleep. The USB Serial/JTAG controller (as well as the attached RISC-V CPU) will be entirely powered down in Deep-sleep mode. If a device needs to be debugged in this mode, it may be preferable to use an external JTAG debugger and a serial interface instead.

The CDC-ACM interface can also be used to reset the SoC and take it into or out of download mode. Generating the correct sequence of handshake signals can be a bit complicated, since most operating systems only allow setting or resetting DTR and RTS separately, but not in tandem. Additionally, some drivers (e.g., the standard CDC-ACM driver on Windows) do not set DTR until RTS is set and the user needs to explicitly set RTS in order to 'propagate' the DTR value. The recommended procedures are introduced below.

To reset the SoC into download mode:

**Table 46.4-1. Reset SoC into Download Mode**

| Action    | Internal state | Note                       |
|-----------|----------------|----------------------------|
| Clear DTR | RTS=?, DTR=0   | Initialize to known values |
| Clear RTS | RTS=0, DTR=0   | -                          |
| Set DTR   | RTS=0, DTR=1   | Set download mode flag     |
| Clear RTS | RTS=0, DTR=1   | Propagate DTR              |
| Set RTS   | RTS=1, DTR=1   | -                          |
| Clear DTR | RTS=1, DTR=0   | Reset SoC                  |
| Set RTS   | RTS=1, DTR=0   | Propagate DTR              |
| Clear RTS | RTS=0, DTR=0   | Clear download flag        |

To reset the SoC into booting from flash:

**Table 46.4-2. Reset SoC into Booting from flash**

| Action    | Internal state | Note                |
|-----------|----------------|---------------------|
| Clear DTR | RTS=?, DTR=0   | -                   |
| Clear RTS | RTS=0, DTR=0   | Clear download flag |
| Set RTS   | RTS=1, DTR=0   | Reset SoC           |
| Clear RTS | RTS=0, DTR=0   | Exit reset          |

## 46.5 Interrupts

ESP32-P4's USB Serial/JTAG Controller can generate the USB\_SERIAL\_JTAG\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#). There are several internal interrupt sources from the USB Serial/JTAG Controller that can generate this interrupt signal.

- USB\_SERIAL\_JTAG\_JTAG\_IN\_FLUSH\_INT: triggered when flush cmd is received for the JTAG bulk out endpoint.
- USB\_SERIAL\_JTAG\_SOF\_INT: triggered when SOF frame is received.
- USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT: triggered when Serial Port OUT Endpoint receives one packet.

- USB\_SERIAL\_JTAG\_SERIAL\_IN\_EMPTY\_INT: triggered when Serial Port IN Endpoint is empty.
- USB\_SERIAL\_JTAG\_PID\_ERR\_INT: triggered when PID error is detected.
- USB\_SERIAL\_JTAG\_CRC5\_ERR\_INT: triggered when CRC5 error is detected.
- USB\_SERIAL\_JTAG\_CRC16\_ERR\_INT: triggered when CRC16 error is detected.
- USB\_SERIAL\_JTAG\_STUFF\_ERR\_INT: triggered when a bit stuffing error is detected.
- USB\_SERIAL\_JTAG\_IN\_TOKEN\_REC\_IN\_EP1\_INT: triggered when IN token for IN endpoint 1 is received.
- USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_INT: triggered when USB bus reset is detected.
- USB\_SERIAL\_JTAG\_OUT\_EP1\_ZERO\_PAYLOAD\_INT: triggered when OUT endpoint 1 receives packet with zero payload.
- USB\_SERIAL\_JTAG\_OUT\_EP2\_ZERO\_PAYLOAD\_INT: triggered when OUT endpoint 2 receives packet with zero payload.
- USB\_SERIAL\_JTAG\_RTS\_CHG\_INT: triggered when level of RTS from USB serial channel is changed.
- USB\_SERIAL\_JTAG\_DTR\_CHG\_INT: triggered when level of DTR from USB serial channel is changed.
- USB\_SERIAL\_JTAG\_GET\_LINE\_CODE\_INT: triggered when level of GET LINE CODING request is received.
- USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_INT: triggered when level of SET LINE CODING request is received.

## 46.6 Register Summary

The addresses in this section are relative to USB Serial/JTAG controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name   | Description   | Address | Access   |
|--|---|---------|----------|
| <b>Configuration Registers</b>                       |   |         |          |
| <a href="#">USB_SERIAL_JTAG_EP1_REG</a>              | FIFO access for the CDC-ACM data IN and OUT endpoints     | 0x0000  | R/W      |
| <a href="#">USB_SERIAL_JTAG_EP1_CONF_REG</a>         | Configuration and control registers for the CDC-ACM FIFOs | 0x0004  | varies   |
| <a href="#">USB_SERIAL_JTAG_CONFO_REG</a>            | PHY hardware configuration                                | 0x0018  | R/W      |
| <a href="#">USB_SERIAL_JTAG_TEST_REG</a>             | Registers used for debugging the PHY                      | 0x001C  | varies   |
| <a href="#">USB_SERIAL_JTAG_MISC_CONF_REG</a>        | Clock enable control                                      | 0x0044  | R/W      |
| <a href="#">USB_SERIAL_JTAG_MEM_CONF_REG</a>         | Memory power control                                      | 0x0048  | R/W      |
| <a href="#">USB_SERIAL_JTAG_CHIP_RST_REG</a>         | CDC-ACM chip reset control                                | 0x004C  | varies   |
| <a href="#">USB_SERIAL_JTAG_GET_LINE_CODE_W0_REG</a> | W0 of GET_LINE_CODING command                             | 0x0058  | R/W      |
| <a href="#">USB_SERIAL_JTAG_GET_LINE_CODE_W1_REG</a> | W1 of GET_LINE_CODING command                             | 0x005C  | R/W      |
| <a href="#">USB_SERIAL_JTAG_CONFIG_UPDATE_REG</a>    | Configuration registers' value update                     | 0x0060  | WT       |
| <a href="#">USB_SERIAL_JTAG_SER_AFIFO_CONFIG_REG</a> | Serial AFIFO configure register                           | 0x0064  | varies   |
| <b>Interrupt Registers</b>                           |   |         |          |
| <a href="#">USB_SERIAL_JTAG_INT_RAW_REG</a>          | Interrupt raw status register                             | 0x0008  | R/WTC/SS |
| <a href="#">USB_SERIAL_JTAG_INT_ST_REG</a>           | Interrupt status register                                 | 0x000C  | RO       |
| <a href="#">USB_SERIAL_JTAG_INT_ENA_REG</a>          | Interrupt enable status register                          | 0x0010  | R/W      |
| <a href="#">USB_SERIAL_JTAG_INT_CLR_REG</a>          | Interrupt clear status register                           | 0x0014  | WT       |
| <b>Status Registers</b>                              |   |         |          |
| <a href="#">USB_SERIAL_JTAG_JFIFO_ST_REG</a>         | JTAG FIFO status and control registers                    | 0x0020  | varies   |
| <a href="#">USB_SERIAL_JTAG_FRAM_NUM_REG</a>         | Last received SOF frame index register                    | 0x0024  | RO       |
| <a href="#">USB_SERIAL_JTAG_IN_EPO_ST_REG</a>        | Control IN endpoint status information                    | 0x0028  | RO       |
| <a href="#">USB_SERIAL_JTAG_IN_EP1_ST_REG</a>        | CDC-ACM IN endpoint status information                    | 0x002C  | RO       |
| <a href="#">USB_SERIAL_JTAG_IN_EP2_ST_REG</a>        | CDC-ACM interrupt IN endpoint status information          | 0x0030  | RO       |
| <a href="#">USB_SERIAL_JTAG_IN_EP3_ST_REG</a>        | JTAG IN endpoint status information                       | 0x0034  | RO       |
| <a href="#">USB_SERIAL_JTAG_OUT_EPO_ST_REG</a>       | Control OUT endpoint status information                   | 0x0038  | RO       |
| <a href="#">USB_SERIAL_JTAG_OUT_EP1_ST_REG</a>       | CDC-ACM OUT endpoint status information                   | 0x003C  | RO       |
| <a href="#">USB_SERIAL_JTAG_OUT_EP2_ST_REG</a>       | JTAG OUT endpoint status information                      | 0x0040  | RO       |

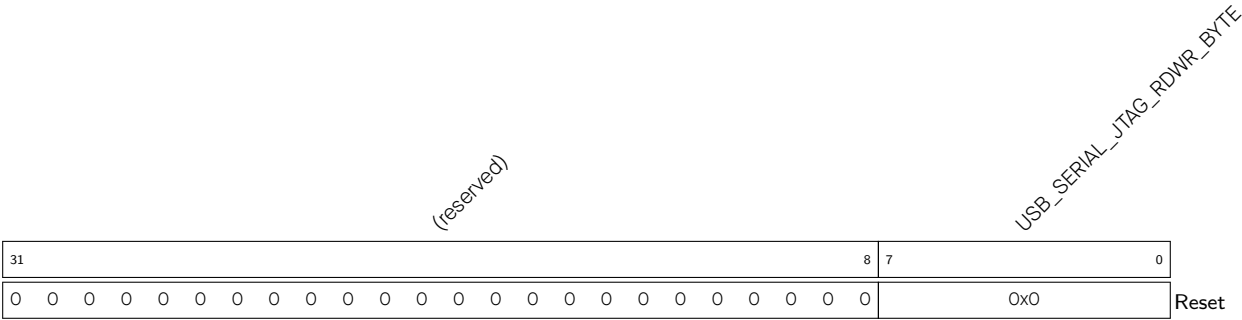
| Name   | Description                   | Address | Access |
|--|-------------------------------|---------|--------|
| <a href="#">USB_SERIAL_JTAG_SET_LINE_CODE_W0_REG</a> | W0 of SET_LINE_CODING command | 0x0050  | RO     |
| <a href="#">USB_SERIAL_JTAG_SET_LINE_CODE_W1_REG</a> | W1 of SET_LINE_CODING command | 0x0054  | RO     |
| <a href="#">USB_SERIAL_JTAG_BUS_RESET_ST_REG</a>     | USB Bus reset status register | 0x0068  | RO     |
| <b>Version Registers</b>                             |                               |         |        |
| <a href="#">USB_SERIAL_JTAG_DATE_REG</a>             | Date register                 | 0x0088  | R/W    |

## 46.7 Registers

The addresses in this section are relative to USB Serial/JTAG controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

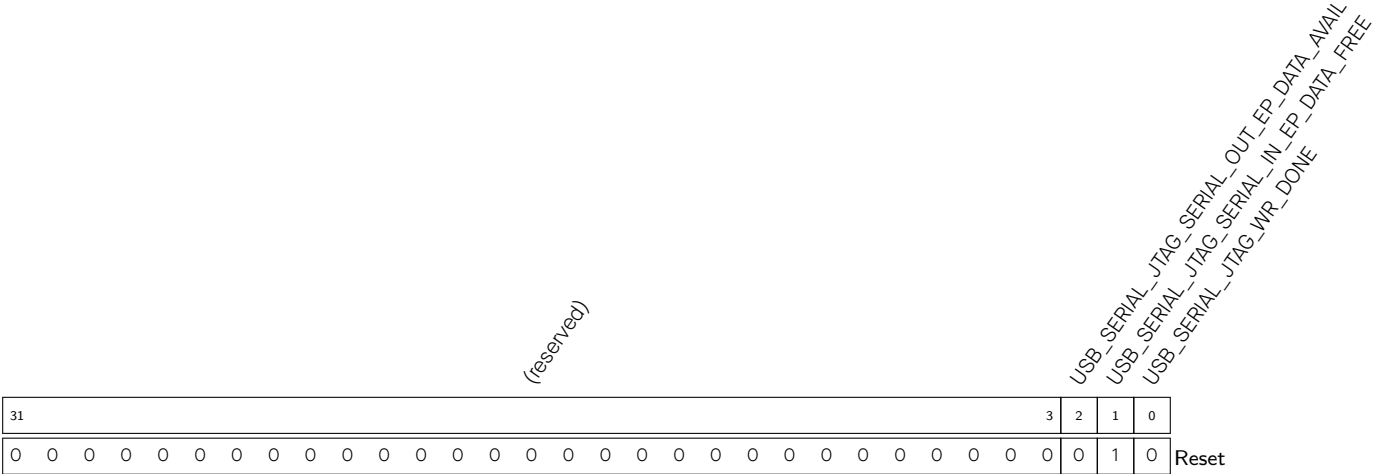
For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 46.1. USB\_SERIAL\_JTAG\_EP1\_REG (0x0000)



**USB\_SERIAL\_JTAG\_RDWR\_BYTE** A write to this register pushes the written data into the CDC TX FIFO; a read from this register pops a byte from the CDC RX FIFO and returns it.  
When [USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#) is set, users can write data (up to 64 bytes) into CDC-ACM TX FIFO through this register.  
When [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#) is set, users can check how many data is received through [USB\\_SERIAL\\_JTAG\\_OUT\\_EP1\\_WR\\_ADDR](#), then read data from CDC-ACM RX FIFO through this register.  
(R/W)

Register 46.2. USB\_SERIAL\_JTAG\_EP1\_CONF\_REG (0x0004)



**USB\_SERIAL\_JTAG\_WR\_DONE** Configures whether to represent writing byte data to CDC-ACM TX FIFO is done.

0: No effect

1: Represents writing byte data to CDC-ACM TX FIFO is done

This bit then stays 0 until data in CDC-ACM TX FIFO is read by the USB Host.

(WT)

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_EP\_DATA\_FREE** Represents whether CDC-ACM TX FIFO has space available.

0: CDC-ACM TX FIFO is full and no data should be written into it

1: CDC-ACM TX FIFO is not full and data can be written into it

After writing [USB\\_SERIAL\\_JTAG\\_WR\\_DONE](#), this bit will be 0 until data in CDC-ACM TX FIFO is read by USB Host.

(RO)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_EP\_DATA\_AVAIL** Represents whether there is data in CDC-ACM RX FIFO.

0: There is no data in CDC-ACM RX FIFO

1: There is data in CDC-ACM RX FIFO

(RO)

**Register 46.3. USB\_SERIAL\_JTAG\_CONFO\_REG (0x0018)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_USB_JTAG_BRIDGE_EN<br>USB_SERIAL_JTAG_USB_PAD_ENABLE<br>USB_SERIAL_JTAG_PULLUP_VALUE<br>USB_SERIAL_JTAG_DM_PULLDOWN<br>USB_SERIAL_JTAG_DP_PULLUP<br>USB_SERIAL_JTAG_DP_PULLDOWN<br>USB_SERIAL_JTAG_PAD_PULLUP<br>USB_SERIAL_JTAG_VREF_OVERRIDE<br>USB_SERIAL_JTAG_VREFL<br>USB_SERIAL_JTAG_VREFH<br>USB_SERIAL_JTAG_EXCHG_PINS<br>USB_SERIAL_JTAG_PHY_SEL |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 1  | 0  | 0  | 0  | 0  | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**USB\_SERIAL\_JTAG\_PHY\_SEL** Configures whether to select internal or external PHY.

0: Internal PHY

1: External PHY

(R/W)

**USB\_SERIAL\_JTAG\_EXCHG\_PINS\_OVERRIDE** Configures whether to enable software control USB

D+ D- exchange.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_EXCHG\_PINS** Configures whether to enable USB D+ D- exchange.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_VREFH** Configures single-end input high threshold.

0: 1.76 V

1: 1.84 V

2: 1.92 V

3: 2.00 V

(R/W)

**USB\_SERIAL\_JTAG\_VREFL** Configures single-end input low threshold.

0: 0.80 V

1: 0.88 V

2: 0.96 V

3: 1.04 V

(R/W)

**USB\_SERIAL\_JTAG\_VREF\_OVERRIDE** Configures whether to enable software control input threshold.

0: Disable

1: Enable

(R/W)

**Continued on the next page...**

**Register 46.3. USB\_SERIAL\_JTAG\_CONFO\_REG (0x0018)**

Continued from the previous page...

**USB\_SERIAL\_JTAG\_PAD\_PULL\_OVERRIDE** Configures whether to enable software to control USB D+ D- pullup and pulldown.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_DP\_PULLUP** Configures whether to enable USB D+ pull up when [USB\\_SERIAL\\_JTAG\\_PAD\\_PULL\\_OVERRIDE](#) is 1.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_DP\_PULLDOWN** Configures whether to enable USB D+ pull down when [USB\\_SERIAL\\_JTAG\\_PAD\\_PULL\\_OVERRIDE](#) is 1.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_DM\_PULLDOWN** Configures whether to enable USB D- pull down when [USB\\_SERIAL\\_JTAG\\_PAD\\_PULL\\_OVERRIDE](#) is 1.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_PULLUP\_VALUE** Configures the pull up value when [USB\\_SERIAL\\_JTAG\\_PAD\\_PULL\\_OVERRIDE](#) is 1.

0: 2.2 K

1: 1.1 K

(R/W)

**USB\_SERIAL\_JTAG\_USB\_PAD\_ENABLE** Configures whether to enable USB pad function.

0: Disable

1: Enable

(R/W)

**USB\_SERIAL\_JTAG\_USB\_JTAG\_BRIDGE\_EN** Configures whether to disconnect USB\_JTAG and internal JTAG.

0: USB\_JTAG is connected to the internal JTAG port of CPU

1: USB\_JTAG and the internal JTAG are disconnected, MTMS, MTDI, and MTCK are output through GPIO Matrix, and MTDO is input through GPIO Matrix

(R/W)



#### Register 46.4. USB\_SERIAL\_JTAG\_TEST\_REG (0x001C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |                            |   |   |   |                            |  |  |  |                             |  |  |  |                            |  |  |  |                            |  |  |  |                             |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|----------------------------|---|---|---|----------------------------|--|--|--|-----------------------------|--|--|--|----------------------------|--|--|--|----------------------------|--|--|--|-----------------------------|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 7 | 6 | 5 | 4     | 3                          | 2 | 1 | 0 |                            |  |  |  |                             |  |  |  |                            |  |  |  |                            |  |  |  |                             |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | Reset |                            |   |   |   |                            |  |  |  |                             |  |  |  |                            |  |  |  |                            |  |  |  |                             |  |  |  |  |  |  |  |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       | USB_SERIAL_JTAG_TEST_RX_DM |   |   |   | USB_SERIAL_JTAG_TEST_RX_DP |  |  |  | USB_SERIAL_JTAG_TEST_RX_RCV |  |  |  | USB_SERIAL_JTAG_TEST_TX_DM |  |  |  | USB_SERIAL_JTAG_TEST_TX_DP |  |  |  | USB_SERIAL_JTAG_TEST_USB_OE |  |  |  |  |  |  |  |

**USB\_SERIAL\_JTAG\_TEST\_ENABLE** Configures whether to enable the test mode of the USB pad.

0: Resume normal operation

1: Enable the test mode of the USB pad

Enabling the test mode of the USB pad allows the USB pad to be controlled/read using the other bits in this register.

(R/W)

**USB\_SERIAL\_JTAG\_TEST\_USB\_OE** Configures whether to enable USB pad output.

0: Set D+ and D- to high impedance

1: Output the values set in `USB_SERIAL_JTAG_TEST_TX_DP` and `USB_SERIAL_JTAG_TEST_TX_DM` on the D+ and D- pins

(R/W)

USB\_SERIAL\_JTAG\_TEST\_TX\_DP Configures value of USB D+ in test mode when  
USB\_SERIAL\_JTAG\_TEST\_USB\_OE is 1. (R/W)

**USB\_SERIAL\_JTAG\_TEST\_TX\_DM** Configures value of USB D- in test mode when [USB\\_SERIAL\\_JTAG\\_TEST\\_USB\\_OE](#) is 1. (R/W)

**USB\_SERIAL\_JTAG\_TEST\_RX\_RCV** Represents the current logical level of the voltage difference between USB D- and USB D+ pads in test mode.

0: USB D- voltage is higher than USB D+

1: USB D+ voltage is higher than USB D-

(RO)

**USB\_SERIAL\_JTAG\_TEST\_RX\_DP** Represents the logical level of the USB D+ pad in test mode.

(RO)

**USB SERIAL JTAG TEST RX DM** Represents the logical level of the USB D- pad in test mode.

(RO)

Register 46.5. USB\_SERIAL\_JTAG\_MISC\_CONF\_REG (0x0044)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_CLK_EN |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                      | 0 |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | Reset |

**USB\_SERIAL\_JTAG\_CLK\_EN** Configures whether to force clock on for register.

0: Support clock only when application writes registers

1: Force clock on for register

(R/W)

Register 46.6. USB\_SERIAL\_JTAG\_MEM\_CONF\_REG (0x0048)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |                            |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|----------------------------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_USB_MEM_CLK_EN |   | USB_SERIAL_JTAG_USB_MEM_PD |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2 | 1                              | 0 |                            |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1                              | 0 | Reset                      |  |

**USB\_SERIAL\_JTAG\_USB\_MEM\_PD** Configures whether to power down USB memory.

0: No effect

1: Power down

(R/W)

**USB\_SERIAL\_JTAG\_USB\_MEM\_CLK\_EN** Configures whether to force clock on for USB memory.

0: No effect

1: Force

(R/W)



**Register 46.9. USB\_SERIAL\_JTAG\_GET\_LINE\_CODE\_W1\_REG (0x005C)**

|            |   |   |   |   |   |   |   |                                  |   |  |  |  |  |  |  |                                  |  |  |  |  |  |  |   |                                |  |  |  |  |  |   |  |   |  |  |  |  |       |  |  |   |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|----------------------------------|---|--|--|--|--|--|--|----------------------------------|--|--|--|--|--|--|---|--------------------------------|--|--|--|--|--|---|--|---|--|--|--|--|-------|--|--|---|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   | USB_SERIAL_JTAG_GET_BCHAR_FORMAT |   |  |  |  |  |  |  | USB_SERIAL_JTAG_GET_BPARITY_TYPE |  |  |  |  |  |  |   | USB_SERIAL_JTAG_GET_BDATA_BITS |  |  |  |  |  |   |  |   |  |  |  |  |       |  |  |   |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   | 24                               |   |  |  |  |  |  |  | 16                               |  |  |  |  |  |  |   | 15                             |  |  |  |  |  |   |  | 8 |  |  |  |  |       |  |  | 7 |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 |  |  |  |  |  |  | 0                                |  |  |  |  |  |  | 0 |                                |  |  |  |  |  | 0 |  |   |  |  |  |  | Reset |  |  |   |  |  |  |  |  |  |  |   |

**USB\_SERIAL\_JTAG\_GET\_BDATA\_BITS** Configures the value of bDataBits set by software, which is requested by GET\_LINE\_CODING command. (R/W)

**USB\_SERIAL\_JTAG\_GET\_BPARITY\_TYPE** Configures the value of bParityType set by software, which is requested by GET\_LINE\_CODING command. (R/W)

**USB\_SERIAL\_JTAG\_GET\_BCHAR\_FORMAT** Configures the value of bCharFormat set by software, which is requested by GET\_LINE\_CODING command. (R/W)

**Register 46.10. USB\_SERIAL\_JTAG\_CONFIG\_UPDATE\_REG (0x0060)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_CONFIG_UPDATE |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                             |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**USB\_SERIAL\_JTAG\_CONFIG\_UPDATE** Configures whether to update the value of configuration registers from APB clock domain to 48 MHz clock domain.

0: No effect

1: Update

(WT)

**Register 46.11. USB\_SERIAL\_JTAG\_SER\_AFIFO\_CONFIG\_REG (0x0064)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_IN_AFIFO_WFULL     |   |   |   |   |   |   |   |   |   |   |       |
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_OUT_AFIFO_EMPTY    |   |   |   |   |   |   |   |   |   |   |       |
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_IN_AFIFO_RESET_RD  |   |   |   |   |   |   |   |   |   |   |       |
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_OUT_AFIFO_RESET_WR |   |   |   |   |   |   |   |   |   |   |       |
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_IN_AFIFO_RESET_RD  |   |   |   |   |   |   |   |   |   |   |       |
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL__JTAG_SERIAL_IN_AFIFO_RESET_WR  |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6  | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | Reset |

USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_WFULL  
 USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_EMPTY  
 USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_RESET\_RD  
 USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_RESET\_WR  
 USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_RESET\_RD  
 USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_RESET\_WR

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_RESET\_WR** Configures whether to reset CDC\_ACM IN async FIFO write clock domain.

0: No effect

1: Reset

(R/W)

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_RESET\_RD** Configures whether to reset CDC\_ACM IN async FIFO read clock domain.

0: No effect

1: Reset

(R/W)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_RESET\_WR** Configures whether to reset CDC\_ACM OUT async FIFO write clock domain.

0: No effect

1: Reset

(R/W)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_RESET\_RD** Configures whether to reset CDC\_ACM OUT async FIFO read clock domain.

0: No effect

1: Reset

(R/W)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_AFIFO\_EMPTY** Represents CDC\_ACM OUT async FIFO empty signal in read clock domain. (RO)

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_AFIFO\_WFULL** Represents CDC\_ACM IN async FIFO full signal in write clock domain. (RO)

Register 46.12. USB\_SERIAL\_JTAG\_INT\_RAW\_REG (0x0008)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_SET_LINE_CODE_INT_RAW<br>USB_SERIAL_JTAG_GET_LINE_CODE_INT_RAW<br>USB_SERIAL_JTAG_DTR_CHG_INT_RAW<br>USB_SERIAL_JTAG_RTS_CHG_INT_RAW<br>USB_SERIAL_JTAG_OUT_EP2_INT_RAW<br>USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_RAW<br>USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_RAW<br>USB_SERIAL_JTAG_USB_BUS_RESET_INT_RAW<br>USB_SERIAL_JTAG_STUFF_ERR_INT_RAW<br>USB_SERIAL_JTAG_CRC16_ERR_INT_RAW<br>USB_SERIAL_JTAG_PID_ERR_INT_RAW<br>USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_RAW<br>USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_RAW<br>USB_SERIAL_JTAG_SOF_INT_RAW<br>USB_SERIAL_JTAG_IN_FLUSH_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | Reset |

**USB\_SERIAL\_JTAG\_JTAG\_IN\_FLUSH\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_JTAG\\_IN\\_FLUSH\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_SOF\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_SOF\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_EMPTY\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_PID\_ERR\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_PID\\_ERR\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_CRC5\_ERR\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_CRC5\\_ERR\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_CRC16\_ERR\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_CRC16\\_ERR\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_STUFF\_ERR\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_STUFF\\_ERR\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_IN\_TOKEN\_REC\_IN\_EP1\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_IN\\_TOKEN\\_REC\\_IN\\_EP1\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_USB\\_BUS\\_RESET\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_OUT\_EP1\_ZERO\_PAYLOAD\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_OUT\\_EP1\\_ZERO\\_PAYLOAD\\_INT](#). (R/WTC/SS)

Continued on the next page...

**Register 46.12. USB\_SERIAL\_JTAG\_INT\_RAW\_REG (0x0008)**

Continued from the previous page...

**USB\_SERIAL\_JTAG\_OUT\_EP2\_ZERO\_PAYLOAD\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_OUT\\_EP2\\_ZERO\\_PAYLOAD\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_RTS\_CHG\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_RTS\\_CHG\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_DTR\_CHG\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_DTR\\_CHG\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_GET\_LINE\_CODE\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_GET\\_LINE\\_CODE\\_INT](#). (R/WTC/SS)

**USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_INT\_RAW** The raw interrupt status of [USB\\_SERIAL\\_JTAG\\_SET\\_LINE\\_CODE\\_INT](#). (R/WTC/SS)

Register 46.13. USB\_SERIAL\_JTAG\_INT\_ST\_REG (0x000C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_SET_LINE_CODE_INT_ST<br>USB_SERIAL_JTAG_GET_LINE_CODE_INT_ST<br>USB_SERIAL_JTAG_DTR_CHG_INT_ST<br>USB_SERIAL_JTAG_RTS_CHG_INT_ST<br>USB_SERIAL_JTAG_OUT_EP2_INT_ST<br>USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_ST<br>USB_SERIAL_JTAG_USB_BUS_RESET_INT_ST<br>USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_ST<br>USB_SERIAL_JTAG_STUFF_ERR_INT_ST<br>USB_SERIAL_JTAG_CRC16_ERR_INT_ST<br>USB_SERIAL_JTAG_CRC5_ERR_INT_ST<br>USB_SERIAL_JTAG_PID_ERR_INT_ST<br>USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_ST<br>USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_ST<br>USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_ST |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | Reset |   |   |   |   |   |   |   |

USB\_SERIAL\_JTAG\_JTAG\_IN\_FLUSH\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_JTAG\\_IN\\_FLUSH\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_SOF\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_SOF\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT\_ST The masked interrupt status of the [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_SERIAL\_IN\_EMPTY\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_PID\_ERR\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_PID\\_ERR\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_CRC5\_ERR\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_CRC5\\_ERR\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_CRC16\_ERR\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_CRC16\\_ERR\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_STUFF\_ERR\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_STUFF\\_ERR\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_IN\_TOKEN\_REC\_IN\_EP1\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_IN\\_TOKEN\\_REC\\_IN\\_EP1\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_USB\\_BUS\\_RESET\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_OUT\_EP1\_ZERO\_PAYLOAD\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_OUT\\_EP1\\_ZERO\\_PAYLOAD\\_INT](#). (RO)

USB\_SERIAL\_JTAG\_OUT\_EP2\_ZERO\_PAYLOAD\_INT\_ST The masked interrupt status of [USB\\_SERIAL\\_JTAG\\_OUT\\_EP2\\_ZERO\\_PAYLOAD\\_INT](#). (RO)

Continued on the next page...



**Register 46.13. USB\_SERIAL\_JTAG\_INT\_ST\_REG (0x000C)**

Continued from the previous page...

|   |     |        |           |        |    |
|---|-----|--------|-----------|--------|----|
| <b>USB_SERIAL_JTAG_RTS_CHG_INT_ST</b><br><a href="#">USB_SERIAL_JTAG_RTS_CHG_INT</a> . (RO)             | The | masked | interrupt | status | of |
| <b>USB_SERIAL_JTAG_DTR_CHG_INT_ST</b><br><a href="#">USB_SERIAL_JTAG_DTR_CHG_INT</a> . (RO)             | The | masked | interrupt | status | of |
| <b>USB_SERIAL_JTAG_GET_LINE_CODE_INT_ST</b><br><a href="#">USB_SERIAL_JTAG_GET_LINE_CODE_INT</a> . (RO) | The | masked | interrupt | status | of |
| <b>USB_SERIAL_JTAG_SET_LINE_CODE_INT_ST</b><br><a href="#">USB_SERIAL_JTAG_SET_LINE_CODE_INT</a> . (RO) | The | masked | interrupt | status | of |

Register 46.14. USB\_SERIAL\_JTAG\_INT\_ENA\_REG (0x0010)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_SET_LINE_CODE_INT_ENA<br>USB_SERIAL_JTAG_GET_LINE_CODE_INT_ENA<br>USB_SERIAL_JTAG_DTR_CHG_INT_ENA<br>USB_SERIAL_JTAG_RTS_CHG_INT_ENA<br>USB_SERIAL_JTAG_OUT_EP2_INT_ENA<br>USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_ENA<br>USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_ENA<br>USB_SERIAL_JTAG_USB_BUS_RESET_INT_ENA<br>USB_SERIAL_JTAG_STUFF_ERR_INT_ENA<br>USB_SERIAL_JTAG_CRC16_ERR_INT_ENA<br>USB_SERIAL_JTAG_CRC5_ERR_INT_ENA<br>USB_SERIAL_JTAG_PID_ERR_INT_ENA<br>USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_ENA<br>USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_ENA<br>USB_SERIAL_JTAG_SOF_INT_ENA<br>USB_SERIAL_JTAG_IN_FLUSH_INT_ENA |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0     |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

USB\_SERIAL\_JTAG\_JTAG\_IN\_FLUSH\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_JTAG\\_IN\\_FLUSH\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_SOF\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_SOF\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_SERIAL\_IN\_EMPTY\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_PID\_ERR\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_PID\\_ERR\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_CRC5\_ERR\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_CRC5\\_ERR\\_INT](#).  
(R/W)

USB\_SERIAL\_JTAG\_CRC16\_ERR\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_CRC16\\_ERR\\_INT](#).  
(R/W)

USB\_SERIAL\_JTAG\_STUFF\_ERR\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_STUFF\\_ERR\\_INT](#).  
(R/W)

USB\_SERIAL\_JTAG\_IN\_TOKEN\_REC\_IN\_EP1\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_IN\\_TOKEN\\_REC\\_IN\\_EP1\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_USB\\_BUS\\_RESET\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_OUT\_EP1\_ZERO\_PAYLOAD\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_OUT\\_EP1\\_ZERO\\_PAYLOAD\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_OUT\_EP2\_ZERO\_PAYLOAD\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_OUT\\_EP2\\_ZERO\\_PAYLOAD\\_INT](#). (R/W)

Continued on the next page...

## Register 46.14. USB\_SERIAL\_JTAG\_INT\_ENA\_REG (0x0010)

Continued from the previous page...

USB\_SERIAL\_JTAG\_RTS\_CHG\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_RTS\\_CHG\\_INT](#).  
(R/W)

USB\_SERIAL\_JTAG\_DTR\_CHG\_INT\_ENA Write 1 to enable [USB\\_SERIAL\\_JTAG\\_DTR\\_CHG\\_INT](#).  
(R/W)

USB\_SERIAL\_JTAG\_GET\_LINE\_CODE\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_GET\\_LINE\\_CODE\\_INT](#). (R/W)

USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_INT\_ENA Write 1 to enable  
[USB\\_SERIAL\\_JTAG\\_SET\\_LINE\\_CODE\\_INT](#). (R/W)

Register 46.15. USB\_SERIAL\_JTAG\_INT\_CLR\_REG (0x0014)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|---|---|-------|---|---|---|---|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_SET_LINE_CODE_INT_CLR<br>USB_SERIAL_JTAG_GET_LINE_CODE_INT_CLR<br>USB_SERIAL_JTAG_DTR_CHG_INT_CLR<br>USB_SERIAL_JTAG_RTS_CHG_INT_CLR<br>USB_SERIAL_JTAG_OUT_EP2_ZERO_PAYLOAD_INT_CLR<br>USB_SERIAL_JTAG_OUT_EP1_ZERO_PAYLOAD_INT_CLR<br>USB_SERIAL_JTAG_USB_BUS_RESET_INT_CLR<br>USB_SERIAL_JTAG_IN_TOKEN_REC_IN_EP1_INT_CLR<br>USB_SERIAL_JTAG_STUFF_ERR_INT_CLR<br>USB_SERIAL_JTAG_CRC16_ERR_INT_CLR<br>USB_SERIAL_JTAG_CRC5_ERR_INT_CLR<br>USB_SERIAL_JTAG_SERIAL_IN_EMPTY_INT_CLR<br>USB_SERIAL_JTAG_SERIAL_OUT_RECV_PKT_INT_CLR<br>USB_SERIAL_JTAG_JTAG_IN_FLUSH_INT_CLR |    |    |    |    |    |    |   |   |       |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16  | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | Reset |   |   |   |   |   |   |   |  |

**USB\_SERIAL\_JTAG\_JTAG\_IN\_FLUSH\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_JTAG\\_IN\\_FLUSH\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_SOF\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_SOF\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_SERIAL\_IN\_EMPTY\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_SERIAL\\_IN\\_EMPTY\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_PID\_ERR\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_PID\\_ERR\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_CRC5\_ERR\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_CRC5\\_ERR\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_CRC16\_ERR\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_CRC16\\_ERR\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_STUFF\_ERR\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_STUFF\\_ERR\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_IN\_TOKEN\_REC\_IN\_EP1\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_IN\\_TOKEN\\_REC\\_IN\\_EP1\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_USB\\_BUS\\_RESET\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_OUT\_EP1\_ZERO\_PAYLOAD\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_OUT\\_EP1\\_ZERO\\_PAYLOAD\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_OUT\_EP2\_ZERO\_PAYLOAD\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_OUT\\_EP2\\_ZERO\\_PAYLOAD\\_INT](#). (WT)

Continued on the next page...

**Register 46.15. USB\_SERIAL\_JTAG\_INT\_CLR\_REG (0x0014)**

Continued from the previous page...

**USB\_SERIAL\_JTAG\_RTS\_CHG\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_RTS\\_CHG\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_DTR\_CHG\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_DTR\\_CHG\\_INT](#). (WT)

**USB\_SERIAL\_JTAG\_GET\_LINE\_CODE\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_GET\\_LINE\\_CODE\\_INT](#).  
(WT)

**USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_INT\_CLR** Write 1 to clear [USB\\_SERIAL\\_JTAG\\_SET\\_LINE\\_CODE\\_INT](#).  
(WT)

**Register 46.16. USB\_SERIAL\_JTAG\_JFIFO\_ST\_REG (0x0020)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |       |   |   |   |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|-------|---|---|---|--|--|
| (reserved)                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_OUT_FIFO_RESET<br>USB_SERIAL_JTAG_IN_FIFO_RESET<br>USB_SERIAL_JTAG_OUT_FIFO_FULL<br>USB_SERIAL_JTAG_OUT_FIFO_EMPTY<br>USB_SERIAL_JTAG_IN_FIFO_CNT<br>USB_SERIAL_JTAG_IN_FIFO_FULL<br>USB_SERIAL_JTAG_IN_FIFO_EMPTY |   |   |   |   |   |   |   |       |   |   |   |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10   |   | 9 | 8 | 7 | 6 | 5 | 4 | 3     | 2 | 1 | 0 |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 1 | 0 | 0 | 1 | 0 | Reset |   |   |   |  |  |

Reset

**USB\_SERIAL\_JTAG\_IN\_FIFO\_CNT** Represents JTAG IN FIFO counter. (RO)**USB\_SERIAL\_JTAG\_IN\_FIFO\_EMPTY** Represents whether JTAG IN FIFO is empty.

0: Not empty

1: Empty

(RO)

**USB\_SERIAL\_JTAG\_IN\_FIFO\_FULL** Represents whether JTAG IN FIFO is full.

0: Not full

1: Full

(RO)

**USB\_SERIAL\_JTAG\_OUT\_FIFO\_CNT** Represents JTAG OUT FIFO counter. (RO)**USB\_SERIAL\_JTAG\_OUT\_FIFO\_EMPTY** Represents whether JTAG OUT FIFO is empty.

0: Not empty

1: Empty

(RO)

**USB\_SERIAL\_JTAG\_OUT\_FIFO\_FULL** Represents whether JTAG OUT FIFO is full.

0: Not full

1: Full

(RO)

**USB\_SERIAL\_JTAG\_IN\_FIFO\_RESET** Configures whether to reset JTAG IN FIFO.

0: No effect

1: Reset

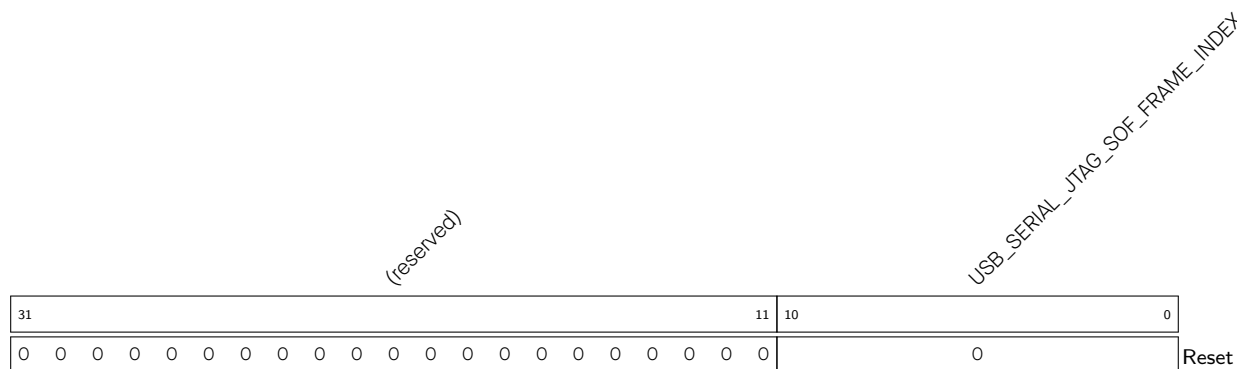
(R/W)

**USB\_SERIAL\_JTAG\_OUT\_FIFO\_RESET** Configures whether to reset JTAG OUT FIFO.

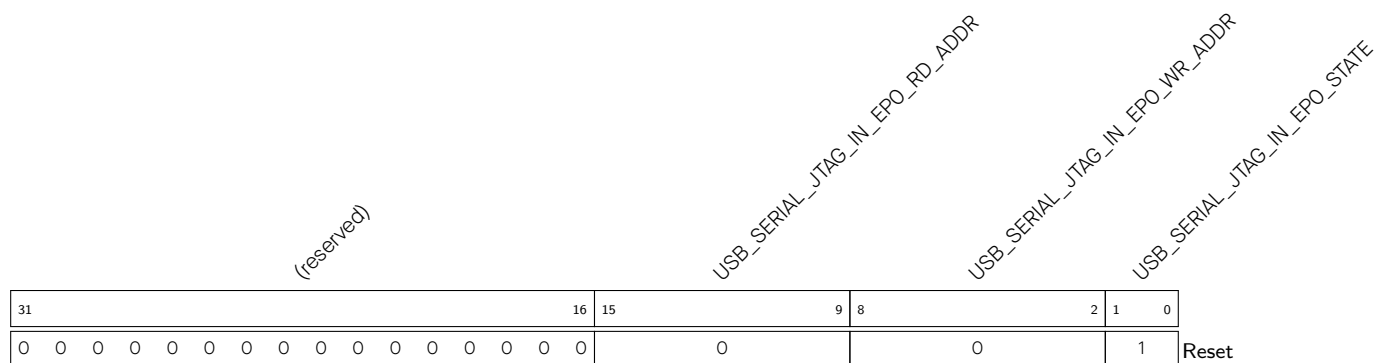
0: No effect

1: Reset

(R/W)

**Register 46.17. USB\_SERIAL\_JTAG\_FRAM\_NUM\_REG (0x0024)**

**USB\_SERIAL\_JTAG\_SOF\_FRAME\_INDEX** Represents frame index of received SOF frame. (RO)

**Register 46.18. USB\_SERIAL\_JTAG\_IN\_EPO\_ST\_REG (0x0028)**

**USB\_SERIAL\_JTAG\_IN\_EPO\_STATE** Represents state of IN Endpoint 0. (RO)

**USB\_SERIAL\_JTAG\_IN\_EPO\_WR\_ADDR** Represents write data address of IN endpoint 0. (RO)

**USB\_SERIAL\_JTAG\_IN\_EPO\_RD\_ADDR** Represents read data address of IN endpoint 0. (RO)

### Register 46.19. USB\_SERIAL\_JTAG\_IN\_EP1\_ST\_REG (0x002C)

|                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |
|------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|
| (reserved)       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP1_RD_ADDR |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP1_WR_ADDR |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP1_STATE |  |  |  |  |  |  |  |
| 3116             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 159                            |  |  |  |  |  |  |  | 82                             |  |  |  |  |  |  |  | 10                           |  |  |  |  |  |  |  |
| 0000000000000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                              |  |  |  |  |  |  |  | 0                              |  |  |  |  |  |  |  | 1Reset                       |  |  |  |  |  |  |  |

**USB\_SERIAL\_JTAG\_IN\_EP1\_STATE** Represents state of IN Endpoint 1. (RO)

**USB\_SERIAL\_JTAG\_IN\_EP1\_WR\_ADDR** Represents write data address of IN endpoint 1. (RO)

USB\_SERIAL\_JTAG\_IN\_EP1\_RD\_ADDR Represents read data address of IN endpoint 1. (RO)

### Register 46.20. USB\_SERIAL\_JTAG\_IN\_EP2\_ST\_REG (0x0030)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP2_RD_ADDR |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP2_WR_ADDR |  |  |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP2_STATE |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                             |  |  |  |  |  |  |  | 15                             |  |  |  |  |  |  |  | 9                            |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  | 2 |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                              |  |  |  |  |  |  |  | 0                              |  |  |  |  |  |  |  | 1                            |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**USB\_SERIAL\_JTAG\_IN\_EP2\_STATE** Represents state of IN Endpoint 2. (RO)

**USB\_SERIAL\_JTAG\_IN\_EP2\_WR\_ADDR** Represents write data address of IN endpoint 2. (RO)

**USB\_SERIAL\_JTAG\_IN\_EP2\_RD\_ADDR** Represents read data address of IN endpoint 2. (RO)



**Register 46.21. USB\_SERIAL\_JTAG\_IN\_EP3\_ST\_REG (0x0034)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |    |   |  |  |  |  |  |                                |   |   |  |  |  |  |  |                              |  |   |   |   |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|----|---|--|--|--|--|--|--------------------------------|---|---|--|--|--|--|--|------------------------------|--|---|---|---|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | USB_SERIAL_JTAG_IN_EP3_RD_ADDR |    |   |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP3_WR_ADDR |   |   |  |  |  |  |  | USB_SERIAL_JTAG_IN_EP3_STATE |  |   |   |   |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                             | 15 |   |  |  |  |  |  |                                | 9 | 8 |  |  |  |  |  |                              |  | 2 | 1 | 0 |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0  | 0 |  |  |  |  |  |                                | 0 |   |  |  |  |  |  | 1                            |  |   |   |   |  |  |  |

Reset

**USB\_SERIAL\_JTAG\_IN\_EP3\_STATE** Represents state of IN Endpoint 3. (RO)**USB\_SERIAL\_JTAG\_IN\_EP3\_WR\_ADDR** Represents write data address of IN endpoint 3. (RO)**USB\_SERIAL\_JTAG\_IN\_EP3\_RD\_ADDR** Represents read data address of IN endpoint 3. (RO)**Register 46.22. USB\_SERIAL\_JTAG\_OUT\_EPO\_ST\_REG (0x0038)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                                 |   |   |  |  |  |  |   |                                 |  |  |  |   |   |   |   |                               |  |  |  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---------------------------------|---|---|--|--|--|--|---|---------------------------------|--|--|--|---|---|---|---|-------------------------------|--|--|--|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | USB_SERIAL_JTAG_OUT_EPO_RD_ADDR |   |   |  |  |  |  |   | USB_SERIAL_JTAG_OUT_EPO_WR_ADDR |  |  |  |   |   |   |   | USB_SERIAL_JTAG_OUT_EPO_STATE |  |  |  |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                              |   |   |  |  |  |  | 9 | 8                               |  |  |  |   | 2 | 1 | 0 |                               |  |  |  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                               | 0 | 0 |  |  |  |  |   | 0                               |  |  |  | 0 |   |   |   |                               |  |  |  |  |  |  |  |
| Reset      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                                 |   |   |  |  |  |  |   |                                 |  |  |  |   |   |   |   |                               |  |  |  |  |  |  |  |

Reset

**USB\_SERIAL\_JTAG\_OUT\_EPO\_STATE** Represents state of OUT Endpoint 0. (RO)**USB\_SERIAL\_JTAG\_OUT\_EPO\_WR\_ADDR** Represents write data address of OUT endpoint 0.When [USB\\_SERIAL\\_JTAG\\_SERIAL\\_OUT\\_RECV\\_PKT\\_INT](#) is detected, there are (USB\_SERIAL\_JTAG\_OUT\_EPO\_WR\_ADDR – 2) bytes data in OUT endpoint 0.

(RO)

**USB\_SERIAL\_JTAG\_OUT\_EPO\_RD\_ADDR** Represents read data address of OUT endpoint 0. (RO)

**Register 46.23. USB\_SERIAL\_JTAG\_OUT\_EP1\_ST\_REG (0x003C)**

|                     |  |  |  |  |  |  |  |  |  |                                      |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
|---------------------|--|--|--|--|--|--|--|--|--|--------------------------------------|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|-------------------------------|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|
| (reserved)          |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_OUT_EP1_REC_DATA_CNT |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_OUT_EP1_RD_ADDR |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_OUT_EP1_WR_ADDR |  |  |  |  |  |  |  |  |  | USB_SERIAL_JTAG_OUT_EP1_STATE |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| 31                  |  |  |  |  |  |  |  |  |  | 23                                   |  |  |  |  |  |  |  |  |  | 22                              |  |  |  |  |  |  |  |  |  | 16                              |  |  |  |  |  |  |  |  |  | 15                            |  |  |  |  |  |  |  |  |  | 9 |  |  |  |  |  |  |  |  |  | 8     |  |  |  |  |  |  |  |  |  | 2 |  |  |  |  |  |  |  |  |  | 1 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  | 0                                    |  |  |  |  |  |  |  |  |  | 0                               |  |  |  |  |  |  |  |  |  | 0                               |  |  |  |  |  |  |  |  |  | 0                             |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |

Reset

**USB\_SERIAL\_JTAG\_OUT\_EP1\_STATE** Represents state of OUT Endpoint 1. (RO)

**USB\_SERIAL\_JTAG\_OUT\_EP1\_WR\_ADDR** Represents write data address of OUT endpoint 1.

When **USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT** is detected, there are  
(**USB\_SERIAL\_JTAG\_OUT\_EP1\_WR\_ADDR** – 2) bytes data in OUT endpoint 1.  
(RO)

**USB\_SERIAL\_JTAG\_OUT\_EP1\_RD\_ADDR** Represents read data address of OUT endpoint 1. (RO)

**USB\_SERIAL\_JTAG\_OUT\_EP1\_REC\_DATA\_CNT** Represents data count in OUT endpoint 1 when one packet is received. (RO)

**Register 46.24. USB\_SERIAL\_JTAG\_OUT\_EP2\_ST\_REG (0x0040)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  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 |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  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 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  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|  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  | 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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  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0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

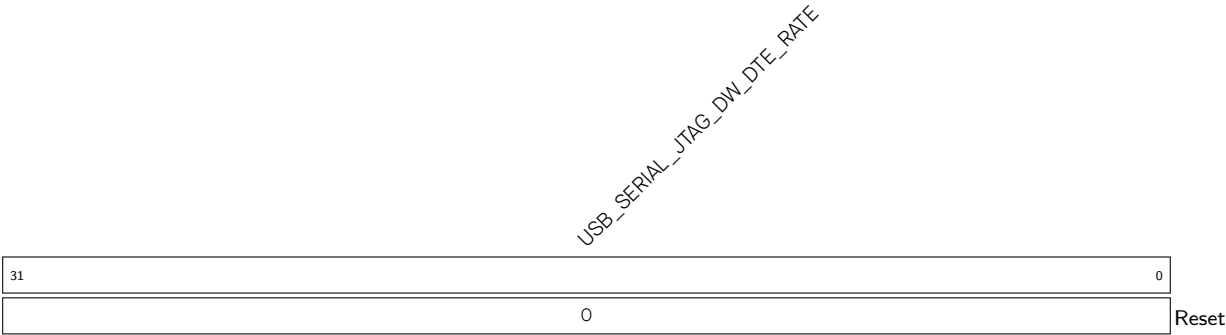
**USB\_SERIAL\_JTAG\_OUT\_EP2\_STATE** Represents state of OUT Endpoint 2. (RO)

**USB\_SERIAL\_JTAG\_OUT\_EP2\_WR\_ADDR** Represents write data address of OUT endpoint 2.

When **USB\_SERIAL\_JTAG\_SERIAL\_OUT\_RECV\_PKT\_INT** is detected there are  
(**USB\_SERIAL\_JTAG\_OUT\_EP2\_WR\_ADDR** – 2) bytes data in OUT endpoint 2.  
(RO)

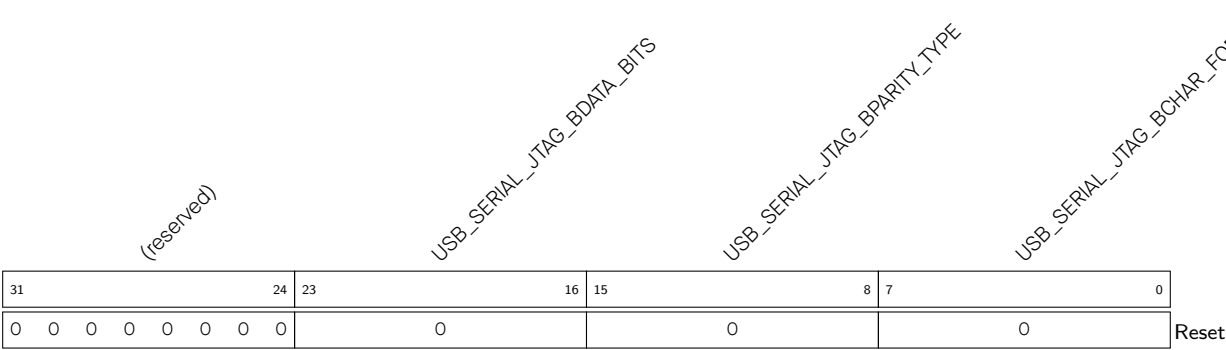
**USB\_SERIAL\_JTAG\_OUT\_EP2\_RD\_ADDR** Represents read data address of OUT endpoint 2. (RO)

Register 46.25. USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_W0\_REG (0x0050)



**USB\_SERIAL\_JTAG\_DW\_DTE\_RATE** Represents the value of dwDTERate set by host through SET\_LINE\_CODING command. (RO)

Register 46.26. USB\_SERIAL\_JTAG\_SET\_LINE\_CODE\_W1\_REG (0x0054)

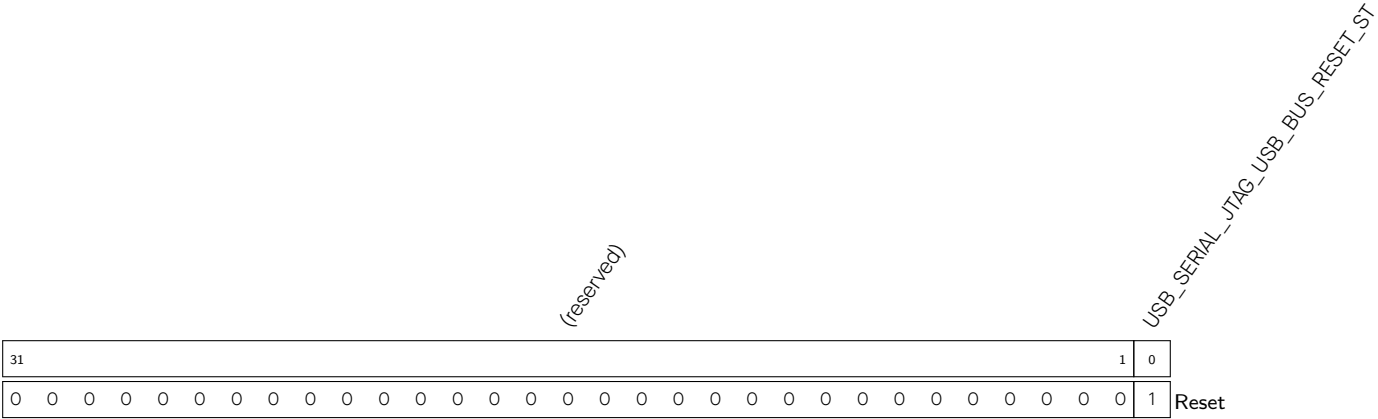


**USB\_SERIAL\_JTAG\_BCHAR\_FORMAT** Represents the value of bCharFormat set by host through SET\_LINE\_CODING command. (RO)

**USB\_SERIAL\_JTAG\_BPARITY\_TYPE** Represents the value of bParityTpye set by host through SET\_LINE\_CODING command. (RO)

**USB\_SERIAL\_JTAG\_BDATA\_BITS** Represents the value of bDataBits set by host through SET\_LINE\_CODING command. (RO)

Register 46.27. USB\_SERIAL\_JTAG\_BUS\_RESET\_ST\_REG (0x0068)

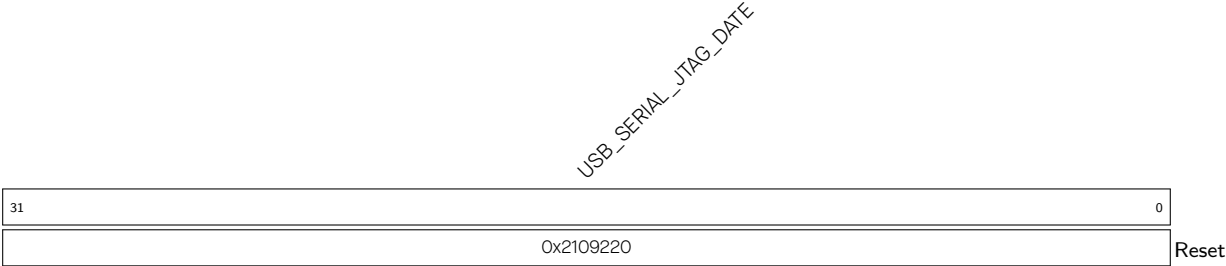


**USB\_SERIAL\_JTAG\_USB\_BUS\_RESET\_ST** Represents whether USB bus reset is released.

- 0: USB Serial/JTAG is in USB bus reset status
- 1: USB bus reset is released

(RO)

Register 46.28. USB\_SERIAL\_JTAG\_DATE\_REG (0x0088)



**USB\_SERIAL\_JTAG\_DATE** Version control register. (R/W)

## Chapter 47

# Ethernet Media Access Controller (EMAC)

## 47.1 Overview

By using the external Ethernet PHY (physical layer), ESP32-P4 can send and receive data via Ethernet MAC (Media Access Controller) according to the IEEE 802.3 standard, as Figure 47.1-1 shows. Ethernet is currently the most commonly used network protocol that controls how data is transmitted over local- and wide-area networks, abbreviated as LAN and WAN, respectively.

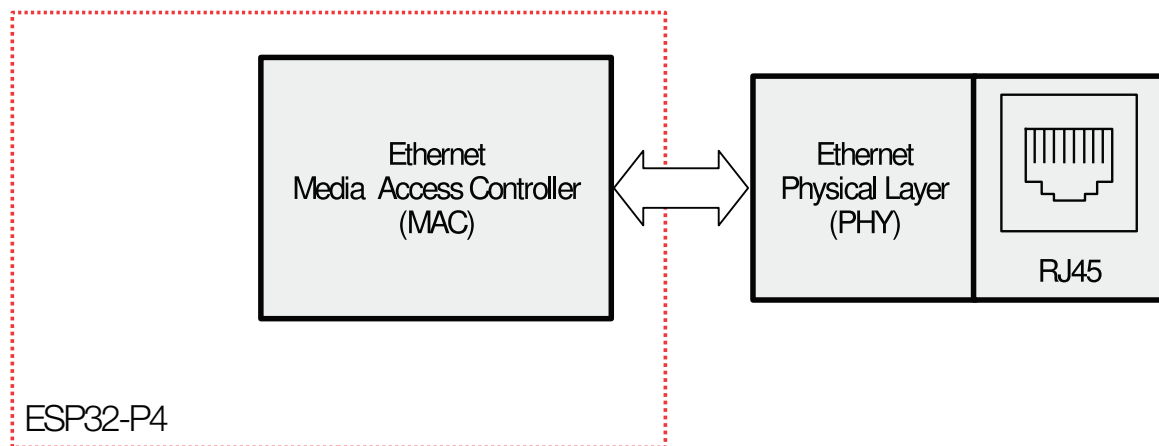


Figure 47.1-1. Ethernet MAC Functionality Overview

ESP32-P4 Ethernet MAC complies with the following standards:

- IEEE 802.3-2002 for Ethernet MAC
- IEEE 1588-2008 standard for precise networked clock synchronization
- IEEE 802.3 standard Media Independent Interface (MII) and Reduced Media Independent Interface (RMII)
- IEEE 802.3az-2010 for Energy Efficient Ethernet
- IEEE 802.1Q for VLAN frame format

## 47.2 Features

- Data rates of 10/100 Mbit/s through an external PHY interface
- Communication with an external Fast Ethernet PHY through IEEE 802.3-compliant MII and RMII interfaces
- Full-duplex and half-duplex modes

- Carrier Sense Multiple Access or Collision Detection (CSMA/CD) protocol in half-duplex mode
- IEEE 802.3x flow control in full-duplex mode
- Optional forwarding of received pause control frame to the user application in full-duplex mode
- Back-pressure flow control in half-duplex mode
- Automatic transmission of zero-quanta pause frame on deassertion of flow control input in full-duplex mode
- Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in Receive paths
- Automatic CRC and padding (all 0) generation controllable on a per-frame basis
- Options for automatic padding generation for data below the minimum frame length
- Programmable frame length supporting jumbo frames of up to 16 KB
- Programmable inter-frame gap (IFG) from 40 to 96 bit times in steps of 8)
- Supports a variety of flexible address filtering modes:
  - Up to eight 48-bit perfect address filters with masks for each byte
  - Up to eight 48-bit source address (SA) address comparison check with masks for each byte
  - Option to pass all multicast addressed frames
  - Promiscuous mode support to pass all frames without any filtering for network monitoring
  - Passes all incoming packets (as per filter) with a status report
- Separate 32-bit status returned for transmission and reception packets
- Supports IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces for the application
- Management Data Input/Output (MDIO) interface for PHY device configuration and management
- Supports checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame
- Supports checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams
- Supports 64-bit timestamp on each transmit and receive frame (see IEEE 1588-2008)
- Supports Energy Efficient Ethernet (see IEEE 802.3az-2010)
- CRC replacement, SA insertion or replacement, and VLAN insertion, replacement or deletion in transmit frames
- Two FIFOs: 256-byte TX FIFO and 256-byte RX FIFO
- Receive status vectors inserted into RX FIFO after the EOF (end of frame) transfer, which enables multiple-frame storage in RX FIFO without requiring another FIFO to store those frames' receive status
- Option to forward good runt frames
- Supports statistics by generating pulses for frames dropped or corrupted due to overflow in RX FIFO
- Automatic re-transmission of collision frames (subject to certain conditions, see Section [47.4.1.1](#))

- Discarding frames in cases of late collisions, excessive collisions, excessive deferrals, and underflow conditions
- Software control to flush TX FIFO

## 47.3 Ethernet MAC Architecture

Figure 47.3-1 shows the block diagram of the Ethernet MAC.

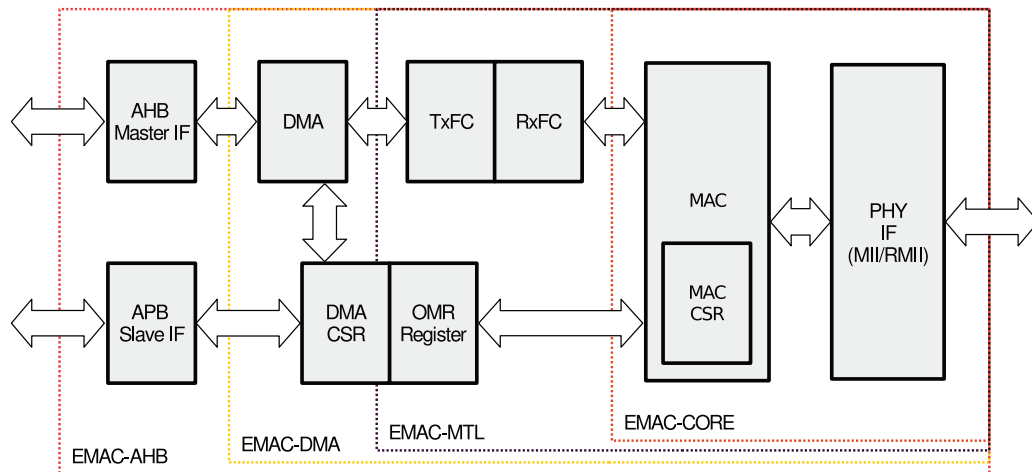


Figure 47.3-1. Ethernet MAC Block Diagram

Ethernet MAC consists of three layers: EMAC\_CORE (MAC Core Layer), EMAC\_MTL (MAC Transition Layer), and EMAC\_DMA (Direct Memory Access). Each of these three layers has two directions: TX and RX. They are connected to the system through the Advanced High Performance Bus (AHB) and the Advanced Peripheral Bus (APB) on the chip. Off the chip, they communicate with the external PHY through the MII and RMII interfaces to establish an Ethernet connection.

## 47.4 Functional Description

### 47.4.1 EMAC\_CORE

The MAC supports two interfaces (see Section 47.4.4) towards the PHY chip. The PHY interface can be selected only once after the chip reset. The MAC core communicates with the application side (DMA side) using the MAC Transmit Interface (MTI), MAC Receive Interface (MRI), and the MAC Control Interface (MCI).

#### 47.4.1.1 Transmission

Transmission is initiated when the MTL application pushes in data with the SOF signal (start of frame) asserted. When the SOF signal is detected, the MAC accepts the data and begins transmitting to the RMII or MII. The time required to transmit the frame data to the RMII or MII after the application initiates transmission is variable, depending on delay factors like IFG delay, time to transmit preamble or SFD (Start Frame Delimiter), and any back-off delays for half-duplex mode. Until then, the MAC does not accept the data received from MTL by deasserting the ready signal.

After the EOF (end of frame) is transmitted to the MAC, the MAC completes normal transmission and then gives the Transmit Status to the MTL. If a normal collision (in half-duplex mode) occurs during transmission, the MAC core makes valid the Transmit Status to the MTL. It will then accept and drop all further data until the next SOF is received. The MTL block should retransmit the same frame from SOF on observing a retry request (in the Status) from the MAC.

The MAC issues an underflow status if the MTL is not able to provide the data continuously during the transmission. During the normal transmission of a frame from the MTL, if the MAC receives an SOF without getting an EOF for the previous frame, then the SOF is ignored and the new frame is considered as a continuation of the previous frame.

### Transmit Flow Control

In full-duplex mode, when the Transmit Flow Control Enable bit ([TFCE](#)) is set to 1, the MAC generates pause frames and transmits them as necessary, with the calculated CRC appended.

Pause frame generation can be initiated in two ways. When the application sets the Flow Control Busy bit ([FCBBA](#)) to 1, or when the RX FIFO is full, a pause frame is transmitted.

- If the application has requested flow control by setting the [FCBBA](#) bit to 1, the MAC will generate and transmit a single pause frame. The value of the pause time in the generated frame is the pause time value programmed in the [PAUSE\\_TIME](#) field. If the application wants to extend or end the pause prior to the time specified in the previously transmitted pause frame, it must request another pause frame transmission after programming the pause time field [PAUSE\\_TIME](#) with an appropriate value.
- If the application has requested flow control when the RX FIFO is full, the MAC will generate and transmit a pause frame. The value of the pause time in the generated frame is the pause time value programmed in the [PAUSE\\_TIME](#) field. If the RX FIFO remains full at a configurable number of slot times ([PLT](#)) before the pause time runs out, a second pause frame will be transmitted. The process will be repeated as long as the RX FIFO remains full. If the FIFO is no longer full prior to the sampling time, the MAC will send a pause frame with zero pause time to indicate to the remote end that the RX buffer is ready to receive new data frames.

### Retransmission During Collision

In half-duplex mode, a collision may occur on the MAC line interface when frames are transmitted to the MAC. The MAC may indicate a retry attempt by giving the status even before the EOF is transferred. Then the MAC will enable the retransmission by popping out the frame again from the FIFO. After more than 96 bytes are popped towards the MAC core, the FIFO controller frees the space in the FIFO, and makes it available to the DMA to push in more data. This means that the retransmission is not possible after this threshold is crossed or when the MAC core indicates a late-collision event.

The MAC transmitter may abort the transmission of a frame because of collision, TX FIFO underflow, loss of carrier, jabber timeout, no carrier, excessive deferral, or late collision. When frame transmission is aborted because of collision, the MAC requests retransmission of the frame.

### Transmit Status Word

At the end of the Ethernet frame transfer, the MAC outputs the transmit status to the application. The detailed description of the Transmit Status is the same as for [TDES0](#).



### 47.4.1.2 Reception

A receive operation is initiated when the MAC detects an SFD on the RMII or MII. The MAC strips the preamble and SFD before proceeding to process the frame. The header fields are checked for filtering and the FCS (Frame Check Sequence) field used to verify the CRC for the frame. The received frame is stored in a shallow buffer until the address filtering is performed. The frame is dropped in the MAC if it fails the address filtering.

The frames received by the MAC are pushed into the RX FIFO. Once the RX FIFO crosses the configured Receive threshold ([RX\\_THRESH\\_CTRL](#)), its status is indicated to the DMA, so that the DMA can initiate a pre-configured burst transfers towards the AHB interface.

In the default cut-through mode, when the FIFO receives 64 bytes or a full packet of data, it pops out the data and indicates the availability to the DMA. Once the DMA initiates the transfer to the AHB interface, the data transmission continues from the FIFO until a complete packet has been transferred. Upon the completion of the EOF frame transfer, the status word will be popped out and transmitted to the DMA controller.

#### Receive Protocol

The receive module strips the preamble and SFD of the received frame. Once the SFD is detected, the MAC begins sending the Ethernet frame data to the RX FIFO, starting from the first byte following the SFD (destination address). If the IEEE 1588 timestamp feature is enabled, the snapshot of system time will be captured whenever an SFD of any frame is detected on MII, and sent to the application unless the MAC filters out and drops the frame.

If the Length/Type field of the receiving frame is less than 0x600 and if the MAC is programmed for the automatic CRC/paddingstripping option, the MAC sends the frame data up to the count specified in the Length/Type field to the RX FIFO, and then starts dropping bytes (including the FCS field). If the Length/Type field is greater than or equal to 0x600, the MAC will send all received Ethernet frame data to the RX FIFO, regardless of the value on the programmed automatic CRC stripping option. By default, the MAC is programmed for the watchdog timer to be enabled, that is frames above 2048 bytes (including DA, SA, LT, data, padding, and FCS) are cut off. This feature can be disabled by programming the Watchdog Disable bit [EMACWATCHDOG](#). However, even if the watchdog timer is disabled, frames longer than 16 KB will still be cut off and the watchdog timeout status will be indicated.

#### Receive Frame Controller

If the [RECEIVE\\_ALL](#) bit in the MAC Frame Filter Register is reset, the MAC performs frame filtering based on the destination and source addresses. The application still needs to perform another level of filtering if it decides not to receive any bad frames like runt, CRC error frames, etc. On detecting a filter failure, the frame is dropped and not transmitted to the application. When the filter parameters change dynamically, if a DA and SA filter failure occurs, the reset of the frame is dropped and the Receive Status word (with zero frame length, CRC Error, and Runt Error bits set) is updated immediately indicating the filter failure.

#### Receive Flow Control

The MAC detects the receiving pause frame and pauses the frame transmission for the delay specified within the received pause frame (in full-duplex mode only). The Pause Frame Detection Function can be enabled or disabled with the [RFCE](#) bit. Once the receive flow control is enabled, the MAC starts monitoring the received frame destination address for any match with the multicast address of the control frame (0x0180 C200 0001).

If a match is detected (i.e., the destination address of the received frame matches the destination address of the reserved control frame), the MAC decides whether to transmit the received control frame to the application, according to the [PCF](#) field.

The MAC also decodes the type, the opcode, and the pause timer field of the receiving control Frame. If the byte count of the status indicates 64 bytes, and if there is no CRC error, the MAC transmitter will pause the transmission of any data frame for the duration of the decoded pause time value multiplied by the slot time (64 byte times for 10/100 Mbit/s mode). Meanwhile, if another pause frame is detected with a zero pause time, the MAC will reset the pause time and give another pause request.

If the received control frame matches neither the type field (0x8808), the opcode (0x00001), nor the byte length (64 bytes), or if there is a CRC error, the MAC will not generate a pause.

In the case of a pause frame with a multicast destination address, the MAC filters the frame according to the address match.

For a pause frame with a unicast destination address, the filtering depends on whether the DA matched the contents of the MAC Address Register 0 and the [UPFD](#) (detecting a pause frame even with a unicast destination address) is set. The [PCF](#) register controls the filtering for control frames in addition to the address filter.

### Receive Operation Multiframe Handling

Since the status is available immediately following the data, the MAC is capable of storing any number of frames into the FIFO, as long as it is not full.

### Error Handling

If the RX FIFO is full before it receives the EOF data from the MAC, an overflow will be declared and the whole frame will be dropped. The status bit [RDESO](#)[11] will reflect the fact that this frame is a partial frame due to overflow. The RX FIFO can perform the filtering of error frames and runt frames, if this function is enabled via [FLUSH\\_TX\\_FIFO](#) and [FWD\\_UNDER\\_GF](#).

In cut-through mode, if a frame's status and length are available when reading an SOF from the RX FIFO, the whole error frame can be dropped. The DMA can flush the error frame being read from the FIFO by clearing [FWD\\_ERR\\_FRAME](#) to 0. The DMA then stops transferring data to the application, internally reads out the rest of the frame, and drops it. The MTL will then start the transfer of the next frame, if it is available. If FIFO is available, the transmission of the next frame will be initiated.

### Receive Status Word

At the end of the Ethernet frame transfer, the MAC outputs the receive status to the application via [EMAC\\_DMA](#). The detailed description of the receive status is the same for bit[31:0] in [RDESO](#).

## 47.4.2 EMAC\_MTL (MAC Transaction Layer)

The MAC Transaction Layer provides FIFO memory to buffer and regulate the frames between the application system memory and the MAC. It also enables the data to be transmitted between the application clock domain and the MAC clock domains. The MTL layer has two data paths, namely the Transmit path and the Receive path. The data path for both directions is 32-bit wide and operates with a simple FIFO protocol.

### 47.4.3 EMAC\_DMA

EMAC has its own DMA module, with independent Transmit and Receive engines and a CSR (Control and Status Registers) space. The Transmit engine transfers data from the system memory to the device port (MTL), while the Receive engine transmits data from the device port to the system memory. The controller uses descriptors to efficiently move data from source to destination with minimal Host CPU intervention. The DMA is designed for packet-oriented data transfer such as frames in Ethernet. The controller can be programmed to interrupt the Host CPU for normal situations, such as the completion of frame transmission or reception, or error conditions.

#### 47.4.3.1 Transmit Descriptors

Figure 47.4-1 shows the structure of the transmit descriptor linked list. Table 47.4-1 through Table 47.4-4 show the descriptions of each transmit descriptor.

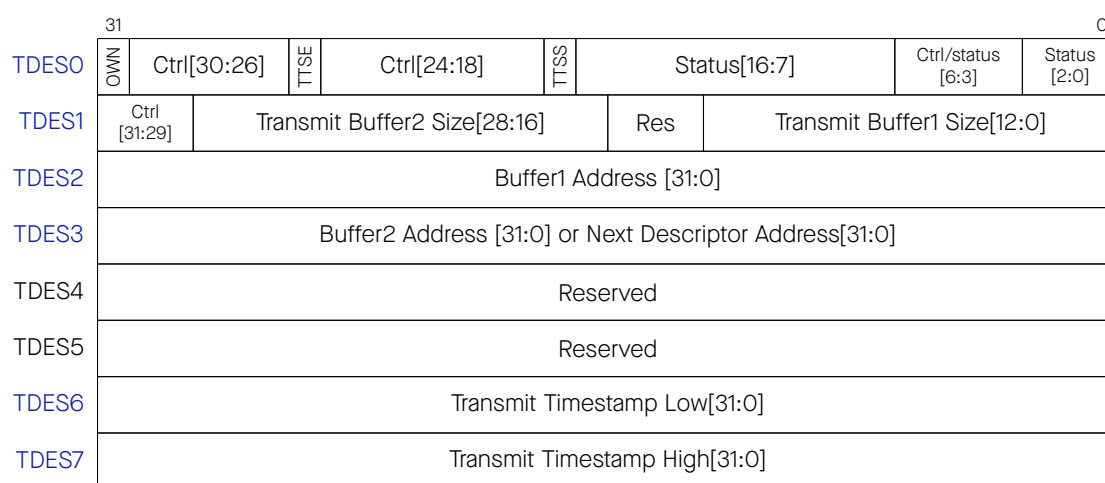


Figure 47.4-1. Transmit Descriptor Linked List

Table 47.4-1. Transmit Descriptor 0 (TDES0)

| Bits | Name                        | Description  |
|------|-----------------------------|--|
| [31] | OWN: Own Bit                | When set, this bit indicates that the descriptor is owned by the DMA. When reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit, either when it completes the frame transmission or when the buffers allocated to the descriptor are empty. The ownership bit of the First Descriptor of the frame should be set after all subsequent descriptors belonging to the same frame have been set. This avoids a possible race condition between fetching a descriptor and the driver setting an ownership bit. |
| [30] | IC: Interrupt on Completion | When set, this bit sets the Transmit Interrupt <a href="#">TRANS_INT</a> after the present frame has been transmitted. This bit is valid only when the last segment bit <a href="#">TDES0[29]</a> is set.  |
| [29] | LS: Last Segment            | When set, this bit indicates that the buffer contains the last segment of the frame, and the TBS1 or TBS2 field in TDES1 should have a non-zero value.   |

| Bits    | Name                             | Description  |
|---------|----------------------------------|--|
| [28]    | FS: First Segment                | When set, this bit indicates that the buffer contains the first segment of a frame.  |
| [27]    | DC: Disable CRC                  | When this bit is set, the MAC does not append a cyclic redundancy check (CRC) to the end of the transmitted frame. This is valid only when the first segment (TDES0[28]) is set.   |
| [26]    | DP: Disable Padding              | When this bit is set, the MAC does not automatically add padding to a frame shorter than 64 bytes. When this bit is reset, the DMA automatically adds padding and CRC to a frame shorter than 64 bytes, and the CRC field is added despite the state of the DC (TDES0[27]) bit. This is valid only when the first segment (TDES0[28]) is set.  |
| [25]    | TTSE: Transmit Time Stamp Enable | When this bit is set, the MAC enables IEEE1588 hardware timestamping for the transmit frame.   |
| [24]    | CRCR: CRC Replacement Control    | When set, the MAC replaces the last four bytes of the transmitted packet with recalculated CRC bytes. The Host should ensure that the CRC bytes are present in the frame being transmitted from the Transmit Buffer. This bit is valid when the First Segment control bit (TDES0[28]) is set. In addition, CRC replacement is done only when Bit TDES0[27] is set to 1.  |
| [23:22] | CIC: Checksum Insertion Control  | <p>These bits control the checksum calculation and insertion. Bit encodings are shown below:</p> <ul style="list-style-type: none"> <li>• 00: Checksum insertion is disabled.</li> <li>• 01: Only IP header checksum calculation and insertion are enabled.</li> <li>• 10: IP header checksum and payload checksum calculation and insertion are enabled, but pseudo-header checksum is not calculated in hardware.</li> <li>• 11: IP Header checksum and payload checksum calculation and insertion are enabled, and pseudo-header checksum is calculated in hardware.</li> </ul> <p>This field is valid when the First Segment control bit (TDES0[28]) is set.</p> |
| [21]    | TER: Transmit End of Ring        | When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.   |
| [20]    | TCH: Second Address Chained      | When set, this bit indicates that the second address in the descriptor is the Next Descriptor address, rather than the second buffer address. When TDES0[20] is set, TBS2 (TDES1[28:16]) is a “don’t care” value. TDES0[21] takes precedence over TDES0[20]. This bit must be set to 1.  |

| Bits    | Name                            | Description  |
|---------|---------------------------------|--|
| [19:18] | VLIC: VLAN Insertion Control    | <p>When set, these bits request the MAC to perform VLAN tagging or untagging before transmitting the frames. If the frame is modified for VLAN tags, the MAC automatically recalculates and replaces the CRC bytes. The following list describes the values of these bits:</p> <ul style="list-style-type: none"> <li>• 00: Do not add a VLAN tag.</li> <li>• 01: Remove the VLAN tag from the frames before transmission. This option should be used only with the VLAN frames.</li> <li>• 10: Insert a VLAN tag with the tag value programmed in VLAN Tag Inclusion or Replacement Register.</li> <li>• 11: Replace the VLAN tag in frames with the Tag value programmed in VLAN Tag Inclusion or Replacement Register. This option should be used only with the VLAN frames.</li> </ul> |
| [17]    | TTSS: Transmit Timestamp Status | <p>This bit is used as a status bit to indicate that a timestamp was captured for the described transmit frame. When this bit is set, <a href="#">TDES6</a> and <a href="#">TDES7</a> have a timestamp value captured for the transmit frame. This bit is valid only when the descriptor's LS (<a href="#">TDES0[29]</a>) is set.</p>  |
| [16]    | IHE: IP Header Error            | <p>When set, this bit indicates that the MAC transmitter detected an error in the IP datagram header. The transmitter checks the header length in the IPv4 packet against the number of header bytes received from the application, and indicates an error status if there is a mismatch. For IPv6 frames, a header error is reported if the main header length is not 40 bytes. Furthermore, the Ethernet Length/Type field value for an IPv4 or IPv6 frame must match the IP header version received with the packet. For IPv4 frames, an error status is also indicated if the Header Length field has a value less than 0x5.</p>   |
| [15]    | ES: Error Summary               | <p>Indicates the logical OR of the following bits:</p> <ul style="list-style-type: none"> <li>• <a href="#">TDES0[16]</a>: IP Header Error</li> <li>• <a href="#">TDES0[14]</a>: Jabber Timeout</li> <li>• <a href="#">TDES0[13]</a>: Frame Flush</li> <li>• <a href="#">TDES0[12]</a>: IP Payload Error</li> <li>• <a href="#">TDES0[11]</a>: Loss of Carrier</li> <li>• <a href="#">TDES0[10]</a>: No Carrier</li> <li>• <a href="#">TDES0[9]</a>: Late Collision</li> <li>• <a href="#">TDES0[8]</a>: Excessive Collision</li> <li>• <a href="#">TDES0[2]</a>: Excessive Deferral</li> <li>• <a href="#">TDES0[1]</a>: Underflow Error</li> </ul>   |
| [14]    | JT: Jabber Timeout              | <p>When set, this bit indicates the MAC transmitter has experienced a jabber timeout. This bit is only set when the EMACJABBER bit (disable jabber) of <a href="#">EMACCONFIG_REG</a> is not set.</p>  |
| [13]    | FF: Frame Flushed               | <p>When set, this bit indicates that the DMA or MTL flushed the frame because of a software Flush command given by the CPU.</p>  |

| Bits  | Name                    | Description  |
|-------|-------------------------|--|
| [12]  | IPE: IP Payload Error   | When set, this bit indicates that the MAC transmitter detected an error in the TCP, UDP, or ICMP IP datagram payload. The transmitter checks the payload length received in the IPv4 or IPv6 header against the actual number of TCP, UDP, or ICMP packet bytes received from the application, and issues an error status in case of a mismatch.   |
| [11]  | LOC: Loss of Carrier    | When set, this bit indicates that a Loss of Carrier occurred during frame transmission (that is, the MII_CRS signal was inactive for one or more transmit clock periods during frame transmission). This is valid only for the frames transmitted without collision and when the MAC operates in the half-duplex mode.   |
| [10]  | NC: No Carrier          | When set, this bit indicates that the carrier sense signal from the PHY was not asserted during transmission.  |
| [9]   | LC: Late Collision      | When set, this bit indicates that frame transmission was aborted because of a collision occurring after the collision window (in MII mode, 64 byte times including Preamble, and 512 byte times including Preamble and Carrier Extension). This bit is not valid if the Underflow Error bit is set.  |
| [8]   | EC: Excessive Collision | When set, this bit indicates that the transmission was aborted after 16 successive collisions while attempting to transmit the current frame. If the EMACRETRY bit of <a href="#">EMACCONFIG_REG</a> is set, this bit is set after the first collision, and the transmission of the frame is aborted.  |
| [7]   | VF: VLAN Frame          | When set, this bit indicates that the transmitted frame was a VLAN-type frame.   |
| [6:3] | Ctrl/status             | These status bits indicate the number of collisions occurring before the frame was transmitted. This count is not valid when the Excessive Collisions bit ( <a href="#">TDES0[8]</a> ) is set. The CPU updates this status field only in the half-duplex mode.   |
| [2]   | ED: Excessive Deferral  | When set, this bit indicates that the transmission has ended because of excessive deferral of over 24,288 bit times (if Jumbo Frame is enabled) if the EMACDEFERRAL bit (deferral check) of <a href="#">EMACCONFIG_REG</a> is set high.  |
| [1]   | UF: Underflow Error     | When set, this bit indicates that the MAC aborted the frame because the data arrived late from the Host memory. Underflow Error indicates that the DMA encountered an empty transmit buffer while transmitting the frame. The transmission process enters the Suspended state and sets both Transmit Underflow Register (Status Register <a href="#">TRANS_UNDFLOW</a> ) and Transmit Interrupt Register (Status Register <a href="#">TRANS_INT</a> ). |
| [0]   | DB: Deferred Bit        | When set, this bit indicates that the MAC defers before transmission because of the presence of a carrier. This bit is valid only in the half-duplex mode.   |

**Table 47.4-2. Transmit Descriptor 1 (TDES1)**

| Bits    | Name                         | Description   |
|---------|------------------------------|---|
| [31:29] | SAIC: SA Insertion Control   | <p>These bits request the MAC to add or replace the Source Address field in the Ethernet frame with the value given in <a href="#">EMACADDROHIGH_REG</a>, <a href="#">EMACADDROLOW_REG</a>, <a href="#">EMACADDRHIGH_REG</a>, and <a href="#">EMACADDRLOW_REG</a>. If the Source Address field is modified in a frame, the MAC automatically recalculates and replaces the CRC bytes. The Bit[31] specifies the MAC Address Register value (1 or 0) that is used for Source Address insertion or replacement. The following list describes the values of Bits[30:29]:</p> <ul style="list-style-type: none"> <li>• 00: Do not include the source address.</li> <li>• 01: Include or insert the source address. For reliable transmission, the application must provide frames without source addresses.</li> <li>• 10: Replace the source address. For reliable transmission, the application must provide frames with source addresses.</li> <li>• 11: Reserved.</li> </ul> <p>These bits are valid when the First Segment control bit (<a href="#">TDES0[28]</a>) is set.</p> |
| [28:16] | TBS2: Transmit Buffer2 Size  | These bits specify the transmit Buffer 2 size in bytes. This field is not valid if <a href="#">TDES0[20]</a> is set.  |
| [15:13] | Reserved                     | Reserved  |
| [12:0]  | TBS1: Transmit Buffer 1 Size | These bits indicate the data buffer byte size in bytes. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor, depending on the value of TCH ( <a href="#">TDES0[20]</a> ).  |

**Table 47.4-3. Transmit Descriptor 2 (TDES2)**

| Bits   | Name                     | Description   |
|--------|--------------------------|---|
| [31:0] | Buffer 1 Address Pointer | These bits indicate the physical address of Buffer 1. |

**Table 47.4-4. Transmit Descriptor 3 (TDES3)**

| Bits   | Name  | Description  |
|--------|---|--|
| [31:0] | Buffer2 Address Pointer (Next Descriptor Address) | These bits specify the physical address of Buffer 2 when a descriptor ring structure is used. If the Second Address Chained ( <a href="#">TDES0[20]</a> ) bit is set, this address specifies the physical memory where the Next Descriptor is present. |

Table 47.4-5. Transmit Descriptor 6 (TDES6)

| Bits   | Name                                | Description  |
|--------|-------------------------------------|--|
| [31:0] | TTSL: Transmit Frame Time Stamp Low | This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding transmit frame. This field has the timestamp only if the Last Segment (TDES0[29]) bit in the descriptor is set, and the Timestamp Status (TDES0[17]) bit is set. |

Table 47.4-6. Transmit Descriptor 7 (TDES7)

| Bits   | Name                                 | Description  |
|--------|--------------------------------------|--|
| [31:0] | TTSH: Transmit Frame Time Stamp High | This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field has the timestamp only if the Last Segment (TDES0[29]) bit in the descriptor is set, and the Timestamp Status (TDES0[17]) bit is set. |

47.4.3.2 Receive Descriptors

Figure 47.4-2 shows the structure of the receive descriptor linked list. Table 47.4-7 through Table 47.4-11 show the descriptions of each receive descriptor.

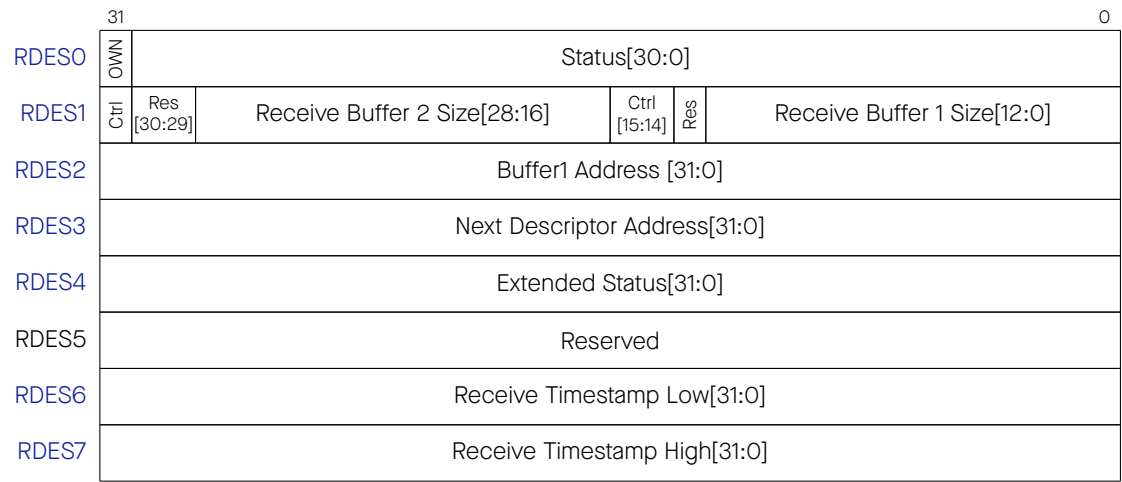


Figure 47.4-2. Receive Descriptor Linked List

Table 47.4-7. Receive Descriptor 0 (RDES0)

| Bits | Name         | Description  |
|------|--------------|--|
| [31] | OWN: Own Bit | When set, this bit indicates that the descriptor is owned by the DMA. When reset, it indicates that the descriptor is owned by the Host. The DMA clears this bit either when it completes the frame reception or when the buffers that are associated with this descriptor are full. |



| Bits    | Name                                 | Description  |
|---------|--------------------------------------|--|
| [30]    | AFM: Destination Address Filter Fail | When set, this bit indicates a frame that failed in the DA Filter in the MAC.  |
| [29:16] | FL: Frame Length                     | These bits indicate the byte length of the received frame that was transmitted to Host memory. This field is valid when Last Descriptor ( <a href="#">RDESO[8]</a> ) is set and either the Descriptor Error ( <a href="#">RDESO[14]</a> ) or Overflow Error bit <a href="#">RDESO[11]</a> are reset. The frame length also includes the two bytes appended to the Ethernet frame when IP checksum calculation (Type 1) is enabled and the received frame is not a MAC control frame.   |
| [15]    | ES: Error Summary                    | Indicates the logical OR of the following bits: <ul style="list-style-type: none"> <li>• <a href="#">RDESO[1]</a>: CRC Error</li> <li>• <a href="#">RDESO[3]</a>: Receive Error</li> <li>• <a href="#">RDESO[4]</a>: Watchdog Timeout</li> <li>• <a href="#">RDESO[6]</a>: Late Collision</li> <li>• <a href="#">RDESO[7]</a>: Giant Frame</li> <li>• <a href="#">RDES4[4:3]</a>: IP Header or Payload Error</li> <li>• <a href="#">RDESO[11]</a>: Overflow Error</li> <li>• <a href="#">RDESO[14]</a>: Descriptor Error</li> </ul> This field is valid only when <a href="#">RDESO[8]</a> is set. |
| [14]    | DE: Descriptor Error                 | When set, this bit indicates a frame truncation caused by a frame that does not fit within the current descriptor buffers, and that the DMA does not own the Next Descriptor. The frame is truncated. This field is valid only when This field is valid only when <a href="#">RDESO[8]</a> is set.   |
| [13]    | SAF: Source Address Filter Fail      | When set, this bit indicates that the SA field of frame failed the SA Filter in the MAC.   |
| [12]    | LE: Length Error                     | When set, this bit indicates that the actual length of the frame received and that the Length/Type field does not match. This bit is valid only when the Frame Type ( <a href="#">RDESO[5]</a> ) bit is reset.   |
| [11]    | OE: Overflow Error                   | When set, this bit indicates that the received frame was damaged because of buffer overflow in MTL.  |
| [10]    | VLAN: VLAN Tag                       | When set, this bit indicates that the frame pointed to by this descriptor is a VLAN frame tagged by the MAC. The VLAN tagging depends on checking the VLAN fields of the received frame based on the VLAN Tag Register) configuration.   |
| [9]     | FS: First Descriptor                 | When set, this bit indicates that this descriptor contains the first buffer of the frame. If the size of the first buffer is 0, the second buffer contains the beginning of the frame. If the size of the second buffer is also 0, the next Descriptor contains the beginning of the frame.  |
| [8]     | LS: Last Descriptor                  | When set, this bit indicates that the buffers pointed to by this descriptor are the last buffers of the frame.   |

| Bits | Name                                      | Description  |
|------|---|--|
| [7]  | IP Checksum Error (Type1), or Giant Frame | <p>When the Advanced Timestamp feature is present, and when this bit set, it indicates that a snapshot of the Timestamp is written in descriptor word 6 (<a href="#">RDES6</a>) and 7 (<a href="#">RDES7</a>). This is valid only when the Last Descriptor bit (<a href="#">RDES0[8]</a>) is set.</p> <p>When IP Checksum Engine (Type 1) is selected, this bit, if set, indicates one of the following:</p> <ul style="list-style-type: none"> <li>• The 16-bit IPv4 header checksum calculated by the core did not match the received checksum bytes.</li> <li>• The header checksum checking is bypassed for non-IPv4 frames.</li> </ul> <p>Otherwise, this bit, when set, indicates the Giant Frame Status. When normal frame processing is enabled, Giant frames are larger than 1,518 bytes (or 1,522 bytes for VLAN or 2,000 bytes when <a href="#">ASS2KP</a> is set). When Jumbo Frame processing is enabled, Giant frames are larger than 9,018 bytes (or 9,022 bytes for VLAN).</p> |
| [6]  | LC: Late Collision                        | When set, this bit indicates that a late collision has occurred while receiving the frame in the half-duplex mode.   |
| [5]  | FT: Frame Type                            | When set, this bit indicates that the Receive Frame is an Ethernet-type frame (the LT field is greater than, or equal to, 1,536 bytes). When reset, it indicates that the received frame is an IEEE 802.3 frame. This bit is not valid for Runt frames which are less than 14 bytes.   |
| [4]  | RWT: Receive Watchdog Timeout             | When set, this bit indicates that the Receive Watchdog Timer has expired while receiving the current frame and the current frame is truncated after the Watchdog Timeout.  |
| [3]  | RE: Receive Error                         | When set, this bit indicates that the MII_RXER signal is asserted while MII_RXDV is asserted during frame reception.   |
| [2]  | DE: Dribble Bit Error                     | When set, this bit indicates that the received frame has a non-integer multiple of bytes (odd nibbles). This bit is valid only in the MII Mode.  |
| [1]  | CE: CRC Error                             | When set, this bit indicates that a Cyclic Redundancy Check (CRC) Error occurred on the received frame. This field is valid only when the Last Descriptor ( <a href="#">RDES0[8]</a> ) is set.   |

| Bits | Name   | Description   |
|------|--|---|
| [0]  | Extended Status Available/<br>RX MAC Address | <p>When the IP Checksum Offload (Type 2) is present, this bit, when set, indicates that the extended status is available in descriptor word 4 (<a href="#">RDES4</a>). This is valid only when the Last Descriptor bit (<a href="#">RDES0[8]</a>) is set. This bit is invalid when Bit 30 is set.</p> <p>When IP Checksum Offload (Type 2) is present, this bit is set even when the IP Checksum Offload engine bypasses the processing of the received frame. The bypassing may be because of a non-IP frame or an IP frame with a non-TCP/UDP/ICMP payload.</p> <p>When the IPC Full Offload is not selected, this bit indicates an RX MAC Address status. When set, this bit indicates that the RX MAC Address registers value (1 to 15) matched the frame's DA field. When reset, this bit indicates that the RX MAC Address Register 0 value matched the DA field.</p> |

**Table 47.4-8. Receive Descriptor 1 (RDES1)**

| Bits    | Name                        | Description   |
|---------|-----------------------------|---|
| [31]    | Ctrl                        | When set, this bit prevents setting the Status Register's RI bit ( <a href="#">RECV_INT</a> ) for the received frame that ends in the buffer indicated by this descriptor. This, in turn, disables the assertion of the interrupt to Host because of the RI for that frame.   |
| [30:29] | Reserved                    | Reserved.   |
| [28:16] | RBS2: Receive Buffer 2 Size | These bits indicate the size of Buffer 2 in bytes. The buffer size must be a multiple of 4, even if the value of <a href="#">RDES3</a> (Buffer 2 address pointer) is not aligned to bus width. In the case where the buffer size is not a multiple of 4, the resulting behavior is undefined. This field is not valid if <a href="#">RDES1[14]</a> is set.  |
| [15]    | RER: Receive End of Ring    | When set, this bit indicates that the descriptor list reached its final descriptor. The DMA returns to the base address of the list, creating a Descriptor Ring.  |
| [14]    | RCH: Second Address Chained | When set, this bit indicates that the second address in the descriptor is the Next Descriptor address rather than the second buffer address. When this bit is set, RBS2 ( <a href="#">RDES1[28:16]</a> ) is a "don't care" value. <a href="#">RDES1[15]</a> takes precedence over <a href="#">RDES1[14]</a> .   |
| [13]    | Reserved                    | Reserved.   |
| [12:0]  | RBS1: Receive Buffer 1 Size | These bits indicate the size of Buffer 1 in bytes. The buffer size must be a multiple of 4, even if the value of <a href="#">RDES2</a> (buffer1 address pointer) is not aligned to bus width. When the buffer size is not a multiple of 4, the resulting behavior is undefined. If this field is 0, the DMA ignores this buffer and uses Buffer 2 or the next descriptor depending on the value of RCH (Bit[14]). |

**Table 47.4-9. Receive Descriptor 2 (RDES2)**

| Bits   | Name                     | Description   |
|--------|--------------------------|---|
| [31:0] | Buffer 1 Address Pointer | These bits indicate the physical address of Buffer 1. |

**Table 47.4-10. Receive Descriptor 3 (RDES3)**

| Bits   | Name  | Description  |
|--------|---|--|
| [31:0] | Buffer 2 Address Pointer<br>(Next Descriptor Address) | These bits indicate the physical address of Buffer 2 when descriptor chaining is used. If the Second Address Chained ( <a href="#">RDES1[14]</a> ) bit is set, then this address contains the pointer to the physical memory where the Next Descriptor is present. |

**Table 47.4-11. Receive Descriptor 4 (RDES4)**

| Bits    | Name              | Description   |
|---------|-------------------|---|
| [31:28] | Reserved          | Reserved.   |
| [27:26] | Reserved          | Reserved.   |
| [25]    | Reserved          | Reserved.   |
| [24]    | Reserved          | Reserved.   |
| [23:21] | Reserved          | Reserved.   |
| [20:18] | Reserved          | Reserved.   |
| [17]    | Reserved          | Reserved.   |
| [16]    | Reserved          | Reserved.   |
| [15]    | Reserved          | Reserved.   |
| [14]    | Timestamp Dropped | When set, this bit indicates that the timestamp was captured for the receive frame but got dropped in the MTL RX FIFO because of overflow.  |
| [13]    | PTP Version       | When set, this bit indicates that the received PTP message is having the IEEE 1588 version 2 format. When reset, it has the version 1 format.   |
| [12]    | PTP Frame Type    | When set, this bit indicates that the PTP message over Ethernet is sent directly over Ethernet. When this bit is not set and the MT (message type) is not 0, it indicates that the PTP message over UDP-IPv4 or UDP-IPv6 is received. |

| Bits   | Name                 | Description   |
|--------|----------------------|---|
| [11:8] | Message Type         | <p>These bits are encoded to give the type of the message received.</p> <ul style="list-style-type: none"> <li>• 0000: Reserved</li> <li>• 0001: SYNC (all clock types)</li> <li>• 0010: Follow_Up (all clock types)</li> <li>• 0011: Delay_Req (all clock types)</li> <li>• 0100: Delay_Resp (all clock types)</li> <li>• 0101: Pdelay_Req (in peer-to-peer transparent clock)</li> <li>• 0110: Pdelay_Resp (in peer-to-peer transparent clock)</li> <li>• 0111: Pdelay_Resp_Follow_Up (in peer-to-peer transparent clock)</li> <li>• 1000: Announce</li> <li>• 1001: Management</li> <li>• 1010: Signaling</li> <li>• 1011-1110: Reserved</li> <li>• 1111: PTP packet with Reserved message type</li> </ul> |
| [7]    | IPv6 Packet Received | When set, this bit indicates that the received packet is an IPv6 packet. This bit is updated only when Bit[10] (IPC) of MAC Configuration Register ( <a href="#">EMACRXIPCOFFLOAD</a> ) is set.   |
| [6]    | IPv4 Packet Received | When set, this bit indicates that the received packet is an IPv4 packet. This bit is updated only when Bit[10] (IPC) of MAC Configuration Register ( <a href="#">EMACRXIPCOFFLOAD</a> ) is set.   |
| [5]    | IP Checksum Bypassed | When set, this bit indicates that the checksum offload engine is bypassed.  |
| [4]    | IP Payload Error     | When set, this bit indicates that the 16-bit IP payload checksum (that is, the TCP, UDP, or ICMP checksum) that the MAC core calculated does not match the corresponding checksum field in the received segment. It is also set when the TCP, UDP, or ICMP segment length does not match the payload length value in the IP Header field. This bit is valid when either Bit[7] or Bit[6] is set.  |
| [3]    | IP Header Error      | When set, this bit indicates that either the 16-bit IPv4 header checksum calculated by the MAC core does not match the received checksum bytes, or the IP datagram version is not consistent with the Ethernet Type value. This bit is valid when either Bit[7] or Bit[6] is set.   |

| Bits  | Name            | Description   |
|-------|-----------------|---|
| [2:0] | IP Payload Type | <p>These bits indicate the type of payload encapsulated in the IP datagram processed by the Receive Checksum Offload Engine (COE). The COE also sets these bits to 00 if it does not process the IP datagram's payload due to an IP header error or fragmented IP.</p> <ul style="list-style-type: none"> <li>• 000: Unknown or did not process IP payload</li> <li>• 001: UDP</li> <li>• 010: TCP</li> <li>• 011: ICMP</li> <li>• 1xx: Reserved</li> </ul> <p>This bit is valid when either Bit[7] or Bit[6] is set.</p> |

**Table 47.4-12. Receive Descriptor 6 (RDES6)**

| Bits   | Name                               | Description   |
|--------|------------------------------------|---|
| [31:0] | RTSH: Receive Frame Time Stamp Low | <p>This field is updated by DMA with the least significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by the Last Descriptor status bit (<a href="#">RDES0[8]</a>).</p> |

**Table 47.4-13. Receive Descriptor 7 (RDES7)**

| Bits   | Name                               | Description  |
|--------|------------------------------------|--|
| [31:0] | RTSH: Receive Frame Timestamp High | <p>This field is updated by DMA with the most significant 32 bits of the timestamp captured for the corresponding receive frame. This field is updated by DMA only for the last descriptor of the receive frame which is indicated by the Last Descriptor status bit (<a href="#">RDES0[8]</a>).</p> |

## 47.4.4 PHY Interface

The MAC and the external PHY communicate through two interfaces:

- Media Independent Interface (MII)
- Reduced Media Independent Interface (RMII)

### 47.4.4.1 Media Independent Interface: MII

The Media Independent Interface (MII) defines the interconnection between MAC sublayers and PHYs at 10 Mbit/s and 100 Mbit/s.

#### MII Signals to PHY

The MII interface signals are shown in Figure [47.4-3](#).

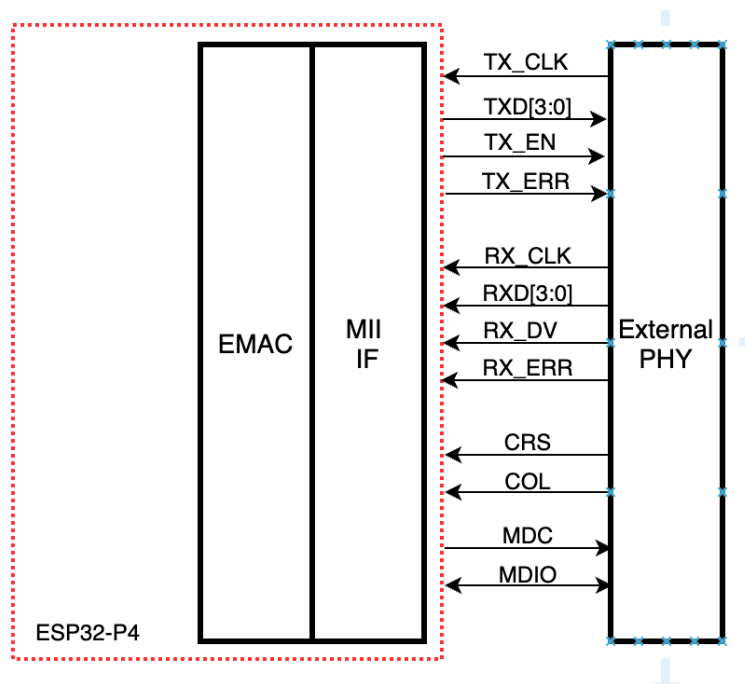


Figure 47.4-3. MII Interface

The MII interface signals are described below:

- **MII\_TX\_CLK**: TX clock signal. This signal provides the reference timing for TX data transmission. It has two frequencies: 2.5 MHz at 10 Mbit/s, and 25 MHz at 100 Mbit/s.
- **MII\_TXD[3:0]**: A bundle of four transmit data signals driven by the MAC sublayer, and qualified (valid data) on the assertion of the MII\_TX\_EN signal. MII\_TXD[0] is the lowest significant bit and MII\_TXD[3] is the highest significant bit. When the MII\_TX\_EN signal is deasserted, the transmit data have no effect on the PHY.
- **MII\_TX\_EN**: Transmission enable signal. This signal indicates that the MAC is presenting nibbles (4 bits) on the MII for transmission. It must be asserted synchronously (MII\_TX\_CLK) with the first nibble of the preamble and must remain asserted while all nibbles to be transmitted are presented to the MII.
- **MII\_TX\_ERR**: Transmit error signal. The signal must be asserted for one or more clock periods (MII\_TX\_CLK) to indicate to the PHY layer that an error was detected somewhere in the frame.
- **MII\_RX\_CLK**: RX clock signal. This signal provides the reference timing for RX data transmission. It has two frequencies: 2.5 MHz at 10 Mbit/s, and 25 MHz at 100 Mbit/s.
- **MII\_RXD[3:0]**: A bundle of four receive data signals driven by the MAC sublayer, and qualified (valid data) on the assertion of the MII\_RX\_DV signal. MII\_RXD[0] is the lowest significant bit and MII\_RXD[3] is the highest significant bit. When MII\_RX\_DV is deasserted and MII\_RX\_ERR is asserted, a specific MII\_RXD[3:0] value is used to transfer specific information from the PHY.
- **MII\_RX\_DV**: Receive data valid signal. This signal indicates that the PHY is presenting recovered and decoded nibbles on the MII for reception. It must be asserted synchronously (MII\_RX\_CLK) with the first recovered nibble of the frame and must remain asserted through the final recovered nibble. It must be deasserted prior to the first clock cycle that follows the final nibble. In order to receive the frame correctly, the MII\_RX\_DV signal must encompass the frame, starting no later than the SFD field.

- MII\_CRS: Carrier sense signal. When the transmit or receive medium is non-idle, the signal is asserted by the PHY. When the transmit or receive medium is idle, the signal is deasserted by the PHY. The PHY must ensure that the MII\_CRS signal remains asserted throughout the duration of a collision condition. This signal does not need to be synchronized with the TX and RX clocks. In full duplex mode the state of this signal is don't care for the MAC sublayer.
- MII\_COL: Collision detection signal. This signal must be asserted by the PHY upon detection of a collision on the medium and must remain asserted while the collision condition persists. This signal is not required to transition synchronously with respect to the TX and RX clocks. In full duplex mode, the state of this signal is don't care for the MAC sublayer.
- MII\_RX\_ERR: Receive error signal. The signal must be asserted for one or more clock periods (MII\_RX\_CLK) to indicate to the MAC sublayer that an error was detected somewhere in the frame.
- MDIO and MDC: Management data input/output and management data clock signal. The two signals constitute a serial bus defined for the Ethernet family of IEEE 802.3 standards, used to transfer control and data information to the PHY, see section [Station Management Agent \(SMA\) Interface](#).

### MII Clock

In MII mode, there are clock signals in two directions between MII and the PHY, namely `clk_tx` and `clk_rx`. `clk_tx` is used to synchronize the TX data, and `clk_rx` is used to synchronize the RX data. Both clocks are provided by the PHY.

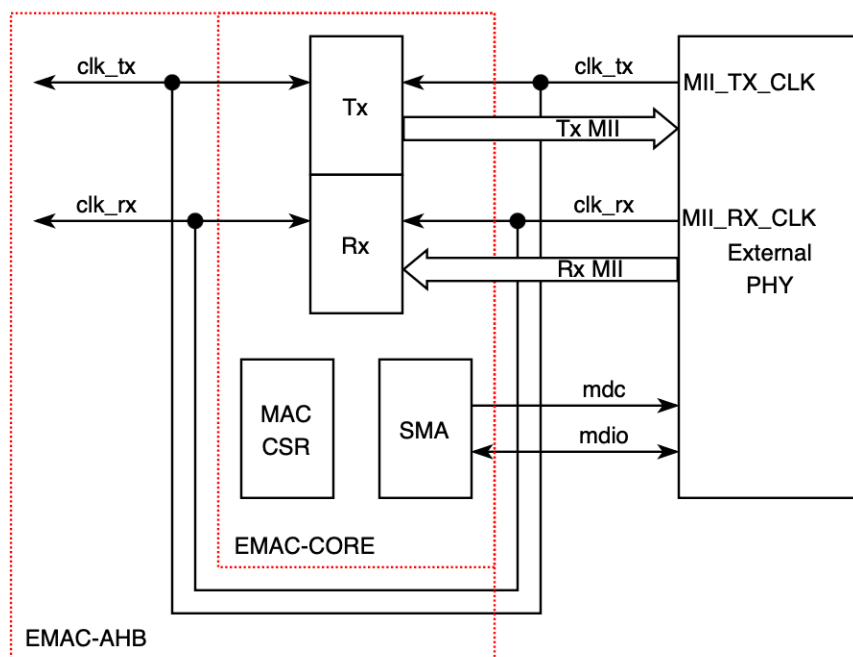


Figure 47.4-4. MII Clock

#### 47.4.4.2 Reduced Media Independent Interface: RMII

RMII interface signals are shown in Figure 47.4-5.



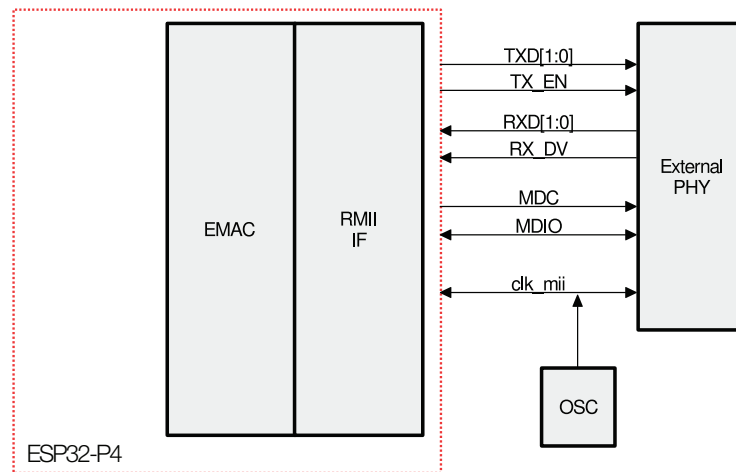


Figure 47.4-5. RMII Interface

### RMII Signals

The Reduced Media Independent Interface (RMII) specification reduces the number of pins between the microcontroller's Ethernet MAC and the external PHY at 10 Mbit/s or 100 Mbit/s. According to the IEEE 802.3u standard, an MII contains 16 pins for data and control. The RMII specification reduces the pin count to 7.

RMII has the following features:

- Supports an operating rate of 10 Mbit/s or 100 Mbit/s
- The clock reference must be 50 MHz.
- The same clock reference must be sourced externally both to the MAC and the external Ethernet PHY.
- Provides independent 2-bit wide TX and RX data paths.

### RMII Clock

The 50 MHz RMII reference clock can be:

- Generated internally by ESP32-P4 and looped back via GPIOs. For GPIO configurations, please refer to [Chapter 8 GPIO Matrix and IO MUX](#).
- Provided by the external crystal and obtained at GPIOs.

The RMII clock is shown in [Figure 47.4-6](#).

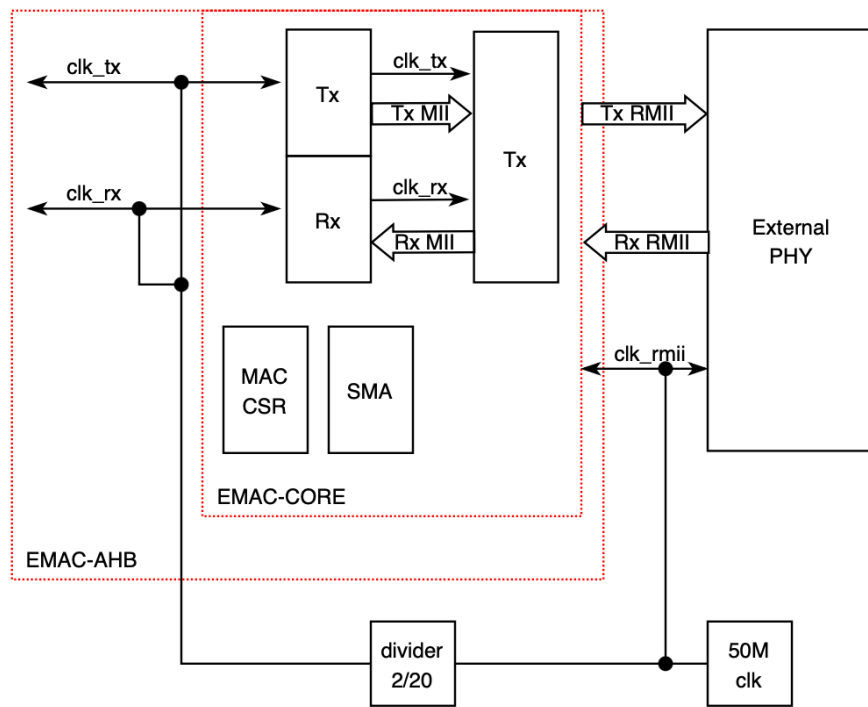


Figure 47.4-6. RMII Clock

#### 47.4.4.3 Station Management Agent (SMA) Interface

As Figure 47.4-3 and Figure 47.4-5 show, the MAC uses MDC and MDIO signals to transfer control and data information to the PHY. The MDC clock signal is generated from the application clock by a clock divider at the maximum frequency of 2.5 MHz. The MDIO data signal transfers to and fro PHY synchronously with the MDC clock signal. Meanwhile, the PHY transmits register data.

- Read a PHY register:
  - Read [MIIBUSY](#) until the MII is in an idle state.
  - Configure [MIIDEV](#) to specify the PHY device to access.
  - Configure [MIIREG](#) to specify the address of the PHY register to access.
  - Configure [MIICSRCLK](#) to set the APB clock frequency.
  - Set [MIIWRITE](#) to 0 for read access.
  - Read [MIIBUSY](#) until the MII is in an idle state.
  - Read [EMACMIIDATA\\_REG](#) to retrieve the value of the PHY register.
- Write a PHY register:
  - Read [MIIBUSY](#) until the MII is in an idle state.
  - Configure [EMACMIIDATA\\_REG](#) to set the value to be written to the PHY register.
  - Configure [MIIDEV](#) to specify the PHY device to access.
  - Configure [MIIREG](#) to specify the address of the PHY register to access.
  - Configure [MIICSRCLK](#) to set the APB clock frequency.

- Set [MIWRITE](#) to 1 for write access.
- Read [MIIBUSY](#) until the MII is in an idle state, which indicates the completion of the write operation.

## 47.4.5 MAC Address Filtering

Address filtering checks the destination and source addresses on all received frames and reports the address filtering status accordingly. Address checking is based on different parameters (Frame filter register) chosen by the application. The filtered frame can also be identified: multicast or broadcast frame. Address filtering uses the station's physical (MAC) address for address checking.

### 47.4.5.1 Unicast Destination Address Filtering

The MAC supports up to 9 MAC addresses for unicast perfect filtering. MAC compares all 48 bits of the received unicast address with the programmed MAC address for any match. By default, [EMACADDR0](#) is always enabled, and the other addresses ([EMACADDR0](#) ~ [EMACADDR8](#)) are selected with an individual enable bit. Each byte of these other addresses ([EMACADDR0](#) ~ [EMACADDR8](#)) can be masked during comparison with the corresponding received DA byte by setting the corresponding Mask Byte Control bit in the register. This helps group address filtering for the DA.

### 47.4.5.2 Multicast Destination Address Filtering

The MAC can be programmed to pass all multicast frames by setting the Pass All Multicast ([PAM](#)) bit in the Frame Filter Register to 1. If the [PAM](#) bit is reset, the MAC the filtering for multicast addresses.

In perfect filtering mode, the multicast address is compared with the programmed MAC Destination Address Registers ([EMACADDR0](#) ~ [EMACADDR8](#)). Group address filtering is also supported.

### 47.4.5.3 Broadcast Address Filter

The MAC does not filter any broadcast frames in the default mode. However, if the MAC is programmed to reject all broadcast frames by setting the Disable Broadcast Frames ([DBF](#)) bit in the Frame Filter Register to 1, all broadcast frames will be dropped.

### 47.4.5.4 Unicast Source Address Filter

The MAC can also perform perfect filtering based on the source address field of the received frames. By default, the Address Filtering Module (AFM) compares the Source Address (SA) field with the values programmed in the SA register. The MAC address registers [1:3] can be configured to contain SA instead of DA for comparison, by setting bit[30] in the corresponding register. Group filtering with SA is also supported. The frames that fail the SA filter are dropped by the MAC if the Source Address Filter Enable ([SAFE](#)) bit in the Frame filter register is set. Otherwise, the result of the SA filter is given as a status bit in the Receive Status word (see Table 47.4-7).

When the [SAFE](#) bit is set to 1, the result of the SA filtering and DA filtering is AND'ed to decide whether the frame needs to be forwarded. This means that either of the filter failure results will drop the frame. Both filters have to pass the frame for the frame to be forwarded to the application.

#### 47.4.5.5 Inverse Filtering Operation

For both destination and source address filtering, there is an option to invert the filter-match result at the final output. These are controlled by the **DAIF** and **SAIF** bits in the Frame filter register, respectively. The **DAIF** bit is applicable for both Unicast and Multicast DA frames. When the **DAIF** bit is set, the result of the unicast/multicast destination address filter is inverted. Similarly, when the **SAIF** bit is set, the result of the unicast SA filter is inverted.

The following two tables summarize the destination address and source address filtering based on the type of the frames received.

**Table 47.4-14. Destination Address Filtering**

| Frame Type | PM | PF | DAIF | PAM | DB | DA Filter Operation   |
|------------|----|----|------|-----|----|---|
| Broadcast  | 1  | X  | X    | X   | X  | Pass  |
|            | 0  | X  | X    | X   | 0  | Pass  |
|            | 0  | X  | X    | X   | 1  | Fail  |
| Unicast    | 1  | X  | X    | X   | X  | Pass all frames   |
|            | 0  | X  | 0    | X   | X  | Pass on perfect/group filter match  |
|            | 0  | X  | 1    | X   | X  | Fail on perfect/group filter match  |
|            | 0  | 1  | 0    | X   | X  | Pass on perfect/group filter match  |
|            | 0  | 1  | 1    | X   | X  | Fail on perfect/group filter match  |
| Multicast  | 1  | X  | X    | X   | X  | Pass all frames   |
|            | X  | X  | X    | 1   | X  | Pass all frames   |
|            | 0  | X  | 0    | 0   | X  | Pass on perfect/group filter match and drop pause control frames if PCF = 0x. |
|            | 0  | 1  | 0    | 0   | X  | Pass on perfect/group filter match and drop pause control frames if PCF = 0x. |
|            | 0  | X  | 1    | 0   | X  | Fail on perfect/group filter match and drop pause control frames if PCF = 0x. |
|            | 0  | 1  | 1    | 0   | X  | Fail on perfect/group filter match and drop pause control frames if PCF = 0x. |

The filtering parameters in the MAC Frame Filter Register described in Table 47.4-14 are as follows.

| Parameter name                              | Parameter setting |
|---|-------------------|
| PM: Pass All Multicast                      | 1: Set            |
| PF: Perfect Filter                          | 0: Cleared        |
| DAIF: Destination Address Inverse Filtering | X: Don't care     |
| PAM: Pass All Multicast                     |                   |
| DB: Disable Broadcast Frames                |                   |

**Table 47.4-15. Source Address Filtering**

| Frame Type | PM | SAIF | SAF | Source Address Filter Operation                                     |
|------------|----|------|-----|---|
| Unicast    | 1  | X    | X   | Pass all frames   |
|            | 0  | 0    | 0   | Pass on perfect/group filter match but do not drop frames that fail |
|            | 0  | 0    | 0   | Fail on perfect/group filter match but do not drop frames that fail |
|            | 0  | 0    | 0   | Pass on perfect/group filter match and drop frames that fail        |
|            | 0  | 0    | 0   | Fail on perfect/group filter match and drop frames that fail        |

The filtering parameters in the MAC Frame Filter Register described in Table 47.4-15 are as follows.

| Parameter name                         | Parameter setting |
|--|-------------------|
| PM: Pass All Multicast                 | 1: Set            |
| SAF: Source Address Filtering          | 0: Cleared        |
| SAIF: Source Address Inverse Filtering | X: Don't care     |

## 47.4.6 Energy Efficient Ethernet (EEE)

Energy Efficient Ethernet (EEE) is an optional operating mode that enables the MAC sublayer along with a series of physical layers to operate in the Low Power Idle (LPI) mode. The EEE mode supports 100 Mbps MAC operations compliant with the IEEE 802.3az-2010 standard. The EEE is supported only in the full-duplex mode when MAC uses MII.

The LPI mode allows power saving by switching off parts of the communication device functionality when there is no data to be transmitted and received. The system on both sides of the link can disable some functionalities and save power during the period of low-link utilization. The MAC controls whether the system should enter or exit the LPI mode and communicate this to the PHY.

### 47.4.6.1 Transmission

To enter the LPI mode, the software must set the [LPIEN](#) bit to indicate to the MAC to stop transmission and initiate the LPI protocol. The MAC completes the transmission in progress, generates its transmission status, and then starts transmitting the LPI pattern instead of the IDLE pattern during the Interframe gap (IFG). The MAC then updates [TLPIEN](#) and generates an interrupt.

To exit the LPI mode, the software must clear the [LPIEN](#) bit to indicate to the MAC. The MAC stops transmitting the LPI pattern, and starts transmitting the IDLE pattern. When the [LPI\\_TW\\_TIMER](#) expires, the MAC updates [TLPIEX](#) and generates an interrupt.

### 47.4.6.2 Reception

When the PHY receives the signals from the link partner to enter into the LPI state, the PHY starts transmitting the LPI pattern. The MAC updates [RLPIEN](#) and generates an interrupt.

When the PHY receives signals from the link partner to exit the LPI state, the PHY stops transmitting the LPI pattern. The MAC updates [RLPIEX](#) and generates an interrupt.

## 47.4.7 Source Address, VLAN, and CRC Control

### 47.4.7.1 Source Address Control

The software can enable source address insertion or replacement for all or some frames:

- Enable source address insertion or replacement for all frames by configuring [SAIRC](#).
- Enable source address insertion or replacement for the current frame by configuring [TDES1\[31:29\]](#) of the frame. When [TDES1\[31\]](#) is set, [MAC\\_ADDRESS1\\_HI](#) and [EMACADDR1LOW\\_REG](#) are used for insertion and replacement. When [TDES1\[31\]](#) is cleared, [MAC\\_ADDRESS0\\_HI](#) and [EMACADDR0LOW\\_REG](#) are used for insertion and replacement. When [ADDRESS\\_ENABLE1](#) is not set, [MAC\\_ADDRESS0\\_HI](#) and [EMACADDR0LOW\\_REG](#) are used for insertion and replacement irrespective of [TDES1\[31\]](#).

### 47.4.7.2 VLAN Control

The software can enable VLAN insertion, replacement, or deletion for all or some frames:

- Enable VLAN insertion, replacement, or deletion for all frames by configuring [VLC](#).
- Enable VLAN insertion, replacement, or deletion for the current frame by configuring [TDES0\[19:18\]](#) of the frame.

### 47.4.7.3 CRC Control

CRC replacement is a feature that the software can use to indicate the MAC to replace the FCS field of the frame being transmitted with the calculated CRC. This feature can be enabled for the current frame by configuring [TDES0\[24\]](#).

CRC replacement is valid only when MAC does not append CRC ([TDES0\[27\]](#) is set), i.e., when FCS is provided by software in frames transmitted. If source address or VLAN control is enabled, the MAC will replace or append FCS fields with CRC when [TDES0\[27\]](#) is set or cleared respectively.

## 47.4.8 Time Stamp

The IEEE 1588-2008 standard defines the Precision Time Protocol (PTP) that allows precise clock synchronization in measurement and control systems implemented with technologies such as local computing, network communication and distributed objects. It supports system-wide synchronization accuracy in the sub-microsecond range with a minimum network and local clock computing resources.

### 47.4.8.1 Transmit Path

The MAC captures a timestamp when the start-of-frame data (SFD) is sent on the MII interface. The frames for which timestamps are captured can be controlled on a per-frame basis. In other words, each transmit frame can be marked to indicate whether a timestamp should be captured for that frame. The MAC does not process the transmitted to identify PTP frames. Rather, it captures the timestamp or not according to the configurations of [TDES0\[25\]](#) by software. The MAC returns the timestamp to the software inside the corresponding transmit descriptor, thus connecting the timestamp automatically to the specific PTP frame. The 64-bit timestamp information is written to the [TDES6](#) and [TDES7](#) fields.

### 47.4.8.2 Receive Path

The MAC processes the received frames to identify valid PTP frames. The snapshot of the time to be sent to the application can be controlled by software via [EMACTSTPCTRL\\_REG](#).

The MAC returns the timestamp to the software inside the corresponding receive descriptor. The extended status (including the timestamp status and IPC status) is written to [RDES4](#), and the timestamp snapshot is written to [RDES6](#) and [RDES7](#).

### 47.4.9 Remote Wakeup

The MAC supports remote wakeup. When the receiver receives a remote wakeup frame or a magic packet, an interrupt will be triggered, and the PMU will be notified to wake up the SoC system.

The software can control whether to use remote wakeup frames to trigger interrupts by configuring [RWKPKTEN](#), whether to use magic packets to trigger interrupts by configuring [MGKPKTEN](#), and whether the MAC drops all received frames in power-down mode by configuring [PWRDWN](#).

### 47.4.10 Good Transmitted and Received Frames

A frame that has been successfully transmitted is considered a “good frame”. In other words, a transmitted frame is considered to be “good”, if the frame transmission is not aborted due to the following errors:

- Jabber timeout ([TDES0\[14\]](#))
- No carrier or loss of carrier ([TDES0\[11:10\]](#))
- Late collision ([TDES0\[9\]](#))
- Frame underflow ([TDES0\[1\]](#))
- Excessive deferral ([TDES0\[2\]](#))
- Excessive collision ([TDES0\[8\]](#))

A received frame is considered to be “good” if the following errors do not occur:

- CRC error ([RDES0\[1\]](#))
- Runt frames (frames shorter than 64 bytes)
- Alignment error (in 10/100 Mbps modes only) ([RDES0\[2\]](#))
- Length error (non-type frames only) ([RDES0\[12\]](#))
- Frame size over the maximum size (for non-type frames over the maximum frame size only) ([RDES0\[7\]](#))
- MII\_RXER input error ([RDES0\[3\]](#))

The maximum frame size depends on the frame type:

- The maximum size of untagged frames = 1518 bytes
- The maximum size of VLAN frames = 1522 bytes

## 47.5 Programming Procedures

### 47.5.1 MAC System Layer Configuration

1. Configure the IO interfaces. For detailed configurations about the MII and the RMII interface, see Chapter [8 GPIO Matrix and IO MUX](#).

2. Configure the EMAC system clock by setting [HP\\_SYS\\_CLKRST\\_EMAC\\_SYS\\_CLK\\_EN](#) to 1.
3. Configure the PHY interface clock:
  - RMII interface: select the RMII interface by configuring [HP\\_SYS\\_PHY\\_INTF\\_SEL](#) to 4.
    - Select RMII reference clock source:
      - \* Reference clock sourced from the external crystal:
        - Configure [HP\\_SYS\\_CLKRST\\_PAD\\_EMAC\\_REF\\_CLK\\_EN](#) to disable [PAD\\_EMAC\\_REF\\_CLK](#) outputted to GPIO.
        - Configure [HP\\_SYS\\_CLKRST\\_REF\\_50M\\_CLK\\_EN](#) to disable [PLL\\_F50M\\_CLK](#).
      - \* Reference clock sourced from ESP32-P4:
        - Configure [HP\\_SYS\\_CLKRST\\_PAD\\_EMAC\\_REF\\_CLK\\_EN](#) to enable [PAD\\_EMAC\\_REF\\_CLK](#) outputted to GPIO.
        - Configure [HP\\_SYS\\_CLKRST\\_REF\\_50M\\_CLK\\_DIV\\_NUM](#) to specify the clock divisor for [PLL\\_F50M\\_CLK](#).
        - Configure [HP\\_SYS\\_CLKRST\\_REF\\_50M\\_CLK\\_EN](#) to enable [PLL\\_F50M\\_CLK](#).
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RMII\\_CLK\\_SRC\\_SEL](#) to specify the clock source of [EMAC\\_RMII\\_CLK](#) as [PAD\\_EMAC\\_TXRX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_SRC\\_SEL](#) to specify the clock source of [EMAC\\_RX\\_CLK](#) as [PAD\\_EMAC\\_TXRX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_DIV\\_NUM](#) to specify the clock divisor for [EMAC\\_RX\\_CLK](#) according to the EMAC line speed (10 Mbit/s or 100 Mbit/s);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_SRC\\_SEL](#) to specify the clock source of [EMAC\\_TX\\_CLK](#) as [PAD\\_EMAC\\_TXRX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_DIV\\_NUM](#) to specify the clock divisor for [EMAC\\_TX\\_CLK](#) according to the EMAC line speed (10 Mbit/s or 100 Mbit/s);
    - Configure [LP\\_AONCLKRST\\_HP\\_PAD\\_EMAC\\_TXRX\\_CLK\\_EN](#) to enable the clock from IO pin [PAD\\_EMAC\\_TXRX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RMII\\_CLK\\_EN](#) to enable [EMAC\\_RMII\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_EN](#) to enable [EMAC\\_RX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_EN](#) to enable [EMAC\\_TX\\_CLK](#);
  - MII interface: select the MII interface by configuring [HP\\_SYS\\_PHY\\_INTF\\_SEL](#) to 0.
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_SRC\\_SEL](#) to specify [EMAC\\_RX\\_CLK](#) as [PAD\\_EMAC\\_RX\\_CLK](#);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_DIV\\_NUM](#) to specify the clock divisor for [EMAC\\_RX\\_CLK](#) according to the EMAC line speed (10 Mbit/s or 100 Mbit/s);
    - Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_SRC\\_SEL](#) to specify [EMAC\\_TX\\_CLK](#) as [PAD\\_EMAC\\_TX\\_CLK](#);



- Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_DIV\\_NUM](#) to specify the clock divisor for EMAC\_TX\_CLK according to the EMAC line speed (10 Mbit/s or 100 Mbit/s);
- Configure [LP\\_AONCLKRST\\_HP\\_PAD\\_EMAC\\_RX\\_CLK\\_EN](#) to enable the clock from IO pin PAD\_EMAC\_RX\_CLK;
- Configure [LP\\_AONCLKRST\\_HP\\_PAD\\_EMAC\\_TX\\_CLK\\_EN](#) to enable the clock from IO pin PAD\_EMAC\_TX\_CLK;
- Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_RX\\_CLK\\_EN](#) to enable EMAC\_RX\_CLK;
- Configure [HP\\_SYS\\_CLKRST\\_EMAC\\_TX\\_CLK\\_EN](#) to enable EMAC\_TX\_CLK;

## 47.5.2 EMAC Initial Configuration

Initialize EMAC\_DMA:

- Reset EMAC by setting [SW\\_RST](#) to 1.
- Wait for the completion of reset until reading 0 from [SW\\_RST](#), which indicates that the reset is done.
- Read [AHB\\_ST](#); a value of 0 indicates that all AHB bus transactions have been completed.
- Configure the AHB bus mode for EMAC\_DMA via [DMABUSMODE\\_REG](#).
- Prepare the linked list and configure the linked list base address via [DMARXBASEADDR\\_REG](#) and [DMATXBASEADDR\\_REG](#).
- Configure the operating mode for EMAC\_DMA and EMAC\_MTL via [DMAOPERATION\\_MODE\\_REG](#).
- Configure whether to enable DMA interrupts via [DMAIN\\_EN\\_REG](#).

Initialize EMAC\_CORE:

- Read [EMACMIADDR\\_REG](#) and [EMACMIIDATA\\_REG](#) for the PHY's connection status, operating frequency, and operating mode.
- Configure [EMACADDROHIGH\\_REG](#) and [EMACADDROLOW\\_REG](#) to specify the MAC address.
- Configure [EMACFF\\_REG](#) to select the packet filtering mode.
- Configure [EMACFC\\_REG](#) for flow control.
- Configure whether to mask MAC interrupts via [EMACINTMASK\\_REG](#).
- Configure the MAC's operating mode for transmission and reception via [EMACCONFIG\\_REG](#).

## 47.5.3 Starting Transmission

- Start EMAC\_DMA transmission by setting [START\\_STOP\\_TRANSMISSION\\_COMMAND](#) to 1.
- Start EMAC\_CORE transmission by setting [EMACTX](#) to 1.
- Detect the TRANS\_INT interrupt if enabled, and wait for the frame transmission to complete.

## 47.5.4 Starting Reception

- Start EMAC\_DMA reception by setting [START\\_STOP\\_RX](#) to 1.

- Start EMAC\_CORE reception by setting [EMACRX](#) to 1.
- Detect the RECV\_INT interrupt if enabled, and wait for the frame reception to complete.

### 47.5.5 TX Entering and Exiting the LPI State

- Configure the LPI timer counter via [EMACLPITIMERSCONTROL\\_REG](#)
- Make the transmitter to enter the LPI state via [EMACLPI\\_CSR\\_REG](#)
- Detect the LPI\_INT interrupt, and wait for [TLPIEN](#) to be set, which indicates that the transmitter has entered the LPI state
- Bring the transmitter out of the LPI state by clearing [LPIEN](#)
- Detect the LPI\_INT interrupt, and wait for [TLPIEX](#) to be set, which indicates that the transmitter has exited the LPI state

### 47.5.6 RX Entering and Exiting the LPI State

- Detect the LPI\_INT interrupt, and wait for [RLPIEN](#) to be set, which indicates that the receiver has entered the LPI state
- Detect the LPI\_INT interrupt, and wait for [RLPIEX](#) to be set, which indicates that the receiver has exited the LPI state

## 47.6 Interrupts

ESP32-P4's EMAC can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- ETH\_MAC\_INTR
- PMT\_INTR
- LPT\_INTR

There are several internal interrupt sources from EMAC that can generate the above interrupt signals.

The following interrupt sources can generate the ETH\_MAC\_INTR interrupt signal:

- [ABN\\_INT\\_SUMM](#): Triggered when [DMAIN\\_AISE](#) is 1 and the following interrupts are triggered.
  - [TRANS\\_PROC\\_STOP](#): Triggered when [DMAIN\\_TSE](#) is 1 and the transmit process stops.
  - [TRANS\\_JABBER\\_TO](#): Triggered when [DMAIN\\_TJTE](#) is 1 and the frame size exceeds 2048 bytes (10240 bytes if the jumbo frame is enabled).
  - [RECV\\_OVERFLOW](#): Triggered when [DMAIN\\_OIE](#) is 1 and the receive buffer overflows during frame reception.
  - [TRANS\\_UNDFLOW](#): Triggered when [DMAIN\\_UIE](#) is 1 and the transmit buffer underflows during frame transmission.
  - [RECV\\_BUF\\_UNAVAIL](#): Triggered when [DMAIN\\_RBUE](#) is 1, the Host owns the Next Descriptor in the Receive List and the DMA cannot acquire it.
  - [RECV\\_PROC\\_STOP](#): Triggered when [DMAIN\\_RSE](#) is 1 and the receive process stops.

- [RECV\\_WDT\\_TO](#): Triggered when [DMAIN\\_RWTE](#) is 1 and the Receive Watchdog Timer has expired while receiving the current frame.
- [EARLY\\_TRANS\\_INT](#): Triggered when [DMAIN\\_ETIE](#) is 1 and the frame has been completely transmitted to MTL TX FIFO.
- [FATAL\\_BUS\\_ERR\\_INT](#): Triggered when [DMAIN\\_FBEE](#) is 1 and a bus error described in [ERROR\\_BITS](#) occurs.
- [NORM\\_INT\\_SUMM](#): Triggered when [DMAIN\\_NISE](#) is 1 and the following interrupts are triggered.
  - [TRANS\\_INT](#): Triggered when [DMAIN\\_TIE](#) is 1 and the transmission completes.
  - [TRANS\\_BUF\\_UNAVAIL](#): Triggered when [DMAIN\\_TBUE](#) is 1, the Host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it.
  - [RECV\\_INT](#): Triggered when [DMAIN\\_RIE](#) is 1 and the frame has been received.
  - [EARLY\\_RECV\\_INT](#): Triggered when [DMAIN\\_ERIE](#) is 1 and the DMA has received the first buffer of the data packet.

[EMAC\\_PMT\\_INT](#): Triggered when [PMTINTMASK](#) is 0, and a magic packet or a remote wakeup frame has been received in power-down mode.

[TS\\_TRI\\_INT](#): Triggered when [TSINTMASK](#) is 0 and any of the following conditions is true:

- The system time value equals or exceeds the value specified in the Target Time registers
- There is an overflow in the System Time Seconds Register

[EMAC\\_LPI\\_INT](#): Triggered when [LPIINTMASK](#) is 0 and any of the following conditions is true:

- The MAC Transmitter enters the LPI state
- The MAC Transmitter exits the LPI state
- The MAC Receiver enters the LPI state
- The MAC Receiver exits the LPI state

The following interrupt sources can generate the [PMT\\_INTR](#) interrupt signal:

- [RWKPRCVD](#): Triggered when a remote wakeup frame is received.
- [MGKPRCVD](#): Triggered when a magic packet is received.

The following interrupt source can generate the [LPI\\_INTR](#) interrupt signal:

- [RLPIEX](#): Triggered when the MAC receiver has stopped receiving the LPI pattern on PHY and has exited the LPI state.

## 47.7 Register Summary

The addresses in this section are relative to EMAC base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name   | Description                                       | Address | Access  |
|--|---|---------|---------|
| <b>DMA configuration and control registers</b> |   |         |         |
| <a href="#">DMABUSMODE_REG</a>                 | Bus mode register                                 | 0x1000  | R/WS/SC |
| <a href="#">DMATXPOLLDEMAND_REG</a>            | Transmit poll demand register                     | 0x1004  | RO/WT   |
| <a href="#">DMARXPOLLDEMAND_REG</a>            | Receive poll demand register                      | 0x1008  | RO/WT   |
| <a href="#">DMARXBASEADDR_REG</a>              | Base address of the first receive descriptor      | 0x100C  | R/W     |
| <a href="#">DMATXBASEADDR_REG</a>              | Base address of the first transmit descriptor     | 0x1010  | R/W     |
| <a href="#">DMASTATUS_REG</a>                  | Base address of interrupt, error and other events | 0x1014  | R/SS/WC |
| <a href="#">DMAOPERATION_MODE_REG</a>          | Operation mode and command register               | 0x1018  | R/SS/WC |
| <a href="#">DMAIN_EN_REG</a>                   | Interrupt disable and enable register             | 0x101C  | R/W     |
| <a href="#">DMAMISSEDFR_REG</a>                | Missed frame and buffer overflow counter register | 0x1020  | R/W     |
| <a href="#">DMARINTWDTIMER_REG</a>             | Receive watchdog timer counter register           | 0x1024  | R/W     |
| <a href="#">DMAAHBSTATUS_REG</a>               | AHB master interface status register              | 0x102C  | RO      |
| <a href="#">DMATXCURRDESC_REG</a>              | Current transmit descriptor register              | 0x1048  | RO      |
| <a href="#">DMARXCURRDESC_REG</a>              | Current receive descriptor register               | 0x104C  | RO      |
| <a href="#">DMATXCURRADDR_BUF_REG</a>          | Current transmit buffer address register          | 0x1050  | RO      |
| <a href="#">DMARXCURRADDR_BUF_REG</a>          | Current receive buffer address register           | 0x1054  | RO      |
| <b>MAC configuration and control registers</b> |   |         |         |
| <a href="#">EMACCONFIG_REG</a>                 | MAC configuration register                        | 0x0000  | R/W     |
| <a href="#">EMACFF_REG</a>                     | Frame filter register                             | 0x0004  | R/W     |
| <a href="#">EMACMIIADDR_REG</a>                | PHY access permission configuration register      | 0x0010  | R/WS/SC |
| <a href="#">EMACMIIDATA_REG</a>                | PHY write and read data register                  | 0x0014  | R/W     |
| <a href="#">EMACFC_REG</a>                     | Frame flow control register                       | 0x0018  | varies  |
| <a href="#">EMACVLANTAG_REG</a>                | 802.1Q VLAN tag register                          | 0x001C  | R/W     |
| <a href="#">EMACDEBUG_REG</a>                  | Status and debug register                         | 0x0024  | RO      |
| <a href="#">PMT_RWUFR_REG</a>                  | Wake-up frame filter register                     | 0x0028  | RO      |

| Name                                     | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">PMT_CSR_REG</a>              | Power management control and status register         | 0x002C  | RO     |
| <a href="#">EMACLPI_CSR_REG</a>          | LPI control and status register                      | 0x0030  | RO     |
| <a href="#">EMACLPITIMERSCONTROL_REG</a> | LPI timer control register                           | 0x0034  | RO     |
| <a href="#">EMACINTS_REG</a>             | Interrupt status register                            | 0x0038  | RO     |
| <a href="#">EMACINTMASK_REG</a>          | Interrupt mask register                              | 0x003C  | R/W    |
| <a href="#">EMACADDR0HIGH_REG</a>        | The higher 16 bits of the first 6-byte MAC address   | 0x0040  | R/W    |
| <a href="#">EMACADDR0LOW_REG</a>         | The lower 32 bits of the first 6-byte MAC address    | 0x0044  | R/W    |
| <a href="#">EMACADDR1HIGH_REG</a>        | The higher 16 bits of the second 6-byte MAC address  | 0x0048  | R/W    |
| <a href="#">EMACADDR1LOW_REG</a>         | The lower 32 bits of the second 6-byte MAC address   | 0x004C  | R/W    |
| <a href="#">EMACADDR2HIGH_REG</a>        | The higher 16 bits of the third 6-byte MAC address   | 0x0050  | R/W    |
| <a href="#">EMACADDR2LOW_REG</a>         | The lower 32 bits of the third 6-byte MAC address    | 0x0054  | R/W    |
| <a href="#">EMACADDR3HIGH_REG</a>        | The higher 16 bits of the fourth 6-byte MAC address  | 0x0058  | R/W    |
| <a href="#">EMACADDR3LOW_REG</a>         | The lower 32 bits of the fourth 6-byte MAC address   | 0x005C  | R/W    |
| <a href="#">EMACADDR4HIGH_REG</a>        | The higher 16 bits of the fifth 6-byte MAC address   | 0x0060  | R/W    |
| <a href="#">EMACADDR4LOW_REG</a>         | The lower 32 bits of the fifth 6-byte MAC address    | 0x0064  | R/W    |
| <a href="#">EMACADDR5HIGH_REG</a>        | The higher 16 bits of the sixth 6-byte MAC address   | 0x0068  | R/W    |
| <a href="#">EMACADDR5LOW_REG</a>         | The lower 32 bits of the sixth 6-byte MAC address    | 0x006C  | R/W    |
| <a href="#">EMACADDR6HIGH_REG</a>        | The higher 16 bits of the seventh 6-byte MAC address | 0x0070  | R/W    |
| <a href="#">EMACADDR6LOW_REG</a>         | The lower 32 bits of the seventh 6-byte MAC address  | 0x0074  | R/W    |
| <a href="#">EMACADDR7HIGH_REG</a>        | The higher 16 bits of the eighth 6-byte MAC address  | 0x0078  | R/W    |
| <a href="#">EMACADDR7LOW_REG</a>         | The lower 32 bits of the eighth 6-byte MAC address   | 0x007C  | R/W    |
| <a href="#">EMACADDR8HIGH_REG</a>        | The higher 16 bits of the ninth 6-byte MAC address   | 0x0080  | R/W    |
| <a href="#">EMACADDR8LOW_REG</a>         | The lower 32 bits of the ninth 6-byte MAC address    | 0x0084  | R/W    |
| <a href="#">EMACCSTATUS_REG</a>          | Interconnection status                               | 0x00D8  | RO     |

| Name                                     | Description  | Address | Access  |
|--|--|---------|---------|
| <a href="#">EMACWDOGTO_REG</a>           | Watchdog timer timeout control register            | 0x00DC  | R/W     |
| <a href="#">EMACTXVLTCTRL_REG</a>        | TX VLAN tag control register                       | 0x0584  | R/W     |
| <a href="#">EMACTSTPCTRL_REG</a>         | Timestamp control register                         | 0x0700  | R/W     |
| <a href="#">EMACSUB2NDINCR_REG</a>       | Sub-second increment register                      | 0x0704  | R/W     |
| <a href="#">EMACSYSTM2ND_REG</a>         | System time second register                        | 0x0708  | RO      |
| <a href="#">EMACSYSTMNS_REG</a>          | System time nanosecond register                    | 0x070C  | RO      |
| <a href="#">EMAC2NDUPT_REG</a>           | System time second update register                 | 0x0710  | R/W     |
| <a href="#">EMACNSUPT_REG</a>            | System time nanosecond update register             | 0x0714  | R/W     |
| <a href="#">EMACTSTPADDEND_REG</a>       | Fine update mode addend                            | 0x0718  | R/W     |
| <a href="#">EMACTGTIME2ND_REG</a>        | Target time second register                        | 0x071C  | R/W     |
| <a href="#">EMACTGTIMENS_REG</a>         | Target time nanosecond register                    | 0x0720  | R/W     |
| <a href="#">EMACSYSTMHIGHWORD2ND_REG</a> | System time nanosecond register (bit 32 to bit 47) | 0x0724  | R/W/SU  |
| <a href="#">EMACTSTPSTATUS_REG</a>       | Timestamp status register                          | 0x0728  | R/SS/RC |

## 47.8 Registers

The addresses in this section are relative to EMAC base address provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 471. DMABUSMODE\_REG (0x1000)**

|                       |    |    |    |            |    |    |    |                     |      |    |     |               |    |   |      |            |   |       |   |             |  |  |  |           |  |  |  |                |  |  |  |               |  |  |  |               |  |  |  |             |  |  |  |
|-----------------------|----|----|----|------------|----|----|----|---------------------|------|----|-----|---------------|----|---|------|------------|---|-------|---|-------------|--|--|--|-----------|--|--|--|----------------|--|--|--|---------------|--|--|--|---------------|--|--|--|-------------|--|--|--|
| (DMAREBUILDINCRBURST) |    |    |    | (reserved) |    |    |    | DMATransmitPriority |      |    |     | DMAAddralibea |    |   |      | RX_DMA_PBL |   |       |   | FIXED_BURST |  |  |  | PRI_RATIO |  |  |  | PROG_BURST_LEN |  |  |  | ALT_DESC_SIZE |  |  |  | DESC_SKIP_LEN |  |  |  | DMA_ARB_SCH |  |  |  |
| SW_RST                |    |    |    |            |    |    |    |                     |      |    |     |               |    |   |      |            |   |       |   |             |  |  |  |           |  |  |  |                |  |  |  |               |  |  |  |               |  |  |  |             |  |  |  |
| 31                    | 30 | 28 | 27 | 26         | 25 | 24 | 23 | 22                  | 17   | 16 | 15  | 14            | 13 | 8 | 7    | 6          | 2 | 1     | 0 |             |  |  |  |           |  |  |  |                |  |  |  |               |  |  |  |               |  |  |  |             |  |  |  |
| 0                     | 0  | 0  | 0  | 0          | 0  | 0  | 0  | 0                   | 0x01 | 0  | 0x0 | 0x01          | 0  | 0 | 0x00 | 0          | 1 | Reset |   |             |  |  |  |           |  |  |  |                |  |  |  |               |  |  |  |               |  |  |  |             |  |  |  |

**DMAREBUILDINCRBURST** Configures whether to rebuild INCRx burst.

0: Not rebuild

1: If the AHB master gets an EBT (retry, split, or losing bus grant), the AHB master interface rebuilds the pending beats of any burst transfer initiated with INCRx using INCRx and SINGLE.

(R/W)

**DMATransmitPriority** Configures whether the transmit DMA has higher priority than the receive DMA during arbitration.

0: Lower priority

1: Higher priority

(R/W)

**DMAMixedBurst** Configures whether to use mixed burst.

0: Not use

1: If the FIXED\_BURST bit is 1, the AHB Master interface starts all bursts of length more than 16 with INCR (undefined burst) whereas it reverts to fixed burst transfers (INCRx and SINGLE) for burst length of 16 and less.

(R/W)

**DMAAddralibea** Configures whether bursts are aligned to address.

0: Not aligned to address

1: If the FIXED\_BURST bit is 1, the AHB interface generates all bursts aligned to the start address LS bits. If the FIXED\_BURST bit is 0, the first burst (accessing the data buffer's start address) is not aligned, but subsequent bursts are aligned to the address.

(R/W)

Continued on the next page...

**Register 471. DMABUSMODE\_REG (0x1000)**

Continued from the previous page...

**PBLX8\_MODE** Configures whether to multiply the PBL (programmable burst length) value by 8.

0: Disable

1: The programmed PBL value (PROG\_BURST\_LEN and RX\_DMA\_PBL) is multiplied by 8. Therefore, the DMA transfers the data in 8, 16, 32, 64, 128, and 256 beats depending on the PBL value.

(R/W)

**USE\_SEP\_PBL** Configures whether to use separate PBL.

0: PROG\_BURST\_LEN is applicable only for TX DMA, and RX DMA uses RX\_DMA\_PBL.

1: PROG\_BURST\_LEN is applicable for both TX and RX DMA.

(R/W)

**RX\_DMA\_PBL** Configure the maximum number of beats to be transferred in one RX DMA transaction, namely the maximum value that is used in a single block Read or Write.

Value range: 1, 2, 4, 8, 16 and 32. Any other value results in undefined behavior.

Valid only when USE\_SEP\_PBL is set.

(R/W)

**FIXED\_BURST** Configures whether the AHB Master interface performs fixed burst transfers.

0: The AHB interface uses SINGLE and INCR burst transfer operations.

1: The AHB interface uses only SINGLE, INCR4, INCR8, or INCR16 during start of the normal burst transfers.

(R/W)

**PRI\_RATIO** Configures the priority ratio in the weighted round-robin arbitration between the RX DMA and TX DMA.

0: 1:1

1: 2:0

2: 3:1

3: 4:1

Valid only when DMA\_ARB\_SCH is 0. (R/W)

**PROG\_BURST\_LEN** Configures the maximum number of beats to be transferred in one DMA transaction.

If the number of beats to be transferred is more than 32, then perform the following steps:

1. Set the PBLx8 mode with PBLX8\_MODE

2. Set the PBL with PROG\_BURST\_LEN

(R/W)

**ALT\_DESC\_SIZE** Configures whether to increase the descriptor size to 32 bytes.

0: Keep 16 bytes

1: Increase to 32 bytes

(R/W)

**DESC\_SKIP\_LEN** Configures the number of Word, Dword, or Lword (depending on the 32-bit, 64-bit, or 128-bit bus) to skip between two unchained descriptors.

The address skipping starts from the end of the current descriptor to the start of next descriptor.

When this field is 0, the descriptor table is taken as contiguous by the DMA in Ring mode. (R/W)

Continued on the next page...

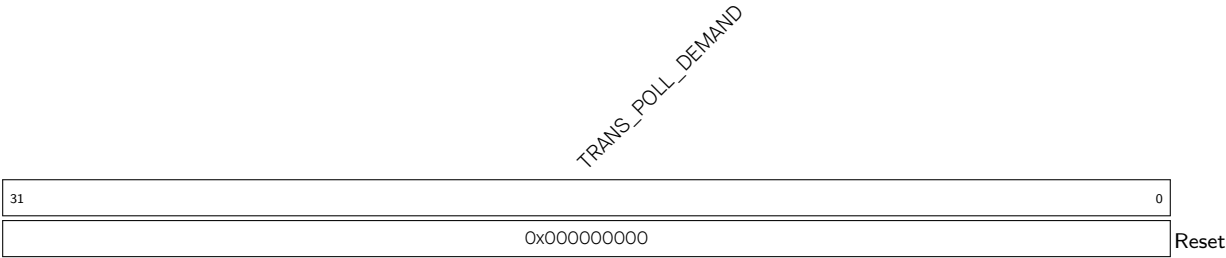


Register 47.1. DMABUSMODE\_REG (0x1000)

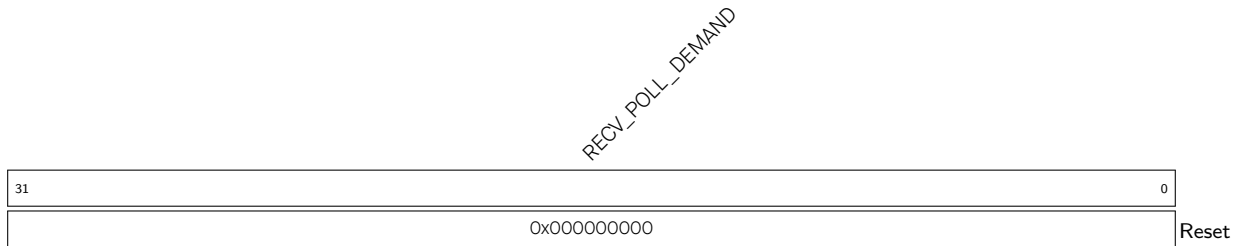
Continued from the previous page...

- DMA\_ARB\_SCH** Configures the arbitration scheme between the transmit and receive paths.  
0: Weighted round-robin with RX:TX or TX:RX. In this case, the priority between the paths is according to the priority specified in PRI\_RATIO.  
1: Fixed priority (The transmit path has priority over receive path).  
(R/W)
- SW\_RST** Configures whether the MAC DMA Controller resets the logic and all internal registers of the MAC.  
0: Release from reset  
1: Reset  
This bit is cleared automatically after the reset operation has completed in all of the ETH\_MAC clock domains.  
(R/WS/SC)

Register 47.2. DMATXPOLLDemand\_REG (0x1004)



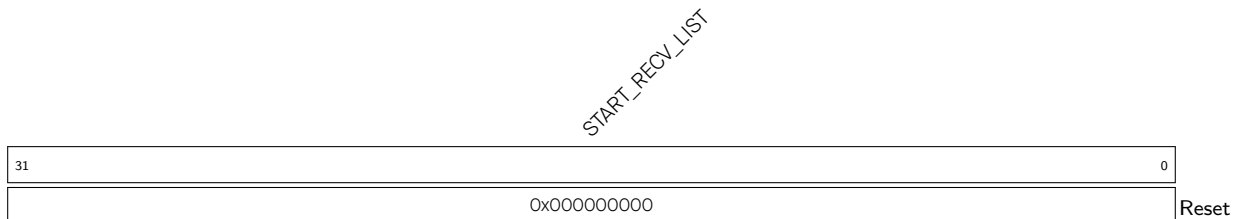
- TRANS\_POLL\_DEMAND** Configures whether to enable the TX DMA to check if the DMA owns the current descriptor.  
Any value: Enable  
When this field is written, the DMA reads the current descriptor pointed to by [DMATXCUR-RDESC\\_REG](#). If that descriptor is not available (owned by the Host), the transmission returns to the Suspend state and the Bit 2 (TU) of Register 5 (Status Register) is asserted. If the descriptor is available, the transmission resumes. (RO/WT)

**Register 47.3. DMARXPOLLDEMAND\_REG (0x1008)**

**RCV\_POLL\_DEMAND** Configures whether to enable the RX DMA to check if the DMA owns the current descriptor.

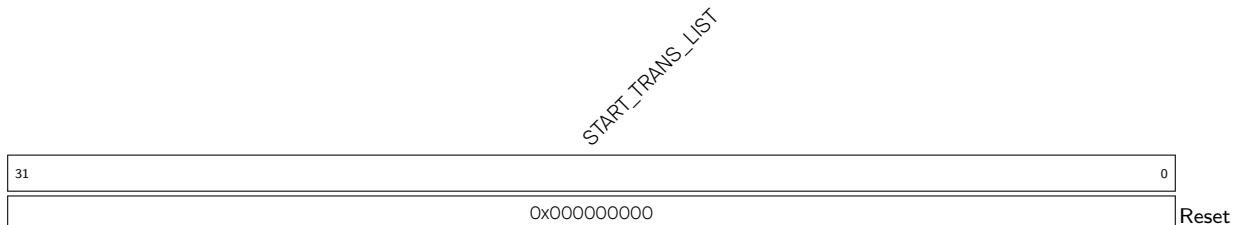
Any value: Enable

When this field is written, the DMA reads the current descriptor pointed to by [DMARXCUR-RDESC\\_REG](#). If that descriptor is not available (owned by the Host), the reception returns to the Suspended state and the Bit 7 (RU) of Register 5 (Status Register) is not asserted. If the descriptor is available, the RX DMA returns to the active state.(RO/WT)

**Register 47.4. DMARXBASEADDR\_REG (0x100C)**

**START\_RECV\_LIST** Configures the base address of the first descriptor in the receive descriptor linked list.

The LSB bits (1:0) are ignored (32-bit wide bus) and internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO). (R/W)

**Register 47.5. DMATXBASEADDR\_REG (0x1010)**

**START\_TRANS\_LIST** Configures the base address of the first descriptor in the Transmit Descriptor list. The LSB bits (1:0) are ignored (32-bit wide bus) and are internally taken as all-zero by the DMA. Therefore, these LSB bits are read-only (RO). (R/W)

**Register 47.6. DMASTATUS\_REG (0x1014)**

|            |    |              |    |            |    |              |  |            |    |            |    |                  |   |                 |    |               |    |              |    |                |    |                   |   |            |   |                 |   |             |   |                |   |                  |   |               |   |              |   |                 |   |                   |   |                 |   |           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|----|--------------|----|------------|----|--------------|--|------------|----|------------|----|------------------|---|-----------------|----|---------------|----|--------------|----|----------------|----|-------------------|---|------------|---|-----------------|---|-------------|---|----------------|---|------------------|---|---------------|---|--------------|---|-----------------|---|-------------------|---|-----------------|---|-----------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |    | EMAC_LPI_INT |    | TS_TRI_INT |    | EMAC_PMT_INT |  | (reserved) |    | ERROR_BITS |    | TRANS_PROC_STATE |   | RECV_PROC_STATE |    | NORM_INT_SUMM |    | ABN_INT_SUMM |    | EARLY_RECV_INT |    | FATAL_BUS_ERR_INT |   | (reserved) |   | EARLY_TRANS_INT |   | RECV_WDT_TO |   | RECV_PROC_STOP |   | RECV_BUF_UNAVAIL |   | TRANS_UNDFLOW |   | TRANS_OVFLOW |   | TRANS_JABBER_TO |   | TRANS_BUF_UNAVAIL |   | TRANS_PROC_STOP |   | TRANS_INT |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|            |    |              |    |            |    |              |  |            |    |            |    |                  |   |                 |    |               |    |              |    |                |    |                   |   |            |   |                 |   |             |   |                |   |                  |   |               |   |              |   |                 |   |                   |   |                 |   |           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         | 30 | 29           | 28 | 27         | 26 | 25           |  | 23         | 22 |            | 20 | 19               |   | 17              | 16 | 15            | 14 | 13           | 12 | 11             | 10 | 9                 | 8 | 7          | 6 | 5               | 4 | 3           | 2 | 1              | 0 |                  |   |               |   |              |   |                 |   |                   |   |                 |   |           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0  | 0            | 0  | 0          | 0  | 0x0          |  | 0x0        |    | 0x0        |    | 0                | 0 | 0               | 0  | 0             | 0  | 0            | 0  | 0              | 0  | 0                 | 0 | 0          | 0 | 0               | 0 | 0           | 0 | 0              | 0 | 0                | 0 | 0             | 0 | 0            | 0 | 0               | 0 | 0                 | 0 | 0               | 0 | 0         | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**EMAC\_LPI\_INT** The raw interrupt status of EMAC\_LPI\_INT. (RO)

**TS\_TRI\_INT** The raw interrupt status of TS\_TRI\_INT. (RO)

**EMAC\_PMT\_INT** The raw interrupt status of EMAC\_PMT\_INT. (RO)

**ERROR\_BITS** Represents the type of error that caused a Bus Error, for example, error response on the AHB interface.

0: Error during RX DMA Write Data Transfer

1: Error during TX DMA Read Data Transfer

2: Error during RX DMA Descriptor Write Access

3: Error during TX DMA Descriptor Write Access

4: Error during RX DMA Descriptor Read Access

5: Error during TX DMA Descriptor Read Access

Valid only when Bit 13 (FBI) is 1. This field does not generate an interrupt. (RO)

**TRANS\_PROC\_STATE** Represents the Transmit DMA FSM state.

0: Stopped; Reset or Stop Transmit Command issued

1: Running; Fetching Transmit Transfer Descriptor

2: Running; Waiting for status

3: Running; Reading Data from Host memory buffer and queuing it to transmit buffer (TX FIFO)

4: TIME\_STAMP write state

5: Reserved for future use

6: Suspended; Transmit Descriptor Unavailable or Transmit Buffer Underflow

7: Running; Closing Transmit Descriptor

This field does not generate an interrupt. (RO)

Continued on the next page...

**Register 47.6. DMASTATUS\_REG (0x1014)**

Continued from the previous page...

**NORM\_INT\_SUMM** Represents the logical OR of the following when the corresponding interrupt bits are enabled in Interrupt Enable Register.

Bit[0]: Transmit Interrupt

Bit[2]: Transmit Buffer Unavailable

Bit[6]: Receive Interrupt

Bit[14]: Early Receive Interrupt

Only unmasked interrupts affect this bit.

This is a sticky bit and must be cleared (by writing 1 to this bit) each time a corresponding bit, which causes this set to be set, is cleared. (R/SS/WC)

**ABN\_INT\_SUMM** Represents the logical OR of the following when the corresponding interrupt bits are enabled in Interrupt Enable Register.

Bit[1]: Transmit Process Stopped

Bit[3]: Transmit Jabber Timeout

Bit[4]: Receive FIFO Overflow

Bit[5]: Transmit Underflow

Bit[7]: Receive Buffer Unavailable

Bit[8]: Receive Process Stopped

Bit[9]: Receive Watchdog Timeout

Bit[10]: Early Transmit Interrupt

Bit[13]: Fatal Bus Error

Only unmasked interrupts affect this bit.

This is a sticky bit and must be cleared each time a corresponding bit, which causes this bit to be set, is cleared. (R/SS/WC)

**EARLY\_RECV\_INT** The raw interrupt status of EARLY\_RECV\_INT. (R/SS/WC)

**FATAL\_BUS\_ERR\_INT** The raw interrupt status of FATAL\_BUS\_ERR\_INT. (R/SS/WC)

**EARLY\_TRANS\_INT** The raw interrupt status of EARLY\_TRANS\_INT. (R/SS/WC)

**RCV\_WDT\_TO** Represents whether the Receive Watchdog Timer expired while receiving the current frame and the current frame is truncated after the watchdog timeout.

0: Not expired

1: Expired

(R/SS/WC)

**RCV\_PROC\_STOP** Represents whether the Receive Process enters the Stopped state.

0: Not stopped

1: Stopped

(R/SS/WC)

Continued on the next page...

**Register 47.6. DMASTATUS\_REG (0x1014)**

Continued from the previous page...

**RECV\_BUF\_UNAVAIL** Represents whether the Receive Buffer is available.

0: Available

1: Unavailable

This bit is set only when the previous Receive Descriptor is owned by the DMA.

When set, the Host owns the Next Descriptor in the Receive List and the DMA cannot acquire it. The Receive Process is suspended.

To resume processing Receive descriptors, the Host should change the ownership of the descriptor and issue a Receive Poll Demand command. If no Receive Poll Demand is issued, the Receive Process resumes when the next recognized incoming frame is received. (R/SS/WC)

**RECV\_INT** The raw interrupt status of RECV\_INT. (R/SS/WC)

**TRANS\_UNDFLOW** Represents whether the Transmit Buffer had an Underflow during frame transmission.

0: No underflow

1: Underflow

When this bit is 1, transmission is suspended and an Underflow Error TDES0[1] is set. (R/SS/WC)

**RECV\_OVFLOW** Represents whether the Receive Buffer had an Overflow during frame reception.

0: No overflow

1: Overflow

If the partial frame is transferred to the application, the overflow status is set in RDES0[11]. (R/SS/WC)

**TRANS\_JABBER\_TO** Represents whether the Transmit Jabber Timer expired, which happens when the frame size exceeds 2,048 (10,240 bytes when the Jumbo frame is enabled).

0: Not expired

1: Expired

When the Jabber Timeout occurs, the transmission process is aborted and placed in the Stopped state. This causes the Transmit Jabber Timeout TDES0[14] flag to assert. (R/SS/WC)

**TRANS\_BUF\_UNAVAIL** Represents whether the Transmit Buffer is available.

0: Available

1: Unavailable

When this bit is 1, the Host owns the Next Descriptor in the Transmit List and the DMA cannot acquire it. Transmission is suspended. Bits[22:20] explain the Transmit Process state transitions.

To resume processing Transmit descriptors, the Host should change the ownership of the descriptor by setting TDES0[31] and then issue a Transmit Poll Demand command. (R/SS/WC)

**TRANS\_PROC\_STOP** Represents whether the transmission is stopped.

0: Not stopped

1: Stopped

(R/SS/WC)

**TRANS\_INT** The raw interrupt status of TRANS\_INT. (R/SS/WC)

**Register 47.7. DMAOPERATION\_MODE\_REG (0x1018)**

|            |   |   |   |   |                                       |    |    |    |    |                                     |   |    |    |    |                             |    |    |   |    |   |    |    |   |   |            |   |   |   |   |   |   |   |       |  |
|------------|---|---|---|---|---------------------------------------|----|----|----|----|-------------------------------------|---|----|----|----|-----------------------------|----|----|---|----|---|----|----|---|---|------------|---|---|---|---|---|---|---|-------|--|
| (reserved) |   |   |   |   | DIS_DROP_TCPIP_ERR_FRAM<br>(reserved) |    |    |    |    | DIS_FLUSH_RECV_FRAMES<br>(reserved) |   |    |    |    | FLUSH_TX_FIFO<br>(reserved) |    |    |   |    | TX_THRESH_CTRL<br>START_STOP_TRANSMISSION_COMMAND<br>(reserved) |    |    |   |   | (reserved) |   |   |   |   | FWD_ERR_FRAME<br>FWD_UNDER_GF<br>DROP_GFRM<br>RX_THRESH_CTRL<br>OPT_SECOND_FRAME<br>START_STOP_RX<br>(reserved) |   |   |       |  |
| 31         |   |   |   |   | 27                                    | 26 | 25 | 24 | 23 | 21                                  |   | 20 | 19 | 17 |                             | 16 | 14 |   | 13 | 12  | 11 | 10 | 9 | 8 | 7          | 6 | 5 | 4 | 3 | 2   | 1 | 0 |       |  |
| 0          | 0 | 0 | 0 | 0 | 0                                     | 0  | 0  | 0  | 0  | 0                                   | 0 | 0  | 0  | 0  | 0                           | 0  | 0  | 0 | 0  | 0   | 0  | 0  | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0   | 0 | 0 | Reset |  |

**DIS\_DROP\_TCPIP\_ERR\_FRAM** Configures whether to disable dropping of TCP/IP checksum error frames.

0: Enable

1: Disable

When FWD\_ERR\_FRAME is 0, this bit is ignored and all error frames are dropped. (R/W)

**DIS\_FLUSH\_RECV\_FRAMES** Configures whether to disable flushing of received frames because of the unavailability of receive descriptors or buffers.

0: Enable

1: Disable

(R/W)

**FLUSH\_TX\_FIFO** Configures whether to flush TX FIFO to default values.

0: Not flush

1: Flush

(R/WS/SC)

**TX\_THRESH\_CTRL** Configures the threshold of TX FIFO. Transmission starts when the frame size within the TX FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted.

0: 64

1: 128

2: 192

3: 256

4: 40

5: 32

6: 24

7: 16

Transmission starts when the frame size within the TX FIFO is larger than the threshold. In addition, full frames with a length less than the threshold are also transmitted.

(R/W)

Continued on the next page...

**Register 47.7. DMAOPERATION\_MODE\_REG (0x1018)**

Continued from the previous page...

**START\_STOP\_TRANSMISSION\_COMMAND** Configures whether to start or stop the transmission.

0: Stop

1: Start

(R/W)

**FWD\_ERR\_FRAME** Configures whether RX FIFO forward frames with error status (CRC error, collision error, giant frame, watchdog timeout, or overflow)

0: Drop

1: Forward

(R/W)

**FWD\_UNDER\_GF** Configures whether the RX FIFO forward undersized (frames with no Error and length less than 64 bytes) good frames including PAD and CRC.

0: Drop

1: Forward

(R/W)

**DROP\_GFRM** Configures whether to the ETH\_MAC drops the received giant frames in the RX FIFO.

0: Not drop

1: Drop

(R/W)

**RX\_THRESH\_CTRL** Configures the threshold of the RX FIFO.

0: 64

1: 32

2: 96

3: 128

Transfer (request) to DMA starts when the frame size within the RX FIFO is larger than the threshold. (R/W)

**OPT\_SECOND\_FRAME** Configures whether the DMA processes the second frame of the Transmit data even before the status for the first frame is obtained.

0: Not process

1: Process

(R/W)

**START\_STOP\_RX** Configures whether to start or stop RX DMA reception.

0: Stop reception after the transfer of the current frame

1: Start reception

(R/W)

**Register 47.8. DMAIN\_EN\_REG (0x101C)**

| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | DMAIN_NISE<br>DMAIN_AISE<br>DMAIN_ERIE<br>DMAIN_FBEE<br>(reserved)<br>DMAIN_ETIE<br>DMAIN_RWTE<br>DMAIN_RSE<br>DMAIN_RBUE<br>DMAIN_RIE<br>DMAIN_UIE<br>DMAIN_OIE<br>DMAIN_TJTE<br>DMAIN_TBUE<br>DMAIN_TSE<br>DMAIN_TIE |    |    |    |    |    |    |   |   |   |       |   |   |   |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|--|----|----|----|----|----|----|---|---|---|-------|---|---|---|---|---|---|--|
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17 | 16   | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6     | 5 | 4 | 3 | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | Reset |   |   |   |   |   |   |  |

**DMAIN\_NISE** Write 1 to enable and write 0 to disable the summary of the following normal interrupt enable bits:

Bit[0]: Transmit Interrupt

Bit[2]: Transmit Buffer Unavailable

Bit[6]: Receive Interrupt

Bit[14]: Early Receive Interrupt

(R/W)

**DMAIN\_AISE** Write 1 to enable and write 0 to disable the summary of the following abnormal interrupt enable bits:

Bit[1]: Transmit Process Stopped

Bit[3]: Transmit Jabber Timeout

Bit[4]: Receive FIFO Overflow

Bit[5]: Transmit Underflow

Bit[7]: Receive Buffer Unavailable

Bit[8]: Receive Process Stopped

Bit[9]: Receive Watchdog Timeout

Bit[10]: Early Transmit Interrupt

Bit[13]: Fatal Bus Error

(R/W)

**DMAIN\_ERIE** Write 1 to enable and write 0 to disable EARLY\_RECV\_INT. (R/W)

**DMAIN\_FBEE** Write 1 to enable and write 0 to disable FATAL\_BUS\_ERR\_INT.(R/W)

**DMAIN\_ETIE** Write 1 to enable and write 0 to disable EARLY\_TRANS\_INT. (R/W)

**DMAIN\_RWTE** Write 1 to enable and write 0 to disable RECV\_WDT\_TO\_INT. (R/W)

**DMAIN\_RSE** Write 1 to enable and write 0 to disable RECV\_PROC\_STOP\_INT. (R/W)

**DMAIN\_RBUE** Write 1 to enable and write 0 to disable RECV\_BUF\_UNAVAIL\_INT. (R/W)

**DMAIN\_RIE** Write 1 to enable and write 0 to disable RECV\_INT. (R/W)

Continued on the next page...



**Register 47.8. DMAIN\_EN\_REG (0x101C)**

Continued from the previous page...

**DMAIN\_UIE** Write 1 to enable and write 0 to disable TRANS\_UNDFLOW\_INT. (R/W)**DMAIN\_OIE** Write 1 to enable and write 0 to disable RECV\_OVFLOW\_INT. (R/W)**DMAIN\_TJTE** Write 1 to enable and write 0 to disable TRANS\_JABBER\_TO\_INT. (R/W)**DMAIN\_TBUE** Write 1 to enable and write 0 to disable TRANS\_BUF\_UNAVAIL\_INT. (R/W)**DMAIN\_TSE** Write 1 to enable and write 0 to disable TRANS\_PROC\_STOP\_INT. (R/W)**DMAIN\_TIE** Write 1 to enable and write 0 to disable TRANS\_INT. (R/W)**Register 47.9. DMAMISSEDFR\_REG (0x1020)**

|            |    |               |    |             |    |               |    |           |       |
|------------|----|---------------|----|-------------|----|---------------|----|-----------|-------|
| (reserved) |    | Overflow_BFOC |    | Overflow_FC |    | Overflow_BMFC |    | Missed_FC |       |
| 31         | 29 | 28            | 27 |             | 17 | 16            | 15 |           | 0     |
| 0          | 0  | 0x0           |    | 0x0         |    | 0x0           |    | 0x0       | Reset |

**Overflow\_BFOC** Represents the status of the overflow frame counter.

0: No overflow.

1: The overflow frame counter (Overflow\_FC) overflows, that is, the RX FIFO overflows with the overflow frame counter at maximum value. In such a scenario, the overflow frame counter is reset to all-zeros.

(R/SS/RC)

**Overflow\_FC** Represents the number of frames missed by the application.

This counter is incremented each time the MTL FIFO overflows. (R/SS/RC)

**Overflow\_BMFC** Represents the status of the missed frame counter.

0: No overflow.

1: The missed frame counter (Missed\_FC) overflows, that is, the Host Receive Buffer being unavailable with the missed frame counter at maximum value. In such a scenario, the Missed frame counter is reset to all-zeros.

(R/SS/RC)

**Missed\_FC** Represents the number of frames missed by the controller because of the Host Receive Buffer being unavailable.

This counter is incremented each time the DMA discards an incoming frame. (R/SS/RC)

**Register 47.10. DMARINTWDTIMER\_REG (0x1024)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | RIWTC |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8     | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x000 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**RIWTC** Configures the number of system clock cycles multiplied by 256.

The watchdog timer gets triggered with the programmed value after the RX DMA completes the transfer of a frame for which the RI (RECV\_INT) status bit is not set because of the setting in the corresponding descriptor RDES1[31].

When the watchdog timer runs out, the RI bit is set and the timer is stopped. The watchdog timer is reset when the RI bit is set high because of the automatic setting of RI as per RDES1[31] of any received frame. (R/W)

**Register 47.11. DMAAHBSTATUS\_REG (0x102C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |        |     |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------|-----|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | AHB_ST |     |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0      |     |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0      | 0x0 | Reset |

**AHB\_ST** Configures the state of the AHB master interface.

0: Idle

1: Active

(R/W)

**Register 47.12. DMATXCURREDESC\_REG (0x1048)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**TRANS\_DECR\_ADDR\_PTR** Represents the address of the current transmit descriptor list updated by the DMA during operation.

This field is cleared on reset. (RO)

**Register 47.13. DMARXCURREDESC\_REG (0x104C)**

|            |   |
|------------|---|
| 31         | 0 |
| 0x00000000 |   |
| Reset      |   |

**RECV\_DECR\_ADDR\_PTR** Represents the address of the current receive descriptor list updated by the DMA during operation.

This field is cleared on reset. (RO)

**Register 47.14. DMATXCURRADDR\_BUF\_REG (0x1050)**

|            |   |
|------------|---|
| 31         | 0 |
| 0x00000000 |   |
| Reset      |   |

**TRANS\_BUFF\_ADDR\_PTR** Represents the address of the Transmit Buffer updated by the DMA during operation.

This field is cleared on reset. (RO)

**Register 47.15. DMARXCURRADDR\_BUF\_REG (0x1054)**

|            |   |
|------------|---|
| 31         | 0 |
| 0x00000000 |   |
| Reset      |   |

**RECV\_BUFF\_ADDR\_PTR** Represents the address of the Receive Buffer updated by the DMA during operation.

This field is cleared on reset. (RO)

Register 47.16. EMACCONFIG\_REG (0x0000)

| (reserved) |     | SAIRC | ASS2KP |    | (reserved) |    | EMACCRC_STRIP |    | (reserved) |    | EMACWATCHDOG |    | EMACJABBER |    | (reserved) |    | EMACJUMBOFRAME |    | EMACINTERFRAMEGAP |   | EMACDISABLECRS |   | EMACMI |     | EMACFESPEED |   | EMACRXDOWN |   | EMACLOOPBACK |       | EMACRXIPCOFFLOAD |  | (reserved) |  | EMACPADCRCSTRIP |  | EMACBACKOFFLIMIT |  | EMACTX |  | EMACRX |  | PLTF |  |
|------------|-----|-------|--------|----|------------|----|---------------|----|------------|----|--------------|----|------------|----|------------|----|----------------|----|-------------------|---|----------------|---|--------|-----|-------------|---|------------|---|--------------|-------|------------------|--|------------|--|-----------------|--|------------------|--|--------|--|--------|--|------|--|
| 31         | 30  | 28    | 27     | 26 | 25         | 24 | 23            | 22 | 21         | 20 | 19           | 17 | 16         | 15 | 14         | 13 | 12             | 11 | 10                | 9 | 8              | 7 | 6      | 5   | 4           | 3 | 2          | 1 | 0            |       |                  |  |            |  |                 |  |                  |  |        |  |        |  |      |  |
| 0          | 0x0 |       | 0      | 0  | 0          | 0  | 0             | 0  | 0          | 0  | 0            | 0  | 0          | 1  | 0          | 0  | 0              | 0  | 0                 | 0 | 0              | 0 | 0      | 0x0 | 0           | 0 | 0          | 0 | 0x0          | Reset |                  |  |            |  |                 |  |                  |  |        |  |        |  |      |  |

**SAIRC** Configures the source address insertion or replacement for all transmitted frames.

Bit 30 specifies which MAC Address register (0 or 1) is used for source address insertion or replacement based on the values of Bits [29:28].

Bits [29:28]:

0, 1: The input mti\_sa\_ctrl\_i and ati\_sa\_ctrl\_i control the SA field generation

2: Insert the content of the MAC Address register (0 or 1) in the SA field of all transmitted frames

3: Replace the the content of MAC Address register (0 or 1) in the SA field of all transmitted frames

Bit 30:

0: Use MAC Address 0 register

1: Use MAC Address 1 register

(R/W)

**ASS2KP** Configures whether the MAC considers received frames of more than 2000 bytes as normal packets or giant frames.

0: Giant frames. In this case, if Bit[20] (JE) is 0, the MAC considers all received frames of size more than 1,518 bytes (1,522 bytes for tagged) as Giant frames.

1: Normal packets.

(R/W)

**EMACCRC\_STRIP** Configures whether to strip and drop the last 4 bytes (FCS) of all frames of Ether type (Length/Type field greater than or equal to 1,536) before forwarding the frame to the application.

0: Not strip and drop

1: Strip and drop

(R/W)

**EMACWATCHDOG** Configures whether to disable the watchdog timer.

0: Enable. In this case, the MAC does not allow a receive frame with more than 2,048 bytes (10,240 if JE is set high) or the value programmed in Watchdog Timeout Register. The MAC cuts off any bytes received after the watchdog limit number of bytes.

1: Disable. In this case, the MAC can receive frames of up to 16,384 bytes.

(R/W)

**EMACJABBER** Configures whether to disable the jabber timer on the transmitter.

0: Enable. In this case, the MAC cuts off the transmitter if the application sends out more than 2,048 bytes of data (10,240 if JE is set high) during transmission.

1: Disable. In this case, the MAC can transfer frames of up to 16,384 bytes.

(R/W)

Continued on the next page...

**Register 47:16. EMACCONFIG\_REG (0x0000)**

Continued from the previous page...

**EMACJUMBOFRAME** Configures whether the MAC allows Jumbo frames of 9,018 bytes (9,022 bytes for VLAN tagged frames) without reporting a giant frame error in the receive frame status.

0: Not allow

1: Allow

(R/W)

**EMACINTERFRAMEGAP** Configures the minimum interframe gap (IFG) between frames during transmission.

0: 96 bit times

1: 88 bit times

2: 80 bit times

3: 72 bit times

4: 64 bit times

5: 56 bit times

6: 48 bit times

7: 40 bit times

In the half-duplex mode, the minimum IFG can be configured only for 64 bit times (IFG = 100).

(R/W)

**EMACDISABLECRS** Configures whether to disable Carrier Sense during transmission.

0: The MAC transmitter generates Loss of Carrier or No Carrier errors because of Carrier Sense and can even abort the transmissions.

1: The MAC transmitter ignores the MII CRS signal during frame transmission in the half-duplex mode. This request results in no errors generated because of Loss of Carrier or No Carrier during such transmission.

(R/W)

**EMACMII** Configures the Ethernet line speed.

0: For 1000 Mbps operations

1: For 10 or 100 Mbps operations

In 10 or 100 Mbps operations, the exact line speed is determined by both this bit and the FES (EMACFESPEED) bit. (R/W)

**EMACFESPEED** Configures the speed in the MII and RMII interface.

0: 10 Mbps

1: 100 Mbps

(R/W)

**EMACRXOWN** Configures whether to disable receive own.

0: The MAC receives all packets that are given by the PHY while transmitting.

1: the MAC disables the reception of frames when TX\_EN triggers an interrupt in the half-duplex mode.

This bit is not applicable if the MAC is operating in the full-duplex mode. (R/W)

Continued on the next page...

**Register 47:16. EMACCONFIG\_REG (0x0000)**

Continued from the previous page...

**EMACLOOPBACK** Configures whether to enable the loopback mode.

0: Disable.

1: Enable. In this case, the MII Receive clock input (CLK\_RX) is required for the loopback to work properly, because the Transmit clock is not looped-back internally.

(R/W)

**EMACDUPLEX** Configures whether to enable full-duplex mode, so that the MAC can transmit and receive simultaneously.

0: Disable

1: Enable

This bit is RO with a default value of 1 in the full-duplex-only configuration. (R/W)

**EMACRXIPCOFFLOAD** Configures whether to enable the checksum offload function

0: Disable

1: Enable

When the checksum offload function is enabled, the MAC calculates the 16-bit one's complement of the one's complement sum of all received Ethernet frame payloads. It also checks whether the IPv4 Header checksum (assumed to be bytes 25/26 or 29/30 (VLAN-tagged) of the received Ethernet frame) is correct for the received frame and gives the status in the receive status word. The MAC also appends the 16-bit checksum calculated for the IP header datagram payload (bytes after the IPv4 header) and appends it to the Ethernet frame transferred to the application (when Type 2 COE is deselected). (R/W)

**EMACRETRY** Configures whether to disable retry, so that the MAC attempts only one transmission, and when a collision occurs on the MII interface the MAC ignores the current frame transmission and reports a Frame Abort with excessive collision error in the transmit frame status.

0: Enable

1: Disable

Valid only in the half-duplex mode. (R/W)

**EMACPADCRCSTRIP** Configures whether to enable automatic Pad or CRC stripping.

0: Disable. In this case, the MAC passes all incoming frames, without modifying them, to the Host.

1: Enable. In this case, the MAC strips the Pad or FCS field on the incoming frames only if the value of the length field is less than 1,536 bytes. All received frames with length field greater than or equal to 1,536 bytes are passed to the application without stripping the Pad or FCS field.

(R/W)

Continued on the next page...

**Register 47:16. EMACCONFIG\_REG (0x0000)**

Continued from the previous page...

**EMACBACKOFFLIMIT** Configures the back-off limit determining the random integer number (r) of slot time delays (4,096 bit times for 1000 Mbps and 512 bit times for 10/100 Mbps) for which the MAC waits before rescheduling a transmission attempt during retries after a collision.

00:  $k = \min(n, 10)$

01:  $k = \min(n, 8)$

10:  $k = \min(n, 4)$

11:  $k = \min(n, 1)$

where  $n$  = retransmission attempt.

The random integer  $r$  takes the value in the range  $0 \leq r < k$ th power of 2

Valid only in the half-duplex mode. (R/W)

**EMACDEFERRALCHECK** Configures whether to enable the deferral check function.

0: Disable

1: Enable

(R/W)

**EMACTX** Configures whether to enable the transmit state machine of the MAC.

0: Disabled after the completion of the transmission of the current frame, and does not transmit any further frames

1: Enabled for transmission on the MII

(R/W)

**EMACRX** Configures whether to enable the receiver state machine of the MAC. 0: Disabled after the completion of the reception of the current frame, and does not receive any further frames from the MII

1: Enabled for receiving frames from the MII

(R/W)

**PLTF** Configures the number of preamble bytes that are added to the beginning of every Transmit frame.

0: 7 bytes of preamble

1: 5 byte of preamble

2: 3 bytes of preamble

3: Reserved

The preamble reduction occurs only when the MAC is operating in the full-duplex mode. (R/W)

### Register 47.17. EMACFF\_REG (0x0004)

[illegible]

**RECEIVE\_ALL** Configures whether to pass all received modules.

0: The MAC Receiver module passes only those frames to the Application that pass the SA or DA address filter.

1: The MAC Receiver module passes all received frames, irrespective of whether they pass the address filter or not, to the Application. The result of the SA or DA filtering is updated (pass or fail) in the corresponding bits in the Receive Status Word.

(R/W)

**VTFE** Configures whether to enable the VLAN Tag filter.

0: Disable. In this case, the MAC forwards all frames irrespective of the match status of the VLAN Tag.

1: Enable. In this case, the MAC drops VLAN-tagged frames that do not match the VLAN Tag comparison.

(R/W)

**SAFE** Configures whether to enable the source address filter.

0: Disable. In this case, the MAC forwards the received frame to the application with an updated SAF bit of the RX Status depending on the SA address comparison.

1: Enable. In this case, the MAC compares the SA field of the received frames with the values programmed in the enabled SA registers. If the comparison fails, the MAC drops the frame.

(R/W)

**SAIF** Configures whether to enable SA inverse filtering.

0: Disable. In this case, frames whose SA does not match the SA registers are marked as failing the SA Address filter.

1: Enable. In this case, the Address Check block operates in inverse filtering mode for the SA address comparison. The frames whose SA matches the SA registers are marked as failing the SA Address filter.

(R/W)

Continued on the next page...



**Register 4717. EMACFF\_REG (0x0004)**

Continued from the previous page...

**PCF** Configures the forwarding of all control frames (including unicast and multicast PAUSE frames).

0: The MAC filters all control frames.

1: The MAC forwards all control frames except PAUSE control frames to application even if they fail the Address filter.

2: The MAC forwards all control frames to application even if they fail the Address Filter.

3: The MAC forwards control frames that pass the Address Filter.

The following conditions should be true for the PAUSE control frames processing:

Condition 1: The MAC is in the full-duplex mode and flow control is enabled by setting Bit 2 (RFE) of Register 6 (Flow Control Register) to 1.

Condition 2: The destination address (DA) of the received frame matches the special multicast address or EMACADDRO when Bit 3 (UP) of the Register 6 (Flow Control Register) is set.

Condition 3: The Type field of the received frame is 0x8808 and the OP CODE field is 0x0001.

(R/W)

**DBF** Configures whether to disable broadcast frames.

0: Enable. The AFM (Address Filtering Module) module passes all received broadcast frames.

1: Disable. The AFM module filters all incoming broadcast frames. In addition, it overrides all other filter settings.

(R/W)

**PAM** Configures whether to pass all multicast frames.

0: Filtering of multicast frame depends on HMC bit

1: All received frames with a multicast destination address (first bit in the destination address field is '1') are passed

(R/W)

**DAIF** Configures whether to enable DA inverse filtering for both unicast and multicast frames.

0: Disable

1: Enable

(R/W)

**PMODE** Configures whether to enable the promiscuous mode.

0: Disable.

1: Enabled. In this case, the Address Filter module passes all incoming frames regardless of its destination or source address. The SA or DA Filter Fails status bits of the Receive Status Word are always cleared when PR (PRI\_RATIO) is set.

(R/W)

**Register 47.18. EMACMIADDR\_REG (0x0010)**

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |        |  |  |  |        |  |  |  |           |  |  |  |         |  |         |  |   |  |       |  |   |  |  |  |   |  |  |  |   |  |   |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------|--|--|--|--------|--|--|--|-----------|--|--|--|---------|--|---------|--|---|--|-------|--|---|--|--|--|---|--|--|--|---|--|---|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MIIDEV |  |  |  | MIIREG |  |  |  | MIICSRCLK |  |  |  | MIWRITE |  | MIIBUSY |  |   |  |       |  |   |  |  |  |   |  |  |  |   |  |   |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16     |  |  |  | 15     |  |  |  | 11        |  |  |  | 10      |  |         |  | 6 |  |       |  | 5 |  |  |  | 2 |  |  |  | 1 |  | 0 |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00   |  |  |  | 0x00   |  |  |  | 0x00      |  |  |  | 0       |  |         |  | 0 |  | Reset |  |   |  |  |  |   |  |  |  |   |  |   |  |

**MIIDEV** Configures which of the 32 possible PHY devices are being accessed. (R/W)

**MIIREG** Configures the desired address register in the selected PHY device. (R/W)

**MIICSRCLK** Configures the CSR clock frequency.

0: APB clock frequency is 80 MHz, and MDC clock frequency is APB\_CLK/42

3: APB clock frequency is 40 MHz, and MDC clock frequency is APB\_CLK/26

Other values are reserved

(R/W)

**MIIWRITE** Configures the direction of the operation that uses [MII\\_DATA](#).

0: Read operation

1: Write operation

(R/W)

**MIIBUSY** Configures the state of the MII.

0: Idle

1: Busy

This bit is used in combination with [MIIREG](#) and [MII\\_DATA](#).

This bit should read logic 0 (default) before writing to [MIIREG](#) and [MII\\_DATA](#).

To read or write to [MIIREG](#) and [MII\\_DATA](#), software (the user) should set this field to 1.

[MII\\_DATA](#) should be kept valid (data remains unchanged) when it is accessed until this field is cleared by hardware (the MAC).

Note that ESP32-P4 MAC does not receive ACK from PHY during a read or write access to [MIIREG](#) and [MII\\_DATA](#). (R/WS/SC)

**Register 47.19. EMACMIIDATA\_REG (0x0014)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |          |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MII_DATA |    |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16       | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x00000  |    |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |   |

**MII\_DATA** Configures the 16-bit data value read from the PHY after a Management Read operation or the 16-bit data value to be written to the PHY before a Management Write operation.(R/W)

**Register 47.20. EMACFC\_REG (0x0018)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |   |   |   |   |   |   |   |      |   |            |   |     |      |      |      |       |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|---|---|---|---|---|---|---|------|---|------------|---|-----|------|------|------|-------|---|-------|
| PAUSE_TIME |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |   |   |   |   |   |   |   | DZPQ |   | (reserved) |   | PLT | UPFD | RFCE | TFCE | FCBBA |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16         |   |   |   |   |   |   |   |      | 8 | 7          | 6 | 5   | 4    | 3    | 2    | 1     | 0 |       |
| 0x00000    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0    | 0 | 0          | 0 | 0x0 | 0    | 0    | 0    | 0     | 0 | Reset |

**PAUSE\_TIME** Configures the value to be used in the Pause Time field in the transmit control frame. If the Pause Time bits is configured to be double-synchronized to the (G)MII clock domain, then consecutive writes to this register should be performed only after at least four clock cycles in the destination clock domain. (R/W)

**DZPQ** Configures whether to disable the automatic generation of the Zero-Quanta Pause Control frames.  
 0: Enable  
 1: Disable  
 (R/W)

**PLT** Configures the threshold of the PAUSE timer at which the PAUSE Frame is automatically retransmitted.  
 0: The threshold is Pause time minus 4 slot times (PT - 4 slot times).  
 1: The threshold is Pause time minus 28 slot times (PT - 28 slot times).  
 2: The threshold is Pause time minus 144 slot times (PT - 144 slot times).  
 3: The threshold is Pause time minus 256 slot times (PT - 256 slot times).  
 The threshold values should be always less than the Pause Time configured in Bits[31:16]. For example, if PT = 100H (256 slot-times), and PLT = 01, then a second PAUSE frame is automatically transmitted 228 (256 - 28) slot times after the first PAUSE frame is transmitted.  
 (R/W)

**UPFD** Configures whether to enable unicast pause frame detection.  
 0: Disable. The MAC only detects Pause frames with a unique multicast address.  
 1: Enable. The MAC can also detect Pause frames with unicast address of the station. This unicast address should be as specified in the EMACADDRO High Register and EMACADDRO Low Register.  
 (R/W)

**RFCE** Configures whether to enable the decode function of the Pause time.  
 0: Disable  
 1: Enable. The MAC decodes the received Pause frame and disables its transmitter for a specified (Pause) time  
 (R/W)

**TFCE** Configures whether to enable transmit flow control in full-duplex mode, and whether to enable the back-pressure feature in half-duplex mode.  
 0: Disable  
 1: Enable  
 (R/W)

Continued on the next page...

**Register 47.20. EMACFC\_REG (0x0018)**

Continued from the previous page...

**FCBBA** Configures whether to enable a Pause Control frame in the full-duplex mode, and whether to activate the back-pressure function in the half-duplex mode if the TFCE bit is set.

0: Disable

1: Enable

In the full-duplex mode, this bit should be read as 0 before writing to the Flow Control register. To initiate a Pause control frame, the Application must set this bit to 1. During a transfer of the Control Frame, this bit continues to be set to signify that a frame transmission is in progress. After the completion of Pause control frame transmission, the MAC resets this bit to 0. The Flow Control register should not be written to until this bit is cleared. (R/WS/SC)

In the half-duplex mode, when this bit is set (and TFCE is set), then backpressure is asserted by the MAC. During backpressure, when the MAC receives a new frame, the transmitter starts sending a JAM pattern resulting in a collision. When the MAC is configured for the full-duplex mode, the BPA is automatically disabled. (R/W)

### Register 47.21. EMACVLANTAG\_REG (0x001C)

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |   |   |        |    |    |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|---|---|--------|----|----|---|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | ESVL<br>VTIM<br>ETV |   |   | VL     |    |    |   |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 19                  |   |   | 18     | 17 | 16 | 0 |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                   | 0 | 0 | 0x0000 |    |    |   |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |

**ESVL** Configures whether to enable S-VLAN.

0: Disable.

1: Enable. The MAC transmitter and receiver also consider the S-VLAN (Type = 0x88A8) frames as valid VLAN tagged frames.

(R/W)

**VTIM** Configures whether to enable VLAN Tag inverse match.

0: Disable. The frames with matched VLAN Tag are marked as matched.

1: Enable. The frames that do not have matching VLAN Tag are marked as matched.

(R/W)

**ETV** Configures whether to enable 12-bit VLAN Tag comparison.

0: Disable. All 16 bits of the 15th and 16th bytes of the received VLAN frame are used for comparison and VLAN hash filtering.

1: Enable. A 12-bit VLAN identifier is used for comparing and filtering instead of the complete 16-bit VLAN tag. Bits [11:0] of VLAN tag are compared with the corresponding field in the received VLAN-tagged frame.

(R/W)

**VL** Configures the 802.1Q VLAN tag to identify the VLAN frames and is compared to the 15th and 16th bytes of the frames being received for VLAN frames.

When the ETV bit is set, only the VID (Bits[11:0]) is used for comparison.

If VL (VL[11:0] if ETV is set) is all zeros, the MAC does not check the fifteenth and 16th bytes for VLAN tag comparison, and declares all frames with a Type field value of 0x8100 or 0x88a8 as VLAN frames.(R/W)

**Register 47.22. EMACDEBUG\_REG (0x0024)**

| (reserved) |   |    |    |    |    |    | MTLTSFFS | MTLTFNES | (reserved) | MTLTFWCS | MTLTFRCS | MACTP | MACTFCS | MACTPES | (reserved) |   |   |   |   |     |   | MTLRFFLS | (reserved) | MTLRFRCs | MTLRFWCAS | (reserved) | MACRFFCS | MACRPES |
|------------|---|----|----|----|----|----|----------|----------|------------|----------|----------|-------|---------|---------|------------|---|---|---|---|-----|---|----------|------------|----------|-----------|------------|----------|---------|
| 31         |   | 26 | 25 | 24 | 23 | 22 | 21       | 20       | 19         | 18       | 17       | 16    | 15      |         | 10         | 9 | 8 | 7 | 6 | 5   | 4 | 3        | 2          | 1        | 0         |            |          |         |
| 0          | 0 | 0  | 0  | 0  | 0  | 0  | 0        | 0        | 0          | 0x0      | 0        | 0x0   | 0       | 0       | 0          | 0 | 0 | 0 | 0 | 0x0 | 0 | 0x0      | 0          | 0        | 0x0       | 0          | Reset    |         |

**MTLTSFFS** Represents whether MTL TX Status FIFO is full and can accept any more frames for transmission.

0: Not Full

1: Full

(RO)

**MTLTFNES** Represents whether MTL TX FIFO is not empty and some data is left for transmission.

0: Empty

1: Not empty

(RO)

**MTLTFWCS** Represents whether MTL TX FIFO Write Controller is active and transferring data to the TX FIFO.

0: Inactive

1: Active

(RO)

**MTLTFRCS** Represents the state of the TX FIFO Read Controller.

0: IDLE state

1: READ state (transferring data to MAC transmitter)

2: Waiting for TXStatus from MAC transmitter

3: Writing the received TXStatus or flushing the TX FIFO

(RO)

**MACTP** Represents whether the MAC transmitter is in the PAUSE condition (in the full-duplex only mode) and hence does not schedule any frame for transmission.

0: Not in pause

1: In pause

(RO)

**MACTFCS** Represents the state of the MAC Transmit Frame Controller module.

0: IDLE state

1: Waiting for Status of the previous frame or IFG or backoff period to be over

2: Generating and transmitting a PAUSE control frame (in the full-duplex mode)

3: Transferring input frame for transmission

(RO)

**MACTPES** Represents the status of the MAC MII transmit protocol engine.

0: IDLE state

1: Actively transmitting data

(RO)

Continued on the next page...

**Register 47.22. EMACDEBUG\_REG (0x0024)**

Continued from the previous page...

**MTLRFFLS** Represents the status of the fill-level of the RX FIFO.

- 0: RX FIFO Empty
  - 1: RX FIFO fill level is below the flow-control deactivate threshold
  - 2: RX FIFO fill level is above the flow-control activate threshold
  - 3: RX FIFO Full
- (RO)

**MTLRFRCs** Represents the state of the RX FIFO read Controller.

- 0: IDLE state
  - 1: Reading frame data
  - 2: Reserved
  - 3: Flushing the frame data and status
- (RO)

**MTLRFWCAS** Represents the state of the MTL RX FIFO Write Controller.

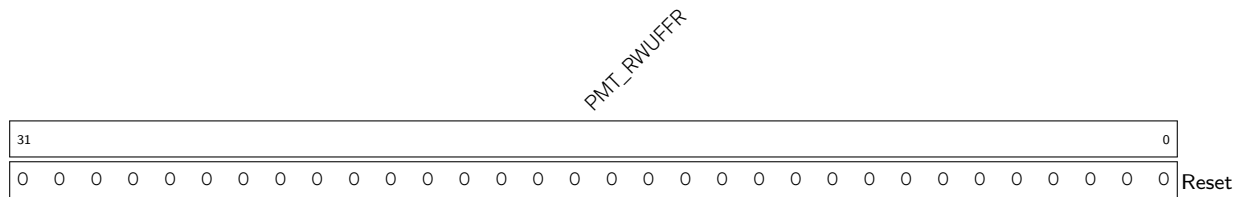
- 0: Inactive
  - 1: Active and is transferring a received frame to the FIFO.
- (RO)

**MACRFFCS** Represents the state of the small FIFO Read (bit 1) and Write (bit 0) controllers of the MAC Receive Frame Controller Module.

- 0: Inactive
  - 1: Active
- (RO)

**MACRPES** Represents the state of the MAC GMII or MII receive protocol engine.

- 0: IDLE
  - 1: Actively receiving data
- (RO)

**Register 47.23. PMT\_RWUFR\_REG (0x0028)**

**WKUPPKTFILTER** When RWKPTR is 0 ~ 3, configures the masking of filter 0 ~ 3 wakeup frame.

Bit[30:0] corresponds to offset+j (j = 0 ~ 30).

Bit[31] has to be 0. 0: Unmask

1: Mask

When RWKPTR is 4, bit[3]/bit[11]/bit[19]/bit[27] configure the target address type, and bit[0]/bit[8]/bit[16]/bit[24] configure whether to enable filter 0 ~ 3.

0: Unicast/Disable

1: Multicast/Enable

When RWKPTR is 5, configures the offset of the filter 0 ~ 3 masked byte.

Bit[7:0] configures the offset of filter 0 masked byte, and [31:24] configures the offset of filter 3 masked byte.

When RWKPTR is 6 ~ 7, configures the 16-bit CRC value of filter 0 ~ 3 masked byte starting from offset based on the formula:

$$G(x) = x^{16} + x^{15} + x^2 + 1$$

Bit[7:0] configures the CRC value of filter 0 or filter 2 masked byte when RWKPTR is 6 or 7 respectively, and bit[31:16] configures the CRC value of filter 1 or filter 3 masked byte when RWKPTR is 6 or 7 respectively.

(R/W)



**Register 47.24. PMT\_CSR\_REG (0x002C)**

| RWKFILTRST<br>(reserved) |    |    |    | RWKPTR |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |    |   |   |   |   |   |   |   |   |   |   |   |   | GLBLUCAST<br>(reserved) |   |   |       | RWKPRCVD<br>MGKPRCVD |   | (reserved) |   | RWKPKTEN<br>MGKPKTEN |   | PWRDWN |  |
|--------------------------|----|----|----|--------|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|----|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------|---|---|-------|----------------------|---|------------|---|----------------------|---|--------|--|
| 31                       | 30 | 29 | 28 | 24     |   |   |   |   |   |   |   |   |   |   |   |   |   | 23         | 10 |   |   |   |   |   |   |   |   |   |   |   |   |                         | 9 | 8 | 7     | 6                    | 5 | 4          | 3 | 2                    | 1 | 0      |  |
| 0                        | 0  | 0  | 0  | 0      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 0 | Reset |                      |   |            |   |                      |   |        |  |

**RWKFILTRST** Configures whether to reset the RWKPTR register.

0: Release from reset

1: Reset

(R/WS/SC)

**RWKPTR** Configures the purpose of the PMT\_RWUFR register. For details, see the description of PMT\_RWUFR. (RO)

**GLBLUCAST** Configures whether to enable the unicast frame of target address filter as the wakeup frame.

0: Disable

1: Enable

(R/W)

**RWKPRCVD** Represents whether a remote wakeup frame event has been received.

0: Not received

1: Received

(R/SS/RC)

**MGKPRCVD** Represents whether a magic frame event has been received.

0: Not received

1: Received

(R/SS/RC)

**RWKPKTEN** Configures whether to enable power management events using remote wakeup frames.

0: Disable

1: Enable

(R/W)

**MGKPKTEN** Configures whether to enable power management events using magic frames.

0: Disable

1: Enable

(R/W)

**PWRDWN** Configures whether the EMAC receiver drops all received frames until it receives the expected magic frame or remote wakeup frame.

Valid only when MGKPKTEN, GLBLUCAST or RWKPKTEN is 1. (R/WS/SC)

**Register 47.25. EMACLPI\_CSR\_REG (0x0030)**

| (reserved) |   |   |   |   |   |   |   |   |   |   |   | LPITXA<br>(reserved)<br>PLS<br>LPIEN |    |    |    | (reserved) |    |   |   | RLPIST<br>TLPIST |   | (reserved) |   | RLPIEX<br>RLPIEN<br>TLPIEX<br>TLPIEN |   |   |   |   |   |   |   |       |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|--------------------------------------|----|----|----|------------|----|---|---|------------------|---|------------|---|--------------------------------------|---|---|---|---|---|---|---|-------|---|---|
| 31         |   |   |   |   |   |   |   |   |   |   |   | 20                                   | 19 | 18 | 17 | 16         | 15 |   |   |                  |   | 10         | 9 | 8                                    | 7 |   |   |   |   | 4 | 3 | 2     | 1 | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0  | 0  | 0  | 0          | 0  | 0 | 0 | 0                | 0 | 0          | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |   |   |

Reset

**LPITXA** Configures the behavior of the MAC when it is entering or coming out of the LPI mode on the transmit side.

0: This bit directly controls behavior of the MAC when it is entering or coming out of the LPI mode.

1: This bit controls behavior of the MAC when it is entering or coming out of the LPI mode in combination with LPIEN. When LPIEN is also 1, the MAC enters the LPI mode only after all outstanding frames (in the core) and pending frames (in the application interface) have been transmitted. The MAC comes out of the LPI mode when the application sends any frame for transmission

(R/W)

**PLS** Configures the link status of the PHY.

0: Link up

1: Link down

(R/W)

**LPIEN** Configures whether the EMAC transmitter enters the LPI state.

0: Exit

1: Enter

This bit is cleared when the LPITXA bit is set and the MAC exits the LPI state because of the arrival of a new packet for transmission.

(R/W/SC)

**RLPIST** Represents the receive LPI state.

0: Inactive

1: The EMAC is receiving the LPI pattern

(RO)

**TLPIST** Represents the transmit LPI state.

0: Inactive

1: The EMAC is transmitting the LPI pattern

(RO)

**RLPIEX** Represents the receive LPI exit state.

0: Inactive

1: The EMAC Receiver has stopped receiving the LPI pattern, exited the LPI state, and resumed the normal reception

(R/SS/RC)

Continued on the next page...

Register 47.25. EMACLPI\_CSR\_REG (0x0030)

Continued from the previous page...

- RLPIEN** Represents the receive LPI entry state.  
0: Inactive  
1: The EMAC Receiver has received an LPI pattern and entered the LPI state (R/SS/RC)
- TLPIEX** Represents the transmit LPI exit state.  
0: Inactive  
1: The EMAC transmitter has exited the LPI state after the user has cleared the LPIEN bit and the LPI\_TW\_TIMER has expired (R/SS/RC)
- TLPIEN** Represents the transmit LPI entry state.  
0: Inactive  
1: The EMAC Transmitter has entered the LPI state because of the setting of the LPIEN bit (R/SS/RC)

Register 47.26. EMACLPITIMERSCONTROL\_REG (0x0034)

|            |    |   |   |   |   |              |    |   |  |   |  |   |  |              |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|----|---|---|---|---|--------------|----|---|--|---|--|---|--|--------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |    |   |   |   |   | LPI_LS_TIMER |    |   |  |   |  |   |  | LPI_TW_TIMER |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31         | 26 |   |   |   |   | 25           | 16 |   |  |   |  |   |  |              | 15 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 0          | 0  | 0 | 0 | 0 | 0 | 0            | 0  | x |  | 3 |  | E |  | 8            | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

- LPI\_LS\_TIMER** Configures the minimum time for which the link status from the PHY should be up.  
Measurement unit: millisecond.  
The default value is 1000 (1 second) as defined in the IEEE standard.  
(R/W)
- LPI\_TW\_TIMER** Configures the minimum time for which the MAC waits after it stops transmitting the LPI pattern to the PHY and before it resumes the normal transmission.  
Measurement unit: millisecond.  
The TLPIEX status bit is set after the expiry of this timer.  
(R/W)

### Register 47.27. EMACINTS\_REG (0x0038)

[illegible]

**LPIINTS** The raw interrupt status of EMAC\_LPI\_INT. (RO)

**TINTS** The raw interrupt status of TS\_TRI\_INT. (R/SS/RC)

**PMTINTS** The raw interrupt status of EMAC\_PMP\_INT. (RO)

### Register 47.28. EMACINTMASK\_REG (0x003C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |           |   |           |   |            |   |            |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------|---|-----------|---|------------|---|------------|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPINTMASK |   | TSINTMASK |   | (reserved) |   | PMTINTMASK |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 11        |   | 10        | 9 | 8          |   | 4          |   | 3          | 2 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0         | 0 | 0         | 0 | 0          | 0 | 0          | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LPIINTMASK** Write 1 to mask EMAC\_LPI\_INT.(R/W)

**TSINTMASK** Write 1 to mask TS\_TRI\_INT. (R/W)

**PMTINTMASK** Write 1 to mask EMAC\_PMP\_INT. (R/W)

### Register 47.29. EMACADDROHIGH\_REG (0x0040)

|        |    |    |    |   |
|--------|----|----|----|---|
| 31     | 30 | 16 | 15 | 0 |
| 1      | 0  | 0  | 0  | 0 |
| 0xFFFF |    |    |    |   |

Reset

**ADDRESS\_ENABLE0** This bit is always set to 1. (RO)

**MAC\_ADDRESS0\_HI** Configures the upper 16 bits of the first 6-byte MAC address [47:32].

The MAC uses this field for filtering the received frames and inserting the MAC address in the Transmit Flow Control (PAUSE) Frames. (R/W)

**Register 47.30. EMACADDR0LOW\_REG (0x0044)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR0LOW\_REG** Configures the lower 32 bits of the first 6-byte MAC address.

The MAC uses this field for filtering the received frames and inserting the MAC address in the Transmit Flow Control (PAUSE) Frames. (R/W)

**Register 47.31. EMACADDR1HIGH\_REG (0x0048)**

|                                   |    |                   |      |            |   |   |   |   |   |    |    |                 |  |  |  |  |  |         |       |
|-----------------------------------|----|-------------------|------|------------|---|---|---|---|---|----|----|-----------------|--|--|--|--|--|---------|-------|
| ADDRESS_ENABLE1<br>SOURCE_ADDRESS |    | MASK_BYTE_CONTROL |      | (reserved) |   |   |   |   |   |    |    | MAC_ADDRESS1_HI |  |  |  |  |  |         |       |
|                                   |    |                   |      |            |   |   |   |   |   |    |    |                 |  |  |  |  |  |         |       |
| 31                                | 30 | 29                | 24   | 23         |   |   |   |   |   | 16 | 15 |                 |  |  |  |  |  |         | 0     |
| 0                                 | 0  |                   | 0x00 | 0          | 0 | 0 | 0 | 0 | 0 | 0  | 0  |                 |  |  |  |  |  | 0x0FFFF | Reset |

**ADDRESS\_ENABLE1** Configures whether to enable perfect filtering using the second MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS** Configures whether to which fields of the received frame EMACADDR1 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR1.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR1HIGH\_REG[15:8]

Bit[28]: EMACADDR1HIGH\_REG[7:0]

Bit[27]: EMACADDR1LOW\_REG[31:24]

Bit[24]: EMACADDR1LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.(R/W)

**MAC\_ADDRESS1\_HI** Configures the upper 16 bits of the second 6-byte MAC address [47:32]. (R/W)

**Register 47.32. EMACADDR1LOW\_REG (0x004C)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR1LOW\_REG** Configures the lower 32 bits of the second 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.33. EMACADDR2HIGH\_REG (0x0050)**

|                                    |    |                    |    |            |    |                 |       |
|------------------------------------|----|--------------------|----|------------|----|-----------------|-------|
| ADDRESS_ENABLE2<br>SOURCE_ADDRESS2 |    | MASK_BYTE_CONTROL2 |    | (reserved) |    | MAC_ADDRESS2_HI |       |
|                                    |    |                    |    |            |    |                 |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15              | 0     |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0               | 0     |
| 0x0FFF                             |    |                    |    |            |    |                 | Reset |

**ADDRESS\_ENABLE2** Configures whether to enable perfect filtering using the third MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS2** Configures whether to which fields of the received frame EMACADDR2 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL2** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR2.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR2HIGH\_REG[15:8]

Bit[28]: EMACADDR2HIGH\_REG[7:0]

Bit[27]: EMACADDR2LOW\_REG[31:24]

Bit[24]: EMACADDR2LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.(R/W)

**MAC\_ADDRESS2\_HI** Configures the upper 16 bits of the third 6-byte MAC address [47:32]. (R/W)

**Register 47.34. EMACADDR2LOW\_REG (0x0054)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR2LOW\_REG** Configures the lower 32 bits of the third 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.35. EMACADDR3HIGH\_REG (0x0058)**

|                 |    |                 |    |                    |    |            |   |                 |   |        |       |
|-----------------|----|-----------------|----|--------------------|----|------------|---|-----------------|---|--------|-------|
| ADDRESS_ENABLE3 |    | SOURCE_ADDRESS3 |    | MASK_BYTE_CONTROL3 |    | (reserved) |   | MAC_ADDRESS3_HI |   |        |       |
| 31              | 30 | 29              | 24 | 23                 | 16 | 15         | 0 |                 |   |        |       |
| 0               | 0  | 0x00            |    | 0                  | 0  | 0          | 0 | 0               | 0 | 0x0FFF | Reset |

**ADDRESS\_ENABLE3** Configures whether to enable perfect filtering using the fourth MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS3** Configures whether to which fields of the received frame EMACADDR3 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL3** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR3.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR3HIGH\_REG[15:8]

Bit[28]: EMACADDR3HIGH\_REG[7:0]

Bit[27]: EMACADDR3LOW\_REG[31:24]

Bit[24]: EMACADDR3LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. (R/W)

**MAC\_ADDRESS3\_HI** Configures the upper 16 bits of the fourth 6-byte MAC address [47:32]. (R/W)

**Register 47.36. EMACADDR3LOW\_REG (0x005C)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR3LOW\_REG** Configures the lower 32 bits of the fourth 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.37. EMACADDR4HIGH\_REG (0x0060)**

|                                    |    |                    |    |            |    |                 |       |
|------------------------------------|----|--------------------|----|------------|----|-----------------|-------|
| ADDRESS_ENABLE4<br>SOURCE_ADDRESS4 |    | MASK_BYTE_CONTROL4 |    | (reserved) |    | MAC_ADDRESS4_HI |       |
|                                    |    |                    |    |            |    |                 |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15              | 0     |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0               | 0     |
| 0x0FFF                             |    |                    |    |            |    |                 | Reset |

**ADDRESS\_ENABLE4** Configures whether to enable perfect filtering using the fifth MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS4** Configures whether to which fields of the received frame EMACADDR4 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL4** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR4.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR4HIGH\_REG[15:8]

Bit[28]: EMACADDR4HIGH\_REG[7:0]

Bit[27]: EMACADDR4LOW\_REG[31:24]

Bit[24]: EMACADDR4LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.(R/W)

**MAC\_ADDRESS4\_HI** Configures the upper 16 bits of the fifth 6-byte MAC address [47:32]. (R/W)



**Register 47.38. EMACADDR4LOW\_REG (0x0064)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR4LOW\_REG** Configures the lower 32 bits of the fifth 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.39. EMACADDR5HIGH\_REG (0x0068)**

|                                    |    |                    |    |            |    |                 |   |   |   |        |       |
|------------------------------------|----|--------------------|----|------------|----|-----------------|---|---|---|--------|-------|
| ADDRESS_ENABLE5<br>SOURCE_ADDRESS5 |    | MASK_BYTE_CONTROL5 |    | (reserved) |    | MAC_ADDRESS5_HI |   |   |   |        |       |
|                                    |    |                    |    |            |    |                 |   |   |   |        |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15              | 0 |   |   |        |       |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0               | 0 | 0 | 0 | 0x0FFF | Reset |

**ADDRESS\_ENABLE5** Configures whether to enable perfect filtering using the sixth MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS5** Configures whether to which fields of the received frame EMACADDR5 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL5** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR5.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR5HIGH\_REG[15:8]

Bit[28]: EMACADDR5HIGH\_REG[7:0]

Bit[27]: EMACADDR5LOW\_REG[31:24]

Bit[24]: EMACADDR5LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address.(R/W)

**MAC\_ADDRESS5\_HI** Configures the upper 16 bits of the sixth 6-byte MAC address [47:32]. (R/W)

**Register 47.40. EMACADDR5LOW\_REG (0x006C)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR5LOW\_REG** Configures the lower 32 bits of the sixth 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.41. EMACADDR6HIGH\_REG (0x0070)**

|                                    |    |                    |    |            |    |                 |       |
|------------------------------------|----|--------------------|----|------------|----|-----------------|-------|
| ADDRESS_ENABLE6<br>SOURCE_ADDRESS6 |    | MASK_BYTE_CONTROL6 |    | (reserved) |    | MAC_ADDRESS6_HI |       |
|                                    |    |                    |    |            |    |                 |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15              | 0     |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0               | 0     |
| 0x0FFF                             |    |                    |    |            |    |                 | Reset |

**ADDRESS\_ENABLE6** Configures whether to enable perfect filtering using the seventh MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS6** Configures whether to which fields of the received frame EMACADDR 6[47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL6** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR6.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR6HIGH\_REG[15:8]

Bit[28]: EMACADDR6HIGH\_REG[7:0]

Bit[27]: EMACADDR6LOW\_REG[31:24]

Bit[24]: EMACADDR6LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. (R/W)

**MAC\_ADDRESS6\_HI** Configures the upper 16 bits of the seventh 6-byte MAC address [47:32]. (R/W)

**Register 47.42. EMACADDR6LOW\_REG (0x0074)**

|            |   |
|------------|---|
| 31         | 0 |
| 0xFFFFFFFF |   |
| Reset      |   |

**EMACADDR6LOW\_REG** Configures the lower 32 bits of the seventh 6-byte MAC address.  
 The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.43. EMACADDR7HIGH\_REG (0x0078)**

|                                    |    |                    |    |            |    |    |   |   |   |   |   |                 |  |   |  |  |  |  |       |
|------------------------------------|----|--------------------|----|------------|----|----|---|---|---|---|---|-----------------|--|---|--|--|--|--|-------|
| ADDRESS_ENABLE7<br>SOURCE_ADDRESS7 |    | MASK_BYTE_CONTROL7 |    | (reserved) |    |    |   |   |   |   |   | MAC_ADDRESS7_HI |  |   |  |  |  |  |       |
|                                    |    |                    |    |            |    |    |   |   |   |   |   |                 |  |   |  |  |  |  |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15 |   |   |   |   |   |                 |  | 0 |  |  |  |  |       |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0x0FFF          |  |   |  |  |  |  | Reset |

**ADDRESS\_ENABLE7** Configures whether to enable perfect filtering using the eighth MAC address.  
 0: Disable  
 1: Enable  
 (R/W)

**SOURCE\_ADDRESS7** Configures whether to which fields of the received frame EMACADDR7 [47:0] compares.  
 0: The DA fields  
 1: The SA fields  
 (R/W)

**MASK\_BYTE\_CONTROL7** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR7.

0: Unmask  
 1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR7HIGH\_REG[15:8]

Bit[28]: EMACADDR7HIGH\_REG[7:0]

Bit[27]: EMACADDR7LOW\_REG[31:24]

Bit[24]: EMACADDR7LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. (R/W)

**MAC\_ADDRESS7\_HI** Configures the upper 16 bits of the eighth 6-byte MAC address [47:32]. (R/W)

**Register 47.44. EMACADDR7LOW\_REG (0x007C)**

|            |   |
|------------|---|
| 31         | 0 |
| 0x0FFFFFFF |   |
| Reset      |   |

**EMACADDR7LOW\_REG** Configures the lower 32 bits of the eighth 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.45. EMACADDR8HIGH\_REG (0x0080)**

|                                    |    |                    |    |            |    |                 |       |
|------------------------------------|----|--------------------|----|------------|----|-----------------|-------|
| ADDRESS_ENABLE8<br>SOURCE_ADDRESS8 |    | MASK_BYTE_CONTROL8 |    | (reserved) |    | MAC_ADDRESS8_HI |       |
|                                    |    |                    |    |            |    |                 |       |
| 31                                 | 30 | 29                 | 24 | 23         | 16 | 15              | 0     |
| 0                                  | 0  | 0x00               |    | 0          | 0  | 0               | 0     |
| 0x0FFF                             |    |                    |    |            |    |                 | Reset |

**ADDRESS\_ENABLE8** Configures whether to enable perfect filtering using the ninth MAC address.

0: Disable

1: Enable

(R/W)

**SOURCE\_ADDRESS8** Configures whether to which fields of the received frame EMACADDR8 [47:0] compares.

0: The DA fields

1: The SA fields

(R/W)

**MASK\_BYTE\_CONTROL8** Configures whether to mask MAC address byte bytes when comparing the received DA or SA with the contents of EMACADDR8.

0: Unmask

1: Mask

The correspondence between the mask control bits and the bytes:

Bit[29]: EMACADDR8HIGH\_REG[15:8]

Bit[28]: EMACADDR8HIGH\_REG[7:0]

Bit[27]: EMACADDR8LOW\_REG[31:24]

Bit[24]: EMACADDR8LOW\_REG[7:0]

You can filter a group of addresses (known as group address filtering) by masking one or more bytes of the address. (R/W)

**MAC\_ADDRESS8\_HI** Configures the upper 16 bits of the ninth 6-byte MAC address [47:32]. (R/W)

**Register 47.46. EMACADDR8LOW\_REG (0x0084)**

|            |   |
|------------|---|
| 31         | 0 |
| 0x0FFFFFFF |   |
| Reset      |   |

**EMACADDR8LOW\_REG** Configures the lower 32 bits of the ninth 6-byte MAC address.

The content of this field is undefined until loaded by the Application after the initialization process. (R/W)

**Register 47.47. EMACSTATUS\_REG (0x00D8)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |   |  |  |            |  |  |  |           |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |  |  |   |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|---|--|--|------------|--|--|--|-----------|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|--|--|---|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved) |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | JABBER_TIMEOUT |   |  |  | (reserved) |  |  |  | LINK_MODE |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |  |  |   |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16         | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                | 5 |  |  |            |  |  |  |           |  |  |  |  |  |  |  |  | 4 | 3 | 1 |   |   |   | 0 |  |  |   |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0          | 0  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                | 0 |  |  |            |  |  |  |           |  |  |  |  |  |  |  |  | 0 | 0 | 0 | 0 | 0 | 0 |   |  |  | 0 |
| Reset      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |            |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |   |  |  |            |  |  |  |           |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |  |  |   |

**JABBER\_TIMEOUT** Represents whether a receive jabber error occurs.

0: Not occur

1: Occur

(RO)

**LINK\_MODE** Represents the current mode of operation of the link.

0: Half-duplex

1: Full-duplex

(RO)

**Register 47.48. EMACWDOGTO\_REG (0x00DC)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |         |  |            |    |        |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------|--|------------|----|--------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PWDOGEN |  | (reserved) |    | WDOGTO |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |  |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17      |  | 16         | 15 | 14     | 13 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |  |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0       |  | 0          | 0  | 0x0000 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |  |

**PWDOGEN** Configures whether the watchdog timeout is programmable.

0: Not programmable. The watchdog timeout for a received frame is controlled by the setting of EMACCONFIG\_REG[23] (WD) and EMACCONFIG\_REG[20] (JE).

1: Programmable via the WDOGTO field if EMACCONFIG\_REG[23] (WD) is 0.

(R/W)

**WDOGTO** Configures the watchdog timeout for a received frame when PWDOGEN is 1 and EMACCONFIG\_REG[23] (WD) is 0.

If the length of a received frame exceeds the value of this field, such frame is terminated and declared as an error frame. (R/W)

**Register 47.49. EMAXVLTCTRL\_REG (0x0584)**

|            |   |   |   |   |   |   |   |   |   |   |   |      |    |     |     |     |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|------|----|-----|-----|-----|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | CSVL |    | VLP | VLC | VLT |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 20   | 19 | 18  | 17  | 16  | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0    | 0  | 0   | 0   | 0   |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**CSVL** Configures which type is inserted or replaced in the 13th and 14th bytes of transmitted frames.

0: C-VLAN type (0x8100)

1: S-VLAN type (0x88A8)

(R/W)

**VLP** Configures what controls VLAN deletion, insertion, or replacement.

0: The control input signal

1: VLC

(R/W)

**VLC** Configures the VLAN tag in transmit frames.

0: No VLAN tag deletion, insertion, or replacement.

1: VLAN tag deletion. The MAC removes the VLAN type (bytes 13 and 14) and VLAN tag (bytes 15 and 16) of all transmitted frames with VLAN tags.

2: VLAN tag insertion. The MAC inserts VLT in bytes 15 and 16 of the frame after inserting the Type value (0x8100/0x88a8) in bytes 13 and 14. This operation is performed on all transmitted frames, irrespective of whether they already have a VLAN tag.

3: VLAN tag replacement. The MAC replaces VLT in bytes 15 and 16 of all VLAN-type transmitted frames (Bytes 13 and 14 are 0x8100/0x88a8).

(R/W)

**VLT** Configures the value of the VLAN tag to be inserted or replaced.

The value must only be changed when the transmit lines are inactive or during the initialization phase. (R/W)

**Register 47.50. EMACTSTPCTRL\_REG (0x0700)**

| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  | TSENMACADDR |  | SNAPTYPSEL |  | TSMSTRENA |  | TSEVNTENA |  | TSIPV4ENA |  | TSIPV6ENA |  | TSVER2ENA |  | TSCTRLSSR |  | TSEWALL |  | (reserved) |  | TSADDRREG |  | TSTRIG |  | TSUPDT |  | TSINIT |  | TSCFUPDT |  | TSENA |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  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 |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  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|  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  | 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 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 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|  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |

**TSENMACADDR** Configures whether to enable the DA MAC address (that matches any MAC Address register) for PTP frame filtering when PTP is directly sent over Ethernet.

0: Disable

1: Enable

(R/W)

**SNAPTYPSEL** Configures the set of PTP packet types for which snapshot needs to be taken, in combination with TSMSTRENA and TSEVNTENA.

SNAPTYPSEL, TSMSTRENA, TSEVNTENA:

00x0: SYNC, Follow\_Up, Delay\_Req, Delay\_Resp

0001: SYNC

0011: Delay\_Req

01x0: SYNC, Follow\_Up, Delay\_Req, Delay\_Resp, Pdelay\_Req, Pdelay\_Resp, Pdelay\_Resp\_Follow\_Up

0101: SYNC, Pdelay\_Req, Pdelay\_Resp

0111: Delay\_Req, Pdelay\_Req, Pdelay\_Resp

10xx: SYNC, Delay\_Req

11xx: Pdelay\_Req, Pdelay\_Resp

(R/W)

**TSMSTRENA** Configures whether to enable snapshot only for messages relevant to the master node.

0: Disable. The snapshot is taken for the messages relevant to the slave node

1: Enable

(R/W)

**TSEVNTENA** Configures whether to enable timestamp snapshot only for event messages (SYNC, Delay\_Req, Pdelay\_Req, Pdelay\_Resp).

0: Disable. The snapshot is taken for all messages except Announce, Management, and Signaling

1: Enable

(R/W)

**TSIPV4ENA** Configures whether to enable the processing of PTP frames sent over IPv4-UDP.

0: Disable. The MAC ignores the PTP transported over UDP-IPv4 packets

1: Enable. The MAC receiver processes the PTP packets encapsulated in UDP over IPv4 packets

(R/W)

Continued on the next page...

**Register 47.50. EMACTSTPCTRL\_REG (0x0700)**

Continued from the previous page...

**TSIPV6ENA** Configures whether to enable the processing of PTP frames sent over IPv6-UDP.

0: Disable. The MAC ignores the PTP transported over UDP-IPv6 packets

1: Enable. The MAC receiver processes the PTP packets encapsulated in UDP over IPv6 packets

(R/W)

**TSIPENA** Configures whether to enable the processing of PTP sent over Ethernet frames.

0: Disable. the MAC ignores the PTP over Ethernet packets

1: Enable. The MAC receiver processes the PTP packets encapsulated directly in the Ethernet frames

(R/W)

**TSVER2ENA** Configures whether to enable PTP packet processing for version 2 format.

0: Disable. The PTP packets are processed using the version 1 format

1: Enable. The PTP packets are processed using the 1588 version 2 format

(R/W)

**TSCTRLSSR** Configures the timeout digital or binary rollover.

0: The Timestamp Low register rolls over after the value of the sub-second register 0x7FFF\_FFFF. The sub-second increment has to be programmed correctly depending on the PTP reference clock frequency and the value of this bit.

1: The Timestamp Low register rolls over after 0x3B9A\_C9FF value (that is, 1 nanosecond accuracy) and increments the timestamp (High) seconds.

(R/W)

**TSENALL** Configures whether to enable timestamp for all frames received by the MAC.

0: Disable

1: Enable

(R/W)

**TSADDREG** Configures whether to update the content of the EMACTSTPADDEND\_REG register in the PTP block for fine correction.

0: Not update

1: Update

This bit should be zero before setting it. (R/WS/SC)

Continued on the next page...



**Register 47.50. EMACTSTPCTRL\_REG (0x0700)**

Continued from the previous page...

**TSTRIG** Configures whether to enable the timestamp interrupt trigger.

0: Disable

1: Enable. The timestamp interrupt is generated when the System Time becomes greater than the value written in the Target Time register

(R/WS/SC)

**TSUPDT** Configures whether to update (add or subtract) the system time with the value specified in EMAC2NDUPT\_REG and EMACNSUPT\_REG.

0: Not update

1: Update

This bit should be read as zero before updating it.

EMACSYSTIMHIGHWORD2ND\_REG is not updated. (R/WS/SC)

**TSINIT** Configures whether to initialize (overwrite) the system time with the value specified in EMAC2NDUPT\_REG and EMACNSUPT\_REG.

0: Not initialize

1: Initialize

This bit should be read as zero before updating it.

EMACSYSTIMHIGHWORD2ND\_REG will be initialized. (R/WS/SC)

**TSCFUPDT** Configures the method used to update the system time.

0: Coarse method

1: Find update method

(R/W)

**TSENA** Configures whether to add the timestamp for the transmit and receive frames.

0: Not add the timestamp, and receive frames and the Timestamp Generator is also suspended

1: Add the timestamp

You need to initialize the Timestamp (system time) after setting this bit to 1.

On the receive side, the MAC processes the 1588 frames only if this bit is set. (R/W)

**Register 47.51. EMACSUB2NDINCR\_REG (0x0704)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SSINC |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8     | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00  |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**SSINC** Configures the value accumulated every clock cycle (PTP clock) with the contents of the sub-second register.

For example, when PTP clock is 50 MHz (the period is 20 ns), you should program 20 (0x14) when the System Time-Nanoseconds register has an accuracy of 1 ns (EMACTSTPCTRL\_REG[9], i.e., the TSCTRLSSR bit is set). When TSCTRLSSR is cleared, the Nanoseconds register has a resolution of 0.465 ns. In this case, you should program a value of 43 (0x2B) that is derived by  $20 \text{ ns} / 0.465$ . (R/W)

**Register 47.52. EMACSYSTIM2ND\_REG (0x0708)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**TSS** Represents the current value of the System Time maintained by the MAC.

Measurement unit: second. (RO)

**Register 47.53. EMACSYSTIMNS\_REG (0x070C)**

|            |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TSSS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**TSSS** Represents the sub-second representation of time, with an accuracy of 0.46 ns.

When EMACTSTPCTRL\_REG[9] (TSCTRLSSR) is set, each bit represents 1 ns and the maximum value is 0x3B9A\_C9FF. (RO)

**Register 47.54. EMAC2NDUPT\_REG (0x0710)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**TSSSUPD** Configures the time to be initialized or added to the system time.

Measurement unit: second. (R/W)

**Register 47.55. EMACNSUPT\_REG (0x0714)**

|    |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|----|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| 31 |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0  | 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**ADDSUB** with Configures whether to subtract or add the system time value the contents of the update register.

0: Add

1: Subtract

(R/W)

**TSSSUPD** Configures the sub-second representation of time, with an accuracy of 0.46 ns.

When EMACTSTPCTRL\_REG[9] (TSCTRLSSR) is set, each bit represents 1 ns and the programmed value should not exceed 0x3B9A\_C9FF. (R/W)

**Register 47.56. EMACTSTPADDEND\_REG (0x0718)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**TSAR** Configures the 32-bit time value to be added to the Accumulator register to achieve time synchronization. (R/W)

**Register 47.57. EMACTGTIME2ND\_REG (0x071C)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**TSTR** Configures the target time.

Measurement unit: second.

When the system time matches or exceeds the target time, an interrupt is generated (if enabled).

(R/W)

(reserved)

TTSLO

(R/W)

(reserved)

TSHWR

Seconds register. (R/W/SU)

Register 47.60. EMACTSTPSTATUS\_REG (0x0728)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TSTRGTERR<br>(reserved)<br>TSTARGET<br>TSSOVF |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4   | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**TSTRGTERR** Represents whether the target time, being programmed in EMACTGTIME2ND\_REG and EMACTGTIMENS\_REG, is already elapsed.

0: Not elapsed

1: Elapsed

(R/SS/RC)

**TSTARGET** Represents whether the system time is greater or equal to the value specified in EMACTGTIME2ND\_REG and EMACTGTIMENS\_REG.

0: Less than the value

1: Greater or equal to the value

(R/SS/RC)

**TSSOVF** Represents whether the second value of the timestamp has overflowed beyond 0xFFFF\_FFFF.

0: No overflow

1: Overflow

(R/SS/RC)

## Chapter 48

# Two-Wire Automotive Interface (TWAI)

The Two-wire Automotive Interface (TWAI®) is a multi-master, multi-cast communication protocol with functions such as error detection and signaling and inbuilt message priorities and arbitration. The TWAI protocol is suited for automotive and industrial applications (see Section 48.2 for more details).

ESP32-P4 contains three TWAI controllers, TWAI 0, TWAI 1, and TWAI 2. Each controller can individually be connected to a TWAI bus via an external transceiver. The TWAI controllers have many advanced features, and can be utilized in a wide range of use cases, such as automotive products, industrial automation controls, building automation, etc.

## 48.1 Features

Each TWAI controller on ESP32-P4 supports the following features:

- Compatibility with ISO 11898-1 protocol (CAN Specification 2.0)
- Standard Frame Format (11-bit ID) and Extended Frame Format (29-bit ID)
- Bit rates from 1 Kbit/s to 1 Mbit/s
- Multiple modes of operation:
  - Normal
  - Listen-only (no influence on bus)
  - Self-test (no acknowledgment required during data transmission)
- 64-byte Receive FIFO
- Special transmissions:
  - Single-shot transmissions (does not automatically re-transmit upon error)
  - Self-reception (the TWAI controller transmits and receives messages simultaneously)
- Acceptance Filter (supports Single and Dual-filter modes)
- Error detection and handling:
  - Error counters
  - Configurable error warning limit
  - Error code capture
  - Arbitration lost capture
  - Automatic transceiver standby

## 48.2 Protocol Overview

### 48.2.1 TWAI Properties

The TWAI protocol connects two or more nodes in a bus network, and allows nodes to exchange messages with deterministic delay. A TWAI bus has the following properties:

**Single Channel and Non-Return-to-Zero:** The bus has only one transmission line for single-channel communication, which is half-duplex. Synchronization is also implemented in this channel, so extra channels (e.g., clock or enable) are not required. The bit stream of a TWAI message is encoded using the Non-Return-to-Zero (NRZ) method.

**Bit Values:** The single channel can either be in a dominant or recessive state, representing a logical 0 and a logical 1 respectively. A node transmitting data in a dominant state always overrides the other node transmitting data in a recessive state. The physical implementation on the bus is left to the application level to decide (e.g., differential pair or a single wire).

**Bit Stuffing:** Certain fields of TWAI messages are bit-stuffed. A transmitter that transmits five consecutive bits of the same value (e.g., dominant value or recessive value) should automatically insert a complementary bit. Likewise, a receiver that receives five consecutive bits of the same value should treat the next bit as a stuffed bit. Bit stuffing is applied to the following fields: SOF, arbitration field, control field, data field, and CRC sequence (see Section [48.2.2](#) for more details).

**Multi-Cast:** All nodes receive the same bits as they are connected to the same bus. Data is consistent across all nodes unless there is a bus error (see Section [48.2.3](#) for more details).

**Multi-Master:** Any node can initiate a transmission. If a transmission is already ongoing, a node will wait until the current transmission is over before initiating a new transmission.

**Message Priority and Arbitration:** If two or more nodes simultaneously initiate a transmission, the TWAI protocol ensures that one node will win arbitration of the bus. The arbitration field of the message transmitted by each node is used to determine which node will win the arbitration.

**Error Detection and Signaling:** Each node actively monitors the bus for errors, and signals the detected errors by transmitting an error frame.

**Fault Confinement:** Each node maintains a set of error counters that are incremented/decremented according to a set of rules. When the error counters surpass a certain threshold, the node will automatically eliminate itself from the network by switching itself off.

**Configurable Bit Rate:** The bit rate for a single TWAI bus is configurable. However, all nodes on the same bus must operate at the same bit rate.

**Transmitters and Receivers:** At any point in time, a TWAI node can either be a transmitter or a receiver.

- A node generating a message is a transmitter. The node remains a transmitter until the bus is idle or until the node loses arbitration. Please note that there could be multiple nodes that act as transmitters during arbitration.
- All nodes that are not transmitters can work as receivers.

## 48.2.2 TWAI Messages

TWAI nodes use messages to transmit data, and signal errors to other nodes when detecting errors on the bus. Messages are split into various frame types, and different frame types have different frame formats.

The TWAI protocol has the following frame types:

- Data frame
- Remote frame
- Error frame
- Overload frame
- Interframe space

The TWAI protocol supports the following frame formats:

- Standard Frame Format (SFF) that uses a 11-bit identifier
- Extended Frame Format (EFF) that uses a 29-bit identifier

### 48.2.2.1 Data Frames and Remote Frames

Data frames are used by nodes to send data to other nodes, and can have a payload of 0 to 8 data bytes. Remote frames are used for nodes to request a data frame with the same identifier from other nodes, and thus they do not contain any data bytes. However, data frames and remote frames share many fields. Figure 48.2-1 illustrates the fields and sub-fields of different frames and formats.

#### Arbitration Field

When two or more nodes transmit data or remote frames simultaneously, the arbitration field is used to determine which node will win arbitration of the bus. In the arbitration field, if a node transmits a recessive bit while detecting a dominant bit, it indicates that another node has overridden its recessive bit. Therefore, the node transmitting the recessive bit has lost arbitration of the bus and should immediately switch to be a receiver.

The arbitration field primarily consists of a frame identifier that is transmitted from the most significant bit first. Given that a dominant bit represents a logical 0, and a recessive bit represents a logical 1:

- A frame with the smallest ID value always wins arbitration.
- Given the same ID and format, data frames always prevail over remote frames due to their **RTR** bits being dominant.
- Given the same first 11 bits of ID, a Standard Format Data Frame always prevails over an Extended Format Data Frame due to its **SRR** bits being recessive.

#### Control Field

The control field primarily consists of the Data Length Code (DLC) which indicates the number of payload data bytes for a data frame, or the number of requested data bytes for a remote frame. The DLC is transmitted from the most significant bit first.

#### Data Field

The data field contains the actual payload data bytes of a data frame. Remote frames do not contain any data field.



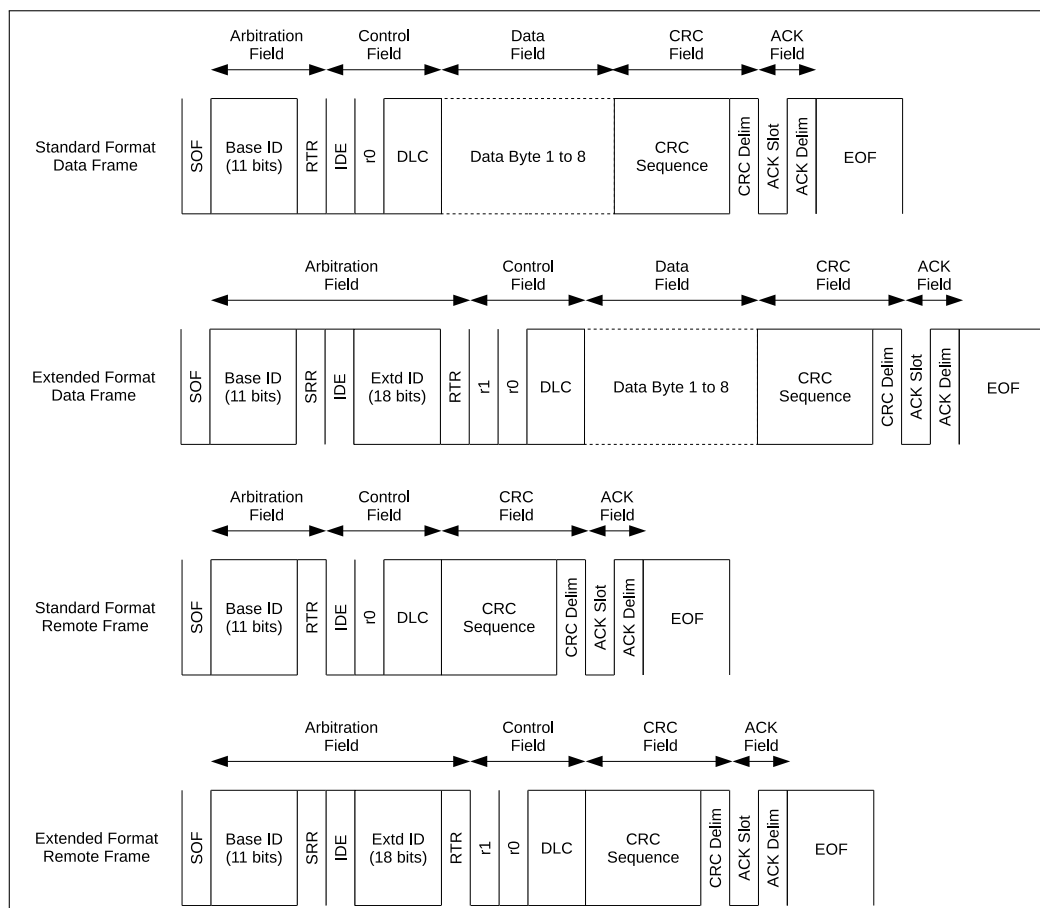


Figure 48.2-1. Bit Fields in Data Frames and Remote Frames

**CRC Field**

The CRC field primarily consists of a CRC sequence. The CRC sequence is a 15-bit cyclic redundancy code calculated from the de-stuffed contents (everything from the SOF to the end of the data field) of a data or remote frame.

**ACK Field**

The ACK field primarily consists of an ACK Slot and an ACK Delim. The ACK field indicates that the receiver has received an effective message from the transmitter.

Table 48.2-1. Data Frames and Remote Frames in SFF and EFF

| Data/Remote Frames | Description   |
|--------------------|---|
| SOF                | The SOF (Start of Frame) is a single dominant bit used to synchronize nodes on the bus.   |
| Base ID            | The Base ID (ID.28 to ID.18) is the 11-bit identifier for SFF, or the first 11 bits of the 29-bit identifier for EFF.   |
| RTR                | The RTR (Remote Transmission Request) bit indicates whether the message is a data frame (dominant) or a remote frame (recessive). This means that a remote frame will always lose arbitration to a data frame if they have the same ID. |

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Table 48.2-1 – cont'd from previous page

| Data/Remote Frames | Description  |
|--------------------|--|
| SRR                | The SRR (Substitute Remote Request) bit is transmitted in EFF to substitute for the RTR bit at the same position in SFF.   |
| IDE                | The IDE (Identifier Extension) bit indicates whether the message is SFF (dominant) or EFF (recessive). This means that a SFF frame will always win arbitration over an EFF frame if they have the same Base ID.  |
| Extd ID            | The Extended ID (ID.17 to ID.0) is the remaining 18 bits of the 29-bit identifier for EFF.   |
| r1                 | The r1 bit (reserved bit 1) is always dominant.  |
| r0                 | The r0 bit (reserved bit 0) is always dominant.  |
| DLC                | The DLC (Data Length Code) is 4-bit long and should contain any value from 0 to 8. Data frames use the DLC to indicate the number of data bytes in the data frame. Remote frames used the DLC to indicate the number of data bytes to request from another node.   |
| Data Bytes         | The data payload of data frames. The number of bytes should match the value of DLC. Data byte 0 is transmitted first, and each data byte is transmitted from the most significant bit first.   |
| CRC Sequence       | The CRC sequence is a 15-bit cyclic redundancy code.   |
| CRC Delim          | The CRC Delim (CRC Delimiter) is a single recessive bit that follows the CRC sequence.   |
| ACK Slot           | The ACK Slot (Acknowledgment Slot) is intended for receiver nodes to indicate that the data or remote frame was received without any issue. The transmitter node will send a recessive bit in the ACK Slot and receiver nodes should override the ACK Slot with a dominant bit if the frame was received without errors. |
| ACK Delim          | The ACK Delim (Acknowledgment Delimiter) is a single recessive bit.  |
| EOF                | The EOF (End of Frame) marks the end of a data or remote frame, and consists of seven recessive bits.  |

### 48.2.2.2 Error and Overload Frames

#### Error Frames

Error frames are transmitted when a node detects a bus error. Error frames notably include an Error Flag which is made up of six consecutive bits of the same value, thus violating the bit-stuffing rule. Therefore, when a particular node detects a bus error and transmits an error frame, all other nodes will then detect a stuff error and transmit their own error frames in response. This has the effect of propagating the detection of a bus error across all nodes on the bus.

When a node detects a bus error, it will transmit an error frame starting from the next bit. However, when a node detects a CRC error, the error frame will start at the bit following the ACK Delim (see Section 48.2.3 for more details). The following Figure 48.2-2 shows different fields of an error frame:

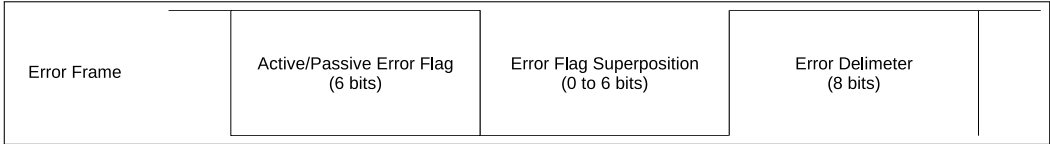


Figure 48.2-2. Fields of an Error Frame

Table 48.2-2. Error Frame

| Error Frame              | Description   |
|--------------------------|---|
| Error Flag               | The Error Flag has two forms, the <a href="#">Active Error Flag</a> consisting of six dominant bits and the <a href="#">Passive Error Flag</a> consisting of six recessive bits (unless overridden by dominant bits of other nodes). Active Error Flags are sent by error active nodes, whilst Passive Error Flags are sent by error passive nodes. |
| Error Flag Superposition | The Error Flag Superposition field meant to allow for other nodes on the bus to transmit their respective Active Error Flags. The superposition field can range from 0 to 6 bits, and ends when the first recessive bit is detected (i.e., the first it of the Delimiter).  |
| Error Delimeter          | The Delimiter field marks the end of the error/overload frame, and consists of eight recessive bits.  |

Overload Frames

An overload frame has the same bit fields as an error frame containing an Active Error Flag. The key difference is in the cases that can trigger the transmission of an overload frame. Figure 48.2-3 below shows the bit fields of an overload frame.

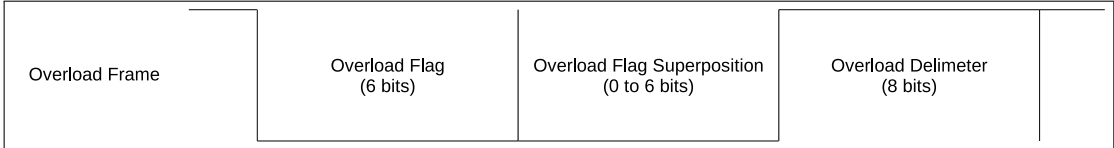


Figure 48.2-3. Fields of an Overload Frame

Table 48.2-3. Overload Frame

| Overload Flag               | Description  |
|-----------------------------|--|
| Overload Flag               | Consists of six dominant bits. Same as an Active Error Flag.   |
| Overload Flag Superposition | Allows for the superposition of Overload Flags from other nodes, similar to an Error Flag Superposition. |
| Overload Delimeter          | Consists of eight recessive bits. Same as an Error Delimeter.  |

Overload frames will be transmitted in the following cases:

- 1. A receiver requires a delay of the next data or remote frame.
- 2. A dominant bit is detected at the first and second bit of [intermission](#).

3. A dominant bit is detected at the eighth (last) bit of an Error Delimiter. Note that in this case, TEC and REC will not be incremented (see Section 48.2.3 for more details).

Transmitting an overload frame due to one of the above cases must also satisfy the following rules:

- The start of an overload frame due to case 1 is only allowed to be started at the first bit time of an expected intermission. In this case, a maximum of two overload frames may be generated.
- The start of an overload frame due to case 2 and 3 is only allowed to be started one bit after detecting the dominant bit.

### 48.2.2.3 Interframe Space

The Interframe Space acts as a separator between frames. Before sending, data frames and remote frames must be separated from preceding frames by an Interframe Space, regardless of the preceding frame's type (data frame, remote frame, error frame, or overload frame). However, error frames and overload frames do not need to be separated from preceding frames.

Figure 48.2-4 shows the fields within an Interframe Space:

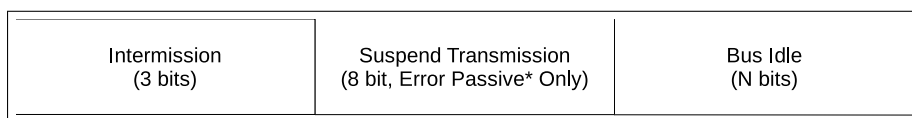


Figure 48.2-4. The Fields within an Interframe Space (\*Error Passive)

Table 48.2-4. Interframe Space

| Interframe Space     | Description   |
|----------------------|---|
| Intermission         | The Intermission consists of three recessive bits.  |
| Suspend Transmission | An Error Passive node that has just transmitted a message must include a Suspend Transmission field. This field consists of eight recessive bits. Error Active nodes should not include this field.       |
| Bus Idle             | The Bus Idle field is of arbitrary length. Bus Idle ends when an SOF is transmitted. If a node has a pending transmission, the SOF should be transmitted at the first bit following Suspend Transmission. |

## 48.2.3 TWAI Errors

### 48.2.3.1 Error Types

Bus Errors in TWAI are categorized into the following types:

#### Bit Error

A Bit Error occurs when a node transmits a bit value (i.e., dominant or recessive) but detects an opposite bit (e.g., a dominant bit is transmitted but a recessive is detected). However, if the transmitted bit is recessive and is located in the Arbitration Field, ACK Slot, or Passive Error Flag, then detecting a dominant bit will not be considered as a Bit Error.

#### Stuff Error

A stuff error occurs when six consecutive bits of the same value are detected (which violates the bit-stuffing encoding rules).

#### CRC Error

The receiver will calculate the CRC value based on the valid bits of received data frames and remote frames (before bit stuffing). A CRC Error occurs when the CRC calculated by the receiver does not match the CRC sequence in the received data frames and remote frames.

#### Format Error

A Format Error occurs when a format-fixed bit field of a message contains an illegal bit. For example, the r1 and r0 fields must be dominant.

#### ACK Error

An ACK Error occurs when a transmitter does not detect a dominant bit at the ACK Slot.

### 48.2.3.2 Error States

TWAI nodes implement fault confinement by maintaining two error counters in each node, where the counter values determine the error state. The two error counters are known as the Transmit Error Counter (TEC) and Receive Error Counter (REC). TWAI has the following error states:

#### Error Active

An Error Active node is able to participate in bus communication and transmit an Active Error Flag when it detects an error.

#### Error Passive

An Error Passive node is able to participate in bus communication and transmit a Passive Error Flag when it detects an error. Error Passive nodes that have transmitted data or remote frames must also include the Suspend Transmission field in the subsequent Interframe Space.

#### Bus Off

A Bus Off node is not permitted to influence the bus in any way (i.e., is not allowed to transmit data).

### 48.2.3.3 Error State Transition

1. A node becomes Error Passive when its TEC and/or REC is greater than or equal to 128. Though the node becomes Error Passive, it still sends an Active Error Flag. Note that once the REC has reached 128, any further increases to its value are invalid until the REC returns to a value less than 128.
2. A node becomes Bus Off when its TEC is greater than or equal to 256.
3. An Error Passive node becomes Error Active when both the TEC and REC are less than or equal to 127.
4. A Bus Off node can become Error Active (with both its TEC and REC reset to 0) after it monitors 128 occurrences of 11 consecutive recessive bits on the bus.

### 48.2.3.4 Error Counter Rules

The TEC and REC are incremented/decremented according to the following rules. **Note that more than one rule can apply to a given message transfer.**

**TEC increment/decrement rules:**

1. When a transmitter sends an Error Flag, the TEC is increased by 8. However, the following scenarios are exempt from this rule:
  - A transmitter is Error Passive and no dominant bit is detected when an Acknowledgment Error is detected and the Passive Error Flag is sent. In this case, the TEC should not be increased.
  - A transmitter transmits an Error Flag due to a Stuff Error during Arbitration. If the stuffed bit should have been recessive but was monitored as dominant, then the TEC should not be increased.
2. If a transmitter detects a Bit Error while sending an Active Error Flag or Overload Flag, the TEC is increased by 8.
3. A node can tolerate up to 7 consecutive dominant bits after sending an Active/Passive Error Flag, or Overload Flag. After detecting the 14th consecutive dominant bit when sending an Active Error Flag or Overload Flag, or the 8th consecutive dominant bit following a Passive Error Flag, a transmitter will increase its TEC by 8 and a receiver will increase its REC by 8. Every additional 8 consecutive dominant bits will also increase the TEC for transmitters or REC for receivers by 8 as well.
4. When a transmitter has transmitted a message, which means getting ACK and no errors until the EOF is completed, the TEC is decremented by 1, unless the TEC is already at 0.

**REC increment/decrement rules:**

1. When a receiver detects a dominant bit as the first bit after sending an Error Flag, the REC is increased by 8.
2. When a receiver detects an error, the REC is increased by 1, except when the detected error was a Bit Error during the transmission of an Active Error Flag or an Overload Flag.
3. If a receiver detects a Bit Error while sending an Active Error Flag or Overload Flag, the REC is increased by 8.
4. When a receiver successfully receives a message, which means getting no errors before ACK Slot and successfully sending ACK, the REC is decremented accordingly.
  - If the REC is between 1 and 127, it will be decremented by 1.
  - If the REC is greater than 127, it will be set to 127.
  - If the REC is 0, it will remain 0.

## 48.2.4 TWAI Bit Timing

### 48.2.4.1 Nominal Bit

The TWAI protocol allows a TWAI bus to operate at a particular bit rate. However, all nodes within a TWAI bus must operate at the same bit rate.

- **The Nominal Bit Rate** is defined as the number of bits transmitted per second.
- **The Nominal Bit Time** is defined as  $1/\text{Nominal Bit Rate}$ .

A single Nominal Bit Time is divided into multiple segments, and each segment is made up of multiple Time Quanta. A **Time Quantum** is a minimum unit of time, and is implemented as some form of prescaled clock signal in each node. Figure 48.2-5 illustrates the segments within a single Nominal Bit Time.

TWAI controllers will operate in time steps of one Time Quanta where the state of the TWAI bus is analyzed. If the bus states in two consecutive Time Quanta are different (i.e., recessive to dominant or vice versa), an edge is generated. The intersection of PBS1 and PBS2 is considered the Sample Point and the sampled bus value is considered the value of that bit.

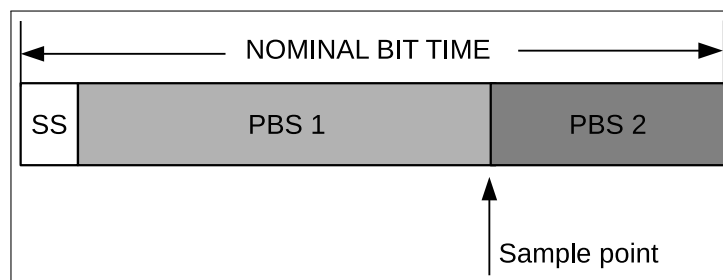


Figure 48.2-5. Layout of a Bit

Table 48.2-5. Segments of a Nominal Bit Time

| Segment | Description   |
|---------|---|
| SS      | The SS (Synchronization Segment) is 1 Time Quantum long. If all nodes are perfectly synchronized, the edge of a bit will lie in the SS.   |
| PBS1    | PBS1 (Phase Buffer Segment 1) can be 1 to 16 Time Quanta long. PBS1 is meant to compensate for the physical delay times within the network. PBS1 can also be lengthened for synchronization purposes. |
| PBS2    | PBS2 (Phase Buffer Segment 2) can be 1 to 8 Time Quanta long. PBS2 is meant to compensate for the information processing time of nodes. PBS2 can also be shortened for synchronization purposes.      |

#### 48.2.4.2 Hard Synchronization and Resynchronization

Due to clock skew and jitter, the bit timing of nodes on the same bus may become out of phase. Therefore, a bit edge may come before or after the SS. To ensure that the internal bit timing clocks of each node are kept in phase, TWAI has various methods of synchronization. The **Phase Error “e”** is measured in the number of Time Quanta and relative to the SS.

- A positive Phase Error ( $e > 0$ ) is when the edge lies after the SS and before the Sample Point (i.e., the edge is late).
- A negative Phase Error ( $e < 0$ ) is when the edge lies after the Sample Point of the previous bit and before SS (i.e., the edge is early).

To correct Phase Errors, there are two forms of synchronization, known as **Hard Synchronization** and **Resynchronization**. **Hard Synchronization** and **Resynchronization** obey the following rules:

- Only one synchronization may occur in a single bit time.
- Synchronizations only occur on recessive to dominant edges.

##### Hard Synchronization

Hard Synchronization occurs on the recessive to dominant (i.e., the first SOF bit after Bus Idle) edges when the bus is idle. All nodes will restart their internal bit timings so that the recessive to dominant edge lies within the SS of the restarted bit timing.

## Resynchronization

Resynchronization occurs on recessive to dominant edges when the bus is not idle. If the edge has a positive Phase Error ( $e > 0$ ), PBS1 is lengthened by a certain number of Time Quanta. If the edge has a negative Phase Error ( $e < 0$ ), PBS2 will be shortened by a certain number of Time Quanta.

The number of Time Quanta to lengthen or shorten depends on the magnitude of the Phase Error, and is also limited by the Synchronization Jump Width (SJW) value which is programmable.

- When the magnitude of the Phase Error (**e**) is less than or equal to the SJW, PBS1/PBS2 are lengthened/shortened by the **e** number of Time Quanta. This has the same effect as Hard Synchronization.
- When the magnitude of the Phase Error is greater than the SJW, PBS1/PBS2 are lengthened/shortened by the SJW number of Time Quanta. This means it may take multiple bits of synchronization before the Phase Error is entirely corrected.

## 48.3 Architectural Overview

The major functional blocks of the TWAI controller are shown in Figure 48.3-1.

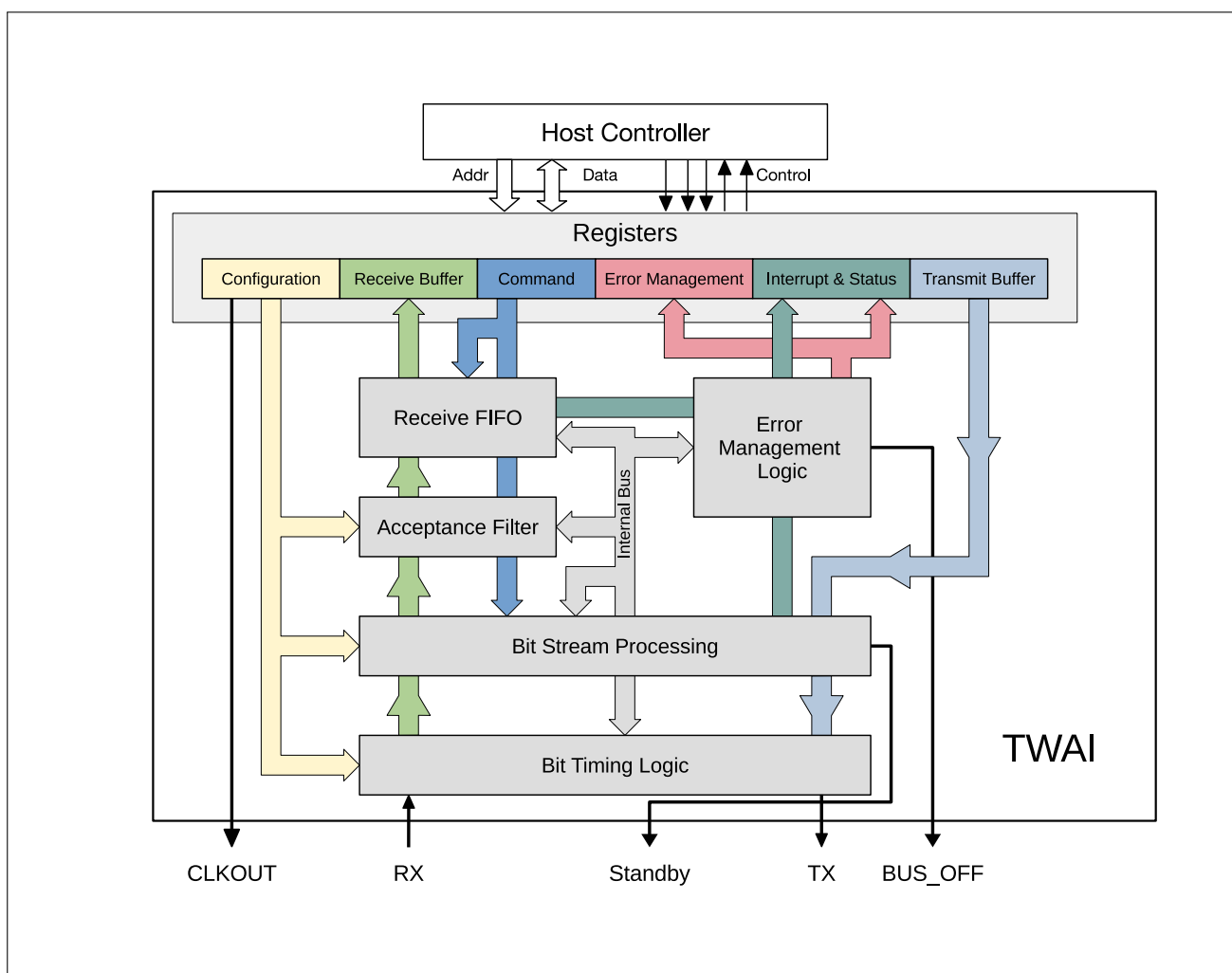


Figure 48.3-1. TWAI Overview Diagram



### 48.3.1 Bit Timing Logic

The Bit Timing Logic (BTL) module transmits and receives messages at the configured bit rate. The BTL module also handles bit timing synchronization so that communication remains stable. A single bit rate consists of multiple programmable segments that allows users to set the number of time quanta to adjust propagation delay and controller processing time, etc.

### 48.3.2 Bit Stream Processor

The Bit Stream Processing (BSP) module handles the frame processing of data from the Transmit Buffer (e.g., bit stuffing and additional CRC fields) and generates a bit stream for the Bit Timing Logic (BTL) module. At the same time, the BSP module is also responsible for processing the received bit stream (e.g., de-stuffing and verifying CRC) from the BTL module and placing the message into the Receive FIFO. The BSP will also detect errors on the TWAI bus and report them to the Error Management Logic (EML).

### 48.3.3 Acceptance Filter

The Acceptance Filter is a programmable message filtering unit that allows the TWAI controller to accept or reject a received message based on the message's ID field. Only accepted messages will be stored in the Receive FIFO. The Acceptance Filter can be configured to Single-filter mode or Dual-filter mode through registers.

### 48.3.4 Receive FIFO

The Receive FIFO is a 64-byte buffer (inside the TWAI controller) that stores received messages accepted by the Acceptance Filter. Messages in the Receive FIFO can vary in size (between 3 to 13 bytes). When the Receive FIFO is full (or does not have enough space to store the currently received message in its entirety), the Overrun Interrupt will be triggered, and any subsequently received messages will be lost until adequate space is cleared in the Receive FIFO. The first message in the Receive FIFO will be mapped to the 13-byte Receive Buffer until that message is cleared (using the Release Receive Buffer command bit). After being cleared, the Receive Buffer will map to the next message in the Receive FIFO, and the space occupied by the previous message in the Receive FIFO can be used to receive new messages.

### 48.3.5 Error Management Logic

The Error Management Logic (EML) module updates the TEC and REC, records error information like error types and positions, and updates the error state of the TWAI controller to ensure that the BSP module generates the correct Error Flags. Furthermore, this module also records the bit position when the TWAI controller loses arbitration.

### 48.3.6 Registers Block

The ESP32-P4 CPU accesses peripherals using 32-bit aligned words. However, the majority of registers in the TWAI controller only contain useful data at the least significant byte (bits [7:0]). Therefore, in these registers, bits [31:8] are ignored on writes, and return 0 on reads.

#### Configuration Registers

The configuration registers store various configuration items for the TWAI controller such as bit rates, Operation mode, Acceptance Filter, etc. Configuration registers can only be modified whilst the TWAI controller is in Reset mode (See Section [48.4.1](#)).

### Command Registers

The command register is used by the CPU to drive the TWAI controller to initiate certain actions such as transmitting a message or clearing the Receive Buffer. The command register can only be modified when the TWAI controller is in Operation mode (see Section [48.4.1](#)).

### Interrupt & Status Registers

The interrupt register indicates what events have occurred in the TWAI controller (each event is represented by a separate bit). The status register indicates the current status of the TWAI controller.

### Error Management Registers

The error management registers include error counters and capture registers. The error counter registers represent TEC and REC values. The capture registers will record information about instances where the TWAI controller detects a bus error, or when it loses arbitration.

### Transmit Buffer Registers

The transmit buffer is a 13-byte buffer used to store a TWAI message to be transmitted.

### Receive Buffer Registers

The Receive Buffer is a 13-byte buffer which stores a single message. The Receive Buffer acts as a window of Receive FIFO, whose first message will be mapped into the Receive Buffer.

Note that the Transmit Buffer registers, Receive Buffer registers, and the Acceptance Filter registers share the same address range (offset 0x0040 to 0x0070). Their access is governed by the following rules:

- When the TWAI controller is in Reset mode, all reads and writes to the address range maps to the Acceptance Filter registers.
- When the TWAI controller is in Operation mode:
  - All reads to the address range maps to the Receive Buffer registers.
  - All writes to the address range maps to the Transmit Buffer registers.

## 48.4 Functional Description

### 48.4.1 Modes

The ESP32-P4 TWAI controller has two working modes: Reset mode and Operation mode. Reset mode and Operation mode are entered by setting or clearing the [TWAI\\_RESET\\_MODE](#) bit.

#### 48.4.1.1 Reset Mode

Entering Reset mode is required in order to modify the various configuration registers of the TWAI controller. When entering Reset mode, the TWAI controller is essentially disconnected from the TWAI bus. When in Reset mode, the TWAI controller will not be able to transmit any messages (including error signals). Any transmission in progress is immediately terminated. Likewise, the TWAI controller will not be able to receive any messages either.

### 48.4.1.2 Operation Mode

In Operation mode, the TWAI controller connects to the bus and write-protects all configuration registers to ensure consistency during operation. When in Operation mode, the TWAI controller can transmit and receive messages (including error signaling) depending on which operation sub-mode the TWAI controller was configured with. The TWAI controller supports the following operation sub-modes:

- **Normal mode:** The TWAI controller can transmit and receive messages including error signals (such as Error and Overload Frames).
- **Self-test mode:** Self-test mode is similar to Normal mode, but the TWAI controller will consider the transmission of a data or remote frame successful and do not generate an ACK error even if it was not acknowledged. This mode is commonly used during the self-test of a TWAI controller.
- **Listen-only mode:** The TWAI controller will be able to receive messages, but will remain completely passive on the TWAI bus. Thus, the TWAI controller will not be able to transmit any messages, acknowledgments, or error signals. The error counters will remain frozen. This mode is useful for TWAI bus monitoring.

Note that when exiting Reset mode (i.e., entering Operation mode), the TWAI controller must wait for 11 consecutive recessive bits to occur before fully connecting to the TWAI bus (i.e., being able to transmit or receive).

### 48.4.2 Bit Timing

The operating bit rate of the TWAI controller must be configured whilst the TWAI controller is in Reset mode. The bit rate is configured using [TWAI\\_BUS\\_TIMING\\_0\\_REG](#) and [TWAI\\_BUS\\_TIMING\\_1\\_REG](#).

The following Table 48.4-1 illustrates the bit fields of [TWAI\\_BUS\\_TIMING\\_0\\_REG](#). The frequency of the TWAI core clock has multiple clock sources that can be configured by the user as needed. See Chapter 9 [Reset and Clock](#) for detailed configuration instructions.

Table 48.4-1. Bit Information of [TWAI\\_BUS\\_TIMING\\_0\\_REG](#) (0x18)

| Bit 31-16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | ..... | Bit 1 | Bit 0 |
|-----------|--------|--------|--------|--------|-------|-------|-------|
| Reserved  | SJW.1  | SJW.0  | BRP.13 | BRP.12 | ..... | BRP.1 | BRP.0 |

#### Notes:

- BRP: The TWAI Time Quanta clock is derived from the XTAL clock (the default is 40 MHz and is configured). The Baud Rate Prescaler (BRP) field is used to define the prescaler according to the equation below, where  $t_{Tq}$  is the Time Quanta clock cycle and  $t_{CLK}$  is TWAI core clock cycle:  

$$t_{Tq} = 2 \times t_{CLK} \times (BRP + 1)$$
- SJW ( $t_{SJW}$ ): Synchronization Jump Width (SJW)  $t_{SJW}$  is configured in SJW[1:0] where  $t_{SJW} = (SJW[1:0] + 1)$ .

The following Table 48.4-2 illustrates the bit fields of [TWAI\\_BUS\\_TIMING\\_1\\_REG](#).

Table 48.4-2. Bit Information of `TWAI_BUS_TIMING_1_REG` (0x1c)

| Bit 31-8 | Bit 7 | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|----------|-------|--------|--------|--------|--------|--------|--------|--------|
| Reserved | SAM   | PBS2.2 | PBS2.1 | PBS2.0 | PBS1.3 | PBS1.2 | PBS1.1 | PBS1.0 |

**Notes:**

- PBS1: The number of Time Quanta in Phase Buffer Segment 1 is defined based on PBS1 + 1.
- PBS2: The number of Time Quanta in Phase Buffer Segment 2 is defined based on PBS2 + 1.
- SAM: Enables triple sampling if set to 1. This is useful for low/medium speed buses to filter spikes on the bus line.

## 48.4.3 Transmit and Receive Buffers

### 48.4.3.1 Overview of Buffers

Table 48.4-3. Buffer Layout for Standard Frame Format and Extended Frame Format

| Standard Frame Format (SFF) |                         | Extended Frame Format (EFF) |                         |
|-----------------------------|-------------------------|-----------------------------|-------------------------|
| Offset Address              | Content                 | Offset Address              | Content                 |
| 0x40                        | TX/RX frame information | 0x40                        | TX/RX frame information |
| 0x44                        | TX/RX identifier 1      | 0x44                        | TX/RX identifier 1      |
| 0x48                        | TX/RX identifier 2      | 0x48                        | TX/RX identifier 2      |
| 0x4c                        | TX/RX data byte 1       | 0x4c                        | TX/RX identifier 3      |
| 0x50                        | TX/RX data byte 2       | 0x50                        | TX/RX identifier 4      |
| 0x54                        | TX/RX data byte 3       | 0x54                        | TX/RX data byte 1       |
| 0x58                        | TX/RX data byte 4       | 0x58                        | TX/RX data byte 2       |
| 0x5c                        | TX/RX data byte 5       | 0x5c                        | TX/RX data byte 3       |
| 0x60                        | TX/RX data byte 6       | 0x60                        | TX/RX data byte 4       |
| 0x64                        | TX/RX data byte 7       | 0x64                        | TX/RX data byte 5       |
| 0x68                        | TX/RX data byte 8       | 0x68                        | TX/RX data byte 6       |
| 0x6c                        | reserved                | 0x6c                        | TX/RX data byte 7       |
| 0x70                        | reserved                | 0x70                        | TX/RX data byte 8       |

Table 48.4-3 illustrates the layout of the Transmit Buffer and Receive Buffer registers. Both the Transmit and Receive Buffer registers share the same address space and are only accessible when the TWAI controller is in Operation mode. The CPU accesses Transmit Buffer registers for write operations, and Receive Buffer registers for read operations. Both buffers share the exact same register layout and fields to store a message (received or to be transmitted). The Transmit Buffer registers are used to configure a TWAI message to be transmitted. The CPU would write to the Transmit Buffer registers specifying the message's frame type, frame format, frame ID, and frame data (payload). Once the Transmit Buffer is configured, the CPU would then initiate the transmission by setting the `TWAI_TX_REQUEST` bit in `TWAI_CMD_REG`.

- For a self-reception request, set the `TWAI_SELF_RX_REQUEST` bit instead.
- For a single-shot transmission, set both the `TWAI_TX_REQUEST` and the `TWAI_ABORT_TX` simultaneously.

The Receive Buffer registers map the first message in the Receive FIFO. The CPU would read the Receive Buffer registers to obtain the first message's frame type, frame format, frame ID, and frame data (payload). Once the message has been read from the Receive Buffer registers, the CPU can set the [TWAI\\_RELEASE\\_BUFFER](#) bit in [TWAI\\_CMD\\_REG](#) to clear the Receive Buffer registers. If there are still messages in the Receive FIFO, the Receive Buffer registers will map the first of the remaining messages again.

#### 48.4.3.2 Frame Information

The frame information is one byte long and specifies a message's frame type, frame format, and length of data. The frame information fields are shown in Table 48.4-4.

**Table 48.4-4. TX/RX Frame Information (SFF/EFF); TWAI Address 0x40**

| Bit 31-8 | Bit 7           | Bit 6            | Bit 5          | Bit 4          | Bit 3              | Bit 2              | Bit 1              | Bit 0              |
|----------|-----------------|------------------|----------------|----------------|--------------------|--------------------|--------------------|--------------------|
| Reserved | FF <sup>1</sup> | RTR <sup>2</sup> | X <sup>3</sup> | X <sup>3</sup> | DLC.3 <sup>4</sup> | DLC.2 <sup>4</sup> | DLC.1 <sup>4</sup> | DLC.0 <sup>4</sup> |

**Notes:**

1. FF: The Frame Format (FF) bit specifies whether the message is Extended Frame Format (EFF) or Standard Frame Format (SFF). The message is EFF when the FF bit is 1, and SFF when the FF bit is 0.
2. RTR: The Remote Transmission Request (RTR) bit specifies whether the message is a data frame or a remote frame. The message is a remote frame when the RTR bit is 1, and a data frame when the RTR bit is 0.
3. X: Don't care, can be any value.
4. DLC: The Data Length Code (DLC) field specifies the number of data bytes for a data frame, or the number of data bytes to request in a remote frame. TWAI data frames are limited to a maximum payload of 8 data bytes, and thus the DLC should range from 0 to 8.

#### 48.4.3.3 Frame Identifier

The Frame Identifier fields occupy two-byte (11-bit) long if the message is SFF, and four-byte (29-bit) long if the message is EFF.

The Frame Identifier fields for an SFF (11-bit) message are shown in Table 48.4-5 ~ 48.4-6.

**Table 48.4-5. TX/RX Identifier 1 (SFF); TWAI Address 0x44**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | ID.10 | ID.9  | ID.8  | ID.7  | ID.6  | ID.5  | ID.4  | ID.3  |

**Table 48.4-6. TX/RX Identifier 2 (SFF); TWAI Address 0x48**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4          | Bit 3          | Bit 2          | Bit 1          | Bit 0          |
|----------|-------|-------|-------|----------------|----------------|----------------|----------------|----------------|
| Reserved | ID.2  | ID.1  | ID.0  | X <sup>1</sup> | X <sup>2</sup> | X <sup>2</sup> | X <sup>2</sup> | X <sup>2</sup> |

**Notes:**

1. Don't care. Recommended to be compatible with receive buffer (i.e., set to RTR) in case of using the self-reception functionality (or together with self-test functionality).

2. Don't care. Recommended to be compatible with receive buffer (i.e., set to 0) in case of using the self-reception functionality (or together with self-test functionality).

The Frame Identifier fields for an EFF (29-bits) message is shown in Table 48.4-7 ~ 48.4-10.

**Table 48.4-7. TX/RX Identifier 1 (EFF); TWAI Address 0x44**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | ID.28 | ID.27 | ID.26 | ID.25 | ID.24 | ID.23 | ID.22 | ID.21 |

**Table 48.4-8. TX/RX Identifier 2 (EFF); TWAI Address 0x48**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | ID.20 | ID.19 | ID.18 | ID.17 | ID.16 | ID.15 | ID.14 | ID.13 |

**Table 48.4-9. TX/RX Identifier 3 (EFF); TWAI Address 0x4c**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | ID.12 | ID.11 | ID.10 | ID.9  | ID.8  | ID.7  | ID.6  | ID.5  |

**Table 48.4-10. TX/RX Identifier 4 (EFF); TWAI Address 0x50**

| Bit 31-8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2          | Bit 1          | Bit 0          |
|----------|-------|-------|-------|-------|-------|----------------|----------------|----------------|
| Reserved | ID.4  | ID.3  | ID.2  | ID.1  | ID.0  | X <sup>1</sup> | X <sup>2</sup> | X <sup>2</sup> |

**Notes:**

1. Don't care. Recommended to be compatible with receive buffer (i.e., set to RTR ) in case of using the self-reception functionality (or together with self-test functionality).
2. Don't care. Recommended to be compatible with receive buffer (i.e., set to 0 ) in case of using the self-reception functionality (or together with self-test functionality).

#### 48.4.3.4 Frame Data

The Frame Data field contains the payloads of transmitted or received data frame, and can range from 0 to 8 bytes. The number of valid bytes should be equal to the DLC. However, if the DLC is larger than eight bytes, the number of valid bytes would still be limited to eight. Remote frames do not have data payloads, so their Frame Data fields will be unused.

For example, when transmitting a data frame with five bytes, the CPU should write five to the DLC field, and then write data to the corresponding register of the first to the fifth data field. Likewise, when the CPU receives a data frame with a DLC of five data bytes, only the first to the fifth data byte will contain valid payload data for the CPU to read.

### 48.4.4 Receive FIFO and Data Overruns

The Receive FIFO is a 64-byte internal buffer used to store received messages in First In First Out order. A single received message can occupy between 3 to 13 bytes of space in the Receive FIFO, and their

endianness is identical to the register layout of the Receive Buffer registers. The Receive Buffer registers are mapped to the bytes of the first message in the Receive FIFO.

When the TWAI controller receives the first message, the value of [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) increases to 1, and the RXI interrupt is activated, automatically updating the first message into the buffer. Subsequently, with each new message received by the TWAI controller, the value of [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) increments by 1, reaching a maximum of 64. When this limit is reached and there is sufficient space remaining in the Receive FIFO, the message will be written into the FIFO.

Once the software reads a message from the Receive Buffer, it can free up the space occupied by the message in the Receive FIFO by setting [TWAI\\_RELEASE\\_BUFFER](#) to 1. This will also decrement [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) by 1. The Receive Buffer will then map to the next message in the Receive FIFO. The software should repeat the above operations until [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) reaches 0. At this point, the RXI interrupt stops being triggered, the data in the receive buffer becomes invalid, and [TWAI\\_STATUS\\_RECEIVE\\_BUFFER](#) is set to 0.

A data overrun occurs when the TWAI controller receives a message, but the Receive FIFO lacks adequate free space to store the received message in its entirety (either due to the message contents being larger than the free space in the Receive FIFO, or the Receive FIFO being completely full).

When a data overrun occurs:

- The free space left in the Receive FIFO is filled with the partial contents of the overrun message. If the Receive FIFO is already full, then none of the overrun message's contents will be stored.
- When data in the Receive FIFO overruns for the first time, a Data Overrun Interrupt will be triggered.
- Each overrun message will still increment the [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) up to a maximum of 64.
- The Receive FIFO will internally mark overrun messages as invalid. The [TWAI\\_STATUS\\_MISS](#) bit can be used to determine whether the message currently mapped to by the Receive Buffer is valid or overrun.

To clear an overrun Receive FIFO, the [TWAI\\_RELEASE\\_BUFFER](#) must be called repeatedly until [TWAI\\_RX\\_MESSAGE\\_COUNTER](#) is 0. This requires users to read all valid messages in the Receive FIFO and clear all overrun messages.

### 48.4.5 Acceptance Filter

The Acceptance Filter allows the TWAI controller to filter out received messages based on their ID (and optionally their first data byte and frame type). Only accepted messages are passed on to the Receive FIFO. The use of Acceptance Filters allows a more lightweight operation of the TWAI controller (e.g., less use of Receive FIFO, fewer Receive Interrupts) since the TWAI Controller only needs to handle a subset of messages.

The Acceptance Filter configuration registers can only be accessed whilst the TWAI controller is in Reset mode, since they share the same address spaces with the Transmit Buffer and Receive Buffer registers.

The configuration registers consist of a 32-bit Acceptance Code Value and a 32-bit Acceptance Mask Value. The Acceptance Code value specifies a bit pattern which each filtered bit of the message must match in order for the message to be accepted. The Acceptance Mask Value is able to mask out certain bits of the Code value (i.e., set as "Don't Care" bits). Each filtered bit of the message must either match the acceptance code or be masked in order for the message to be accepted, as demonstrated in Figure 48.4-1.

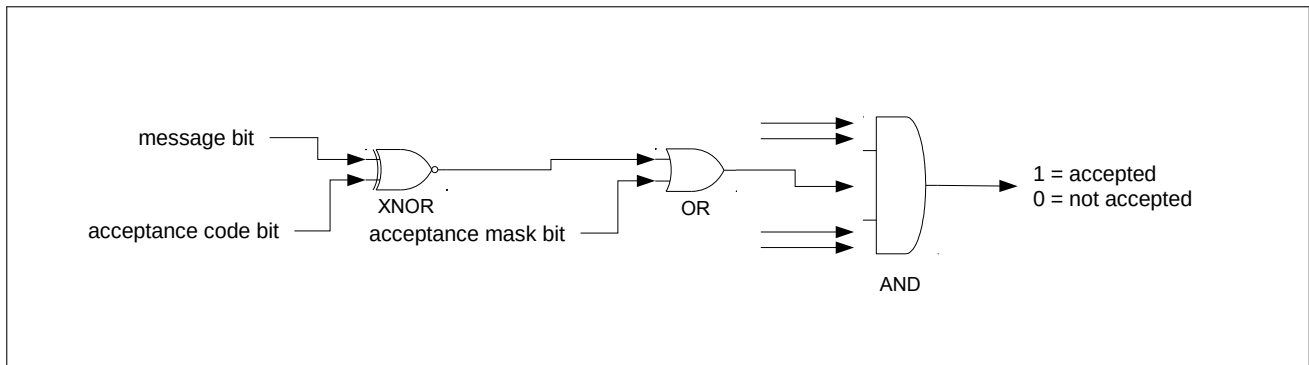


Figure 48.4-1. Acceptance Filter

The TWAI controller Acceptance Filter allows the 32-bit Acceptance Code and Mask Values to either define a single filter (i.e., Single-filter mode), or two filters (i.e., Dual-filter mode). How the Acceptance Filter interprets the 32-bit code and mask values is dependent on the filter mode and the format of received messages (i.e., SFF or EFF).

#### 48.4.5.1 Single-Filter Mode

Single Filter mode is enabled by setting the `TWAI_ACCEPTANCE_FILTER_MODE` bit to 1. This will cause the 32-bit code and mask values to define a single filter. The single filter can filter the following bits of data or remote frames:

- SFF
  - The entire 11-bit ID
  - RTR bit
  - Data byte 1 and Data byte 2
- EFF
  - The entire 29-bit ID
  - RTR bit

The following Figure 48.4-2 illustrates how the 32-bit code and mask values will be interpreted under Single-filter mode.

#### 48.4.5.2 Dual-Filter Mode

Dual-filter mode is enabled by clearing the `TWAI_ACCEPTANCE_FILTER_MODE` bit to 0. This will cause the 32-bit code and mask values to define a two separate filters referred to as filter 1 or filter 2. Under Dual-filter mode, a message will be accepted if it is accepted by one of the two filters.

The two filters can filter the following bits of data or remote frames:

- SFF
  - The entire 11-bit ID
  - RTR bit
  - Data byte 1 (for filter 1 only)



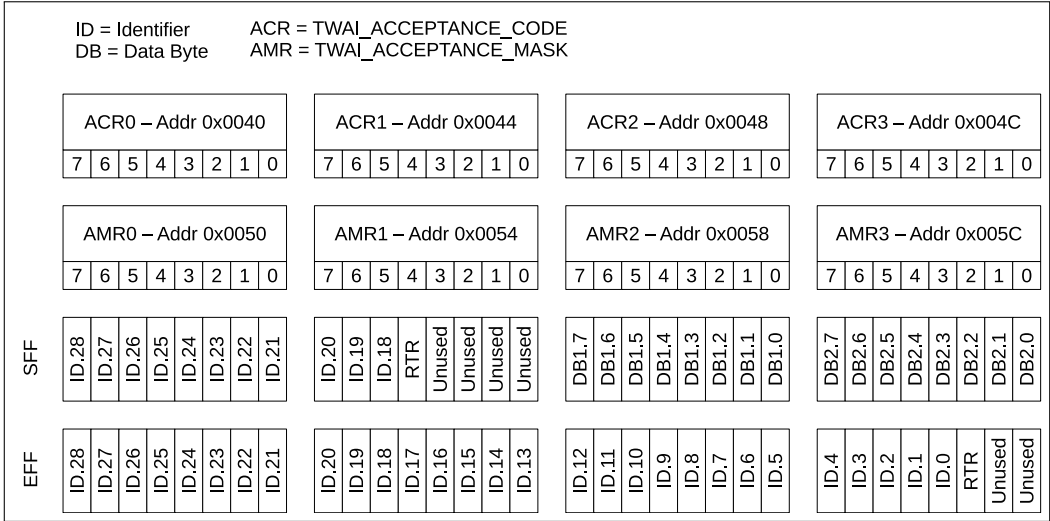


Figure 48.4-2. Single-Filter Mode

- EFF
  - The first 16 bits of the 29-bit ID

The following Figure 48.4-3 illustrates how the 32-bit code and mask values will be interpreted in Dual-filter mode.

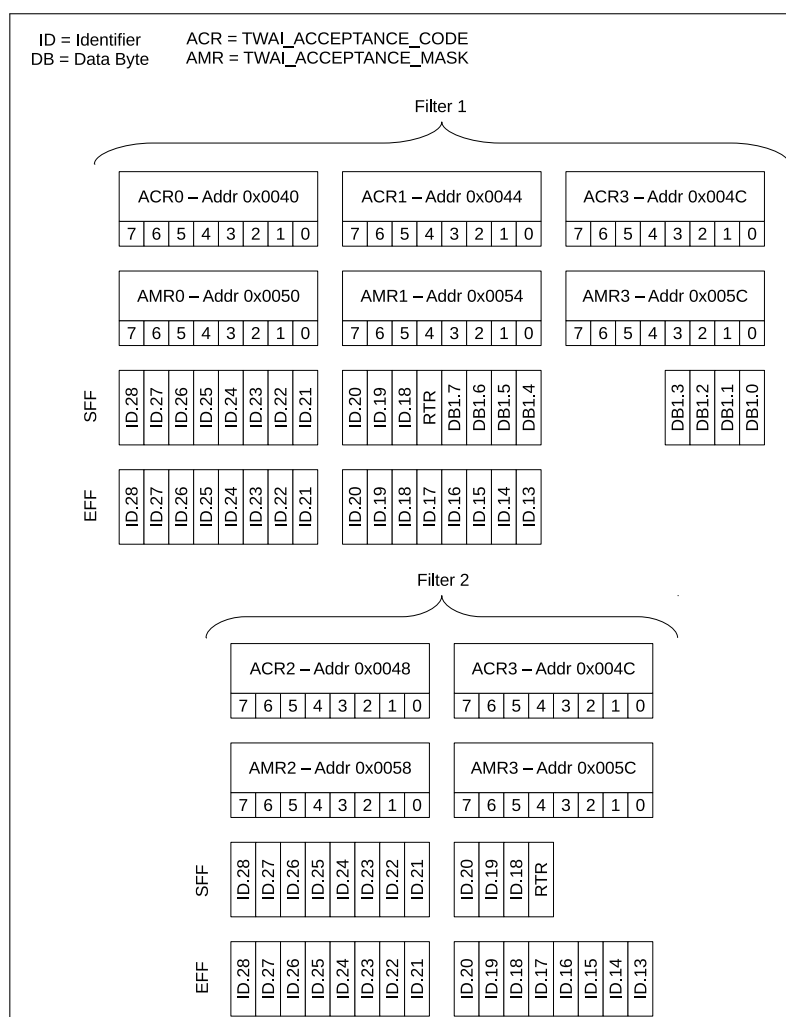


Figure 48.4-3. Dual-Filter Mode

## 48.4.6 Error Management

The TWAI protocol requires that each TWAI node maintains the Transmit Error Counter (TEC) and Receive Error Counter (REC). The value of both error counters determines the current error state of the TWAI controller (i.e., Error Active, Error Passive, Bus-Off). The TWAI controller stores the TEC and REC values in [TWAI\\_TX\\_ERR\\_CNT\\_REG](#) and [TWAI\\_RX\\_ERR\\_CNT\\_REG](#) respectively, and they can be read by the CPU anytime. In addition to the error states, the TWAI controller also offers an Error Warning Limit (EWL) feature that can warn users of the occurrence of severe bus errors before the TWAI controller enters the Error Passive state.

The current error state of the TWAI controller is indicated via a combination of the following values and status bits: TEC, REC, [TWAI\\_STATUS\\_ERR](#), and [TWAI\\_STATUS\\_NODE\\_BUS\\_OFF](#). Certain changes to these values and bits will also trigger interrupts, so that users are notified of error state transitions (see section 48.5). The following figure 48.4-4 shows the relation between the error states, values and bits, and error state related interrupts.

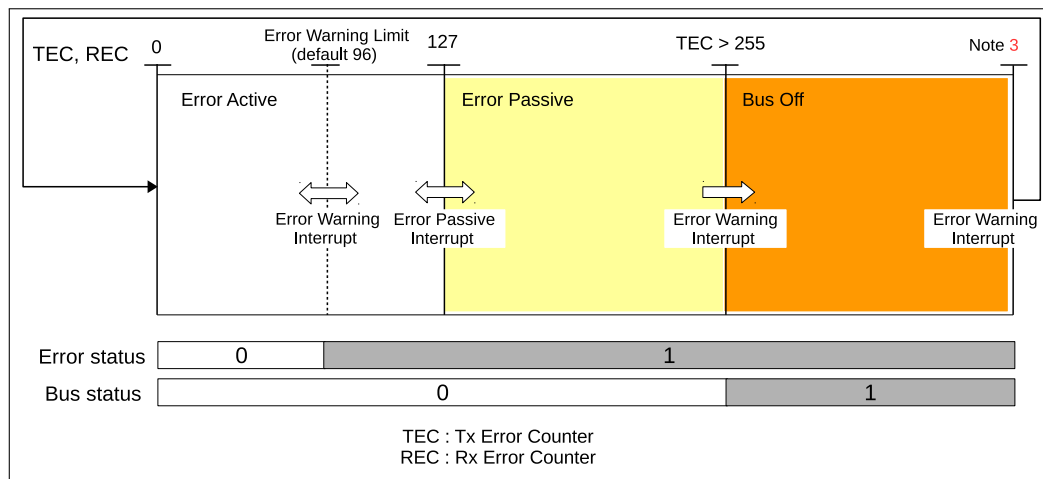


Figure 48.4-4. Error State Transition

#### 48.4.6.1 Error Warning Limit

The Error Warning Limit (EWL) is a configurable threshold value for the TEC and REC, which will trigger an interrupt when exceeded. The EWL is intended to serve as a warning about severe TWAI bus errors, and is triggered before the TWAI controller enters the Error Passive state. The EWL is configured in [TWAI\\_ERR\\_WARNING\\_LIMIT\\_REG](#) and can only be configured whilst the TWAI controller is in Reset mode. The [TWAI\\_ERR\\_WARNING\\_LIMIT\\_REG](#) has a default value of 96.

When the values of TEC and/or REC are larger than or equal to the EWL value, the [TWAI\\_STATUS\\_ERR](#) bit is immediately set to 1. Likewise, when the values of both the TEC and REC are smaller than the EWL value, the [TWAI\\_STATUS\\_ERR](#) bit is immediately reset to 0. The Error Warning Interrupt is triggered whenever the value of the [TWAI\\_STATUS\\_ERR](#) bit (or the [TWAI\\_STATUS\\_NODE\\_BUS\\_OFF](#)) changes.

#### 48.4.6.2 Error Passive

The TWAI controller is in the Error Passive state when the TEC or REC value exceeds 127. Likewise, when both the TEC and REC are less than or equal to 127, the TWAI controller enters the Error Active state. The Error Passive Interrupt is triggered whenever the TWAI controller transitions from the Error Active state to the Error Passive state or vice versa.

#### 48.4.6.3 Bus-Off and Bus-Off Recovery

The TWAI controller enters the Bus-Off state when the TEC value exceeds 255. On entering the Bus-Off state, the TWAI controller will automatically do the following:

- Set REC to 0
- Set TEC to 127
- Set the [TWAI\\_STATUS\\_NODE\\_BUS\\_OFF](#) bit to 1
- Enter Reset mode

The Error Warning Interrupt is triggered whenever the value of the [TWAI\\_STATUS\\_NODE\\_BUS\\_OFF](#) bit (or the [TWAI\\_STATUS\\_ERR](#) bit) changes.

To return to the Error Active state, the TWAI controller must undergo Bus-Off Recovery. Bus-Off Recovery requires the TWAI controller to observe 128 occurrences of 11 consecutive recessive bits on the bus. To initiate Bus-Off Recovery (after entering the Bus-Off state), the TWAI controller should enter Operation mode by setting the [TWAI\\_RESET\\_MODE](#) bit to 0. The TEC tracks the progress of Bus-Off Recovery by decrementing the TEC each time when the TWAI controller observes 11 consecutive recessive bits. When Bus-Off Recovery has completed (i.e., TEC has decremented from 127 to 0), the [TWAI\\_STATUS\\_NODE\\_BUS\\_OFF](#) bit will automatically be reset to 0, thus triggering the Error Warning Interrupt.

### 48.4.7 Error Code Capture

The Error Code Capture (ECC) feature allows the TWAI controller to record the error type and bit position of a TWAI bus error in the form of an error code. Upon detecting a TWAI bus error, the Bus Error Interrupt is triggered and the error code is recorded in [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#). Subsequent bus errors will trigger the Bus Error Interrupt, but their error codes will not be recorded until the current error code is read from [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#).

The following Table 48.4-11 shows the fields of the [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#):

**Table 48.4-11. Bit Information of [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#) (0x30)**

| Bit 31-8 | Bit 7               | Bit 6               | Bit 5            | Bit 4              | Bit 3              | Bit 2              | Bit 1              | Bit 0              |
|----------|---------------------|---------------------|------------------|--------------------|--------------------|--------------------|--------------------|--------------------|
| Reserved | ERRC.1 <sup>1</sup> | ERRC.0 <sup>1</sup> | DIR <sup>2</sup> | SEG.4 <sup>3</sup> | SEG.3 <sup>3</sup> | SEG.2 <sup>3</sup> | SEG.1 <sup>3</sup> | SEG.0 <sup>3</sup> |

**Notes:**

- **ERRC:** The Error Code (ERRC) indicates the type of bus error; 00 for bit error, 01 for format error, 10 for stuff error, and 11 for other types of error.
- **DIR:** The Direction (DIR) indicates whether the TWAI controller was transmitting or receiving when the bus error occurred; 0 for the transmitter, 1 for the receiver.
- **SEG:** The Error Segment (SEG) indicates the segment of the TWAI message at which the bus error occurred.

The following Table 48.4-12 shows how to interpret the SEG.0 to SEG.4 bits.

**Table 48.4-12. Bit Information of Bits SEG.4 - SEG.0**

| Bit SEG.4 | Bit SEG.3 | Bit SEG.2 | Bit SEG.1 | Bit SEG.0 | Description    |
|-----------|-----------|-----------|-----------|-----------|----------------|
| 0         | 0         | 0         | 1         | 1         | start of frame |
| 0         | 0         | 0         | 1         | 0         | ID.28 ~ ID.21  |
| 0         | 0         | 1         | 1         | 0         | ID.20 ~ ID.18  |
| 0         | 0         | 1         | 0         | 0         | bit SRTR       |
| 0         | 0         | 1         | 0         | 1         | bit IDE        |
| 0         | 0         | 1         | 1         | 1         | ID.17 ~ ID.13  |
| 0         | 1         | 1         | 1         | 1         | ID.12 ~ ID.5   |
| 0         | 1         | 1         | 1         | 0         | ID.4 ~ ID.0    |
| 0         | 1         | 1         | 0         | 0         | bit RTR        |
| 0         | 1         | 1         | 0         | 1         | reserved bit 1 |
| 0         | 1         | 0         | 0         | 1         | reserved bit 0 |

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Table 48.4-12 – cont'd from previous page

| Bit SEG.4 | Bit SEG.3 | Bit SEG.2 | Bit SEG.1 | Bit SEG.0 | Description            |
|-----------|-----------|-----------|-----------|-----------|------------------------|
| 0         | 1         | 0         | 1         | 1         | data length code       |
| 0         | 1         | 0         | 1         | 0         | data field             |
| 0         | 1         | 0         | 0         | 0         | CRC sequence           |
| 1         | 1         | 0         | 0         | 0         | CRC delimiter          |
| 1         | 1         | 0         | 0         | 1         | ACK slot               |
| 1         | 1         | 0         | 1         | 1         | ACK delimiter          |
| 1         | 1         | 0         | 1         | 0         | end of frame           |
| 1         | 0         | 0         | 1         | 0         | intermission           |
| 1         | 0         | 0         | 0         | 1         | active error flag      |
| 1         | 0         | 1         | 1         | 0         | passive error flag     |
| 1         | 0         | 0         | 1         | 1         | tolerate dominant bits |
| 1         | 0         | 1         | 1         | 1         | error delimiter        |
| 1         | 1         | 1         | 0         | 0         | overload flag          |

**Notes:**

- Bit SRTR: under Standard Frame Format.
- Bit IDE: Identifier Extension Bit, 0 for Standard Frame Format.

## 48.4.8 Arbitration Lost Capture

The Arbitration Lost Capture (ALC) feature allows the TWAI controller to record the bit position where it loses arbitration. When the TWAI controller loses arbitration, the bit position is recorded in [TWAI\\_ARB\\_LOST\\_CAP\\_REG](#) and the Arbitration Lost Interrupt is triggered.

Subsequent losses in arbitration will trigger the Arbitration Lost Interrupt, but will not be recorded in [TWAI\\_ARB\\_LOST\\_CAP\\_REG](#) until the current Arbitration Lost Capture is read from the [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#).

Table 48.4-13 illustrates bits and fields of [TWAI\\_ERR\\_CODE\\_CAP\\_REG](#) whilst Figure 48.4-5 illustrates the bit positions of a TWAI message.

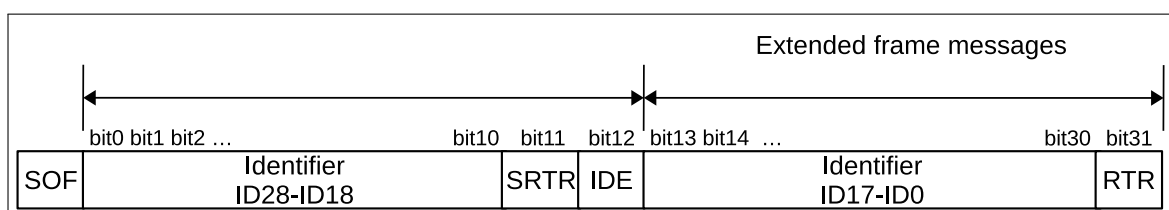


Figure 48.4-5. Positions of Arbitration Lost Bits

Table 48.4-13. Bit Information of [TWAI\\_ARB\\_LOST\\_CAP\\_REG](#) (0x2c)

| Bit 31-5 | Bit 4                | Bit 3                | Bit 2                | Bit 1                | Bit 0                |
|----------|----------------------|----------------------|----------------------|----------------------|----------------------|
| Reserved | BITNO.4 <sup>1</sup> | BITNO.3 <sup>1</sup> | BITNO.2 <sup>1</sup> | BITNO.1 <sup>1</sup> | BITNO.0 <sup>1</sup> |

**Notes:**

- BITNO: Bit Number (BITNO) indicates the nth bit of a TWAI message where arbitration was lost.

### 48.4.9 Transceiver Auto-Standby

It is common for TWAI transceivers to support a Standby mode to lower power consumption. TWAI transceivers will usually generate a standby signal that is asserted by the connected TWAI controller, thus allowing the controller to place the transceiver into standby when appropriate (e.g., when the bus will be idle for an extended period of time). Transceivers will exit Standby mode if the controller de-asserts the standby signal, or if the transceiver detects bus activity (also known as a wake-up feature).

ESP32-P4's TWAI controller supports both hardware control (i.e., automatic) and software control (i.e., manual) of the standby signal to control the switching of TWAI transceivers connected to the chip. When hardware controlled, the TWAI controller will automatically assert the standby signal when the bus remains idle for longer than a configurable amount of time. When software controlled, the standby signal can be manually asserted/de-asserted directly by the software.

- Hardware output:
  1. Set the [TWAI\\_HW\\_STANDBY\\_EN](#) field in the [TWAI\\_HW\\_CFG\\_REG](#) register to enable standby function for hardware.
  2. Configure the [TWAI\\_HW\\_STANDB\\_CNT\\_REG](#) register. This register indicates the time required before hardware triggers the standby signal after entering idle status, in which the value indicates the number of cycles of the TWAI controller operating clock (40 MHz by default).
- Software output:
  1. Set the [TWAI\\_SW\\_STANDBY\\_EN](#) field in the [TWAI\\_SW\\_STANDBY\\_CFG\\_REG](#) register to generate standby signals in the TWAI controller.

The standby signal generated using either of the above methods will be pulled down (cleared) when either of the following conditions is met:

1. The standby signal will be automatically cleared when the TWAI controller's receiver exits the idle status (such as when receiving a new message).
2. Users can also pull down the standby signal by setting the [TWAI\\_SW\\_STANDBY\\_CLR](#) field in the [TWAI\\_SW\\_STANDBY\\_CFG\\_REG](#) register.

## 48.5 Interrupts

ESP32-P4's TWAI can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- TWAI\_INT

There are several internal interrupt sources from the TWAI that can generate the above interrupt signal. The interrupt sources from the TWAI are listed with their trigger conditions and the resulted interrupt signal in Table 48.5-1.

**Table 48.5-1. TWAI's Internal Interrupt Sources**

| Internal Interrupt Source | Trigger Condition   | Interrupt Signal |
|---------------------------|---|------------------|
| TWAI_RECEIVE_INT (RXI)    | The Receive Interrupt (RXI) is asserted whenever the TWAI controller has received messages that are pending to be read from the Receive Buffer (i.e., when <a href="#">TWAI_RX_MESSAGE_COUNTER_REG</a> > 0). Pending received messages includes valid messages in the Receive FIFO and also overrun messages. The RXI will not be deasserted until all pending received messages are cleared using the <a href="#">TWAI_RELEASE_BUFFER</a> command bit.   | TWAI_INT         |
| TWAI_TRANSMIT_INT (TXI)   | The Transmit Interrupt (TXI) is triggered whenever Transmit Buffer becomes free, indicating another message can be loaded into the Transmit Buffer for transmission. The Transmit Buffer becomes free under the following scenarios: <ul style="list-style-type: none"> <li>• A message transmission has completed successfully, i.e., acknowledged without any errors. Any failed messages will automatically be resent.</li> <li>• A single shot transmission has completed (successfully or unsuccessfully, indicated by the <a href="#">TWAI_STATUS_TRANSMISSION_COMPLETE</a> bit).</li> <li>• A message transmission was aborted using the <a href="#">TWAI_ABORT_TX</a> command bit.</li> </ul> | TWAI_INT         |

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Table 48.5-1 – cont'd from previous page

| Internal Interrupt Source  | Trigger Condition   | Interrupt Signal |
|----------------------------|---|------------------|
| TWAI_ERR_WARNING_INT (EWI) | <p>The Error Warning Interrupt (EWI) is triggered whenever there is a change to the <a href="#">TWAI_STATUS_ERR</a> and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> bits of the <a href="#">TWAI_STATUS_REG</a> (i.e., transition from 0 to 1 or vice versa). Thus, an EWI could indicate one of the following events, depending on the values <a href="#">TWAI_STATUS_ERR</a> and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> at the moment when the EWI is triggered.</p> <ul style="list-style-type: none"> <li>• If <a href="#">TWAI_STATUS_ERR</a> = 0 and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> = 0: <ul style="list-style-type: none"> <li>– If the TWAI controller was in the Error Active state, it indicates both the TEC and REC have returned below the threshold value set by <a href="#">TWAI_ERR_WARNING_LIMIT_REG</a>.</li> <li>– If the TWAI controller was previously in the Bus Off Recovery state, it indicates that Bus Recovery has completed successfully.</li> </ul> </li> <li>• If <a href="#">TWAI_STATUS_ERR</a> = 1 and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> = 0: The TEC or REC error counters have exceeded the threshold value set by <a href="#">TWAI_ERR_WARNING_LIMIT_REG</a>.</li> <li>• If <a href="#">TWAI_STATUS_ERR</a> = 1 and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> = 1: The TWAI controller has entered the BUS_OFF state (due to the TEC &gt;= 256).</li> <li>• If <a href="#">TWAI_STATUS_ERR</a> = 0 and <a href="#">TWAI_STATUS_NODE_BUS_OFF</a> = 1: The TWAI controller's TEC has dropped below the threshold value set by <a href="#">TWAI_ERR_WARNING_LIMIT_REG</a> during BUS_OFF recovery.</li> </ul> | TWAI_INT         |

Cont'd on next page



Table 48.5-1 – cont'd from previous page

| Internal Interrupt Source       | Trigger Condition   | Interrupt Signal |
|---------------------------------|---|------------------|
| TWAI_DATA_OVERRUN_INT (DOI)     | The Data Overrun Interrupt (DOI) is triggered whenever the Receive FIFO has overrun. The DOI indicates that the Receive FIFO is full and should be cleared immediately to prevent any further overrun messages. The DOI is only triggered by the first message that causes the Receive FIFO to overrun (i.e., the transition from the Receive FIFO not being full to the Receive FIFO overflowing). Any subsequent overrun messages will not trigger the DOI again. The DOI could be triggered again when all received messages (valid or overrun) have been cleared. | TWAI_INT         |
| TWAI_TS_COUNTER_OVFL_INT        | The Timestamp Overflow Interrupt is triggered whenever the 32-bit counter of the TWAI controller timestamp has overflowed.  | TWAI_INT         |
| TWAI_ERR_PASSIVE_INT (EPI)      | The Error Passive Interrupt (EPI) is triggered whenever the TWAI controller switches from Error Active to Error Passive, or vice versa.   | TWAI_INT         |
| TWAI_ARBITRATION_LOST_INT (ALI) | The Arbitration Lost Interrupt (ALI) is triggered whenever the TWAI controller is attempting to transmit a message and loses arbitration. The bit position where the TWAI controller lost arbitration is automatically recorded in Arbitration Lost Capture register ( <a href="#">TWAI_ARB_LOST_CAP_REG</a> ). When the ALI occurs again, the Arbitration Lost Capture register will no longer record the new bit location until it is cleared (via CPU reading this register).  | TWAI_INT         |
| TWAI_BUS_ERR_INT (BEI)          | The Bus Error Interrupt (BEI) is triggered whenever the TWAI controller detects an error on the TWAI bus. When a bus error occurs, the Bus Error type and its bit position are automatically recorded in the Error Code Capture register ( <a href="#">TWAI_ERR_CODE_CAP_REG</a> ). When the BEI occurs again, the Error Code Capture register will no longer record new error information until it is cleared (via a read from the CPU).   | TWAI_INT         |
| TWAI_IDLE_INT (BISI)            | The Bus Idle Status Interrupt (BISI) is triggered when the number of clock cycles of the TWAI controller in the idle status exceeds the pre-configured value in the <a href="#">TWAI_IDLE_INTR_CNT_REG</a> register. Users can configure this interrupt to get the TWAI controller idle status and further decide whether to turn off the external TWAI receiver to reduce the overall power consumption (see Section <a href="#">48.4.9</a> ).   | TWAI_INT         |

The TWAI controller's interrupt signal to the interrupt matrix will be asserted whenever one or more interrupt bits are set in the [TWAI\\_INTERRUPT\\_REG](#), and de-asserted when all bits in [TWAI\\_INTERRUPT\\_REG](#) are cleared. The majority of interrupt bits in [TWAI\\_INTERRUPT\\_REG](#) are automatically cleared when the register is read, except for the Receive Interrupt which can only be cleared when all the messages are released by setting the [TWAI\\_RELEASE\\_BUFFER](#) bit.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [48.6 Register Summary](#).

## 48.6 Register Summary

'|' here means a separate line to distinguish between TWAI working modes discussed in Section [48.4.1 Modes](#). The left describes the access in Operation mode. The right belongs to Reset mode and is marked in red. The addresses in this section are relative to Two-wire Automotive Interface base address provided in Table [6.3-2](#) in Chapter [6 System and Memory](#).

The abbreviations given in Column **Access** are explained in Section [Access Types for Registers](#).

| Name  | Description                       | Address | Access    |
|---|-----------------------------------|---------|-----------|
| <b>Configuration Registers</b>              |                                   |         |           |
| <a href="#">TWAI_MODE_REG</a>               | Mode Register                     | 0x0000  | R/W       |
| <a href="#">TWAI_CMD_REG</a>                | Command Register                  | 0x0004  | WO        |
| <a href="#">TWAI_BUS_TIMING_0_REG</a>       | Bus Timing Register 0             | 0x0018  | R/W       |
| <a href="#">TWAI_BUS_TIMING_1_REG</a>       | Bus Timing Register 1             | 0x001C  | R/W       |
| <a href="#">TWAI_ERR_WARNING_LIMIT_REG</a>  | Error Warning Limit Register      | 0x0034  | R/W       |
| <a href="#">TWAI_CLOCK_DIVIDER_REG</a>      | Clock Divider Register            | 0x007C  | R/W       |
| <a href="#">TWAI_SW_STANDBY_CFG_REG</a>     | Software Standby Register         | 0x0080  | R/W       |
| <a href="#">TWAI_HW_CFG_REG</a>             | Hardware Standby Register         | 0x0084  | R/W       |
| <a href="#">TWAI_HW_STANDBY_CNT_REG</a>     | Standby Time Length Register      | 0x0088  | R/W       |
| <a href="#">TWAI_IDLE_INTR_CNT_REG</a>      | Idle Status Time Length Register  | 0x008C  | R/W       |
| <b>Status Registers</b>                     |                                   |         |           |
| <a href="#">TWAI_STATUS_REG</a>             | Status Register                   | 0x0008  | RO        |
| <a href="#">TWAI_ARB_LOST_CAP_REG</a>       | Arbitration Lost Capture Register | 0x002C  | RO        |
| <a href="#">TWAI_ERR_CODE_CAP_REG</a>       | Error Code Capture Register       | 0x0030  | RO        |
| <a href="#">TWAI_RX_ERR_CNT_REG</a>         | Receive Error Counter Register    | 0x0038  | R/W       |
| <a href="#">TWAI_TX_ERR_CNT_REG</a>         | Transmit Error Counter Register   | 0x003C  | R/W       |
| <a href="#">TWAI_RX_MESSAGE_COUNTER_REG</a> | Receive Message Counter Register  | 0x0074  | RO        |
| <b>Interrupt Registers</b>                  |                                   |         |           |
| <a href="#">TWAI_INTERRUPT_REG</a>          | Interrupt Mask Register           | 0x000C  | RO        |
| <a href="#">TWAI_INTERRUPT_ENABLE_REG</a>   | Interrupt Enable Register         | 0x0010  | varies    |
| <b>Data Registers</b>                       |                                   |         |           |
| <a href="#">TWAI_DATA_0_REG</a>             | Data Register 0                   | 0x0040  | R/W       |
| <a href="#">TWAI_DATA_1_REG</a>             | Data Register 1                   | 0x0044  | R/W       |
| <a href="#">TWAI_DATA_2_REG</a>             | Data Register 2                   | 0x0048  | R/W       |
| <a href="#">TWAI_DATA_3_REG</a>             | Data Register 3                   | 0x004C  | R/W       |
| <a href="#">TWAI_DATA_4_REG</a>             | Data Register 4                   | 0x0050  | R/W       |
| <a href="#">TWAI_DATA_5_REG</a>             | Data Register 5                   | 0x0054  | R/W       |
| <a href="#">TWAI_DATA_6_REG</a>             | Data Register 6                   | 0x0058  | R/W       |
| <a href="#">TWAI_DATA_7_REG</a>             | Data Register 7                   | 0x005C  | R/W       |
| <a href="#">TWAI_DATA_8_REG</a>             | Data Register 8                   | 0x0060  | R/W   R/O |
| <a href="#">TWAI_DATA_9_REG</a>             | Data Register 9                   | 0x0064  | R/W   R/O |
| <a href="#">TWAI_DATA_10_REG</a>            | Data Register 10                  | 0x0068  | R/W   R/O |
| <a href="#">TWAI_DATA_11_REG</a>            | Data Register 11                  | 0x006C  | R/W   R/O |
| <a href="#">TWAI_DATA_12_REG</a>            | Data Register 12                  | 0x0070  | R/W   R/O |

| Name   | Description                        | Address | Access |
|--|------------------------------------|---------|--------|
| <b>Timestamp Register</b>                    |                                    |         |        |
| <a href="#">TWAI_TIMESTAMP_DATA_REG</a>      | Timestamp Data Register            | 0x0094  | RO     |
| <a href="#">TWAI_TIMESTAMP_PRESCALER_REG</a> | Timestamp Configuration Register 0 | 0x0098  | R/W    |
| <a href="#">TWAI_TIMESTAMP_CFG_REG</a>       | Timestamp Configuration Register 1 | 0x009C  | R/W    |

## 48.7 Registers

'|' here means a separate line. The left describes the access in Operation mode. The right belongs to Reset mode with red color. The addresses in this section are relative to Two-wire Automotive Interface base address (each TWAI 0 and TWAI 1 has an individual base address) provided in Table 6.3-2 in Chapter 6 [System and Memory](#).

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 48.1. TWAI\_MODE\_REG (0x0000)

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |   |   |   |   |       |
|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|---|---|---|---|-------|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_ACCEPTANCE_FILTER_MODE |  |  |  |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_SELF_TEST_MODE         |  |  |  |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_LISTEN_ONLY_MODE       |  |  |  |   |   |   |   |       |
|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_RESET_MODE             |  |  |  |   |   |   |   |       |
| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 4                           |  |  |  | 3 | 2 | 1 | 0 |       |
| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                           |  |  |  | 0 | 0 | 0 | 1 | Reset |

**TWAI\_RESET\_MODE** Configures the Operation mode of the TWAI Controller.

- 0: Operation mode
  - 1: Reset mode
- (R/W)

**TWAI\_LISTEN\_ONLY\_MODE** Configures whether to enter the Listen-only mode.

- 0: No effect
  - 1: Listen-only mode. In this mode, the nodes will only receive messages from the bus, without generating the acknowledge signal or updating the RX error counter.
- (R/W)

**TWAI\_SELF\_TEST\_MODE** Configures whether to enter the Self-test mode.

- 0: No effect
  - 1: Enter the Self-test mode. In this mode, the TX nodes can perform a successful transmission without receiving the acknowledge signal. This mode is often used to test a single node with the self-reception request command.
- (R/W)

**TWAI\_ACCEPTANCE\_FILTER\_MODE** Configures the filter mode.

- 0: Dual-filter mode
  - 1: Single-filter mode
- (R/W)

Register 48.2. TWAI\_CMD\_REG (0x0004)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |       |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|-------|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_SELF_RX_REQUEST<br>TWAI_CLEAR_DATA_OVERRUN<br>TWAI_RELEASE_BUFFER<br>TWAI_ABORT_TX<br>TWAI_TX_REQUEST |   |       |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 4 | 3 | 2 | 1  | 0 | Reset |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0     | 0 |  |

**TWAI\_TX\_REQUEST** Configures whether to drive nodes to start transmission.

- 0: No effect
- 1: Drive nodes to start transmission

(WO)

**TWAI\_ABORT\_TX** Configures whether to cancel a pending transmission request.

- 0: No effect
- 1: Cancel a pending transmission request

(WO)

**TWAI\_RELEASE\_BUFFER** Configures whether to release the RX buffer.

- 0: No effect
- 1: Release the RX buffer

(WO)

**TWAI\_CLEAR\_DATA\_OVERRUN** Configures whether to clear the data overrun status bit.

- 0: No effect
- 1: Clear the data overrun status bit

(WO)

**TWAI\_SELF\_RX\_REQUEST** Configures whether to drive nodes to start transmitting messages while also receiving messages on the bus simultaneously.

- 0: No effect
- 1: Drive nodes to start transmitting messages while also receiving messages on the bus (set the value of [TWAI\\_TX\\_REQUEST](#) to 0, or only transmission is allowed)

(WO)

### Register 48.3. TWAI\_BUS\_TIMING\_0\_REG (0x0018)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |    |                 |    |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|----|-----------------|----|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_SYNC_JUMP_WIDTH |    | TWAI_BAUD_PRESC |    |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                   | 15 | 14              | 13 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0                  |    | 0x00            |    |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_BAUD\_PRESC** Configures baud rate prescaler value, determining the frequency dividing ratio.

0: Low

1: High

(R/W)

**TWAI\_SYNC\_JUMP\_WIDTH** Configures Synchronization Jump Width (SJW), ranging from 1 ~ 4 Tq wide. (R/W)

#### Register 48.4. TWAI\_BUS\_TIMING\_1\_REG (0x001C)

Diagram illustrating the structure of the TWAI\_TSR register (32 bits):

- Bits 31 to 6: (reserved)
- Bits 5 to 3: TWAI\_TIME\_SEGMENT1
- Bits 2 to 0: TWAI\_TIME\_SAMPLING

**TWAI\_TIME\_SEGMENT1** Configures the width of PBS1. (R/W)

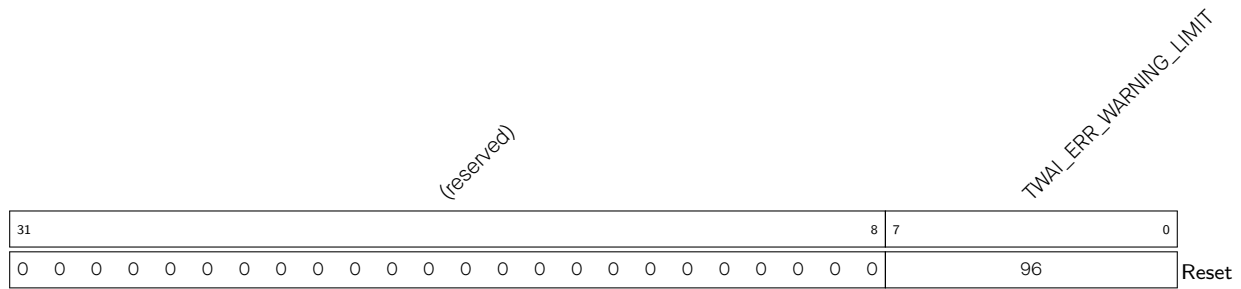
**TWAI\_TIME\_SEGMENT2** Configures the width of PBS2. (R/W)

**TWAI\_TIME\_SAMPLING** Configures the number of sample points.

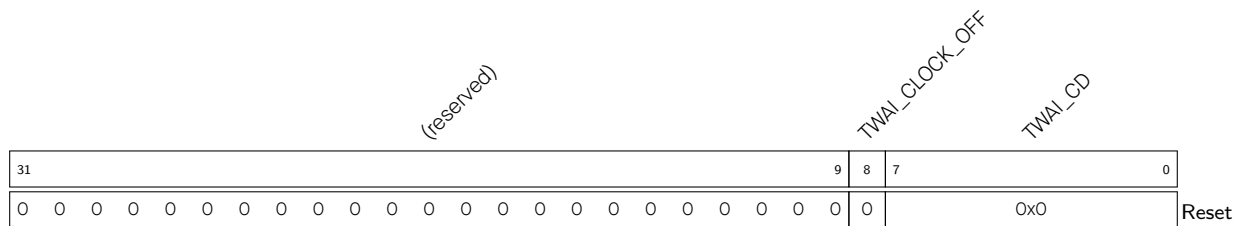
0: The bus is sampled once

1: The bus is sampled three times

(R/W)

**Register 48.5. TWAI\_ERR\_WARNING\_LIMIT\_REG (0x0034)**

**TWAI\_ERR\_WARNING\_LIMIT** Configures error warning threshold. When any of the error counter values ([TWAI\\_RX\\_ERR\\_CNT](#) or [TWAI\\_TX\\_ERR\\_CNT](#)) exceeds the threshold, the TWAI controller enters an error state; when all the error counter values are below the threshold, the TWAI controller exits the error state. An error warning interrupt will be triggered if the TWAI controller enters or exits an error state. (R/W)

**Register 48.6. TWAI\_CLOCK\_DIVIDER\_REG (0x007C)**

**TWAI\_CD** Configures the divisor of the external CLKOUT pin. (R/W)

**TWAI\_CLOCK\_OFF** Configures whether or not to enable the external CLKOUT pin in Reset mode.

0: Enable the external CLKOUT pin

1: Disable the external CLKOUT pin

(R/W)



Register 48.7. TWAI\_SW\_STANDBY\_CFG\_REG (0x0080)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_SW_STANDBY_CLR<br>TWAI_SW_STANDBY_EN |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2   | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1   | 0 | Reset |

**TWAI\_SW\_STANDBY\_EN** Configures whether to set standby signals with software.

0: No effect

1: Set standby signals

(R/W)

**TWAI\_SW\_STANDBY\_CLR** Configures whether to clear standby signals with software.

0: No effect

1: Clear standby signals

(R/W)

Register 48.8. TWAI\_HW\_CFG\_REG (0x0084)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_HW_STANDBY_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

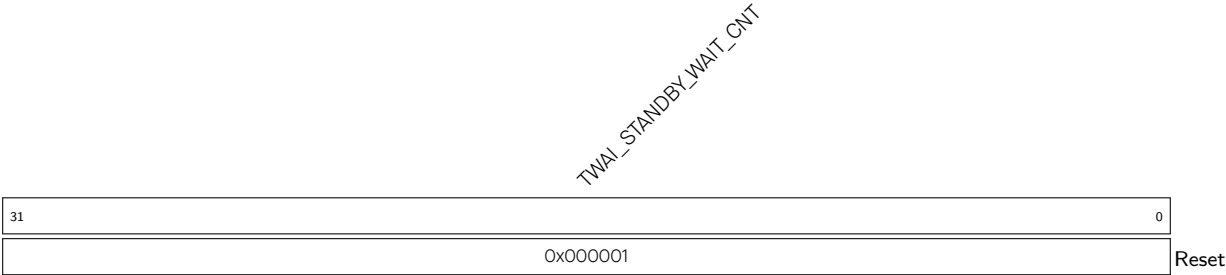
**TWAI\_HW\_STANDBY\_EN** Configures whether to enable the automatic standby function for hardware.

0: No effect

1: Enable the automatic standby function for hardware

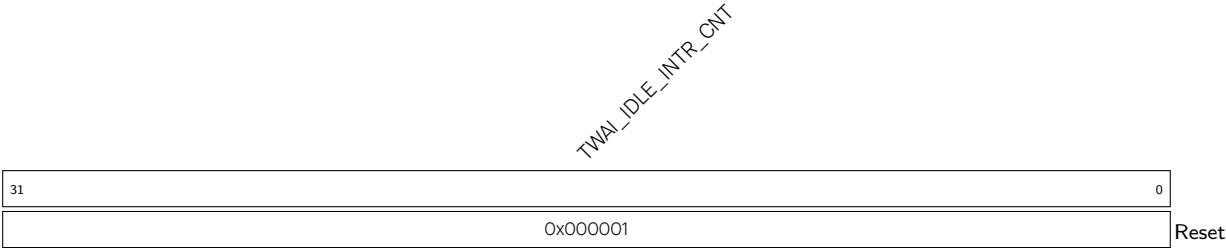
(R/W)

Register 48.9. TWAI\_HW\_STANDBY\_CNT\_REG (0x0088)



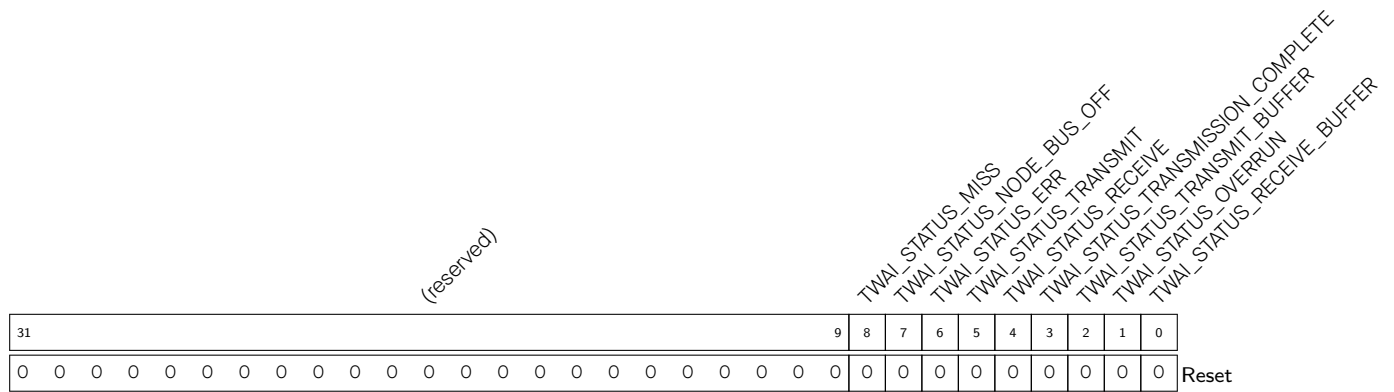
**TWAI\_STANDBY\_WAIT\_CNT** Configures the time required before hardware triggers the standby signal after entering idle status.  
Measurement unit: TWAI controller clock cycles.  
(R/W)

Register 48.10. TWAI\_IDLE\_INTR\_CNT\_REG (0x008C)



**TWAI\_IDLE\_INTR\_CNT** Configures the time required before hardware generates the bus idle status interrupt signal after entering idle status.  
Measurement unit: TWAI controller clock cycles.  
(R/W)

## Register 48.11. TWAI\_STATUS\_REG (0x0008)



**TWAI\_STATUS\_RECEIVE\_BUFFER** Represents whether or not the RX buffer is empty.

0: Empty

1: Not empty, with at least one received data packet.

(RO)

**TWAI\_STATUS\_OVERRUN** Represents whether or not the RX FIFO is full.

0: Not full

1: Full, and data overrun has occurred

(RO)

**TWAI\_STATUS\_TRANSMIT\_BUFFER** Represents whether or not the TX buffer is empty.

0: Not empty

1: Empty, and the CPU may write a message into it

(RO)

**TWAI\_STATUS\_TRANSMISSION\_COMPLETE** Represents whether or not the TWAI controller has sent an entire packet to the bus.

0: Not sent

1: Sent

(RO)

**TWAI\_STATUS\_RECEIVE** Represents whether or not the TWAI Controller is receiving a message from the bus.

0: Not receiving

1: Receiving

(RO)

**TWAI\_STATUS\_TRANSMIT** Represents whether or not the TWAI Controller is transmitting a message to the bus.

0: Not transmitting

1: Transmitting

(RO)

**TWAI\_STATUS\_ERR** Represents at least one of the RX/TX error counter has reached or exceeded the value set in register [TWAI\\_ERR\\_WARNING\\_LIMIT\\_REG](#). (RO)

Continued on the next page...

Register 48.11. LP\_UART\_INT\_RAW\_REG (0x0004)

Continued from the previous page...

**TWAI\_STATUS\_NODE\_BUS\_OFF** Represents whether or not the TWAI Controller involves in bus activities in bus-off status.

0: Involved

1: No longer involved

(RO)

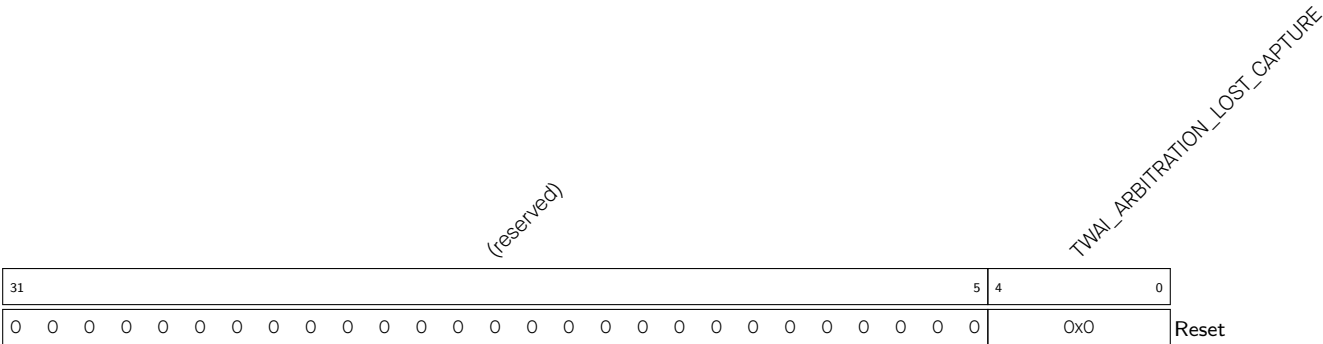
**TWAI\_STATUS\_MISS** Represents whether or not the data packet in the RX FIFO is complete.

0: The current packet is complete

1: The current packet is missing

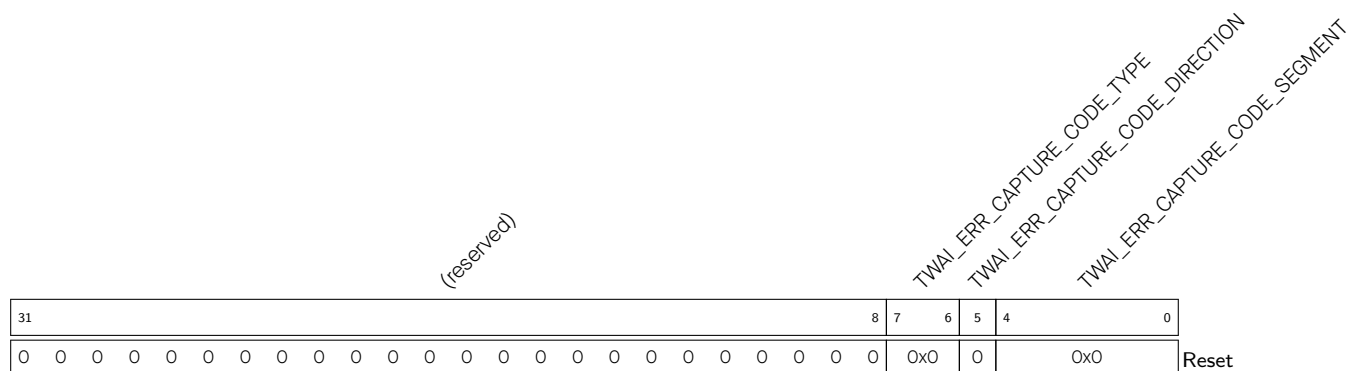
(RO)

Register 48.12. TWAI\_ARB\_LOST\_CAP\_REG (0x002C)



**TWAI\_ARB\_LOST\_CAPTURE** Represents the bit position of lost arbitration. (RO)

### Register 48.13. TWAI\_ERR\_CODE\_CAP\_REG (0x0030)



|                                      |  |
|--------------------------------------|--|
| <b>TWAI_ERR_CAPTURE_CODE_SEGMENT</b> | Represents the location of errors, see Table 48.4-11 for details. (RO) |
|--------------------------------------|--|

**TWAI\_ERR\_CAPTURE\_CODE\_DIRECTION** Represents transmission direction of the node when an error occurs.

0: Error occurs when transmitting a message

1: Error occurs when receiving a message

(RO)

**TWAI\_ERR\_CAPTURE\_CODE\_TYPE** Represents error types.

0: Bit error

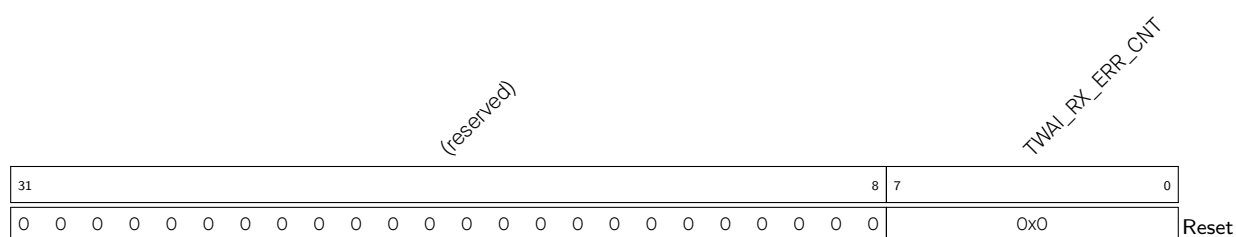
1: Form error

2: Stuff error

### 3: Others

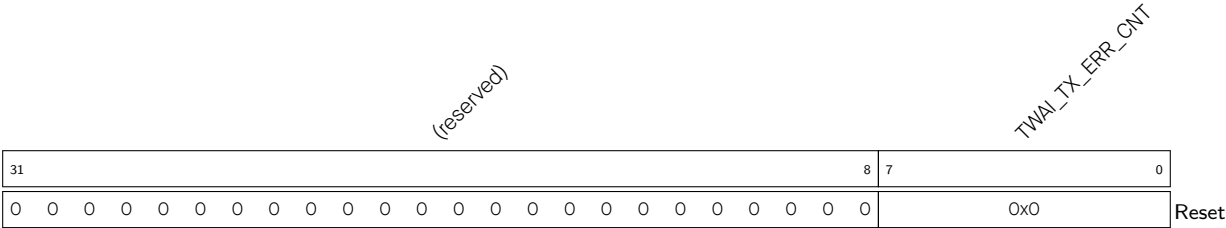
(RO)

#### Register 48.14. TWAI\_RX\_ERR\_CNT\_REG (0x0038)



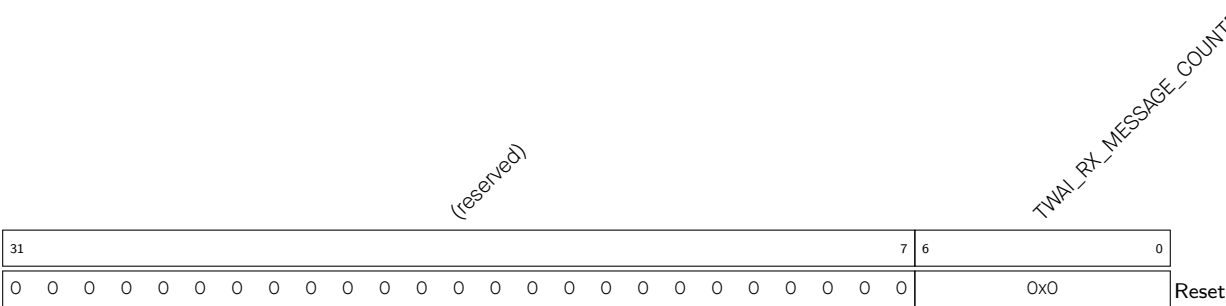
**TWAI\_RX\_ERR\_CNT** The RX error counter register, which reflects value changes in reception status.  
(R/W)

Register 48.15. TWAI\_TX\_ERR\_CNT\_REG (0x003C)



**TWAI\_TX\_ERR\_CNT** The TX error counter register, which reflects value changes in transmission status. (R/W)

Register 48.16. TWAI\_RX\_MESSAGE\_COUNTER\_REG (0x0074)



**TWAI\_RX\_MESSAGE\_COUNTER** Represents the number of messages available within the RX FIFO. (RO)

Register 48.17. TWAI\_INTERRUPT\_REG (0x000C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_IDLE_INT_ST<br>TWAI_BUS_ERR_INT_ST<br>TWAI_ARBITRATION_LOST_INT_ST<br>TWAI_ERR_PASSIVE_INT_ST<br>TWAI_TS_COUNTER_OVFL_INT_ST<br>TWAI_DATA_OVERRUN_INT_ST<br>TWAI_ERR_WARNING_INT_ST<br>TWAI_TRANSMIT_INT_ST<br>TWAI_RECEIVE_INT_ST |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9 | 8   | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |   |   |   |   |   |   |   |       |

**TWAI\_RECEIVE\_INT\_ST** The masked interrupt status of [TWAI\\_RX\\_INT](#). (RO)

**TWAI\_TRANSMIT\_INT\_ST** The masked interrupt status of [TWAI\\_TX\\_INT](#). (RO)

**TWAI\_ERR\_WARNING\_INT\_ST** The masked interrupt status of [TWAI\\_ERR\\_WARN\\_INT](#). (RO)

**TWAI\_DATA\_OVERRUN\_INT\_ST** The masked interrupt status of [TWAI\\_OVERRUN\\_INT](#). (RO)

**TWAI\_TS\_COUNTER\_OVFL\_INT\_ST** The masked interrupt status of [TWAI\\_TS\\_COUNTER\\_OVFL\\_INT](#). (RO)

**TWAI\_ERR\_PASSIVE\_INT\_ST** The masked interrupt status of [TWAI\\_ERR\\_PASSIVE\\_INT](#). (RO)

**TWAI\_ARBITRATION\_LOST\_INT\_ST** The masked interrupt status of [TWAI\\_ARB\\_LOST\\_INT](#). (RO)

**TWAI\_BUS\_ERR\_INT\_ST** The masked interrupt status of [TWAI\\_BUS\\_ERR\\_INT](#). (RO)

**TWAI\_IDLE\_INT\_ST** The masked interrupt status of [TWAI\\_BUS\\_STATE\\_INT](#). (RO)

Register 48.18. TWAI\_INTERRUPT\_ENABLE\_REG (0x0010)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |  |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|--|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  | TWAI_IDLE_INT_ENA<br>TWAI_BUS_ERR_INT_ENA<br>TWAI_ARBITRATION_LOST_INT_ENA<br>TWAI_ERR_PASSIVE_INT_ENA<br>TWAI_TS_COUNTER_OVFL_INT_ENA<br>TWAI_EXT_DATA_OVERRUN_INT_ENA<br>TWAI_EXT_ERR_TRANSMIT_INT_ENA<br>TWAI_EXT_RECEIVE_INT_ENA |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  | 9  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |  |   |   |   |   |   |   |   |   |   |       |

**TWAI\_EXT\_RECEIVE\_INT\_ENA** Write 1 to enable the [TWAI\\_RX\\_INT](#) interrupt. (R/W)

**TWAI\_EXT\_TRANSMIT\_INT\_ENA** Write 1 to enable the [TWAI\\_TX\\_INT](#) interrupt. (R/W)

**TWAI\_EXT\_ERR\_WARNING\_INT\_ENA** Write 1 to enable the [TWAI\\_ERR\\_WARN\\_INT](#) interrupt. (R/W)

**TWAI\_EXT\_DATA\_OVERRUN\_INT\_ENA** Write 1 to enable the [TWAI\\_OVERRUN\\_INT](#) interrupt. (R/W)

**TWAI\_TS\_COUNTER\_OVFL\_INT\_ENA** Write 1 to enable the [TWAI\\_TS\\_COUNTER\\_OVFL\\_INT](#) interrupt. (R/W)

**TWAI\_ERR\_PASSIVE\_INT\_ENA** Write 1 to enable the [TWAI\\_ERR\\_PASSIVE\\_INT](#) interrupt. (R/W)

**TWAI\_ARBITRATION\_LOST\_INT\_ENA** Write 1 to enable the [TWAI\\_ARB\\_LOST\\_INT](#) interrupt. (R/W)

**TWAI\_BUS\_ERR\_INT\_ENA** Write 1 to enable the [TWAI\\_BUS\\_ERR\\_INT](#) interrupt. (R/W)

**TWAI\_IDLE\_INT\_ENA** Write 1 to enable the [TWAI\\_BUS\\_STATE\\_INT](#) interrupt. (RO)

Register 48.19. TWAI\_DATA\_0\_REG (0x0040)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|-------|--|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_0 |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_0** In Operation mode, configures the 0th byte information of the data to be transmitted, or reads the 0th byte information of the data received. In Reset mode, configures the 1th byte of the filter code. (R/W)



**Register 48.20. TWAI\_DATA\_1\_REG (0x0044)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_1 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_1** In Operation mode, configures the 1st byte information of the data to be transmitted, or reads the 1st byte information of the data received. In Reset mode, configures the 2nd byte of the filter code. (R/W)

**Register 48.21. TWAI\_DATA\_2\_REG (0x0048)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_2 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_2** In Operation mode, configures the 2nd byte information of the data to be transmitted, or reads the 2nd byte information of the data received. In Reset mode, configures the 3rd byte of the filter code. (R/W)

**Register 48.22. TWAI\_DATA\_3\_REG (0x004C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |   |     |  |  |  |       |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|---|-----|--|--|--|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_DATA_3 |   |     |  |  |  |       |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8           | 7 |     |  |  |  | 0     |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0           | 0 | 0x0 |  |  |  | Reset |  |

**TWAI\_DATA\_3** In Operation mode, configures the 3rd byte information of the data to be transmitted, or reads the 3rd byte information of the data received. In Reset mode, configures the 4th byte of the filter code. (R/W)

### Register 48.23. TWAI\_DATA\_4\_REG (0x0050)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_4 |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_4** In Operation mode, configures the 4th byte information of the data to be transmitted, or reads the 4th byte information of the data received. In Reset mode, configures the 1st byte of the masked filter code. (R/W)

### Register 48.24. TWAI\_DATA\_5\_REG (0x0054)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_5 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 7           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**TWAI\_DATA\_5** In Operation mode, configures the 5th byte information of the data to be transmitted, or reads the 5th byte information of the data received. In Reset mode, configures the 2nd byte of the masked filter code. (R/W)

### Register 48.25. TWAI\_DATA\_6\_REG (0x0058)

[illegible]

**TWAI\_DATA\_6** In Operation mode, configures the 6th byte information of the data to be transmitted, or reads the 6th byte information of the data received. In Reset mode, configures the 3rd byte of the masked filter code. (R/W)

**Register 48.26. TWAI\_DATA\_7\_REG (0x005C)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |             |   |     |  |  |  |       |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------|---|-----|--|--|--|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TWAI_DATA_7 |   |     |  |  |  |       |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8           | 7 |     |  |  |  | 0     |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0           | 0 | 0x0 |  |  |  | Reset |  |

**TWAI\_DATA\_7** In Operation mode, configures the 7th byte information of the data to be transmitted, or reads the 7th byte information of the data received. In Reset mode, configures the 4th byte of the masked filter code. (R/W)

**Register 48.27. TWAI\_DATA\_8\_REG (0x0060)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_8 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_8** In Operation mode, configures the 8th byte information of the data to be transmitted, or reads the 8th byte information of the data received. (R/W)  
In Reset mode, reserved. (RO)

**Register 48.28. TWAI\_DATA\_9\_REG (0x0064)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |             |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_9 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8           | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0         |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_9** In Operation mode, configures the 9th byte information of the data to be transmitted, or reads the 9th byte information of the data received. (R/W)  
In Reset mode, reserved. (RO)

**Register 48.29. TWAI\_DATA\_10\_REG (0x0068)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_10 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8            | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0          |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

**TWAI\_DATA\_10** In Operation mode, configures the 10th byte information of the data to be transmitted, or reads the 10th byte information of the data received. (R/W)  
 In Reset mode, reserved. (RO)

**Register 48.30. TWAI\_DATA\_11\_REG (0x006C)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_11 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8            | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0          |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

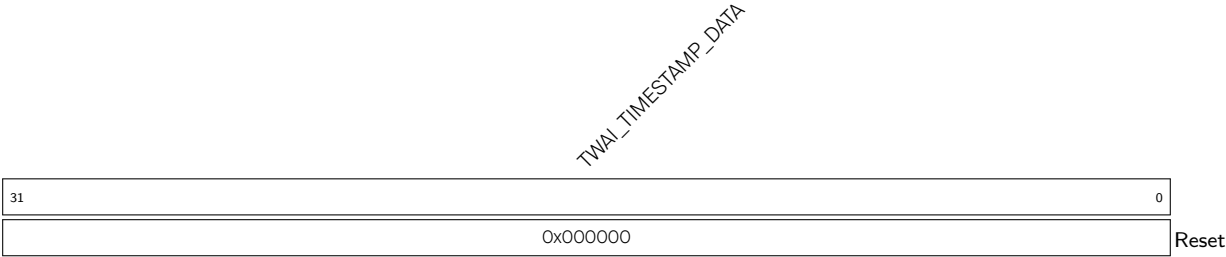
**TWAI\_DATA\_11** In Operation mode, configures the 11th byte information of the data to be transmitted, or reads the 11th byte information of the data received. (R/W)  
 In Reset mode, reserved. (RO)

**Register 48.31. TWAI\_DATA\_12\_REG (0x0070)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TWAI_DATA_12 |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8            | 7 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0          |   |   |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |

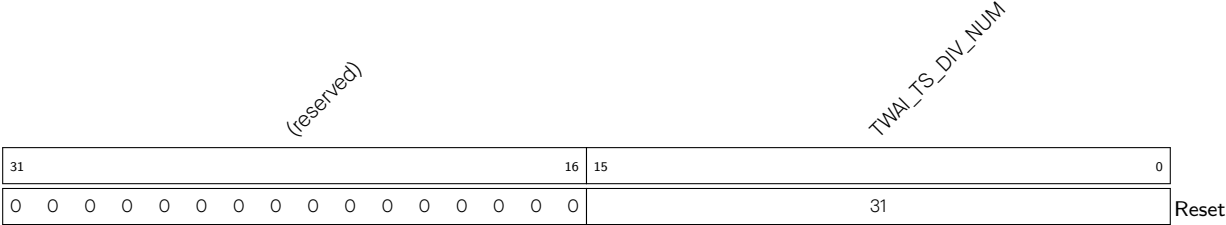
**TWAI\_DATA\_12** In Operation mode, configures the 12th byte information of the data to be transmitted, or reads the 12th byte information of the data received. (R/W)  
 In Reset mode, reserved. (RO)

Register 48.32. TWAI\_TIMESTAMP\_DATA\_REG (0x0094)



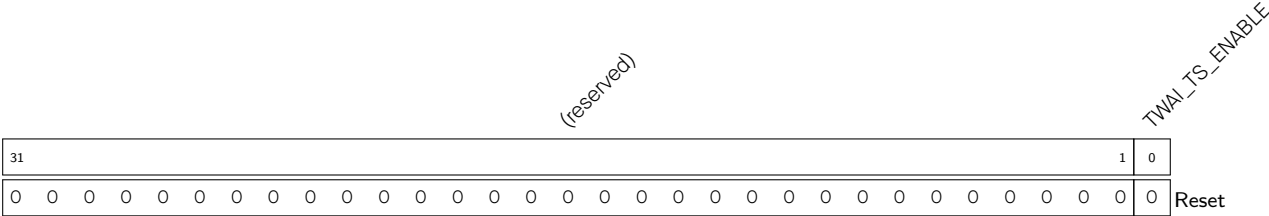
**TWAI\_TIMESTAMP\_DATA** The timestamp of the TWAI frame indicated by the RX FIFO read pointer corresponds to the time when the current TWAI frame was received. Valid only when [TWAI\\_TS\\_ENABLE](#) is enabled. (RO)

Register 48.33. TWAI\_TIMESTAMP\_PRESCALER\_REG (0x0098)



**TWAI\_TS\_DIV\_NUM** Configures the clock divisor of the timestamp counter. (R/W)

Register 48.34. TWAI\_TIMESTAMP\_CFG\_REG (0x009C)



**TWAI\_TS\_ENABLE** Configures whether to enable the timestamp collection function.

- 0: Disable
- 1: Enable

(R/W)

## Chapter 49

# SD/MMC Host Controller (SDHOST)

## 49.1 Overview

The ESP32-P4 memory card interface controller provides a hardware interface between the Advanced Peripheral Bus (APB) and an external memory device. The memory card interface allows the ESP32-P4 to be connected to SDIO (secure digital I/O) memory cards, MMC (multimedia cards) and devices with a CE-ATA (Consumer Electronics Advanced Transport Architecture) interface. It supports two external cards (Card0 and Card1). All SD/MMC module interface signals only connect to GPIO pins via GPIO matrix.

## 49.2 Features

This module supports the following features:

- Two external cards
- SD memory Card specification V3.0 and V3.01, with a maximum transfer rate of DDR50
- MMC: V4.41, V4.5, and V4.51, with a maximum transfer rate of DDR50
- CE-ATA: V1.1
- 1-bit, 4-bit, and 8-bit modes

The SD/MMC controller topology is shown in Figure 49.2-1. The controller supports two peripherals, but they cannot function at the same time.

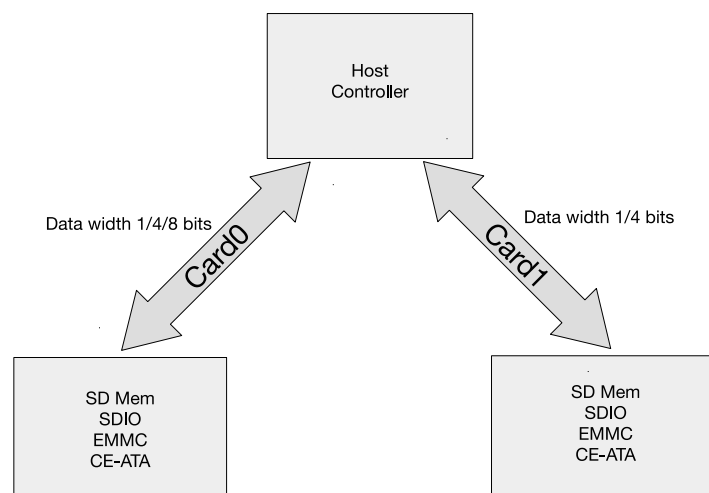


Figure 49.2-1. SD/MMC Controller Topology

## 49.3 SD/MMC External Interface Signals

The primary external interface signals, which enable the SD/MMC controller to communicate with an external device, are clock (sdhost\_cclk\_out\_1.eg:card1), command (sdhost\_ccmd\_out\_1), and data signals (sdhost\_cdata\_in\_1[7:0]/sdhost\_cdata\_out\_1[7:0]). Additional signals include the card interrupt, card detect, and write protect signals. The direction of each signal is shown in Figure 49.3-1. The direction and description of each pin are listed in Table 49.3-1.

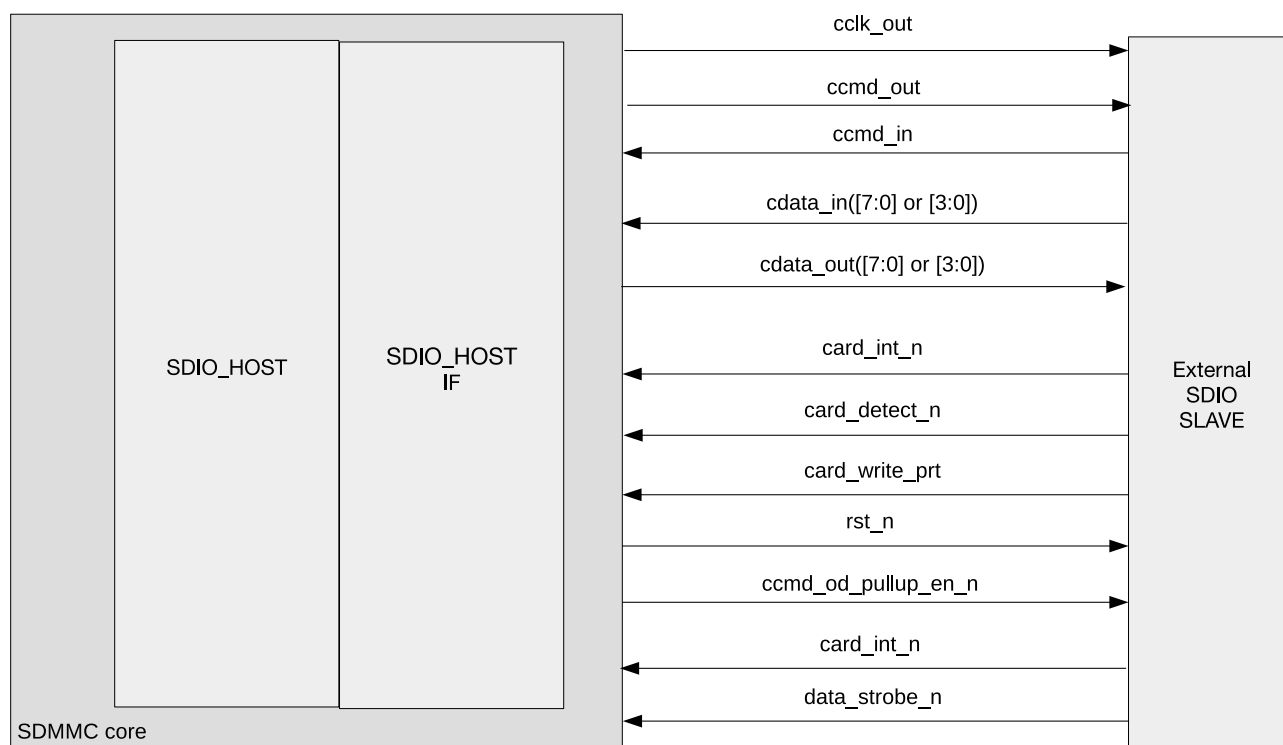


Figure 49.3-1. SD/MMC Controller External Interface Signals

Table 49.3-1. SD/MMC Signal Description

| Signal                | Direction | Description                        |
|-----------------------|-----------|------------------------------------|
| sdhost_cclk_out       | Output    | Clock signals for slave device     |
| sdhost_ccmd           | Duplex    | Duplex command/response lines      |
| sdhost_cdata          | Duplex    | Duplex data read/write lines       |
| sdhost_card_detect_n  | Input     | Card detection input line          |
| sdhost_card_write_prt | Input     | Card write protection status input |

## 49.4 Functional Description

### 49.4.1 SD/MMC Host Controller Architecture

The SD/MMC host controller consists of two main functional blocks, as shown in Figure 49.4-1:

- Bus Interface Unit (BIU): Provides the APB interface for registers, access to RAM data, and DMA data read and write operations.

- Card Interface Unit (CIU): Handles external memory card interface protocols and provides clock control.

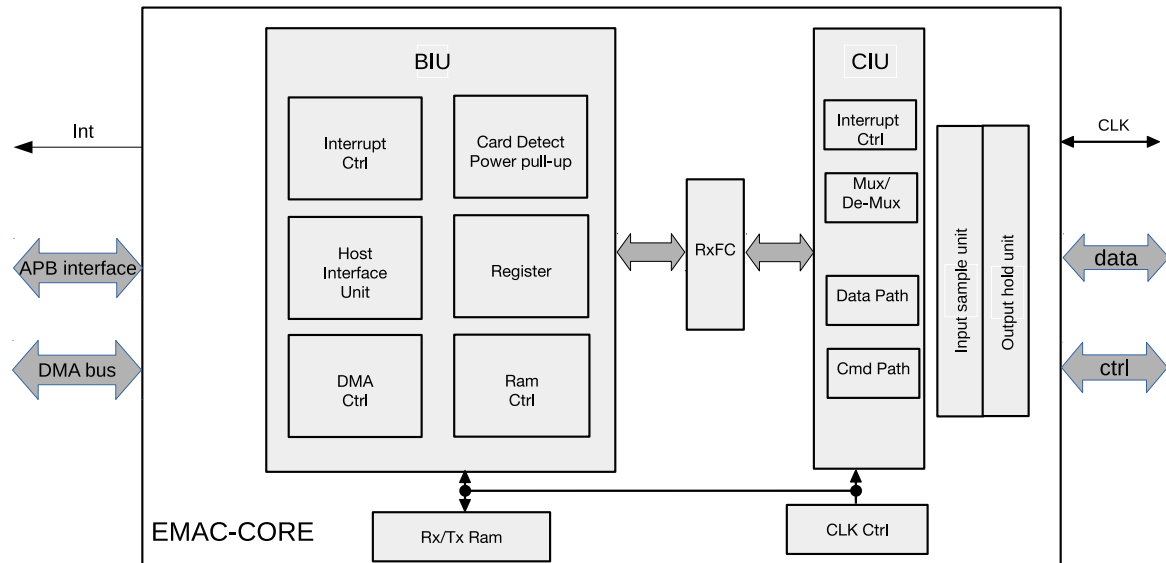


Figure 49.4-1. SDIO Host Block Diagram

#### 49.4.1.1 Bus Interface Unit (BIU)

The BIU provides access to registers and RAM data through the Host Interface Unit (HIU). Additionally, it provides a method to access to memory data through a DMA interface. Figure 49.4-1 illustrates the internal components of the BIU.

The BIU provides the following functions:

- Host interface
- DMA interface
- Interrupt control
- Register access
- FIFO access
- Power-up/pull-up control and card detection

#### 49.4.1.2 Card Interface Unit (CIU)

The CIU module implements the dedicated card slot specifications. Within the CIU, the command path control unit and data path control unit are used to interface with the command and data ports, respectively, of the SD/MMC/CE-ATA cards. The CIU also provides clock control. Figure 49.4-1 illustrates the internal structure of the CIU, which consists of the following primary functional blocks:

- Command path
- Data path
- SDIO interrupt control
- Clock control
- MUX (multiplexer) and De-MUX (de-multiplexer) unit



## 49.4.2 Command Path

The command path performs the following functions:

- Configures clock parameters
- Configures card command parameters
- Sends commands to card bus (sdhost\_ccmd\_out line)
- Receives responses from card bus (sdhost\_ccmd\_in line)
- Sends responses to BIU
- Drives the P-bit on the command line

The command path state machine is shown in Figure 49.4-2.

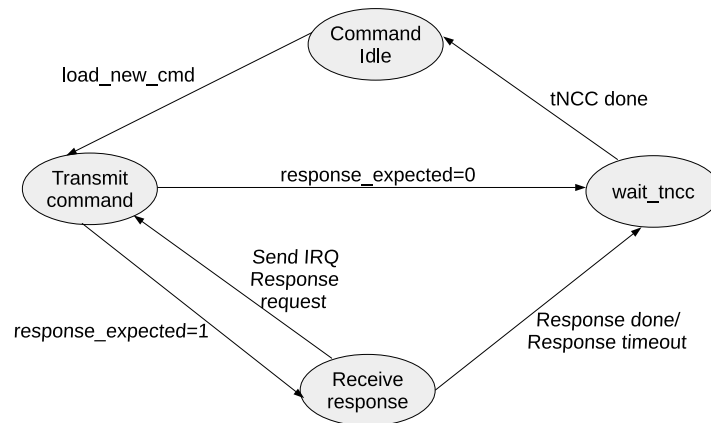


Figure 49.4-2. Command Path State Machine

## 49.4.3 Data Path

The data path block pops RAM data and transmits them on sdhost\_cdata\_out during a write-data transfer, or it receives data on sdhost\_cdata\_in and pushes them into RAM during a read-data transfer. The data path loads new data parameters, i.e., expected data, read/write data transfer, stream/block transfer, block size, byte count, card type, timeout registers, etc., whenever a data transfer command is not in progress.

If the `SDHOST_DATA_EXPECTED` bit is set in the `SDHOST_CMD_REG` register, the new command is a data transfer command and the data path starts one of the following operations:

- Transmitting data if the `SDHOST_READ_WRITE` bit is 1
- Receiving data if the `SDHOST_READ_WRITE` bit is 0

### 49.4.3.1 Data Transmit

The module starts data transmission two clock cycles after a response for the data write command is received. This occurs even if the command path detects a response error or a cyclic redundancy check (CRC) error in a response. If no response is received from the card until the response timeout, no data will be transmitted. Depending on the value of the `SDHOST_TRANSFER_MODE` bit in the `SDHOST_CMD_REG` register, the data transmit state machine adds data to the card's data bus in a stream or in block(s). The data transmit state machine is shown in Figure 49.4-3.

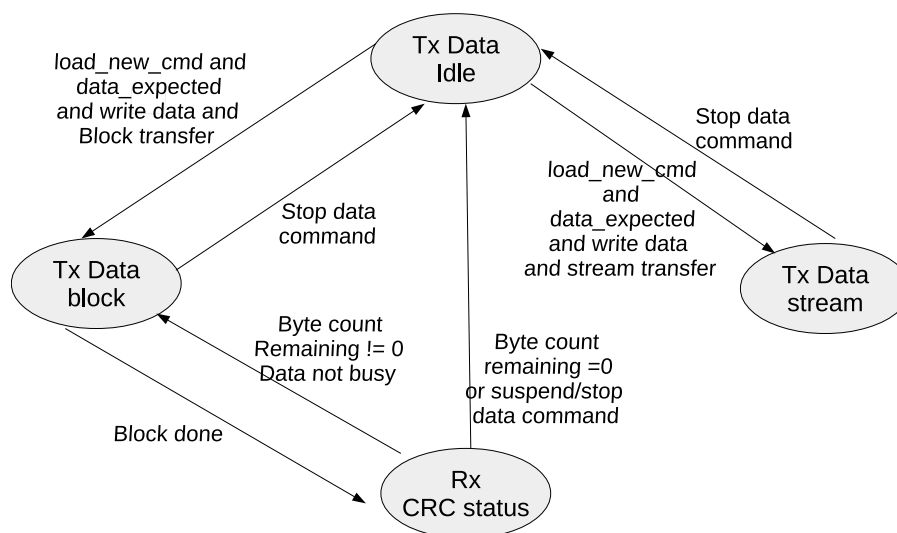


Figure 49.4-3. Data Transmit State Machine

### 49.4.3.2 Data Receive

The module receives data two clock cycles after the end bit of a data read command, even if the command path detects a response error or a CRC error. If no response is received from the card and a response timeout occurs, the BIU does not receive a signal about the completion of the data transfer. If the command sent by the CIU is an illegal operation for the card, it would prevent the card from starting a read-data transfer, and the BIU will not receive a signal about the completion of the data transfer.

If no data is received by the data timeout, the data path signals a data timeout to the BIU, which marks an end to the data transfer. Based on the value of the `SDHOST_TRANSFER_MODE` bit in the `SDHOST_CMD_REG` register, the data receive state machine gets data from the card's data bus in a stream or block(s). The data receive state machine is shown in Figure 49.4-4.

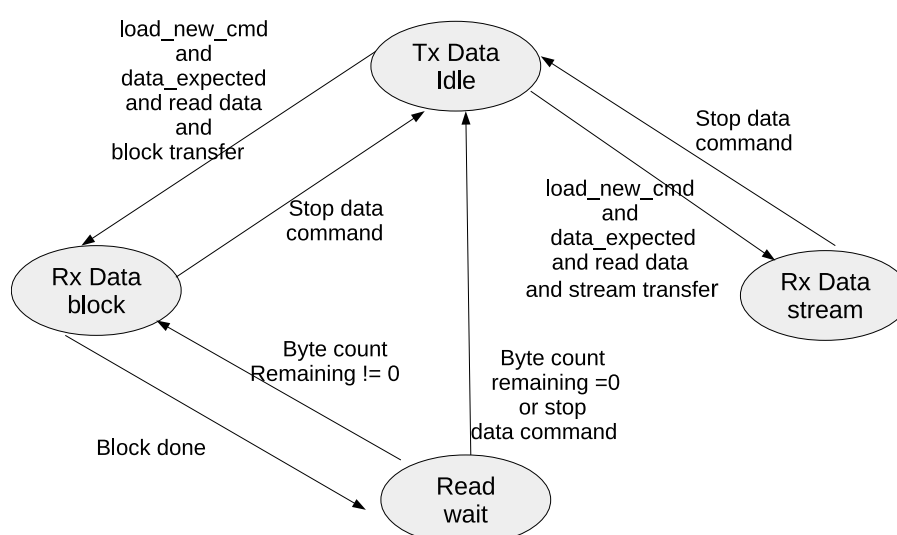


Figure 49.4-4. Data Receive State Machine

## 49.5 Software Restrictions for CIU Operations

- Only one card at a time can be selected to execute a command or data transfer. For example, when data are being transferred to or from a card, a new command must not be issued to another card. A new command, however, can be issued to the same card, allowing it to read the device status or stop the transfer.
- Only one data transfer command can be issued at a time.
- During an open-ended card write operation, if the card clock is stopped because RAM is empty, the software must first fill RAM with data, and start the card clock. Only then can it issue a stop/abort command to the card.
- During an SDIO/Combo card transfer, if the card function is suspended and the software wants to resume the suspended transfer, it must first reset and then release RAM by configuring the [SDHOST\\_FIFO\\_RESET](#) bit, and then issue the resume command as if it were a new data transfer command.
- When issuing card reset commands (CMD0, CMD15 or CMD52\_reset) while a card data transfer is in progress, the software must set the [SDHOST\\_STOP\\_ABORT\\_CMD](#) bit in the [SDHOST\\_CMD\\_REG](#) register, so that the CIU can stop the data transfer after issuing the card reset command.
- When the controlling bit for end bit error is set in the [SDHOST\\_RINTSTS\\_REG](#) register, the CIU cannot control SDIO interrupts. In such a case, the software must ignore SDIO interrupts and issue a stop/abort command to the card, so that the card stops transmitting data.
- If the card clock is stopped because RAM is full during a card read, the software must read at least two RAM addresses to restart the card clock.
- Only one CE-ATA device at a time can be selected for a command or data transfer. For example, when data are transferred from a CE-ATA device, a new command must not be sent to another CE-ATA device.
- If the CE-ATA device interrupts are enabled (nIEN=0), a new SDHOST\_RW\_BLK command must not be sent to the same device if the execution of a SDHOST\_RW\_BLK command is already in progress. Only the Command Completion Signal Disable (CCSD) command can be sent while waiting for the Command Completion Signal (CCS).
- If, however, the CE-ATA device interrupts are disabled (nIEN=1), a new command can be issued to the same device, allowing it to read status information.
- Open-ended transfers are not supported for CE-ATA devices.
- The sdhost\_send\_auto\_stop signal is not supported (software must not set the [SDHOST\\_SEND\\_AUTO\\_STOP](#) bit) for CE-ATA transfers.

After configuring the command start bit to 1, the values of the following registers cannot be changed before a command has been issued:

- CMD - command
- CMDARG - command argument
- BYTCNT - byte count
- BLKSIZ - block size
- CLKDIV - clock divider

- CKLENA - clock enable
- CLKSRC - clock source
- TMOUT - timeout
- CTYPE - card type

## 49.6 RAM for Receiving and Transmitting Data

The submodule RAM is a buffer area for transmitting and receiving data. It can be divided into two units: one is for transmitting data, and the other is for receiving data. The process of transmitting and receiving data can be achieved by the CPU and DMA for reading and writing. The latter method is described in detail in Section [49.8](#).

### 49.6.1 TX RAM Module

There are two ways to enable a write operation: CPU and DMA write.

For CPU write operations to TX RAM, write the data directly into the [SDHOST\\_BUFFIFO\\_REG](#) register via the APB interface. The corresponding FIFO width is 32 bits and the depth is 512.

For DMA write operations to TX RAM, set up DMA linked list descriptors as described in Section [49.8](#).

### 49.6.2 RX RAM Module

There are two ways to enable a read operation: CPU and DMA read.

For CPU read operations from RX RAM, read the data directly from the [SDHOST\\_BUFFIFO\\_REG](#) register via the APB interface. The corresponding FIFO width is 32 bits and the depth is 512.

For DMA read operations from RX RAM, set up DMA linked list descriptors as described in Section [49.8](#).

## 49.7 DMA Linked List

Each unit in the linked list structure consists of two parts: a descriptor and a data buffer. In other words, each descriptor points to a unique data buffer and to the next descriptor in the linked list. Figure [49.7-1](#) shows the linked list.

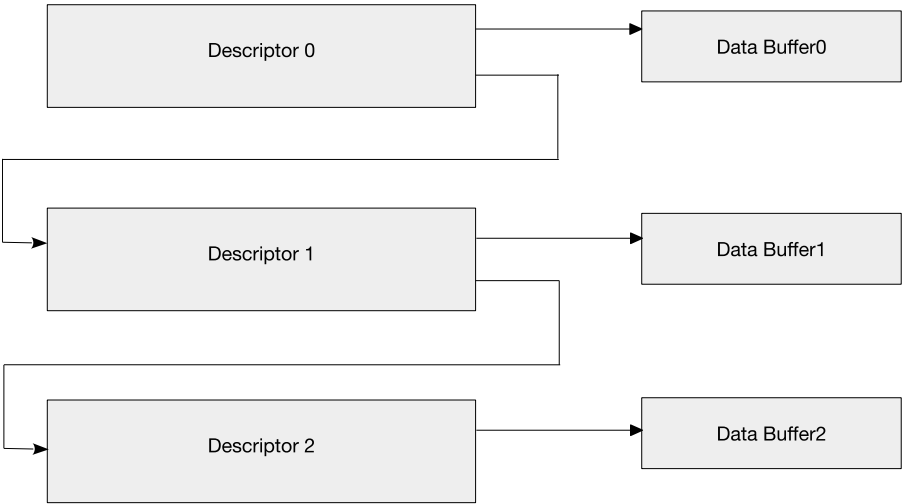


Figure 49.7-1. Linked List Structure

49.8 DMA Descriptor Format

Each descriptor consists of four words as shown in 49.8-1. Table 49.8-1, Table 49.8-2, Table 49.8-3, Table 49.8-4 provide the descriptions of these four words.

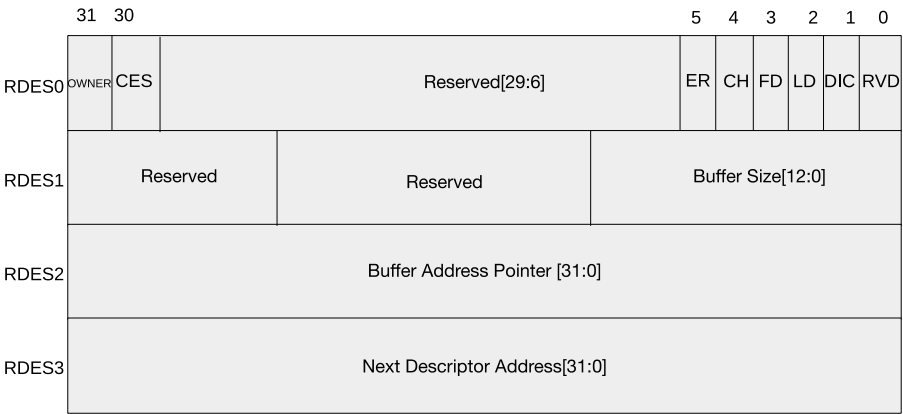


Figure 49.8-1. Descriptor Format

The DES0 field contains control and status information.

Table 49.8-1. DES0 Descriptor Field

| Bits | Name  | Description  |
|------|-------|--|
| 31   | OWNER | When set to 1, this bit indicates that the descriptor is owned by the DMA Controller. When reset to 0, it indicates that the descriptor is owned by the host. The DMA clears this bit when it completes the data transfer. |

| Bits | Name                                  | Description  |
|------|---------------------------------------|--|
| 30   | CES (Card Error Summary)              | <p>This bit indicates the status of the card's read/write operations.</p> <p>This bit is the logical OR of the following bits in the <a href="#">SDHOST_RINTSTS_REG</a> register.</p> <ul style="list-style-type: none"> <li>• EBE: End Bit Error</li> <li>• RTO: Response Timeout</li> <li>• RCRC: Response CRC</li> <li>• SBE: Start Bit Error</li> <li>• DRTO: Data Read Timeout</li> <li>• DCRC: Data CRC for Receive</li> <li>• RE: Response Error</li> </ul> |
| 29:6 | Reserved                              | Reserved   |
| 5    | ER (End of Ring)                      | When set to 1, this bit indicates that the linked list has reached its final descriptor. The DMA Controller then returns to the base address of the linked list, creating a linked list ring.  |
| 4    | CH (Second Address Chained)           | When set to 1, this bit indicates that the second address in the descriptor is the next descriptor address. When this bit is set to 1, BS2 (DES1[25:13]) must be all zeros.  |
| 3    | FD (First Descriptor)                 | When set to 1, this bit indicates that this descriptor contains the first buffer of the data. If the size of the first buffer is 0, the next descriptor contains the beginning of the data.  |
| 2    | LD (Last Descriptor)                  | This bit is associated with the last data block of a DMA transfer. When set to 1, the bit indicates that the buffers pointed by this descriptor are the last buffers of the data. After this descriptor is completed, the remaining byte count is 0. In other words, after the descriptor with the LD bit set is completed, the remaining byte count should be 0.  |
| 1    | DIC (Disable Interrupt on Completion) | When set to 1, this bit prevents the setting of the TI/RI bit of the DMA Status Register ( <a href="#">SDHOST_IDSTS_REG</a> ) for the data that ends in the buffer pointed by this descriptor.   |
| 0    | Reserved                              | Reserved   |

The DES1 field contains the buffer size.

**Table 49.8-2. DES1 Descriptor Field**

| Bits  | Name     | Description |
|-------|----------|-------------|
| 31:26 | Reserved | Reserved    |
| 25:13 | Reserved | Reserved    |

| Bits | Name             | Description  |
|------|------------------|--|
| 12:0 | BS (Buffer Size) | These bits indicate the size of the data buffer byte size, which must be a multiple of four. When the buffer size is not a multiple of four, the resulting behavior is undefined. This field must not be zero. |

The DES2 field contains the address pointer to the data buffer.

**Table 49.8-3. DES2 Descriptor Field**

| Bits | Name                   | Description  |
|------|------------------------|--|
| 31:0 | Buffer Address Pointer | These bits indicate the address of the data buffer. The buffer address must be word-aligned. |

The DES3 field contains the address pointer to the next descriptor if the present descriptor is not the last one in a linked list structure.

**Table 49.8-4. DES3 Descriptor Field**

| Bits | Name                    | Description  |
|------|-------------------------|--|
| 31:0 | Next Descriptor Address | If CH (DESO[4]) is set to 1, these bits contains the pointer to the next descriptor.<br>If this is not the last descriptor in a linked list structure, bits 1 and 0 must be zero, i.e., DES3[1:0] = 0. |

## 49.9 Programming Procedures

### 49.9.1 Initializing Registers

To initialize registers, perform the following steps:

1. Write to the control register [SDHOST\\_CTRL\\_REG](#), the raw interrupt register [SDHOST\\_RINTSTS\\_REG](#), and SDIO interrupt mask register [SDHOST\\_INTMASK\\_REG](#) to clear pending interrupts and configure controlling and interrupt parameters.
2. Write clock divider configuration register [SDHOST\\_CLKDIV\\_REG](#), clock source selection register [SDHOST\\_CLKSRC\\_REG](#), and clock enable register [SDHOST\\_CLKENA\\_REG](#) to configure the card clock.
3. Write other configuration registers based on card parameters. For example, configure
  - card bus width ([SDHOST\\_CTYPE\\_REG](#))
  - user ID ([SDHOST\\_USRID\\_REG](#))
  - UHS mode voltage and DDR ([SDHOST\\_UHS\\_REG](#))
  - EMMC mode start bit ([SDHOST\\_EMMCDDR\\_REG](#))
  - SDIO mode ([SDHOST\\_CLK\\_EDGE\\_SEL\\_REG](#))
  - timeout value ([SDHOST\\_TMOUT\\_REG](#))

- debounce filter ([SDHOST\\_DEBNCE\\_REG](#))
- internal phase shift ([SDHOST\\_ENSHIFT\\_REG](#))

You can reset the card with [SDHOST\\_RST\\_N\\_REG](#).

## 49.9.2 Sending Commands

To send commands, perform the following steps:

1. Write the command argument register [SDHOST\\_CMDARG\\_REG](#) with the appropriate command argument parameter.
2. For data transfer, write the data size register [SDHOST\\_BYTCNT\\_REG](#), the block size register [SDHOST\\_BLKSIZE\\_REG](#) register, and the card threshold control register [SDHOST\\_CARDTHRCTL\\_REG](#) to configure data transfer parameters.
3. Data transfer can be achieved by DMA or FIFO, and DMA is preferable.
  - To transmit and receive data via DMA, configure the DMA Controller according to Section [49.9.3](#), Section [49.9.4](#), and Section [49.9.5](#).
  - To transmit and receive data via FIFO, configure the FIFO threshold via FIFO configuration register [SDHOST\\_FIFOTH\\_REG](#). For writing to a card, software should write data to the FIFO via [SDHOST\\_BUFFIFO\\_REG](#) continuously during command execution.
4. Configure and start the command via the [SDHOST\\_CMD\\_REG](#).
5. Wait until the [SDHOST\\_START\\_CMD](#) bit in the [SDHOST\\_CMD\\_REG](#) register is cleared by hardware upon command reception. When hardware cannot receive the command, it will set the 12th bit HLE in the [SDHOST\\_RINTSTS\\_REG](#) register to 1.
6. Read the [SDHOST\\_RINTSTS\\_REG](#) register or enable interrupts to check command execution status. If needed, read the [SDHOST\\_RESP<sub>n</sub>\\_REG](#) (*n* ranges from 0 ~ 3) register to get command response from the card.
7. If data is read from the card via FIFO, software can get the data returned by the card via reading the [SDHOST\\_BUFFIFO\\_REG](#) register.

Please refer to the card specification for the command format, and configure register field values depending on the command format.

## 49.9.3 Initializing DMA

To initialize the DMA Controller, perform the following steps:

1. Write to the DMA bus mode register ([SDHOST\\_BMOD\\_REG](#)) to configure the host bus's access parameters.
2. Write to the DMA interrupt enable register ([SDHOST\\_IDINTEN\\_REG](#)) to mask unnecessary interrupt causes.
3. Create either a transmit or receive linked list. Then write the starting address of the first descriptor in the linked list to the DMA Controller's linked list base address register ([SDHOST\\_DBADDR\\_REG](#)).
4. The DMA Controller engine proceeds to get descriptors from the linked list.



## 49.9.4 Initializing DMA Transmission

To initialize DMA transmission, perform the following steps:

1. The host sets up the descriptor fields (DESO-DES3) for transmission, and sets the OWNER bit (DESO[31]) to 1. The host also prepares the data buffer.
2. The host writes the write data command to the command register [SDHOST\\_CMD\\_REG](#).
3. The host sets the required transmit threshold via the [SDHOST\\_TX\\_WMARK](#) field in the [SDHOST\\_FIFOTH\\_REG](#) register.
4. The DMA Controller engine fetches the descriptor and checks the OWNER bit. If the OWNER bit is not set, it means that the host owns the descriptor. In this case, the DMA Controller enters a suspend state and asserts the Descriptor Unable interrupt via the [SDHOST\\_IDSTS\\_REG](#) register. The host then needs to release the DMA Controller by writing any value to [SDHOST\\_PLDMND\\_REG](#).
5. The DMA Controller waits for the Command Done (CMDD) bit in the [SDHOST\\_RINTSTS\\_REG](#) register to be set to 1 with no errors from BIU, which indicates that a transfer has completed.
6. The DMA Controller engine waits for a DMA interface request from BIU. This request is generated based on the configured transmit threshold value. For the last byte of data that cannot be accessed using a burst, a single transfer is performed on the AHB bus.
7. The DMA Controller fetches the transmit data from the data buffer in the host memory and transfers them to RAM in preparation for transmission to the card.
8. When data span across multiple descriptors, the DMA Controller fetches the next descriptor and continues with its operation with the next descriptor. The Last Descriptor bit indicates whether the data span multiple descriptors or not.
9. When data transmission is complete, the status information is updated in the [SDHOST\\_IDSTS\\_REG](#) register by setting the [SDHOST\\_IDSTS\\_TI](#) bit to 1 if it has already been enabled. Also, the OWNER bit is cleared by the DMA Controller by updating the DESO field.

## 49.9.5 Initializing DMA Reception

To initialize DMA reception, perform the following steps:

1. The host sets up the descriptor fields (DESO-DES3) for reception, and sets the OWNER bit (DESO[31]) to 1.
2. The host writes the read data command in the [SDHOST\\_CMD\\_REG](#) register in BIU.
3. The host sets the required receive threshold level via the [SDHOST\\_RX\\_WMARK](#) field in the [SDHOST\\_FIFOTH\\_REG](#) register.
4. The DMA Controller engine fetches the descriptor and checks the OWNER bit. If the OWNER bit is not set, it means that the host owns the descriptor. In this case, the DMA enters suspend state and asserts the Descriptor Unable interrupt via the [SDHOST\\_IDSTS\\_REG](#) register. The host then needs to release the DMA Controller by writing any value to [SDHOST\\_PLDMND\\_REG](#).
5. The DMA Controller waits for the Command Done (CMDD) bit in the [SDHOST\\_RINTSTS\\_REG](#) register to be set to 1 with no errors from BIU, which indicates that a reception has been completed.

6. The DMA Controller engine waits for a DMA interface request from BIU. This request is generated based on the configured receive threshold value. For the last byte of data that cannot be accessed using a burst, a single transfer is performed on the AHB bus.
7. The DMA Controller fetches the data from RAM and transfers them to the host memory.
8. When data span across multiple descriptors, the DMA Controller fetches the next descriptor and continues with its operation with the next descriptor. The Last Descriptor bit indicates whether the data span multiple descriptors or not.
9. When data reception is complete, the status information is updated in the [SDHOST\\_IDSTS\\_REG](#) register by setting the [SDHOST\\_IDSTS\\_RI](#) bit to 1, if it has already been enabled. Also, the OWNER bit is cleared by the DMA Controller by updating the DESO field.

## 49.10 Clock Phase Selection

The phase of the SD/MMC Host Controller clock source is configurable, so as to adjust the setup time sequence for the input or output data signals.

The clock source of the SD/MMC Host Controller can be a high-performance clock at a high frequency or a low-power clock at a low frequency. When the clock source is a high-performance clock, the internal signal clock phase, output signal driving clock phase, and input signal sampling clock phase can be configured via the [SDHOST\\_DLL\\_CLK\\_CONF\\_REG](#), in the unit of 1/64 clock source period. When the clock source is a low-power clock, the internal signal clock phase, output signal driving clock phase, and input signal sampling clock phase can be configured via the system clock register. The phase options are 0 degrees, 90 degrees, 180 degrees, and 270 degrees, or in other words the unit is 1/4 clock source period.

For details, please see Chapter 9 [Reset and Clock](#).

## 49.11 Interrupt

The SD/MMC Host Controller can generate interrupt signal SDIO\_HOST\_INTR triggered by the following interrupt sources, and send the interrupt signals to the [Interrupt Matrix](#).

- SDIO\_INT: Interrupts from SDIO cards
- EBE: Triggered when an error in end bit occurs, or no data CRC received
- ACD: Triggered when an automatically sent command has been executed
- SBE/BCI: Triggered when an error in the start bit occurs
- HLE: Triggered when a write error occurs during hardware-lock period
- FRUN: Triggered when the FIFO is empty or full
- HTO: Triggered when the host does not fill data before timeout period
- DRTO: Triggered when a data read operation times out
- RTO: Triggered when card response times out
- DCRC: Triggered when data CRC error occurs
- RCRC: Triggered when a card response CRC error occurs

- RXDR: Triggered during read operations from card when FIFO level is greater than Receive-Threshold level
- TXDR: Triggered during write operations to card when FIFO level reaches less than or equal to Transmit-Threshold level.
- DTO: Triggered when data transfer completes
- CMDD: Triggered when a command has been executed
- RE: Triggered when response error occurs
- CD: Triggered when a card is detected
- IDSTS\_RI: Triggered when data pointed by a DMA descriptor list have been received
- IDSTS\_TI: Triggered when data pointed by a DMA descriptor list have been transmitted
- IDSTS\_FBE: Triggered when a fatal bus error occurs and the host is stopped during data transmission or reception. When triggered, the DMA disables all bus access.
- IDSTS\_DU: Triggered when a DMA descriptor list is not available because the OWNER bit is 0 (DESO [31] = 0)

The [SDHOST\\_RINTSTS\\_REG](#) and [SDHOST\\_IDSTS\\_REG](#) register contains all the bits that might cause an interrupt. The [SDHOST\\_INTMASK\\_REG](#) and [SDHOST\\_IDINTEN\\_REG](#) register contains an enable bit for each of the events that can cause an interrupt.

There are three interrupt summary bits in the [SDHOST\\_IDSTS\\_REG](#) register: the card error interrupt summary bit (bit 5 [SDHOST\\_IDSTS\\_CES](#)), the normal interrupt summary bit (bit 8 [SDHOST\\_IDSTS\\_NIS](#)), and the abnormal interrupt summary bit (bit 9 [SDHOST\\_IDSTS\\_AIS](#)). Interrupts are cleared by writing 1 to the corresponding bit. When all the enabled interrupts within a group are cleared, the corresponding summary bit is also cleared.

Interrupts are not queued. If another interrupt event occurs before the driver has responded to the previous interrupt, no additional interrupts are generated. For example, the [SDHOST\\_IDSTS\\_RI](#) indicates that one or more data were transferred to the host buffer.

An interrupt is generated only once for simultaneous multiple events. The driver must scan the [SDHOST\\_RINTSTS\\_REG](#) and [SDHOST\\_IDSTS\\_REG](#) register for the interrupt cause.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

## 49.12 Register Summary

The addresses in this section are relative to the SD/MMC Host Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                    | Description                             | Address | Access |
|---|---|---------|--------|
| <b>Configuration registers</b>          |   |         |        |
| <a href="#">SDHOST_CTRL_REG</a>         | Control register                        | 0x0000  | R/W    |
| <a href="#">SDHOST_CLKDIV_REG</a>       | Clock divider configuration             | 0x0008  | R/W    |
| <a href="#">SDHOST_CLKSRC_REG</a>       | Clock source selection                  | 0x000C  | R/W    |
| <a href="#">SDHOST_CLKENA_REG</a>       | Clock enable register                   | 0x0010  | R/W    |
| <a href="#">SDHOST_TMOUT_REG</a>        | Data and response timeout configuration | 0x0014  | R/W    |
| <a href="#">SDHOST_CTYPE_REG</a>        | Card bus width configuration            | 0x0018  | R/W    |
| <a href="#">SDHOST_BLKSIZE_REG</a>      | Card data block size configuration      | 0x001C  | R/W    |
| <a href="#">SDHOST_BYTCNT_REG</a>       | Data transfer length configuration      | 0x0020  | R/W    |
| <a href="#">SDHOST_CMDARG_REG</a>       | Command argument data                   | 0x0028  | R/W    |
| <a href="#">SDHOST_CMD_REG</a>          | Command and boot configuration          | 0x002C  | R/W    |
| <a href="#">SDHOST_FIFOTH_REG</a>       | FIFO configuration                      | 0x004C  | R/W    |
| <a href="#">SDHOST_DEBNCE_REG</a>       | Debounce filter time configuration      | 0x0064  | R/W    |
| <a href="#">SDHOST_USRID_REG</a>        | User ID (scratchpad)                    | 0x0068  | R/W    |
| <a href="#">SDHOST_UHS_REG</a>          | UHS-1                                   | 0x0074  | R/W    |
| <a href="#">SDHOST_RST_N_REG</a>        | Card reset                              | 0x0078  | R/W    |
| <a href="#">SDHOST_BMOD_REG</a>         | Burst mode transfer configuration       | 0x0080  | R/W    |
| <a href="#">SDHOST_PLDMND_REG</a>       | Poll demand configuration               | 0x0084  | WO     |
| <a href="#">SDHOST_DBADDR_REG</a>       | Linked-list base address                | 0x0088  | R/W    |
| <a href="#">SDHOST_CARDTHRCTL_REG</a>   | Card Threshold Control                  | 0x0100  | R/W    |
| <a href="#">SDHOST_EMMCDDR_REG</a>      | eMMC DDR register                       | 0x010C  | R/W    |
| <a href="#">SDHOST_ENSHIFT_REG</a>      | Enable Phase Shift                      | 0x0110  | R/W    |
| <a href="#">SDHOST_CLK_EDGE_SEL_REG</a> | SDIO control register                   | 0x0800  | R/W    |
| <a href="#">SDHOST_DLL_CLK_CONF_REG</a> | SDIO DLL clock control                  | 0x0808  | R/W    |
| <b>Interrupt registers</b>              |   |         |        |
| <a href="#">SDHOST_INTMASK_REG</a>      | SDIO interrupt mask register            | 0x0024  | R/W    |
| <a href="#">SDHOST_MINTSTS_REG</a>      | Masked interrupt status register        | 0x0040  | RO     |
| <a href="#">SDHOST_RINTSTS_REG</a>      | Raw interrupt register                  | 0x0044  | R/W1C  |
| <a href="#">SDHOST_IDSTS_REG</a>        | DMA interrupt register                  | 0x008C  | R/W1C  |
| <a href="#">SDHOST_IDINTEN_REG</a>      | DMA interrupt enable register           | 0x0090  | R/W    |
| <b>Status registers</b>                 |   |         |        |
| <a href="#">SDHOST_RESPO_REG</a>        | Response data                           | 0x0030  | RO     |
| <a href="#">SDHOST_RESP1_REG</a>        | Long response data                      | 0x0034  | RO     |
| <a href="#">SDHOST_RESP2_REG</a>        | Long response data                      | 0x0038  | RO     |
| <a href="#">SDHOST_RESP3_REG</a>        | Long response data                      | 0x003C  | RO     |
| <a href="#">SDHOST_STATUS_REG</a>       | SD/MMC status                           | 0x0048  | RO     |
| <a href="#">SDHOST_CDETECT_REG</a>      | Card detect                             | 0x0050  | RO     |

| Name                                       | Description                                   | Address | Access |
|--|---|---------|--------|
| <a href="#">SDHOST_WRTprt_REG</a>          | Card write protection (WP) status             | 0x0054  | RO     |
| <a href="#">SDHOST_TCBCNT_REG</a>          | Transferred byte count                        | 0x005C  | RO     |
| <a href="#">SDHOST_TBBCNT_REG</a>          | Transferred byte count                        | 0x0060  | RO     |
| <a href="#">SDHOST_DSCADDR_REG</a>         | Host descriptor address pointer               | 0x0094  | RO     |
| <a href="#">SDHOST_BUFADDR_REG</a>         | Host buffer address pointer                   | 0x0098  | RO     |
| <b>Transmit and receive data registers</b> |   |         |        |
| <a href="#">SDHOST_BUFFIFO_REG</a>         | Software write and read transmit data by FIFO | 0x0200  | R/W    |

## 49.13 Registers

The addresses in this section are relative to the SD/MMC Host Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 49.1. SDHOST\_CTRL\_REG (0x0000)**

|            |   |   |   |   |   |                          |    |    |   |   |   |   |   |   |   |            |    |    |   |   |   |  |   |   |   |   |   |   |       |  |  |
|------------|---|---|---|---|---|--------------------------|----|----|---|---|---|---|---|---|---|------------|----|----|---|---|---|--|---|---|---|---|---|---|-------|--|--|
| (reserved) |   |   |   |   |   | SDHOST_USE_INTERNAL_DMAC |    |    |   |   |   |   |   |   |   | (reserved) |    |    |   |   |   | SDHOST_CEATA_DEVICE_INTERRUPT_STATUS<br>SDHOST_SEND_AUTO_STOP_CCSD<br>SDHOST_SEND_ABORT_READ_DATA<br>SDHOST_SEND_IRQ_RESPONSE<br>(reserved)<br>(reserved)<br>SDHOST_INT_ENABLE<br>SDHOST_DMA_RESET<br>SDHOST_FIFO_RESET<br>SDHOST_CONTROLLER_RESET |   |   |   |   |   |   |       |  |  |
| 31         |   |   |   |   |   | 26                       | 25 | 24 |   |   |   |   |   |   |   | 12         | 11 | 10 | 9 | 8 | 7 | 6  | 5 | 4 | 3 | 2 | 1 | 0 | Reset |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0                        | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0  | 0  | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 |   |       |  |  |

**SDHOST\_CONTROLLER\_RESET** Configures whether to reset the controller. This bit is auto-cleared after controller reset.

0: No effect

1: Reset

(R/W)

**SDHOST\_FIFO\_RESET** Configures whether to reset FIFO. This bit is auto-cleared after FIFO reset.

0: No effect

1: Reset

(R/W)

**SDHOST\_DMA\_RESET** Configures whether to reset DMA interface. This bit is auto-cleared after DMA reset.

0: No effect

1: Reset

(R/W)

**SDHOST\_INT\_ENABLE** Write 1 to enable global interrupt port. (R/W)

**SDHOST\_READ\_WAIT** Configures whether to send read-wait to SDIO cards.

0: Clear read wait

1: Assert read wait

(R/W)

Continued on the next page...

**Register 49.1. CTRL\_REG (0x0000)**

Continued from the previous page...

**SDHOST\_SEND\_IRQ\_RESPONSE** Configures whether to send auto interrupt request (IRQ) response.

This bit automatically clears once a response is sent.

To wait for MMC card interrupts, the host issues a CMD40 command and waits for an interrupt response from MMC card(s). In the meantime, if the host wants SD/MMC to exit waiting for the interrupt state, it can set this bit, at which time SD/MMC command state-machine sends a CMD40 response on the bus and returns to the idle state.

0: No effect

1: Send auto IRQ response

(R/W)

**SDHOST\_ABORT\_READ\_DATA** Configures whether to abort read data. This bit is automatically cleared once the data state machine is reset to idle.

After a suspend-command is issued during a read-operation, software polls the card to find when the suspend-event occurred. Once the suspend-event has occurred, software sets the bit which will reset the data state machine that is waiting for the next block of data.

0: No effect

1: Abort read data

(R/W)

**SDHOST\_SEND\_CCSD** Configures whether to send Command Completion Signal Disable (CCSD) to CE-ATA device. Once the CCSD pattern is sent to the device, SD/MMC automatically clears the SDHOST\_SEND\_CCSD bit. It also sets the Command Done (CD) bit in the SDHOST\_RINTSTS\_REG register.

Software sets this bit only if the current command is expecting CCS (that is, RW\_BLK), and if interrupts are enabled for the CE-ATA device.

0: No effect

1: Send CCSD to CE-ATA device

(R/W)

**SDHOST\_SEND\_AUTO\_STOP\_CCSD** Configures whether to send an internally-generated STOP command (CMD12) to the CE-ATA device. After sending the CCSD, SD/MMC automatically clears the SDHOST\_SEND\_AUTO\_STOP\_CCSD bit. After sending this internally-generated STOP command, the Auto Command Done (ACD) bit in SDHOST\_RINTSTS\_REG is set.

Always Set SDHOST\_SEND\_AUTO\_STOP\_CCSD and SDHOST\_SEND\_CCSD bits together, SDHOST\_SEND\_AUTO\_STOP\_CCSD should not be set independently of SDHOST\_SEND\_CCSD.

0: No effect

1: Send internally-generated STOP command (CMD12) to the CE-ATA device

(R/W)

Continued on the next page...

**Register 49.1. CTRL\_REG (0x0000)**

Continued from the previous page...

**SDHOST\_CEATA\_DEVICE\_INTERRUPT\_STATUS** Write 1 to enable interrupts in CE-ATA device (nIEN = 0 in ATE control register).

Software should appropriately write to this bit after the power-on reset or any other reset to the CE-ATA device. After reset, the CE-ATA device's interrupt is usually disabled (nIEN = 1). If the host enables the CE-ATA device's interrupt, then software should set this bit. (R/W)

**SDHOST\_USE\_INTERNAL\_DMACH** Configures whether to use DMA for data transfer.

0: Not use

1: Use

(R/W)

**Register 49.2. SDHOST\_CLKDIV\_REG (0x0008)**

|                     |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|---------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| SDHOST_CLK_DIVIDER3 |  |  |  |  |  |  |  | SDHOST_CLK_DIVIDER2 |  |  |  |  |  |  |  | SDHOST_CLK_DIVIDER1 |  |  |  |  |  |  |  | SDHOST_CLK_DIVIDER0 |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31                  |  |  |  |  |  |  |  | 24                  |  |  |  |  |  |  |  | 23                  |  |  |  |  |  |  |  | 16                  |  |  |  |  |  |  |  | 15    |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0x0                 |  |  |  |  |  |  |  | 0x0                 |  |  |  |  |  |  |  | 0x0                 |  |  |  |  |  |  |  | 0x0                 |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**SDHOST\_CLK\_DIVIDER0** Configures clock divider0 value. Clock divisor is  $2^n$ , where  $n = 0$  bypasses the divider (divisor of 1). For example, a value of 1 means divided by  $2^1 = 2$ , a value of 0xFF means divided by  $2^{255} = 510$ , and so on. (R/W)

**SDHOST\_CLK\_DIVIDER1** Configures clock divider1 value. Clock divisor is  $2^n$ , where  $n = 0$  bypasses the divider (divisor of 1). For example, a value of 1 means divided by  $2^1 = 2$ , a value of 0xFF means divided by  $2^{255} = 510$ , and so on. (R/W)

**SDHOST\_CLK\_DIVIDER2** Configures clock divider2 value. Clock divisor is  $2^n$ , where  $n = 0$  bypasses the divider (divisor of 1). For example, a value of 1 means divided by  $2^1 = 2$ , a value of 0xFF means divided by  $2^{255} = 510$ , and so on. (R/W)

**SDHOST\_CLK\_DIVIDER3** Configures clock divider3 value. Clock divisor is  $2^n$ , where  $n = 0$  bypasses the divider (divisor of 1). For example, a value of 1 means divided by  $2^1 = 2$ , a value of 0xFF means divided by  $2^{255} = 510$ , and so on. (R/W)



### Register 49.3. SDHOST\_CLKSRC\_REG (0x000C)

Diagram illustrating the SDHOST\_CLKSRC\_REG register structure. The register is 32 bits wide, divided into three fields:

- Reserved:** 28 bits (bits 31-4), labeled "(reserved)".
- SDHOST\_CLKSRC:** 4 bits (bits 3-0), labeled "SDHOST\_CLKSRC\_REG".
- Reset:** 4 bits (bits 3-0), labeled "Reset", with a value of 0x0.

**SDHOST\_CLKSRC\_REG** Configures clock divider source for two SD cards. Each card has two bits assigned to it. For example, bit[1:0] are assigned to card 0, and bit[3:2] are assigned to card 1. Card 1/0 maps and internally routes clock divider[0:3] outputs to cclk\_out[1:0] pins, depending on bit value. For every card's clock divider source:

0x0: Clock divider 0

0x1: Clock divider 1

0x2: Clock divider 2

0x3: Clock divider 3

(R/W)

#### Register 49.4. SDHOST\_CLKENA\_REG (0x0010)

[illegible]

**SDHOST\_CCLK\_ENABLE** Configures whether to enable two SD card clocks or one MMC card clock.

One bit per card. For every card's bit:

0: Clock disabled

1: Clock enabled

(R/W)

**SDHOST\_LP\_ENABLE** Configures whether to disable the clock when the card is in an IDLE state.

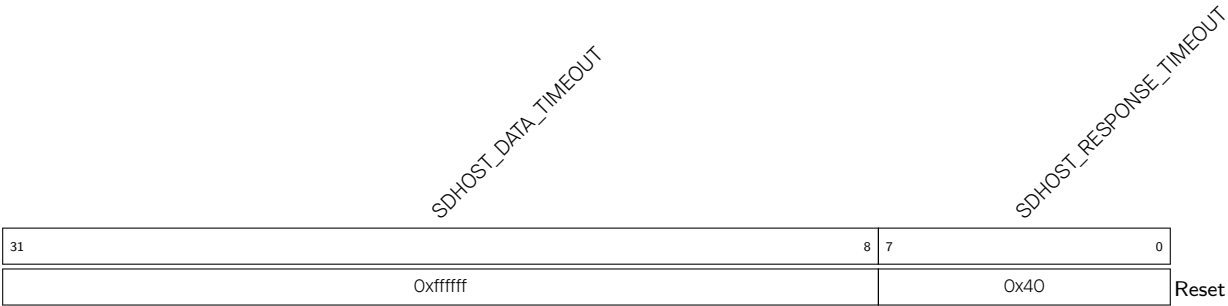
One bit per card. For every card's bit:

0: Clock disabled

1: Clock enabled

(R/W)

Register 49.5. SDHOST\_TMOUT\_REG (0x0014)

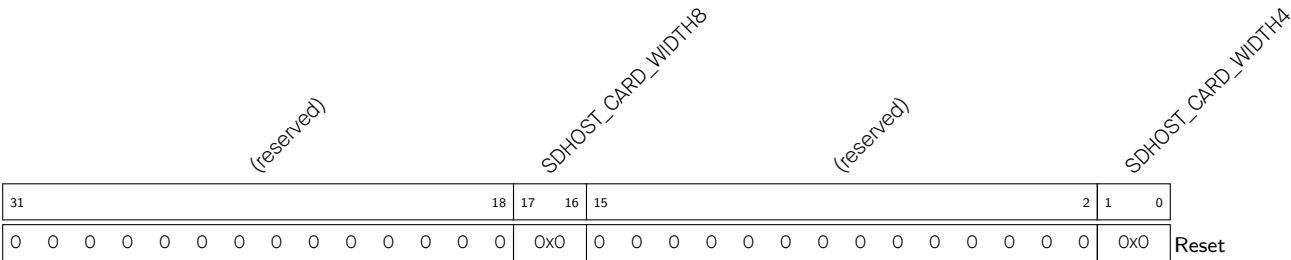


**SDHOST\_RESPONSE\_TIMEOUT** Configures response timeout value. Measurement unit: Card output clock period. (R/W)

**SDHOST\_DATA\_TIMEOUT** Configures card data read timeout value. This value is also used for data starvation by host timeout. The timeout counter is started only after the card clock is stopped. Measurement unit: Card output clock period.

NOTE: The software timer should be used if the timeout value is in the order of 100 ms. In this case, read data timeout interrupt (DRT0) needs to be disabled.  
(R/W)

Register 49.6. SDHOST\_CTYPE\_REG (0x0018)



**SDHOST\_CARD\_WIDTH4** Configures whether the card is 1-bit or 4-bit mode. One bit per card. Bit[0] corresponds to card[0]. For every card's bit:

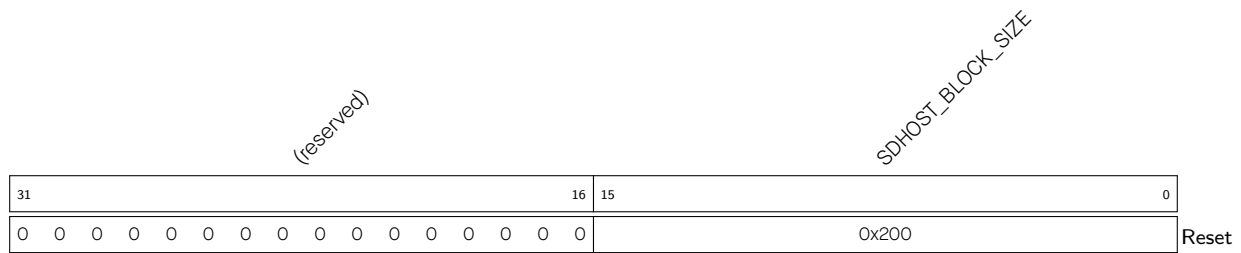
- 0: 1-bit mode
- 1: 4-bit mode

(R/W)

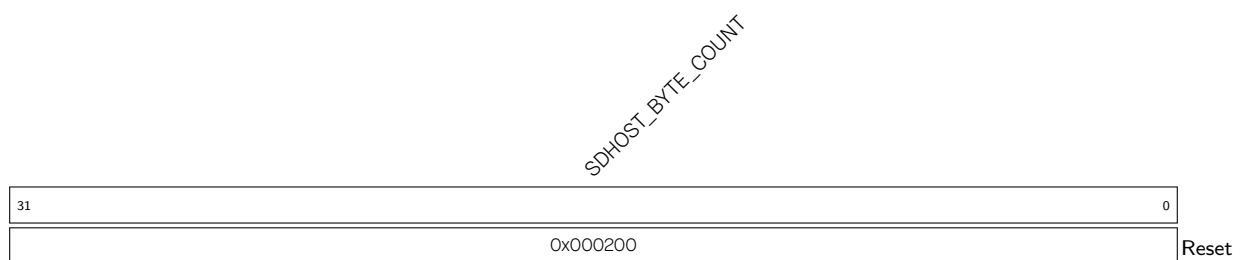
**SDHOST\_CARD\_WIDTH8** Configures whether the card is 8-bit mode. One bit per card. Bit[0] corresponds to card[0]. For every card's bit:

- 0: Non 8-bit mode
- 1: 8-bit mode

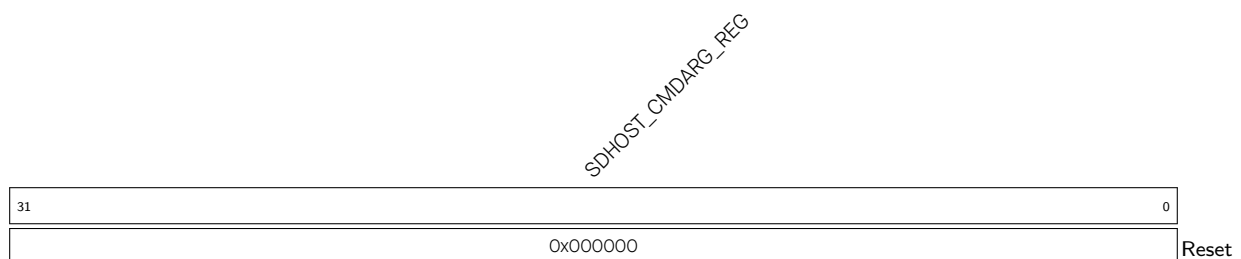
(R/W)

**Register 49.7. SDHOST\_BLKSIZE\_REG (0x001C)**

**SDHOST\_BLOCK\_SIZE** Configures the Block Size. (R/W)

**Register 49.8. SDHOST\_BYTCNT\_REG (0x0020)**

**SDHOST\_BYTE\_COUNT** Configures the number of bytes to be transferred, should be an integral multiple of Block Size for block transfers. For data transfers of undefined byte lengths, the byte count should be set to 0. When the byte count is set to 0, it is the responsibility of the host to explicitly send a stop/abort command to terminate data transfer. (R/W)

**Register 49.9. SDHOST\_CMDARG\_REG (0x0028)**

**SDHOST\_CMDARG\_REG** Configures the value indicates the command argument to be passed to the card. (R/W)

**Register 49.10. SDHOST\_CMD\_REG (0x002C)**

|                                |    |    |    |   |    |   |    |   |    |    |     |                    |    |    |    |   |    |    |   |                  |   |   |     |   |       |
|--------------------------------|----|----|----|---|----|---|----|---|----|----|-----|--------------------|----|----|----|---|----|----|---|------------------|---|---|-----|---|-------|
| SDHOST_START_CMD<br>(reserved) |    |    |    | SDHOST_USE_HOLE_REG<br>SDHOST_VOLT_SWITCH<br>(reserved) |    |   |    | SDHOST_CCS_EXPECTED<br>SDHOST_READ_CEATA_DEVICE<br>SDHOST_UPDATE_CLOCK_REGISTERS_ONLY |    |    |     | SDHOST_CARD_NUMBER |    |    |    | SDHOST_SEND_INITIALIZATION<br>SDHOST_STOP_ABORT_CMD<br>SDHOST_WAIT_PRIVDATA_COMPLETE<br>SDHOST_SEND_AUTO_STOP<br>SDHOST_TRANSFER_MODE<br>SDHOST_READ_WRITE<br>SDHOST_DATA_EXPECTED<br>SDHOST_CHECK_RESPONSE CRC<br>SDHOST_RESPONSE_LENGTH<br>SDHOST_RESPONSE_EXPECT |    |    |   | SDHOST_CMD_INDEX |   |   |     |   |       |
| 31                             | 30 | 29 | 28 | 27  | 24 |   | 23 | 22  | 21 | 20 | 16  |                    | 15 | 14 | 13 | 12  | 11 | 10 | 9 | 8                | 7 | 6 | 5   | 0 |       |
| 0                              | 0  | 1  | 0  | 0   | 0  | 0 | 0  | 0   | 0  | 0  | 0x0 |                    | 0  | 0  | 0  | 0   | 0  | 0  | 0 | 0                | 0 | 0 | 0x0 |   | Reset |

**SDHOST\_CMD\_INDEX** Configures the Command index send to card. (R/W)

**SDHOST\_RESPONSE\_EXPECT** Configures whether to expect response from card.

0: No response expected from card

1: Response expected from card

(R/W)

**SDHOST\_RESPONSE\_LENGTH** Configures response length from card.

0: Short response expected from card

1: Long response expected from card

(R/W)

**SDHOST\_CHECK\_RESPONSE\_CRC** Configures whether to check response CRC.

0: Do not check

1: Check response CRC

(R/W)

**SDHOST\_DATA\_EXPECTED** Configures whether to expect data transfer.

0: No data transfer expected

1: Data transfer expected

(R/W)

**SDHOST\_READ\_WRITE** Configures data transfer direction.

0: Read from card

1: Write to card

(R/W)

**SDHOST\_TRANSFER\_MODE** Configures data transfer mode.

0: Block data transfer command

1: Stream data transfer command

(R/W)

**SDHOST\_SEND\_AUTO\_STOP** Configures whether to automatically send stop command.

0: No stop command is sent at the end of data transfer

1: Send stop command at the end of data transfer

(R/W)

Continued on the next page...

**Register 49.10. SDHOST\_CMD\_REG (0x002C)**

Continued from the previous page...

**SDHOST\_WAIT\_PRVDATA\_COMPLETE** Configures whether to send command at once.

0: Send command at once, even if previous data transfer has not completed

1: Wait for previous data transfer to complete before sending Command

(R/W)

**SDHOST\_STOP\_ABORT\_CMD** Configures whether the stop/abort command stops data transfer.

0: Neither stop nor abort command can stop the current data transfer. If abort is sent to the card device currently selected, or the card device is not in data-transfer mode, then bit should be set to 0

1: Stop or abort command intended to stop current data transfer in progress

(R/W)

**SDHOST\_SEND\_INITIALIZATION** Configures whether to send initialization sequence (80 clocks of 1) before sending this command. After powered on, 80 clocks must be sent to card for initialization before sending any commands to card. Bit should be set while sending the first command to card so that the controller will initialize clocks before sending command to card.

0: Do not send initialization sequence before sending this command

1: Send initialization sequence before sending this command

(R/W)

**SDHOST\_CARD\_NUMBER** Configures card number in use, the physical slot number of the card being accessed. In SD-only mode, up to two cards are supported. (R/W)

**SDHOST\_UPDATE\_CLOCK\_REGISTERS\_ONLY** Configures whether to only update clock register value into card clock domain.

Following register values are transferred into card clock domain: SDHOST\_CLKDIV\_REG, SDHOST\_CLRSRC\_REG, and SDHOST\_CLKENA\_REG.

When this bit is set, there will be no Command Done interrupts because no command is sent to SD\_MMC\_CEATA cards.

0: Normal command sequence

1: Do not send commands, just update clock register value into card clock domain

(R/W)

**SDHOST\_READ\_CEATA\_DEVICE** Configures whether to read access CE-ATA device.

This bit is used to disable read data timeout indication while performing CE-ATA read transfers.

0: Host is not performing read access (RW\_REG or RW\_BLK) towards CE-ATA device

1: Host is performing read access (RW\_REG or RW\_BLK) towards CE-ATA device

(R/W)

Continued on the next page...

**Register 49.10. SDHOST\_CMD\_REG (0x002C)**

Continued from the previous page...

**SDHOST\_CCS\_EXPECTED** Configures whether to expect Command Completion Signal (CCS).

0: Interrupts are not enabled in CE-ATA device (nIEN = 1 in ATA control register), or command does not expect CCS from CE-ATA device

1: Interrupts are enabled in CE-ATA device (nIEN = 0), and RW\_BLK command expects CCS from CE-ATA device

(R/W)

**SDHOST\_VOLT\_SWITCH** Configures whether to enable voltage switching.

0: No voltage switching

1: Voltage switching enabled, must be set for CMD11 only

(R/W)

**SDHOST\_USE\_HOLE\_REG** Configures whether to use Hold Register.

0: CMD and DATA sent to card bypassing HOLD Register

1: CMD and DATA sent to card through the HOLD Register

(R/W)

**SDHOST\_START\_CMD** Configures whether to start the command.

0: Not start

1: Start

Once command is served by the CIU, this bit is automatically cleared.

When this bit is set, host should not attempt to write to any command registers. If a write is attempted, hardware lock error is set in raw interrupt register. (R/W/SC)

**Register 49.11. SDHOST\_FIFOTH\_REG (0x004C)**

|            |     |    |    |                                      |     |  |    |            |   |    |    |                 |  |  |  |            |  |  |  |                 |  |  |       |
|------------|-----|----|----|--------------------------------------|-----|--|----|------------|---|----|----|-----------------|--|--|--|------------|--|--|--|-----------------|--|--|-------|
| (reserved) |     |    |    | SDHOST_DMA_MULTIPLE_TRANSACTION_SIZE |     |  |    | (reserved) |   |    |    | SDHOST_RX_WMARK |  |  |  | (reserved) |  |  |  | SDHOST_TX_WMARK |  |  |       |
| 31         | 30  | 28 | 27 | 26                                   |     |  | 16 | 15         |   | 12 | 11 |                 |  |  |  |            |  |  |  |                 |  |  | 0     |
| 0          | 0x0 | 0  |    |                                      | 0x0 |  |    | 0          | 0 | 0  | 0  |                 |  |  |  | 0x0        |  |  |  |                 |  |  | Reset |

**SDHOST\_TX\_WMARK** Configures FIFO threshold watermark level when transmitting data to card.

When FIFO data count is less than or equal to this number, DMA/FIFO request is raised. During end of packet, request or interrupt is generated, regardless of threshold programming.

In non-DMA mode, when transmitting FIFO threshold (TXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, on last interrupt, host is responsible for filling FIFO with only the required remaining bytes (not before FIFO is full or after CIU completes data transfers, because FIFO may not be empty).

In DMA mode, at end of packet, if last transfer is less than burst size, DMA controller does single cycles until required bytes are transferred. (R/W)

**SDHOST\_RX\_WMARK** Configures FIFO threshold watermark level when receiving data from card.

When FIFO data count reaches greater than this number, DMA/FIFO request is raised. During end of packet, request is generated regardless of threshold programming in order to complete any remaining data.

In non-DMA mode, when receiver FIFO threshold (RXDR) interrupt is enabled, then interrupt is generated instead of DMA request. During end of packet, interrupt is not generated if threshold programming is larger than any remaining data. It is responsibility of host to read remaining bytes on seeing Data Transfer Done interrupt.

In DMA mode, at end of packet, even if remaining bytes are less than threshold, DMA request does single transfers to flush out any remaining bytes before Data Transfer Done interrupt is set. (R/W)

**SDHOST\_DMA\_MULTIPLE\_TRANSACTION\_SIZE** Configures burst size of multiple transaction, should be programmed same as DMA controller multiple-transaction-size SDHOST\_SRC/DEST\_MSIZ.

0x0: 1-byte transfer

0x1: 4-byte transfer

0x2: 8-byte transfer

0x3: 16-byte transfer

0x4: 32-byte transfer

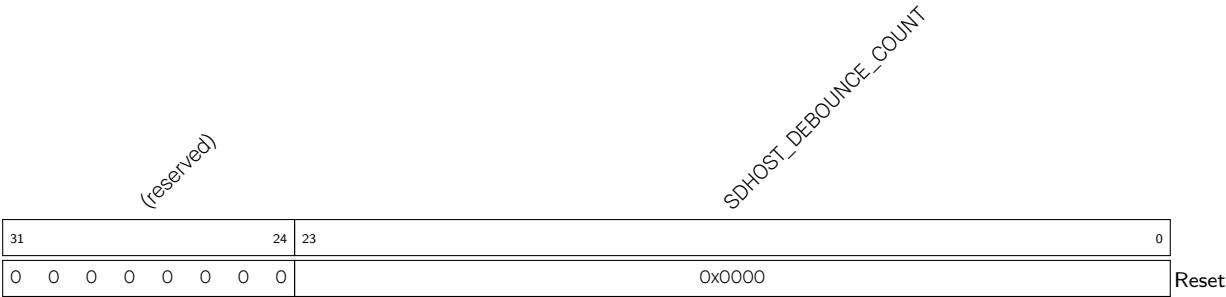
0x5: 64-byte transfer

0x6: 128-byte transfer

0x7: 256-byte transfer

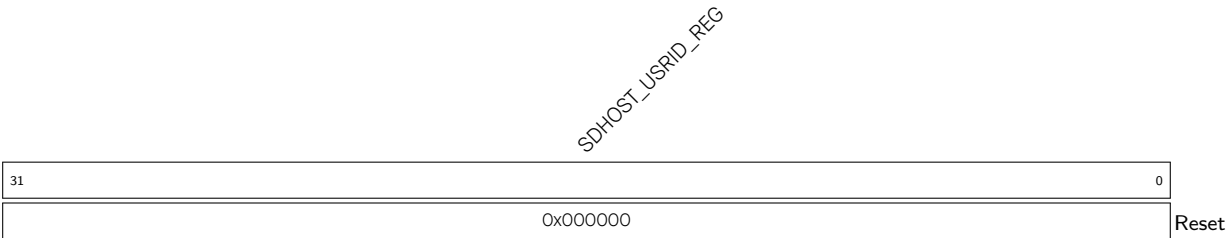
(R/W)

Register 49.12. SDHOST\_DEBNCE\_REG (0x0064)



**SDHOST\_DEBOUNCE\_COUNT** Configures the number of host clocks (clk) used by debounce filter logic. The typical debounce time is 5 ~ 25 ms to prevent the card instability when the card is inserted or removed. (R/W)

Register 49.13. SDHOST\_USRID\_REG (0x0068)



**SDHOST\_USRID\_REG** Configures user identification, value set by users. Can also be used as a scratchpad register by users. (R/W)



**Register 49.14. SDHOST\_UHS\_REG (0x0074)**

|                             |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |                                 |    |    |  |  |  |  |  |  |  |  |  |  |  |  |                 |  |   |       |  |   |   |
|-----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|---------------------------------|----|----|--|--|--|--|--|--|--|--|--|--|--|--|-----------------|--|---|-------|--|---|---|
| (reserved)                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SDHOST_DDR_REG |  |  | (reserved)                      |    |    |  |  |  |  |  |  |  |  |  |  |  |  | SDHOST_VOLT_REG |  |   |       |  |   |   |
| 31                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 18             |  |  | 17                              | 16 | 15 |  |  |  |  |  |  |  |  |  |  |  |  |                 |  | 2 |       |  | 1 | 0 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0            |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |    |  |  |  |  |  |  |  |  |  |  |  |  | 0x0             |  |   | Reset |  |   |   |

**SDHOST\_VOLT\_REG** Configures High Voltage mode per card. Bit[0] corresponds to card[0]. For every card bit:

0: 3.3 V VDD

1: 1.8 V VDD

(R/W)

**SDHOST\_DDR\_REG** Configures DDR (double data rate) mode selecton per card. Bit[0] corresponds to card[0]. For every card bit:

0: Non-DDR mdoe

1: DDR mdoe

(R/W)

**Register 49.15. SDHOST\_RST\_N\_REG (0x0078)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|---|---|-------|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SDHOST_CARD_RESET |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2                 | 1 | 0 |       |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x1               |   |   | Reset |

**SDHOST\_CARD\_RESET** Configures hardware reset per card. Bit[0] corresponds to card[0]. These bits cause the cards to enter the pre-idle state, which requires them to be re-initialized. For every card bit:

0: Reset

1: Active mode

(R/W)

**Register 49.16. SDHOST\_BMOD\_REG (0x0080)**

|            |   |   |   |   |   |   |   |   |   |    |                 |   |                |   |            |   |                |   |                 |   |
|------------|---|---|---|---|---|---|---|---|---|----|-----------------|---|----------------|---|------------|---|----------------|---|-----------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |    | SDHOST_BMOD_PBL |   | SDHOST_BMOD_DE |   | (reserved) |   | SDHOST_BMOD_FB |   | SDHOST_BMOD_SWR |   |
| 31         |   |   |   |   |   |   |   |   |   | 11 | 10              | 8 | 7              | 6 |            | 2 | 1              | 0 |                 |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0               | 0 | 0              | 0 | 0          | 0 | 0              | 0 | 0               | 0 |
|            |   |   |   |   |   |   |   |   |   |    | 0x0             |   | 0              | 0 | 0          | 0 | 0              | 0 | 0               | 0 |
|            |   |   |   |   |   |   |   |   |   |    |                 |   |                |   |            |   |                |   | Reset           |   |

**SDHOST\_BMOD\_SWR** Configures whether to reset all DMA internal registers. It is automatically cleared after one clock cycle.

0: No effect

1: Reset

(R/W)

**SDHOST\_BMOD\_FB** Configures whether the AHB Master interface performs fixed burst transfers.

0: Use SINGLE and INCR burst transfer operations

1: Only use SINGLE, INCR4, INCR8 or INCR16 burst transfers

(R/W)

**SDHOST\_BMOD\_DE** Configures whether to enable the DMA.

0: Not enable

1: Enable

(R/W)

**SDHOST\_BMOD\_PBL** Configures the maximum number of beats to be performed in one DMA transaction.

0x0: 1-beat transfer

0x1: 4-beat transfer

0x2: 8-beat transfer

0x3: 16-beat transfer

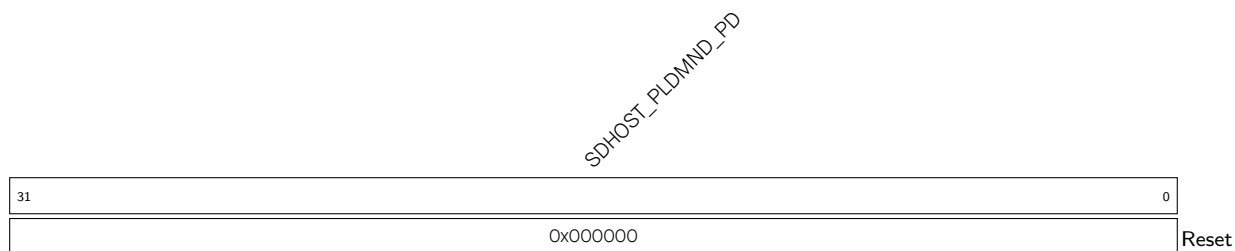
0x4: 32-beat transfer

0x5: 64-beat transfer

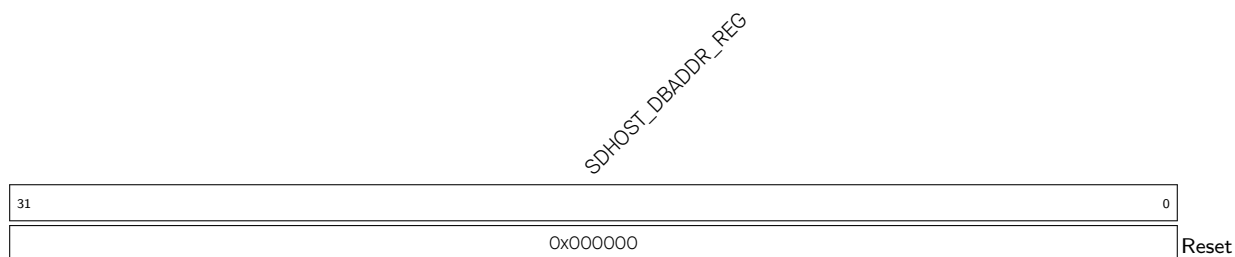
0x6: 128-beat transfer

0x7: 256-beat transfer

(R/W)

**Register 49.17. SDHOST\_PLDMND\_REG (0x0084)**

**SDHOST\_PLDMND\_PD** Configures the DMA FSM to resume normal descriptor fetch operation. If the OWNER bit of a descriptor is not set, the FSM goes to the Suspend state, software needs to write any value into this field for the FSM to resume normal descriptor fetch operation. (WO)

**Register 49.18. SDHOST\_DBADDR\_REG (0x0088)**

**SDHOST\_DBADDR\_REG** Configures the base address of the linked list (First Descriptor). Bit[1:0] are ignored and taken as all-zero by the DMA internally. (R/W)

### Register 49.19. SDHOST\_CARDTHRCTL\_REG (0x0100)

|                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|
| SDHOST_CARDTHRESHOLD_REG |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | SDHOST_CARDCLRINTEN_REG<br>SDHOST_CARDRDTHREN_REG |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
| 31                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 | 0 |
| 0x00                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |

**SDHOST\_CARDRDTHREN\_REG** Configures whether to enable card read threshold.

0: Not enable

1: Enable

(R/W)

**SDHOST\_CARDCLRINTEN\_REG** Configures whether to enable busy clear interrupt generation.

0: Not enable

1: Enable

(R/W)

**SDHOST\_CARDTHRESHOLD\_REG** Configures the card read threshold. Measurement unit: byte.

This field is valid only when SDHOST\_CARDRDTHREN\_REG is set to 1.

The value should be less than the FIFO size 512.(R/W)

### Register 49.20. SDHOST\_EMMCDDR\_REG (0x010C)

Diagram illustrating the structure of the `SDHOST_HALFSTARTBIT_REG` register. The register is 32 bits wide, divided into two main sections:

- Reserved Bits (31-1):** A large section labeled `(reserved)` occupies bits 31 down to bit 1.
- SDHOST\_HALFSTARTBIT\_REG (0):** A single bit field at bit 0, labeled `SDHOST_HALFSTARTBIT_REG`.

The bottom right corner shows the value `0x0` and the label `Reset`.

**SDHOST\_HALFSTARTBIT\_REG** Configures the start bit detection mechanism duration of start bit.

Each bit refers to one card. Set this bit to 1 for eMMC4.5 and above, set to 0 for SD applications.

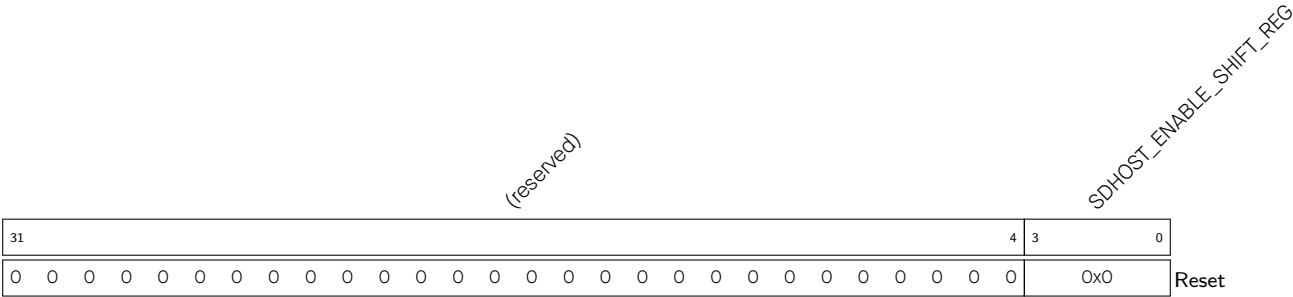
For eMMC4.5, start bit can be:

0: Full cycle

1: Less than one full cycle

(R/W)

Register 49.21. SDHOST\_ENSHIFT\_REG (0x0110)

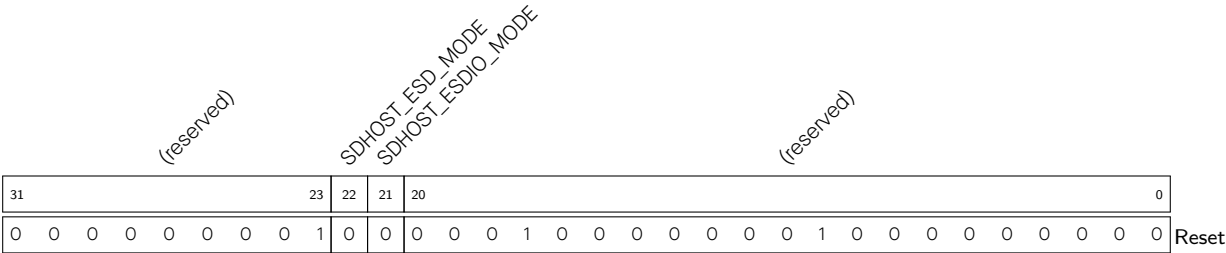


**SDHOST\_ENABLE\_SHIFT\_REG** Configures the amount of phase shift provided on the default enables in the design. Two bits are assigned for each card, e.g., bit[1:0] are assigned to card 0. For every card:

- 0x0: Default phase shift
- 0x1: Enables shifted to next immediate positive edge
- 0x2: Enables shifted to next immediate negative edge
- 0x3: Reserved

(R/W)

Register 49.22. SDHOST\_CLK\_EDGE\_SEL\_REG (0x0800)



**SDHOST\_ESDIO\_MODE** Configures whether to enable eSDIO mode.

- 0: Not enable
- 1: Enable

(R/W)

**SDHOST\_ESD\_MODE** Configures whether to enable eSD mode.

- 0: Not enable
- 1: Enable

(R/W)

### Register 49.23. SDHOST\_DLL\_CLK\_CONF\_REG (0x0808)

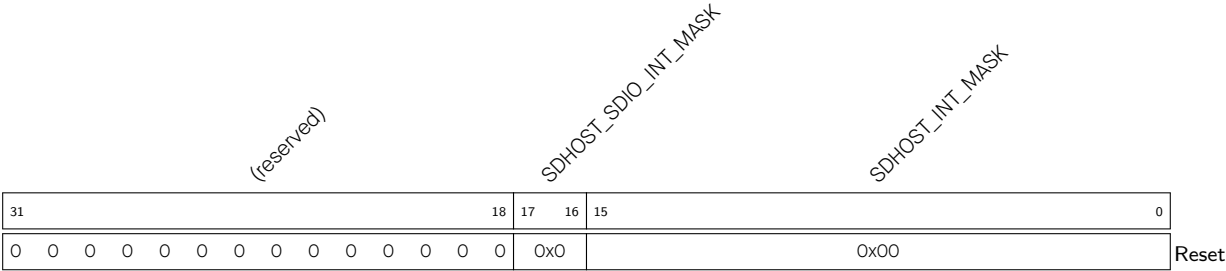
|                     |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |    |  |  |  |  |                              |  |  |  |  |       |  |  |  |  |            |  |  |  |  |   |  |  |  |  |   |  |   |  |  |
|---------------------|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|----|--|--|--|--|------------------------------|--|--|--|--|-------|--|--|--|--|------------|--|--|--|--|---|--|--|--|--|---|--|---|--|--|
| (reserved)          |  |  |  |  |  |  |  |  |  | SDHOST_DLL_CCLK_IN_SAM_PHASE |  |  |  |  |  |  |  |  |  | SDHOST_DLL_CCLK_IN_DRV_PHASE |  |  |  |  |    |  |  |  |  | SDHOST_DLL_CCLK_IN_SLF_PHASE |  |  |  |  |       |  |  |  |  | (reserved) |  |  |  |  |   |  |  |  |  |   |  |   |  |  |
| 31                  |  |  |  |  |  |  |  |  |  | 21                           |  |  |  |  |  |  |  |  |  | 20                           |  |  |  |  | 15 |  |  |  |  | 14                           |  |  |  |  | 9     |  |  |  |  | 8          |  |  |  |  | 3 |  |  |  |  | 2 |  | 0 |  |  |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  | 0                            |  |  |  |  |  |  |  |  |  | 0                            |  |  |  |  | 0  |  |  |  |  | 0                            |  |  |  |  | 0 0 0 |  |  |  |  | Reset      |  |  |  |  |   |  |  |  |  |   |  |   |  |  |

**SDHOST\_DLL\_CCLK\_IN\_SLF\_PHASE** Configures the clock phase of the internal signal when selecting high frequency clock. Unit is 1/64 of clock cycle. (R/W)

**SDHOST\_DLL\_CCLK\_IN\_DRV\_PHASE** Configures the clock phase of the output signal when selecting high frequency clock. Unit is 1/64 of clock cycle. (R/W)

**SDHOST\_DLL\_CCLK\_IN\_SAM\_PHASE** Configures the clock phase of the input signal when selecting high frequency clock. Unit is 1/64 of clock cycle. (R/W)

Register 49.24. SDHOST\_INTMASK\_REG (0x0024)

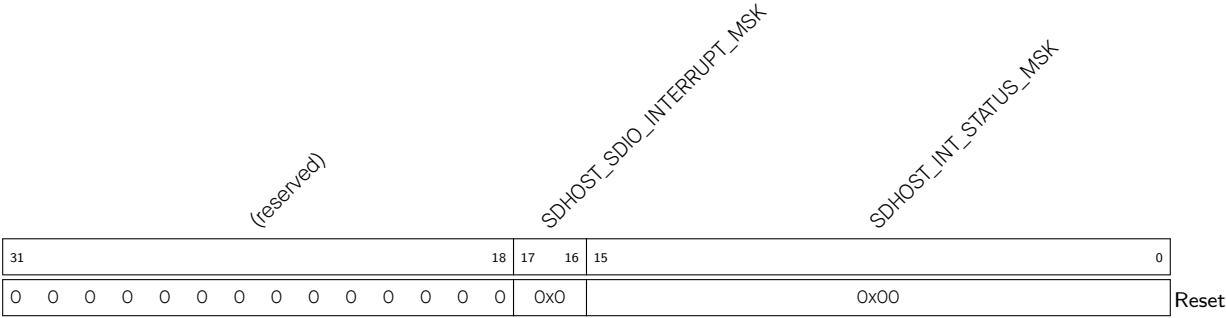


**SDHOST\_INT\_MASK** Write 1 to correspond bit to enable correspond interrupt. For every bit:

- Bit 15 (EBE): End-bit error/no CRC error
  - Bit 14 (ACD): Auto command done
  - Bit 13 (SBE/BCI): Rx Start Bit Error
  - Bit 12 (HLE): Hardware locked write error
  - Bit 11 (FRUN): FIFO underrun/overflow error
  - Bit 10 (HTO): Data starvation-by-host timeout
  - Bit 9 (DRT0): Data read timeout
  - Bit 8 (RTO): Response timeout
  - Bit 7 (DCRC): Data CRC error
  - Bit 6 (RCRC): Response CRC error
  - Bit 5 (RXDR): Receive FIFO data request
  - Bit 4 (TXDR): Transmit FIFO data request
  - Bit 3 (DTO): Data transfer over
  - Bit 2 (CMDD): Command done
  - Bit 1 (RE): Response error
  - Bit 0 (CD): Card detect
- (R/W)

**SDHOST\_SDIO\_INT\_MASK** Write 1 to correspond bit to enable interrupt from correspond card. One bit per card. Bit[0] corresponds to card[0]. (R/W)

Register 49.25. SDHOST\_MINTSTS\_REG (0x0040)



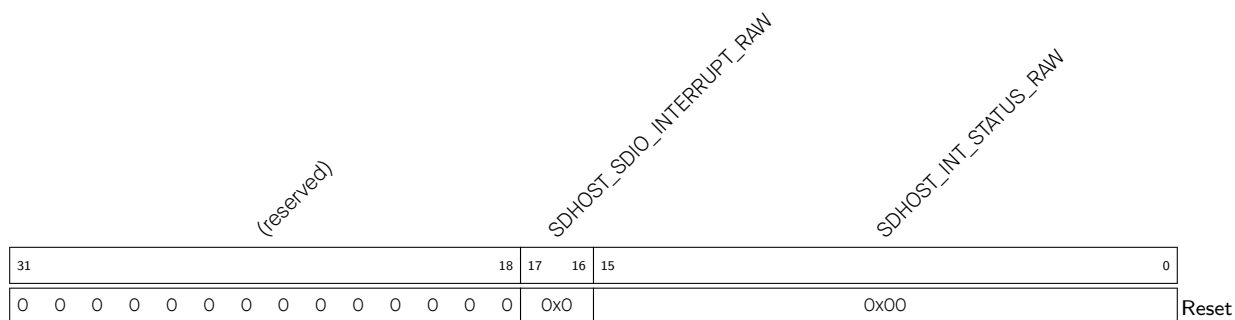
**SDHOST\_INT\_STATUS\_MSK** The masked interrupt status. For every bit:

- Bit 15 (EBE): End-bit error/no CRC error
- Bit 14 (ACD): Auto command done
- Bit 13 (SBE/BCI): RX Start Bit Error
- Bit 12 (HLE): Hardware locked write error
- Bit 11 (FRUN): FIFO underrun/overflow error
- Bit 10 (HTO): Data starvation by host timeout
- Bit 9 (DTRO): Data read timeout
- Bit 8 (RTO): Response timeout
- Bit 7 (DCRC): Data CRC error
- Bit 6 (RCRC): Response CRC error
- Bit 5 (RXDR): Receive FIFO data request
- Bit 4 (TXDR): Transmit FIFO data request
- Bit 3 (DTO): Data transfer over
- Bit 2 (CMDD): Command done
- Bit 1 (RE): Response error
- Bit 0 (CD): Card detect (RO)

**SDHOST\_SDIO\_INTERRUPT\_MSK** The masked interrupt status from SDIO card. One bit for each card. Bit[0] corresponds to card[0]. (RO)



### Register 49.26. SDHOST\_RINTSTS\_REG (0x0044)



**SDHOST\_INT\_STATUS\_RAW** The raw interrupt status. For every bit:

- Bit 15 (EBE): End-bit error/no CRC error
  - Bit 14 (ACD): Auto command done
  - Bit 13 (SBE/BCI): RX Start Bit Error
  - Bit 12 (HLE): Hardware locked write error
  - Bit 11 (FRUN): FIFO underrun/overflow error
  - Bit 10 (HTO): Data starvation by host timeout
  - Bit 9 (DTRO): Data read timeout
  - Bit 8 (RTO): Response timeout
  - Bit 7 (DCRC): Data CRC error
  - Bit 6 (RCRC): Response CRC error
  - Bit 5 (RXDR): Receive FIFO data request
  - Bit 4 (TXDR): Transmit FIFO data request
  - Bit 3 (DTO): Data transfer over
  - Bit 2 (CMDD): Command done
  - Bit 1 (RE): Response error
  - Bit 0 (CD): Card detect
- (R/WIC)

**SDHOST\_SDIO\_INTERRUPT\_RAW** The raw interrupt status from SDIO card. One bit per card. Bit[0] corresponds to card[0]. (R/W1C)

### Register 49.27. SDHOST\_IDSTS\_REG (0x008C)

[illegible]

**SDHOST\_IDSTS\_TI** The raw interrupt status of Transmit Interrupt. Indicates that data transmission is finished for a descriptor. (R/W1C)

**SDHOST\_IDSTS\_RI** The raw interrupt status of Receive Interrupt. Indicates the completion of data reception for a descriptor. (R/W1C)

**SDHOST\_IDSTS\_FBE** The raw interrupt status of Fatal Bus Error Interrupt. Indicates that a Bus Error occurred (SDHOST\_IDSTS\_REG[12:10]). (R/W1C)

**SDHOST\_IDSTS\_DU** The raw interrupt status of Descriptor Unavailable Interrupt. This bit is set when the descriptor is unavailable due to OWNER bit = 0 (DESO[31] = 0). (R/W1C)

**SDHOST\_IDSTS\_CES** The raw interrupt status of Card Error Summary. Indicates the status of the transaction to/from the card, also present in SDHOST\_RINTSTS\_REG. Indicates the logical OR of the following bits:

EBE: End-bit error/no CRC error

SBE/BCI: RX Start Bit Error

DRT0: Data read timeout

RTO: Response timeout

DCRC: Data CRC error

RCRC: Response CRC error

RE: Response error

The abort condition of the DMA depends on the setting of this field. If this field is enabled, then the DMA aborts on a response error. (R/W1C)

**SDHOST\_IDSTS\_NIS** The raw interrupt status of Normal Interrupt Summary. Logical OR of SDHOST\_IDSTS\_REG[1:0]. Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes this field to be set is cleared by software. (R/WIC)

**SDHOST\_IDSTS\_AIS** The raw interrupt status of Abnormal Interrupt Summary. Logical OR of SDHOST\_IDSTS\_REG[2], SDHOST\_IDSTS\_REG[4]. Only unmasked bits affect this bit. This is a sticky bit and must be cleared each time a corresponding bit that causes this field to be set is cleared by software. (R/W1C)

Continued on the next page...

**Register 49.27. SDHOST\_IDSTS\_REG (0x008C)**

Continued from the previous page...

**SDHOST\_IDSTS\_FBE\_CODE** Represents the type of error that caused a Bus Error, valid only when SDHOST\_IDSTS\_REG[2] is set.

0x1: Host Abort received during transmission

0x2: Host Abort received during reception

Others: Reserved

(RO)

**SDHOST\_IDSTS\_FSM** Represents DMA FSM present state.

0x0: DMA\_IDLE (idle state)

0x1: DMA\_SUSPEND (suspend state)

0x2: DESC\_RD (descriptor reading state)

0x3: DESC\_CHK (descriptor checking state)

0x4: DMA\_RD\_REQ\_WAIT (read-data request waiting state)

0x5: DMA\_WR\_REQ\_WAIT (write-data request waiting state)

0x6: DMA\_RD (data-read state)

0x7: DMA\_WR (data-write state)

0x8: DESC\_CLOSE (descriptor close state)

(RO)

**Register 49.28. SDHOST\_IDINTEN\_REG (0x0090)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                   |   |                   |   |            |   |                    |   |                   |       |                    |   |                   |  |                   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------|---|-------------------|---|------------|---|--------------------|---|-------------------|-------|--------------------|---|-------------------|--|-------------------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | SDHOST_IDINTEN_AI |   | SDHOST_IDINTEN_NI |   | (reserved) |   | SDHOST_IDINTEN_CES |   | SDHOST_IDINTEN_DU |       | SDHOST_IDINTEN_FBE |   | SDHOST_IDINTEN_RI |  | SDHOST_IDINTEN_TI |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 10                |   | 9                 | 8 | 7          | 6 | 5                  | 4 | 3                 | 2     | 1                  | 0 |                   |  |                   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                 | 0 | 0                 | 0 | 0          | 0 | 0                  | 0 | 0                 | Reset |                    |   |                   |  |                   |  |

**SDHOST\_IDINTEN\_TI** Write 1 to enable interrupt of Transmit. (R/W)

**SDHOST\_IDINTEN\_RI** Write 1 to enable interrupt of Receive. (R/W)

**SDHOST\_IDINTEN\_FBE** Write 1 to enable interrupt of Fatal Bus Error. (R/W)

**SDHOST\_IDINTEN\_DU** Write 1 to enable interrupt of Descriptor Unavailable. (R/W)

**SDHOST\_IDINTEN\_CES** Write 1 to enable interrupt of Card Error summary. (R/W)

**SDHOST\_IDINTEN\_NI** Write 1 to enable interrupt of Normal Interrupt Summary. (R/W)

**SDHOST\_IDINTEN\_AI** Write 1 to enable interrupt of Abnormal Interrupt Summary. (R/W)

**Register 49.29. SDHOST\_RESP0\_REG (0x0030)**

SDHOST\_RESPONSE0\_REG

|          |   |
|----------|---|
| 31       | 0 |
| 0x000000 |   |
| Reset    |   |

**SDHOST\_RESPONSE0\_REG** Represents bit[31:0] of response. (RO)

**Register 49.30. SDHOST\_RESP1\_REG (0x0034)**

SDHOST\_RESPONSE1\_REG

|          |   |
|----------|---|
| 31       | 0 |
| 0x000000 |   |
| Reset    |   |

**SDHOST\_RESPONSE1\_REG** Represents bit[63:32] of long response. (RO)

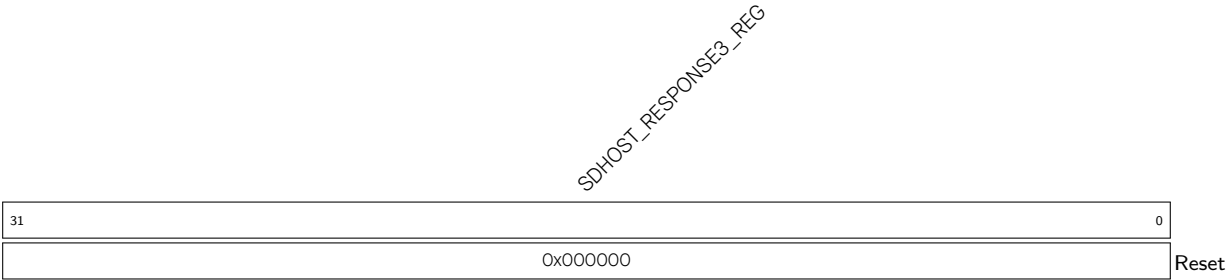
**Register 49.31. SDHOST\_RESP2\_REG (0x0038)**

SDHOST\_RESPONSE2\_REG

|          |   |
|----------|---|
| 31       | 0 |
| 0x000000 |   |
| Reset    |   |

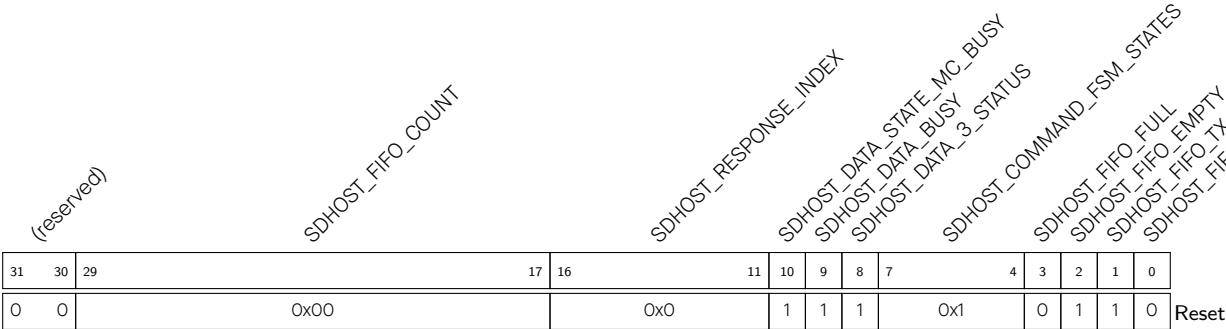
**SDHOST\_RESPONSE2\_REG** Represents bit[95:64] of long response. (RO)

Register 49.32. SDHOST\_RESP3\_REG (0x003C)



**SDHOST\_RESPONSE3\_REG** Represents bit[127:96] of long response. (RO)

Register 49.33. SDHOST\_STATUS\_REG (0x0048)



**SDHOST\_FIFO\_RX\_WATERMARK** Represents whether the FIFO reached Receive watermark level, not qualified with data transfer.  
0: Not reach  
1: Reach  
(RO)

**SDHOST\_FIFO\_TX\_WATERMARK** Represents whether the FIFO reached Transmit watermark level, not qualified with data transfer.  
0: Not reach  
1: Reach  
(RO)

**SDHOST\_FIFO\_EMPTY** Represents whether the FIFO is empty.  
0: Not empty  
1: Empty  
(RO)

**SDHOST\_FIFO\_FULL** Represents whether the FIFO is full.  
0: Not full  
1: Full  
(RO)

Continued on the next page...

**Register 49.33. SDHOST\_STATUS\_REG (0x0048)**

Continued from the previous page...

**SDHOST\_COMMAND\_FSM\_STATES** Represents the command FSM states.

0x0: Idle  
0x1: Send init sequence  
0x2: Send cmd start bit  
0x3: Send cmd tx bit  
0x4: Send cmd index + arg  
0x5: Send cmd crc7  
0x6: Send cmd end bit  
0x7: Receive resp start bit  
0x8: Receive resp IRQ response  
0x9: Receive resp tx bit  
0xA: Receive resp cmd idx  
0xB: Receive resp data  
0xC: Receive resp crc7  
0xD: Receive resp end bit  
0xE: Cmd path wait NCC  
0xF: Wait, cmd-to-response turnaround  
(RO)

**SDHOST\_DATA\_3\_STATUS** Represents the value of the sdhost\_card\_data[3] signal, which indicates whether card is present.

0: Card not present  
1: Card present  
(RO)

**SDHOST\_DATA\_BUSY** Represents inverted value of the sdhost\_card\_data[0] signal, which indicates card data is busy.

0: Card data not busy  
1: Card data busy  
(RO)

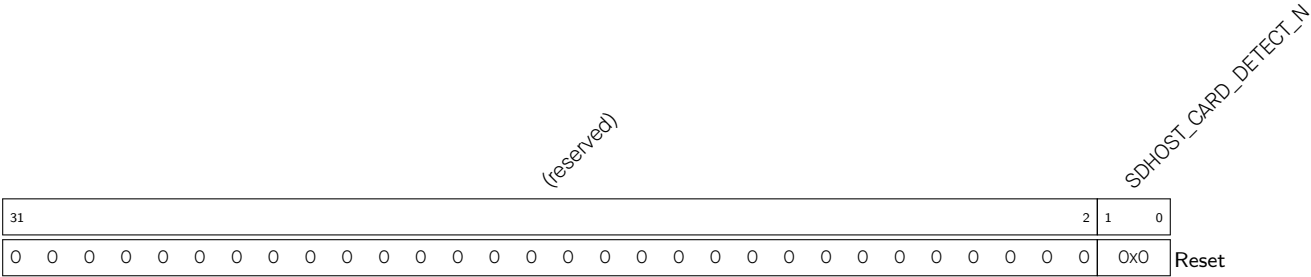
**SDHOST\_DATA\_STATE\_MC\_BUSY** Represents whether the data transmit or receive state-machine is busy.

0: Not busy  
1: Busy  
(RO)

**SDHOST\_RESPONSE\_INDEX** Represents index of previous response, including any auto-stop sent by core. (RO)

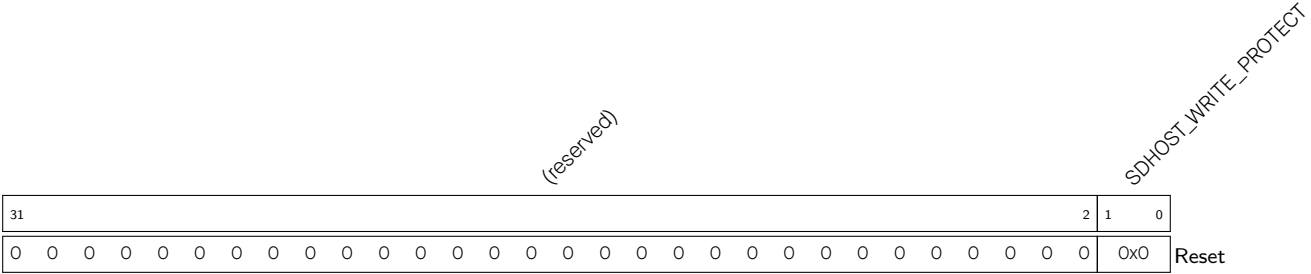
**SDHOST\_FIFO\_COUNT** Represents FIFO count, number of filled locations in FIFO. (RO)

Register 49.34. SDHOST\_CDETECT\_REG (0x0050)



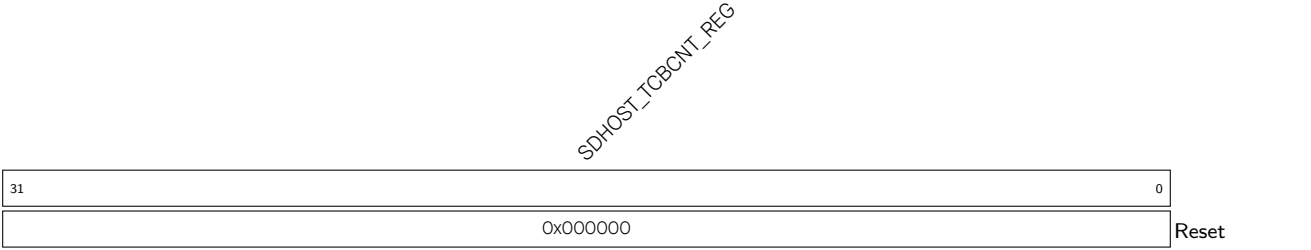
**SDHOST\_CARD\_DETECT\_N** Represents value on sdhost\_card\_detect\_n input ports. One bit per card. Bit[0] corresponds to card[0]. (RO)

Register 49.35. SDHOST\_WRTprt\_REG (0x0054)

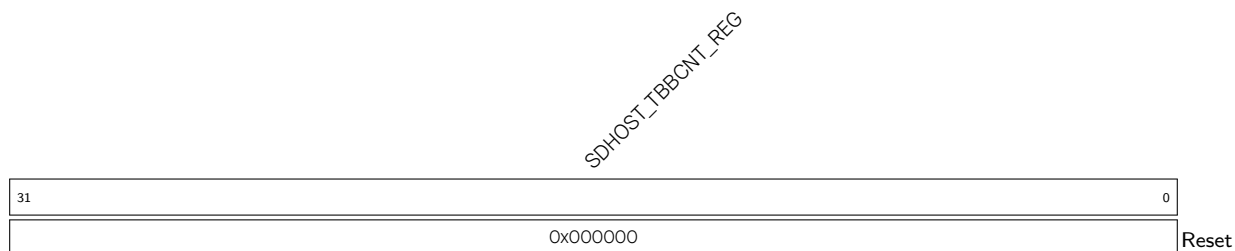


**SDHOST\_WRITE\_PROTECT** Represents value on sdhost\_card\_write\_prt input ports, one bit per card. Bit[0] corresponds to card[0]. (RO)

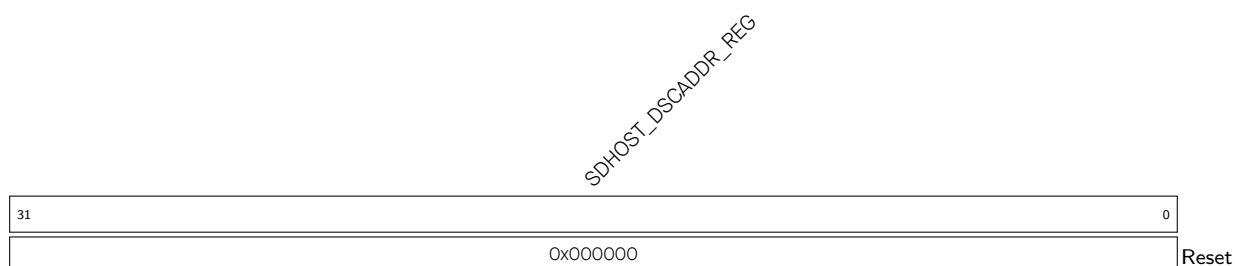
Register 49.36. SDHOST\_TCBCNT\_REG (0x005C)



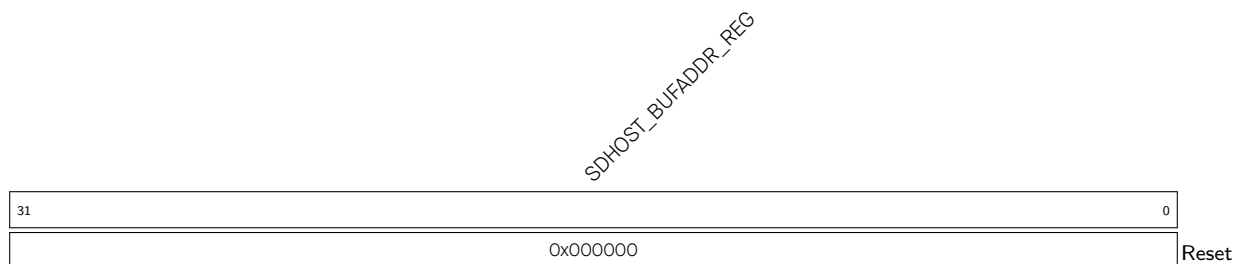
**SDHOST\_TCBCNT\_REG** Represents the number of bytes transferred by the CIU unit to the card. (RO)

**Register 49.37. SDHOST\_TBBCNT\_REG (0x0060)**

**SDHOST\_TBBCNT\_REG** Represents the number of bytes transferred between Host/DMA memory and BIU FIFO. (RO)

**Register 49.38. SDHOST\_DSCADDR\_REG (0x0094)**

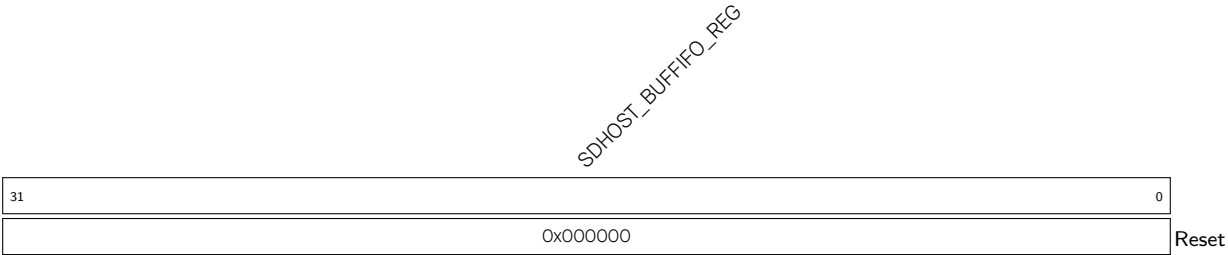
**SDHOST\_DSCADDR\_REG** Represents the Descriptor Address Pointer, points to the start address of current descriptor read by DMA. (RO)

**Register 49.39. SDHOST\_BUFADDR\_REG (0x0098)**

**SDHOST\_BUFADDR\_REG** Represents the Buffer Address Pointer, points to the current Data Buffer Address being accessed by the DMA. (RO)



Register 49.40. SDHOST\_BUFFIFO\_REG (0x0200)



**SDHOST\_BUFFIFO\_REG**    Date received or to be transmitted between FIFO and software directly. This register points to the current Data FIFO. (R/W)

## Chapter 50

### LED PWM Controller (LEDC)

#### 50.1 Overview

The LED PWM Controller is a peripheral designed to generate PWM signals for LED control. It has specialized features such as automatic duty cycle fading. However, the LED PWM Controller can also be used to generate PWM signals for other purposes.

#### 50.2 Features

The LED PWM Controller has the following features:

- Eight independent PWM generators (i.e., eight channels)
- Maximum PWM duty cycle resolution: 20 bits
- Four independent timers that support fractional division
- Adjustable phase of PWM signal output
- PWM duty cycle dithering
- Automatic duty cycle fading — gradual increase/decrease of a PWM's duty cycle without interference from the processor. An interrupt will be generated upon fade completion
- Up to 16 duty cycle ranges for each PWM generator to generate gamma curve signals - each range can be independently configured in terms of fading direction (increase or decrease), fading amount (the amount by which the duty cycle increases or decreases each time), the number of fades (how many times the duty cycle fades in one range), and fading frequency
- PWM signal output in low-power mode (Light-sleep mode)
- Event generation and task response related to the Event Task Matrix (ETM) peripheral

Note that the four timers are identical regarding their features and operation. The following sections refer to the timers collectively as Timer $x$  (where  $x$  ranges from 0 to 3). Likewise, the eight PWM generators are also identical in features and operation, and thus are collectively referred to as PWM $n$  (where  $n$  ranges from 0 to 7).

#### 50.3 Architectural Overview

Figure 50.3-1 shows the architecture of the LED PWM Controller.

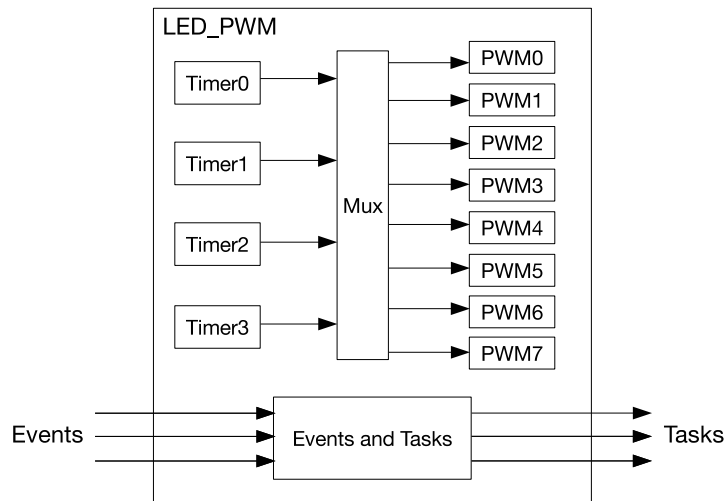


Figure 50.3-1. LED PWM Architecture

Each of the four timers has an internal timebase counter (i.e., a counter that counts on cycles of a reference clock) and thus can be independently configured (i.e., configurable clock divider, and counter overflow value). Each PWM generator selects one of the timers by configuring the `LEDC_TIMER_SEL_CHn`, and uses the timer's counter value `timerx_cnt` as a reference to generate its PWM signal.

Figure 50.3-2 illustrates the main functional blocks of the timer and the PWM generator.

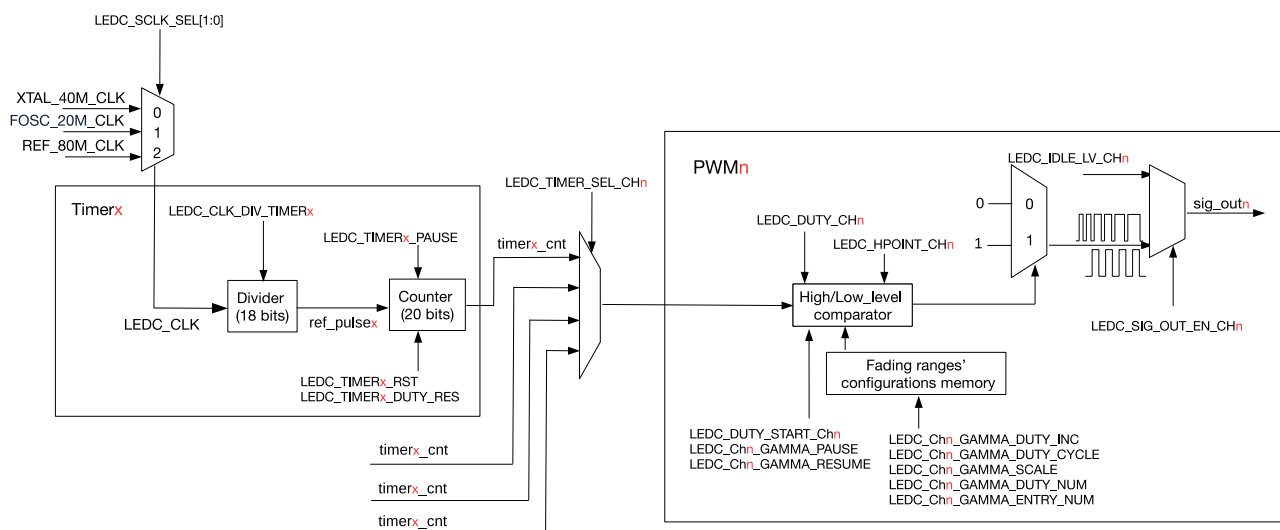


Figure 50.3-2. Timer and PWM Generator Block Diagram

## 50.4 Functional Description

### 50.4.1 Timers

Each timer in LED PWM Controller internally maintains a timebase counter. Referring to Figure 50.3-2, this clock signal used by the timebase counter is named `ref_pulsex`. All timers use the same clock source `LEDC_CLK`, which is then passed through a clock divider to generate `ref_pulsex` for the counter.

### 50.4.1.1 Clock Source

LED PWM registers configured by software are clocked by APB\_CLK. To use the LED PWM peripheral, the APB\_CLK signal going to the LED PWM has to be enabled. The APB\_CLK signal to LED PWM can be enabled by setting the HP\_SYS\_CLKRST\_LEDC\_APB\_CLK\_EN field in the HP\_SYS\_CLKRST\_SOC\_CLK\_CTRL3\_REG register. The LEDC\_CLK signal to LED PWM can be enabled by setting the HP\_SYS\_CLKRST\_LEDC\_CLK\_EN field in the HP\_SYS\_CLKRST\_PERI\_CLK\_CTRL22\_REG register. The LED PWM peripheral can be reset via software by setting the HP\_SYS\_CLKRST\_RST\_EN\_LEDC field in the HP\_SYS\_CLKRST\_HP\_RST\_EN1\_REG register.

Timers in the LED PWM Controller choose their common clock source from one of the following clock signals: XTAL\_40M\_CLK, FOSC\_20M\_CLK, and REF\_80M\_CLK. The procedure for selecting a clock source signal for LEDC\_CLK is described below:

- XTAL\_40M\_CLK: Set PCR\_LEDC\_SCLK\_SEL[1:0] to 0
- FOSC\_20M\_CLK: Set PCR\_LEDC\_SCLK\_SEL[1:0] to 1
- REF\_80M\_CLK: Set PCR\_LEDC\_SCLK\_SEL[1:0] to 2

The LEDC\_CLK signal will then be passed through the clock divider.

For more information, please refer to Chapter 9 [Reset and Clock](#).

### 50.4.1.2 Clock Divider Configuration

The LEDC\_CLK signal is passed through a clock divider to generate the ref\_pulse<sub>x</sub> signal for the counter. The frequency of ref\_pulse<sub>x</sub> is equal to the frequency of LEDC\_CLK divided by the divisor LEDC\_CLK\_DIV (see Figure 50.3-2).

The clock divider is a fractional divider. Thus, the divisor LEDC\_CLK\_DIV can be non-integer values. LEDC\_CLK\_DIV is configured according to the following equation.

$$\text{LEDC\_CLK\_DIV} = A + \frac{B}{256}$$

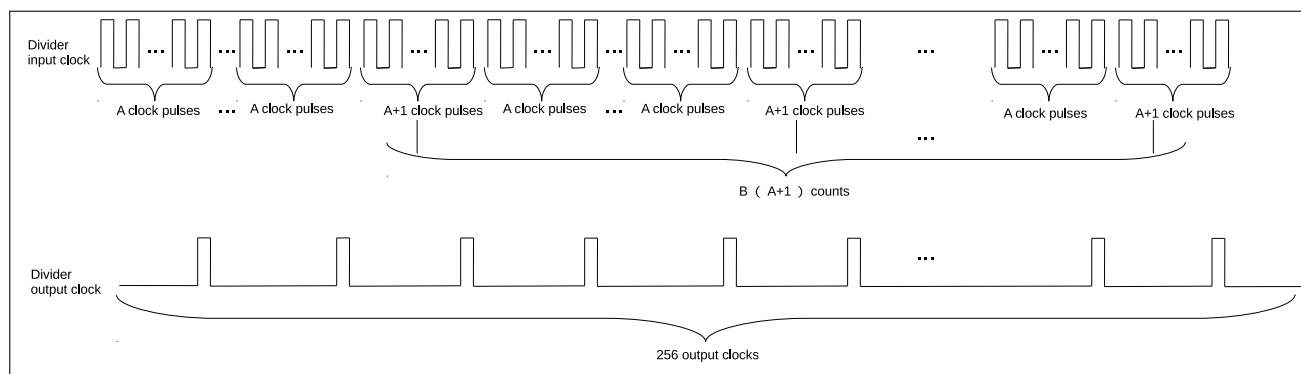
- The integer part  $A$  corresponds to the most significant 10 bits of LEDC\_CLK\_DIV\_TIMER<sub>x</sub> (i.e., LEDC\_TIMER<sub>x</sub>\_CONF\_REG[22:13])
- The fractional part  $B$  corresponds to the least significant 8 bits of LEDC\_CLK\_DIV\_TIMER<sub>x</sub> (i.e., LEDC\_TIMER<sub>x</sub>\_CONF\_REG[12:5])

When the fractional part  $B$  is 0, LEDC\_CLK\_DIV is equivalent to an integer divisor (i.e., an integer prescaler). In other words, a ref\_pulse<sub>x</sub> clock pulse is generated after every  $A$  number of LEDC\_CLK clock pulses.

However, when  $B$  is not 0, LEDC\_CLK\_DIV becomes a non-integer divisor. The clock divider implements non-integer frequency division by alternating between  $A$  and  $(A+1)$  LEDC\_CLK clock pulses per ref\_pulse<sub>x</sub> clock pulse. In this way, the average frequency of ref\_pulse<sub>x</sub> clock pulse will be the desired frequency (i.e., the non-integer divided frequency). For every 256 ref\_pulse<sub>x</sub> clock pulses:

- A number of  $B$  ref\_pulse<sub>x</sub> clock pulses are generated every  $(A+1)$  LEDC\_CLK clock pulses
- A number of  $(256-B)$  ref\_pulse<sub>x</sub> clock pulses are generated every  $A$  LEDC\_CLK clock pulses
- The ref\_pulse<sub>x</sub> clock pulses generated every  $(A+1)$  pulses are evenly distributed amongst those generated every  $A$  pulses

Figure 50.4-1 illustrates the relation between LEDC\_CLK clock pulses and ref\_pulse $x$  clock pulses when LEDC\_CLK\_DIV is a non-integer value.

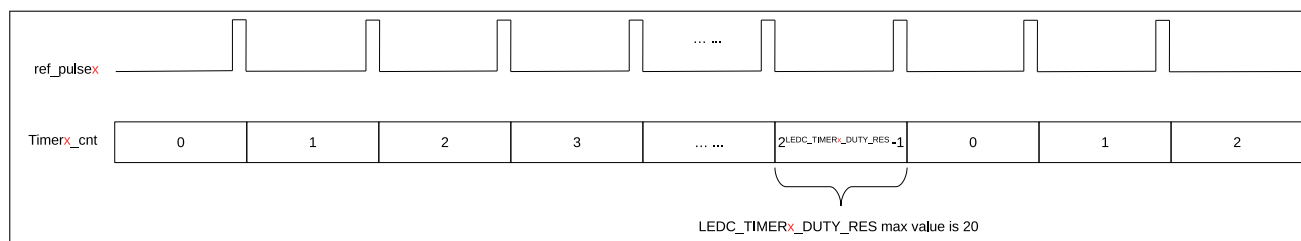


**Figure 50.4-1. Frequency Division When LEDC\_CLK\_DIV is a Non-Integer Value**

To change the timer's clock divisor at runtime, first configure the `LEDC_CLK_DIV_TIMER $x$`  field, and then set the `LEDC_TIMER $x$ _PARA_UP` field to apply the new configuration. This will cause the newly configured values to take effect upon the next overflow of the counter. The `LEDC_TIMER $x$ _PARA_UP` field will be automatically cleared by hardware.

### 50.4.1.3 20-Bit Counter

Each timer contains a 20-bit timebase counter that uses ref\_pulse $x$  as its reference clock (see Figure 50.3-2). The `LEDC_TIMER $x$ _DUTY_RES` field configures the actual used bit width of this 20-bit counter. Hence, the maximum resolution of the PWM signal is 20 bits. The counter counts up to  $2^{\text{LEDC\_TIMER}_x\text{\_DUTY\_RES}} - 1$ , overflows and begins counting from 0 again. The counter's value can be read, reset, and suspended by software. Figure 50.4-2 shows the relationship between the counter and PWM resolution.



**Figure 50.4-2. Relationship Between Counter And Resolution**

Every time the counter overflows, it can trigger the `LEDC_TIMER $x$ _OVF_INT` interrupt (generated automatically by hardware without configuration). It can also be configured to trigger `LEDC_OVF_CNT_CH $n$ _INT` interrupt after overflowing `LEDC_OVF_NUM_CH $n$  + 1` times. To configure `LEDC_OVF_CNT_CH $n$ _INT` interrupt, please:

1. Configure `LEDC_TIMER_SEL_CH $n$`  to select the timer for the PWM generator
2. Enable the overflow counter by setting `LEDC_OVF_CNT_EN_CH $n$`
3. Configure `LEDC_OVF_NUM_CH $n$`  with the number of counter overflows (that triggers an interrupt) minus 1
4. Enable the overflow interrupt by setting `LEDC_OVF_CNT_CH $n$ _INT_ENA`
5. Configure `LEDC_TIMER $x$ _DUTY_RES` to specify the counter bit width for the selected Timer $x$  and wait for a `LEDC_OVF_CNT_CH $n$ _INT` interrupt

To change the overflow value at runtime, first set the `LEDC_TIMERx_DUTY_RES` field, and then set the `LEDC_TIMERx_PARA_UP` field. This will cause the newly configured values to take effect upon the next overflow of the counter. If `LEDC_OVF_CNT_EN_CHn` field is reconfigured, `LEDC_PARA_UP_CHn` should be set to apply the new configuration. In summary, these configuration values need to be updated by setting `LEDC_TIMERx_PARA_UP` or `LEDC_PARA_UP_CHn`. `LEDC_TIMERx_PARA_UP` and `LEDC_PARA_UP_CHn` will be automatically cleared by hardware.

Referring to Figure 50.3-2, the frequency of a PWM generator output signal (`sig_outn`) is dependent on the frequency of the timer's clock source `LEDC_CLK`, the clock divisor `LEDC_CLK_DIV`, and the duty resolution (counter width) `LEDC_TIMERx_DUTY_RES`:

$$f_{\text{PWM}} = \frac{f_{\text{LEDC\_CLK}}}{\text{LEDC\_CLK\_DIV} \cdot 2^{\text{LEDC\_TIMERx\_DUTY\_RES}}}$$

Based on the formula above, the desired duty resolution can be calculated as follows:

$$\text{LEDC\_TIMERx\_DUTY\_RES} = \log_2 \left( \frac{f_{\text{LEDC\_CLK}}}{f_{\text{PWM}} \cdot \text{LEDC\_CLK\_DIV}} \right)$$

Table 50.4-1 lists the commonly-used frequencies and their corresponding resolutions.

**Table 50.4-1. Commonly-used Frequencies and Resolutions**

| LEDC_CLK              | PWM Frequency | Highest Resolution (bit) <sup>1</sup> | Lowest Resolution (bit) <sup>2</sup> |
|-----------------------|---------------|---------------------------------------|--------------------------------------|
| REF_80M_CLK (80 MHz)  | 1 kHz         | 16                                    | 6                                    |
| REF_80M_CLK (80 MHz)  | 5 kHz         | 13                                    | 3                                    |
| REF_80M_CLK (80 MHz)  | 10 kHz        | 12                                    | 2                                    |
| XTAL_40M_CLK (40 MHz) | 1 kHz         | 15                                    | 5                                    |
| XTAL_40M_CLK (40 MHz) | 4 kHz         | 13                                    | 3                                    |
| FOSC_20M_CLK (20 MHz) | 1 kHz         | 14                                    | 4                                    |
| FOSC_20M_CLK (20 MHz) | 2 kHz         | 13                                    | 3                                    |

<sup>1</sup> The highest resolution is calculated when the clock divisor `LEDC_CLK_DIV` is 1. If the highest resolution calculated by the formula is higher than the counter's width 20 bits, then the highest resolution should be 20 bits.

<sup>2</sup> The lowest resolution is calculated when the clock divisor `LEDC_CLK_DIV` is  $1023 + \frac{255}{256}$ . If the lowest resolution calculated by the formula is lower than 0, then the lowest resolution should be 1.

## 50.4.2 PWM Generators

To generate a PWM signal, a PWM generator (`PWMn`) needs a timer (`Timerx`). Each PWM generator can be configured separately by setting `LEDC_TIMER_SEL_CHn` to use one of four timers to generate the PWM output.

As shown in Figure 50.3-2, each PWM generator has a comparator and two multiplexers. A PWM generator compares the timer's 20-bit counter value (`Timerx_cnt`) to two trigger values `Hpointn` and `Lpointn`. When the timer's counter value is equal to `Hpointn` or `Lpointn`, the PWM signal is high or low, respectively, as described below:

- If `Timer $x$ _cnt == Hpoint $n$` , `sig_out $n$`  is 1.
- If `Timer $x$ _cnt == Lpoint $n$` , `sig_out $n$`  is 0.

Figure 50.4-3 illustrates how `Hpoint $n$`  and `Lpoint $n$`  are used to generate a fixed duty cycle PWM output signal.

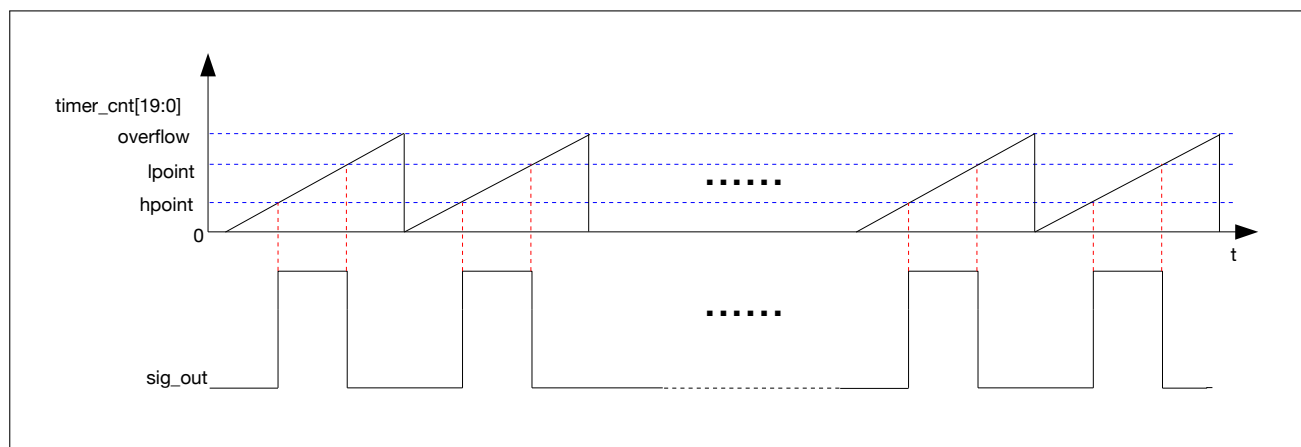


Figure 50.4-3. LED PWM Output Signal Diagram

For a particular PWM generator (PWM $n$ ), its `Hpoint $n$`  is sampled from the `LEDC_HPOINT_CH $n$`  field each time the selected timer's counter overflows. Likewise, `Lpoint $n$`  is also sampled on every counter overflow and is calculated from the sum of the `LEDC_DUTY_CH $n$ [24:4]` and `LEDC_HPOINT_CH $n$`  fields. By setting `Hpoint $n$`  and `Lpoint $n$`  via the `LEDC_HPOINT_CH $n$`  and `LEDC_DUTY_CH $n$ [24:4]` fields, the relative phase and duty cycle of the PWM output can be set.

The PWM output signal (`sig_out $n$` ) is enabled by setting `LEDC_SIG_OUT_EN_CH $n$` . When `LEDC_SIG_OUT_EN_CH $n$`  is cleared, PWM signal output is disabled, and the output signal (`sig_out $n$` ) will output a constant level specified by `LEDC_IDLE_LV_CH $n$` .

The bits `LEDC_DUTY_CH $n$ [3:0]` are used to dither the duty cycles of the PWM output signal (`sig_out $n$` ) by periodically altering the duty cycle of `sig_out $n$` . When `LEDC_DUTY_CH $n$ [3:0]` is not 0, then for every 16 cycles of `sig_out $n$` , `LEDC_DUTY_CH $n$ [3:0]` of those cycles will have PWM pulses that are one timer tick longer than the other (16- `LEDC_DUTY_CH $n$ [3:0]`) cycles. For instance, if `LEDC_DUTY_CH $n$ [24:4]` is set to 10 and `LEDC_DUTY_CH $n$ [3:0]` is set to 5, then 5 of 16 cycles will have a PWM pulse with a duty value of 11 and the rest of the 16 cycles will have a PWM pulse with a duty value of 10. The average duty cycle after 16 cycles is 10.3125.

If fields `LEDC_TIMER_SEL_CH $n$` , `LEDC_HPOINT_CH $n$` , `LEDC_DUTY_CH $n$ [24:4]`, and `LEDC_SIG_OUT_EN_CH $n$`  are reconfigured, `LEDC_PARA_UP_CH $n$`  must be set to apply the new configuration. This will cause the newly configured values to take effect upon the next overflow of the counter. `LEDC_PARA_UP_CH $n$`  field will be automatically cleared by hardware.

### 50.4.3 Duty Cycle Fading

The PWM generators can fade the duty cycle of a PWM output signal (i.e., gradually change the duty cycle from one value to another). Each PWM generator can have up to 16 duty cycle ranges, which can be independently configured in terms of fading direction (increase or decrease), fading amount, the number of fades, and fading frequency. If Duty Cycle Fading is enabled, every range's `Lpoint $n$`  value will change

according to its fading configuration.

### 50.4.3.1 Linear Duty Cycle Fading

Linear fading PWM signals can be generated by configuring the direction, fading amount, the number of fades, and fading frequency of the first duty cycle range.

The programming procedures will be described in detail in the section [50.6](#).

After the procedures, the PWM generator can fade the duty cycle of a PWM signal once per LEDC\_CH $n$ \_GAMMA\_DUTY\_CYCLE times of counter overflows. Every time when the PWM signal is faded, Lpoint $n$  increases or decreases (configured by LEDC\_CH $n$ \_GAMMA\_DUTY\_INC) by LEDC\_CH $n$ \_GAMMA\_SCALE, and the duty cycle increases or decreases (configured by LEDC\_CH $n$ \_GAMMA\_DUTY\_INC) by

$$\frac{\text{LEDC\_CH}_n\text{\_GAMMA\_SCALE}}{\text{LEDC\_TIMER}_x\text{\_DUTY\_RES}}$$

The duty cycle is faded for LEDC\_CH $n$ \_GAMMA\_DUTY\_NUM times. After that, the PWM generator stops fading and keeps outputting signals at this duty cycle. Upon each fading the duty cycle increases or decreases by the same amount, and therefore the PWM signal is a linear fading signal.

Figure 50.4-4 shows a linear fading PWM signal.

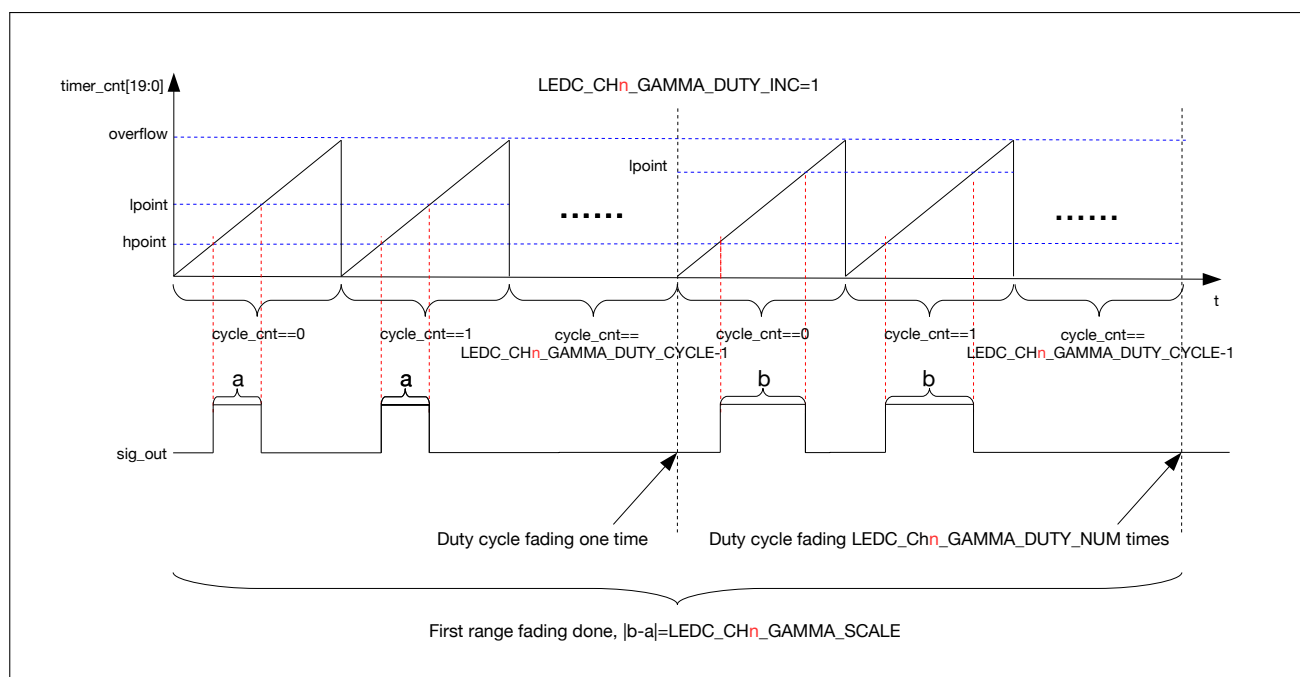


Figure 50.4-4. Output Signal of Linear Duty Cycle Fading

### 50.4.3.2 Gamma Curve Fading

Gamma curve fading PWM signals can be generated by configuring the fading direction, fading amount, the number of fades and fading frequency of multiple duty cycle fading ranges.

The programming procedures will be described in detail in the section [50.6](#).



After the procedures, the PWM generator can generate a PWM signal with `LEDC_CH $n$ _GAMMA_ENTRY_NUM` ranges. The duty cycle of the PWM signal fades according to the configurations of range 0 first, and then range 1, till range (`LEDC_CH $n$ _GAMMA_ENTRY_NUM` – 1) (the last range) where Duty Cycle Fading ends. The PWM signal fades independently in each range. According to the configuration of each range, every time when the counter overflows for `LEDC_CH $n$ _GAMMA_DUTY_CYCLE` times, `Lpoint $n$`  increases or decreases (configured by `LEDC_CH $n$ _GAMMA_DUTY_INC`) by `LEDC_CH $n$ _GAMMA_SCALE`, and accordingly the duty cycle increases or decreases (configured by `LEDC_CH $n$ _GAMMA_DUTY_INC`) by

$$\frac{\text{LEDC\_CH}_n\text{\_GAMMA\_SCALE}}{\text{LEDC\_TIMER}_x\text{\_DUTY\_RES}}$$

After the duty cycle fades for `LEDC_CH $n$ _GAMMA_DUTY_NUM` times in a range, Duty Cycle Fading in this range finishes.

When Duty Cycle Fading finishes in all ranges (the number of ranges is specified by `LEDC_CH $n$ _GAMMA_ENTRY_NUM`), the PWM signal stops fading and keeps the duty cycle of the last fade. Given that the duty cycle fades differently and linearly in each range, several linear fading ranges would be fitted to a gamma curve.

Figure 50.4-5 illustrates a gamma curve fading PWM signal.

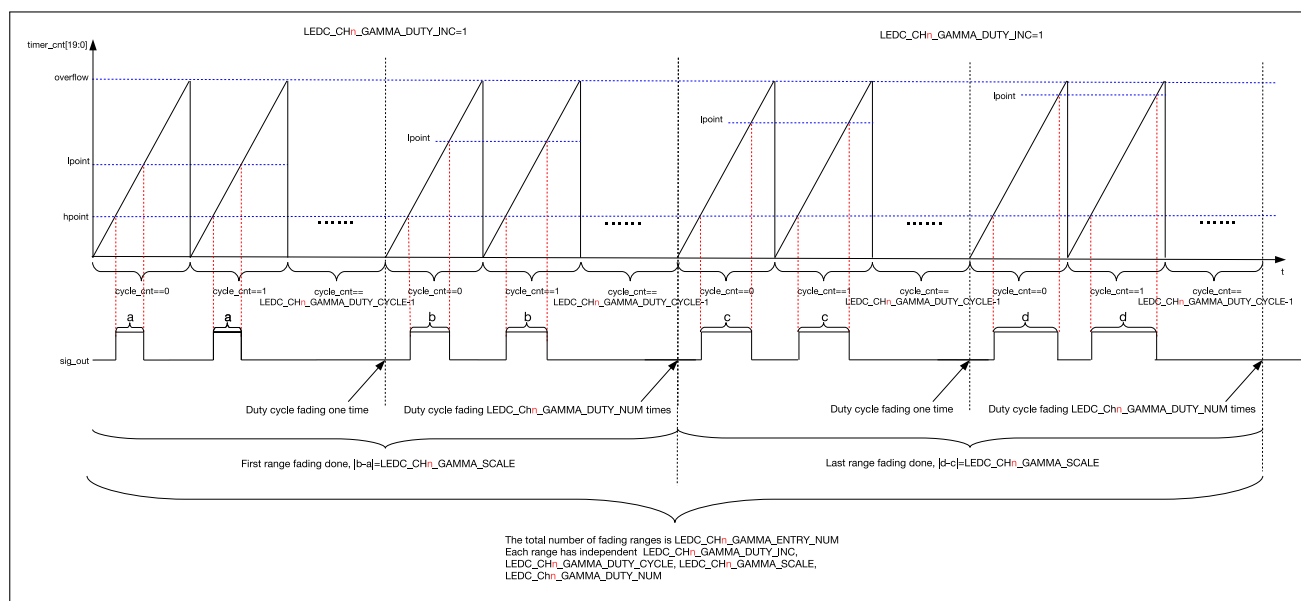


Figure 50.4-5. Output Signal of Gamma Curve Fading

### 50.4.3.3 Suspend and Resume Duty Cycle Fading

To suspend Duty Cycle Fading that has already been started, write 1 to the `LEDC_CH $n$ _GAMMA_PAUSE` field of the `LEDC_CH $n$ _GAMMA_CONF_REG` register. Once `LEDC_CH $n$ _GAMMA_PAUSE` is set to 1, the PWM signal keeps the duty cycle of the most recent fade.

To resume Duty Cycle Fading, write 1 to the `LEDC_CH $n$ _GAMMA_RESUME` field of the `LEDC_CH $n$ _GAMMA_CONF_REG` register. Once `LEDC_CH $n$ _GAMMA_RESUME` is set to 1, the PWM signal resumes fading from the range where the suspension occurs, until fading in the last range finishes. The fading will continue from the state when it was paused until all the ranges complete duty cycle fading (when

`LEDC_CH $n$ _GAMMA_RESUME` is set to 1, `LEDC_CH $n$ _GAMMA_PAUSE` is cleared automatically by hardware.

### 50.4.4 Event Task Matrix Feature

The LEDC on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows LEDC's ETM tasks to be triggered by any peripherals' ETM events, or LEDC's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to LEDC. For more information, please refer to [Chapter 12 Event Task Matrix \(ETM\)](#).

ETM-related events and tasks are enabled by configuring corresponding fields of `LEDC_EVT_TASK_ENO_REG`, `LEDC_EVT_TASK_EN1_REG` and `LEDC_EVT_TASK_EN2_REG` registers. For the correspondence between events, tasks, and fields, Please refer to [Section 50.8](#)).

LEDC can receive the following ETM tasks:

- `LEDC_TASK_DUTY_SCALE_UPDATE_CH $n$` : If the `LEDC_TASK_DUTY_SCALE_UPDATE_CH $n$ _EN` field is enabled, upon receiving the `LEDC_TASK_DUTY_SCALE_UPDATE_CH $n$`  task, PWM $n$  generates fading PWM signals according to the newly configured `LEDC_CH $n$ _GAMMA_SCALE` field.
- `LEDC_TASK_TIMER $x$ _RES_UPDATE`: If the `LEDC_TASK_TIMER $x$ _RES_UPDATE_EN` field is enabled, upon receiving the `LEDC_TASK_TIMER $x$ _RES_UPDATE` task, Timer $x$  updates its counter's overflow value to the value configured in the `LEDC_TIMER $x$ _DUTY_RES` field at the next overflow of the counter.
- `LEDC_TASK_TIMER $x$ _CAP`: If the `LEDC_TASK_TIMER $x$ _CAP_EN` field is enabled, upon receiving the `LEDC_TASK_TIMER $x$ _CAP` task, Timer $x$  captures its counter's value, and stores the value into the `LEDC_TIMER $x$ _CNT_CAP` field of register `LEDC_TIMER $x$ _CNT_CAP_REG`.
- `LEDC_TASK_SIG_OUT_DIS_CH $n$` : If the `LEDC_TASK_SIG_OUT_DIS_CH $n$ _EN` field is enabled, upon receiving the `LEDC_TASK_SIG_OUT_DIS_CH $n$`  task, PWM $n$ 's signal output is disabled, and the output signal (sig\_out $n$ ) outputs a constant level as specified by field `LEDC_IDLE_LV_CH $n$` , as shown in [Figure 50.3-2](#).
- `LEDC_TASK_OVF_CNT_RST_CH $n$` : If the `LEDC_TASK_OVF_CNT_RST_CH $n$ _EN` field is enabled, upon receiving the `LEDC_TASK_OVF_CNT_RST_CH $n$`  task, PWM $n$  timer's overflow counter is reset to 0.
- `LEDC_TASK_TIMER $x$ _RST`: If the `LEDC_TASK_TIMER $x$ _RST_EN` field is enabled, upon receiving the `LEDC_TASK_TIMER $x$ _RST` task, Timer $x$ 's counter is reset to 0.
- `LEDC_TASK_TIMER $x$ _RESUME` and `LEDC_TASK_TIMER $x$ _PAUSE`: If the `LEDC_TASK_TIMER $x$ _PAUSE_RESUME_EN` field is enabled, upon receiving the `LEDC_TASK_TIMER $x$ _RESUME` and `LEDC_TASK_TIMER $x$ _PAUSE` task, Timer $x$  is suspended and resumed alternately. That is, when the task is received, Timer $x$  is paused; and when the task is received again, Timer $x$  is resumed.
- `LEDC_TASK_GAMMA_RESTART_CH $n$` : If the `LEDC_TASK_GAMMA_RESTART_CH $n$ _EN` field is enabled, upon receiving the `LEDC_TASK_GAMMA_RESTART_CH $n$`  task, the PWM $n$  restarts to generate the fading PWM signal.
- `LEDC_TASK_GAMMA_PAUSE_CH $n$` : If the `LEDC_TASK_GAMMA_PAUSE_CH $n$ _EN` field is enabled, upon receiving the `LEDC_TASK_GAMMA_PAUSE_CH $n$`  task, PWM $n$  suspends Duty Cycle Fading at the next timer overflow. That is, after the task has been received, PWM $n$  keeps the duty cycle of the last fade.

- LEDC\_TASK\_GAMMA\_RESUME\_CH $n$ : If the [LEDC\\_TASK\\_GAMMA\\_RESUME\\_CH \$n\$ \\_EN](#) field is enabled, upon receiving the LEDC\_TASK\_GAMMA\_RESUME\_CH $n$  task, PWM $n$  resumes Duty Cycle Fading at the next counter overflow. That is, after the task has been received, PWM $n$  resumes fading from the range where the suspension occurs.

LEDC can generate the following ETM events:

- LEDC\_EVT\_DUTY\_CHNG\_END\_CH $n$ : Generated when the [LEDC\\_EVT\\_DUTY\\_CHNG\\_END\\_CH \$n\$ \\_EN](#) field is enabled, and PWM $n$  has finished Duty Cycle Fading.
- LEDC\_EVT\_OVF\_CNT\_PLS\_CH $n$ : Generated when the [LEDC\\_EVT\\_OVF\\_CNT\\_PLS\\_CH \$n\$ \\_EN](#) field is enabled and when PWM $n$  timer's counter overflows for [LEDC\\_OVF\\_NUM\\_CH \$n\$](#)  + 1 times.
- LEDC\_EVT\_TIME\_OVF\_TIMER $x$ : Generated when the [LEDC\\_EVT\\_TIME\\_OVF\\_TIMER \$x\$ \\_EN](#) field is enabled and Timer $x$ 's counter overflows.
- LEDC\_EVT\_TIMER $x$ \_CMP: Generated when the [LEDC\\_EVT\\_TIMER \$x\$ \\_CMP\\_EN](#) field is enabled and the value of Timer $x$ 's counter reaches that of the [LEDC\\_TIMER \$x\$ \\_CMP](#) field of register [LEDC\\_TIMER \$x\$ \\_CMP\\_REG](#).

In practical applications, LEDC's ETM events can trigger its own ETM tasks. For example, LEDC\_EVT\_DUTY\_CHNG\_END\_CH $n$  event can trigger the LEDC\_TASK\_GAMMA\_RESTART\_CH $n$  task, thus starting the next fading directly after the current fading is completed.

## 50.5 Interrupts

ESP32-P4's LEDC can generate the LEDC\_INT interrupt signal, which will be sent to the [Interrupt Matrix](#).

Interrupt signal LEDC\_INT can be generated by the following internal interrupt sources:

- LEDC\_OVF\_CNT\_CH $n$ \_INT: Triggered when the timer counter overflows for [LEDC\\_OVF\\_NUM\\_CH \$n\$](#)  + 1 times and the register [LEDC\\_OVF\\_CNT\\_EN\\_CH \$n\$](#)  is set to 1.
- LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT: Triggered when a fade on PWM $n$  has finished.
- LEDC\_TIMER $x$ \_OVF\_INT: Triggered when Timer $x$  has reached its maximum counter value.

The above interrupt sources can only be triggered when the interrupt enable register [XXX\\_ENA](#) is set to 1. Write 1 to [XXX\\_CLR](#) will clear the interrupt ([XXX](#) is the interrupt source name).

## 50.6 Programming Procedures

The configuration process of the LED PWM controller to generate PWM signals is as follows:

1. Configure the Timer $x$  according to section [50.4.1](#). After that, the clock source, divider, and counter are ready.
2. Configure the PWM $n$  generator according to section [50.4.2](#). After that, PWM $n$  selects one of the four timers and the phase and duty cycle of the PWM $n$  output is set.
3. Choose the corresponding configuration process based on the different duty cycle fading types:
  - (a) Linear duty cycle fading:
    - i. Configure the [LEDC\\_DUTY\\_CH \$n\$](#)  field with the initial value of [Lpoint \$n\$](#) .

- ii. Set the `LEDC_DUTY_START_CHn` field to enable Duty Cycle Fading. When this field is cleared, Duty Cycle Fading will be disabled.
  - iii. Write the linear duty cycle fading configuration to (`LEDC_CHn_MEM` starting address + duty cycle range number \* 4), the `LEDC_CHn_MEM` starting address is provided in Table 50.7-1. Please note that the following bit names are just for easier description, and there are no such register fields.
    - Bit 0 of the configuration data is used to configure the direction (hereafter referred to as `LEDC_CHn_GAMMA_DUTY_INC`). When it is set or cleared, the `Lpointn` will increase or decrease in the current configured range.
    - Bit 1 to 10 of the configuration data is used to configure the number of times the counter overflows per an increment or decrement of `Lpointn` (hereafter referred to as `LEDC_CHn_GAMMA_DUTY_CYCLE`). In other words, `Lpointn` will increase or decrease after the counter overflows for the configured number of times.
    - Bit 11 to 20 of the configuration data is used to configure the amount by which `Lpointn` increase or decrease in the current configured range (hereafter referred to as `LEDC_CHn_GAMMA_SCALE`).
    - Bit 21 to 30 of the configuration data is used to configure the number of fades in the current configured range (hereafter referred to as `LEDC_CHn_GAMMA_DUTY_NUM`).
    - The duty cycle range number (from 0 to 15) specifies to which range the above configuration data apply. For linear duty cycle fading only the first range needs to be configured, so the duty cycle range number should be configured as 0.
  - iv. Configure the number of ranges per each fading (1 in this case) via the `LEDC_CHn_GAMMA_ENTRY_NUM` field of the `LEDC_CHn_GAMMA_CONF_REG`. Once the specified number of ranges have been faded, Duty Cycle Fading stops and the PWM generator triggers the `LEDC_DUTY_CHNG_END_CHn_INT` interrupt. For linear duty cycle fading there is only one duty cycle range (i.e., the first one), so configure `LEDC_CHn_GAMMA_ENTRY_NUM` as 1.
  - v. Set the `LEDC_PARA_UP_CHn` field to apply the above configurations. After this field is set, the configurations for Duty Cycle Fading will take effect upon the next overflow of the counter, and the PWM generator will output a linear fading PWM signal following configurations. `LEDC_PARA_UP_CHn` field will be automatically cleared by hardware.
- (b) Gamma curve fading:
- i. The same as Step 1 in Section 50.4.3.1.
  - ii. The same as Step 2 in Section 50.4.3.1.
  - iii. Configure multiple duty cycle ranges with the following steps. Write the gamma curve fading configuration to (`LEDC_CHn_MEM` starting address + duty cycle range number \* 4), the `LEDC_CHn_MEM` starting address is provided in Table 50.7-1.
    - Bit 0 of the configuration data is used to configure the direction (hereafter referred to as `LEDC_CHn_GAMMA_DUTY_INC`). When it is set or cleared, the `Lpointn` will increment or decrement in the current configured range.

- Bit 1 to 10 of the configuration data is used to configure the number of times the counter overflows per an increase or decrease of Lpoint $n$  (hereafter referred to as LEDC\_CH $n$ \_GAMMA\_DUTY\_CYCLE). In other words, Lpoint $n$  will increase or decrease after the counter overflows for the configured number of times.
  - Bit 11 to 20 of the configuration data is used to configure the amount by which Lpoint $n$  increase or decrease in the current configured range (hereafter referred to as LEDC\_CH $n$ \_GAMMA\_SCALE).
  - Bit 21 to 30 of the configuration data is used to configure the number of fades in the current configured range (hereafter referred to as LEDC\_CH $n$ \_GAMMA\_DUTY\_NUM).
  - The duty cycle range number (from 0 to 15) specifies to which range the above configuration data apply. For gamma curve fading, it must start from 0 and increase by 1 for the next range to be configured.
  - Once the above procedures are finished, the configuration for one range is complete. Other ranges are configured by repeating the same set of procedures. You can configure any number of ranges from 0 to 15, and each can be configured independently.
- iv. After all required ranges are configured, write the total number of ranges configured in Step 3 to the LEDC\_CH $n$ \_GAMMA\_ENTRY\_NUM field of the LEDC\_CH $n$ \_GAMMA\_CONF\_REG register.
- v. Set the LEDC\_PARA\_UP\_CH $n$  field to apply the above configuration. After this field is set, the configurations for duty cycle fading will take effect upon the next overflow of the counter, and the PWM generator will output a gamma curve fading PWM signal following the configurations. LEDC\_PARA\_UP\_CH $n$  field will be automatically cleared by hardware.

After the above procedures, the LED PWM controller will generate the desired PWM signals.

At any time, duty cycle fading can be suspended or resumed, more details can be found in section 50.4.3.3. If the duty cycle fading configurations need to be changed before the PWM signals stop fading (that is, the LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT has not been triggered), the duty cycle fading needs to be suspended before changing the configurations. However, if the duty cycle fading configurations need to be changed after the PWM signals stop fading (that is, the LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT has been triggered), the configurations can be changed directly.

At any time, PWM signal output can be enabled or disabled by software, and the output signal level can be changed, more details can be found in section 50.4.2.

## 50.7 Memory Blocks

Each LEDC channel has a memory to store duty cycle fading configuration data. Each memory can store configuration data for up to 16 ranges. The addresses in this section are relative to LED PWM Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

**Table 50.7-1. LEDC Memory Blocks**

| Name             | Description       | Size | Starting Address           | Ending Address                   | Access |
|------------------|-------------------|------|----------------------------|----------------------------------|--------|
| LEDC_CH $n$ _MEM | Memory of PWM $n$ | 64 B | $0x400 + \text{PWM}n * 64$ | $0x400 + (\text{PWM}n + 1) * 64$ | WR     |

## 50.8 Register Summary

The addresses in this section are relative to LED PWM Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                 | Description                               | Address | Access |
|--------------------------------------|---|---------|--------|
| <b>Configuration Register</b>        |   |         |        |
| <a href="#">LEDC_CHO_CONFO_REG</a>   | Configuration register 0 for channel 0    | 0x0000  | varies |
| <a href="#">LEDC_CHO_HPOINT_REG</a>  | High point register for channel 0         | 0x0004  | R/W    |
| <a href="#">LEDC_CHO_DUTY_REG</a>    | Initial duty cycle register for channel 0 | 0x0008  | R/W    |
| <a href="#">LEDC_CHO_CONF1_REG</a>   | Configuration register 1 for channel 0    | 0x000C  | R/W/SC |
| <a href="#">LEDC_CH1_CONFO_REG</a>   | Configuration register 0 for channel 1    | 0x0014  | varies |
| <a href="#">LEDC_CH1_HPOINT_REG</a>  | High point register for channel 1         | 0x0018  | R/W    |
| <a href="#">LEDC_CH1_DUTY_REG</a>    | Initial duty cycle register for channel 1 | 0x001C  | R/W    |
| <a href="#">LEDC_CH1_CONF1_REG</a>   | Configuration register 1 for channel 1    | 0x0020  | R/W/SC |
| <a href="#">LEDC_CH2_CONFO_REG</a>   | Configuration register 0 for channel 2    | 0x0028  | varies |
| <a href="#">LEDC_CH2_HPOINT_REG</a>  | High point register for channel 2         | 0x002C  | R/W    |
| <a href="#">LEDC_CH2_DUTY_REG</a>    | Initial duty cycle register for channel 2 | 0x0030  | R/W    |
| <a href="#">LEDC_CH2_CONF1_REG</a>   | Configuration register 1 for channel 2    | 0x0034  | R/W/SC |
| <a href="#">LEDC_CH3_CONFO_REG</a>   | Configuration register 0 for channel 3    | 0x003C  | varies |
| <a href="#">LEDC_CH3_HPOINT_REG</a>  | High point register for channel 3         | 0x0040  | R/W    |
| <a href="#">LEDC_CH3_DUTY_REG</a>    | Initial duty cycle register for channel 3 | 0x0044  | R/W    |
| <a href="#">LEDC_CH3_CONF1_REG</a>   | Configuration register 1 for channel 3    | 0x0048  | R/W/SC |
| <a href="#">LEDC_CH4_CONFO_REG</a>   | Configuration register 0 for channel 4    | 0x0050  | varies |
| <a href="#">LEDC_CH4_HPOINT_REG</a>  | High point register for channel 4         | 0x0054  | R/W    |
| <a href="#">LEDC_CH4_DUTY_REG</a>    | Initial duty cycle register for channel 4 | 0x0058  | R/W    |
| <a href="#">LEDC_CH4_CONF1_REG</a>   | Configuration register 1 for channel 4    | 0x005C  | R/W/SC |
| <a href="#">LEDC_CH5_CONFO_REG</a>   | Configuration register 0 for channel 5    | 0x0064  | varies |
| <a href="#">LEDC_CH5_HPOINT_REG</a>  | High point register for channel 5         | 0x0068  | R/W    |
| <a href="#">LEDC_CH5_DUTY_REG</a>    | Initial duty cycle register for channel 5 | 0x006C  | R/W    |
| <a href="#">LEDC_CH5_CONF1_REG</a>   | Configuration register 1 for channel 5    | 0x0070  | R/W/SC |
| <a href="#">LEDC_CH6_CONFO_REG</a>   | Configuration register 0 for channel 6    | 0x0078  | varies |
| <a href="#">LEDC_CH6_HPOINT_REG</a>  | High point register for channel 6         | 0x007C  | R/W    |
| <a href="#">LEDC_CH6_DUTY_REG</a>    | Initial duty cycle register for channel 6 | 0x0080  | R/W    |
| <a href="#">LEDC_CH6_CONF1_REG</a>   | Configuration register 1 for channel 6    | 0x0084  | R/W/SC |
| <a href="#">LEDC_CH7_CONFO_REG</a>   | Configuration register 0 for channel 7    | 0x008C  | varies |
| <a href="#">LEDC_CH7_HPOINT_REG</a>  | High point register for channel 7         | 0x0090  | R/W    |
| <a href="#">LEDC_CH7_DUTY_REG</a>    | Initial duty cycle register for channel 7 | 0x0094  | R/W    |
| <a href="#">LEDC_CH7_CONF1_REG</a>   | Configuration register 1 for channel 7    | 0x0098  | R/W/SC |
| <a href="#">LEDC_TIMER0_CONF_REG</a> | Timer 0 configuration register            | 0x00A0  | varies |
| <a href="#">LEDC_TIMER1_CONF_REG</a> | Timer 1 configuration register            | 0x00A8  | varies |
| <a href="#">LEDC_TIMER2_CONF_REG</a> | Timer 2 configuration register            | 0x00B0  | varies |
| <a href="#">LEDC_TIMER3_CONF_REG</a> | Timer 3 configuration register            | 0x00B8  | varies |



| Name                                    | Description                                | Address | Access   |
|---|--|---------|----------|
| <a href="#">LEDC_CHO_GAMMA_CONF_REG</a> | LEDC channel 0 gamma config register       | 0x0100  | varies   |
| <a href="#">LEDC_CH1_GAMMA_CONF_REG</a> | LEDC channel 1 gamma config register       | 0x0104  | varies   |
| <a href="#">LEDC_CH2_GAMMA_CONF_REG</a> | LEDC channel 2 gamma config register       | 0x0108  | varies   |
| <a href="#">LEDC_CH3_GAMMA_CONF_REG</a> | LEDC channel 3 gamma config register       | 0x010C  | varies   |
| <a href="#">LEDC_CH4_GAMMA_CONF_REG</a> | LEDC channel 4 gamma config register       | 0x0110  | varies   |
| <a href="#">LEDC_CH5_GAMMA_CONF_REG</a> | LEDC channel 5 gamma config register       | 0x0114  | varies   |
| <a href="#">LEDC_CH6_GAMMA_CONF_REG</a> | LEDC channel 6 gamma config register       | 0x0118  | varies   |
| <a href="#">LEDC_CH7_GAMMA_CONF_REG</a> | LEDC channel 7 gamma config register       | 0x011C  | varies   |
| <a href="#">LEDC_EVT_TASK_ENO_REG</a>   | LEDC event task enable bit register 0      | 0x0120  | R/W      |
| <a href="#">LEDC_EVT_TASK_EN1_REG</a>   | LEDC event task enable bit register 1      | 0x0124  | R/W      |
| <a href="#">LEDC_EVT_TASK_EN2_REG</a>   | LEDC event task enable bit register 2      | 0x0128  | R/W      |
| <a href="#">LEDC_TIMER0_CMP_REG</a>     | LEDC timer 0 compare value register        | 0x0140  | R/W      |
| <a href="#">LEDC_TIMER1_CMP_REG</a>     | LEDC timer 1 compare value register        | 0x0144  | R/W      |
| <a href="#">LEDC_TIMER2_CMP_REG</a>     | LEDC timer 2 compare value register        | 0x0148  | R/W      |
| <a href="#">LEDC_TIMER3_CMP_REG</a>     | LEDC timer 3 compare value register        | 0x014C  | R/W      |
| <a href="#">LEDC_CONF_REG</a>           | LEDC global configuration register         | 0x0170  | R/W      |
| <b>Status Register</b>                  |  |         |          |
| <a href="#">LEDC_CHO_DUTY_R_REG</a>     | Current duty cycle register for channel 0  | 0x0010  | RO       |
| <a href="#">LEDC_CH1_DUTY_R_REG</a>     | Current duty cycle register for channel 1  | 0x0024  | RO       |
| <a href="#">LEDC_CH2_DUTY_R_REG</a>     | Current duty cycle register for channel 2  | 0x0038  | RO       |
| <a href="#">LEDC_CH3_DUTY_R_REG</a>     | Current duty cycle register for channel 3  | 0x004C  | RO       |
| <a href="#">LEDC_CH4_DUTY_R_REG</a>     | Current duty cycle register for channel 4  | 0x0060  | RO       |
| <a href="#">LEDC_CH5_DUTY_R_REG</a>     | Current duty cycle register for channel 5  | 0x0074  | RO       |
| <a href="#">LEDC_CH6_DUTY_R_REG</a>     | Current duty cycle register for channel 6  | 0x0088  | RO       |
| <a href="#">LEDC_CH7_DUTY_R_REG</a>     | Current duty cycle register for channel 7  | 0x009C  | RO       |
| <a href="#">LEDC_TIMER0_VALUE_REG</a>   | Timer 0 current counter value register     | 0x00A4  | RO       |
| <a href="#">LEDC_TIMER1_VALUE_REG</a>   | Timer 1 current counter value register     | 0x00AC  | RO       |
| <a href="#">LEDC_TIMER2_VALUE_REG</a>   | Timer 2 current counter value register     | 0x00B4  | RO       |
| <a href="#">LEDC_TIMER3_VALUE_REG</a>   | Timer 3 current counter value register     | 0x00BC  | RO       |
| <a href="#">LEDC_TIMER0_CNT_CAP_REG</a> | LEDC timer 0 captured count value register | 0x0150  | RO       |
| <a href="#">LEDC_TIMER1_CNT_CAP_REG</a> | LEDC timer 1 captured count value register | 0x0154  | RO       |
| <a href="#">LEDC_TIMER2_CNT_CAP_REG</a> | LEDC timer 2 captured count value register | 0x0158  | RO       |
| <a href="#">LEDC_TIMER3_CNT_CAP_REG</a> | LEDC timer 3 captured count value register | 0x015C  | RO       |
| <b>Interrupt Register</b>               |  |         |          |
| <a href="#">LEDC_INT_RAW_REG</a>        | Interrupt raw status register              | 0x00C0  | R/WTC/SS |
| <a href="#">LEDC_INT_ST_REG</a>         | Interrupt masked status register           | 0x00C4  | RO       |
| <a href="#">LEDC_INT_ENA_REG</a>        | Interrupt enable register                  | 0x00C8  | R/W      |
| <a href="#">LEDC_INT_CLR_REG</a>        | Interrupt clear register                   | 0x00CC  | WT       |
| <b>Version Register</b>                 |  |         |          |
| <a href="#">LEDC_DATE_REG</a>           | Version control register                   | 0x0174  | R/W      |

## 50.9 Registers

The addresses in this section are relative to LED PWM Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).



Register 50.1. LEDC\_CH $n$ \_CONFO\_REG ( $n$ : 0-7) (0x0000+0x14\* $n$ )

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |   |    |    |   |                              |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---|----|----|---|------------------------------|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | LEDC_OVF_CNT_RESET_CH <sub>n</sub><br>LEDC_OVF_CNT_EN_CH <sub>n</sub> |    |    |   | LEDC_OVF_NUM_CH <sub>n</sub> |   |   |   | LEDC_PARA_UP_CH <sub>n</sub><br>LEDC_IDLE_LV_CH <sub>n</sub><br>LEDC_SIG_OUT_EN_CH <sub>n</sub><br>LEDC_TIMER_SEL_CH <sub>n</sub> |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 17 | 16  | 15 | 14 |   |                              |   |   | 5 | 4   | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0   | 0  | 0  | 0 | 0                            | 0 | 0 | 0 | 0   | 0 | 0 | 0 | Reset |

**LEDC\_TIMER\_SEL\_CH $n$**  Configures which timer is channel  $n$  selected.

- 0: Select Timer 0
  - 1: Select Timer 1
  - 2: Select Timer 2
  - 3: Select Timer 3
- (R/W)

**LEDC\_SIG\_OUT\_EN\_CH $n$**  Configures whether to enable signal output on channel  $n$ .

- 0: Signal output disable
  - 1: Signal output enable
- (R/W)

**LEDC\_IDLE\_LV\_CH $n$**  Configures the output value when channel  $n$  is inactive. Valid only when [LEDC\\_SIG\\_OUT\\_EN\\_CH \$n\$](#)  is 0.

- 0: Output level is low
  - 1: Output level is high
- (R/W)

**LEDC\_PARA\_UP\_CH $n$**  Configures whether to update [LEDC\\_HPOINT\\_CH \$n\$](#) , [LEDC\\_DUTY\\_START\\_CH \$n\$](#) , [LEDC\\_SIG\\_OUT\\_EN\\_CH \$n\$](#) , [LEDC\\_TIMER\\_SEL\\_CH \$n\$](#) , [LEDC\\_OVF\\_CNT\\_EN\\_CH \$n\$](#)  fields and duty cycle range configurations for channel  $n$ , and will be automatically cleared by hardware.

- 0: Invalid. No effect
  - 1: Update
- (WT)

**LEDC\_OVF\_NUM\_CH $n$**  Configures the maximum times of overflow minus 1. The [LEDC\\_OVF\\_CNT\\_CH \$n\$ \\_INT](#) interrupt will be triggered when channel  $n$  overflows for ([LEDC\\_OVF\\_NUM\\_CH \$n\$](#)  + 1) times. (R/W)

**LEDC\_OVF\_CNT\_EN\_CH $n$**  Configures whether to enable the [ovf\\_cnt](#) of channel  $n$ .

- 0: Disable
  - 1: Enable
- (R/W)

Continued on the next page...



**Register 50.4. LEDC\_CH $n$ \_CONF1\_REG ( $n$ : 0-7) (0x000C+0x14\* $n$ )**

Diagram illustrating the structure of the LEDC\_DUTY\_START\_CHn register. The register is 32 bits wide. Bit 31 is labeled LEDC\_DUTY\_START\_CHn. Bits 30-0 are labeled (reserved). Bit 0 is labeled Reset.

**LEDC\_DUTY\_START\_CH<sub>n</sub>** Configures whether the duty cycle fading configurations take effect.

0: Not take effect

1: Take effect

(R/W/SC)

**Register 50.5. LEDC\_TIMER<sub>x</sub>\_CONF\_REG (x: 0-3) (0x00A0+0x8\*x)**

|            |  |  |  |  |    |  |  |  |  |  |    |    |    |    |   |  |  |  |  |  |  |  |  |  |   |  |  |  |   |                                 |  |  |  |   |       |  |  |  |  |                                   |  |  |  |  |       |  |  |  |  |
|------------|--|--|--|--|----|--|--|--|--|--|----|----|----|----|---|--|--|--|--|--|--|--|--|--|---|--|--|--|---|---------------------------------|--|--|--|---|-------|--|--|--|--|-----------------------------------|--|--|--|--|-------|--|--|--|--|
| (reserved) |  |  |  |  |    |  |  |  |  | LEDC_TIMER <del>×</del> _PARA_UP<br>(reserved) |    |    |    |    |   |  |  |  |  | LEDC_TIMER <del>×</del> _RST<br>LEDC_TIMER <del>×</del> _PAUSE |  |  |  |  |   |  |  |  |   | LEDC_CLK_DIV_TIMER <del>×</del> |  |  |  |   |       |  |  |  |  | LEDC_TIMER <del>×</del> _DUTY_RES |  |  |  |  |       |  |  |  |  |
| 31         |  |  |  |  | 27 |  |  |  |  | 26   | 25 | 24 | 23 | 22 |   |  |  |  |  |  |  |  |  |  |   |  |  |  | 5 |                                 |  |  |  | 4 | 0     |  |  |  |  |                                   |  |  |  |  |       |  |  |  |  |
| 0          |  |  |  |  | 0  |  |  |  |  | 0  |    |    |    |    | 0 |  |  |  |  | 0  |  |  |  |  | 0 |  |  |  |   | 0                               |  |  |  |   | 0x000 |  |  |  |  | 0x0                               |  |  |  |  | Reset |  |  |  |  |

**LEDC\_TIMERx\_DUTY\_RES** Configures the bit width of the counter in timer **x**. Valid values are 1 to 20. (R/W)

**LEDC\_CLK\_DIV\_TIMER $x$**  Configures the divisor for the divider in timer  $x$ .

The least significant eight bits represent the fractional part. The most significant ten bits represent the integer part. (R/W)

**LEDC\_TIMER<sub>x</sub>\_PAUSE** Configures whether to pause the counter in timer *x*.

0: Normal

1: Pause

(R/W)

**LEDC\_TIMER $x$ \_RST** Configures whether to reset timer  $x$ . The counter will show 0 after reset.

0: Not reset

1: Reset

(R/W)

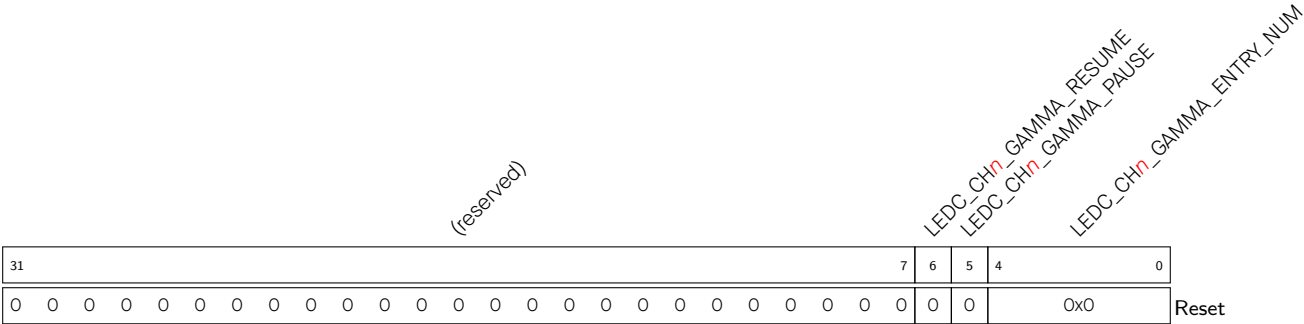
**LEDC\_TIMERx\_PARA\_UP** Configures whether to update LEDC\_CLK\_DIV\_TIMERx and LEDC\_TIMERx DUTY RES.

0: Invalid. No effect

1: Update

(WT)

Register 50.6. LEDC\_CHn\_GAMMA\_CONF\_REG (n: 0-7) (0x0100+0x4\*n)



**LEDC\_CHn\_GAMMA\_ENTRY\_NUM** Configures the number of duty cycle fading ranges for LEDC channel n. (R/W)

**LEDC\_CHn\_GAMMA\_PAUSE** Configures whether to pause duty cycle fading of LEDC channel n.

0: Invalid. No effect

1: Pause

(WT)

**LEDC\_CHn\_GAMMA\_RESUME** Configures whether to resume duty cycle fading of LEDC channel n.

0: Invalid. No effect

1: Resume

(WT)

### Register 50.7. LEDC\_EVT\_TASK\_EN0\_REG (0x0120)

[illegible]

**LEDC\_EVT\_DUTY\_CHNG\_END\_CH $n$ \_EN ( $n$ : 0-7)** Configures whether to enable the LEDC\_EVT\_DUTY\_CHNG\_END\_CH $n$  event.

0: Disable

1: Enable

(R/W)

**LEDC\_EVT\_OVF\_CNT\_PLS\_CH $n$ \_EN ( $n$ : 0-7)** Configures whether to enable the LEDC\_EVT\_OVF\_CNT\_PLS\_CH $n$  event.

0: Disable

1: Enable

(R/W)

**LEDC\_EVT\_TIME\_OVF\_TIMER<sub>x</sub>\_EN (x: 0-3)** Configures whether to enable the LEDC\_EVT\_TIME\_OVF\_TIMER<sub>x</sub> event.

0: Disable

1: Enable

(R/W)

**LEDC\_EVT\_TIMER<sub>x</sub>\_CMP\_EN (x: 0-3)** Configures whether to enable the LEDC\_EVT\_TIMER<sub>x</sub>\_CMP event.

0: Disable

1: Enable

(R/W)

**LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH $n$ \_EN ( $n$ : 0-7)** Configures whether to enable the LEDC\_TASK\_DUTY\_SCALE\_UPDATE\_CH $n$  task.

0: Disable

1: Enable

(R/W)

### Register 50.8. LEDC\_EVT\_TASK\_EN1\_REG (0x0124)

[illegible]

|  |            |         |    |        |
|--|------------|---------|----|--------|
| <b>LEDC_TASK_TIMER<sub>x</sub>_RES_UPDATE_EN</b> ( <b>x</b> : 0-3) | Configures | whether | to | enable |
| LEDC_TASK_TIMER <sub>x</sub> _RES_UPDATE task.                     |            |         |    |        |
| 0: Disable   |            |         |    |        |
| 1: Enable  |            |         |    |        |
| (R/W)  |            |         |    |        |

**LEDC\_TASK\_TIMER<sub>x</sub>\_CAP\_EN (x: 0-3)** Configures whether to enable LEDC\_TASK\_TIMER<sub>x</sub>\_CAP task.

0: Disable

1: Enable

(R/W)

|  |            |         |    |        |
|--|------------|---------|----|--------|
| <b>LEDC_TASK_SIG_OUT_DIS_CH<math>n</math>_EN (<math>n</math>: 0-7)</b> | Configures | whether | to | enable |
| LEDC_TASK_SIG_OUT_DIS_CH $n$ task.                                     |            |         |    |        |
| 0: Disable   |            |         |    |        |
| 1: Enable  |            |         |    |        |
| (R/W)  |            |         |    |        |

|  |            |         |    |        |
|--|------------|---------|----|--------|
| <b>LEDC_TASK_OVF_CNT_RST_CH</b> <i>n</i> _EN ( <i>n</i> : 0-7) | Configures | whether | to | enable |
| LEDC_TASK_OVF_CNT_RST_CH <i>n</i> task.                        |            |         |    |        |
| 0: Disable   |            |         |    |        |
| 1: Enable  |            |         |    |        |
| (R/W)  |            |         |    |        |

**LEDC\_TASK\_TIMER<sub>x</sub>\_RST\_EN (x: 0-3)** Configures whether to enable LEDC\_TASK\_TIMER<sub>x</sub>\_RST task.

0: Disable

1: Enable

(R/W)

**LEDC\_TASK\_TIMER<sub>x</sub>\_PAUSE\_RESUME\_EN (x: 0-3)** Configures whether to enable LEDC\_TASK\_TIMER<sub>x</sub>\_PAUSE and LEDC\_TASK\_TIMER<sub>x</sub>\_RESUME task.

0: Disable

1: Enable

(R/W)

### Register 50.9. LEDC\_EVT\_TASK\_EN2\_REG (0x0128)

|            |   |   |   |   |   |   |    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|----|--|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |    | LDC_TASK_GAMMA_RESUME_CH7_EN<br>LDC_TASK_GAMMA_RESUME_CH6_EN<br>LDC_TASK_GAMMA_RESUME_CH5_EN<br>LDC_TASK_GAMMA_RESUME_CH4_EN<br>LDC_TASK_GAMMA_RESUME_CH3_EN<br>LDC_TASK_GAMMA_RESUME_CH2_EN<br>LDC_TASK_GAMMA_PAUSE_CH1_EN<br>LDC_TASK_GAMMA_PAUSE_CH0_EN<br>LDC_TASK_GAMMA_PAUSE_CH7_EN<br>LDC_TASK_GAMMA_PAUSE_CH6_EN<br>LDC_TASK_GAMMA_PAUSE_CH5_EN<br>LDC_TASK_GAMMA_PAUSE_CH4_EN<br>LDC_TASK_GAMMA_PAUSE_CH3_EN<br>LDC_TASK_GAMMA_PAUSE_CH2_EN<br>LDC_TASK_GAMMA_RESTART_CH1_EN<br>LDC_TASK_GAMMA_RESTART_CH0_EN |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|            |   |   |   |   |   |   |    |  |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31         |   |   |   |   |   |   | 24 | 23   | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |

|   |            |         |    |        |
|---|------------|---------|----|--------|
| <b>LEDC_TASK_GAMMA_RESTART_CH</b> <i>n</i> <b>_EN</b> ( <i>n</i> : 0-7) | Configures | whether | to | enable |
| LEDC_TASK_GAMMA_RESTART_CH <i>n</i> task.                               |            |         |    |        |
| 0: Disable  |            |         |    |        |
| 1: Enable   |            |         |    |        |
| (R/W)   |            |         |    |        |

|   |            |         |    |        |
|---|------------|---------|----|--------|
| <b>LEDC_TASK_GAMMA_PAUSE_CH</b> <i>n</i> <b>_EN</b> ( <i>n</i> : 0-7) | Configures | whether | to | enable |
| LEDC_TASK_GAMMA_PAUSE_CH <i>n</i> task.                               |            |         |    |        |
| 0: Disable  |            |         |    |        |
| 1: Enable   |            |         |    |        |
| (R/W)   |            |         |    |        |

|  |  |
|--|--|
| LEDC_TASK_GAMMA_RESUME_CH $n$ _EN ( $n$ : 0-7) | Configures whether to enable LEDC_TASK_GAMMA_RESUME_CH $n$ task. |
| 0: Disable                                     |  |
| 1: Enable                                      |  |
| (R/W)  |  |

**Register 50.10. LEDC\_TIMER<sub>x</sub>\_CMP\_REG (x: 0-3) (0x0140+0x4\*x)**

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER_CMP |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 20             | 19    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              | 0x000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**LEDC\_TIMERx\_CMP** Configures the comparison value for LEDC timer *x*. (R/W)

### Register 50.11. LEDC\_CONF\_REG (0x0170)

|    |    |   |   |   |   |   |   |   |   |   |   |    |   |   |   |   |   |   |   |   |   |   |
|----|----|---|---|---|---|---|---|---|---|---|---|----|---|---|---|---|---|---|---|---|---|---|
| 31 | 30 |   |   |   |   |   |   |   |   |   |   | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEDC\_GAMMA\_RAM\_CLK\_EN (reserved) LEDC\_GAMMA\_RAM\_CLK\_EN\_CH7 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH6 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH5 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH4 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH3 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH2 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH1 LEDC\_GAMMA\_RAM\_CLK\_EN\_CH0

Reset

**LEDC\_GAMMA\_RAM\_CLK\_EN\_CH $n$  ( $n$ : 0-7)** Configures whether to open LEDC channel  $n$  gamma RAM clock gate.

0: Open the clock gate only when an application writes or reads LEDC channel *n* gamma RAM

1: Force open the clock gate for LEDC channel *n* gamma RAM

(R/W)

**LEDC\_CLK\_EN** Configures whether to open the register clock gate.

0: Open the clock gate only when an application writes registers

1: Force open the clock gate for register

(R/W)

Register 50.12. LEDC\_CH $n$ \_DUTY\_R\_REG ( $n$ : 0-7) (0x0010+0x14\* $n$ )

Register structure for LEDC\_DUTY\_CHn\_R:

- Bits 31-25: (reserved)
- Bits 24-0: LEDC\_DUTY\_CHn\_R (Duty value, shown as 0x000000)
- Reset: Indicated at the bottom right of the register structure.

**LEDC\_DUTY\_CH $n$ \_R** Represents the current duty cycle of output signal on channel  $n$ . (RO)

**Register 50.13. LEDC\_TIMER<sub>x</sub>\_VALUE\_REG (x: 0-3) (0x00A4+0x8\*x)**

|                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER_CNT |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**LEDC\_TIMER $x$ \_CNT** Represents the current counter value of timer  $x$ . (RO)



**Register 50.14. LEDC\_TIMER $x$ \_CNT\_CAP\_REG ( $x$ : 0-3) (0x0150+0x4\* $x$ )**

|            |   |   |   |   |   |   |   |   |   |   |    |                                  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|----|----------------------------------|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |    | LEDC_TIMER <del>x</del> _CNT_CAP |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   | 20 | 19                               |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0x000                            |  |  |  |  |  |  |  |  |  |  |   | Reset |

**LEDC\_TIMER $x$ \_CNT\_CAP** Represents the captured LEDC timer  $x$  count value. (RO)

**Register 50.15. LEDC\_INT\_RAW\_REG (0x00C0)**

|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|--|--|--------------------------------|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH7_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH6_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH5_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH4_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH3_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH2_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH1_INT_RAW       |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH0_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH1_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH2_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH3_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH4_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH5_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_DUTY_CHNG_END_CH6_INT_RAW |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER3_OVF_INT_RAW        |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER2_OVF_INT_RAW        |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER1_OVF_INT_RAW        |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  | LEDC_TIMER0_OVF_INT_RAW        |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
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|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
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|            |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |
| </         |  |  |  |  |  |  |  |  |  |  |  |                                |  |  |  |  |  |  |  |  |  |  |  |

**LEDC\_TIMER $x$ \_OVF\_INT\_RAW ( $x$ : 0-3)** Raw status bit: The raw interrupt status of LEDC\_TIMER $x$ \_OVF\_INT. Triggered when the timer  $x$  has reached its maximum counter value. (R/WTC/SS)

**LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT\_RAW ( $n$ : 0-7)** Raw status bit: The raw interrupt status of LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT. Triggered when the fading of duty has finished. (R/WTC/SS)

**LEDC\_OVF\_CNT\_CH $n$ \_INT\_RAW ( $n$ : 0-7)** Raw status bit: The raw interrupt status of LEDC\_OVF\_CNT\_CH $n$ \_INT. Triggered when the ovf\_cnt has reached the value specified by LEDC\_OVF\_NUM\_CH $n$ . (R/WTC/SS)

## Register 50.16. LEDC\_INT\_ST\_REG (0x00C4)

|              |  |  |  |  |  |  |  |  |  |  |  |   |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--------------|--|--|--|--|--|--|--|--|--|--|--|---|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved)   |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH7_INT_ST<br>LEDC_OVF_CNT_CH6_INT_ST<br>LEDC_OVF_CNT_CH5_INT_ST<br>LEDC_OVF_CNT_CH4_INT_ST<br>LEDC_OVF_CNT_CH3_INT_ST<br>LEDC_OVF_CNT_CH2_INT_ST<br>LEDC_OVF_CNT_CH1_INT_ST<br>LEDC_DUTY_CHNG_END_CH0_INT_ST<br>LEDC_DUTY_CHNG_END_CH7_INT_ST<br>LEDC_DUTY_CHNG_END_CH6_INT_ST<br>LEDC_DUTY_CHNG_END_CH5_INT_ST<br>LEDC_DUTY_CHNG_END_CH4_INT_ST<br>LEDC_DUTY_CHNG_END_CH3_INT_ST<br>LEDC_TIMER3_OVF_INT_ST<br>LEDC_TIMER2_OVF_INT_ST<br>LEDC_TIMER1_OVF_INT_ST<br>LEDC_TIMER0_OVF_INT_ST |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 3120         |  |  |  |  |  |  |  |  |  |  |  | 19  | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 000000000000 |  |  |  |  |  |  |  |  |  |  |  | 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |   |   |       |

Reset

**LEDC\_TIMER $x$ \_OVF\_INT\_ST ( $x$ : 0-3)** Masked status bit: The masked interrupt status of LEDC\_TIMER $x$ \_OVF\_INT. Valid only when LEDC\_TIMER $x$ \_OVF\_INT\_ENA is set to 1. (RO)

**LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT\_ST ( $n$ : 0-7)** Masked status bit: The masked interrupt status of LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT. Valid only when LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT\_ENA is set to 1. (RO)

**LEDC\_OVF\_CNT\_CH $n$ \_INT\_ST ( $n$ : 0-7)** Masked status bit: The masked interrupt status of LEDC\_OVF\_CNT\_CH $n$ \_INT. Valid only when LEDC\_OVF\_CNT\_CH $n$ \_INT\_ENA is set to 1. (RO)

## Register 50.17. LEDC\_INT\_ENA\_REG (0x00C8)

|              |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
|--------------|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|
| (reserved)   |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH7_INT_ENA<br>LEDC_OVF_CNT_CH6_INT_ENA<br>LEDC_OVF_CNT_CH5_INT_ENA<br>LEDC_OVF_CNT_CH4_INT_ENA<br>LEDC_OVF_CNT_CH3_INT_ENA<br>LEDC_OVF_CNT_CH2_INT_ENA<br>LEDC_OVF_CNT_CH1_INT_ENA<br>LEDC_DUTY_CHNG_END_CH0_INT_ENA<br>LEDC_DUTY_CHNG_END_CH7_INT_ENA<br>LEDC_DUTY_CHNG_END_CH6_INT_ENA<br>LEDC_DUTY_CHNG_END_CH5_INT_ENA<br>LEDC_DUTY_CHNG_END_CH4_INT_ENA<br>LEDC_DUTY_CHNG_END_CH3_INT_ENA<br>LEDC_DUTY_CHNG_END_CH2_INT_ENA<br>LEDC_TIMER3_OVF_INT_ENA<br>LEDC_TIMER2_OVF_INT_ENA<br>LEDC_TIMER1_OVF_INT_ENA<br>LEDC_TIMER0_OVF_INT_ENA |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |
| 3120         |  |  |  |  |  |  |  |  |  |  |  | 19   | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |
| 000000000000 |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Reset        |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |

Reset

**LEDC\_TIMER $x$ \_OVF\_INT\_ENA ( $x$ : 0-3)** Enable bit: Write 1 to enable LEDC\_TIMER $x$ \_OVF\_INT. (R/W)

**LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT\_ENA ( $n$ : 0-7)** Enable bit: Write 1 to enable LEDC\_DUTY\_CHNG\_END\_CH $n$ \_INT. (R/W)

**LEDC\_OVF\_CNT\_CH $n$ \_INT\_ENA ( $n$ : 0-7)** Enable bit: Write 1 to enable LEDC\_OVF\_CNT\_CH $n$ \_INT. (R/W)

Register 50.18. LEDC\_INT\_CLR\_REG (0x00CC)

|                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |              |  |  |  |      |  |      |  |   |   |   |   |   |   |   |   |       |
|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--------------|--|--|--|------|--|------|--|---|---|---|---|---|---|---|---|-------|
| (reserved)     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LEDC_OVF_CNT_CH7_INT_CLR<br>LEDC_OVF_CNT_CH6_INT_CLR<br>LEDC_OVF_CNT_CH5_INT_CLR<br>LEDC_OVF_CNT_CH4_INT_CLR<br>LEDC_OVF_CNT_CH3_INT_CLR<br>LEDC_OVF_CNT_CH2_INT_CLR<br>LEDC_OVF_CNT_CH1_INT_CLR<br>LEDC_DUTY_CHNG_END_CH0_INT_CLR<br>LEDC_DUTY_CHNG_END_CH7_INT_CLR<br>LEDC_DUTY_CHNG_END_CH6_INT_CLR<br>LEDC_DUTY_CHNG_END_CH5_INT_CLR<br>LEDC_DUTY_CHNG_END_CH4_INT_CLR<br>LEDC_DUTY_CHNG_END_CH3_INT_CLR<br>LEDC_DUTY_CHNG_END_CH2_INT_CLR<br>LEDC_TIMER3_OVF_INT_CLR<br>LEDC_TIMER2_OVF_INT_CLR<br>LEDC_TIMER1_OVF_INT_CLR<br>LEDC_TIMER0_OVF_INT_CLR |    |              |  |  |  |      |  |      |  |   |   |   |   |   |   |   |   |       |
| 3120           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 19   | 18 | 171615141312 |  |  |  | 1110 |  | 98   |  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 00000000000000 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0  | 00000000     |  |  |  | 00   |  | 0000 |  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**LEDC\_TIMER<sub>x</sub>\_OVF\_INT\_CLR (x: 0-3)** Clear bit: Write 1 to clear LEDC\_TIMER<sub>x</sub>\_OVF\_INT. (WT)

**LEDC\_DUTY\_CHNG\_END\_CH<sub>n</sub>\_INT\_CLR (n: 0-7)** Clear bit: Write 1 to clear LEDC\_DUTY\_CHNG\_END\_CH<sub>n</sub>\_INT. (WT)

**LEDC\_OVF\_CNT\_CH<sub>n</sub>\_INT\_CLR (n: 0-7)** Clear bit: Write 1 to clear LEDC\_OVF\_CNT\_CH<sub>n</sub>\_INT. (WT)

Register 50.19. LEDC\_DATE\_REG (0x0174)

|            |    |    |   |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------|----|----|---|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| (reserved) |    |    |   | LEDC_LEDC_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31         | 28 | 27 |   |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0          | 0  | 0  | 0 | 0x2303070      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**LEDC\_LEDC\_DATE** Configures the version. (R/W)

## Chapter 51

# Motor Control PWM (MCPWM)

## 51.1 Overview

The **Motor Control Pulse Width Modulator** (MCPWM) peripheral is intended for motor and power control. It provides six PWM outputs that can be set up to operate in several topologies. One common topology uses a pair of PWM outputs driving an H-bridge to control motor rotation speed and rotation direction.

The MCPWM can be divided into five main modules: PWM timers, PWM operators, Capture module, Event Task Matrix (ETM) module, and Fault Detection module. Each PWM timer provides timing references that can either run freely or be synced to other timers or external sources. Each PWM operator has all the necessary control resources to generate waveform pairs for one PWM channel. The Capture module is used for systems that need to accurately time external events. The ETM module responds to tasks received by the MCPWM, generating corresponding events depending on the state of motion. The Fault Detection module is used to capture external faults, allowing the system to respond by choice.

ESP32-P4 has two MCPWM peripherals, which are MCPWM0 and MCPWM1.

## 51.2 Features

An MCPWM peripheral has one clock divider (prescaler), three PWM timers, three PWM operators, a Capture module, an ETM module, and a Fault Detection module. MCPWM's core clock can be selected from three clock sources: PLL\_F160M\_CLK, XTAL\_CLK, and RC\_FAST\_CLK (configured by the HP\_SYS\_CLKRST\_MCPWM $n$ \_CLK\_SRC\_SEL field of the [HP\\_SYS\\_CLKRST\\_PERI\\_CLK\\_CTRL20\\_REG](#) register). Figure 51.2-1 shows the submodules inside MCPWM and the signals on the interface. PWM timers are used for generating timing references. The PWM operators generate the desired waveform based on the timing references. Any PWM operator can be configured to use the timing references of any PWM timers. Different PWM operators can use the same PWM timer's timing reference to generate PWM signals, or different PWM timers' values to generate separate PWM signals. Different PWM timers can also be synchronized together.

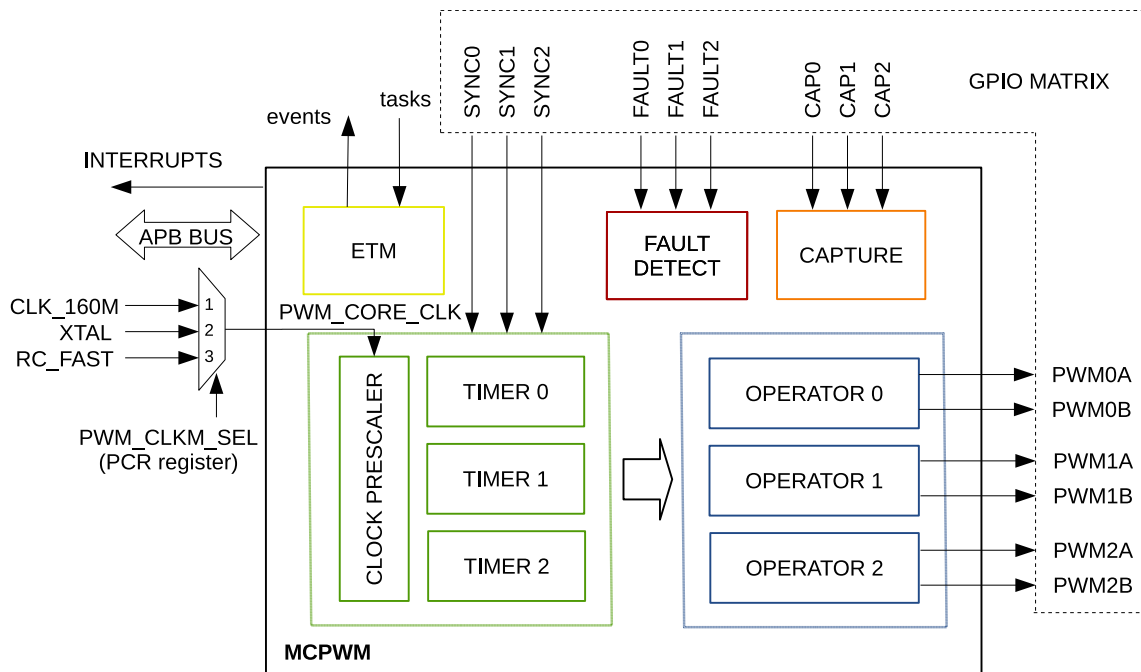


Figure 51.2-1. MCPWM Module Overview

Below is an overview of the submodules' functionality in Figure 51.2-1:

- PWM Timers 0, 1, and 2:
  - Every PWM timer has a dedicated 8-bit clock prescaler.
  - The 16-bit counter in the PWM timer can work in Count-Up Mode, Count-Down Mode, or Count-Up-Down Mode.
  - A hardware sync or software sync can trigger a reload on the PWM timer with a phase register. It will also trigger the prescaler's restart, so that the timer's clock can also be synced. The source of the hard sync can come from any GPIO or any other PWM timer's sync\_out. The source of the soft sync comes from writing toggle value to the `MCPWM_TIMERn_SYNC_SW` bit.
- PWM Operators 0, 1, and 2:
  - Every PWM operator has two PWM outputs: PWMxA and PWMxB. They can work independently, in symmetric or asymmetric configurations.
  - The control of the PWM signal can be updated asynchronously.
  - Configurable dead time on rising and falling edges; each set up independently.
  - All events can trigger CPU interrupts.
  - Modulating of PWM output by high-frequency carrier signals, useful when gate drivers are insulated with a transformer.
  - Period, time stamps, and important control registers have shadow registers with flexible updating methods.
- Fault Detection Module:
  - Programmable fault handling in both cycle-by-cycle mode and one-shot mode.

- A fault condition can force the PWM output to either high or low logic levels.
- Capture Module:
  - Clock of the capture module is the same as MCPWM's core clock.
  - Speed measurement of rotating machinery.
  - Measurement of elapsed time between position sensor pulses
  - Period and duty cycle measurement of pulse train signals
  - Decoding current or voltage amplitude derived from duty-cycle-encoded signals of current/voltage sensors
  - Three individual capture channels, each of which with a time-stamp register (32-bit)
  - Selection of edge polarity and prescaling of input capture signals
  - The capture timer can sync with a PWM timer or external signals.
  - Interrupt on each of the three capture channels
- ETM Module:
  - Generation of different events depending on the different running states of each timer and operator.
  - Each timer and operator responds to its corresponding task and automatically performs the corresponding operation.
  - Each event and task can be enabled independently. When an event is not enabled, the corresponding event will not be generated. When a task is not enabled, the corresponding task will not be responded to.

## 51.3 Modules

### 51.3.1 Overview

The key modules in each MCPWM are timer module, operator module, fault detection module, capture module, and ETM module. See their functions in the following sections.

#### 51.3.1.1 Timer Module

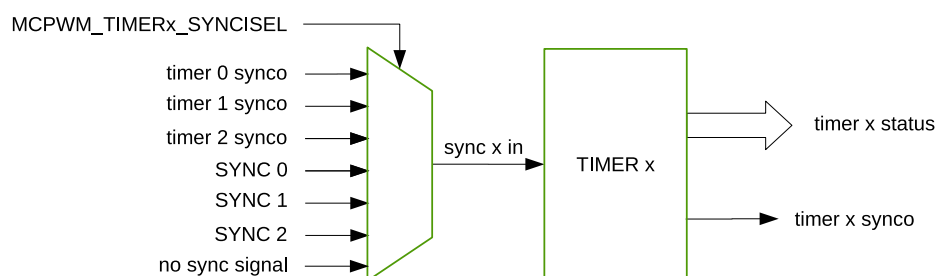


Figure 51.3-1. Timer Module

This module generates a timer, which can count at a specified period. It can work in Count-Up Mode, Count-Down Mode, or Count-Up-Down Mode. It supports different synchronization input sources (a total of seven optional input sources) for reloading the count value and direction, allowing synchronization among multiple timers. Furthermore, it provides synchronization output options (a total of four optional output sources) for use by other timers.

The timer $x$  status in the figure represents the timer status output by the timer module, such as the counting mode, and count value equal to zero or period.

#### 51.3.1.2 Operator Module

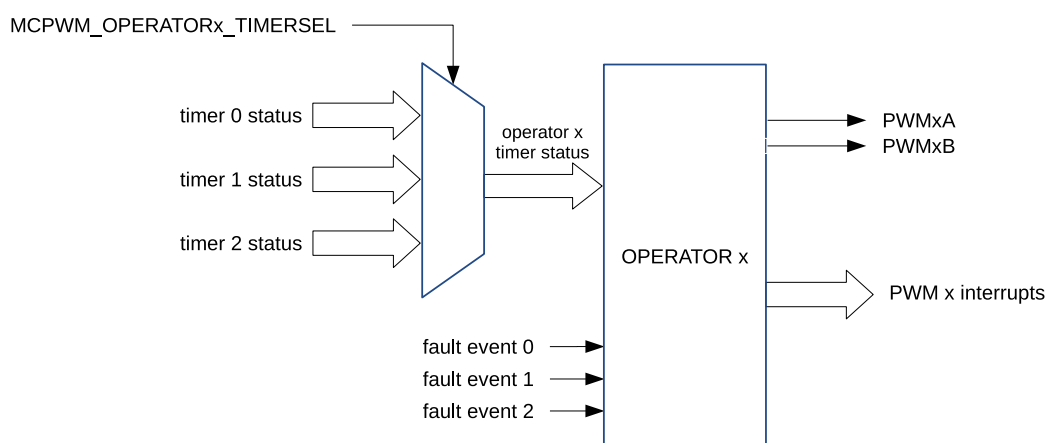


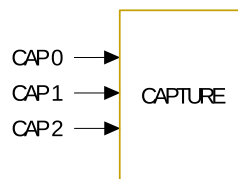
Figure 51.3-2. Operator Module

A PWM operator contains a PWM generator, a dead time generator, and a PWM carrier module. Their functions are shown in Table 51.3-1.

**Table 51.3-1. Functions of Each Submodule in the Operator Module**

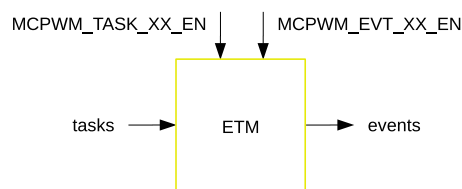
| Submodule           | Functions   |
|---------------------|---|
| PWM Generator       | Generate PWM signals according to the configured duty cycle and waveform.   |
| Dead Time Generator | Choose to add dead time to the rising and falling edges of the PWM signal generated by the PWM generator (add delays to the rising and falling edges), and perform operations such as inversion.  |
| PWM Carrier         | Choose to add a carrier to the PWM signal generated by the dead time generator. The carrier frequency and the first pulse duration of the PWM waveform after adding the carrier can be configured.  |
| Fault Detector      | Detect faults and generate corresponding fault events, respond to fault events based on the specified interval mode (one-shot mode or cycle-by-cycle mode), and when a fault event occurs, take action on the PWM signal generated by the PWM carrier in the specified way. |

### 51.3.1.3 Capture Module

**Figure 51.3-3. Capture Module**

The module contains a timer that can be synchronized. When the input capture signal is valid, the count value of the timer is captured.

### 51.3.1.4 ETM Module

**Figure 51.3-4. ETM Module**

The module responds to received tasks, or generate and output events. Each event and task can be enabled independently.



## 51.3.2 PWM Timer Module

MCPWM has three PWM timer modules. Any of them can determine the necessary event timing for any of the three PWM operator modules. By using the synchronization signals from the GPIO matrix, built-in synchronization logic allows multiple PWM timer modules in one or more MCPWM peripherals to work together as a system.

### 51.3.2.1 Configurations of the PWM Timer Module

Users can configure the following functions of the PWM timer module:

- Control how often events occur by specifying the PWM timer frequency or period.
- Configure a particular PWM timer to synchronize phases with other PWM timers or modules.
- Configure the following timer counting modes: count-up, count-down, count-up-down.
- Change the rate of the PWM timer clock (PT\_CLK) with a prescaler. Each timer has its own prescaler configured with `MCPWM_TIMER $n$ _PRESCALE` of the register `MCPWM_TIMER0_CFGO_REG`. The PWM timer increments or decrements at a slower pace, depending on the setting of this field. The new `MCPWM_TIMER $n$ _PRESCALE` configuration value will take effect when the timer stops and starts counting again.

### 51.3.2.2 PWM Timer's Working Modes and Timing Event Generation

The PWM timer has three working modes, selected by the PWM $x$  timer mode field:

- Count-Up Mode:  
The PWM timer increments from zero until reaching the value configured in the period field. Once done, the PWM timer returns to zero and starts increasing again. PWM period = the value of the period field + 1.  
Note: The period field is `MCPWM_TIMER $n$ _PERIOD` ( $x = 0, 1, 2$ ), i.e., `MCPWM_TIMER0_PERIOD`, `MCPWM_TIMER1_PERIOD`, `MCPWM_TIMER2_PERIOD`.
- Count-Down Mode:  
The PWM timer decrements to zero, starting from the value configured in the period field. Once done, the PWM timer returns to the period value and starts decrementing again. In this case, the PWM period = the value of period field + 1.
- Count-Up-Down Mode:  
This is a combination of the two modes mentioned above. The PWM timer starts increasing from zero until the period value is reached. Then, the timer decreases back to zero. The PWM timer cycles incrementally and decrementally in this mode. The PWM period = the value of the period field  $\times$  2.

Figures 51.3-5 to 51.3-8 show PWM timer waveforms in different modes, including timer behavior during synchronization events. In Count-Up mode, the counting direction after synchronization is always counting up. In Count-Down mode, the counting direction after synchronization is always counting down. In Count-Up-Down Mode, the counting direction after synchronization can be chosen by setting the `MCPWM_TIMER $n$ _PHASE_DIRECTION`.

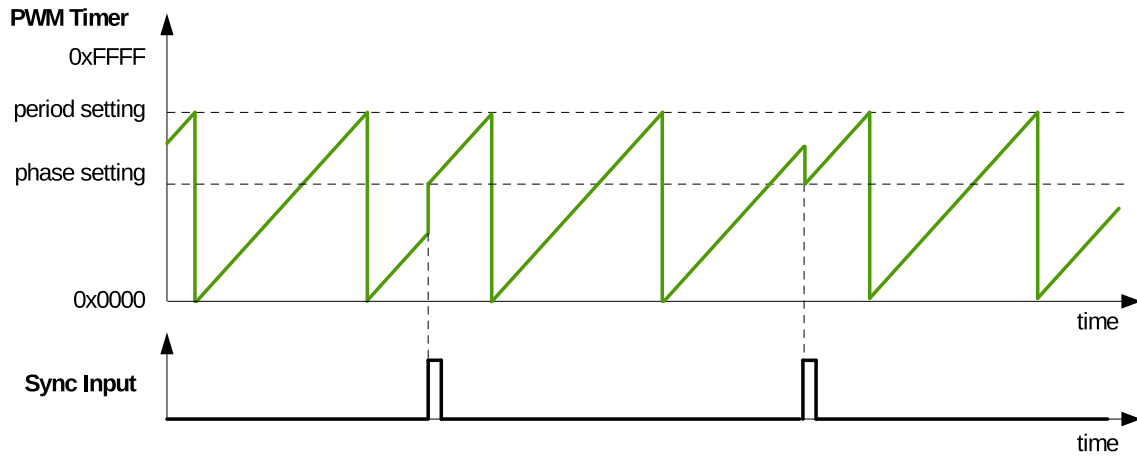


Figure 51.3-5. Count-Up Mode Waveform

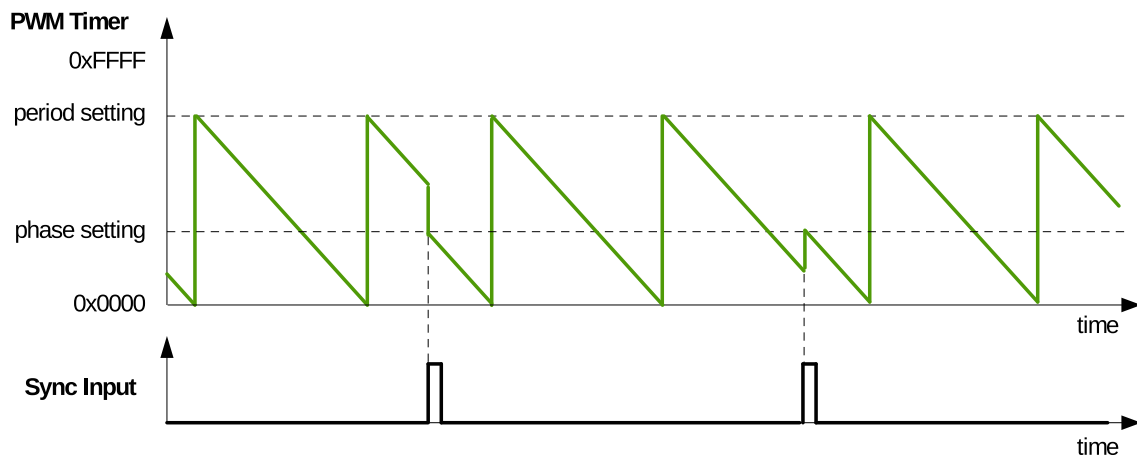


Figure 51.3-6. Count-Down Mode Waveforms

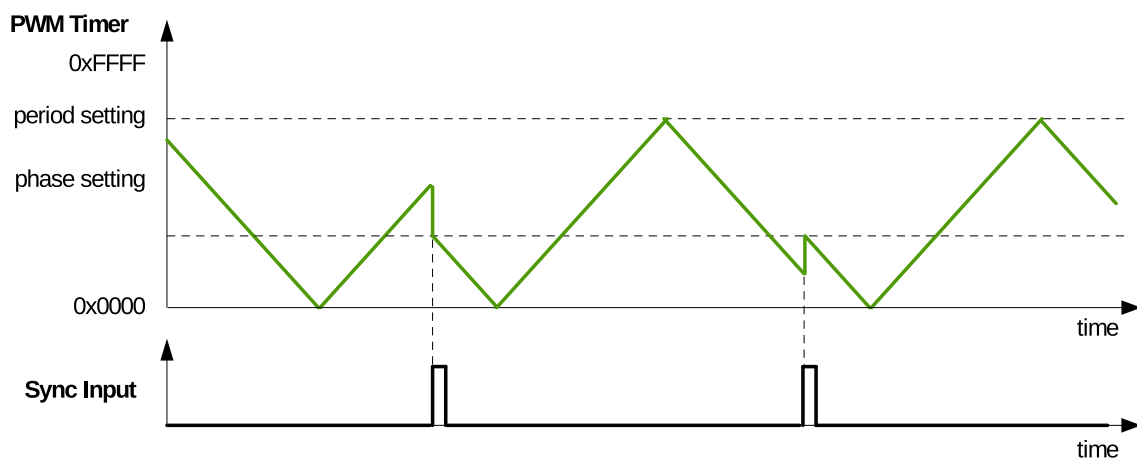


Figure 51.3-7. Count-Up-Down Mode Waveforms, Count-Down at Synchronization Event

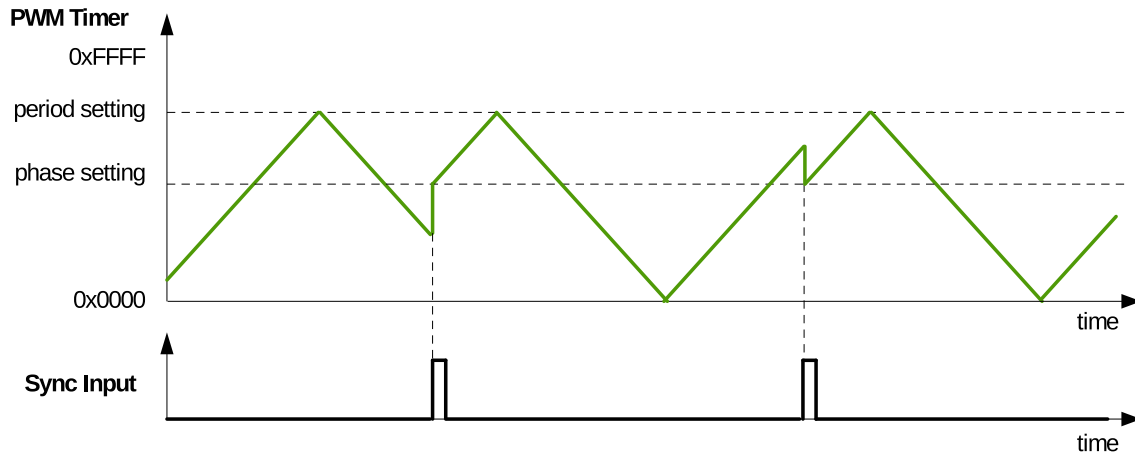


Figure 51.3-8. Count-Up-Down Mode Waveforms, Count-Up at Synchronization Event

When the PWM timer is running, it generates the following timing events periodically and automatically:

- UTEP: The timing event generated when the PWM timer's value is equal to the value of the period field (`MCPWM_TIMER $n$ _PERIOD`) and when the PWM timer is increasing.
- UTEZ: The timing event generated when the PWM timer's value equals zero and when the PWM timer is increasing.
- DTEP: The timing event generated when the PWM timer's value equals the value of the period field (`MCPWM_TIMER $n$ _PERIOD`) and when the PWM timer is decreasing.
- DTEZ: The timing event generated when the PWM timer's value equals zero and when the PWM timer is decreasing.

Figures 51.3-9 to 51.3-11 show the timing waveforms of U/DTEP and U/DTEZ.

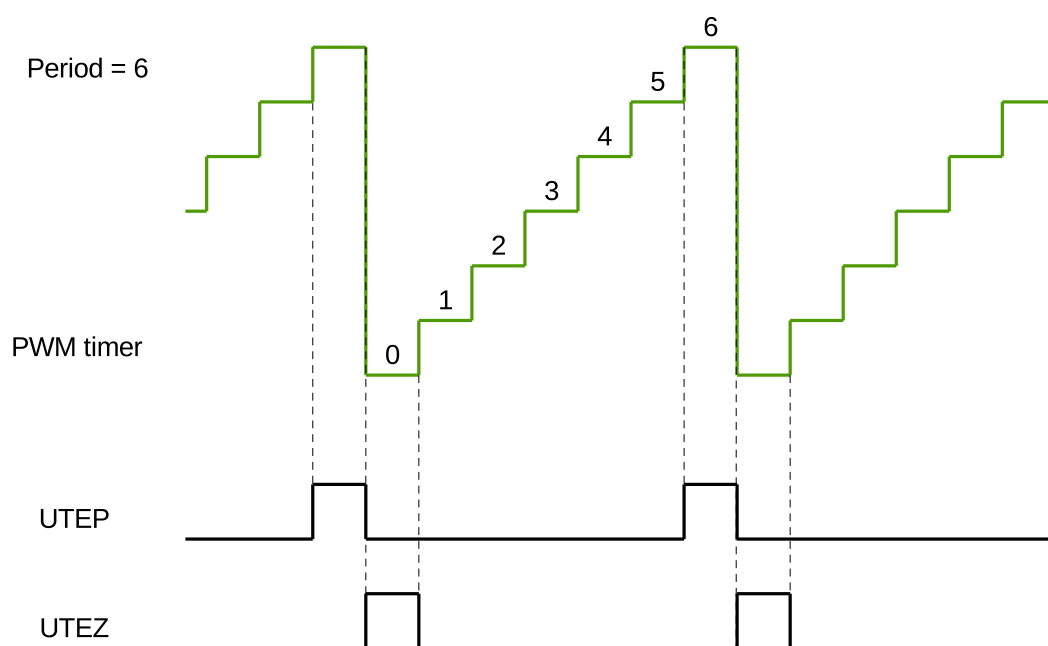


Figure 51.3-9. UTEP and UTEZ Generation in Count-Up Mode

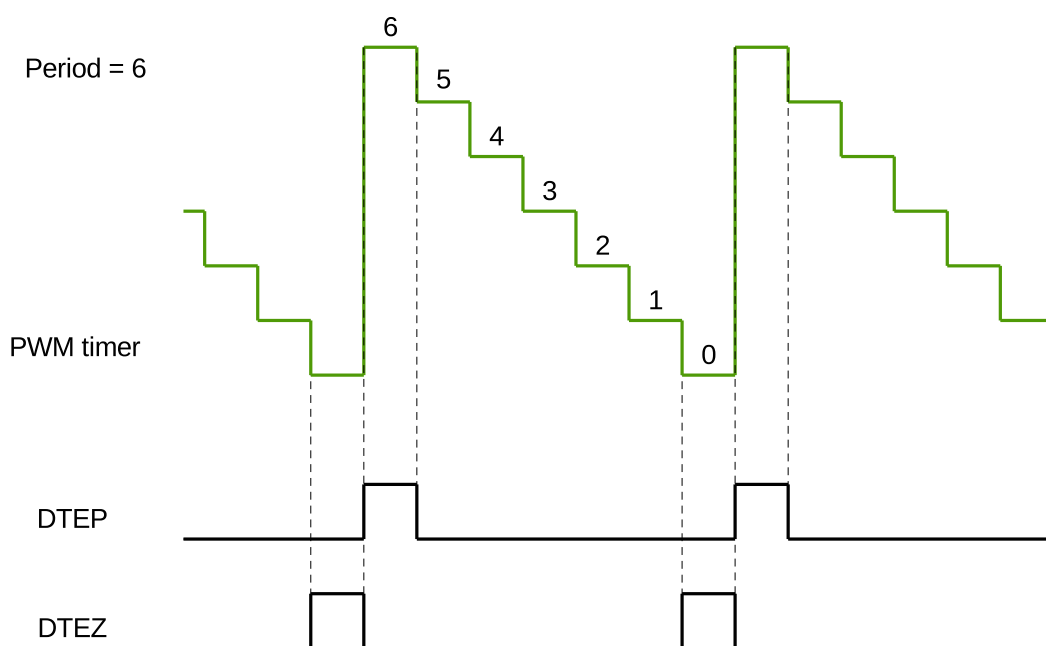


Figure 51.3-10. DTEP and DTEZ Generation in Count-Down Mode

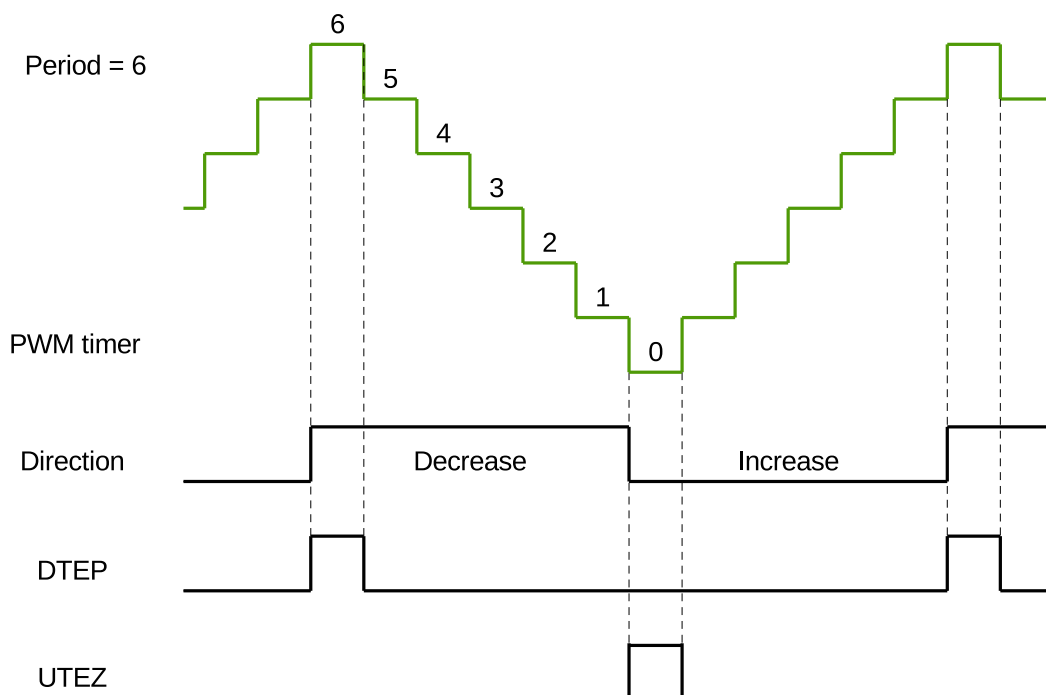


Figure 51.3-11. DTEP and UTEZ Generation in Count-Up-Down Mode

Please note that in the Count-Up-Down Mode, when the counting direction is increasing, the timer range is [0, period value - 1], and when the counting direction is decreasing, the timer range is [period value, 1]. That is, in this mode, when synchronizing the timer to 0, decreasing counting direction will be illegal, namely, `MCPWM_TIMER $n$ _PHASE_DIRECTION` cannot be set to 1. Similarly, when synchronizing the timer to period value, increasing counting direction will be illegal, namely, `MCPWM_TIMER $n$ _PHASE_DIRECTION` cannot be set to 0. Therefore, when the timer is synchronized to 0, the counting direction can only be increasing, and `MCPWM_TIMER $n$ _PHASE_DIRECTION` will be 0. When the timer is synchronized to the period value, the counting direction can only be decreasing, and `MCPWM_TIMER $n$ _PHASE_DIRECTION` will be 1.

### 51.3.2.3 Shadow Register of PWM Timer

The PWM timer's period register and the PWM timer's clock prescaler register have shadow registers. The shadow registers can back up the values that are about to be written to the valid registers. It also supports writing the values saved into the active register at a specific moment of hardware synchronization. The functionality of both register types is as follows:

- Active Register: Directly responsible for controlling all actions performed by hardware.
- Shadow Register: Acts as a temporary buffer for a value to be written to the active register. At a specific, user-configured point in time, the value saved in the shadow register is copied to the active register. Before this happens, the content of the shadow register has no direct effect on the controlled hardware. This helps to prevent erroneous operation of the hardware, which may happen when a register is asynchronously modified by software. Both the shadow register and the active register have the same memory address. The software always writes into, or reads from the shadow register.

The moment of updating the clock prescaler's active register is at the time when the timer starts operating. When `MCPWM_GLOBAL_UP_EN` is set to 1, the moment of updating the period active register can be selected by the following ways:

- By configuring the update method register `MCPWM_TIMERn_PERIOD_UPMETHOD` to 0, the update will start immediately.
- By configuring the update method register `MCPWM_TIMERn_PERIOD_UPMETHOD` to 1, the update can start when the PWM timer is equal to zero.
- By configuring the update method register `MCPWM_TIMERn_PERIOD_UPMETHOD` to 2, the update can start when the PWM timer is synchronized.
- By configuring the update method register `MCPWM_TIMERn_PERIOD_UPMETHOD` to 3, the update can start when the PWM timer is equal to zero or is synchronized.
- Software can also trigger a globally forced update bit `MCPWM_GLOBAL_FORCE_UP` which will prompt all registers in the module to be updated according to shadow registers.

### 51.3.2.4 PWM Timer Synchronization and Phase Locking

The PWM modules adopt a flexible synchronization method. Each PWM timer has a synchronization input and a synchronization output. The synchronization input can be selected from three synchronization outputs of the three PWM timers and three synchronization signals from the GPIO matrix. The synchronization output can be generated when the PWM timer's value equals to period or zero, the synchronization input signal is active, or software synchronizes. Thus, each PWM timer can flexibly select the synchronization input for different phase synchronization methods. During synchronization, the PWM timer clock prescaler will reset its counter and restart dividing the clock in order to ensure the correctness of the timer.

## 51.3.3 PWM Operator Module

The PWM Operator module has the following functions:

- Generates a PWM signal pair, based on timing references obtained from the corresponding PWM timer.

- Each signal out of the PWM signal pair includes a specific pattern of dead time (i.e., adding delays to the rising and falling edges of the PWM signal).
- Superimposes a carrier on the PWM signal, if configured to do so.
- Handles response under fault conditions.

Figure 51.3-12 shows the block diagram of a PWM operator.

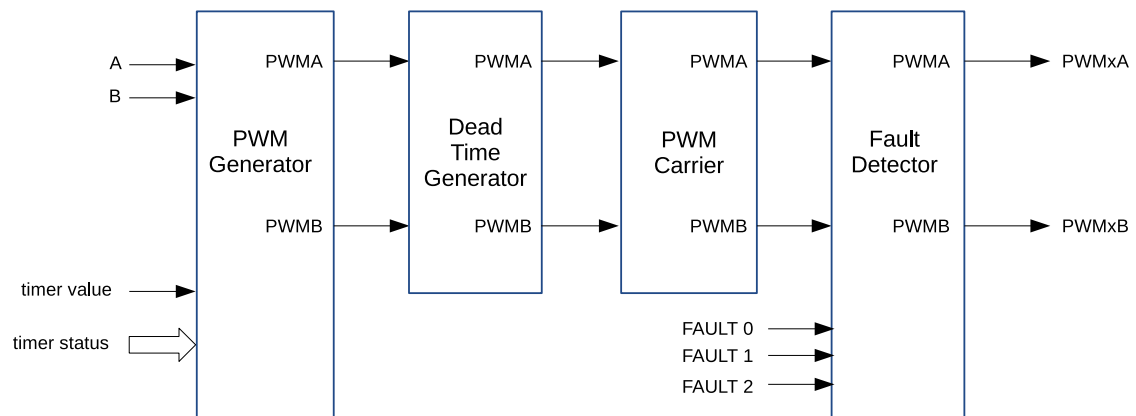


Figure 51.3-12. Block Diagram of A PWM Operator



### 51.3.3.1 PWM Generator Module

#### Purpose of the PWM Generator Module

In this module, important timing events are generated or imported. The events are then converted into specific actions to generate the desired waveforms at the PWMxA and PWMxB outputs.

The PWM generator module performs the following actions:

- Generation of timing events based on time stamps configured using the A and B registers. Events happen when the following conditions are met (for the configuration of registers A and B, see section [51.3.3.1](#)):
  - UTEA: the PWM timer is counting up and its value is equal to register A.
  - UTEB: the PWM timer is counting up and its value is equal to register B.
  - DTEA: the PWM timer is counting down and its value is equal to register A.
  - DTEB: the PWM timer is counting down and its value is equal to register B.
- Generation of U/DTO, U/DT1 timing events based on fault or synchronization events.
  - UTO: the PWM timer is counting up and FAULT0 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 0) or FAULT1 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 1) or FAULT2 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 2) or synchronized (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 3).
  - UT1: the PWM timer is counting up and FAULT0 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 0) or FAULT1 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 1) or FAULT2 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 2) or synchronized (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 3).
  - DTO: the PWM timer is counting down and FAULT0 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 0) or FAULT1 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 1) or FAULT2 detected (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 2) or synchronized (field [MCPWM\\_GENn\\_TO\\_SEL](#) is set to 3).
  - DT1: the PWM timer is counting down and FAULT0 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 0) or FAULT1 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 1) or FAULT2 detected (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 2) or synchronized (field [MCPWM\\_GENn\\_T1\\_SEL](#) is set to 3).
- Management of priority when these timing events occur concurrently.
- Generation of set, clear, and toggle actions, based on the timing events.
- Controlling of the PWM duty cycle, depending on the configuration of the PWM generator module.
- Handling of new time stamp values, using shadow registers to prevent glitches in the PWM cycle.

#### Shadow Register of PWM Generator

The time stamp registers A and B used by the hardware have shadow registers, which are registers [MCPWM\\_GENn\\_A\\_REG](#) and [MCPWM\\_GENn\\_B\\_REG](#). Shadowing provides a way of updating registers in sync with the hardware.

When [MCPWM\\_GLOBAL\\_UP\\_EN](#) is set to 1, the shadow registers can be written to the active register at a specified time. The update method field for [MCPWM\\_GENn\\_A\\_REG](#) and [MCPWM\\_GENn\\_B\\_REG](#) is [MCPWM\\_GENn\\_CFG\\_UPMETHOD](#). Software can also trigger a globally forced update bit

[MCPWM\\_GLOBAL\\_FORCE\\_UP](#) which will prompt all registers in the module to be updated according to shadow registers. For a description of the shadow registers, please see Section 51.3.2.3.

### Timing Events

For convenience, all timing signals and events are summarized in Table 51.3-2.

**Table 51.3-2. Timing Events Used in PWM Generator**

| Signal               | Event Description                                     | PWM Timer Operation   |
|----------------------|---|-----------------------|
| DTEP                 | PWM timer value is equal to the period register value | PWM timer counts down |
| DTEZ                 | PWM timer value is equal to zero                      |                       |
| DTEA                 | PWM timer value is equal to register A                |                       |
| DTEB                 | PWM timer value is equal to register B                |                       |
| DTO event            | Based on fault or synchronization events              |                       |
| DT1 event            | Based on fault or synchronization events              |                       |
| UTEP                 | PWM timer value is equal to the period register value | PWM timer counts up   |
| UTEZ                 | PWM timer value is equal to zero                      |                       |
| UTEA                 | PWM timer value is equal to register A                |                       |
| UTEB                 | PWM timer value is equal to register B                |                       |
| UTO event            | Based on fault or synchronization events              |                       |
| UT1 event            | Based on fault or synchronization events              |                       |
| Software-force event | Software-initiated asynchronous event                 | N/A                   |

The purpose of a software-force event is to impose non-continuous or continuous changes on the PWM<sub>x</sub>A and PWM<sub>x</sub>B outputs. The change is done asynchronously. Software-force control is handled by the [MCPWM\\_GEN<sub>n</sub>\\_FORCE\\_REG](#) registers.

The selection and configuration of T0/T1 in the PWM generator module is independent of the configuration of fault events in the fault handler module. A particular trip event may or may not be configured to cause trip action in the fault handler submodule, but the same event can be used by the PWM generator to trigger T0/T1 for controlling PWM waveforms.

It is important to know that when the PWM timer is in Count-Up-Down Mode. It will always decrement after a TEP event, and increment after a TEZ event. So, when the PWM timer is in Count-Up-Down Mode, DTEP and UTEZ events will occur, while UTEP and DTEZ events never occurs.

The PWM generator can handle multiple events at the same time. Events are prioritized by the hardware and relevant details are provided in Table 51.3-3 and Table 51.3-4. Priority levels range from 1 (the highest) to 7 (the lowest). Please note that the priority of TEP and TEZ events depends on the PWM timer's counting mode.

If the value of A or B is set to be greater than the period, then U/DTEA and U/DTEB will never occur.

**Table 51.3-3. Timing Events Priority When PWM Timer Increments**

| Priority Level | Event                 |
|----------------|-----------------------|
| 1 (highest)    | Software-forced event |
| 2              | UTEP                  |

| Priority Level | Event |
|----------------|-------|
| 3              | UTO   |
| 4              | UT1   |
| 5              | UTEB  |
| 6              | UTEA  |
| 7 (lowest)     | UTEZ  |

Table 51.3-4. Timing Events Priority when PWM Timer Decrements

| Priority level | Event                 |
|----------------|-----------------------|
| 1 (highest)    | Software-forced event |
| 2              | DTEZ                  |
| 3              | DT0                   |
| 4              | DT1                   |
| 5              | DTEB                  |
| 6              | DTEA                  |
| 7 (lowest)     | DTEP                  |

## Notes:

1. UTEP and UTEZ do not happen simultaneously. When the PWM timer is in Count-Up Mode, UTEP will always happen one cycle earlier than UTEZ, as demonstrated in Figure 51.3-9, so their action on PWM signals will not interrupt each other. When the PWM timer is in Count-Up-Down Mode, UTEP will not occur.
2. DTEP and DTEZ do not happen simultaneously. When the PWM timer is in Count-Down Mode, DTEZ will always happen one cycle earlier than DTEP, as demonstrated in Figure 51.3-10, so their action on PWM signals will not interrupt each other. When the PWM timer is in Count-Up-Down Mode, DTEZ will not occur.

**PWM Signal Generation**

The PWM generator module controls the behavior of outputting PWMxA and PWMxB when a particular timing event occurs. The timing events are further qualified by the PWM timer's counting mode (increment or decrement). Knowing the counting mode, the module may then perform an independent action at each stage of the PWM timer counting up or down.

The following actions may be configured on PWMxA and PWMxB outputs:

- Set High: Set the output of PWMxA or PWMxB to a high level.
- Clear Low: Clear the output of PWMxA or PWMxB by setting it to a low level.
- Toggle: Change the current output level of PWMxA or PWMxB to the opposite value. If it is currently pulled up, then pull it down, or vice versa.
- Do Nothing: Keep both outputs PWMxA and PWMxB unchanged. In this state, interrupts can still be triggered.

Actions on outputs is configured by using registers `MCPWM_GENn_A_REG` and

[MCPWM\\_GENn\\_B\\_REG](#). So, the action to be taken on each output is set independently. Also, there is great flexibility in selecting actions to be taken on a given output based on events. More specifically, any event listed in Table 51.3-2 can operate on either output of PWMx<sub>A</sub> or PWMx<sub>B</sub>. To check out registers for particular generator 0, 1, or 2, please refer to the register description in Section 51.5.

### Waveforms for Common Configurations

In the configuration of various waveforms below, period refers to the configuration value stored in the period register of the PWM timer selected by the PWM operator (i.e., [MCPWM\\_TIMERn\\_PERIOD](#) ( $x = 0, 1, 2$ )). For configuration methods, please refer to the section 51.3.2. A and B denote the time stamp registers A and B used by the hardware. For register configuration, please refer to the section 51.3.3.1. UTEA/B, UTEZ/P, DTEA/B, DTEZ/P, DTO/1, and UTO/1 represent different timing events of the PWM generator. For event definition, please refer to the section 51.3.3.1. The upward arrow, downward arrow, and T mark signify setting the PWM waveform high, setting it low, toggling it when the timing event occurs. See section 51.3.3.1 for configuration. PWMx<sub>A</sub> and PWMx<sub>B</sub> are the output signals of PWM generator $x$ .

Figure 51.3-13 presents the symmetrical PWM waveform generated when the PWM timer is in Count-Up-Down mode. DC 0%–100% modulation can be calculated via the formula below:

$$Duty = (Period - A) \div Period$$

If A matches the PWM timer value and the PWM timer is incrementing, then the PWM output is pulled up. If A matches the PWM timer value while the PWM timer is decrementing, then the PWM output is pulled low.

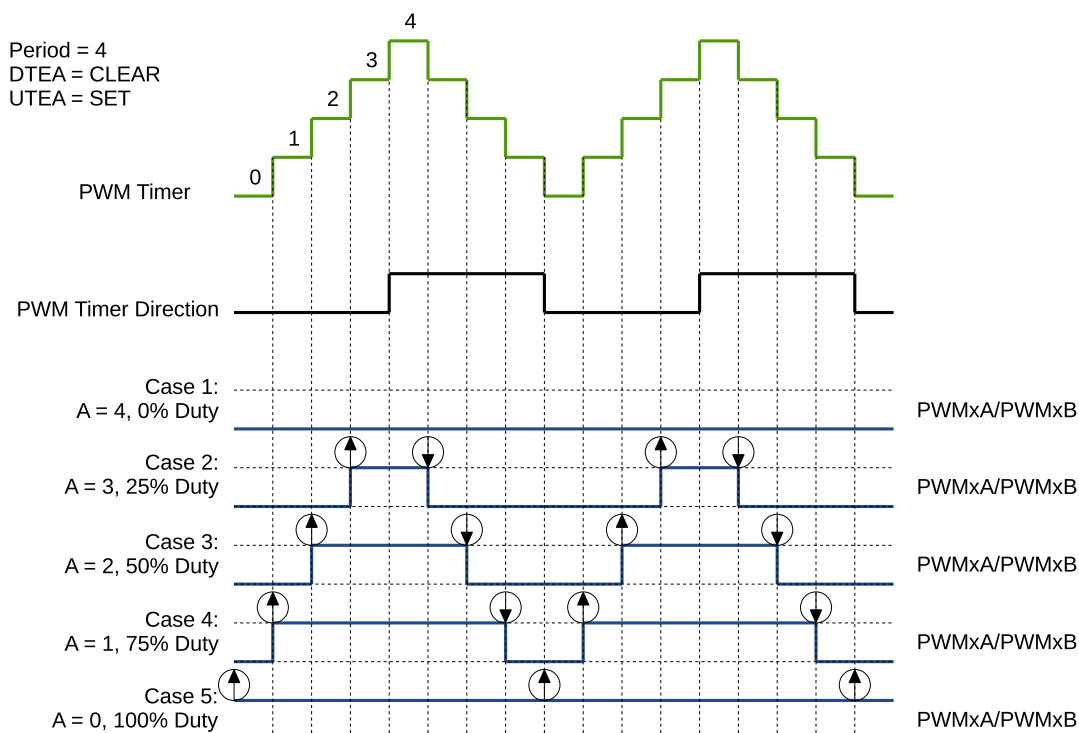


Figure 51.3-13. Symmetrical Waveform in Count-Up-Down Mode

The PWM waveforms in Figures 51.3-14 to 51.3-17 show some common PWM generator configurations.

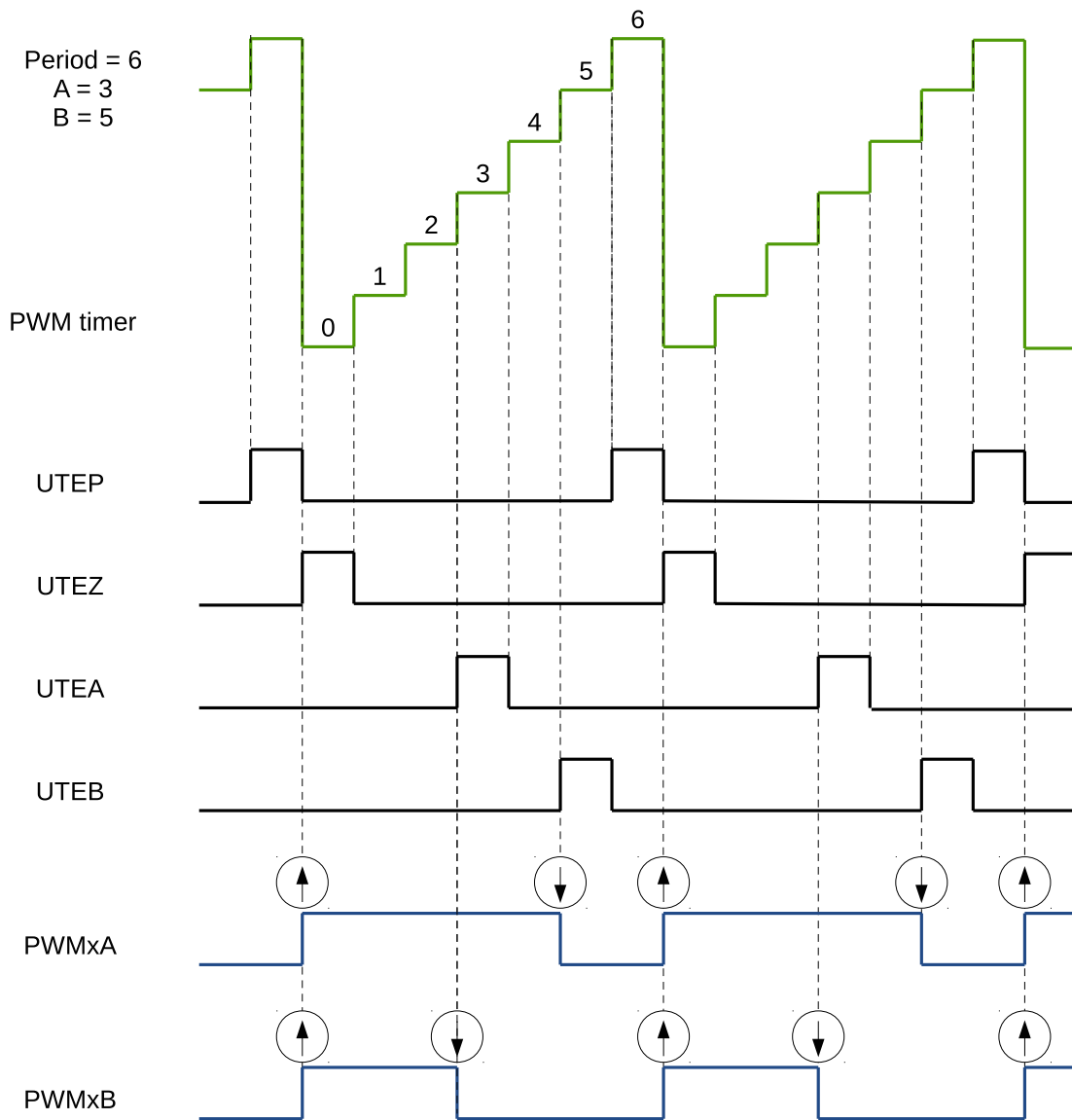


Figure 51.3-14. Count-Up, Single Edge Asymmetric Waveform, with Independent Modulation on PWMxA and PWMxB — Active High

The duty modulation for PWMxA is set by B, active high and proportional to B.

The duty modulation for PWMxB is set by A, active high and proportional to A.

$$Period = (MCPWM\_TIMER\_PERIOD + 1) \times T_{PT\_clk}$$

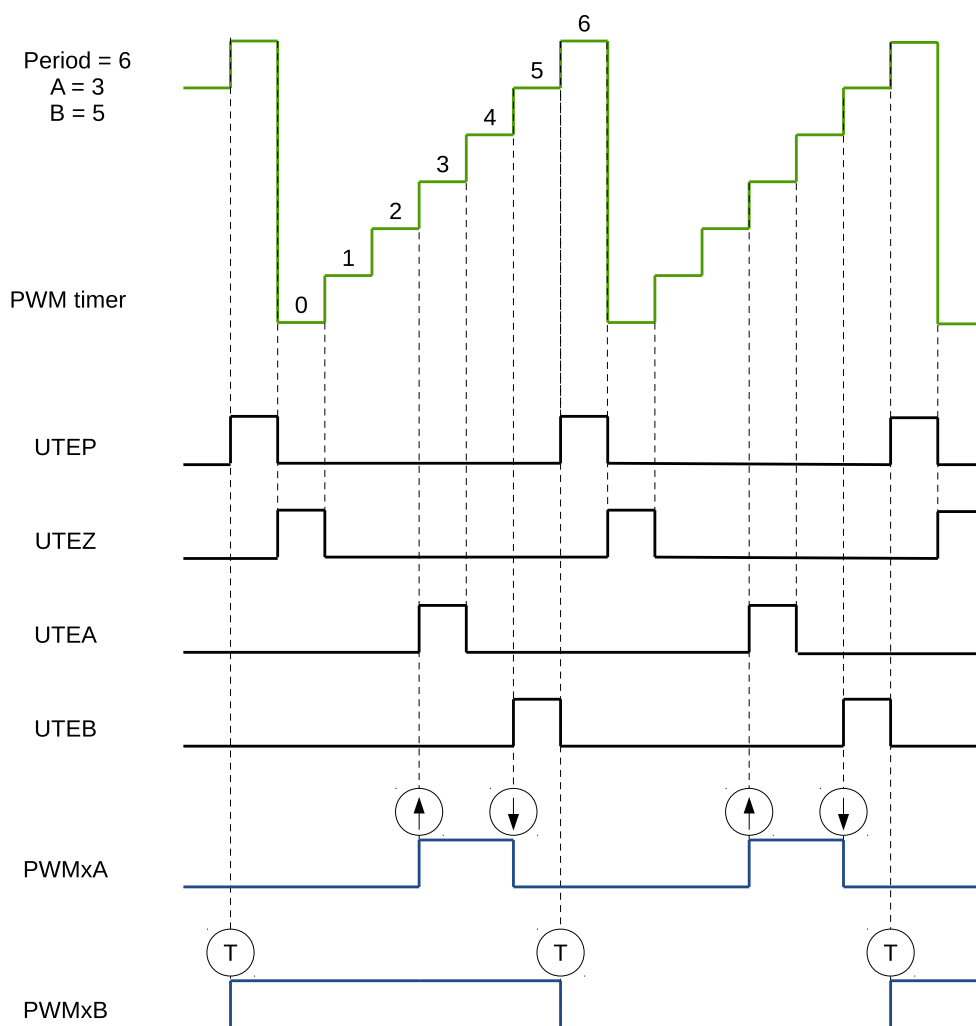


Figure 51.3-15. Count-Up, Pulse Placement Asymmetric Waveform with Independent Modulation on PWMxA

Pulses may be generated anywhere within the PWM cycle (zero to period).

PWMxA's high time duty is proportional to (B - A).

$$Period = (MCPWM\_TIMERn\_PERIOD + 1) \times T_{PT\_clk}$$

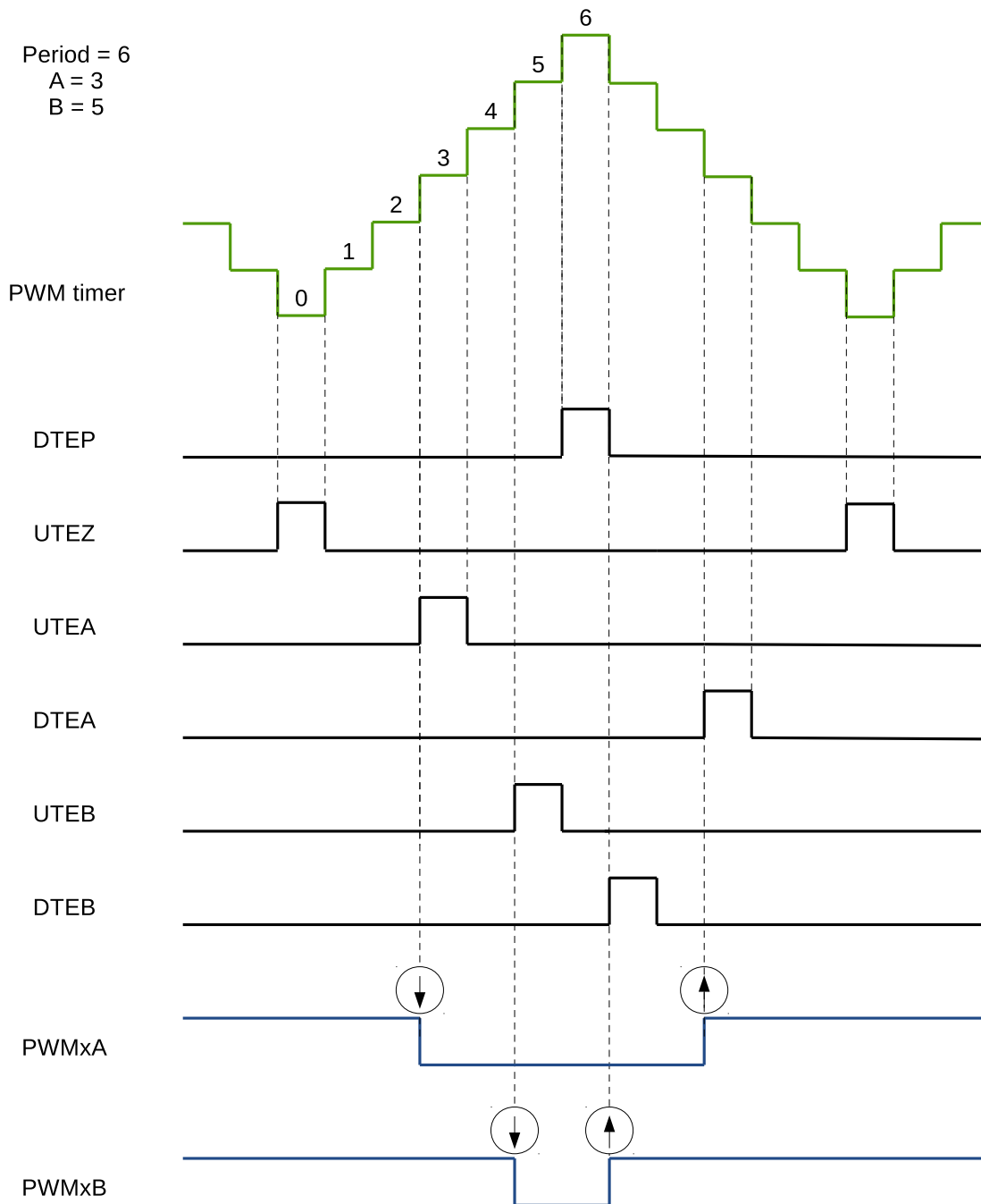


Figure 51.3-16. Count-Up-Down, Dual Edge Symmetric Waveform, with Independent Modulation on PWMxA and PWMxB — Active High

The duty modulation for PWMxA is set by A, active high and proportional to A.  
The duty modulation for PWMxB is set by B, active high and proportional to B.  
Outputting PWMxA and PWMxB can drive separate switches.

$$Period = (2 \times MCPWM\_TIMER\_PERIOD) \times T_{PT\_clk}$$

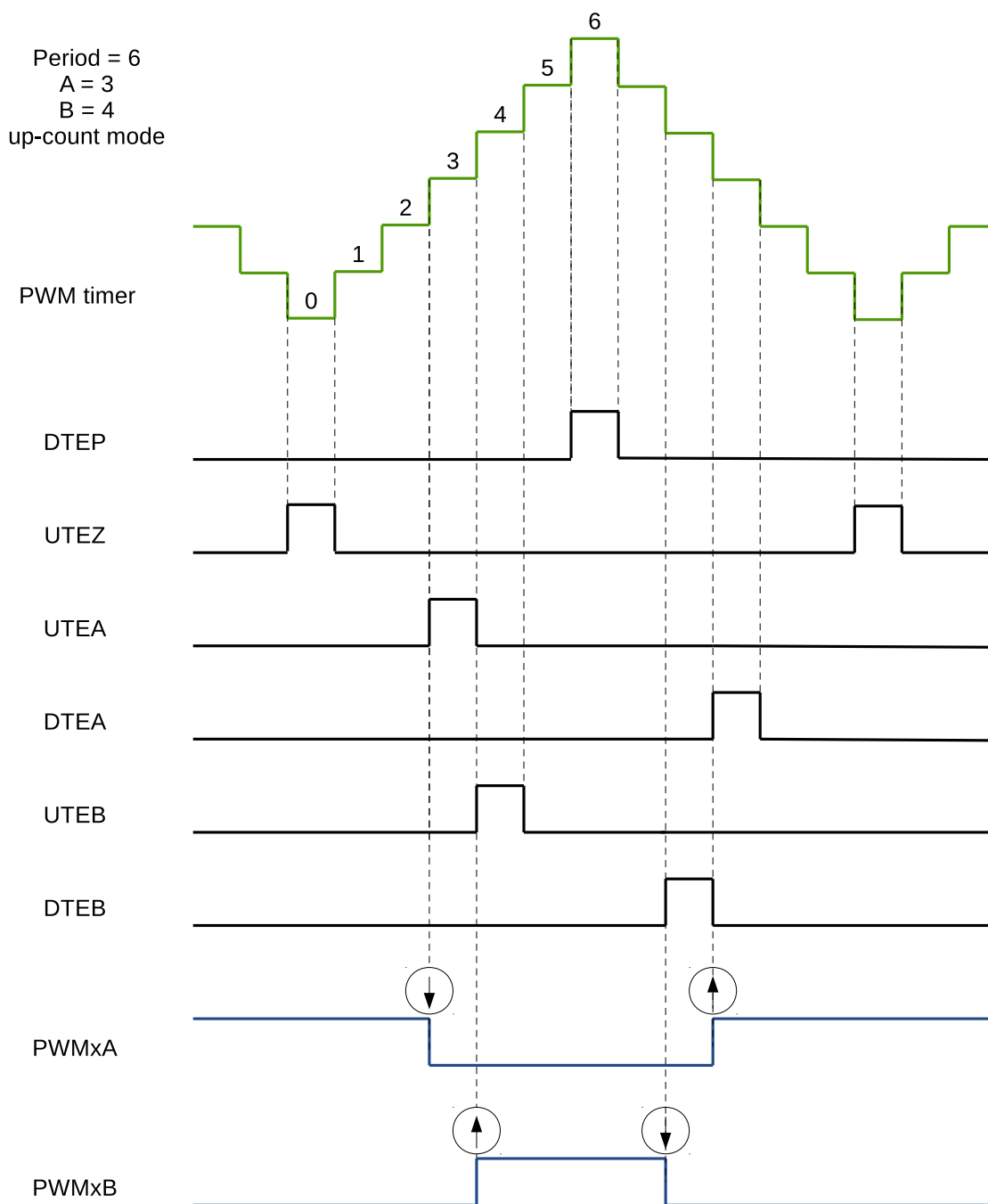


Figure 51.3-17. Count-Up-Down, Dual Edge Symmetric Waveform, with Independent Modulation on PWMxA and PWMxB – Complementary

The duty modulation of PWMxA is set by A, is active high and proportional to A.

The duty modulation of PWMxB is set by B, is active low and proportional to B.

Outputs PWMx can drive upper/lower (complementary) switches.

Dead time = B – A. Edge placement is configurable by software. Dead time generator module supports configuring edge delay methods when required.

$$Period = (2 \times MCPWM\_TIMERn\_PERIOD) \times T_{PT\_clk}$$



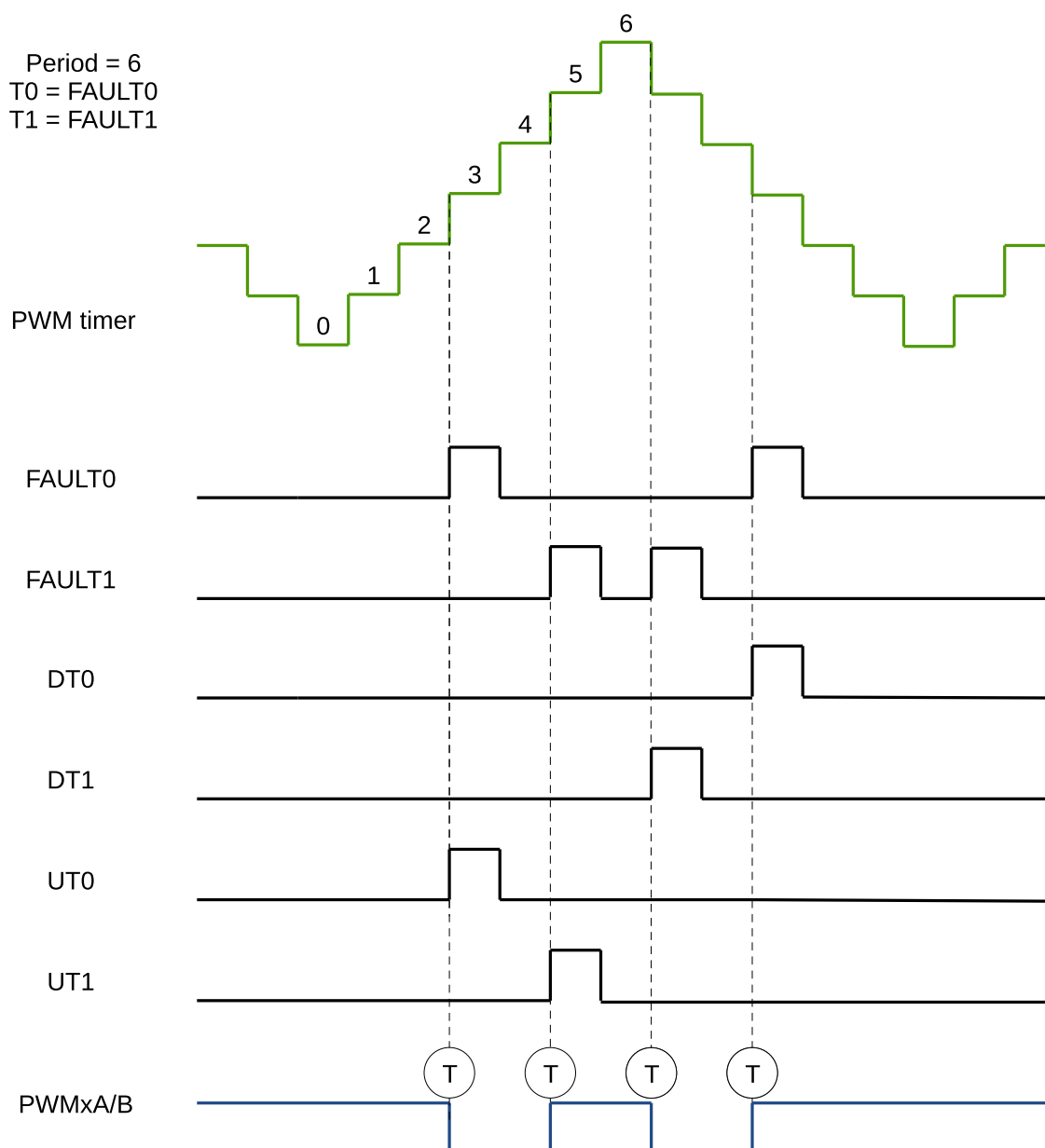


Figure 51.3-18. Count-Up-Down, Fault or Synchronization Events, with Same Modulation on PWMxA and PWMxB

Figure 51.3-18 shows a waveform when UT0/1 and DT0/1 events are generated. In this example, T0 selects FAULT0 and T1 selects FAULT1. The events selected by T0 and T1 can be configured independently, these events can be FAULT0, FAULT1, FAULT2 or synchronous. For detailed configuration, see section 51.3.3.1.

### Software-Force Events

There are two types of software-force events inside the PWM generator:

- Non-continuous-immediate (NCI) software-force events: Such types of events are immediately effective on PWM outputs when triggered by software. The forcing is non-continuous, which means the next active timing events will be able to alter the PWM outputs.
- Continuous (CNTU) software-force events: Such types of events are continuous. The forced PWM outputs will continue until they are released by software. The events' triggers are configurable. They can

be configured to be timing events or immediate events.

For NCI software-force events, set register [MCPWM\\_GENn\\_A\\_NCIFORCE](#) or [MCPWM\\_GENn\\_B\\_NCIFORCE](#) to 1 and then to 0 to trigger the NCI software-forced events of PWMxA or PWMxB. Configure register [MCPWM\\_GENn\\_A\\_NCIFORCE\\_MODE](#) or [MCPWM\\_GENn\\_B\\_NCIFORCE\\_MODE](#) to specify the operation on the PWMxA or PWMxB waveform when the NCI software-force event occurs. Configuring the registers to 0 or 3 means no operation, 1 means low level, and 2 means high level.

For CNTU software-force events, set register [MCPWM\\_GENn\\_CNTUFORCE\\_UPMETHOD](#) to specify the trigger method of CNTU software-force events. Setting all bits to 0 means trigger CNTU software-force events immediately, setting bit 0 to 1 means the TEZ event triggers CNTU software-force events, setting bit 1 to 1 means the TEP event triggers CNTU software-force events, setting bit 2 to 1 means the TEA event triggers CNTU software-force events, setting bit 3 to 1 means the TEB event triggers CNTU software-force events, setting bit 4 to 1 means CNTU software-force events triggered when the PWM timer selected by the PWM generator is synchronized, and setting bit 5 to 1 means the CNTU software-forced events will not be triggered. Configure register [MCPWM\\_GENn\\_A\\_CNTUFORCE\\_MODE](#) or [MCPWM\\_GENn\\_B\\_CNTUFORCE\\_MODE](#) to specify the operation on the PWMxA or PWMxB waveform when the CNTU software-force events occur. Configuring the registers to 0 or 3 means no operation, 1 means low level, and 2 means high level.

Figure 51.3-19 shows a waveform of NCI software-force events. NCI events are used to force PWMxA output low. Forcing on PWMxB is disabled in this case.

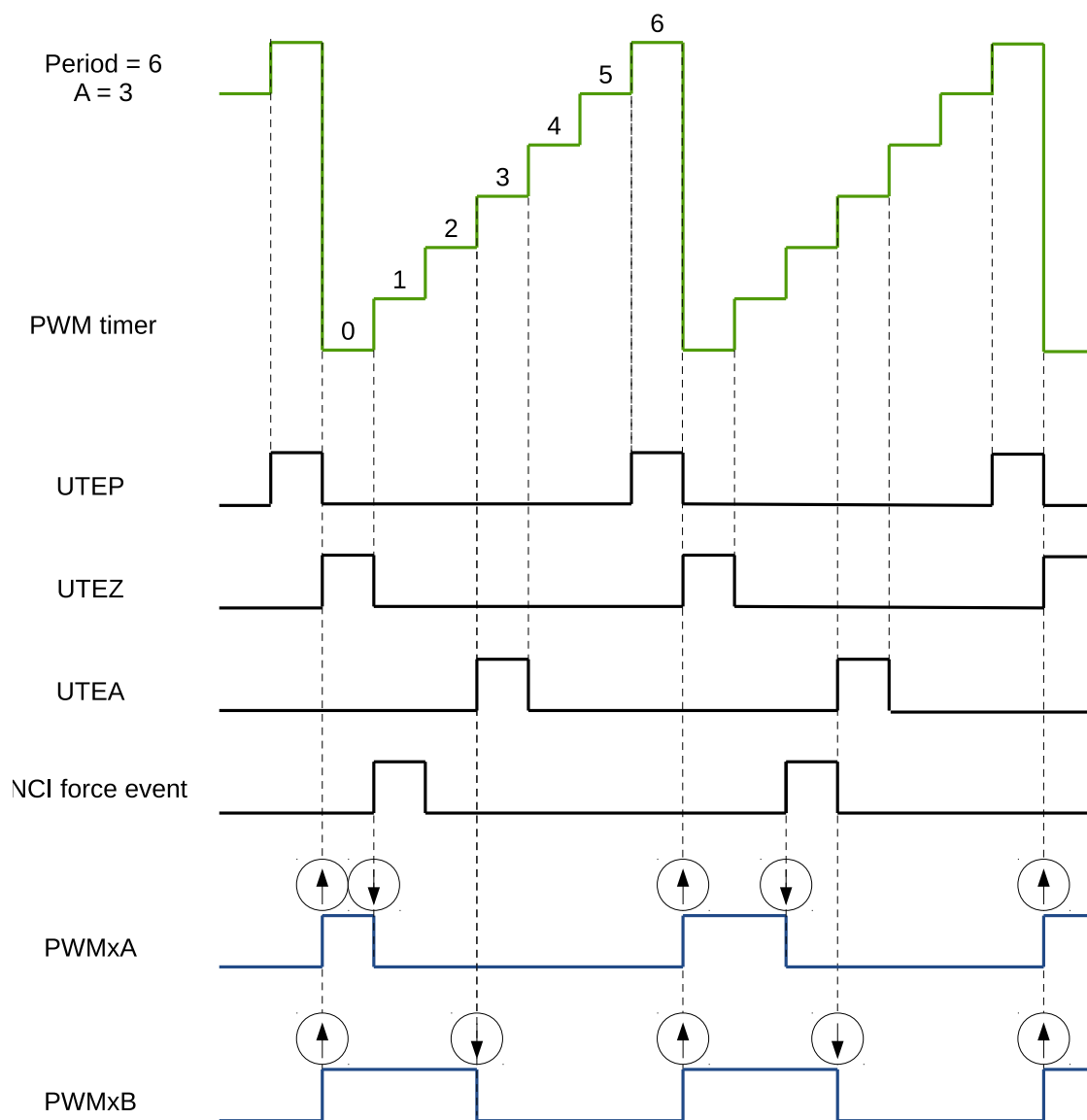


Figure 51.3-19. Example of an NCI Software-Force Event on PWMxA

Figure 51.3-20 shows a waveform of CNTU software-force events. TEZ events are selected as triggers for CNTU software-force events. CNTU is used to force the PWMxB output low. Forcing on PWMxA is disabled.

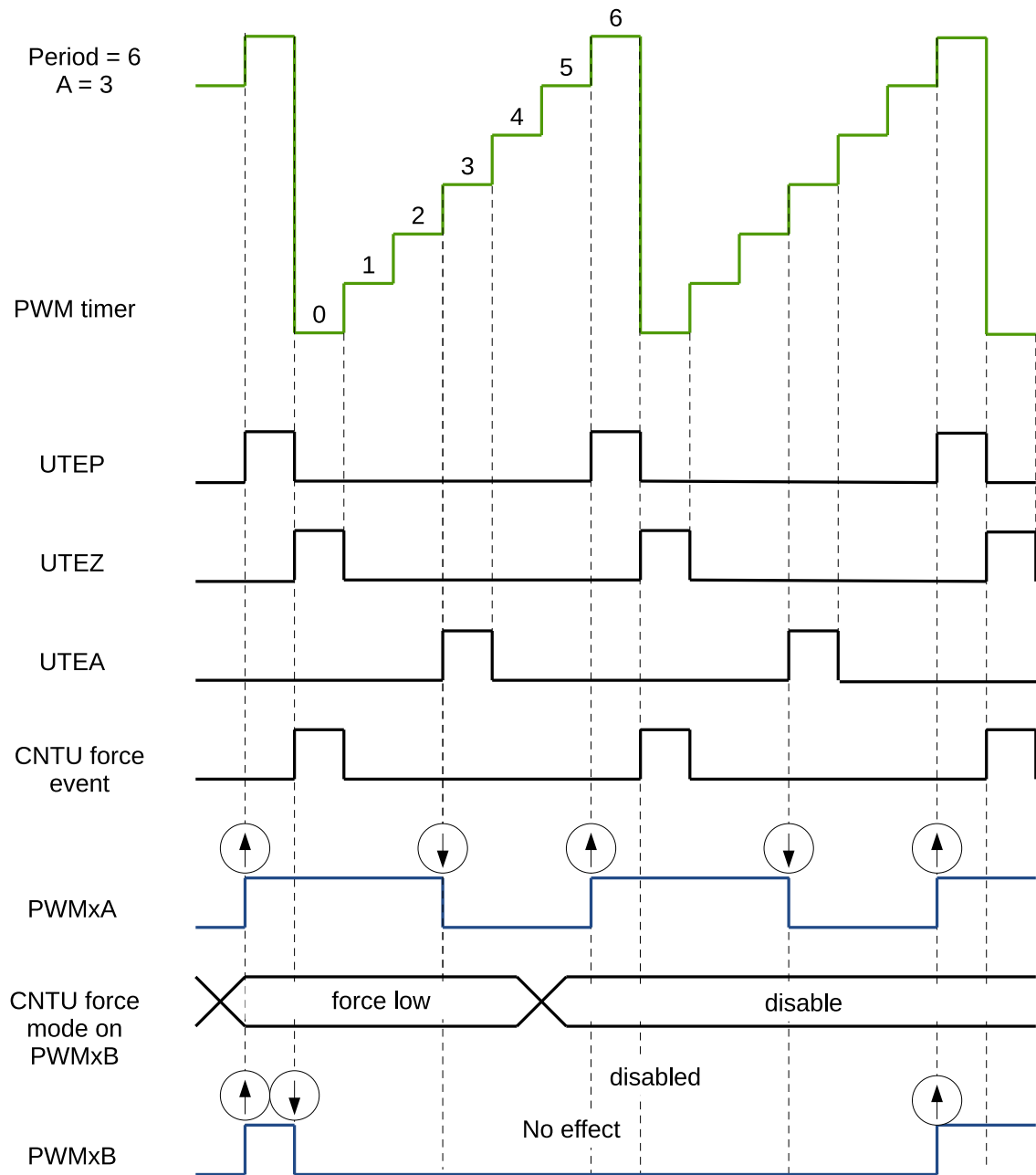


Figure 51.3-20. Example of a CNTU Software-Force Event on PWMxB

### 51.3.3.2 Dead Time Generator Module

#### Purpose of the Dead Time Generator Module

Section 51.3.3.1 introduced several options to generate signals on PWMxA and PWMxB outputs, with a specific placement of signal edges. The required dead time is obtained by altering the edge placement between signals and by setting the signal's duty cycle. Another option to control the dead time is to use a specialized module – Dead Time Generator.

The key functions of the Dead Time Generator module are as follows:

- Generating output signal pairs (PWMxA and PWMxB) with a dead time from a common source, which can be either the input signal PWMxA or PWMxB.
- Creating a dead time by adding delay to signal edges:
  - Rising edge delay (RED)
  - Falling edge delay (FED)
- Can generate PWM signal in various format. The typical dead time configurations are:
  - Active high complementary (AHC)
  - Active low complementary (ALC)
  - Active high (AH)
  - Active low (AL)
- This module may also be bypassed, if the dead time is configured directly in the generator module.

#### Shadow Register of Dead Time Generator

Delay registers RED and FED are shadowed with registers `MCPWM_DT $n$ _RED_CFG_REG` and `MCPWM_DT $n$ _FED_CFG_REG`. When `MCPWM_GLOBAL_UP_EN` is set to 1, the values saved in the shadow registers can be written to the active register at the specified time. The update method register for `MCPWM_DT $n$ _RED_CFG_REG` is `MCPWM_DB $n$ _RED_UPMETHOD`. The update method register for `MCPWM_DT $n$ _FED_CFG_REG` is `MCPWM_DB $n$ _FED_UPMETHOD`. The Software can also trigger a globally forced update bit `MCPWM_GLOBAL_FORCE_UP` which will prompt all registers in the module to be updated according to shadow registers. For the description of shadow registers, please see section 51.3.2.3.

## Highlights for Operation of the Dead Time Generator

Options for setting up the dead time module are shown in Figure 51.3-21.

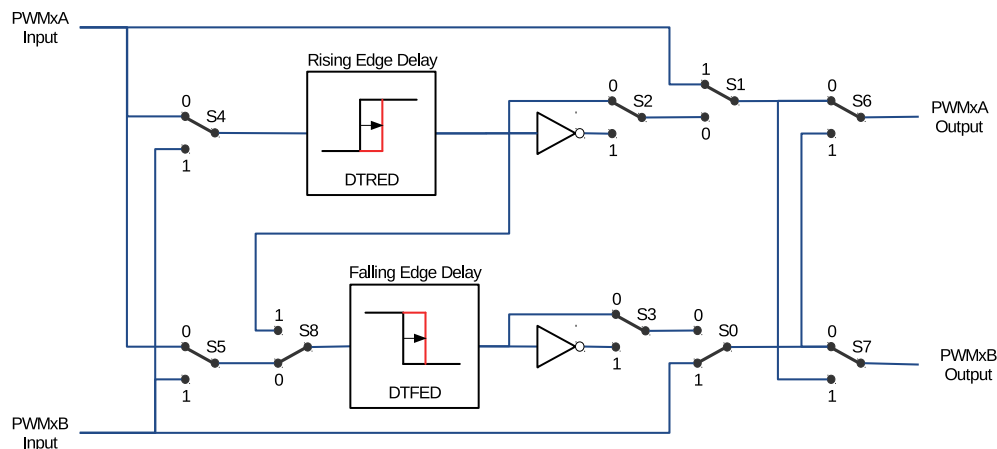


Figure 51.3-21. Options for Setting up the Dead Time Generator Module

S0-S8 in the figure above are switches controlled by fields in register `MCPWM_DTn_CFG_REG` shown in Table 51.3-5.

Table 51.3-5. Dead Time Generator Switches Control Fields

| Switch | Field                                |
|--------|--------------------------------------|
| S0     | <code>MCPWM_DBn_B_OUTBYPASS</code>   |
| S1     | <code>MCPWM_DBn_A_OUTBYPASS</code>   |
| S2     | <code>MCPWM_DBn_RED_OUTINVERT</code> |
| S3     | <code>MCPWM_DBn_FED_OUTINVERT</code> |
| S4     | <code>MCPWM_DBn_RED_INSEL</code>     |
| S5     | <code>MCPWM_DBn_FED_INSEL</code>     |
| S6     | <code>MCPWM_DBn_A_OUTSWAP</code>     |
| S7     | <code>MCPWM_DBn_B_OUTSWAP</code>     |
| S8     | <code>MCPWM_DBn_DEB_MODE</code>      |

All switch combinations are supported, but not all of them represent the typical modes of use. Table 51.3-6 documents some typical dead time configurations. In these configurations, the position of S4 and S5 sets PWMxA as the common source of both falling edge delay (FED) and rising edge delay (RED). The modes presented in table 51.3-6 may be categorized as follows:

Table 51.3-6. Typical Dead Time Generator Operating Modes

| Mode | Mode Description                                    | S0 | S1 | S2 | S3 |
|------|---|----|----|----|----|
| 1    | PWMxA and PWMxB Pass Through/No Delay               | 1  | 1  | X  | X  |
| 2    | Active High Complementary (AHC), see Figure 51.3-22 | 0  | 0  | 0  | 1  |
| 3    | Active Low Complementary (ALC), see Figure 51.3-23  | 0  | 0  | 1  | 0  |
| 4    | Active High (AH), see Figure 51.3-24                | 0  | 0  | 0  | 0  |

| Mode | Mode Description  | S0 | S1 | S2     | S3     |
|------|---|----|----|--------|--------|
| 5    | Active Low (AL), see Figure 51.3-25   | 0  | 0  | 1      | 1      |
| 6    | PWMxA Output = PWMxA In (No Delay)<br>PWMxB Output = PWMxA Input with Falling Edge Delay      | 0  | 1  | 0 or 1 | 0 or 1 |
| 7    | PWMxA Output = PWMxA Input with Rising Edge Delay<br>PWMxB Output = PWMxB Input with No Delay | 1  | 0  | 0 or 1 | 0 or 1 |

**Note:**

For all the modes above, the position of the binary switches S4 to S8 is set to 0.

- **Mode 1: Bypass delays on both FED and RED**

In this mode, the dead time module is disabled. Signals of PWMxA and PWMxB pass through without any modifications.

- **Mode 2-5: Classical Dead Time Polarity Settings**

These four modes represent typical configurations of polarity and should cover the active-high/low modes in available industry power switch gate drivers. The typical waveforms are shown in Figures 51.3-22 to 51.3-25.

- **Modes 6 and 7: Bypass delay on the falling edge (FED) or rising edge (RED)**

In these two modes, either RED or FED is bypassed. As a result, the corresponding delay is not applied.

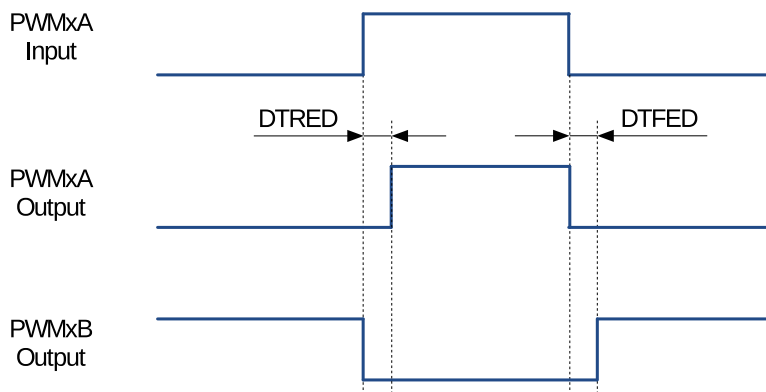


Figure 51.3-22. Active High Complementary (AHC) Dead Time Waveforms

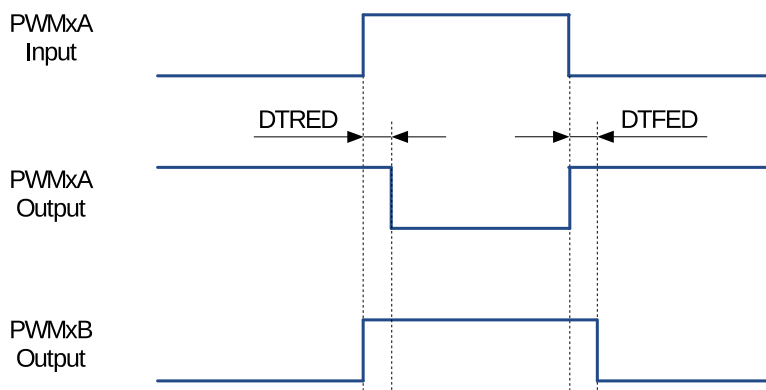


Figure 51.3-23. Active Low Complementary (ALC) Dead Time Waveforms

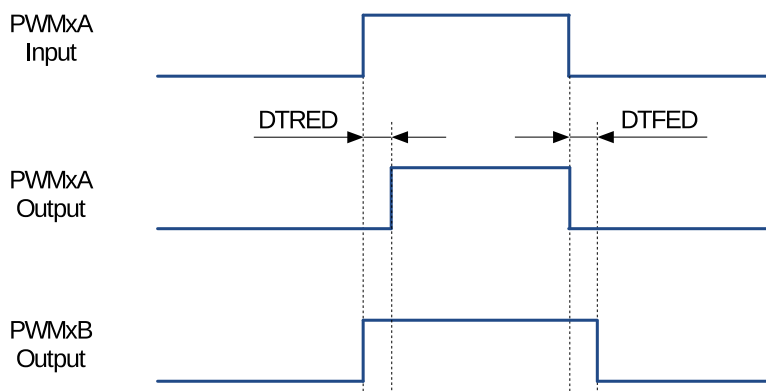


Figure 51.3-24. Active High (AH) Dead Time Waveforms



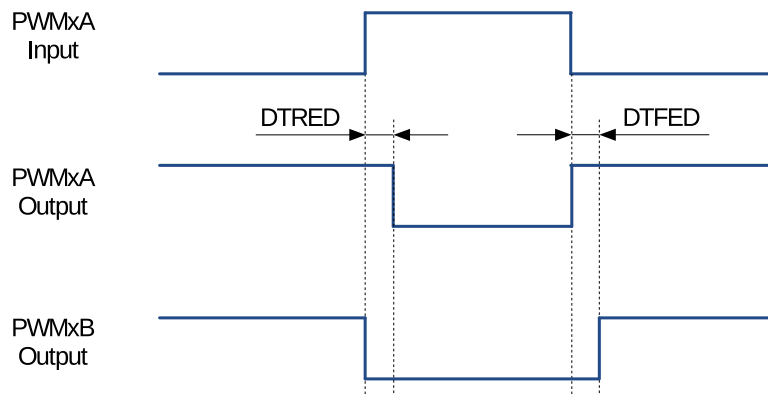


Figure 51.3-25. Active Low (AL) Dead Time Waveforms

RED and FED delays may be set up independently. The delay value is programmed using the 16-bit field `MCPWM_DB $n$ _RED` and `MCPWM_DB $n$ _FED`. The register value represents the number of clock (DT\_CLK) periods by which a signal edge is delayed. DT\_CLK can be selected from PWM\_clk or PT\_clk through register `MCPWM_DB $n$ _CLK_SEL`.

To calculate the delay on the falling edge (FED) and rising edge (RED), use the following formulas:

$$FED = MCPWM\_DTn\_FED \times T_{DT\_clk}$$

$$RED = MCPWM\_DTn\_RED \times T_{DT\_clk}$$

### 51.3.3.3 PWM Carrier Module

The coupling of PWM output to a motor driver may need isolation with a transformer. Transformers deliver only AC signals, while the duty cycle of a PWM signal may range anywhere from 0% to 100%. The PWM carrier module passes such a PWM signal through a transformer by using a high frequency carrier to modulate the signal.

#### Function Overview

The following key characteristics of this module are configurable:

- Carrier frequency
- Pulse width of the first pulse
- Duty cycle of the second and the subsequent pulses
- Enabling/disabling the carrier function

#### Operational Highlights

The PWM carrier clock (PC\_clk) is derived from PWM\_CLK. The frequency and duty cycle are configured by the `MCPWM_CHOPPERn_PRESCALE` and `MCPWM_CHOPPERn_DUTY` bits in the `MCPWM_CARRIERn_CFG_REG` register. The purpose of one-shot pulses is to provide the high-energy impulse to reliably turn on the power switch. Subsequent pulses sustain the power-on status. The width of a one-shot pulse is configurable with the `MCPWM_CHOPPERn_OSHTWTH` field. Enabling/disabling of the carrier module is done with the `MCPWM_CHOPPERn_EN` bit.

#### Waveform Examples

Figure 51.3-26 shows an example of waveforms, where a carrier is superimposed on original PWM pulses. This figure does not show the first one-shot pulse and the duty-cycle control. Related details are covered in the following two sections.

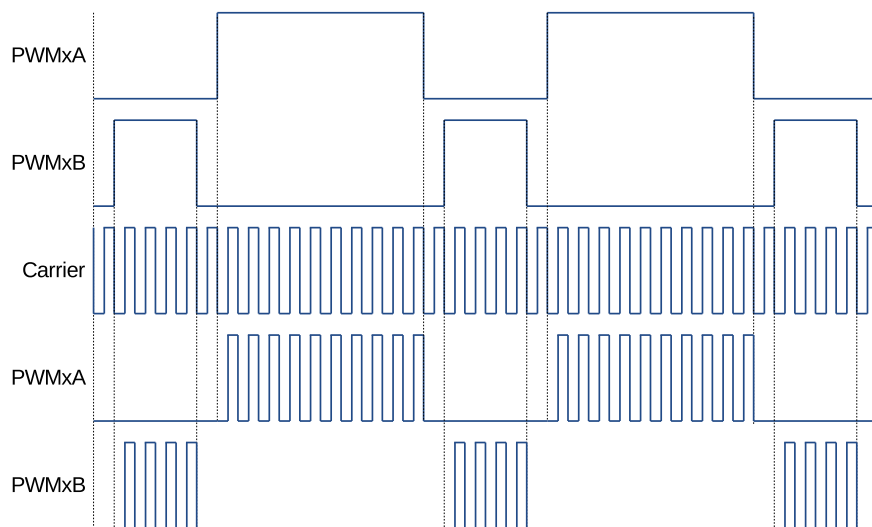


Figure 51.3-26. Example of Waveforms Showing PWM Carrier Action

## One-Shot Pulse

The width of the first pulse can be configured to 16 different values, which can be calculated by the following equation:

$$T_{1stpulse} = T_{PWM\_clk} \times 8 \times (MCPWM\_CARRIERn\_PRESCALE + 1) \times (MCPWM\_CARRIERn\_OSHTWTH + 1)$$

Where:

- $T_{PWM\_clk}$  is the period of the PWM clock (PWM\_clk).
- $(MCPWM\_CARRIERn\_OSHTWTH + 1)$  is the width of the first pulse (whose value ranges from 1 to 16).
- $(MCPWM\_CARRIERn\_PRESCALE + 1)$  is the PWM carrier clock's (PC\_clk) prescaler value.

The first one-shot pulse and subsequent sustaining pulses are shown in Figure 51.3-27.

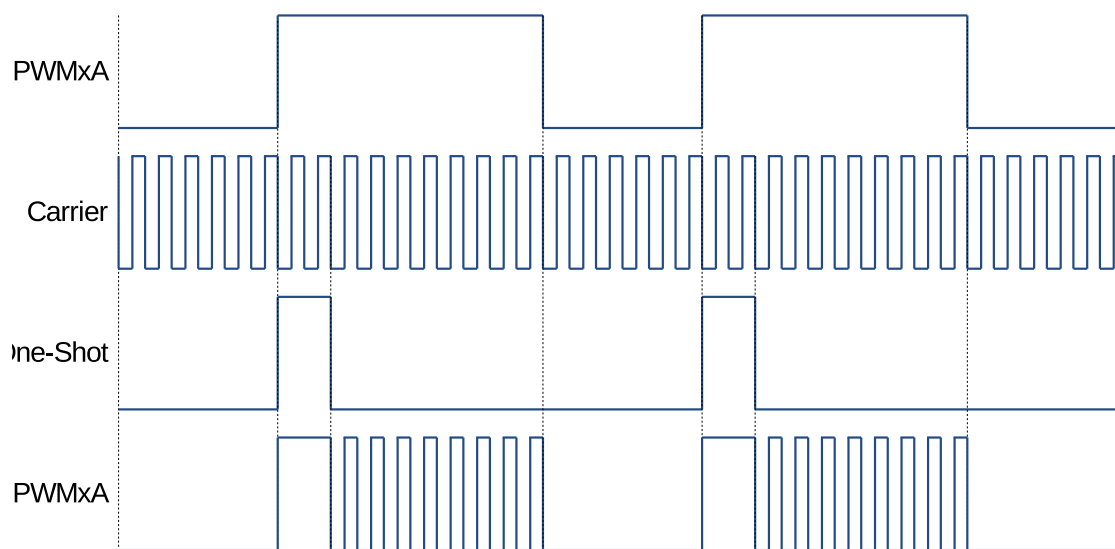


Figure 51.3-27. Example of the First Pulse and the Subsequent Sustaining Pulses of the PWM Carrier Sub-module

## Duty Cycle Control

After issuing the first one-shot pulse, the remaining PWM signal is modulated according to the carrier frequency. Users can configure the duty cycle of this signal. Tuning of duty may be required, so that the signal passes through the isolating transformer and can still operate (turn on/off) the motor drive, changing rotation speed and direction.

The duty cycle may be set to one of seven values, using `MCPWM_CHOPPERn_DUTY`, or bits [7:5] of register `MCPWM_CARRIERn_CFG_REG`.

Below is the formula for calculating the duty cycle:

$$Duty = MCPWM\_CARRIERn\_DUTY \div 8$$

All seven settings of the duty cycle are shown in Figure 51.3-28.

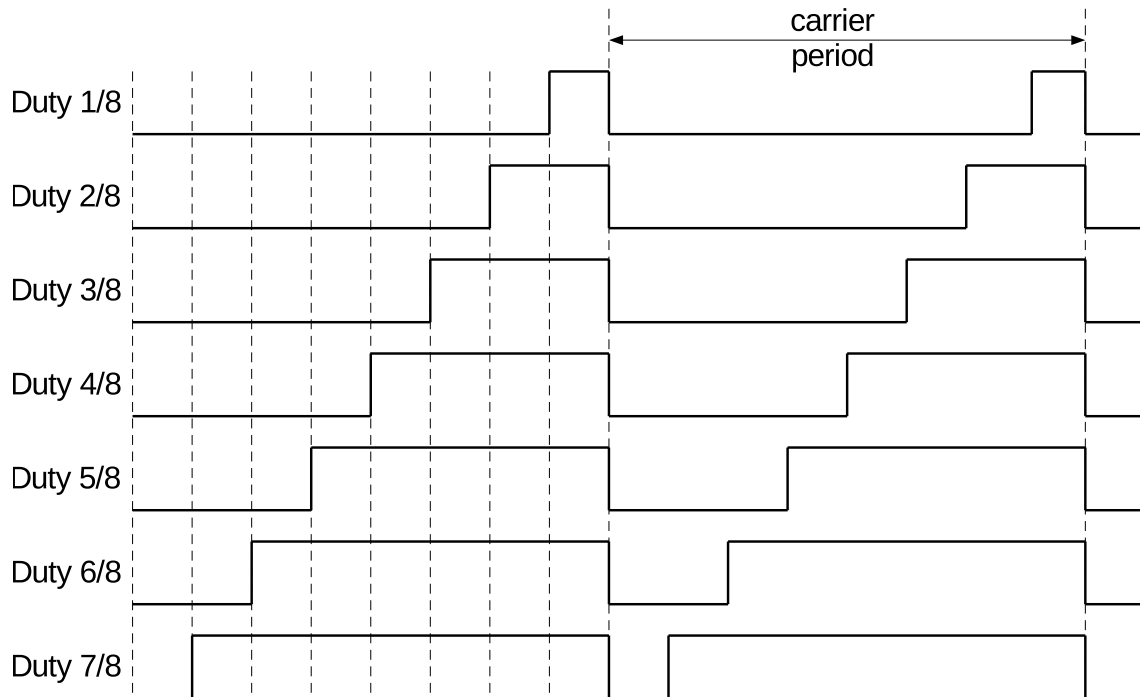


Figure 51.3-28. Possible Duty Cycle Settings for Sustaining Pulses in the PWM Carrier Submodule

#### 51.3.3.4 Fault Detection Module

Each MCPWM peripheral is connected to three fault signals (FAULT0, FAULT1, and FAULT2) which are sourced from the GPIO matrix. These signals are intended to indicate external fault conditions, and may be preprocessed by the Fault Detection module to generate fault events. Fault events can then execute the user code to control MCPWM outputs in response to specific faults.

##### Function of Fault Detection Module

The key actions performed by the fault detection module are:

- Forcing outputs PWMxA and PWMxB, upon detected fault, to one of the following states:
  - High
  - Low
  - Toggle
  - No action taken
- Execution of one-shot trip (OST) upon detection of over-current conditions/short circuits.
- Cycle-by-cycle trip (CBC) to provide current-limiting operation.
- Allocation of either one-shot or cycle-by-cycle operation for each fault signal.
- Generation of interrupts for each fault input.
- Support for software-force tripping.
- Enabling or disabling of module function as required.

## Operation and Configuration Tips

This section provides the operational tips and set-up options for the Fault Detection module.

Fault signals coming from pins are sampled and synced in the GPIO matrix. In order to guarantee the successful sampling of fault pulses, each pulse duration must be at least two APB clock cycles. The Fault Detection module will then sample fault signals by using PWM\_clk. So, the duration of fault pulses coming from GPIO matrix must be at least one PWM\_clk cycle. Differently put, regardless of the period relation between APB clock and PWM\_clk, the width of fault signal pulses on pins must be at least equal to the sum of two APB clock cycles and one PWM\_clk cycle.

Each level of fault signals, FAULT0 to FAULT2, can be used by the Fault Detection module to generate fault events (fault\_event0 to fault\_event2). Every fault event can be configured individually to provide CBC action, OST action, or none.

- **Cycle-by-Cycle (CBC) action:**

When CBC action is triggered, the state of PWMxA and PWMxB will be changed immediately according to the configuration of fields [MCPWM\\_TZn\\_A\\_CBC\\_U/D](#) and [MCPWM\\_TZn\\_B\\_CBC\\_U/D](#). Different actions can be indicated when the PWM timer is incrementing or decrementing. Different CBC action interrupts can be triggered for different fault events. Status field [MCPWM\\_TZn\\_CBC\\_ON](#) indicates whether a CBC action is on or off. When the fault event is no longer present, CBC actions on PWMxA/B will be cleared at a specified point, which is either a D/UTEP or D/UTEZ event. Field [MCPWM\\_TZn\\_CBCPULSE](#) determines at which event PWMxA and PWMxB will be able to resume normal actions. Therefore, in this mode, the CBC action is cleared or refreshed upon every PWM cycle.

- **One-Shot (OST) action:**

When OST action is triggered, the state of PWMxA and PWMxB will be changed immediately, depending on the setting of fields [MCPWM\\_TZn\\_A\\_OST\\_U/D](#) and [MCPWM\\_TZn\\_B\\_OST\\_U/D](#). Different actions can be configured when PWM timer is incrementing or decrementing. Different OST action interrupts can be triggered from different fault events. Status field [MCPWM\\_TZn\\_OST\\_ON](#) indicates whether an OST action is on or off. The OST actions on PWMxA/B are not automatically cleared when the fault event is no longer present. One-shot actions must be cleared manually by setting the [MCPWM\\_TZn\\_CLR\\_OST](#) bit.

## 51.3.4 Capture Module

### 51.3.4.1 Introduction

The capture module contains three complete capture channels. Channel inputs CAPO, CAP1, and CAP2 are sourced from the GPIO matrix. Thanks to the flexibility of the GPIO matrix, CAPO, CAP1, and CAP2 can be configured from any pin input. Multiple capture channels can be sourced from the same pin input, while prescaling for each channel can be set differently. Also, capture channels are sourced from different pins. This provides several options for handling capture signals by hardware in the background, instead of having them processed directly by the CPU. A capture module has the following independent key resources:

- One 32-bit timer (counter) which can be synchronized with the PWM timer, another module, or software.
- Three capture channels, each equipped with a 32-bit time-stamp and a capture prescaler.
- Independent edge polarity (rising/falling edge) selection for any capture channel.
- Input capture signal prescaling (from 1 to 256).

- Interrupt capabilities on any of the three capture events.

### 51.3.4.2 Capture Timer

The capture timer is a 32-bit counter incrementing continuously. It is enabled by setting `MCPWM_CAP_TIMER_EN` to 1. Its operating clock source is MCPWM core clock. When `MCPWM_CAP_SYNCI_EN` is configured, the counter will be loaded with phase stored in register `MCPWM_CAP_TIMER_PHASE_REG` at the time of a sync event. Sync events can select from PWM timers sync-out, or PWM module sync-in by configuring `MCPWM_CAP_SYNCI_SEL`. Sync events can also be generated by setting `MCPWM_CAP_SYNC_SW`. The capture timer provides timing references for all three capture channels.

### 51.3.4.3 Capture Channel

The capture signal coming to a capture channel will be inverted first, if needed, and then prescaled. Each capture channel has a prescaler register of `MCPWM_CAPn_PRESCALE`. Finally, specified edges of preprocessed capture signal will trigger capture events. Setting `MCPWM_CAPn_EN` to enable a capture channel. The capture event occurs at the time selected by the `MCPWM_CAPn_MODE`. When a capture event occurs, the capture timer's value is stored in time-stamp register `MCPWM_CAP_CHn_REG`. Different interrupts can be generated for different capture channels at capture events. The edge that triggers a capture event is recorded in register `MCPWM_CAPn_EDGE`. The capture event can be also forced by software setting `MCPWM_CAPn_SW`.

## 51.3.5 ETM Module

### 51.3.5.1 Overview

The MCPWM peripheral on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows MCPWM's ETM tasks to be triggered by any peripherals' ETM events, or MCPWM's ETM events to trigger any peripherals' ETM tasks. The capture module, the fault detection module, three timers, and three operators can generate events and respond to tasks independently. This section introduces the ETM tasks and events related to MCPWM. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

### 51.3.5.2 MCPWM-Related ETM Events

When setting enable field to 1, after the generation condition is met, the corresponding event would be generated. For details, please refer to Table 51.3-7 below:

Table 51.3-7. MCPWM-Related ETM Events

| Enable Field                                 | Generation Condition   | Event Generated                                       |
|--|--|---|
| <code>MCPWM_EVT_CAP<sub>n</sub>_EN</code>    | CAP <sub>n</sub> capture event occurs                                    | <code>MCPWM<sub>m</sub>_EVT_CAP<sub>n</sub></code>    |
| <code>MCPWM_EVT_TZ<sub>n</sub>_OST_EN</code> | PWM operator <sub>n</sub> performs a One-Shot trip (OST) operation       | <code>MCPWM<sub>m</sub>_EVT_TZ<sub>n</sub>_OST</code> |
| <code>MCPWM_EVT_TZ<sub>n</sub>_CBC_EN</code> | PWM operator <sub>n</sub> performs a cycle-by-cycle trip (CBC) operation | <code>MCPWM<sub>m</sub>_EVT_TZ<sub>n</sub>_CBC</code> |
| <code>MCPWM_EVT_F<sub>n</sub>_CLR_EN</code>  | Fault event fault_event <sub>n</sub> is cleared                          | <code>MCPWM<sub>m</sub>_EVT_F<sub>n</sub>_CLR</code>  |

<sup>1</sup> See Section 51.3.3.1 for a detailed description of timer stamp A and B.

| Enable Field             | Generation Condition  | Event Generated            |
|--------------------------|---|----------------------------|
| MCPWM_EVT_Fn_EN          | Fault event fault_event $n$ is generated  | MCPWM $m$ _EVT_Fn          |
| MCPWM_EVT_OPn_TEB_EN     | The count value of the timer that PWM operator $n$ selects is equal to the value of timer stamp B <sup>1</sup>      | MCPWM $m$ _EVT_OPn_TEB     |
| MCPWM_EVT_OPn_TEA_EN     | The count value of the timer that PWM operator $n$ selects is equal to the value of timer stamp A <sup>1</sup>      | MCPWM $m$ _EVT_OPn_TEA     |
| MCPWM_EVT_OPn_TEE1_EN    | The count value of the timer that PWM operator $n$ selects is equal to the value of register MCPWM_OPn_TSTMP_E1_REG | MCPWM $m$ _EVT_OPn_TEE1    |
| MCPWM_EVT_OPn_TEE2_EN    | The count value of the timer that PWM operator $n$ selects is equal to the value of register MCPWM_OPn_TSTMP_E2_REG | MCPWM $m$ _EVT_OPn_TEE2    |
| MCPWM_EVT_TIMERn_TEP_EN  | The count value of timer $n$ is equal to the period value MCPWM_TIMERn_PERIOD                                       | MCPWM $m$ _EVT_TIMERn_TEP  |
| MCPWM_EVT_TIMERn_TEZ_EN  | The count value of timer $n$ is equal to 0  | MCPWM $m$ _EVT_TIMERn_TEZ  |
| MCPWM_EVT_TIMERn_STOP_EN | Timer $n$ 's count stops  | MCPWM $m$ _EVT_TIMERn_STOP |

<sup>1</sup> See Section 51.3.3.1 for a detailed description of timer stamp A and B.

### 51.3.5.3 MCPWM-Related ETM Tasks

When setting the enable field to 1, after inputting valid tasks, the corresponding response operation would be generated. For details, please refer to Table 51.3-8 below:

Table 51.3-8. ETM Related Tasks

| Enable Field                   | Valid Task Input                 | Response Operation  |
|--------------------------------|----------------------------------|---|
| MCPWM_TASK_CAPn_EN             | MCPWM $m$ _TASK_CAPn             | CAP $n$ channel performs a capture operation  |
| MCPWM_TASK_CLRn_OST_EN         | MCPWM $m$ _TASK_CLRn_OST         | PWM operator $n$ clears the One-Shot Trip operation   |
| MCPWM_TASK_TZn_OST_EN          | MCPWM $m$ _TASK_TZn_OST          | PWM operator $n$ performs a One-Shot Trip (OST) operation   |
| MCPWM_TASK_TIMERn_PERIOD_UP_EN | MCPWM $m$ _TASK_TIMERn_PERIOD_UP | The period of timer $n$ is updated to the value configured in the period register MCPWM_TIMERn_PERIOD |
| MCPWM_TASK_TIMERn_SYNC_EN      | MCPWM $m$ _TASK_TIMERn_SYNC      | Timer $n$ performs a sync operation   |
| MCPWM_TASK_GEN_STOP_EN         | MCPWM $m$ _TASK_GEN_STOP         | All the timers stop counting and the PWM signals output by all PWM operators remain unchanged         |

| Enable Field                 | Valid Task Input               | Response Operation  |
|------------------------------|--------------------------------|---|
| MCPWM_TASK_CMPR $n$ _B_UP_EN | MCPWM $m$ _TASK_CMPR $n$ _B_UP | Timer stamp B of the PWM operator $n$ is updated to the value of the shadow register MCPWM_GEN $n$ _B |
| MCPWM_TASK_CMPR $n$ _A_UP_EN | MCPWM $m$ _TASK_CMPR $n$ _A_UP | Timer stamp A of the PWM operator $n$ is updated to the value of the shadow register MCPWM_GEN $n$ _A |

## 51.4 Interrupts

ESP32-P4's MCPWM0 can generate the PWM0\_INTR interrupt signal and MCPWM1 can generate the PWM1\_INTR interrupt signal. The PWM $n$ \_INTR will be sent to the [Interrupt Matrix](#).

Interrupt signal PWM $n$ \_INTR can be generated by the following internal interrupt sources:

- MCPWM\_TIMER $x$ \_STOP\_INT: Triggered when timer $x$  stops.
- MCPWM\_TIMER $x$ \_TEZ\_INT: Triggered by the TEZ event of PWM timer $x$ .
- MCPWM\_TIMER $x$ \_TEP\_INT: Triggered by the TEP event of PWM timer $x$ .
- MCPWM\_FAULT $x$ \_INT: Triggered when fault\_event $x$  starts.
- MCPWM\_FAULT $x$ \_CLR\_INT: Triggered after fault\_event $x$  ends.
- MCPWM\_CMPR $x$ \_TEA\_INT: Triggered by the TEA event of PWM operator $x$ .
- MCPWM\_CMPR $x$ \_TEB\_INT: Triggered by the TEB event of PWM operator $x$ .
- MCPWM\_TZ $x$ \_CBC\_INT: Triggered by the CBC action of PWM $x$ .
- MCPWM\_TZ $x$ \_OST\_INT: Triggered by the OST action of PWM $x$ .
- MCPWM\_CAP $x$ \_INT: Triggered by the capture event on channel $x$ .

The above interrupt sources can only be triggered when the interrupt enable register `interrupt_source_name_ENA` is set to 1. Write 1 to `interrupt_source_name_CLR` will clear the interrupt.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [51.5 Register Summary](#).



## 51.5 Register Summary

The addresses in this section are relative to Motor Control PWM base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <b>Prescaler Configuration</b>                   |   |         |        |
| <a href="#">MCPWM_CLK_CFG_REG</a>                | PWM clock prescaler register  | 0x0000  | R/W    |
| <b>MCPWM Timer 0 Configuration and Status</b>    |   |         |        |
| <a href="#">MCPWM_TIMER0_CFG0_REG</a>            | PWM timer0 period and update method configuration register            | 0x0004  | R/W    |
| <a href="#">MCPWM_TIMER0_CFG1_REG</a>            | PWM timer0 working mode and start/stop control configuration register | 0x0008  | varies |
| <a href="#">MCPWM_TIMER0_SYNC_REG</a>            | PWM timer0 sync function configuration register                       | 0x000C  | R/W    |
| <a href="#">MCPWM_TIMER0_STATUS_REG</a>          | PWM timer0 status register  | 0x0010  | RO     |
| <b>MCPWM Timer 1 Configuration and Status</b>    |   |         |        |
| <a href="#">MCPWM_TIMER1_CFG0_REG</a>            | PWM timer1 period and update method configuration register            | 0x0014  | R/W    |
| <a href="#">MCPWM_TIMER1_CFG1_REG</a>            | PWM timer1 working mode and start/stop control configuration register | 0x0018  | varies |
| <a href="#">MCPWM_TIMER1_SYNC_REG</a>            | PWM timer1 sync function configuration register                       | 0x001C  | R/W    |
| <a href="#">MCPWM_TIMER1_STATUS_REG</a>          | PWM timer1 status register  | 0x0020  | RO     |
| <b>MCPWM Timer 2 Configuration and status</b>    |   |         |        |
| <a href="#">MCPWM_TIMER2_CFG0_REG</a>            | PWM timer2 period and update method configuration register            | 0x0024  | R/W    |
| <a href="#">MCPWM_TIMER2_CFG1_REG</a>            | PWM timer2 working mode and start/stop control configuration register | 0x0028  | varies |
| <a href="#">MCPWM_TIMER2_SYNC_REG</a>            | PWM timer2 sync function configuration register                       | 0x002C  | R/W    |
| <a href="#">MCPWM_TIMER2_STATUS_REG</a>          | PWM timer2 status register  | 0x0030  | RO     |
| <b>Common Configuration for MCPWM Timers</b>     |   |         |        |
| <a href="#">MCPWM_TIMER_SYNCI_CFG_REG</a>        | Synchronization input selection for three PWM timers                  | 0x0034  | R/W    |
| <a href="#">MCPWM_OPERATOR_TIMERSEL_REG</a>      | Select specific timer for PWM operators                               | 0x0038  | R/W    |
| <b>MCPWM Operator 0 Configuration and Status</b> |   |         |        |
| <a href="#">MCPWM_GEN0_STMP_CFG_REG</a>          | Transfer status and update method for time stamp registers A and B    | 0x003C  | varies |
| <a href="#">MCPWM_GEN0_TSTMP_A_REG</a>           | Shadow register for register A  | 0x0040  | R/W    |
| <a href="#">MCPWM_GEN0_TSTMP_B_REG</a>           | Shadow register for register B  | 0x0044  | R/W    |
| <a href="#">MCPWM_GEN0_CFG0_REG</a>              | Fault event T0 and T1 handling  | 0x0048  | R/W    |
| <a href="#">MCPWM_GEN0_FORCE_REG</a>             | Permissives to force PWMOA and PWMOB outputs by software              | 0x004C  | R/W    |

| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">MCPWM_GEN0_A_REG</a>                 | Actions triggered by events on PWM0A                               | 0x0050  | R/W    |
| <a href="#">MCPWM_GEN0_B_REG</a>                 | Actions triggered by events on PWM0B                               | 0x0054  | R/W    |
| <a href="#">MCPWM_DTO_CFG_REG</a>                | Dead time type selection and configuration                         | 0x0058  | R/W    |
| <a href="#">MCPWM_DTO_FED_CFG_REG</a>            | Shadow register for falling edge delay (FED)                       | 0x005C  | R/W    |
| <a href="#">MCPWM_DTO_RED_CFG_REG</a>            | Shadow register for rising edge delay (RED)                        | 0x0060  | R/W    |
| <a href="#">MCPWM_CARRIER0_CFG_REG</a>           | Carrier enable and configuratoin                                   | 0x0064  | R/W    |
| <a href="#">MCPWM_FH0_CFG0_REG</a>               | Actions on PWM0A and PWM0B trip events                             | 0x0068  | R/W    |
| <a href="#">MCPWM_FH0_CFG1_REG</a>               | Software triggers for fault handler actions                        | 0x006C  | R/W    |
| <a href="#">MCPWM_FH0_STATUS_REG</a>             | Status of fault events   | 0x0070  | RO     |
| <b>MCPWM Operator 1 Configuration and Status</b> |  |         |        |
| <a href="#">MCPWM_GEN1_STMP_CFG_REG</a>          | Transfer status and update method for time stamp registers A and B | 0x0074  | varies |
| <a href="#">MCPWM_GEN1_TSTMP_A_REG</a>           | Shadow register for register A                                     | 0x0078  | R/W    |
| <a href="#">MCPWM_GEN1_TSTMP_B_REG</a>           | Shadow register for register B                                     | 0x007C  | R/W    |
| <a href="#">MCPWM_GEN1_CFG0_REG</a>              | Fault event T0 and T1 handling                                     | 0x0080  | R/W    |
| <a href="#">MCPWM_GEN1_FORCE_REG</a>             | Permissives to force PWM1A and PWM1B outputs by software           | 0x0084  | R/W    |
| <a href="#">MCPWM_GEN1_A_REG</a>                 | Actions triggered by events on PWM1A                               | 0x0088  | R/W    |
| <a href="#">MCPWM_GEN1_B_REG</a>                 | Actions triggered by events on PWM1B                               | 0x008C  | R/W    |
| <a href="#">MCPWM_DT1_CFG_REG</a>                | Dead time type selection and configuration                         | 0x0090  | R/W    |
| <a href="#">MCPWM_DT1_FED_CFG_REG</a>            | Shadow register for falling edge delay (FED)                       | 0x0094  | R/W    |
| <a href="#">MCPWM_DT1_RED_CFG_REG</a>            | Shadow register for rising edge delay (RED)                        | 0x0098  | R/W    |
| <a href="#">MCPWM_CARRIER1_CFG_REG</a>           | Carrier enable and configuratoin                                   | 0x009C  | R/W    |
| <a href="#">MCPWM_FH1_CFG0_REG</a>               | Actions on PWM1A and PWM1B trip events                             | 0x00A0  | R/W    |
| <a href="#">MCPWM_FH1_CFG1_REG</a>               | Software triggers for fault handler actions                        | 0x00A4  | R/W    |
| <a href="#">MCPWM_FH1_STATUS_REG</a>             | Status of fault events   | 0x00A8  | RO     |
| <b>MCPWM Operator 2 Configuration and Status</b> |  |         |        |
| <a href="#">MCPWM_GEN2_STMP_CFG_REG</a>          | Transfer status and update method for time stamp registers A and B | 0x00AC  | varies |
| <a href="#">MCPWM_GEN2_TSTMP_A_REG</a>           | Shadow register for register A                                     | 0x00B0  | R/W    |
| <a href="#">MCPWM_GEN2_TSTMP_B_REG</a>           | Shadow register for register B                                     | 0x00B4  | R/W    |
| <a href="#">MCPWM_GEN2_CFG0_REG</a>              | Fault event T0 and T1 handling                                     | 0x00B8  | R/W    |
| <a href="#">MCPWM_GEN2_FORCE_REG</a>             | Permissives to force PWM2A and PWM2B outputs by software           | 0x00BC  | R/W    |
| <a href="#">MCPWM_GEN2_A_REG</a>                 | Actions triggered by events on PWM2A                               | 0x00C0  | R/W    |
| <a href="#">MCPWM_GEN2_B_REG</a>                 | Actions triggered by events on PWM2B                               | 0x00C4  | R/W    |
| <a href="#">MCPWM_DT2_CFG_REG</a>                | Dead time type selection and configuration                         | 0x00C8  | R/W    |
| <a href="#">MCPWM_DT2_FED_CFG_REG</a>            | Shadow register for falling edge delay (FED)                       | 0x00CC  | R/W    |
| <a href="#">MCPWM_DT2_RED_CFG_REG</a>            | Shadow register for rising edge delay (RED)                        | 0x00D0  | R/W    |
| <a href="#">MCPWM_CARRIER2_CFG_REG</a>           | Carrier enable and configuratoin                                   | 0x00D4  | R/W    |
| <a href="#">MCPWM_FH2_CFG0_REG</a>               | Actions on PWM2A and PWM2B trip events                             | 0x00D8  | R/W    |
| <a href="#">MCPWM_FH2_CFG1_REG</a>               | Software triggers for fault handler actions                        | 0x00DC  | R/W    |
| <a href="#">MCPWM_FH2_STATUS_REG</a>             | Status of fault events   | 0x00E0  | RO     |

| Name  | Description   | Address | Access       |
|---|---|---------|--------------|
| <b>Fault Detection Configuration and Status</b> |   |         |              |
| <a href="#">MCPWM_FAULT_DETECT_REG</a>          | Fault detection configuration and status              | 0x00E4  | varies       |
| <b>Capture Configuration and Status</b>         |   |         |              |
| <a href="#">MCPWM_CAP_TIMER_CFG_REG</a>         | Configure capture timer                               | 0x00E8  | varies       |
| <a href="#">MCPWM_CAP_TIMER_PHASE_REG</a>       | Phase for capture timer sync                          | 0x00EC  | R/W          |
| <a href="#">MCPWM_CAP_CHO_CFG_REG</a>           | Capture channel 0 configuration and enable            | 0x00F0  | varies       |
| <a href="#">MCPWM_CAP_CH1_CFG_REG</a>           | Capture channel 1 configuration and enable            | 0x00F4  | varies       |
| <a href="#">MCPWM_CAP_CH2_CFG_REG</a>           | Capture channel 2 configuration and enable            | 0x00F8  | varies       |
| <a href="#">MCPWM_CAP_CHO_REG</a>               | ch0 capture value status register                     | 0x00FC  | RO           |
| <a href="#">MCPWM_CAP_CH1_REG</a>               | ch1 capture value status register                     | 0x0100  | RO           |
| <a href="#">MCPWM_CAP_CH2_REG</a>               | ch2 capture value status register                     | 0x0104  | RO           |
| <a href="#">MCPWM_CAP_STATUS_REG</a>            | Edge of last capture trigger                          | 0x0108  | RO           |
| <b>Enable Update of Active Registers</b>        |   |         |              |
| <a href="#">MCPWM_UPDATE_CFG_REG</a>            | Enable update   | 0x010C  | R/W          |
| <b>Manage Interrupts</b>                        |   |         |              |
| <a href="#">MCPWM_INT_ENA_REG</a>               | Interrupt enable bits                                 | 0x0110  | R/W          |
| <a href="#">MCPWM_INT_RAW_REG</a>               | Raw interrupt status                                  | 0x0114  | R/WTC<br>/SS |
| <a href="#">MCPWM_INT_ST_REG</a>                | Masked interrupt status                               | 0x0118  | RO           |
| <a href="#">MCPWM_INT_CLR_REG</a>               | Interrupt clear bits                                  | 0x011C  | WT           |
| <b>MCPWM Event Enable Registers</b>             |   |         |              |
| <a href="#">MCPWM_EVT_EN_REG</a>                | MCPWM event enable register                           | 0x0120  | R/W          |
| <a href="#">MCPWM_EVT_EN2_REG</a>               | MCWM event enable register2                           | 0x0128  | R/W          |
| <b>MCPWM Task Enable Register</b>               |   |         |              |
| <a href="#">MCPWM_TASK_EN_REG</a>               | MCPWM task enable register                            | 0x0124  | R/W          |
| <b>MCPWM Generator Configuration Registers</b>  |   |         |              |
| <a href="#">MCPWM_OPO_TSTMP_E1_REG</a>          | Generator0 time stamp E1 value configuration register | 0x012C  | R/W          |
| <a href="#">MCPWM_OPO_TSTMP_E2_REG</a>          | Generator0 time stamp E2 value configuration register | 0x0130  | R/W          |
| <a href="#">MCPWM_OP1_TSTMP_E1_REG</a>          | Generator1 time stamp E1 value configuration register | 0x0134  | R/W          |
| <a href="#">MCPWM_OP1_TSTMP_E2_REG</a>          | Generator1 time stamp E2 value configuration register | 0x0138  | R/W          |
| <a href="#">MCPWM_OP2_TSTMP_E1_REG</a>          | Generator2 time stamp E1 value configuration register | 0x013C  | R/W          |
| <a href="#">MCPWM_OP2_TSTMP_E2_REG</a>          | Generator2 time stamp E2 value configuration register | 0x0140  | R/W          |
| <b>MCPWM APB Configuration Register</b>         |   |         |              |
| <a href="#">MCPWM_CLK_REG</a>                   | MCPWM APB configuration register                      | 0x0144  | R/W          |
| <b>Version Register</b>                         |   |         |              |
| <a href="#">MCPWM_VERSION_REG</a>               | Version control register                              | 0x0148  | R/W          |

## 51.6 Registers

The addresses in this section are relative to Motor Control PWM base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 51.1. MCPWM\_CLK\_CFG\_REG (0x0000)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                    |   |   |  |  |  |  |  |       |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------|---|---|--|--|--|--|--|-------|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CLK_PRESCALE |   |   |  |  |  |  |  |       |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8                  | 7 | 0 |  |  |  |  |  |       |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x0                |   |   |  |  |  |  |  | Reset |  |

**MCPWM\_CLK\_PRESCALE** Configures the prescaler value of the clock, so that the period of  $PWM\_clk = 6.25ns * (PWM\_CLK\_PRESCALE + 1)$ . (R/W)

**Register 51.2. MCPWM\_TIMER<sub>n</sub>\_CFG0\_REG (*n*: 0-2) (0x0004+0x10\**n*)**

|            |  |  |  |  |  |   |  |  |  |  |  |    |  |    |  |    |  |   |  |      |  |  |  |                                  |  |  |  |  |  |  |  |   |  |     |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|---|--|--|--|--|--|----|--|----|--|----|--|---|--|------|--|--|--|----------------------------------|--|--|--|--|--|--|--|---|--|-----|--|--|--|--|--|--|--|------------------------------------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  | MCPWM_TIMER <sub>n</sub> _PERIOD_UPMETHOD |  |  |  |  |  |    |  |    |  |    |  |   |  |      |  |  |  | MCPWM_TIMER <sub>n</sub> _PERIOD |  |  |  |  |  |  |  |   |  |     |  |  |  |  |  |  |  | MCPWM_TIMER <sub>n</sub> _PRESCALE |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  | 26  |  |  |  |  |  | 25 |  | 24 |  | 23 |  |   |  |      |  |  |  |                                  |  |  |  |  |  |  |  | 8 |  | 7   |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  | 0   |  |  |  |  |  | 0  |  | 0  |  | 0  |  | 0 |  | 0xff |  |  |  |                                  |  |  |  |  |  |  |  |   |  | 0x0 |  |  |  |  |  |  |  |                                    |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |

**MCPWM\_TIMER<sub>n</sub>\_PRESCALE** Configures the prescaler value of timer<sub>n</sub>, so that the period of  $PTO\_clk = \text{Period of } PWM\_clk * (PWM\_TIMER_n\_PRESCALE + 1)$ . (R/W)

**MCPWM\_TIMER<sub>n</sub>\_PERIOD** Configures the period shadow of PWM timer<sub>n</sub>.  
(R/W)

**MCPWM\_TIMER<sub>n</sub>\_PERIOD\_UPMETHOD** Configures the update method for active register of PWM timer<sub>n</sub> period.

0: Immediate

1: TEZ

2: Sync

3: TEZ or sync

TEZ here and below means timer equals zero event.

(R/W)

Register 51.3. MCPWM\_TIMERn\_CFG1\_REG(*n*: 0-2) (0x0008+0x10\**n*)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |   |                    |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------|---|--------------------|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_TIMERn_MOD |   | MCPWM_TIMERn_START |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5 | 4                | 3 | 2                  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0              |   | 0x0                | Reset |

**MCPWM\_TIMERn\_START** Configures conditions to start/stop PWM timer*n*.

- 0: If PWM timer0 starts, then stops at TEZ
- 1: If timer0 starts, then stops at TEP
- 2: PWM timer0 starts and runs on
- 3: Timer0 starts and stops at the next TEZ
- 4: Timer0 starts and stops at the next TEP
- 5: Invalid. No effect
- 6: Invalid. No effect
- 7: Invalid. No effect

TEP here and below means the event that happens when the timer equals to period.

(R/W/SC)

**MCPWM\_TIMERn\_MOD** Configures the working mode of PWM timer*n*.

- 0: Freeze
- 1: Increase mode
- 2: Decrease mode
- 3: Up-down mode

(R/W)

Register 51.4. MCPWM\_TIMER $n$ \_SYNC\_REG ( $n$ : 0-2) (0x000C+0x10\* $n$ )

|            |   |   |   |   |   |   |   |   |   |    |   |    |                                   |  |  |   |   |       |   |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|----|---|----|-----------------------------------|--|--|---|---|-------|---|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |    | MCPWM_TIMER <sub>n</sub> _PHASE_DIRECTION |    | MCPWM_TIMER <sub>n</sub> _SYNC_SW |  |  |   |   |       |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   | 21 | 20  | 19 |                                   |  |  |   | 4 | 3     | 2 | 1 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0   | 0  |                                   |  |  | 0 | 0 | 0     | 0 | 0 |   |  |
|            |   |   |   |   |   |   |   |   |   |    |   |    |                                   |  |  |   |   | Reset |   |   |   |  |

**MCPWM\_TIMERn\_SYNCI\_EN** Configures whether to enable timer $n$  reloading with phase on sync input event.

0: Disable

1: Enable

(R/W)

**MCPWM\_TIMER $n$ \_SYNC\_SW** Configures whether to trigger a software sync.

0: No effect

1: Trigger a software sync

(R/W)

**MCPWM\_TIMER $n$ \_SYNCO\_SEL** Configures PWM timer $n$  sync out selection.

0: sync\_in. The sync out will always generate when toggling the `MCPWM_TIMER0_SYNC_SW` bit.

1: TEZ

2: TEP

3: No effect

(R/W)

**MCPWM\_TIMER $n$ \_PHASE** Configures the phase for timer $n$  reload on sync event.

(R/W)

**MCPWM\_TIMER $n$ \_PHASE\_DIRECTION** Configures the PWM timer $n$ 's direction when timer $n$  mode is up-down mode.

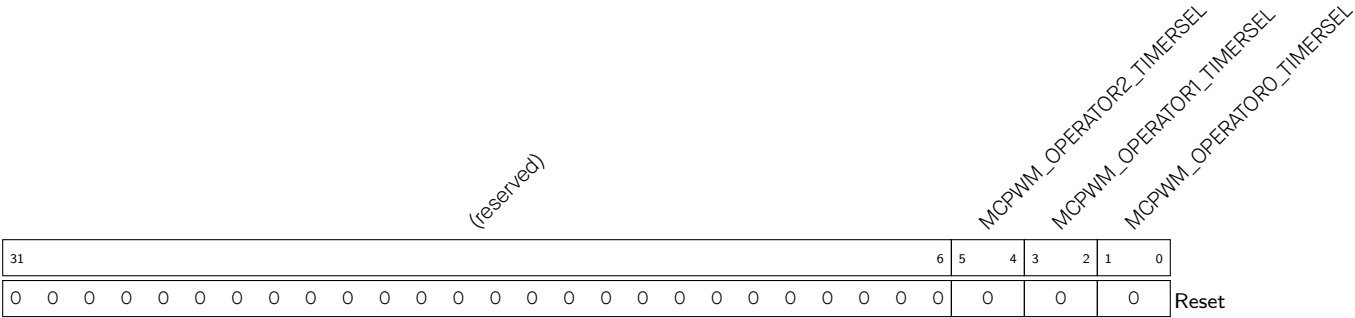
0: Increase

1: Decrease

(R/W)



Register 51.7. MCPWM\_OPERATOR\_TIMERSEL\_REG (0x0038)



**MCPWM\_OPERATOR***n***\_TIMERSEL** Configures which PWM timer will be the timing reference for PWM operator*n*.

0: timer0

1: timer1

2: timer2

3: Invalid, will select timer2

(R/W)



**Register 51.8. MCPWM\_GEN $n$ \_STMP\_CFG\_REG ( $n$ : 0-2) (0x003C+0x38\* $n$ )**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                      |   |   |   |                                      |   |  |   |                                     |  |       |  |                                     |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------------------------------|---|---|---|--------------------------------------|---|--|---|-------------------------------------|--|-------|--|-------------------------------------|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CMPR <sub>n</sub> _B_SHDW_FULL |   |   |   | MCPWM_CMPR <sub>n</sub> _A_SHDW_FULL |   |  |   | MCPWM_CMPR <sub>n</sub> _B_UPMETHOD |  |       |  | MCPWM_CMPR <sub>n</sub> _A_UPMETHOD |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 10                                   |   | 9 | 8 | 7                                    | 4 |  | 3 | 0                                   |  | Reset |  |                                     |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                    | 0 | 0 |   | 0                                    |   |  |   |                                     |  |       |  |                                     |  |  |  |

**MCPWM\_CMPR $n$ \_A\_UPMETHOD** Configures the update method for PWM generator $n$  time stamp A's active register.

When all bits are set to 0: Immediately

When bit0 is set to 1: TEZ

When bit1 is set to 1: TEP

When bit2 is set to 1: Sync

When bit3 is set to 1: Disable the update

(R/W)

**MCPWM\_CMPR $n$ \_B\_UPMETHOD** Configures the update method for PWM generator $n$  time stamp B's active register.

When all bits are set to 0: Immediately

When bit0 is set to 1: TEZ

When bit1 is set to 1: TEP

When bit2 is set to 1: Sync

When bit3 is set to 1: Disable the update

(R/W)

**MCPWM\_CMPR $n$ \_A\_SHDW\_FULL** Configures whether the value in the shadow register is written to the corresponding active register at a specific time. This field is set and reset by hardware.

0: Write the latest value in the shadow register to A's active register

1: Write the value to the PWM generator $n$  time stamp A's shadow register, and wait to be transferred to A's active register

(R/SC/WTC)

**MCPWM\_CMPR $n$ \_B\_SHDW\_FULL** Configures whether the value in the shadow register is written to the corresponding active register at a specific time. This field is set and reset by hardware.

0: Write the latest value in the shadow register to B's active register

1: Write the value to the PWM generator $n$  time stamp B's shadow register, and wait to be transferred to B's active register

(R/SC/WTC)

Register 51.9. MCPWM\_GEN $n$ \_TSTMP\_A\_REG( $n$ : 0-2) (0x0040+0x38\* $n$ )

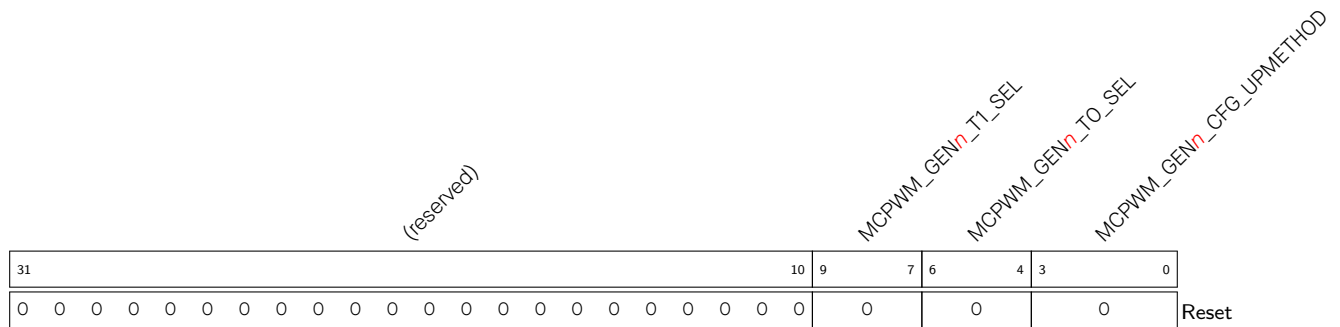
|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CMPR <sub>n</sub> _A |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**MCPWM\_CMPR $n$ \_A** Configures the value of PWM generator  $n$  time stamp A's shadow register.  
(R/W)

Register 51.10. MCPWM\_GEN $n$ \_TSTMP\_B\_REG( $n$ : 0-2) (0x0044+0x38\* $n$ )

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CMPR <sub>n</sub> B |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**MCPWM\_CMPR $n$ \_B** Configures the value of PWM generator  $n$  time stamp B's shadow register.  
(R/W)

Register 51.11. MCPWM\_GEN $n$ \_CFG\_REG( $n$ : 0-2) (0x0048+0x38\* $n$ )

**MCPWM\_GEN $n$ \_CFG\_UPMETHOD** Configures the update method for PWM generator $n$ 's active register.

When all bits are set to 0: Immediately

When bit0 is set to 1: TEZ

When bit1 is set to 1: TEP

When bit2 is set to 1: Sync

When bit3 is set to 1: Disable the update

(R/W)

**MCPWM\_GEN $n$ \_TO\_SEL** Configures source selection for PWM generator $n$  event\_t0, take effect immediately.

0: fault\_event0

1: fault\_event1

2: fault\_event2

3: sync\_taken

4: Invalid, selects nothing

(R/W)

**MCPWM\_GEN $n$ \_T1\_SEL** Configures source selection for PWM generator $n$  event\_t1, take effect immediately.

0: fault\_event0

1: fault\_event1

2: fault\_event2

3: sync\_taken

4: Invalid, selects nothing

(R/W)

**Register 51.12. MCPWM\_GEN $n$ \_FORCE\_REG( $n$ : 0-2) (0x004C+0x38\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |      |    |  |    |   |       |   |   |   |  |  |  |  |  |   |  |  |                                  |  |  |  |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|------|----|--|----|---|-------|---|---|---|--|--|--|--|--|---|--|--|----------------------------------|--|--|--|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_GEN <sub>n</sub> _B_NCIFORCE_MODE |    |    |      |    | MCPWM_GEN <sub>n</sub> _B_CNTUFORCE_MODE |    |   |       |   | MCPWM_GEN <sub>n</sub> _A_NCIFORCE_MODE |   |  |  |  | MCPWM_GEN <sub>n</sub> _A_CNTUFORCE_MODE |  |   |  |  | MCPWM_GEN <sub>n</sub> _UPMETHOD |  |  |  |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                                      | 15 | 14 | 13   | 12 | 11                                       | 10 | 9 | 8     | 7 | 6                                       | 5 |  |  |  |  |  | 0 |  |  |                                  |  |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                       | 0  | 0  | 0x20 |    |  |    |   | Reset |   |   |   |  |  |  |  |  |   |  |  |                                  |  |  |  |  |

**MCPWM\_GEN $n$ \_CNTUFORCE\_UPMETHOD** Configures the update method for continuous software force of PWM generator $n$ .

When all bits are set to 0: Immediately

When bit0 is set to 1: TEZ

When bit1 is set to 1: TEP

When bit2 is set to 1: TEA

When bit3 is set to 1: TEB

When bit4 is set to 1: Sync

When bit5 is set to 1: Disable update

TEA/B means an event generated when the timer's value equals to that of register A/B.

(R/W)

**MCPWM\_GEN $n$ \_A\_CNTUFORCE\_MODE** Configures the continuous software force mode for PWM $n$

A.

0: Disabled

1: Low

2: High

3: Disabled

(R/W)

**MCPWM\_GEN $n$ \_B\_CNTUFORCE\_MODE** Configures the continuous software force mode for PWM $n$

B.

0: Disabled

1: Low

2: High

3: Disabled

(R/W)

**MCPWM\_GEN $n$ \_A\_NCIFORCE** Configures whether to trigger the non-continuous immediate software-force event for PWM $n$  A.

0: Invalid

1: Trigger a force event

(R/W)

Continued on the next page...

**Register 51.12. MCPWM\_GEN $n$ \_FORCE\_REG( $n$ : 0-2) (0x004C+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_GEN $n$ \_A\_NCIFORCE\_MODE** Configures non-continuous immediate software force mode for PWM $n$  A.

0: Disabled

1: Low

2: High

3: Disabled

(R/W)

**MCPWM\_GEN $n$ \_B\_NCIFORCE** Configures whether to trigger the non-continuous immediate software-force event for PWM $n$  B.

0: Invalid

1: Trigger a force event

(R/W)

**MCPWM\_GEN $n$ \_B\_NCIFORCE\_MODE** Configures non-continuous immediate software force mode for PWM $n$  B.

0: Disabled

1: Low

2: High

3: Disabled

(R/W)

Register 51.13. MCPWM\_GEN $n$ \_A\_REG( $n$ : 0-2) (0x0050+0x38\* $n$ )

| (reserved) |   |   |   |   |   |   |   | MCPWM_GEN <sub>n</sub> _A_DT1 |    | MCPWM_GEN <sub>n</sub> _A_DTO |    | MCPWM_GEN <sub>n</sub> _A_DTEB |    | MCPWM_GEN <sub>n</sub> _A_DTEA |    | MCPWM_GEN <sub>n</sub> _A_DTEP |    | MCPWM_GEN <sub>n</sub> _A_DTEZ |    | MCPWM_GEN <sub>n</sub> _A_UT1 |    | MCPWM_GEN <sub>n</sub> _A_UTO |   | MCPWM_GEN <sub>n</sub> _A_UTEB |   | MCPWM_GEN <sub>n</sub> _A_UTEA |   | MCPWM_GEN <sub>n</sub> _A_UTEZ |   |   |   |       |
|------------|---|---|---|---|---|---|---|-------------------------------|----|-------------------------------|----|--------------------------------|----|--------------------------------|----|--------------------------------|----|--------------------------------|----|-------------------------------|----|-------------------------------|---|--------------------------------|---|--------------------------------|---|--------------------------------|---|---|---|-------|
| 31         |   |   |   |   |   |   |   | 24                            | 23 | 22                            | 21 | 20                             | 19 | 18                             | 17 | 16                             | 15 | 14                             | 13 | 12                            | 11 | 10                            | 9 | 8                              | 7 | 6                              | 5 | 4                              | 3 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                             | 0  | 0                             | 0  | 0                              | 0  | 0                              | 0  | 0                              | 0  | 0                              | 0  | 0                             | 0  | 0                             | 0 | 0                              | 0 | 0                              | 0 | 0                              | 0 | 0 | 0 | Reset |

**MCPWM\_GEN $n$ \_A\_UTEZ** Configures action on PWM $n$  A triggered by event TEZ when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_A\_UTEZ** Configures action on PWM $n$  A triggered by event TEP when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_A\_UTEA** Configures action on PWM $n$  A triggered by event TEA when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_A\_UTEB** Configures action on PWM $n$  A triggered by event TEB when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

Continued on the next page...

**Register 51.13. MCPWM\_GEN $n$ \_A\_REG( $n$ : 0-2) (0x0050+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_GEN $n$ \_A\_UT0** Configures action on PWM $n$  A triggered by event\_t0 when timer increasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_A\_UT1** Configures action on PWM $n$  A triggered by event\_t1 when timer increasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_A\_DTEZ** Configures action on PWM $n$  A triggered by event TEZ when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_A\_DTEP** Configures action on PWM $n$  A triggered by event TEP when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_A\_DTEA** Configures action on PWM $n$  A triggered by event TEA when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

Continued on the next page...

**Register 51.13. MCPWM\_GEN $n$ \_A\_REG( $n$ : 0-2) (0x0050+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_GEN $n$ \_A\_DTEB** Configures action on PWM $n$  A triggered by event TEB when timer decreasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_A\_DTO** Configures action on PWM $n$  A triggered by event\_t0 when timer decreasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_A\_DT1** Configures action on PWM $n$  A triggered by event\_t1 when timer decreasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)



Register 51.14. MCPWM\_GEN $n$ \_B\_REG( $n$ : 0-2) (0x0054+0x38\* $n$ )

| (reserved) |   |    |    |    |    |    |    | MCPWM_GEN <sub>n</sub> _B_DT1 |    | MCPWM_GEN <sub>n</sub> _B_DTO |    | MCPWM_GEN <sub>n</sub> _B_DTEB |    | MCPWM_GEN <sub>n</sub> _B_DTEA |    | MCPWM_GEN <sub>n</sub> _B_DTEP |   | MCPWM_GEN <sub>n</sub> _B_DTEZ |   | MCPWM_GEN <sub>n</sub> _B_UT1 |   | MCPWM_GEN <sub>n</sub> _B_UTO |   | MCPWM_GEN <sub>n</sub> _B_UTEA |   | MCPWM_GEN <sub>n</sub> _B_UTEZ |       |
|------------|---|----|----|----|----|----|----|-------------------------------|----|-------------------------------|----|--------------------------------|----|--------------------------------|----|--------------------------------|---|--------------------------------|---|-------------------------------|---|-------------------------------|---|--------------------------------|---|--------------------------------|-------|
| 31         |   | 24 | 23 | 22 | 21 | 20 | 19 | 18                            | 17 | 16                            | 15 | 14                             | 13 | 12                             | 11 | 10                             | 9 | 8                              | 7 | 6                             | 5 | 4                             | 3 | 2                              | 1 | 0                              |       |
| 0          | 0 | 0  | 0  | 0  | 0  | 0  | 0  | 0                             | 0  | 0                             | 0  | 0                              | 0  | 0                              | 0  | 0                              | 0 | 0                              | 0 | 0                             | 0 | 0                             | 0 | 0                              | 0 | 0                              | Reset |

**MCPWM\_GEN $n$ \_B\_UTEZ** Configures action on PWM $n$  B triggered by event TEZ when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_B\_UTEZ** Configures action on PWM $n$  B triggered by event TEP when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_B\_UTEA** Configures action on PWM $n$  B triggered by event TEA when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_B\_UTEB** Configures action on PWM $n$  B triggered by event TEB when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_B\_UTO** Configures action on PWM $n$  B triggered by event\_t0 when timer increasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

Continued on the next page...

**Register 51.14. MCPWM\_GEN $n$ \_B\_REG( $n$ : 0-2) (0x0054+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_GEN $n$ \_B\_UT1** Configures action on PWM $n$  B triggered by event\_t1 when timer increasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_B\_DTEZ** Configures action on PWM $n$  B triggered by event TEZ when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_B\_DTEP** Configures action on PWM $n$  B triggered by event TEP when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_B\_DTEA** Configures action on PWM $n$  B triggered by event TEA when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

**MCPWM\_GEN $n$ \_B\_DTEB** Configures action on PWM $n$  B triggered by event TEB when timer decreasing.

- 0: No change
  - 1: Low
  - 2: High
  - 3: Toggle
- (R/W)

Continued on the next page...

**Register 51.14. MCPWM\_GEN $n$ \_B\_REG( $n$ : 0-2) (0x0054+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_GEN $n$ \_B\_DTO** Configures action on PWM $n$  B triggered by event\_t0 when timer decreasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**MCPWM\_GEN $n$ \_B\_DT1** Configures action on PWM $n$  B triggered by event\_t1 when timer decreasing.

0: No change

1: Low

2: High

3: Toggle

(R/W)

**Register 51.15. MCPWM\_DT $n$ \_CFG\_REG( $n$ : 0-2) (0x0058+0x38\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |       |    |   |   |   |   |  |   |   |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|-------|----|---|---|---|---|--|---|---|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_DB <sub>n</sub> _CLK_SEL<br>MCPWM_DB <sub>n</sub> _B_OUTBYPASS<br>MCPWM_DB <sub>n</sub> _A_OUTBYPASS<br>MCPWM_DB <sub>n</sub> _FED_OUTINVERT<br>MCPWM_DB <sub>n</sub> _RED_OUTINVERT<br>MCPWM_DB <sub>n</sub> _FED_INSEL<br>MCPWM_DB <sub>n</sub> _RED_INSEL<br>MCPWM_DB <sub>n</sub> _A_OUTSWAP<br>MCPWM_DB <sub>n</sub> _DEB_MODE<br>MCPWM_DB <sub>n</sub> _RED_UPMETHOD<br>MCPWM_DB <sub>n</sub> _FED_UPMETHOD |    |    |    |    |    |    |       |    |   |   |   |   |  |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 18  | 17 | 16 | 15 | 14 | 13 | 12 | 11    | 10 | 9 | 8 | 7 | 4 |  | 3 | 0 |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0  | 0  | 0  |    | 0  |    | Reset |    |   |   |   |   |  |   |   |  |

**MCPWM\_DBn\_FED\_UPMETHOD** Configures the update method for FED (Falling edge delay) active register.

0: Immediate

Bit0 is set to 1: TEZ

Bit1 is set to 1: TEP

Bit2 is set to 1: Sync

Bit3 is set to 1: Disable the update

(R/W)

**MCPWM\_DBn\_RED\_UPMETHOD** Configures the update method for RED (Rising edge delay) active register.

0: Immediate

Bit0 is set to 1: TEZ

Bit1 is set to 1: TEP

Bit2 is set to 1: Sync

Bit3 is set to 1: Disable the update

(R/W)

**MCPWM\_DB $\bar{n}$ \_DEB\_MODE** Configures the S8 switch in Table 51.3-5.

0: FED/RED take effect on different paths separately

1: FED/RED take effect on B path, A out is in bypass or dulpB mode

(R/W)

**MCPWM\_DBn\_A\_OUTSWAP** Configures the S6 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DBn\_B\_OUTSWAP** Configures the S7 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DBn\_RED\_INSEL** Configures the S4 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DBn\_FED\_INSEL** Configures the S5 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DBn\_RED\_OUTINVERT** Configures the S2 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

Continued on the next page...

**Register 51.15. MCPWM\_DT $n$ \_CFG\_REG( $n$ : 0-2) (0x0058+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_DB $n$ \_FED\_OUTINVERT** Configures the S3 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DB $n$ \_A\_OUTBYPASS** Configures the S1 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DB $n$ \_B\_OUTBYPASS** Configures the S0 switch in Table 51.3-5. For typical configurations, please refer to Table 51.3-6. (R/W)

**MCPWM\_DB $n$ \_CLK\_SEL** Configures dead time generator  $n$  clock selection.

0: PWM\_CLK

1: PT\_CLK

(R/W)

**Register 51.16. MCPWM\_DT $n$ \_FED\_CFG\_REG( $n$ : 0-2) (0x005C+0x38\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | MCPWM_DB <sub>n</sub> _FED |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**MCPWM\_DB $n$ \_FED** Configures the shadow register for FED. (R/W)

**Register 51.17. MCPWM\_DT $n$ \_RED\_CFG\_REG( $n$ : 0-2) (0x0060+0x38\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                            |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | MCPWM_DB <sub>n</sub> _RED |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                         |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                          |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

**MCPWM\_DB $n$ \_RED** Configures the shadow register for RED. (R/W)

**Register 51.18. MCPWM\_CARRIER $n$ \_CFG\_REG( $n$ : 0-2) (0x0064+0x38\* $n$ )**

|                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                       |   |  |    |                                     |  |                                  |  |                                      |   |                                |       |   |  |   |
|-----------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------|---|--|----|-------------------------------------|--|----------------------------------|--|--------------------------------------|---|--------------------------------|-------|---|--|---|
| (reserved)                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CHOPPER <sub>n</sub> _IN_INVERT |   | MCPWM_CHOPPER <sub>n</sub> _OUT_INVERT |    | MCPWM_CHOPPER <sub>n</sub> _OSHTWTH |  | MCPWM_CHOPPER <sub>n</sub> _DUTY |  | MCPWM_CHOPPER <sub>n</sub> _PRESCALE |   | MCPWM_CHOPPER <sub>n</sub> _EN |       |   |  |   |
| 31                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 14                                    |   | 13                                     | 12 | 11                                  |  | 8                                |  | 7                                    | 5 |                                | 4     | 1 |  | 0 |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                                     | 0 | 0                                      |    | 0                                   |  | 0                                |  | 0                                    |   | 0                              | Reset |   |  |   |

**MCPWM\_CHOPPER $n$ \_EN** Configures whether to enable carrier $n$ .

0: Bypassed

1: Enabled

(R/W)

**MCPWM\_CHOPPER $n$ \_PRESCALE** Configures the prescale value of PWM carrier $n$  clock (PC\_clk), so that period of PC\_clk = period of PWM\_clk \* (PWM\_CARRIER $n$ \_PRESCALE + 1). (R/W)

**MCPWM\_CHOPPER $n$ \_DUTY** Configures carrier duty. Duty = PWM\_CARRIER $n$ \_DUTY / 8. (R/W)

**MCPWM\_CHOPPER $n$ \_OSHTWTH** Configures width of the first pulse. Measurement unit: Periods of the carrier. (R/W)

**MCPWM\_CHOPPER $n$ \_OUT\_INVERT** Configures whether to invert the output of PWM $n$  A and PWM $n$  B for this submodule.

0: Normal

1: Invert

(R/W)

**MCPWM\_CHOPPER $n$ \_IN\_INVERT** Configures whether to invert the input of PWM $n$  A and PWM $n$  B for this submodule.

0: Normal

1: Invert

(R/W)

Register 51.19. MCPWM\_FH<sub>n</sub>\_CFG0\_REG(*n*: 0-2) (0x0068+0x38\**n*)

[illegible]

**MCPWM\_TZ<sub>n</sub>\_SW\_CBC** Configures whether to enable software force cycle-by-cycle mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZ<sub>n</sub>\_F2\_CBC** Configures whether event\_f2 will trigger cycle-by-cycle mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZn\_F1\_CBC** Configures whether event\_f1 will trigger cycle-by-cycle mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZ<sub>n</sub>\_FO\_CBC** Configures whether event\_f0 will trigger cycle-by-cycle mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZ<sub>n</sub>\_SW\_OST** Configures whether to enable software force one-shot mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZ<sub>n</sub>\_F2\_OST** Configures whether event\_f2 will trigger one-shot mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZ<sub>n</sub>\_F1\_OST** Configures whether event\_f1 will trigger one-shot mode action.

0: Disable

1: Enable

(R/W)

**MCPWM\_TZn\_Fn\_OST** Configures whether event\_f0 will trigger one-shot mode action.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 51.19. MCPWM\_FH $n$ \_CFG0\_REG( $n$ : 0-2) (0x0068+0x38\* $n$ )**

Continued from the previous page...

**MCPWM\_TZ $n$ \_A\_CBC\_D** Configures cycle-by-cycle mode action on PWM $n$  A when fault event occurs and timer is decreasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ $n$ \_A\_CBC\_U** Configures cycle-by-cycle mode action on PWM $n$  A when fault event occurs and timer is increasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ $n$ \_A\_OST\_D** Configures one-shot mode action on PWM $n$  A when fault event occurs and timer is decreasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ $n$ \_A\_OST\_U** Configures one-shot mode action on PWM $n$  A when fault event occurs and timer is increasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ $n$ \_B\_CBC\_D** Configures cycle-by-cycle mode action on PWM $n$  B when fault event occurs and timer is decreasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

Continued on the next page...



**Register 51.19. MCPWM\_FH<sub>n</sub>\_CFG0\_REG(*n*: 0-2) (0x0068+0x38\**n*)**

Continued from the previous page...

**MCPWM\_TZ<sub>n</sub>\_B\_CBC\_U** Configures cycle-by-cycle mode action on PWM<sub>n</sub> B when fault event occurs and timer is increasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ<sub>n</sub>\_B\_OST\_D** Configures one-shot mode action on PWM<sub>n</sub> B when fault event occurs and timer is decreasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

**MCPWM\_TZ<sub>n</sub>\_B\_OST\_U** Configures one-shot mode action on PWM<sub>n</sub> B when fault event occurs and timer is increasing.

- 0: Do nothing
  - 1: Force low
  - 2: Force high
  - 3: Toggle
- (R/W)

Register 51.20. MCPWM\_FH<sub>n</sub>\_CFG1\_REG(*n*: 0-2) (0x006C+0x38\**n*)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                  |   |   |   |                                  |   |   |   |                                 |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_TZ <sub>n</sub> _FORCE_OST |   |   |   | MCPWM_TZ <sub>n</sub> _FORCE_CBC |   |   |   | MCPWM_TZ <sub>n</sub> _CBCPULSE |   |   |   | MCPWM_TZ <sub>n</sub> _CLR_OST |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 5                                | 4 | 3 | 2 | 1                                | 0 |   |   |                                 |   |   |   |                                |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0                                | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**MCPWM\_TZ<sub>n</sub>\_CLR\_OST** Configures whether to generate a one-shot mode action clear by software.

0: No effect

1: Triggers a clear for ongoing one-shot mode action by software

(R/W)

**MCPWM\_TZ<sub>n</sub>\_CBCPULSE** Configures the refresh moment selection of cycle-by-cycle mode action.

0: Select nothing, will not refresh

Bit0 is set to 1: TEZ

Bit1 is set to 1: TEP

(R/W)

**MCPWM\_TZ<sub>n</sub>\_FORCE\_CBC** Configures whether to generate a software cycle-by-cycle mode action.

0: No effect

1: Triggers a cycle-by-cycle mode action by software

(R/W)

**MCPWM\_TZ<sub>n</sub>\_FORCE\_OST** Configures whether to generate a software one-shot mode action.

0: No effect

1: Triggers a one-shot mode action by software

(R/W)

Register 51.21. MCPWM\_FH<sub>*n*</sub>\_STATUS\_REG(*n*: 0-2) (0x0070+0x38\**n*)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                      |   |                                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_TZ <sub><i>n</i></sub> _OST_ON |   | MCPWM_TZ <sub><i>n</i></sub> _CBC_ON |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2                                    | 1 | 0                                    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                    | 0 | 0                                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**MCPWM\_TZ<sub>*n*</sub>\_CBC\_ON** Represents whether an cycle-by-cycle mode action is on going.

0: No action

1: Ongoing

(RO)

**MCPWM\_TZ<sub>*n*</sub>\_OST\_ON** Represents whether a one-shot mode action is ongoing.

0: No action

1: Ongoing

(RO)

Register 51.22. MCPWM\_FAULT\_DETECT\_REG (0x00E4)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_EVENT_F2<br>MCPWM_EVENT_F1<br>MCPWM_EVENT_F0<br>MCPWM_F2_POLE<br>MCPWM_F1_POLE<br>MCPWM_F0_POLE<br>MCPWM_F2_EN<br>MCPWM_F1_EN<br>MCPWM_F0_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

**MCPWM\_F<sub>*n*</sub>\_EN** Configures whether to enable event\_*fn* generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_F<sub>*n*</sub>\_POLE** Configures event\_*fn* trigger polarity on FAULT<sub>*n*</sub> source from GPIO matrix.

0: Level low

1: Level high

(R/W)

**MCPWM\_EVENT\_F<sub>*n*</sub>** Represents whether an event\_*fn* is ongoing. This field is set and reset by hardware.

0: No action

1: Ongoing

(RO)

Register 51.23. MCPWM\_CAP\_TIMER\_CFG\_REG (0x00E8)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                   |   |   |   |                     |   |       |   |                    |  |  |  |                    |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------|---|---|---|---------------------|---|-------|---|--------------------|--|--|--|--------------------|--|--|--|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | MCPWM_CAP_SYNC_SW |   |   |   | MCPWM_CAP_SYNC1_SEL |   |       |   | MCPWM_CAP_SYNC1_EN |  |  |  | MCPWM_CAP_TIMER_EN |  |  |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 6                 |   | 5 | 4 |                     | 2 |       | 1 | 0                  |  |  |  |                    |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                 | 0 |   |   | 0                   | 0 | Reset |   |                    |  |  |  |                    |  |  |  |

**MCPWM\_CAP\_TIMER\_EN** Configures whether to enable capture timer increment incrementing under APB\_CLK.

0: Disable

1: Enable

(R/W)

**MCPWM\_CAP\_SYNC1\_EN** Configures whether to enable capture timer sync.

0: Disable

1: Enable

(R/W)

**MCPWM\_CAP\_SYNC1\_SEL** Configures the selection of capture module sync input.

0: None

1: Timer0 sync\_out

2: Timer1 sync\_out

3: Timer2 sync\_out

4: SYNC0 from GPIO matrix

5: SYNC1 from GPIO matrix

6: SYNC2 from GPIO matrix

7: None

(R/W)

**MCPWM\_CAP\_SYNC\_SW** When [MCPWM\\_CAP\\_SYNC1\\_EN](#) is set to 1, configures whether to trigger a capture timer sync so that capture timer is loaded with value in phase register.

0: No effect

1: Trigger a capture timer sync

(WT)

### Register 51.24. MCPWM\_CAP\_TIMER\_PHASE\_REG (0x00EC)

Diagram illustrating the MCPWM\_CAP\_PHASE register structure. The register is 32 bits wide, with bit 31 on the left and bit 0 on the right. Bit 0 is labeled "Reset".

**MCPWM\_CAP\_PHASE** Configures phase value for capture timer sync operation.  
(R/W)

Register 51.25. MCPWM\_CAP\_CH $n$ \_CFG\_REG ( $n$ : 0-2) (0x00F0+0x4\* $n$ )

[illegible]

**MCPWM\_CAP $n$ \_EN** Configures whether to enable capture on channel  $n$ .

0: Disable

1: Enable

(R/W)

**MCPWM\_CAPn\_MODE** Configures the edge of capture on channel 0 after prescaling.  
When bit0 is set to 1: enable capture on the falling edge.  
When bit1 is set to 1: enable capture on the rising edge.  
(R/W)

**MCPWM\_CAPn\_PRESALE** Configures the prescale value on the rising edge of CAPO. Prescale value = PWM\_CAPO\_PRESALE + 1. (R/W)

**MCPWM\_CAP $n$ \_IN\_INVERT** Configures whether to invert CAP $n$  from GPIO matrix before prescale.  
 0: Normal  
 1: Invert  
 (R/W)

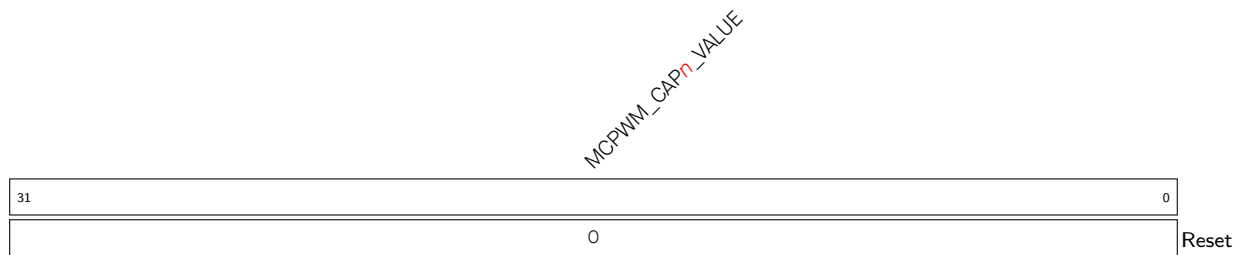
**MCPWM\_CAP<sub>n</sub>\_SW** Configures whether to trigger a software-forced capture on channel 0.

0: Not trigger

1: Trigger

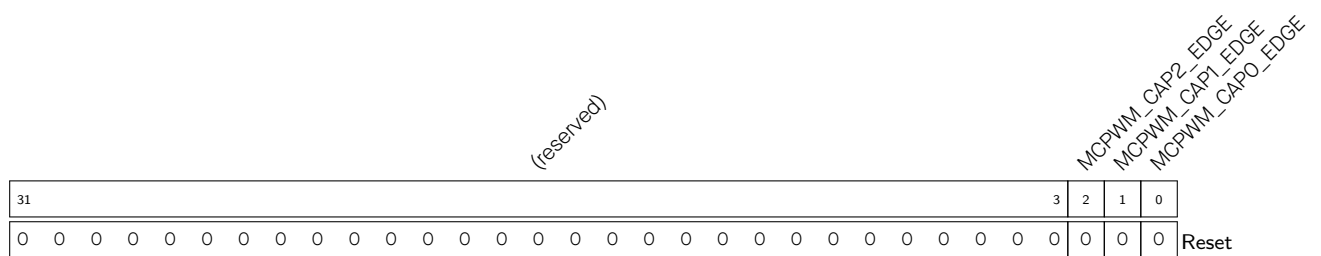
(WT)

Register 51.26. MCPWM\_CAP\_CH $n$ \_REG ( $n$ : 0-2) (0x00FC+0x4\* $n$ )



**MCPWM\_CAP $n$ \_VALUE** Represents value of last capture on CAP $n$ . (RO)

### Register 51.27. MCPWM\_CAP\_STATUS\_REG (0x0108)



**MCPWM\_CAP $n$ \_EDGE** Represents the edge of the last capture trigger on channel  $n$ .

0: Rising edge

1: Falling edge

(RO)



**Register 51.28. MCPWM\_UPDATE\_CFG\_REG (0x010C)**

Continued from the previous page...

**MCPWM\_OP1\_FORCE\_UP** Configures whether to trigger a forced update of active registers in PWM operator 1.

0: No effect

1: Trigger a forced update

(R/W)

**MCPWM\_OP2\_UP\_EN** Configures whether to update active registers in PWM operator 2 when [MCPWM\\_GLOBAL\\_UP\\_EN](#) is set to 1.

0: No effect

1: Update active registers in PWM operator 2

(R/W)

**MCPWM\_OP2\_FORCE\_UP** Configures whether to trigger a forced update of active registers in PWM operator 2.

0: No effect

1: Trigger a forced update

(R/W)



Register 51.29. MCPWM\_INT\_ENA\_REG (0x0110)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>MCPWM_CAP2_INT_ENA</div> <div>MCPWM_CAP1_INT_ENA</div> <div>MCPWM_CAP0_INT_ENA</div> <div>MCPWM_TZ2_INT_ENA</div> <div>MCPWM_TZ1_OST_INT_ENA</div> <div>MCPWM_TZ0_OST_INT_ENA</div> <div>MCPWM_TZ1_OST_INT_ENA</div> <div>MCPWM_TZ0_OST_INT_ENA</div> <div>MCPWM_TZ1_CBC_INT_ENA</div> <div>MCPWM_TZ0_CBC_INT_ENA</div> <div>MCPWM_CMPR2_INT_ENA</div> <div>MCPWM_CMPR1_TEB_INT_ENA</div> <div>MCPWM_CMPR0_TEB_INT_ENA</div> <div>MCPWM_CMPR2_TEA_INT_ENA</div> <div>MCPWM_CMPR1_TEA_INT_ENA</div> <div>MCPWM_FAULT2_CLR_INT_ENA</div> <div>MCPWM_FAULT1_CLR_INT_ENA</div> <div>MCPWM_FAULT0_CLR_INT_ENA</div> <div>MCPWM_FAULT2_INT_ENA</div> <div>MCPWM_FAULT1_INT_ENA</div> <div>MCPWM_FAULT0_INT_ENA</div> <div>MCPWM_TIMER2_TEP_INT_ENA</div> <div>MCPWM_TIMER1_TEP_INT_ENA</div> <div>MCPWM_TIMER0_TEP_INT_ENA</div> <div>MCPWM_TIMER2_TEZ_INT_ENA</div> <div>MCPWM_TIMER1_TEZ_INT_ENA</div> <div>MCPWM_TIMER0_TEZ_INT_ENA</div> <div>MCPWM_TIMER2_STOP_INT_ENA</div> <div>MCPWM_TIMER1_STOP_INT_ENA</div> <div>MCPWM_TIMER0_STOP_INT_ENA</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MCPWM\_TIMER0\_STOP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER0\\_STOP\\_INT](#). (R/W)

**MCPWM\_TIMER1\_STOP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER1\\_STOP\\_INT](#). (R/W)

**MCPWM\_TIMER2\_STOP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER2\\_STOP\\_INT](#). (R/W)

**MCPWM\_TIMER0\_TEZ\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER0\\_TEZ\\_INT](#). (R/W)

**MCPWM\_TIMER1\_TEZ\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER1\\_TEZ\\_INT](#). (R/W)

**MCPWM\_TIMER2\_TEZ\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER2\\_TEZ\\_INT](#). (R/W)

**MCPWM\_TIMER0\_TEP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER0\\_TEP\\_INT](#). (R/W)

**MCPWM\_TIMER1\_TEP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER1\\_TEP\\_INT](#). (R/W)

**MCPWM\_TIMER2\_TEP\_INT\_ENA** Write 1 to enable [MCPWM\\_TIMER2\\_TEP\\_INT](#). (R/W)

**MCPWM\_FAULT0\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT0\\_INT](#). (R/W)

**MCPWM\_FAULT1\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT1\\_INT](#). (R/W)

**MCPWM\_FAULT2\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT2\\_INT](#). (R/W)

**MCPWM\_FAULT0\_CLR\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT0\\_CLR\\_INT](#). (R/W)

**MCPWM\_FAULT1\_CLR\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT1\\_CLR\\_INT](#). (R/W)

**MCPWM\_FAULT2\_CLR\_INT\_ENA** Write 1 to enable [MCPWM\\_FAULT2\\_CLR\\_INT](#). (R/W)

**MCPWM\_CMPRO\_TEA\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPRO\\_TEA\\_INT](#). (R/W)

**MCPWM\_CMPR1\_TEA\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPR1\\_TEA\\_INT](#). (R/W)

**MCPWM\_CMPR2\_TEA\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPR2\\_TEA\\_INT](#). (R/W)

**MCPWM\_CMPRO\_TEB\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPRO\\_TEB\\_INT](#). (R/W)

**MCPWM\_CMPR1\_TEB\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPR1\\_TEB\\_INT](#). (R/W)

**MCPWM\_CMPR2\_TEB\_INT\_ENA** Write 1 to enable [MCPWM\\_CMPR2\\_TEB\\_INT](#). (R/W)

**MCPWM\_TZO\_CBC\_INT\_ENA** Write 1 to enable [MCPWM\\_TZO\\_CBC\\_INT](#). (R/W)

Continued on the next page...

**Register 51.29. MCPWM\_INT\_ENA\_REG (0x0110)**

Continued from the previous page...

**MCPWM\_TZ1\_CBC\_INT\_ENA** Write 1 to enable [MCPWM\\_TZ1\\_CBC\\_INT](#). (R/W)

**MCPWM\_TZ2\_CBC\_INT\_ENA** Write 1 to enable [MCPWM\\_TZ2\\_CBC\\_INT](#). (R/W)

**MCPWM\_TZ0\_OST\_INT\_ENA** Write 1 to enable [MCPWM\\_TZ0\\_OST\\_INT](#). (R/W)

**MCPWM\_TZ1\_OST\_INT\_ENA** Write 1 to enable [MCPWM\\_TZ1\\_OST\\_INT](#). (R/W)

**MCPWM\_TZ2\_OST\_INT\_ENA** Write 1 to enable [MCPWM\\_TZ2\\_OST\\_INT](#). (R/W)

**MCPWM\_CAPO\_INT\_ENA** Write 1 to enable [MCPWM\\_CAPO\\_INT](#). (R/W)

**MCPWM\_CAP1\_INT\_ENA** Write 1 to enable [MCPWM\\_CAP1\\_INT](#). (R/W)

**MCPWM\_CAP2\_INT\_ENA** Write 1 to enable [MCPWM\\_CAP2\\_INT](#). (R/W)

## Register 51.30. MCPWM\_INT\_RAW\_REG (0x0114)

| <div>(reserved)</div> <div>MCPWM_CAP2_INT_RAW</div> <div>MCPWM_CAP1_INT_RAW</div> <div>MCPWM_CAPO_INT_RAW</div> <div>MCPWM_TZ2_OST_INT_RAW</div> <div>MCPWM_TZ1_OST_INT_RAW</div> <div>MCPWM_TZ0_OST_INT_RAW</div> <div>MCPWM_TZ2_CBC_INT_RAW</div> <div>MCPWM_TZ1_CBC_INT_RAW</div> <div>MCPWM_TZ0_CBC_INT_RAW</div> <div>MCPWM_CMPR2_INT_RAW</div> <div>MCPWM_CMPR1_TEB_INT_RAW</div> <div>MCPWM_CMPR0_TEB_INT_RAW</div> <div>MCPWM_CMPR2_TEA_INT_RAW</div> <div>MCPWM_CMPR1_TEA_INT_RAW</div> <div>MCPWM_FAULT2_CLR_INT_RAW</div> <div>MCPWM_FAULT1_CLR_INT_RAW</div> <div>MCPWM_FAULT0_CLR_INT_RAW</div> <div>MCPWM_TIMER2_TEP_INT_RAW</div> <div>MCPWM_TIMER1_TEP_INT_RAW</div> <div>MCPWM_TIMER0_TEP_INT_RAW</div> <div>MCPWM_TIMER2_TEZ_INT_RAW</div> <div>MCPWM_TIMER1_TEZ_INT_RAW</div> <div>MCPWM_TIMER0_TEZ_INT_RAW</div> <div>MCPWM_TIMER2_STOP_INT_RAW</div> <div>MCPWM_TIMER1_STOP_INT_RAW</div> <div>MCPWM_TIMER0_STOP_INT_RAW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MCPWM\_TIMER0\_STOP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER0\\_STOP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER1\_STOP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER1\\_STOP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER2\_STOP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER2\\_STOP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER0\_TEZ\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER0\\_TEZ\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER1\_TEZ\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER1\\_TEZ\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER2\_TEZ\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER2\\_TEZ\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER0\_TEP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER0\\_TEP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER1\_TEP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER1\\_TEP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TIMER2\_TEP\_INT\_RAW** Represents the raw status of [MCPWM\\_TIMER2\\_TEP\\_INT](#).  
(R/WTC/SS)

**MCPWM\_FAULT0\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT0\\_INT](#). (R/WTC/SS)

**MCPWM\_FAULT1\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT1\\_INT](#). (R/WTC/SS)

**MCPWM\_FAULT2\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT2\\_INT](#). (R/WTC/SS)

**MCPWM\_FAULT0\_CLR\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT0\\_CLR\\_INT](#).  
(R/WTC/SS)

**MCPWM\_FAULT1\_CLR\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT1\\_CLR\\_INT](#).  
(R/WTC/SS)

Continued on the next page...

**Register 51.30. MCPWM\_INT\_RAW\_REG (0x0114)**

Continued from the previous page...

**MCPWM\_FAULT2\_CLR\_INT\_RAW** Represents the raw status of [MCPWM\\_FAULT2\\_CLR\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPRO\_TEA\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPRO\\_TEA\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPR1\_TEA\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPR1\\_TEA\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPR2\_TEA\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPR2\\_TEA\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPRO\_TEB\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPRO\\_TEB\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPR1\_TEB\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPR1\\_TEB\\_INT](#).  
(R/WTC/SS)

**MCPWM\_CMPR2\_TEB\_INT\_RAW** Represents the raw status of [MCPWM\\_CMPR2\\_TEB\\_INT](#).  
(R/WTC/SS)

**MCPWM\_TZO\_CBC\_INT\_RAW** Represents the raw status of [MCPWM\\_TZO\\_CBC\\_INT](#). (R/WTC/SS)

**MCPWM\_TZ1\_CBC\_INT\_RAW** Represents the raw status of [MCPWM\\_TZ1\\_CBC\\_INT](#). (R/WTC/SS)

**MCPWM\_TZ2\_CBC\_INT\_RAW** Represents the raw status of [MCPWM\\_TZ2\\_CBC\\_INT](#). (R/WTC/SS)

**MCPWM\_TZO\_OST\_INT\_RAW** Represents the raw status of [MCPWM\\_TZO\\_OST\\_INT](#). (R/WTC/SS)

**MCPWM\_TZ1\_OST\_INT\_RAW** Represents the raw status of [MCPWM\\_TZ1\\_OST\\_INT](#). (R/WTC/SS)

**MCPWM\_TZ2\_OST\_INT\_RAW** Represents the raw status of [MCPWM\\_TZ2\\_OST\\_INT](#). (R/WTC/SS)

**MCPWM\_CAPO\_INT\_RAW** Represents the raw status of [MCPWM\\_CAPO\\_INT](#). (R/WTC/SS)

**MCPWM\_CAP1\_INT\_RAW** Represents the raw status of [MCPWM\\_CAP1\\_INT](#). (R/WTC/SS)

**MCPWM\_CAP2\_INT\_RAW** Represents the raw status of [MCPWM\\_CAP2\\_INT](#). (R/WTC/SS)

**Register 51.31. MCPWM\_INT\_ST\_REG (0x0118)**

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>MCPWM_CAP2_INT_ST</div> <div>MCPWM_CAP1_INT_ST</div> <div>MCPWM_CAO_INT_ST</div> <div>MCPWM_TZ2_OST_INT_ST</div> <div>MCPWM_TZ1_OST_INT_ST</div> <div>MCPWM_TZO_OST_INT_ST</div> <div>MCPWM_TZ2_CBC_INT_ST</div> <div>MCPWM_TZ1_CBC_INT_ST</div> <div>MCPWM_TZO_CBC_INT_ST</div> <div>MCPWM_CMPR2_TEB_INT_ST</div> <div>MCPWM_CMPR1_TEB_INT_ST</div> <div>MCPWM_CMPR2_TEA_INT_ST</div> <div>MCPWM_CMPR1_TEA_INT_ST</div> <div>MCPWM_FAULT2_CLR_INT_ST</div> <div>MCPWM_FAULT1_CLR_INT_ST</div> <div>MCPWM_FAULT2_INT_ST</div> <div>MCPWM_FAULT1_INT_ST</div> <div>MCPWM_TIMER2_TEP_INT_ST</div> <div>MCPWM_TIMER1_TEP_INT_ST</div> <div>MCPWM_TIMER2_TEZ_INT_ST</div> <div>MCPWM_TIMER1_TEZ_INT_ST</div> <div>MCPWM_TIMER2_STOP_INT_ST</div> <div>MCPWM_TIMER1_STOP_INT_ST</div> <div>MCPWM_TIMER2_STOP_INT_ST</div> <div>MCPWM_TIMER1_STOP_INT_ST</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

Reset

**MCPWM\_TIMER0\_STOP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER0\\_STOP\\_INT](#). (RO)

**MCPWM\_TIMER1\_STOP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER1\\_STOP\\_INT](#). (RO)

**MCPWM\_TIMER2\_STOP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER2\\_STOP\\_INT](#). (RO)

**MCPWM\_TIMER0\_TEZ\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER0\\_TEZ\\_INT](#). (RO)

**MCPWM\_TIMER1\_TEZ\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER1\\_TEZ\\_INT](#). (RO)

**MCPWM\_TIMER2\_TEZ\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER2\\_TEZ\\_INT](#). (RO)

**MCPWM\_TIMER0\_TEP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER0\\_TEP\\_INT](#). (RO)

**MCPWM\_TIMER1\_TEP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER1\\_TEP\\_INT](#). (RO)

**MCPWM\_TIMER2\_TEP\_INT\_ST** Represents the masked status of [MCPWM\\_TIMER2\\_TEP\\_INT](#). (RO)

**MCPWM\_FAULT0\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT0\\_INT](#). (RO)

**MCPWM\_FAULT1\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT1\\_INT](#). (RO)

**MCPWM\_FAULT2\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT2\\_INT](#). (RO)

**MCPWM\_FAULT0\_CLR\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT0\\_CLR\\_INT](#). (RO)

**MCPWM\_FAULT1\_CLR\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT1\\_CLR\\_INT](#). (RO)

Continued on the next page...

**Register 51.31. MCPWM\_INT\_ST\_REG (0x0118)**

Continued from the previous page...

**MCPWM\_FAULT2\_CLR\_INT\_ST** Represents the masked status of [MCPWM\\_FAULT2\\_CLR\\_INT](#). (RO)

**MCPWM\_CMPRO\_TEA\_INT\_ST** Represents the masked status of [MCPWM\\_CMPRO\\_TEA\\_INT](#). (RO)

**MCPWM\_CMPR1\_TEA\_INT\_ST** Represents the masked status of [MCPWM\\_CMPR1\\_TEA\\_INT](#). (RO)

**MCPWM\_CMPR2\_TEA\_INT\_ST** Represents the masked status of [MCPWM\\_CMPR2\\_TEA\\_INT](#). (RO)

**MCPWM\_CMPRO\_TEB\_INT\_ST** Represents the masked status of [MCPWM\\_CMPRO\\_TEB\\_INT](#). (RO)

**MCPWM\_CMPR1\_TEB\_INT\_ST** Represents the masked status of [MCPWM\\_CMPR1\\_TEB\\_INT](#). (RO)

**MCPWM\_CMPR2\_TEB\_INT\_ST** Represents the masked status of [MCPWM\\_CMPR2\\_TEB\\_INT](#). (RO)

**MCPWM\_TZO\_CBC\_INT\_ST** Represents the masked status of [MCPWM\\_TZO\\_CBC\\_INT\\_ST](#). (RO)

**MCPWM\_TZ1\_CBC\_INT\_ST** Represents the masked status of [MCPWM\\_TZ1\\_CBC\\_INT\\_ST](#). (RO)

**MCPWM\_TZ2\_CBC\_INT\_ST** Represents the masked status of [MCPWM\\_TZ2\\_CBC\\_INT\\_ST](#). (RO)

**MCPWM\_TZO\_OST\_INT\_ST** Represents the masked status of [MCPWM\\_TZO\\_OST\\_INT](#). (RO)

**MCPWM\_TZ1\_OST\_INT\_ST** Represents the masked status of [MCPWM\\_TZ1\\_OST\\_INT](#). (RO)

**MCPWM\_TZ2\_OST\_INT\_ST** Represents the masked status of [MCPWM\\_TZ2\\_OST\\_INT](#). (RO)

**MCPWM\_CAPO\_INT\_ST** Represents the masked status of [MCPWM\\_CAPO\\_INT](#). (RO)

**MCPWM\_CAP1\_INT\_ST** Represents the masked status of [MCPWM\\_CAP1\\_INT](#). (RO)

**MCPWM\_CAP2\_INT\_ST** Represents the masked status of [MCPWM\\_CAP2\\_INT](#). (RO)

Register 51.32. MCPWM\_INT\_CLR\_REG (0x011C)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>MCPWM_CAP2_INT_CLR</div> <div>MCPWM_CAP1_INT_CLR</div> <div>MCPWM_CAPO_INT_CLR</div> <div>MCPWM_TZ2_OST_INT_CLR</div> <div>MCPWM_TZ1_OST_INT_CLR</div> <div>MCPWM_TZO_OST_INT_CLR</div> <div>MCPWM_TZ2_CBC_INT_CLR</div> <div>MCPWM_TZ1_CBC_INT_CLR</div> <div>MCPWM_TZO_CBC_INT_CLR</div> <div>MCPWM_CMPR2_TEB_INT_CLR</div> <div>MCPWM_CMPR1_TEB_INT_CLR</div> <div>MCPWM_CMPRO_TEB_INT_CLR</div> <div>MCPWM_CMPR2_TEA_INT_CLR</div> <div>MCPWM_CMPR1_TEA_INT_CLR</div> <div>MCPWM_CMPRO_TEA_INT_CLR</div> <div>MCPWM_FAULT2_CLR_INT_CLR</div> <div>MCPWM_FAULT1_CLR_INT_CLR</div> <div>MCPWM_FAULT0_CLR_INT_CLR</div> <div>MCPWM_TIMER2_TEP_INT_CLR</div> <div>MCPWM_TIMER1_TEP_INT_CLR</div> <div>MCPWM_TIMER0_TEP_INT_CLR</div> <div>MCPWM_TIMER2_TEZ_INT_CLR</div> <div>MCPWM_TIMER1_TEZ_INT_CLR</div> <div>MCPWM_TIMER0_TEZ_INT_CLR</div> <div>MCPWM_TIMER2_STOP_INT_CLR</div> <div>MCPWM_TIMER1_STOP_INT_CLR</div> <div>MCPWM_TIMER0_STOP_INT_CLR</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MCPWM\_TIMER0\_STOP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER0\\_STOP\\_INT](#). (WT)

**MCPWM\_TIMER1\_STOP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER1\\_STOP\\_INT](#). (WT)

**MCPWM\_TIMER2\_STOP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER2\\_STOP\\_INT](#). (WT)

**MCPWM\_TIMER0\_TEZ\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER0\\_TEZ\\_INT](#). (WT)

**MCPWM\_TIMER1\_TEZ\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER1\\_TEZ\\_INT](#). (WT)

**MCPWM\_TIMER2\_TEZ\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER2\\_TEZ\\_INT](#). (WT)

**MCPWM\_TIMER0\_TEP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER0\\_TEP\\_INT](#). (WT)

**MCPWM\_TIMER1\_TEP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER1\\_TEP\\_INT](#). (WT)

**MCPWM\_TIMER2\_TEP\_INT\_CLR** Write 1 to clear [MCPWM\\_TIMER2\\_TEP\\_INT](#). (WT)

**MCPWM\_FAULT0\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT0\\_INT](#). (WT)

**MCPWM\_FAULT1\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT1\\_INT](#). (WT)

**MCPWM\_FAULT2\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT2\\_INT](#). (WT)

**MCPWM\_FAULT0\_CLR\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT0\\_CLR\\_INT](#). (WT)

**MCPWM\_FAULT1\_CLR\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT1\\_CLR\\_INT](#). (WT)

**MCPWM\_FAULT2\_CLR\_INT\_CLR** Write 1 to clear [MCPWM\\_FAULT2\\_CLR\\_INT](#). (WT)

**MCPWM\_CMPRO\_TEA\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPRO\\_TEA\\_INT](#). (WT)

**MCPWM\_CMPR1\_TEA\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPR1\\_TEA\\_INT](#). (WT)

**MCPWM\_CMPR2\_TEA\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPR2\\_TEA\\_INT](#). (WT)

**MCPWM\_CMPRO\_TEB\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPRO\\_TEB\\_INT](#). (WT)

**MCPWM\_CMPR1\_TEB\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPR1\\_TEB\\_INT](#). (WT)

**MCPWM\_CMPR2\_TEB\_INT\_CLR** Write 1 to clear [MCPWM\\_CMPR2\\_TEB\\_INT](#). (WT)

**MCPWM\_TZO\_CBC\_INT\_CLR** Write 1 to clear [MCPWM\\_TZO\\_CBC\\_INT](#). (WT)

Continued on the next page...

**Register 51.32. MCPWM\_INT\_CLR\_REG (0x011C)**

Continued from the previous page...

**MCPWM\_TZ1\_CBC\_INT\_CLR** Write 1 to clear [MCPWM\\_TZ1\\_CBC\\_INT](#). (WT)

**MCPWM\_TZ2\_CBC\_INT\_CLR** Write 1 to clear [MCPWM\\_TZ2\\_CBC\\_INT](#). (WT)

**MCPWM\_TZ0\_OST\_INT\_CLR** Write 1 to clear [MCPWM\\_TZ0\\_OST\\_INT](#). (WT)

**MCPWM\_TZ1\_OST\_INT\_CLR** Write 1 to clear [MCPWM\\_TZ1\\_OST\\_INT](#). (WT)

**MCPWM\_TZ2\_OST\_INT\_CLR** Write 1 to clear [MCPWM\\_TZ2\\_OST\\_INT](#). (WT)

**MCPWM\_CAPO\_INT\_CLR** Write 1 to clear [MCPWM\\_CAPO\\_INT](#). (WT)

**MCPWM\_CAP1\_INT\_CLR** Write 1 to clear [MCPWM\\_CAP1\\_INT](#). (WT)

**MCPWM\_CAP2\_INT\_CLR** Write 1 to clear [MCPWM\\_CAP2\\_INT](#). (WT)



### Register 51.33. MCPWM\_EVT\_EN\_REG (0x0120)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>MCPWM_EVT_CAP2_EN</div> <div>MCPWM_EVT_CAP1_EN</div> <div>MCPWM_EVT_CAP0_EN</div> <div>MCPWM_EVT_TZ2_EN</div> <div>MCPWM_EVT_TZ1_EN</div> <div>MCPWM_EVT_TZ0_EN</div> <div>MCPWM_EVT_TZ2_OST_EN</div> <div>MCPWM_EVT_TZ1_OST_EN</div> <div>MCPWM_EVT_TZ0_OST_EN</div> <div>MCPWM_EVT_TZ2_OBC_EN</div> <div>MCPWM_EVT_TZ1_OBC_EN</div> <div>MCPWM_EVT_TZ0_OBC_EN</div> <div>MCPWM_EVT_F2_CLR_EN</div> <div>MCPWM_EVT_F1_CLR_EN</div> <div>MCPWM_EVT_F0_CLR_EN</div> <div>MCPWM_EVT_F2_EN</div> <div>MCPWM_EVT_F1_EN</div> <div>MCPWM_EVT_F0_EN</div> <div>MCPWM_EVT_OP2_TEB_EN</div> <div>MCPWM_EVT_OP1_TEB_EN</div> <div>MCPWM_EVT_OP0_TEB_EN</div> <div>MCPWM_EVT_OP2_TEA_EN</div> <div>MCPWM_EVT_OP1_TEA_EN</div> <div>MCPWM_EVT_OP0_TEA_EN</div> <div>MCPWM_EVT_TIMER2_TEP_EN</div> <div>MCPWM_EVT_TIMER1_TEP_EN</div> <div>MCPWM_EVT_TIMER0_TEP_EN</div> <div>MCPWM_EVT_TIMER2_TEZ_EN</div> <div>MCPWM_EVT_TIMER1_TEZ_EN</div> <div>MCPWM_EVT_TIMER0_TEZ_EN</div> <div>MCPWM_EVT_TIMER2_STOP_EN</div> <div>MCPWM_EVT_TIMER1_STOP_EN</div> <div>MCPWM_EVT_TIMER0_STOP_EN</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**MCPWM\_EVT\_TIMER0\_STOP\_EN** Configures whether to enable timer0 stop event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER1\_STOP\_EN** Configures whether to enable timer1 stop event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER2\_STOP\_EN** Configures whether to enable timer2 stop event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER0\_TEZ\_EN** Configures whether to enable timer0 equal zero event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER1\_TEZ\_EN** Configures whether to enable timer1 equal zero event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER2\_TEZ\_EN** Configures whether to enable timer2 equal zero event generation.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 51.33. MCPWM\_EVT\_EN\_REG (0x0120)**

Continued from the previous page...

**MCPWM\_EVT\_TIMER0\_TEP\_EN** Configures whether to enable timer0 equal period event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER1\_TEP\_EN** Configures whether to enable timer1 equal period event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TIMER2\_TEP\_EN** Configures whether to enable timer2 equal period event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_OPO\_TEA\_EN** Configures whether to enable PWM generator0 timer equal A event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_OP1\_TEA\_EN** Configures whether to enable PWM generator1 timer equal A event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_OP2\_TEA\_EN** Configures whether to enable PWM generator2 timer equal A event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_OPO\_TEB\_EN** Configures whether to enable PWM generator0 timer equal B event generation.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 51.33. MCPWM\_EVT\_EN\_REG (0x0120)**

Continued from the previous page...

**MCPWM\_EVT\_OP1\_TEB\_EN** Configures whether to enable PWM generator1 timer equal B event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_OP2\_TEB\_EN** Configures whether to enable PWM generator2 timer equal B event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F0\_EN** Configures whether to enable FAULT0 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F1\_EN** Configures whether to enable FAULT1 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F2\_EN** Configures whether to enable FAULT2 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F0\_CLR\_EN** Configures whether to enable FAULT0 clear event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F1\_CLR\_EN** Configures whether to enable FAULT1 clear event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_F2\_CLR\_EN** Configures whether to enable FAULT2 clear event generation.

0: Disable

1: Enable

(R/W)

Continued on the next page...

**Register 51.33. MCPWM\_EVT\_EN\_REG (0x0120)**

Continued from the previous page...

**MCPWM\_EVT\_TZ0\_CBC\_EN** Configures whether to enable cycle by cycle trip0 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TZ1\_CBC\_EN** Configures whether to enable cycle by cycle trip1 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TZ2\_CBC\_EN** Configures whether to enable cycle by cycle trip2 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TZ0\_OST\_EN** Configures whether to enable one shot trip0 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TZ1\_OST\_EN** Configures whether to enable one shot trip1 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_TZ2\_OST\_EN** Configures whether to enable one shot trip2 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_CAPO\_EN** Configures whether to enable capture0 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_CAP1\_EN** Configures whether to enable capture1 event generation.

0: Disable

1: Enable

(R/W)

**MCPWM\_EVT\_CAP2\_EN** Configures whether to enable capture2 event generation.

0: Disable

1: Enable

(R/W)

### Register 51.34. MCPWM\_EVT\_EN2\_REG (0x0128)

Register 0x00000000: MCPWM\_TEE1\_EN

Bit 31: (reserved)

Bit 6: MCPWM\_TEE1\_EN

Bit 5: MCPWM\_EVT\_OPO\_TEE1\_EN

Bit 4: MCPWM\_EVT\_OP1\_TEE1\_EN

Bit 3: MCPWM\_EVT\_OPO\_TEE2\_EN

Bit 2: MCPWM\_EVT\_OP1\_TEE2\_EN

Bit 1: MCPWM\_EVT\_OPO\_TEE1\_EN

Bit 0: MCPWM\_EVT\_OP1\_TEE1\_EN

**MCPWM\_EVT\_OP $n$ \_TEE1\_EN** Configures whether to generate the MCPWM\_EVT\_OP $n$ \_TEE1 event when the PWM generator $n$  timer equals OP $n$ \_TSTMP\_E1\_REG.

0: Not generate

## 1: Generate

(R/W)

**MCPWM\_EVT\_OPn\_TEE2\_EN** Configures whether to generate the MCPWM\_EVT\_OPn\_TEE2 event when the PWM generatorn timer equals OPn\_TSTMP\_E2\_REG.

0: Not generate

1: Generate

(R/W)

### Register 51.35. MCPWM\_TASK\_EN\_REG (0x0124)

[illegible]

**MCPWM\_TASK\_CMPRO\_A\_UP\_EN** Configures whether to receive update task of PWM generator0 timer stamp A's shadow register.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CMPR1\_A\_UP\_EN** Configures whether to receive update task of PWM generator1 timer stamp A's shadow register.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CMPR2\_A\_UP\_EN** Configures whether to receive update task of PWM generator2 timer stamp A's shadow register.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CMPRO\_B\_UP\_EN** Configures whether to receive update task of PWM generator0 timer stamp B's shadow register.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CMPR1\_B\_UP\_EN** Configures whether to receive update task of PWM generator1 timer stamp B's shadow register.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CMPR2\_B\_UP\_EN** Configures whether to receive update task of PWM generator2 timer stamp B's shadow register.

0: No effect

1: Receive

(R/W)

Continued on the next page...

**Register 51.35. MCPWM\_TASK\_EN\_REG (0x0124)**

Continued from the previous page...

**MCPWM\_TASK\_GEN\_STOP\_EN** Configures whether to receive all PWM generate stop task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER0\_SYNC\_EN** Configures whether to receive timer0 sync task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER1\_SYNC\_EN** Configures whether to receive timer1 sync task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER2\_SYNC\_EN** Configures whether to receive timer2 sync task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER0\_PERIOD\_UP\_EN** Configures whether to receive timer0 period update task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER1\_PERIOD\_UP\_EN** Configures whether to receive timer1 period update task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TIMER2\_PERIOD\_UP\_EN** Configures whether to receive timer2 period update task.

0: No effect

1: Receive

(R/W)

Continued on the next page...

**Register 51.35. MCPWM\_TASK\_EN\_REG (0x0124)**

Continued from the previous page...

**MCPWM\_TASK\_TZ0\_OST\_EN** Configures whether to receive one shot trip0 task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TZ1\_OST\_EN** Configures whether to receive one shot trip1 task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_TZ2\_OST\_EN** Configures whether to receive one shot trip2 task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CLRO\_OST\_EN** Configures whether to receive one shot trip0 clear task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CLR1\_OST\_EN** Configures whether to receive one shot trip1 clear task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CLR2\_OST\_EN** Configures whether to receive one shot trip2 clear task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CAPO\_EN** Configures whether to receive capture0 task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CAP1\_EN** Configures whether to receive capture1 task.

0: No effect

1: Receive

(R/W)

**MCPWM\_TASK\_CAP2\_EN** Configures whether to receive capture2 task.

0: No effect

1: Receive

(R/W)



**Register 51.36. MCPWM\_OP $n$ \_TSTMP\_E1\_REG ( $n$ : 0-2) (0x012C+0x8\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |    |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | MCPWM_OP <sub>n</sub> _TSTMP_E1 |    |  |  |  |  |  |  |  |  |  |  |  |  |       |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16                              | 15 |  |  |  |  |  |  |  |  |  |  |  |  |       |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               |    |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |   |

**MCPWM\_OP $n$ \_TSTMP\_E1** Configures the time stamp E1 value of the generator $n$ . (R/W)

**Register 51.37. MCPWM\_OP $n$ \_TSTMP\_E2\_REG( $n$ : 0-2) (0x0130+0x8\* $n$ )**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | MCPWM_OP <sub>n</sub> _TSTMP_E2 |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                              |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                               |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

**MCPWM\_OP $n$ \_TSTMP\_E2** Configures the time stamp E2 value of the generator $n$ . (R/W)

**Register 51.38. MCPWM\_CLK\_REG (0x0144)**

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1 | 0            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**MCPWM\_CLK\_EN** Configures whether to force open register clock gate.

0: Open the clock gate only when application writes registers

1: Force open the clock gate for register

(R/W)

Register 51.39. MCPWM\_VERSION\_REG (0x0148)

|            |    |    |   |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|----|----|---|------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |    |    |   | MCPWM_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         | 28 | 27 | 0 |            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 0          | 0  | 0  | 0 | 0x2212290  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

MCPWM\_DATE Version control register. (R/W)

## Chapter 52

# Remote Control Peripheral (RMT)

## 52.1 Overview

The Remote Control (RMT) module is designed to transmit and receive infrared remote control signals. A variety of remote control protocols can be encoded/decoded via software based on the RMT module. The RMT module converts pulse codes stored in the module's built-in RAM into output signals, or converts input signals into pulse codes and stores them in RAM. In addition, the RMT module optionally modulates its output signals with a carrier wave, or optionally demodulates and filters its input signals.

The RMT module has eight channels, numbered from zero to seven. Each channel is able to independently transmit or receive signals.

- Channel 0 ~ 3 (TX channel) are dedicated to transmitting signals;
- Channel 4 ~ 7 (RX channel) are dedicated to receiving signals.

Each TX/RX channel has the same functionality controlled by a dedicated set of registers and is able to independently transmit or receive data. Channel 3 and channel 7 support GDMA access, so the two channels also have a set of GDMA-related control and status registers. TX channels are indicated by *n* which is used as a placeholder for the channel number, and by *m* for RX channels.

## 52.2 Features

The RMT module has the following features:

- Eight channels:
  - TX channels 0 ~ 3
  - RX channels 4 ~ 7
  - Eight channels share a 384 x 32-bit RAM
- The transmitter supports:
  - Normal TX mode
  - Wrap TX mode
  - Continuous TX mode
  - Modulation on TX pulses
  - Multiple channels transmitting data simultaneously (programmable)
  - GDMA access supported by TX channel 3

- The receiver supports:
  - Normal RX mode
  - Wrap RX mode
  - RX filtering
  - Demodulation on RX pulses
  - GDMA access supported by RX channel 7

## 52.3 Functional Description

### 52.3.1 Architecture

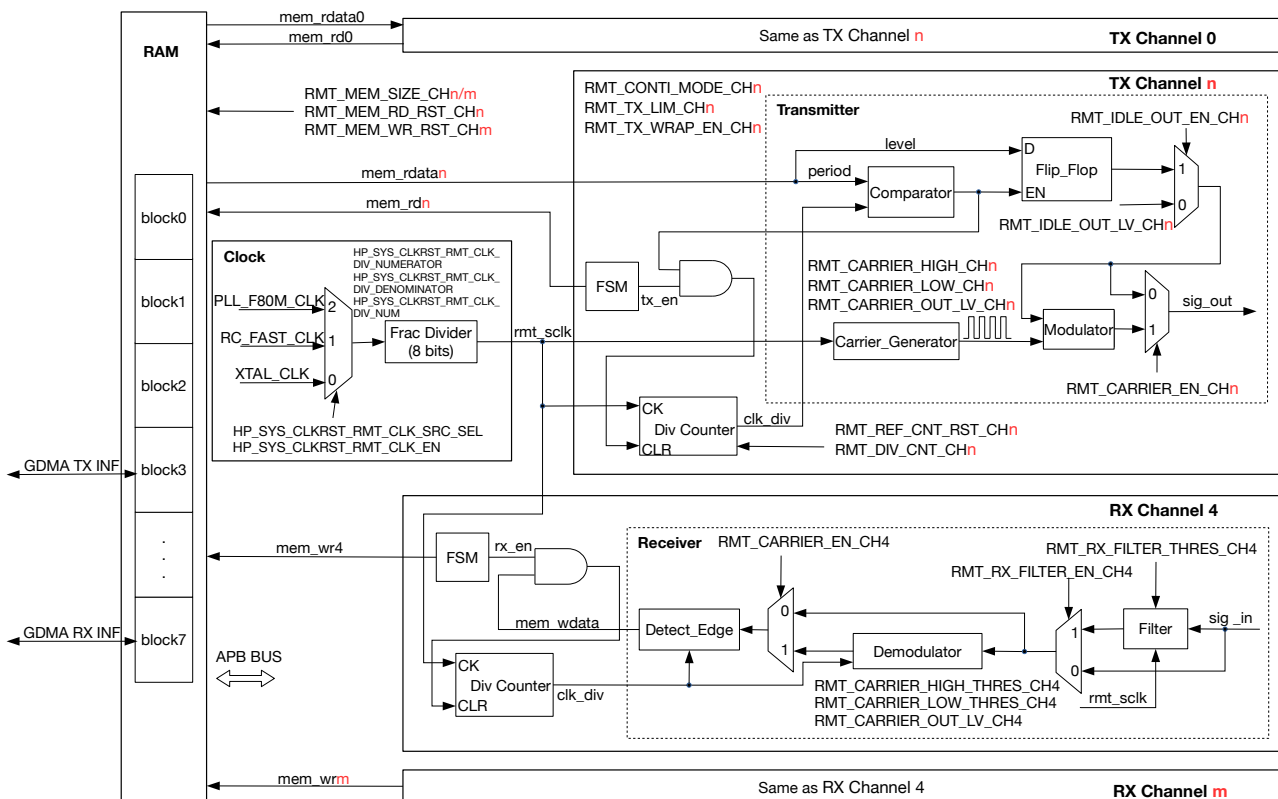


Figure 52.3-1. RMT Architecture

As shown in Figure 52.3-1, each TX channel has:

- 1 x clock divider counter (Div Counter)
- 1 x state machine (FSM)
- 1 x transmitter

Each RX channel has:

- 1 x clock divider counter (Div Counter)

- 1 x state machine (FSM)
- 1 x receiver

The eight channels share a 384 x 32-bit RAM.

## 52.3.2 RAM

### 52.3.2.1 Structure of RAM

Figure 52.3-2 shows the format of pulse code in RAM. Each pulse code contains a 16-bit entry with two fields: “level” and “period”. “level” (0 or 1) indicates a low-/high-level value that has been received or is going to be sent, while “period” points out the number of clock cycles (see `clk_div` in Figure 52.3-1) that the level lasts for.

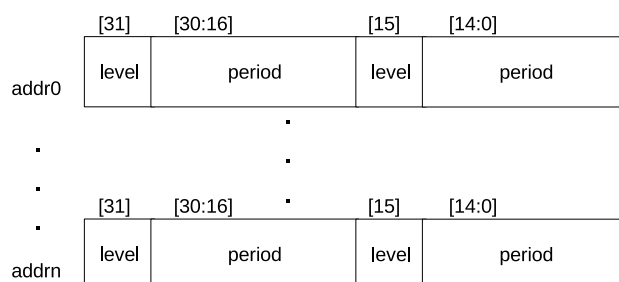


Figure 52.3-2. Format of Pulse Code in RAM

The minimum value for the period is zero (0) and is interpreted as a transmission end-marker. For a non-zero period (i.e., not an end-marker), its value is limited by APB clock and RMT clock according to the formula below:

$$3 \times T_{apb\_clk} + 5 \times T_{rmt\_sclk} < period \times T_{clk\_div} \quad (1)$$

**Note:**

According to the formula above and the frequency of `rmt_sclk`, the pulse width (i.e.,  $period \times T_{clk\_div}$ ) able to be captured by RMT is limited as follows:

- The minimum value of pulse width should be larger than  $(3 \times T_{apb\_clk} + 5 \times T_{rmt\_sclk})$ .
- The maximum value of pulse width should be smaller than or equal to (the maximum period  $\times$  the maximum  $T_{clk\_div}$ ), i.e.,  $((2^{15} - 1) \times \text{the maximum } T_{rmt\_sclk} \times 256)$ .

For more information about the `rmt_sclk` frequency, or APB\_CLK frequency, see Section 52.3.3, or Chapter 9 [Reset and Clock](#).

### 52.3.2.2 Use of RAM

The RAM is divided into eight 48 x 32-bit blocks. By default, each channel uses one block (block 0 for channel 0, block 1 for channel 1, and so on).

If the data size of one single transfer is larger than one block size of TX channel  $n$  or RX channel  $m$ , users can configure the channel:

- to enable [wrap mode](#) by setting [RMT\\_MEM\\_TX/RX\\_WRAP\\_EN\\_CH \$n/m\$](#) ;
- or to use more blocks by configuring [RMT\\_MEM\\_SIZE\\_CH \$n/m\$](#) .

Setting [RMT\\_MEM\\_SIZE\\_CH \$n/m\$](#)  > 1 allows channel  $n/m$  to use the memory of the subsequent channels, i.e., block  $(n/m) \sim \text{block } (n/m + \text{RMT\_MEM\_SIZE\_CH}_{n/m} - 1)$ . In such case, the subsequent channels  $(n/m + 1) \sim (n/m + \text{RMT\_MEM\_SIZE\_CH}_{n/m} - 1)$  can not be used since their RAM blocks are occupied. For example, if channel 0 is configured to use block 0 and block 1, then channel 1 will be unavailable since its block is occupied, while channel 2 and channel 3 are not affected and can be used normally.

Note that the RAM used by each channel is mapped from low address to high address. Under such mapping, channel 0 is able to use the RAM blocks for channels 1, 2 ... and 7 by setting [RMT\\_MEM\\_SIZE\\_CH0](#), but channel 7 can not use the blocks for channels 0, 1, ... or 6. Therefore, the value of [RMT\\_MEM\\_SIZE\\_CH \$n\$](#)  should not exceed  $(8 - n)$  and the value of [RMT\\_MEM\\_SIZE\\_CH \$m\$](#)  should not exceed  $(8 - m)$ .

The RMT RAM can be accessed via APB bus, or read by the transmitter and written by the receiver. To avoid any possible access conflict between the receiver writing RAM and the APB bus reading RAM, RMT can be configured to designate the RAM block's owner, be it the receiver or the APB bus, by configuring [RMT\\_MEM\\_OWNER\\_CH \$m\$](#) . If this ownership is violated, a flag signal [RMT\\_MEM\\_OWNER\\_ERR\\_CH \$m\$](#)  will be generated.

### 52.3.2.3 RAM Access

APB bus is able to access RAM in FIFO mode and in NONFIFO (Direct Address) mode, depending on the configuration of [RMT\\_APB\\_FIFO\\_MASK](#):

- 0: Use FIFO mode;
- 1: Use NONFIFO mode.

Channels 3 and 7 also support GDMA access.

#### FIFO Mode

In FIFO mode, the APB reads data from or writes data to RAM via a fixed address stored in [RMT\\_CH \$n/m\$ DATA\\_REG](#).

#### NONFIFO Mode

In NONFIFO mode, the APB writes data to or reads data from a continuous address range.

- The write-starting address of TX channel  $n$  is: RMT base address +  $0x800 + (n - 1) \times 48$ . The access address for the second data and the following data are RMT base address +  $0x800 + (n - 1) \times 48 + 0x4$ , and so on, incremented by  $0x4$ .
- The read-starting address of RX channel  $m$  is: RMT base address +  $0x8C0 + (m - 1) \times 48$ . The access address for the second data and the following data are RMT base address +  $0x8C0 + (m - 1) \times 48 + 0x4$ , and so on, incremented by  $0x4$ .

#### GDMA Mode

Channel 3 also supports GDMA access. If [RMT\\_DMA\\_ACCESS\\_EN\\_CH3](#) is set, RAM of channel 3 only allows GDMA access. FIFO access or NOFIFO access to channel 3 by the APB bus are forbidden, otherwise

**unpredictable consequences may occur.**

To ensure correct data transmission,

1. GDMA should be started first.
2. RMT can only start transmitting data after GDMA channel gets data ready, otherwise, unexpected data may be sent.

In **normal TX mode**, when the RAM of channel 3 is fully written by GDMA, an [RMT\\_APB\\_MEM\\_WR\\_ERR\\_CH3](#) interrupt is triggered. Setting [RMT\\_MEM\\_TX\\_WRAP\\_EN\\_CH3](#) allows channel 3 to transmit more data than one block can fit, with no software operation needed.

Channel 7 also supports GDMA access. If [RMT\\_DMA\\_ACCESS\\_EN\\_CH7](#) is set, the RAM of channel 7 is allowed to transmit data to GDMA. Note in this mode, channel 7's RAM can also be accessed by APB via NONFIFO mode.

In **normal RX mode**, when the size of data read by GDMA from channel 7 is equal to its RAM size, an [RMT\\_APB\\_MEM\\_RD\\_ERR\\_CH7](#) is triggered and the subsequent data is discarded. If [RMT\\_MEM\\_RX\\_WRAP\\_EN\\_CH7](#) is set, data of more than one block size can be received with no software wrap operation needed. If channel 7's RAM is full but the GDMA still does not start receiving data from the channel, the newly received data by this channel will replace the previous data.

**Note:**

When channel 7 receives an end-marker, a GDMA `in_suc_eof` interrupt is generated. Two bytes are written to GDMA if the `period[14:0]` is 0, and four bytes to GDMA if the `period[30:16]` is 0.

### 52.3.3 Clock

The clock source of RMT can be `PLL_F80M_CLK`, `RC_FAST_CLK`, or `XTAL_CLK`, depending on the configuration of [HP\\_SYS\\_CLKRST\\_RMT\\_CLK\\_SRC\\_SEL](#). RMT clock can be enabled by setting [HP\\_SYS\\_CLKRST\\_RMT\\_CLK\\_EN](#). RMT working clock (see `rmt_sclk` in Figure 52.3-1) is obtained by dividing the selected clock source with a fractional divider. The divider is  $\text{HP\_SYS\_CLKRST\_RMT\_CLK\_DIV\_NUM} + 1 + \text{HP\_SYS\_CLKRST\_RMT\_CLK\_DIV\_NUMERATOR}$  or [HP\\_SYS\\_CLKRST\\_RMT\\_CLK\\_DIV\\_DENOMINATOR](#).

For more information, see Chapter 9 *Reset and Clock*. [RMT\\_DIV\\_CNT\\_CHn/m](#) is used to configure the divider coefficient of internal clock divider for RMT channels. The coefficient is normally equal to the value of [RMT\\_DIV\\_CNT\\_CHn/m](#), except value 0 that represents divider 256. The clock divider can be reset by setting [RMT\\_REF\\_CNT\\_RST\\_CHn/m](#). The clock generated from the divider can be used by the counter (see Figure 52.3-1).

### 52.3.4 Transmitter

**Note:**

Updating the configuration described in this and subsequent sections requires setting [RMT\\_CONF\\_UPDATE\\_CHn/m](#) first. See Section 52.3.6.

### 52.3.4.1 Normal TX Mode

When `RMT_TX_START_CH $n$`  is set, the transmitter of channel  $n$  starts reading and transmitting pulse codes from the starting address of its RAM block. The codes are sent starting from low-address entry. When an end-marker (a zero period) is encountered, the transmitter stops the transmission, returns to idle state and generates an `RMT_CH $n$ _TX_END_INT` interrupt. Setting `RMT_TX_STOP_CH $n$`  to 1 also stops the transmission and immediately sets the transmitter back to idle. The output level of a transmitter in idle state is determined by the “level” field of the end-marker or by the content of `RMT_IDLE_OUT_LV_CH $n$` , depending on the configuration of `RMT_IDLE_OUT_EN_CH $n$` :

- 0: The level in idle state is determined by the “level” field of the end-marker;
- 1: The level is determined by `RMT_IDLE_OUT_LV_CH $n$` .

### 52.3.4.2 Wrap TX Mode

To transmit more pulse codes than that can be fitted in the channel's RAM, users can enable wrap TX mode for channel  $n$  by setting `RMT_MEM_TX_WRAP_EN_CH $n$` . In this mode, the transmitter transmits the data from RAM in loops till an end-marker is encountered. For example, if `RMT_MEM_SIZE_CH $n$`  = 1, the transmitter starts transmitting data from the address  $48 \times n$ , and then the data from higher RAM address. Once the transmitter finishes transmitting data from  $(48 \times (n + 1) - 1)$ , it continues transmitting data from  $48 \times n$  again till an end-marker is encountered. Wrap mode is also applicable for `RMT_MEM_SIZE_CH $n$`  > 1.

When the size of transmitted pulse codes is larger than or equal to the value set by `RMT_TX_LIM_CH $n$` , an `RMT_CH $n$ _TX_THR_EVENT_INT` interrupt is generated. In wrap mode, `RMT_TX_LIM_CH $n$`  can be set to a half or a fraction of the size of the channel's RAM block. When an `RMT_CH $n$ _TX_THR_EVENT_INT` interrupt is detected by software, the already used RAM region can be updated by new pulse codes. In such way, the transmitter can seamlessly transmit unlimited pulse codes in wrap mode.

**Note:**

If RAM is accessed by GDMA, more pulse codes than one block size can be transmitted with no additional operation needed. If accessed by APB bus, wrap mode has to be enabled via software to transmit more data than one block size.

### 52.3.4.3 TX Modulation

Transmitter output can be modulated with a carrier wave by setting `RMT_CARRIER_EN_CH $n$` . The carrier waveform is configurable. In a carrier cycle, the high level lasts for  $(\text{RMT\_CARRIER\_HIGH\_CH}_n + 1)$  `rmt_sclk` cycles, while the low level lasts for  $(\text{RMT\_CARRIER\_LOW\_CH}_n + 1)$  `rmt_sclk` cycles. When `RMT_CARRIER_OUT_LV_CH $n$`  is set, carrier wave is added on the high-level of output signals; while `RMT_CARRIER_OUT_LV_CH $n$`  is cleared, carrier wave is added on the low-level of output signals. Carrier wave can be added on all output signals during modulation, or just added on valid pulse codes (the data stored in RAM), which can be set by configuring `RMT_CARRIER_EFF_EN_CH $n$` :

- 0: Add carrier wave on all output signals;
- 1: Add carrier wave only on valid signals.



#### 52.3.4.4 Continuous TX Mode

The continuous TX mode can be enabled by setting `RMT_TX_CONTI_MODE_CHn`. In this mode, the transmitter transmits the pulse codes from RAM in loops:

- If an end-marker is encountered, the transmitter starts transmitting from the first data of the channel's RAM again.
- If no end-marker is encountered, the transmitter starts transmitting from the first data again after the last data is transmitted.

If `RMT_TX_LOOP_CNT_EN_CHn` is set, the loop counting is incremented by 1 each time an end-marker is encountered. If the counting reaches the value set by `RMT_TX_LOOP_NUM_CHn`, an `RMT_CHn_TX_LOOP_INT` interrupt is generated. If `RMT_LOOP_STOP_EN_CHn` is set, the transmission stops immediately once an `RMT_CHn_TX_LOOP_INT` interrupt is generated, otherwise, the transmission will continue. In an end-maker, if its period[14:0] is 0, then the period of the previous data must satisfy:

$$6 \times T_{apb\_clk} + 12 \times T_{rmt\_sclk} < period \times T_{clk\_div} \quad (2)$$

The period of the other data only need to satisfy [relation \(1\)](#).

#### 52.3.4.5 Simultaneous TX Mode

RMT module supports multiple channels transmitting data simultaneously. To use this function, follow the steps below:

1. Configure `RMT_TX_SIM_CHn` to choose which multiple channels are used to transmit data simultaneously.
2. Set `RMT_TX_SIM_EN` to enable this transmission mode.
3. Set `RMT_TX_START_CHn` for each selected channel, to start data transmitting.

The transmission starts once the final channel is configured. RMT module also supports simultaneous transmission of channels 0 ~ 2's RAM accessed by APB bus and channel 3's RAM accessed by GDMA.

### 52.3.5 Receiver

#### 52.3.5.1 Normal RX Mode

The receiver of channel *m* is controlled by `RMT_RX_EN_CHm`:

- 0: The receiver stops receiving data;
- 1: The receiver starts working.

When the receiver becomes active, it starts counting from the first edge of the signal, detecting signal levels and counting clock cycles the level lasts for. Each cycle count (period) is then written back to RAM together with the level information (level). When the receiver detects no change in a signal level for a number of clock cycles more than the value set by `RMT_IDLE_THRES_CHm`, the receiver will stop receiving data, return to idle state, and generate an `RMT_CHm_RX_END_INT` interrupt. Please note that `RMT_IDLE_THRES_CHm` should be configured to a maximum value according to your application, otherwise a valid received level may be mistaken as a level in idle state. If the RAM space of this RX channel is used up by the received data, the receiver stops receiving data, and an `RMT_CHm_ERR_INT` interrupt is triggered by RAM FULL event.

### 52.3.5.2 Wrap RX Mode

To receive more pulse codes than can be fitted in the channel's RAM, users can enable wrap mode for channel  $m$  by configuring `RMT_MEM_RX_WRAP_EN_CHm`. But if RAM is accessed by GDMA, more pulse codes than one block size can be received with no additional operation needed. If accessed by APB bus, wrap mode has to be enabled to transmit more data than one block size. In wrap mode, the receiver stores the received data to RAM space of this channel in loops. Receiving ends, when the receiver detects no change in a signal level for a number of clock cycles more than the value set by `RMT_IDLE_THRES_CHm`. The receiver returns to idle state and generates an `RMT_CHm_RX_END_INT` interrupt. For example, if `RMT_MEM_SIZE_CHm` is set to 1, the receiver starts receiving data and stores the data to address  $48 * m$ , and then to higher RAM address. When the receiver finishes storing the received data to  $(48 * (m + 1) - 1)$ , the receiver continues receiving data and storing data to the address  $48 * m$  again, till no change is detected on a signal level for more than `RMT_IDLE_THRES_CHm` clock cycles. Wrap mode is also applicable for `RMT_MEM_SIZE_CHm > 1`.

An `RMT_CHm_RX_THR_EVENT_INT` interrupt is generated when the size of received pulse codes is larger than or equal to the value set by `RMT_CHm_RX_LIM_REG`. In wrap mode, `RMT_CHm_RX_LIM_REG` can be set to a half or a fraction of the size of the channel's RAM block. When an `RMT_CHm_RX_THR_EVENT_INT` interrupt is detected, the already used RAM region can be updated by subsequent data.

### 52.3.5.3 RX Filtering

Users can enable the receiver to filter input signals by setting `RMT_RX_FILTER_EN_CHm` for channel  $m$ . The filter samples input signals continuously, and detects the signals which remain unchanged for a continuous `RMT_RX_FILTER_THRES_CHm` rmt\_sclk cycles as valid, otherwise, the signals will be detected as invalid. Only the valid signals can pass through this filter. The filter removes pulses with a length of less than `RMT_RX_FILTER_THRES_CHm` rmt\_sclk cycles.

### 52.3.5.4 RX Demodulation

Users can enable RX demodulation on input signals or on filtered signals by setting `RMT_CARRIER_EN_CHm`. RX demodulation can be applied to high-level carrier wave or low-level carrier wave, depending on the configuration of `RMT_CARRIER_OUT_LV_CHm`:

- 0: Demodulate low-level carrier wave;
- 1: Demodulate high-level carrier wave.

Users can configure `RMT_CARRIER_HIGH_THRES_CHm` and `RMT_CARRIER_LOW_THRES_CHm` to set the thresholds to demodulate high-level carrier or low-level carrier. If the high-level of a signal lasts for less than `RMT_CARRIER_HIGH_THRES_CHm` clk\_div cycles, or the low-level lasts for less than `RMT_CARRIER_LOW_THRES_CHm` clk\_div cycles, such level is detected as a carrier and then is filtered out.

## 52.3.6 Configuration Update

To update RMT registers configuration, please set `RMT_CONF_UPDATE_CHn/m` for each channel first. All the bits/fields listed in the second column of Table 52.3-1 should follow this rule.

Table 52.3-1. Configuration Update

| Register                     | Bit/Field Configuration Update |
|------------------------------|--------------------------------|
| TX Channel                   |                                |
| RMT_CH $n$ CONFO_REG         | RMT_CARRIER_OUT_LV_CH $n$      |
|                              | RMT_CARRIER_EN_CH $n$          |
|                              | RMT_CARRIER_EFF_EN_CH $n$      |
|                              | RMT_DIV_CNT_CH $n$             |
|                              | RMT_TX_STOP_CH $n$             |
|                              | RMT_IDLE_OUT_EN_CH $n$         |
|                              | RMT_IDLE_OUT_LV_CH $n$         |
|                              | RMT_TX_CONTI_MODE_CH $n$       |
| RMT_CH $n$ CARRIER_DUTY_REG  | RMT_CARRIER_HIGH_CH $n$        |
|                              | RMT_CARRIER_LOW_CH $n$         |
| RMT_CH $n$ TX_LIM_REG        | RMT_TX_LOOP_CNT_EN_CH $n$      |
|                              | RMT_TX_LOOP_NUM_CH $n$         |
|                              | RMT_TX_LIM_CH $n$              |
| RMT_TX_SIM_REG               | RMT_TX_SIM_EN                  |
| RX Channel                   |                                |
| RMT_CH $m$ CONFO_REG         | RMT_CARRIER_OUT_LV_CH $m$      |
|                              | RMT_CARRIER_EN_CH $m$          |
|                              | RMT_IDLE_THRES_CH $m$          |
|                              | RMT_DIV_CNT_CH $m$             |
| RMT_CH $m$ CONF1_REG         | RMT_RX_FILTER_THRES_CH $m$     |
|                              | RMT_RX_EN_CH $m$               |
| RMT_CH $m$ RX_CARRIER_RM_REG | RMT_CARRIER_HIGH_THRES_CH $m$  |
|                              | RMT_CARRIER_LOW_THRES_CH $m$   |
| RMT_CH $m$ RX_LIM_REG        | RMT_RX_LIM_CH $m$              |
| RMT_REF_CNT_RST_REG          | RMT_REF_CNT_RST_CH $m$         |

## 52.4 Interrupts

ESP32-P4's RMT can generate the RMT\_INTR interrupt signal that will be sent to the [Interrupt Matrix](#).

The following interrupt sources can generate the RMT\_INTR interrupt signal:

- RMT\_CH $n$ \_ERR\_INT: Triggered when channel  $n$  does not read or write data correctly. For example, the transmitter still tries to read data from RAM when the RAM is empty.
- RMT\_CH $m$ \_ERR\_INT: Triggered when channel  $m$  does not read or write data correctly. For example, the receiver still tries to write data into RAM when the RAM is full.
- RMT\_CH $n$ \_TX\_THR\_EVENT\_INT: Triggered when the amount of data the transmitter has sent matches the value of RMT\_CH $n$ \_TX\_LIM\_REG.
- RMT\_CH $m$ \_RX\_THR\_EVENT\_INT: Triggered each time when the amount of data received by the receiver reaches the value set in RMT\_CH $m$ \_RX\_LIM\_REG.
- RMT\_CH $n$ \_TX\_END\_INT: Triggered when the transmitter has finished transmitting signals.

- RMT\_CH $m$ \_RX\_END\_INT: Triggered when the receiver has finished receiving signals.
- RMT\_CH $n$ \_TX\_LOOP\_INT: Triggered when the loop counting reaches the value set by [RMT\\_TX\\_LOOP\\_NUM\\_CH \$n\$](#)  in continuous TX mode.
- RMT\_CH3\_DMA\_ACCESS\_FAIL\_INT: Triggered when the result of (the entries written to channel 3's RAM - the entries transmitted by channel 3) is larger than channel 3's RAM size, but DAM keeps writing data to this channel.
- RMT\_CH7\_DMA\_ACCESS\_FAIL\_INT: Triggered when the result of (the entries received by channel 7's RAM - the entries read by GDMA) is larger than channel 7's RAM size, but channel 7 keeps receiving data.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [52.5 Register Summary](#).

## 52.5 Register Summary

The addresses in this section are relative to Remote Control Peripheral base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                      | Description   | Address | Access |
|---|---|---------|--------|
| <b>FIFO R/W registers</b>                 |   |         |        |
| <a href="#">RMT_CH0DATA_REG</a>           | The read and write data register for channel 0 by APB FIFO access | 0x0000  | HRO    |
| <a href="#">RMT_CH1DATA_REG</a>           | The read and write data register for channel 1 by APB FIFO access | 0x0004  | HRO    |
| <a href="#">RMT_CH2DATA_REG</a>           | The read and write data register for channel 2 by APB FIFO access | 0x0008  | HRO    |
| <a href="#">RMT_CH3DATA_REG</a>           | The read and write data register for channel 3 by APB FIFO access | 0x000C  | HRO    |
| <a href="#">RMT_CH4DATA_REG</a>           | The read and write data register for channel 4 by APB FIFO access | 0x0010  | HRO    |
| <a href="#">RMT_CH5DATA_REG</a>           | The read and write data register for channel 5 by APB FIFO access | 0x0014  | HRO    |
| <a href="#">RMT_CH6DATA_REG</a>           | The read and write data register for channel 6 by APB FIFO access | 0x0018  | HRO    |
| <a href="#">RMT_CH7DATA_REG</a>           | The read and write data register for channel 7 by APB FIFO access | 0x001C  | HRO    |
| <b>Configuration registers</b>            |   |         |        |
| <a href="#">RMT_CH0CONFO_REG</a>          | Configuration register 0 for channel 0                            | 0x0020  | varies |
| <a href="#">RMT_CH1CONFO_REG</a>          | Configuration register 0 for channel 1                            | 0x0024  | varies |
| <a href="#">RMT_CH2CONFO_REG</a>          | Configuration register 0 for channel 2                            | 0x0028  | varies |
| <a href="#">RMT_CH3CONFO_REG</a>          | Configuration register 0 for channel 3                            | 0x002C  | varies |
| <a href="#">RMT_CH4CONFO_REG</a>          | Configuration register 0 for channel 4                            | 0x0030  | R/W    |
| <a href="#">RMT_CH4CONF1_REG</a>          | Configuration register 1 for channel 4                            | 0x0034  | varies |
| <a href="#">RMT_CH5CONFO_REG</a>          | Configuration register 0 for channel 5                            | 0x0038  | R/W    |
| <a href="#">RMT_CH5CONF1_REG</a>          | Configuration register 1 for channel 5                            | 0x003C  | varies |
| <a href="#">RMT_CH6CONFO_REG</a>          | Configuration register 0 for channel 6                            | 0x0040  | R/W    |
| <a href="#">RMT_CH6CONF1_REG</a>          | Configuration register 1 for channel 6                            | 0x0044  | varies |
| <a href="#">RMT_CH7CONFO_REG</a>          | Configuration register 0 for channel 7                            | 0x0048  | R/W    |
| <a href="#">RMT_CH7CONF1_REG</a>          | Configuration register 1 for channel 7                            | 0x004C  | varies |
| <a href="#">RMT_CH4_RX_CARRIER_RM_REG</a> | Carrier remove register for channel 4                             | 0x0090  | R/W    |
| <a href="#">RMT_CH5_RX_CARRIER_RM_REG</a> | Carrier remove register for channel 5                             | 0x0094  | R/W    |
| <a href="#">RMT_CH6_RX_CARRIER_RM_REG</a> | Carrier remove register for channel 6                             | 0x0098  | R/W    |
| <a href="#">RMT_CH7_RX_CARRIER_RM_REG</a> | Carrier remove register for channel 7                             | 0x009C  | R/W    |
| <a href="#">RMT_SYS_CONF_REG</a>          | RMT APB configuration register                                    | 0x00C0  | R/W    |
| <a href="#">RMT_REF_CNT_RST_REG</a>       | RMT clock divider reset register                                  | 0x00C8  | WT     |
| <b>Status registers</b>                   |   |         |        |

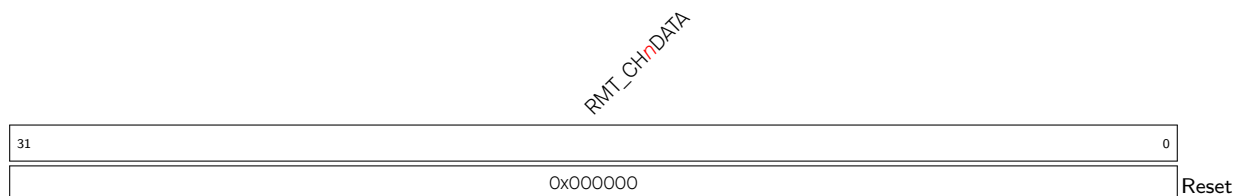
| Name                                     | Description                                     | Address | Access   |
|--|---|---------|----------|
| <a href="#">RMT_CH0STATUS_REG</a>        | Status register for channel 0                   | 0x0050  | RO       |
| <a href="#">RMT_CH1STATUS_REG</a>        | Status register for channel 1                   | 0x0054  | RO       |
| <a href="#">RMT_CH2STATUS_REG</a>        | Status register for channel 2                   | 0x0058  | RO       |
| <a href="#">RMT_CH3STATUS_REG</a>        | Status register for channel 3                   | 0x005C  | RO       |
| <a href="#">RMT_CH4STATUS_REG</a>        | Status register for channel 4                   | 0x0060  | RO       |
| <a href="#">RMT_CH5STATUS_REG</a>        | Status register for channel 5                   | 0x0064  | RO       |
| <a href="#">RMT_CH6STATUS_REG</a>        | Status register for channel 6                   | 0x0068  | RO       |
| <a href="#">RMT_CH7STATUS_REG</a>        | Status register for channel 7                   | 0x006C  | RO       |
| <b>Interrupt registers</b>               |   |         |          |
| <a href="#">RMT_INT_RAW_REG</a>          | Interrupt raw signal status register            | 0x0070  | R/WTC/SS |
| <a href="#">RMT_INT_ST_REG</a>           | Interrupt signal status register                | 0x0074  | RO       |
| <a href="#">RMT_INT_ENA_REG</a>          | Interrupt enable signal configuration register  | 0x0078  | R/W      |
| <a href="#">RMT_INT_CLR_REG</a>          | Interrupt clear signal configuration register   | 0x007C  | WT       |
| <b>Carrier wave duty cycle registers</b> |   |         |          |
| <a href="#">RMT_CH0CARRIER_DUTY_REG</a>  | Duty cycle configuration register for channel 0 | 0x0080  | R/W      |
| <a href="#">RMT_CH1CARRIER_DUTY_REG</a>  | Duty cycle configuration register for channel 1 | 0x0084  | R/W      |
| <a href="#">RMT_CH2CARRIER_DUTY_REG</a>  | Duty cycle configuration register for channel 2 | 0x0088  | R/W      |
| <a href="#">RMT_CH3CARRIER_DUTY_REG</a>  | Duty cycle configuration register for channel 3 | 0x008C  | R/W      |
| <b>TX event configuration registers</b>  |   |         |          |
| <a href="#">RMT_CH0_TX_LIM_REG</a>       | Configuration register for channel 0 TX event   | 0x00A0  | varies   |
| <a href="#">RMT_CH1_TX_LIM_REG</a>       | Configuration register for channel 1 TX event   | 0x00A4  | varies   |
| <a href="#">RMT_CH2_TX_LIM_REG</a>       | Configuration register for channel 2 TX event   | 0x00A8  | varies   |
| <a href="#">RMT_CH3_TX_LIM_REG</a>       | Configuration register for channel 3 TX event   | 0x00AC  | varies   |
| <a href="#">RMT_TX_SIM_REG</a>           | RMT TX synchronous register                     | 0x00C4  | R/W      |
| <b>RX event configuration registers</b>  |   |         |          |
| <a href="#">RMT_CH4_RX_LIM_REG</a>       | Configuration register for channel 4 RX event   | 0x00B0  | R/W      |
| <a href="#">RMT_CH5_RX_LIM_REG</a>       | Configuration register for channel 5 RX event   | 0x00B4  | R/W      |
| <a href="#">RMT_CH6_RX_LIM_REG</a>       | Configuration register for channel 6 RX event   | 0x00B8  | R/W      |
| <a href="#">RMT_CH7_RX_LIM_REG</a>       | Configuration register for channel 7 RX event   | 0x00BC  | R/W      |
| <b>Version register</b>                  |   |         |          |
| <a href="#">RMT_DATE_REG</a>             | Version control register                        | 0x00CC  | R/W      |

## 52.6 Registers

The addresses in this section are relative to Remote Control Peripheral base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

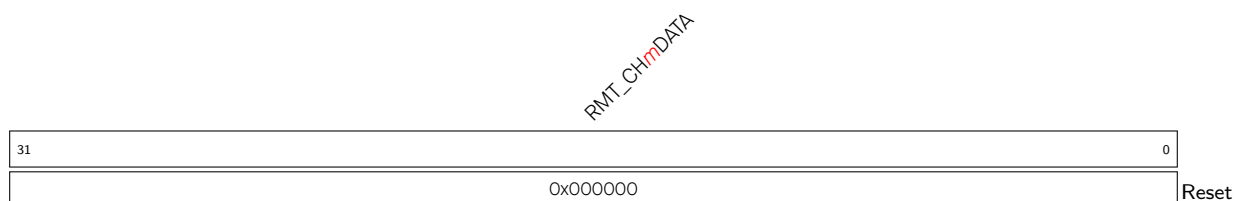
For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

**Register 52.1. RMT\_CH $n$ DATA\_REG ( $n$ : 0-3) (0x0000+0x4\* $n$ )**



**RMT\_CH $n$ DATA** Read and write data for channel  $n$  via APB FIFO. (HRO)

**Register 52.2. RMT\_CH $m$ DATA\_REG ( $m$ : 4-7) (0x0000+0x4\* $m$ )**



**RMT\_CH $m$ DATA** Read and write data for channel  $n$  via APB FIFO. (HRO)

Register 52.3. RMT\_CH $n$ CONF0\_REG ( $n$ : 0-3) (0x0020+0x4\* $n$ )

[illegible]

**RMT\_TX\_START\_CH $n$**  Configures whether to enable sending data in channel  $n$ .

0: No effect

1: Enable

(WT)

**RMT\_MEM\_RD\_RST\_CH $n$**  Configures whether to reset RAM read address accessed by the transmitter for channel  $n$ .

0: No effect

1: Reset

(WT)

**RMT\_APB\_MEM\_RST\_CH $n$**  Configures whether to reset RAM W/R address accessed by APB FIFO for channel  $n$ .

0: No effect

1: Reset

(WT)

**RMT\_TX\_CONTI\_MODE\_CH $n$**  Configures whether to enable continuous TX mode for channel  $n$ .

0: No Effect

1: Enable

In this mode, the transmitter starts transmission from the first data. If an end-marker is encountered, the transmitter starts transmitting data from the first data again; if no end-marker is encountered, the transmitter starts transmitting the first data again when the last data is transmitted.

(R/W)

**RMT\_MEM\_TX\_WRAP\_EN\_CH $n$**  Configures whether to enable wrap TX mode for channel  $n$ .

0: No effect

1: Enable

In this mode, if the TX data size is larger than the channel's RAM block size, the transmitter continues transmitting the first data to the last data in loops.

(R/W)

**RMT\_IDLE\_OUT\_LV\_CH $n$**  Configures the level of output signal for channel  $n$  when the transmitter is in idle state. (R/W)

Continued on the next page...



**Register 52.3. RMT\_CH $n$ CONFO\_REG ( $n$ : 0-3) (0x0020+0x4\* $n$ )**

Continued from the previous page...

**RMT\_IDLE\_OUT\_EN\_CH $n$**  Configures whether to enable the output for channel  $n$  in idle state.

0: No effect

1: Enable

(R/W)

**RMT\_TX\_STOP\_CH $n$**  Configures whether to stop the transmitter of channel  $n$  sending data out.

0: No effect

1: Stop

(R/W/SC)

**RMT\_DIV\_CNT\_CH $n$**  Configures the divider for clock of channel  $n$ .

Measurement unit: rmt\_sclk

(R/W)

**RMT\_MEM\_SIZE\_CH $n$**  Configures the maximum number of memory blocks allocated to channel  $n$ .

(R/W)

**RMT\_CARRIER\_EFF\_EN\_CH $n$**  Configures whether to add carrier modulation on the output signal only at data-sending state for channel  $n$ .

0: Add carrier modulation on the output signal at data-sending state and idle state for channel  $n$

1: Add carrier modulation on the output signal only at data-sending state for channel  $n$

Only valid when RMT\_CARRIER\_EN\_CH $n$  is 1.

(R/W)

**RMT\_CARRIER\_EN\_CH $n$**  Configures whether to enable the carrier modulation on output signal for channel  $n$ .

0: Disable

1: Enable

(R/W)

**RMT\_CARRIER\_OUT\_LV\_CH $n$**  Configures the position of carrier wave for channel  $n$ .

0: Add carrier wave on low level

1: Add carrier wave on high level

(R/W)

**RMT\_CONF\_UPDATE\_CH $n$**  Synchronization bit for channel  $n$ . (WT)

**RMT\_DMA\_ACCESS\_EN\_CH3** Configures whether to enable the DMA access function for channel

3. This field is reserved for channel 0 ~ 2.

0: Disable

1: Enable

(R/W)

**Register 52.4. RMT\_CH $m$ CONFO\_REG ( $m$ : 4-7) (0x0030, 0x0038, 0x0040, 0x0048)**

|            |    |    |    |                                    |    |    |        |                                |  |  |  |                              |  |  |     |                       |   |  |  |                                |  |  |       |  |  |   |  |                             |  |  |  |
|------------|----|----|----|------------------------------------|----|----|--------|--------------------------------|--|--|--|------------------------------|--|--|-----|-----------------------|---|--|--|--------------------------------|--|--|-------|--|--|---|--|-----------------------------|--|--|--|
| (reserved) |    |    |    | RMT_CARRIER_OUT_LV_CH <sup>m</sup> |    |    |        | RMT_CARRIER_EN_CH <sup>m</sup> |  |  |  | RMT_MEM_SIZE_CH <sup>m</sup> |  |  |     | RMT_DMA_ACCESS_EN_CH7 |   |  |  | RMT_IDLE_THRES_CH <sup>m</sup> |  |  |       |  |  |   |  | RMT_DIV_CNT_CH <sup>m</sup> |  |  |  |
| 31         | 30 | 29 | 28 | 27                                 | 24 | 23 | 22     |                                |  |  |  |                              |  |  |     | 8                     | 7 |  |  |                                |  |  |       |  |  | 0 |  |                             |  |  |  |
| 0          | 0  | 1  | 1  | 0x1                                |    | 0  | 0x7fff |                                |  |  |  |                              |  |  | 0x2 |                       |   |  |  |                                |  |  | Reset |  |  |   |  |                             |  |  |  |

Reset

**RMT\_DIV\_CNT\_CH $m$**  Configures the clock divider of channel  $m$ .

Measurement unit: rmt\_sclk

(R/W)

**RMT\_IDLE\_THRES\_CH $m$**  Configures RX threshold. When no edge is detected on the input signal for continuous clock cycles longer than this field value, the receiver stops receiving data.

Measurement unit: clk\_div

(R/W)

**RMT\_DMA\_ACCESS\_EN\_CH7** Configures whether to enable the DMA access function for channel 7. This field is reserved for channel 4 ~ 6.

0: Disable

1: Enable

(R/W)

**RMT\_MEM\_SIZE\_CH $m$**  Configures the maximum number of memory blocks allocated to channel  $m$ .

(R/W)

**RMT\_CARRIER\_EN\_CH $m$**  Configures whether to enable carrier demodulation on output signal for channel  $m$ .

0: Disable

1: Enable

(R/W)

**RMT\_CARRIER\_OUT\_LV\_CH $m$**  Configures the position of carrier wave for channel  $m$ .

0: Demodulate carrier wave on low level

1: Demodulate carrier wave on high level

(R/W)

Register 52.5. RMT\_CH $m$ CONF1\_REG ( $m$ : 4-7) (0x0034, 0x003C, 0x0044, 0x004C)

|                                 |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    |  |    |   |     |  |  |   |   |   |   |   |   |       |
|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|----|----|----|--|----|---|-----|--|--|---|---|---|---|---|---|-------|
| (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    | RMT_CONF_UPDATE_CH <sup>m</sup><br>(reserved)<br>RMT_MEM_RX_WRAP_EN_CH <sup>m</sup><br>RMT_RX_FILTER_THRES_CH <sup>m</sup><br>RMT_RX_FILTER_EN_CH <sup>m</sup><br>RMT_MEM_OWNER_CH <sup>m</sup><br>RMT_APB_MEM_RST_CH <sup>m</sup><br>RMT_MEM_WRP_RST_CH <sup>m</sup><br>RMT_RX_EN_CH <sup>m</sup> |    |   |     |  |  |   |   |   |   |   |   |       |
| 31                              |  |  |  |  |  |  |  |  |  |  |  |  | 16 | 15 | 14 | 13   | 12 |   |     |  |  | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |    |    |    | 0  | 0  | 0 | 0xf |  |  |   | 0 | 1 | 0 | 0 | 0 | Reset |

**RMT\_RX\_EN\_CH $m$**  Configures whether to enable the receiver to start receiving data in channel  $m$ .

0: Disable

1: Enable

(R/W)

**RMT\_MEM\_WR\_RST\_CH $m$**  Configures whether to reset RAM write address accessed by the receiver for channel  $m$ .

0: No effect

1: Reset

(WT)

**RMT\_APB\_MEM\_RST\_CH $m$**  Configures whether to reset RAM W/R address accessed by APB FIFO for channel  $m$ .

0: No effect

1: Reset

(WT)

**RMT\_MEM\_OWNER\_CH $m$**  Configures the ownership of channel  $m$ 's RAM block.

0: APB bus is using the RAM

1: Receiver is using the RAM

(R/W/SC)

**RMT\_RX\_FILTER\_EN\_CH $m$**  Configures whether to enable the receiver's filter for channel  $m$ .

0: Disable

1: Enable

(R/W)

**RMT\_RX\_FILTER\_THRES\_CH $m$**  Configures whether the receiver, when receiving data, ignores the input pulse when its width is shorter than this register value in units of rmt\_sclk cycles.

0: No effect

1: Reset

(R/W)

**RMT\_MEM\_RX\_WRAP\_EN\_CH $m$**  Configures whether to enable wrap RX mode for channel  $m$ .

0: Disable

1: Enable

In this mode, if the RX data size is larger than channel  $m$ 's RAM block size, the receiver stores the RX data from the first address to the last address in loops.

(R/W)

**RMT\_CONF\_UPDATE\_CH $m$**  Synchronization bit for channel  $m$ . (WT)

**Register 52.6. RMT\_CH $m$ \_RX\_CARRIER\_RM\_REG ( $m$ : 4-7) (0x0090, 0x0094, 0x0098, 0x009C)**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| RMT_CARRIER_HIGH_THRES_CH <sub>m</sub> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | RMT_CARRIER_LOW_THRES_CH <sub>m</sub> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x00                                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**RMT\_CARRIER\_LOW\_THRES\_CH $m$**  Configures the low level period in a carrier modulation mode for channel  $m$ , which is equal to (RMT\_CARRIER\_LOW\_THRES\_CH $m$  + 1). (R/W)

**RMT\_CARRIER\_HIGH\_THRES\_CH $m$**  Configures the high level period in a carrier modulation mode for channel  $m$ , which is equal to (RMT\_CARRIER\_HIGH\_THRES\_CH $m$  + 1). (R/W)

**Register 52.7. RMT\_SYS\_CONF\_REG (0x00C0)**

|            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |            |  |   |  |
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| RMT_CLK_EN |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | (reserved) |  | ( |  |
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**RMT\_APB\_FIFO\_MASK** Configures the memory access mode.

0: Access memory by FIFO

1: Access memory directly

(R/W)

**RMT\_CLK\_EN** Configures whether to enable signal of RMT register clock gate.

0: Power down the drive clock of registers

1: Power up the drive clock of registers

(R/W)

Register 52.8. RMT\_REF\_CNT\_RST\_REG (0x00C8)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |   |   |       |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|---|---|-------|
| (reserved)                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | RMT_REF_CNT_RST_CH7<br>RMT_REF_CNT_RST_CH6<br>RMT_REF_CNT_RST_CH5<br>RMT_REF_CNT_RST_CH4<br>RMT_REF_CNT_RST_CH3<br>RMT_REF_CNT_RST_CH2<br>RMT_REF_CNT_RST_CH1<br>RMT_REF_CNT_RST_CH0 |   |   |   |   |   |   |   |   |       |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 8  | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |       |

**RMT\_REF\_CNT\_RST\_CH $n$**  ( $n$ : 0-3) Configures whether to reset the clock divider of channel  $n$ .  
0: No effect  
1: Reset  
(WT)

**RMT\_REF\_CNT\_RST\_CH $m$**  ( $m$ : 4-7) Configures whether to reset the clock divider of channel  $m$ .  
0: No effect  
1: Reset  
(WT)



**Register 52.10. RMT\_CH $m$ STATUS\_REG ( $m$ : 4-7) (0x0050+0x4\* $m$ )**

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| (reserved) |    |    |    | RMT_APB_MEM_RD_ERR_CH <sup>m</sup> |    |    |    | RMT_MEM_FULL_CH <sup>m</sup> |  |  |  | RMT_MEM_OWNER_ERR_CH <sup>m</sup> |  |  |  | RMT_STATE_CH <sup>m</sup> |  |  |  | (reserved) |  |  |  | RMT_APB_MEM_RADDR_CH <sup>m</sup> |  |  |  | (reserved) |  |  |  | RMT_MEM_WADDR_EX_CH <sup>m</sup> |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 28 | 27 | 26 | 25                                 | 24 | 22 | 21 | 20                           |  |  |  |                                   |  |  |  |                           |  |  |  |            |  |  |  |                                   |  |  |  |            |  |  |  |                                  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Reset

**RMT\_MEM\_WADDR\_EX\_CH $m$**  Represents the memory address offset when receiver of channel  $m$  is using the RAM. (RO)

**RMT\_APB\_MEM\_RADDR\_CH $m$**  Represents the memory address offset when reads RAM over APB bus. (RO)

**RMT\_STATE\_CH $m$**  Represents the FSM status of channel  $m$ . (RO)

**RMT\_MEM\_OWNER\_ERR\_CH $m$**  Represents whether the ownership of memory block is wrong.

- 0: The ownership of memory block is correct
- 1: The ownership of memory block is wrong

(RO)

**RMT\_MEM\_FULL\_CH $m$**  Represents whether the receiver receives more data than the memory can fit.

- 0: The receiver does not receive more data than the memory can fit
- 1: The receiver receives more data than the memory can fit

(RO)

**RMT\_APB\_MEM\_RD\_ERR\_CH $m$**  Represents whether the offset address exceeds memory size (overflows) when reads RAM via APB bus.

- 0: Not exceed
- 1: Exceed

(RO)

## Register 52.11. RMT\_INT\_RAW\_REG (0x0070)

|  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>RMT_CH7_DMA_ACCESS_FAIL_INT_RAW</div> <div>RMT_CH3_DMA_ACCESS_FAIL_INT_RAW</div> <div>RMT_CH7_RX_THR_EVENT_INT_RAW</div> <div>RMT_CH6_RX_THR_EVENT_INT_RAW</div> <div>RMT_CH5_RX_THR_EVENT_INT_RAW</div> <div>RMT_CH4_RX_THR_EVENT_INT_RAW</div> <div>RMT_CH7_ERR_INT_RAW</div> <div>RMT_CH6_ERR_INT_RAW</div> <div>RMT_CH5_ERR_INT_RAW</div> <div>RMT_CH4_ERR_INT_RAW</div> <div>RMT_CH7_RX_END_INT_RAW</div> <div>RMT_CH6_RX_END_INT_RAW</div> <div>RMT_CH5_RX_END_INT_RAW</div> <div>RMT_CH4_RX_END_INT_RAW</div> <div>RMT_CH3_TX_LOOP_INT_RAW</div> <div>RMT_CH2_TX_LOOP_INT_RAW</div> <div>RMT_CH1_TX_LOOP_INT_RAW</div> <div>RMT_CH0_TX_THR_EVENT_INT_RAW</div> <div>RMT_CH3_TX_THR_EVENT_INT_RAW</div> <div>RMT_CH2_TX_THR_EVENT_INT_RAW</div> <div>RMT_CH1_TX_THR_EVENT_INT_RAW</div> <div>RMT_CH0_TX_THR_EVENT_INT_RAW</div> <div>RMT_CH3_TX_END_INT_RAW</div> <div>RMT_CH2_TX_END_INT_RAW</div> <div>RMT_CH1_TX_END_INT_RAW</div> <div>RMT_CH0_TX_END_INT_RAW</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**RMT\_CH $n$ \_TX\_END\_INT\_RAW ( $n$ : 0-3)** The raw interrupt status of [RMT\\_CH \$n\$ \\_TX\\_END\\_INT](#). (R/WTC/SS)

**RMT\_CH $n$ \_ERR\_INT\_RAW ( $n$ : 0-3)** The raw interrupt status of [RMT\\_CH \$n\$ \\_ERR\\_INT](#). (R/WTC/SS)

**RMT\_CH $n$ \_TX\_THR\_EVENT\_INT\_RAW ( $n$ : 0-3)** The raw interrupt status of [RMT\\_CH \$n\$ \\_TX\\_THR\\_EVENT\\_INT](#). (R/WTC/SS)

**RMT\_CH $n$ \_TX\_LOOP\_INT\_RAW ( $n$ : 0-3)** The raw interrupt status of [RMT\\_CH \$n\$ \\_TX\\_LOOP\\_INT](#). (R/WTC/SS)

**RMT\_CH $m$ \_RX\_END\_INT\_RAW ( $m$ : 4-7)** The raw interrupt status of [RMT\\_CH \$m\$ \\_RX\\_END\\_INT](#). (R/WTC/SS)

**RMT\_CH $m$ \_ERR\_INT\_RAW ( $m$ : 4-7)** The raw interrupt status of [RMT\\_CH \$m\$ \\_ERR\\_INT](#). (R/WTC/SS)

**RMT\_CH $m$ \_RX\_THR\_EVENT\_INT\_RAW ( $m$ : 4-7)** The raw interrupt status of [RMT\\_CH \$m\$ \\_RX\\_THR\\_EVENT\\_INT](#). (R/WTC/SS)

**RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT\_RAW ( $n$ : 3)** The raw interrupt status of [RMT\\_CH \$n\$ \\_DMA\\_ACCESS\\_FAIL\\_INT](#). (R/WTC/SS)

**RMT\_CH $m$ \_DMA\_ACCESS\_FAIL\_INT\_RAW ( $m$ : 7)** The raw interrupt status of [RMT\\_CH \$m\$ \\_DMA\\_ACCESS\\_FAIL\\_INT](#). (R/WTC/SS)



### Register 52.12. RMT\_INT\_ST\_REG (0x0074)

[illegible]

**RMT\_CH*n*\_TX\_END\_INT\_ST** (*n*: 0-3) The masked interrupt status of **RMT\_CH*n*\_TX\_END\_INT**. (RO)

**RMT\_CHn\_ERR\_INT\_ST** (*n*: 0-3) The masked interrupt status of **RMT\_CHn\_ERR\_INT**. (RO)

**RMT\_CH $n$ \_TX\_THR\_EVENT\_INT\_ST** ( $n$ : 0-3) The masked interrupt status of  
RMT\_CH $n$ \_TX\_THR\_EVENT\_INT. (RO)

**RMT\_CH***n*\_TX\_LOOP\_INT\_ST (*n*: 0-3) The masked interrupt status of **RMT\_CH***n*\_TX\_LOOP\_INT.  
(RO)

**RMT\_CH***m*\_RX\_END\_INT\_ST (*m*: 4-7) The masked interrupt status of **RMT\_CH***m*\_RX\_END\_INT.  
(RO)

**RMT\_CH $m$ \_ERR\_INT\_ST** ( $m$ : 4-7) The masked interrupt status of **RMT\_CH $m$ \_ERR\_INT**. (RO)

**RMT\_CHm\_RX\_THR\_EVENT\_INT\_ST** (*m*: 4-7) The masked interrupt status of **RMT\_CHm\_RX\_THR\_EVENT\_INT**. (RO)

**RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT\_ST** ( $n$ : 3) The masked interrupt status of RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT. (RO)

**RMT\_CHm\_DMA\_ACCESS\_FAIL\_INT\_ST** (*m*: 7) The masked interrupt status of **RMT\_CHm\_DMA\_ACCESS\_FAIL\_INT**. (RO)

Register 52.13. RMT\_INT\_ENA\_REG (0x0078)

|   |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|-------|
| <div>(reserved)</div> <div>RMT_CH7_DMA_ACCESS_FAIL_INT_ENA</div> <div>RMT_CH3_DMA_ACCESS_FAIL_INT_ENA</div> <div>RMT_CH7_RX_THR_EVENT_INT_ENA</div> <div>RMT_CH6_RX_THR_EVENT_INT_ENA</div> <div>RMT_CH5_RX_THR_EVENT_INT_ENA</div> <div>RMT_CH4_RX_THR_EVENT_INT_ENA</div> <div>RMT_CH7_ERR_INT_ENA</div> <div>RMT_CH6_ERR_INT_ENA</div> <div>RMT_CH5_ERR_INT_ENA</div> <div>RMT_CH4_ERR_INT_ENA</div> <div>RMT_CH7_RX_END_INT_ENA</div> <div>RMT_CH6_RX_END_INT_ENA</div> <div>RMT_CH5_RX_END_INT_ENA</div> <div>RMT_CH4_RX_END_INT_ENA</div> <div>RMT_CH3_TX_LOOP_INT_ENA</div> <div>RMT_CH2_TX_LOOP_INT_ENA</div> <div>RMT_CH1_TX_LOOP_INT_ENA</div> <div>RMT_CH0_TX_LOOP_INT_ENA</div> <div>RMT_CH3_TX_THR_EVENT_INT_ENA</div> <div>RMT_CH2_TX_THR_EVENT_INT_ENA</div> <div>RMT_CH1_TX_THR_EVENT_INT_ENA</div> <div>RMT_CH0_TX_THR_EVENT_INT_ENA</div> <div>RMT_CH3_ERR_INT_ENA</div> <div>RMT_CH2_ERR_INT_ENA</div> <div>RMT_CH1_ERR_INT_ENA</div> <div>RMT_CH0_ERR_INT_ENA</div> <div>RMT_CH3_TX_END_INT_ENA</div> <div>RMT_CH2_TX_END_INT_ENA</div> <div>RMT_CH1_TX_END_INT_ENA</div> <div>RMT_CH0_TX_END_INT_ENA</div> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |       |
| 0   | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

RMT\_CH $n$ \_TX\_END\_INT\_ENA ( $n$ : 0-3) Write 1 to enable [RMT\\_CH \$n\$ \\_TX\\_END\\_INT](#). (R/W)

RMT\_CH $n$ \_ERR\_INT\_ENA ( $n$ : 0-3) Write 1 to enable [RMT\\_CH \$n\$ \\_ERR\\_INT](#). (R/W)

RMT\_CH $n$ \_TX\_THR\_EVENT\_INT\_ENA ( $n$ : 0-3) Write 1 to enable [RMT\\_CH \$n\$ \\_TX\\_THR\\_EVENT\\_INT](#). (R/W)

RMT\_CH $n$ \_TX\_LOOP\_INT\_ENA ( $n$ : 0-3) Write 1 to enable [RMT\\_CH \$n\$ \\_TX\\_LOOP\\_INT](#). (R/W)

RMT\_CH $m$ \_RX\_END\_INT\_ENA ( $m$ : 4-7) Write 1 to enable [RMT\\_CH \$m\$ \\_RX\\_END\\_INT](#). (R/W)

RMT\_CH $m$ \_ERR\_INT\_ENA ( $m$ : 4-7) Write 1 to enable [RMT\\_CH \$m\$ \\_ERR\\_INT](#). (R/W)

RMT\_CH $m$ \_RX\_THR\_EVENT\_INT\_ENA ( $m$ : 4-7) Write 1 to enable [RMT\\_CH \$m\$ \\_RX\\_THR\\_EVENT\\_INT](#). (R/W)

RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT\_ENA ( $n$ : 3) Write 1 to enable [RMT\\_CH \$n\$ \\_DMA\\_ACCESS\\_FAIL\\_INT](#). (R/W)

RMT\_CH $m$ \_DMA\_ACCESS\_FAIL\_INT\_ENA ( $m$ : 7) Write 1 to enable [RMT\\_CH \$m\$ \\_DMA\\_ACCESS\\_FAIL\\_INT](#). (R/W)

## Register 52.14. RMT\_INT\_CLR\_REG (0x007C)

|            |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        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|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-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| (reserved) |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   | RMT_CH7_DMA_ACCESS_FAIL_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH3_DMA_ACCESS_FAIL_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH7_RX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH6_RX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH5_RX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH4_RX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH7_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH6_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH5_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH4_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH7_RX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH6_RX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH5_RX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH4_RX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH3_TX_LOOP_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH2_TX_LOOP_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH1_TX_LOOP_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH0_TX_LOOP_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH3_TX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH2_TX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH1_TX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH0_TX_THR_EVENT_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH3_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH2_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH1_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH0_ERR_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH3_TX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH2_TX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH1_TX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH0_TX_END_INT_CLR |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Reset                           |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                              |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                     |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                               | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                            | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

RMT\_CH $n$ \_TX\_END\_INT\_CLR ( $n$ : 0-3) Write 1 to clear RMT\_CH $n$ \_TX\_END\_INT. (WT)

RMT\_CH $n$ \_ERR\_INT\_CLR ( $n$ : 0-3) Write 1 to clear RMT\_CH $n$ \_ERR\_INT. (WT)

RMT\_CH $n$ \_TX\_THR\_EVENT\_INT\_CLR ( $n$ : 0-3) Write 1 to clear RMT\_CH $n$ \_TX\_THR\_EVENT\_INT. (WT)

RMT\_CH $n$ \_TX\_LOOP\_INT\_CLR ( $n$ : 0-3) Write 1 to clear RMT\_CH $n$ \_TX\_LOOP\_INT. (WT)

RMT\_CH $m$ \_RX\_END\_INT\_CLR ( $m$ : 4-7) Write 1 to clear RMT\_CH $m$ \_RX\_END\_INT. (WT)

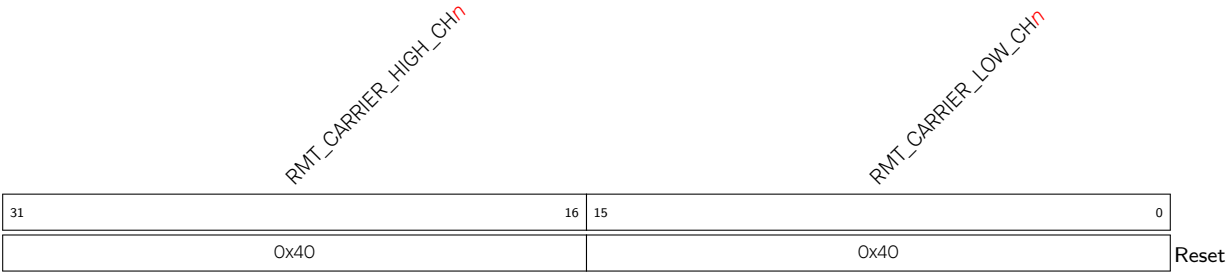
RMT\_CH $m$ \_ERR\_INT\_CLR ( $m$ : 4-7) Write 1 to clear RMT\_CH $m$ \_ERR\_INT. (WT)

RMT\_CH $m$ \_RX\_THR\_EVENT\_INT\_CLR ( $m$ : 4-7) Write 1 to clear RMT\_CH $m$ \_RX\_THR\_EVENT\_INT.  
(WT)

RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT\_CLR ( $n$ : 3) Write 1 to clear RMT\_CH $n$ \_DMA\_ACCESS\_FAIL\_INT.  
(WT)

RMT\_CH $m$ \_DMA\_ACCESS\_FAIL\_INT\_CLR ( $m$ : 7) Write 1 to clear RMT\_CH $m$ \_DMA\_ACCESS\_FAIL\_INT.  
(WT)

Register 52.15. RMT\_CHnCARRIER\_DUTY\_REG (n: 0-3) (0x0080+0x4\*n)



**RMT\_CARRIER\_LOW\_CHn** Configures carrier wave's low level clock period for channel *n*.  
Measurement unit: rmt\_sclk  
(R/W)

**RMT\_CARRIER\_HIGH\_CHn** Configures carrier wave's high level clock period for channel *n*.  
Measurement unit: rmt\_sclk  
(R/W)

Register 52.16. RMT\_CH $n$ \_TX\_LIM\_REG ( $n$ : 0-3) (0x00A0+0x4\* $n$ )

|            |   |   |   |   |   |   |   |   |   |  |    |    |    |                                 |    |  |  |                            |      |   |   |  |       |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|--|----|----|----|---------------------------------|----|--|--|----------------------------|------|---|---|--|-------|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   | RMT_LOOP_STOP_EN_CH <sup>n</sup><br>RMT_LOOP_COUNT_RESET_CH <sup>n</sup><br>RMT_TX_LOOP_CNT_EN_CH <sup>n</sup> |    |    |    | RMT_TX_LOOP_NUM_CH <sup>n</sup> |    |  |  | RMT_TX_LIM_CH <sup>n</sup> |      |   |   |  |       |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |  | 22 | 21 | 20 | 19                              | 18 |  |  |                            |      | 9 | 8 |  |       |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0  | 0                               | 0  |  |  |                            | 0x80 |   |   |  | Reset |  |  |   |

Reset

**RMT\_TX\_LIM\_CH $n$**  Configures the maximum entries that channel  $n$  can send out. (R/W)

**RMT\_TX\_LOOP\_NUM\_CH $n$**  Configures the maximum loop count when Continuous TX mode is valid.  
(R/W)

**RMT\_TX\_LOOP\_CNT\_EN\_CH $n$**  Configures whether to enable loop count.  
0: No effect  
1: Enable  
(R/W)

**RMT\_LOOP\_COUNT\_RESET\_CH $n$**  Configures whether to reset the loop count when continuous TX mode is enabled.  
0: No effect  
1: Reset  
(WT)

**RMT\_LOOP\_STOP\_EN\_CH $n$**  Configures whether to enable the loop send stop function after the loop counter counts to loop number for channel  $n$ .  
0: No effect  
1: Enable  
(R/W)

## Register 52.17. RMT\_TX\_SIM\_REG (0x00C4)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |   |   |   |   |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|---|---|---|---|
| (reserved)  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | RMT_TX_SIM_EN<br>RMT_TX_SIM_CH3<br>RMT_TX_SIM_CH2<br>RMT_TX_SIM_CH1<br>RMT_TX_SIM_CH0 |   |   |   |   |   |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 5   | 4 | 3 | 2 | 1 | 0 |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0   | 0 | 0 | 0 | 0 |   |
|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset   |   |   |   |   |   |

**RMT\_TX\_SIM\_CH $n$**  ( $n$ : 0-3) Configures whether to enable channel  $n$  to start sending data synchronously with other enabled channels.

0: No effect

1: Enable

(R/W)

**RMT\_TX\_SIM\_EN** Configures whether to enable multiple of channels to start sending data synchronously.

0: No effect

1: Enable

(R/W)

Register 52.18. RMT\_CH $m$ \_RX\_LIM\_REG ( $m$ : 4-7) (0x00B0, 0x00B4, 0x00B8, 0x00BC)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        |   |   |      |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------------|---|---|------|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RMT_CH $m$ _RX_LIM_REG |   |   |      |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                        | 9 | 8 |      |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                      | 0 | 0 | 0x80 |  |  | 0 |

Reset

**RMT\_CH $m$ \_RX\_LIM\_REG** Configures the maximum entries that channel  $m$  can receive. (R/W)

## Register 52.19. RMT\_DATE\_REG (0x00CC)

|            |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |           |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |
|------------|--|--|--|----|--|--|--|----|--|--|--|---|--|--|--|-----------|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|-------|--|--|--|
| (reserved) |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  | RMT_DATE  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |       |  |  |  |
| 31         |  |  |  | 28 |  |  |  | 27 |  |  |  |   |  |  |  |           |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |       |  |  |  |
| 0          |  |  |  | 0  |  |  |  | 0  |  |  |  | 0 |  |  |  | 0x2201111 |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  | Reset |  |  |  |

**RMT\_DATE** Version control register. (R/W)

## Chapter 53

### Parallel IO Controller (PARLIO)

#### 53.1 Introduction

ESP32-P4 contains a Parallel IO controller (PARLIO) capable of transferring data between external devices and internal memory on a parallel bus through General Direct Memory Access (GDMA). The PARLIO consists of a TX unit and an RX unit, serving as a transmitter and a receiver respectively. With the two units combined, PARLIO achieves full-duplex communication.

Due to its flexibility, PARLIO can function as a general interface to connect various peripherals. For example, with SPI as the master device and PARLIO as the slave device, a peer-to-peer transfer can be achieved. For detailed application examples, refer to Section [53.8](#).

#### 53.2 Glossary

This section covers terminology used to describe the functionality of PARLIO.

|                           |   |
|---------------------------|---|
| <b>RX unit</b>            | Module in PARLIO responsible for receiving data from the external parallel bus and storing them into internal memory.   |
| <b>TX unit</b>            | Module in PARLIO responsible for transmitting data from internal memory to external parallel bus.   |
| <b>RXD</b>                | Parallel data received from the IO interface of the RX unit.  |
| <b>TXD</b>                | Parallel data sent from the IO interface of the TX unit.  |
| <b>Frame</b>              | Transferred data unit from the moment the START signal is set to the moment the End of Frame (EOF) signal is received.  |
| <b>Free-running clock</b> | Clock that toggles continuously as opposed to clock that only toggles when valid data is incoming, and remains constant for the rest of the time.   |
| <b>GDMA SUC EOF</b>       | Signal that indicates GDMA successful end of frame. When GDMA receives this signal, a GDMA interrupt will be triggered, indicating that the current frame is correct and the receive is finished. |
| <b>GDMA ERR EOF</b>       | Signal that indicates GDMA error end of frame. When GDMA receives this signal, a GDMA interrupt will be triggered, indicating that the current frame has error and the receive is finished.       |
| <b>CDC</b>                | Clock domain crossing.  |

#### 53.3 Features

The PARLIO module has the following main features:

- Various clock sources:
  - Including external IO clock PAD\_CLK\_TX/RX and internal system clock XTAL\_CLK, PLL\_F160M\_CLK, and RC\_FAST\_CLK
  - Maximum IO clock frequency of 40 MHz
  - Integer and fractional clock frequency division
- 1/2/4/8/16-bit configurable data bus width
- Full-duplex communication with 16-bit data bus width
- Bit reversal when data bus width is 1/2/4-bit
- RX unit for receiving IO parallel data, which supports:
  - Output clock gating
  - RX unit input and output clock inverse
  - Various receive modes
  - Configurable GDMA SUC EOF generation
  - Configurable IO pin of external enable signal
- TX unit for sending IO parallel data, which supports:
  - Output clock gating
  - TX unit input and output clock inverse
  - Configurable TX EOF generation
  - Valid signal output
  - Configurable bus idle value



## 53.4 Architectural Overview

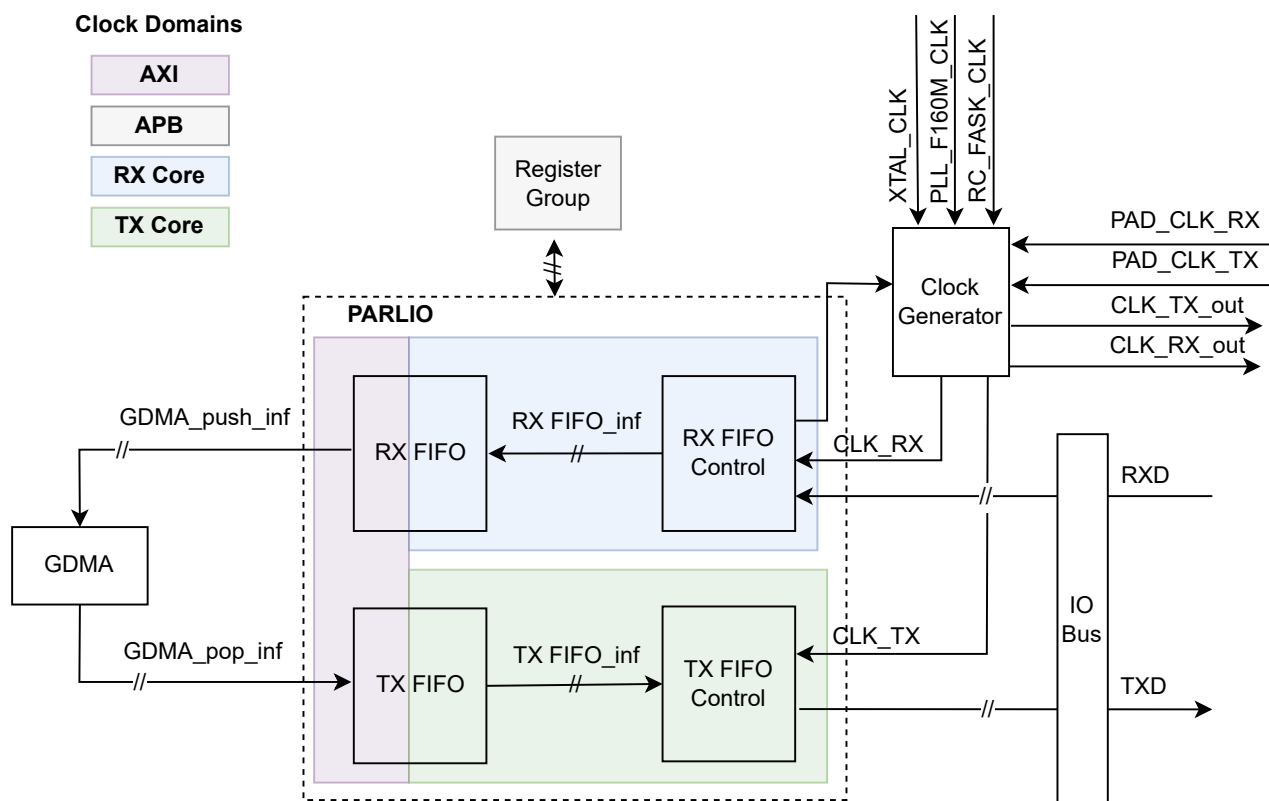


Figure 53.4-1. PARLIO Architecture

Figure 53.4-1 shows the architecture of PARLIO. In addition to the RX unit and the TX unit, a group of status configuration registers is also included.

The RX unit synchronizes RXD to the AXI clock domain through an asynchronous FIFO interface, converts RXD to standard GDMA interface data, and sends it to the internal memory.

The TX unit fetches data from internal memory through GDMA, synchronizes the data to the TX Core clock domain through an asynchronous FIFO interface, and converts the data to TXD for parallel IO bus output.

## 53.5 Functional Description

### 53.5.1 Clock Generator

There are four input clock domains in PARLIO, namely, RX Core, TX Core, AXI, and APB, as shown in Figure 53.4-1.

The status configuration register group works in the APB clock domain.

The GDMA interface logic works in the AXI clock domain.

The RX Core clock domain has four clock sources for selection, i.e., the internal system clock source XTAL\_CLK, RC\_FAST\_CLK, PLL\_F160M\_CLK, and the external clock source (PAD\_CLK\_RX), as shown in Figure 53.5-1. Clock sources can be selected by configuring `HP_SYS_CLKRST_PARLIO_RX_CLK_SRC_SEL`.

The clock can be divided by configuring `HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_NUM`, `HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_DENOMINATOR`, and `HP_SYS_CLKRST_PARLIO_RX_CLK_DIV_NUMERATOR`. The clock division factor can be configured up to  $(2^8 - 1)$ .

The TX Core clock domain has four clock sources for selection, i.e., the internal system clock sources `XTAL_CLK`, `RC_FAST_CLK`, `PLL_F160M_CLK` and the external clock source (`PAD_CLK_TX`), as shown in Figure 53.5-1. Clock sources can be selected by configuring `HP_SYS_CLKRST_PARLIO_TX_CLK_SRC_SEL`. The clock can be divided by configuring `HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_NUM`, `HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_DENOMINATOR`, and `HP_SYS_CLKRST_PARLIO_TX_CLK_DIV_NUMERATOR`. The clock division factor can be configured up to  $(2^8 - 1)$ .

The input clock of the TX and RX units can be inverted. The operating clock of the TX and RX units can also be inverted before being output to IO. The TX and RX units also support clock gating of the output clock.

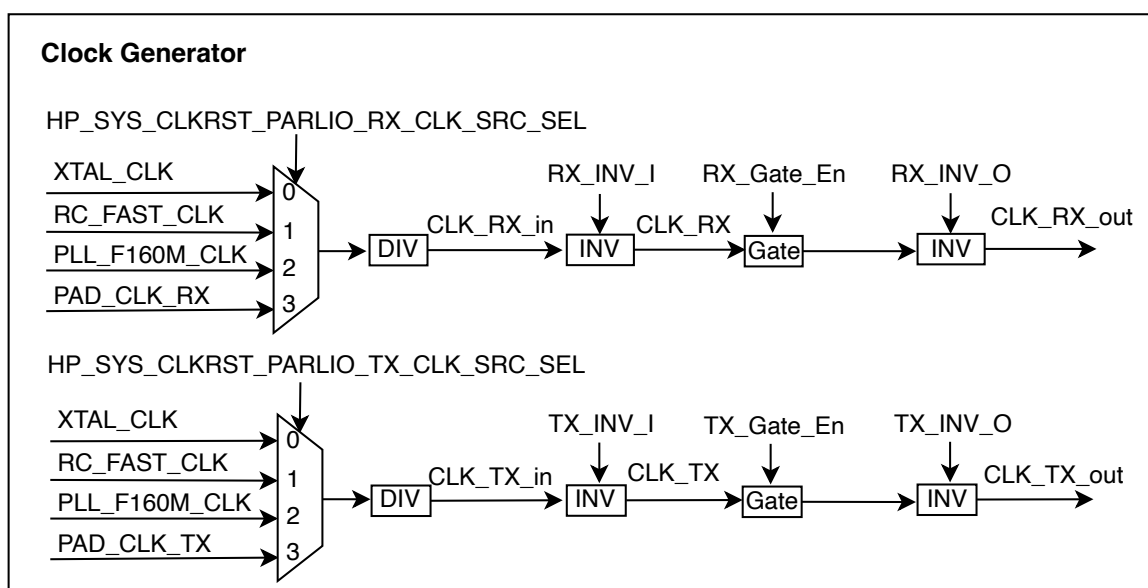


Figure 53.5-1. PARLIO Clock Generation

## 53.5.2 Clock & Reset Restriction

Due to the versatility of PARLIO, the PAD clocks (`PAD_CLK_TX/RX`) of PARLIO may come from different masters (external devices or internal clock sources). These clocks might be either free-running clock or not. If the clock is not free-running, some internal control signals of PARLIO cannot process CDC, so there are certain restrictions during the operation.

1. During the reset of the asynchronous FIFO, it takes two clock cycles to synchronize within AXI clock domain and Core clock domain. Therefore, if the reset of AXI clock domain is performed with a clock that is not free-running, the reset synchronization must be performed two clock cycles in advance. The specific operation is shown in the table below.

Table 53.5-1. Operations to Reset AXI Clock Domain with Clock Restrictions

| Clock Restriction      |                        | Specific Operation   |
|------------------------|------------------------|--|
| The Current Frame      | The Next Frame         |  |
| Free-running clock     | Not free-running clock | Users can reset the next frame transfer before switching to the clock that is not free-running. After the reset is completed, users can switch the clock.                      |
| Not free-running clock | Free-running clock     | The next frame can be reset freely. Users only need to ensure that there is an interval of two clock cycles between the reset and the start of the transfer.                   |
| Not free-running clock | Not free-running clock | If the next frame transfer needs to be reset, users need to first switch to the internal free-running clock, and then switch to the actual clock after the reset is completed. |

2. Due to the restrictions caused by a clock that is not free-running, [PARL\\_IO\\_RX\\_START](#) and [PARL\\_IO\\_TX\\_START](#) cannot perform CDC processing. Therefore, it is necessary to wait until [PARL\\_IO\\_RX\\_START](#) and [PARL\\_IO\\_TX\\_START](#) are stable before starting the data transfer. Otherwise, the transfer might enter a metastable state.

Here are the specific operation steps for the RX unit:

- Clear [HP\\_SYS\\_CLKRST\\_PARLIO\\_RX\\_CLK\\_EN](#) to turn off RX Core clock domain;
- Write 1 to [PARL\\_IO\\_RX\\_START](#);
- Set [HP\\_SYS\\_CLKRST\\_PARLIO\\_RX\\_CLK\\_EN](#) to turn on RX Core clock domain;
- Operate the external device to start sending data;
- Clear [HP\\_SYS\\_CLKRST\\_PARLIO\\_RX\\_CLK\\_EN](#) to turn off RX Core clock domain;
- Write 0 to [PARL\\_IO\\_RX\\_START](#).

Here are the specific operation steps for the TX unit:

- Clear [HP\\_SYS\\_CLKRST\\_PARLIO\\_TX\\_CLK\\_EN](#) to turn off TX Core clock domain;
- Write 1 to [PARL\\_IO\\_TX\\_START](#);
- Set [HP\\_SYS\\_CLKRST\\_PARLIO\\_TX\\_CLK\\_EN](#) to turn on TX Core clock domain;
- Operate the external device to start receiving data;
- Clear [HP\\_SYS\\_CLKRST\\_PARLIO\\_TX\\_CLK\\_EN](#) to turn off TX Core clock domain;
- Write 0 to [PARL\\_IO\\_TX\\_START](#).

3. Reset should follow the requirements below:

- The clock reset during the chip start-up should follow the sequence below:
  - (a) Reset APB clock domain;
  - (b) Reset GDMA clock domain;
  - (c) Reset Core clock domain.
- Inter-frame transfer requires Core clock domain reset and async FIFO reset.

### 53.5.3 Master-Slave Mode

The TX and RX units can function as both master and slave.

When the TX unit serves as master, it is necessary to set the internal free-running clock as the clock source. The TX unit drives TXD on the rising edge of the clock.

When the TX unit functions as a slave device, there are three scenarios, as shown in the table below.

Table 53.5-2. Requirements for TX Unit Operating as Slave with Clock Restrictions

| Clock Restriction      |                                      | Requirement   |
|------------------------|--------------------------------------|---|
| Clock Sent by Master   | Clock Waveform                       |   |
| Free-running clock     | Any waveform                         | There is no requirement for the sampling edge of the master clock.  |
| Not free-running clock | Positive waveform<br>(Figure 53.5-2) | The master clock should sample TXD at the falling edge.   |
| Not free-running clock | Negative waveform<br>(Figure 53.5-3) | The master device should invert the original clock and convert it to the waveform as Figure 53.5-2 shows before output. |

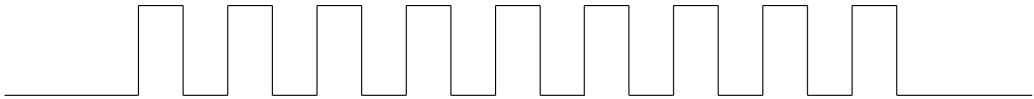


Figure 53.5-2. Positive Waveform

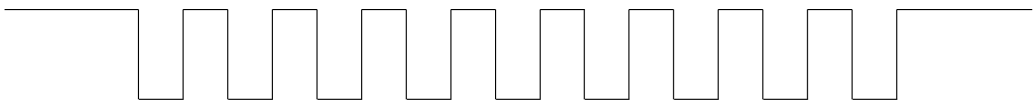


Figure 53.5-3. Negative Waveform

When the RX unit serves as the master, it is required to set the clock source as the internal free-running clock. The RX unit drives RXD on the rising edge of the clock.

When the RX unit functions as the slave, there are three scenarios, as shown in the table below.

Table 53.5-3. Requirements for RX Unit Operating as Slave with Clock Restrictions

| Clock Restriction      |                                   | Requirement  |
|------------------------|-----------------------------------|--|
| Clock Sent by Master   | Clock Waveform                    |  |
| Free-running clock     | Any waveform                      | There is no requirement for the sampling edge of the master clock, and the valid data is subject to the external enable signal.  |
| Not free-running clock | Positive waveform (Figure 53.5-2) | It is required for the master device to drive the data at the rising edge and the RX unit to sample the data at the falling edge (i.e., to inverse the master clock).      |
| Not free-running clock | Negative waveform (Figure 53.5-3) | It is required for the master device to drive the data at the falling edge and the RX unit to sample the data at the rising edge (i.e., to use the original master clock). |

### 53.5.4 Receive Modes of the RX Unit

PARLIO supports eight receive modes, which can be divided into three major categories according to the enable signal:

- Level Enable mode: data received is enabled by the external signal level;
- Pulse Enable mode: data received is enabled by the external signal pulse;
- Software Enable mode: the enable signal of data received can be configured by users directly.

The RX unit also supports inverse of the external enable signal. If the external enable signal is active-low, users can enable the function by setting `PARL_IO_RX_EXT_EN_INV` to switch to the corresponding receive mode introduced as follows.

#### 53.5.4.1 Level Enable Mode

Figure 53.5-4 shows the Level Enable mode. In this mode, an active level on the external enable signal must be aligned with valid data. Since the external level enable signal occupies one IO pin, there are at most 15 IO pins left usable for RXD.

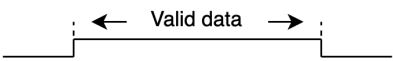
| Mode                | Sub-mode | Description  |
|---------------------|----------|--|
| <b>LEVEL_ENABLE</b> | \        | <b>signal level high</b>   |
|                     |          |  |

Figure 53.5-4. Level Enable Mode for RX Unit

#### 53.5.4.2 Pulse Enable Mode

Pulse Enable mode can be divided into six sub-modes depending on the pulse active level and its alignment with valid data. For detailed classification, see Figure 53.5-5.

Sub-modes 1 ~ 4 all contain start pulse and end pulse. The difference lies in whether start pulse and end pulse are aligned with valid data.

Sub-modes 5 ~ 6 only contain start pulse and the end of valid data is signaled by configuring `PARL_IO_RX_BITLEN`.

Since the external pulse enable signal occupies one IO pin, there are at most 15 IO pins left usable for RXD. However, in sub-mode 5 and sub-mode 6, as the data is considered valid after the pulse's first edge and before the pulse's last edge, the enable signal IO pin can serve as a data IO pin at the same time. Therefore, there are 16 IO pins usable for RXD in these two sub-modes.

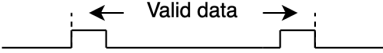
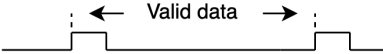
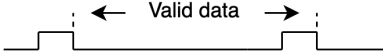
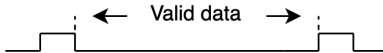
| Mode                | Sub-mode  | Description  |
|---------------------|-----------|--|
| <b>PULSE_ENABLE</b> | sub-mode1 | <b><i>pulse start(data bit include) &amp;&amp; pulse end(data bit include)</i></b> |
|                     |           |  |
|                     | sub-mode2 | <b><i>pulse start(data bit include) &amp;&amp; pulse end(data bit exclude)</i></b> |
|                     |           |  |
|                     | sub-mode3 | <b><i>pulse start(data bit exclude) &amp;&amp; pulse end(data bit include)</i></b> |
|                     |           |  |
|                     | sub-mode4 | <b><i>pulse start(data bit exclude) &amp;&amp; pulse end(data bit exclude)</i></b> |
|                     |           |  |
|                     | sub-mode5 | <b><i>pulse start(data bit include) &amp;&amp; length end</i></b>                  |
|                     | sub-mode6 | <b><i>pulse start(data bit exclude) &amp;&amp; length end</i></b>                  |

Figure 53.5-5. Sub-Modes of Pulse Enable Mode for RX Unit

#### 53.5.4.3 Software Enable Mode

The enable signal in Software Enable mode is determined by the internal configuration register. If users switch to this mode, the receive will only be activated when both `PARL_IO_RX_SW_EN` and `PARL_IO_RX_START` are set to 1.

Since the enable signal does not occupy IO pins on the interface, there are at most 16 IO pins usable by the RXD. Due to the differences of clock domains, the enable signal cannot be aligned with valid data. Thus, the validity of data needs to be identified by the valid clock edge. In this case, the RX Core clock needs to be aligned with valid data.

| Mode             | Sub-mode | Description  |
|------------------|----------|--|
| <b>SW_ENABLE</b> | /        | /  |
|                  |          |  |

Figure 53.5-6. Software Enable Mode for RX Unit

### 53.5.5 RX Unit GDMA SUC EOF Generation

The RX unit generates a GDMA SUC EOF signal to indicate the end of current frame transfer and sends it to the GDMA interface. GDMA SUC EOF can be generated by an external enable signal or triggered by the internally configured bit length.

- When GDMA SUC EOF is generated by the internally configured bit length, there is no restriction on the receive mode selection. However, [PARL\\_IO\\_RX\\_BITLEN](#) must be configured. If the configured value of [PARL\\_IO\\_RX\\_BITLEN](#) is less than the actual received data, the GDMA SUC EOF will be triggered in advance. In this case, the RX unit stops reading data from the FIFO, but the FIFO continues to receive external data until an [RX\\_FIFO\\_WOVF\\_INT](#) interrupt is triggered.
- When GDMA SUC EOF is generated by the external enable signal, only sub-modes 1 and 3 of Pulse Enable mode can be selected. In this mode, the transfer is not affected by the value of [PARL\\_IO\\_RX\\_BITLEN](#), and the transferred data length of the frame is not limited.

### 53.5.6 TX Unit EOF Generation

The TX unit generates an EOF signal and triggers the TX\_EOF\_INT interrupt to indicate the end of current frame transfer. The TX EOF signal can be generated by a GDMA-configured EOF signal or triggered by the internally configured bit length.

- When TX EOF is generated by the internally configured bit length, [PARL\\_IO\\_TX\\_BITLEN](#) must be configured. If the configured value of [PARL\\_IO\\_TX\\_BITLEN](#) is less than the actual transmitted data, the TX EOF signal will be triggered in advance.
- When TX EOF is generated by a GDMA-configured EOF signal, the transfer is not affected by the value of [PARL\\_IO\\_TX\\_BITLEN](#), and the transferred data length of the frame is not limited. The transfer does not end until the GDMA-configured EOF signal is received.

### 53.5.7 RX Unit Timeout

The RX unit supports the receive timeout. If the RX FIFO has not been receiving valid data for a long time, the timeout will be triggered. In such case, a GDMA ERR EOF signal will be generated and sent to the GDMA interface to indicate the end of the receiving. Configure [PARL\\_IO\\_RX\\_TIMEOUT\\_THRES](#) to set the timeout threshold.

The timeout function is enabled by default and can be disabled by users. The upper threshold of the configurable timeout is  $(2^{16} - 1)$  cycles of GDMA clock domain, and the lower threshold depends on the relative frequency relationship between GDMA clock domain and RX Core clock domain. It is recommended to set a relatively large value for [PARL\\_IO\\_RX\\_TIMEOUT\\_THRES](#) to avoid undesired GDMA ERR EOF signals.

### 53.5.8 Output Clock Gating of TX Unit

The TX unit supports output clock gating. The clock gating function is disabled by default, and can be enabled by software via setting [PARL\\_IO\\_TX\\_GATING\\_EN](#). The gating signal is fixed as the highest bit of TXD, and when the bit is at high level, the clock signal can be toggled. There are currently two configurable control sources for the highest bit of TXD, i.e., the GDMA output data and the valid signal. Write 0 to [PARL\\_IO\\_TX\\_VALID\\_OUTPUT\\_EN](#) to select the GDMA output data as the control source. In this case, it is

required to configure the bit width of the TX unit to a maximum. Write 1 to [PARL\\_IO\\_TX\\_VALID\\_OUTPUT\\_EN](#) to select the valid signal as the control source. In this case, there is no limit to the bit width.

When the gating function is enabled, there are at most 15 IO pins left usable for TXD as the gating signal occupies one IO.

### 53.5.9 Valid Signal Output of TX Unit

The TX unit can generate a valid signal aligned with TXD. Configure [PARL\\_IO\\_TX\\_VALID\\_OUTPUT\\_EN](#) to choose whether to output it to TXD. The polarity of the valid signal is fixed to active high.

The valid output function is disabled by default. When enabled, the output valid signal occupies the most significant bit (MSB) of the TXD, which means that no matter what the original value is, the 15th bit of TXD remains high and is output as the valid signal. However, the valid signal pin does not affect the bus width configuration. For example, if the data bus width is 1 bit, the valid output function can still be enabled with a fixed pin as TXD[15] while the data pin is TXD[0].

**Note:**

When the valid signal output function and the clock gating function are enabled at the same time, the highest bit of TXD (i.e., the gating signal) is continuously at high level. In cases where software requires the bit not to continuously stay at high level, do not enable the two functions simultaneously.

### 53.5.10 Bus Idle Value of TX Unit

The TX unit is regarded as in idle state when it is not transmitting data. It supports a configurable bus idle value.

The bus idle value is 0x0 by default, and its maximum configurable value is 0xFF. Note that the configured idle value should not conflict with other enabled functions. For example, when the MSB of TXD is used as the valid signal, users should avoid configuring the MSB of the idle value as 1.

### 53.5.11 Data Transfer in a Single Frame

The RX unit and the TX unit transfer data in the unit of bits, i.e., a single frame transfers 1 bit of data at least.

When the RX unit generates GDMA EOF signals through bit length, the maximum length of the single-frame transmission is  $(2^{19} - 1)$  bits. When the RX unit generates GDMA EOF signals through the enable signal from an external device, there is no limit to the amount of bits of the single-frame transmission.

When the TX unit generates EOF signals through bit length, the maximum length of a single frame transmission is  $(2^{19} - 1)$  bits. When the TX unit generates EOF signals through GDMA-configured EOF signals, there is no limit to the amount of bits of the single-frame transmission.

Since PARLIO transfers data in the unit of bytes on the GDMA side, it will process the IO data when it is not aligned with the bytes.

- When receiving data, PARLIO will automatically pad 0 to the high bits of the data stored in memory via GDMA to make it aligned with bytes.



- When sending data, PARLIO will truncate the data retrieved from memory according to the configured value of `PARL_IO_TX_BITLEN`. Data exceeding the value will not be sent.

When the configured data bus width is 2/4/8/16-bit, the bit length must be configured as a multiple of the corresponding bus width.

### 53.5.12 Bit Reversal in One Byte

The sequence of data within one byte can be reversed when data bus width is 1/2/4-bit. Taking the RX unit as an example, when the configured bus width is 2 bits, the data needs to be packed into one byte before being written into the RX FIFO.

Presume that the original bit sequence is:

{ { b\_0, b\_1 }, { b\_2, b\_3 }, { b\_4, b\_5 }, { b\_6, b\_7 } }

If the bit reversal is enabled, the sequence will be reordered to:

{ { b\_6, b\_7 }, { b\_4, b\_5 }, { b\_2, b\_3 }, { b\_0, b\_1 } }

## 53.6 Interrupts

ESP32-P4's PARLIO module can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- `PARL_IO_TX_INTR`
- `PARL_IO_RX_INTR`

There are several internal interrupt sources from PARLIO that can generate the above interrupt signals. The interrupt sources from PARLIO are listed with their trigger conditions and the resulted interrupt signals in Table 53.6-1.

**Table 53.6-1. PARLIO's Internal Interrupt Sources**

| Internal Interrupt Source      | Trigger Condition   | Interrupt Signal             |
|--------------------------------|---|------------------------------|
| <code>TX_FIFO_EMPTY_INT</code> | TX FIFO is empty, indicating possible error in the data sent by TX    | <code>PARL_IO_TX_INTR</code> |
| <code>RX_FIFO_WOVF_INT</code>  | RX FIFO is full, indicating possible error in the data received by RX | <code>PARL_IO_RX_INTR</code> |
| <code>TX_EOF_INT</code>        | TX finishes sending a complete frame of data                          | <code>PARL_IO_TX_INTR</code> |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section 53.9 [Register Summary](#).

## 53.7 Programming Procedures

### 53.7.1 Data Receiving Operation Process

This section introduces the programming procedure for receiving data through RX unit. To receive parallel data from IO pins that are connected to external devices and store the data in the internal memory, perform the following procedure. For a detailed description of the clock and reset operation restrictions in the RX unit, refer to Section 53.5.2.

1. Reset the RX unit. For specific reset scenarios and sequences, refer to Section 53.5.2.
2. Set [PARL\\_IO\\_RX\\_FIFO\\_WOVF\\_INT\\_CLR](#) and [PARL\\_IO\\_RX\\_FIFO\\_WOVF\\_INT\\_ENA](#).
3. Select the RXD IO pins. If a PAD clock is used, the clock IO pin also needs to be configured.
4. Select the clock source and divide the clock by configuring clock registers.
5. Turn off the clock of RX Core clock domain.
6. Select the receive mode and enable functions required as described in Sections 53.3 and 53.5.
7. Configure GDMA inlink list.
8. Set [PARL\\_IO\\_RX\\_REG\\_UPDATE](#) to synchronize the register signals.
9. Set [PARL\\_IO\\_RX\\_START](#).
10. Turn on the clock of RX Core clock domain.
11. Operate the external device to start sending data.
12. Poll the GDMA SUC EOF interrupt.
13. Clear the GDMA SUC EOF interrupt.
14. Turn off the clock of RX Core clock domain.
15. Clear [PARL\\_IO\\_RX\\_START](#).

### 53.7.2 Data Transmitting Operation Process

This section introduces the programming procedure for transmitting data through TX unit. To transmit parallel data from internal memory to the IO pins that are connected to external devices, perform the following procedure. For detailed description of the clock and reset operation restrictions for the TX unit, refer to Section 53.5.2.

1. Reset the TX unit. For specific reset scenarios and sequences, refer to Section 53.5.2.
2. Set [PARL\\_IO\\_TX\\_FIFO\\_EMPTY\\_INT\\_CLR](#), [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#), [PARL\\_IO\\_TX\\_FIFO\\_EMPTY\\_INT\\_ENA](#), and [PARL\\_IO\\_TX\\_EOF\\_INT\\_ENA](#) in sequence.
3. Select the TXD IO pins. If a PAD clock is used, the clock IO PAD also needs to be configured.
4. Select the clock source and divide the clock by configuring clock registers.
5. Turn off the clock of TX Core clock domain.
6. Select the functions required as described in Section 53.5.

7. Configure GDMA outlink list.
8. Poll the [PARL\\_IO\\_TX\\_READY](#).
9. Set [PARL\\_IO\\_TX\\_START](#).
10. Turn on the clock of TX Core clock domain.
11. Operate the external device to start receiving data.
12. Poll the [PARL\\_IO\\_TX\\_EOF\\_INT\\_ST](#).
13. Set [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#).
14. Turn off the clock of TX Core clock domain.
15. Clear [PARL\\_IO\\_TX\\_START](#).

## 53.8 Application Examples

This section introduces some PARLIO application examples and their detailed operation process. All peripherals used in the examples are from ESP series chips and can work with PARLIO to form a complete data path.

### Note:

The data paths constructed in the examples may not be the optimal. For example, users can use the SPI peripherals on two identical ESP chips to complete the peer-to-peer transfer in real case instead of using PARLIO to work with SPI. However, these examples demonstrate the flexibility of the PARLIO interface to a certain extent.

### 53.8.1 Co-working with SPI

In this example, external SPI sends data as a master device and PARLIO RX unit receives data as a slave device, and at the same time, PARLIO TX sends data as a master device and SPI receives data as a slave device, thus achieving a peer-to-peer serial data transfer.

- Follow the operation process below to achieve SPI transmit and PARLIO receive:
  1. Configure SPI clock.
  2. Configure SPI as the master device.
  3. Configure signal pins. Connect FSPICLK to PAD\_CLK\_RX, FSPICSO to RXD[15], and FSPID to RXD[0].
  4. Write the data sent into the SPI buffer and configure the bit length of the data sent.
  5. Set [SPI\\_UPDATE](#) to update the configured register value.
  6. Reset PARLIO RX unit.
  7. Configure PARLIO RX unit clock.
  8. Turn off the PARLIO RX Core clock domain.
  9. Configure PARLIO receive mode as sub-mode 1 of LEVEL Enable mode. Configure RX unit data bus width as 1 bit. Configure [PARL\\_IO\\_RX\\_BITLEN](#) according to the sending length of SPI. Set [PARL\\_IO\\_RX\\_REG\\_UPDATE](#).

10. Configure PARLIO GDMA inlink list.
  11. Set [PARL\\_IO\\_RX\\_START](#).
  12. Turn on the PARLIO RX Core clock domain.
  13. Set [SPI\\_USR](#) to start transmitting data of SPI.
  14. Poll GDMA SUC EOF interrupt.
  15. Clear [PARL\\_IO\\_RX\\_START](#).
- Follow the operation process below to achieve PARLIO transmit and SPI receive:
    1. Configure SPI clock.
    2. Configure SPI as the slave device.
    3. Configure signal pins. Connect FSPICLK to PAD\_CLK\_TX, FSPICSO to TXD[15], and FSPID to TXD[0].
    4. Set [SPI\\_RD\\_BIT\\_ORDER](#) to invert the bit order.
    5. Set [SPI\\_UPDATE](#) to update the configured register value.
    6. Reset PARLIO TX unit.
    7. Set [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#) and [PARL\\_IO\\_TX\\_EOF\\_INT\\_ENA](#).
    8. Configure PARLIO TX unit clock.
    9. Turn off the clock of TX Core clock domain.
    10. Configure data bus width as 1 bit. Write 1 to [PARL\\_IO\\_TX\\_VALID\\_OUTPUT\\_EN](#). Configure [PARL\\_IO\\_TX\\_BITLEN](#).
    11. Configure GDMA outlink list.
    12. Poll [PARL\\_IO\\_TX\\_READY](#).
    13. Write 1 to [PARL\\_IO\\_TX\\_START](#).
    14. Turn on the clock of TX Core clock domain.
    15. Start data transfer.
    16. Poll [PARL\\_IO\\_TX\\_EOF\\_INT\\_ST](#).
    17. Set [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#).
    18. Turn off the clock of TX Core clock domain.
    19. Clear [PARL\\_IO\\_TX\\_START](#).

## 53.8.2 Co-working with I2S

In this example, external I2S sends data as a master device and PARLIO RX unit receives data as a slave device. PARLIO supports the transmission of the I2S TDM MSB alignment standard and the TDM PCM standard. When the I2S transfer protocol is the TDM MSB alignment standard, it is required to configure the receive mode of PARLIO as Level Enable mode. When the I2S transfer protocol is the TDM PCM standard, it is required to configure the receive mode of PARLIO as the sub-mode 4 of Pulse Enable mode and set [PARL\\_IO\\_RX\\_EXT\\_EN\\_INV](#).

This section takes the TDM PCM alignment standard as an example. The specific operation process is as follows:

1. Configure I2S clock.
2. Configure signal pins. Connect I2SO\_BCK\_out to PAD\_CLK\_RX, I2SO\_WS\_out to RXD[15], and I2SO\_Data\_out to RXD[0].
3. Configure I2S as the master device.
4. Configure the I2S TX data mode and channel mode required. Set [I2S\\_TX\\_UPDATE](#).
5. Reset I2S TX unit and TX FIFO.
6. Enable [I2S\\_TX\\_DONE\\_INT](#).
7. Configure I2S GDMA outlink list.
8. Set [I2S\\_TX\\_STOP\\_EN](#).
9. Reset PARLIO RX unit.
10. Configure PARLIO RX unit clock.
11. Turn off PARLIO RX Core clock domain.
12. Configure PARLIO receive mode as sub-mode 4 of Pulse Enable mode and set [PARL\\_IO\\_RX\\_EXT\\_EN\\_INV](#) to configure the RX unit data bus width as 1 bit. Configure [PARL\\_IO\\_TX\\_BITLEN](#) according to the length of the data sent by I2S. Set [PARL\\_IO\\_RX\\_REG\\_UPDATE](#).
13. Configure PARLIO GDMA inlink list.
14. Set [PARL\\_IO\\_RX\\_START](#).
15. Turn on PARLIO RX Core clock domain.
16. Set [I2S\\_TX\\_START](#) to start transmitting data.
17. Poll [I2S\\_TX\\_DONE\\_INT](#).
18. Poll GDMA SUC EOF interrupt.
19. Clear [I2S\\_TX\\_START](#).
20. Clear [PARL\\_IO\\_RX\\_START](#).

### 53.8.3 Co-working with LCD

In this example, PARLIO TX unit sends data as a master device and external LCD controller receives data as a slave device. The I8080/MOTO6800 format is used. 8-bit parallel data is transferred between devices. The specific operation process is as follows:

1. Configure signal pins. Connect CLK\_TX\_out to LCD pixel clock PCLK, TXD[7:0] to LCD data input pin, TXD[8] to LCD CS pin, TXD[9] to LCD CD pin.
2. Reset PARLIO TX unit.
3. Set [PARL\\_IO\\_TX\\_FIFO\\_EMPTY\\_INT\\_CLR](#), [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#), [PARL\\_IO\\_TX\\_FIFO\\_EMPTY\\_INT\\_ENA](#), and [PARL\\_IO\\_TX\\_EOF\\_INT\\_ENA](#) in sequence.
4. Configure PARLIO TX unit clock.

5. Turn off the clock of TX Core clock domain.
6. Configure data bus width as 16 bit. Configure [PARL\\_IO\\_TX\\_BITLEN](#).
7. Configure GDMA outlink list. Note that the data sent in the linked list should conform to I8080/MOTO6800 format. The lower eight bits are valid parallel data. The 9th and 10th bits are respectively CS, CD. The MSB is the constant 1. The remaining bits are arbitrary values.
8. Poll [PARL\\_IO\\_TX\\_READY](#).
9. Write 1 to [PARL\\_IO\\_TX\\_START](#).
10. Turn on the clock of TX Core clock domain.
11. Start data transfer.
12. Poll [PARL\\_IO\\_TX\\_EOF\\_INT\\_ST](#).
13. Set [PARL\\_IO\\_TX\\_EOF\\_INT\\_CLR](#).
14. Turn off the clock of TX Core clock domain.
15. Clear [PARL\\_IO\\_TX\\_START](#).

## 53.9 Register Summary

The addresses in this section are relative to Parallel IO Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name   | Description   | Address | Access   |
|--|---|---------|----------|
| <b>PARLIO RX Configuration Registers</b>                   |   |         |          |
| <a href="#">PARL_IO_RX_MODE_CFG_REG</a>                    | PARLIO RX sampling mode configuration register        | 0x0000  | R/W      |
| <a href="#">PARL_IO_RX_DATA_CFG_REG</a>                    | PARLIO RX data configuration register                 | 0x0004  | R/W      |
| <a href="#">PARL_IO_RX_GENRL_CFG_REG</a>                   | PARLIO RX general configuration register              | 0x0008  | R/W      |
| <a href="#">PARL_IO_RX_START_CFG_REG</a>                   | PARLIO RX start configuration register                | 0x000C  | R/W      |
| <b>PARLIO TX Configuration Registers</b>                   |   |         |          |
| <a href="#">PARL_IO_TX_DATA_CFG_REG</a>                    | PARLIO TX data configuration register                 | 0x0010  | R/W      |
| <a href="#">PARL_IO_TX_START_CFG_REG</a>                   | PARLIO TX start configuration register                | 0x0014  | R/W      |
| <a href="#">PARL_IO_TX_GENRL_CFG_REG</a>                   | PARLIO TX general configuration register              | 0x0018  | R/W      |
| <b>PARLIO Configuration and Status Registers</b>           |   |         |          |
| <a href="#">PARL_IO_FIFO_CFG_REG</a>                       | PARLIO FIFO configuration register                    | 0x001C  | R/W      |
| <a href="#">PARL_IO_REG_UPDATE_REG</a>                     | PARLIO register update configuration register         | 0x0020  | WT       |
| <a href="#">PARL_IO_ST_REG</a>                             | PARLIO module status register                         | 0x0024  | RO       |
| <b>PARLIO Interrupt Configuration and Status Registers</b> |   |         |          |
| <a href="#">PARL_IO_INT_ENA_REG</a>                        | PARLIO interrupt enable signal configuration register | 0x0028  | R/W      |
| <a href="#">PARL_IO_INT_RAW_REG</a>                        | PARLIO interrupt raw signal status register           | 0x002C  | R/SS/WTC |
| <a href="#">PARL_IO_INT_ST_REG</a>                         | PARLIO interrupt signal status register               | 0x0030  | RO       |
| <a href="#">PARL_IO_INT_CLR_REG</a>                        | PARLIO interrupt clear signal configuration register  | 0x0034  | WT       |
| <b>PARLIO RX/TX Status Registers</b>                       |   |         |          |
| <a href="#">PARL_IO_RX_STO_REG</a>                         | PARLIO RX status register 0                           | 0x0038  | RO       |
| <a href="#">PARL_IO_RX_ST1_REG</a>                         | PARLIO RX status register 1                           | 0x003C  | RO       |
| <a href="#">PARL_IO_TX_STO_REG</a>                         | PARLIO TX status register 0                           | 0x0040  | RO       |
| <b>PARLIO Clock Configuration Registers</b>                |   |         |          |
| <a href="#">PARL_IO_RX_CLK_CFG_REG</a>                     | PARLIO RX clock configuration register                | 0x0044  | R/W      |
| <a href="#">PARL_IO_TX_CLK_CFG_REG</a>                     | PARLIO TX clock configuration register                | 0x0048  | R/W      |
| <a href="#">PARL_IO_CLK_REG</a>                            | PARLIO clock configuration register                   | 0x0120  | R/W      |
| <b>PARLIO Version Register</b>                             |   |         |          |
| <a href="#">PARL_IO_VERSION_REG</a>                        | Version control register                              | 0x03FC  | R/W      |

## 53.10 Registers

The addresses in this section are relative to Parallel IO Controller base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

### Register 53.1. PARL\_IO\_RX\_MODE\_CFG\_REG (0x0000)

[illegible]

**PARL\_IO\_RX\_EXT\_EN\_SEL** Configures the RX external enable signal from IO PAD. (R/W)

**PARL\_IO\_RX\_SW\_EN** Configures whether to enable data sampling by software.

0: Disable

1: Enable

(R/W)

**PARL\_IO\_RX\_EXT\_EN\_INV** Configures whether to invert the external enable signal.

0: No effect

1: Invert

(R/W)

**PARL\_IO\_RX\_PULSE\_SUBMODE\_SEL** Configures the RXD pulse sampling sub-mode.

0: Positive pulse start (data bit included) & Positive pulse end (data bit included)

1: Positive pulse start (data bit included) & Positive pulse end (data bit excluded)

2: Positive pulse start (data bit excluded) & Positive pulse end (data bit included)

3: Positive pulse start (data bit excluded) & Positive pulse end (data bit excluded)

4: Positive pulse start (data bit included) & Length end

5: Positive pulse start (data bit excluded) & Length end

(R/W)

**PARL\_IO\_RX\_SMP\_MODE\_SEL** Configures the RXD sampling mode.

0: External Level Enable mode

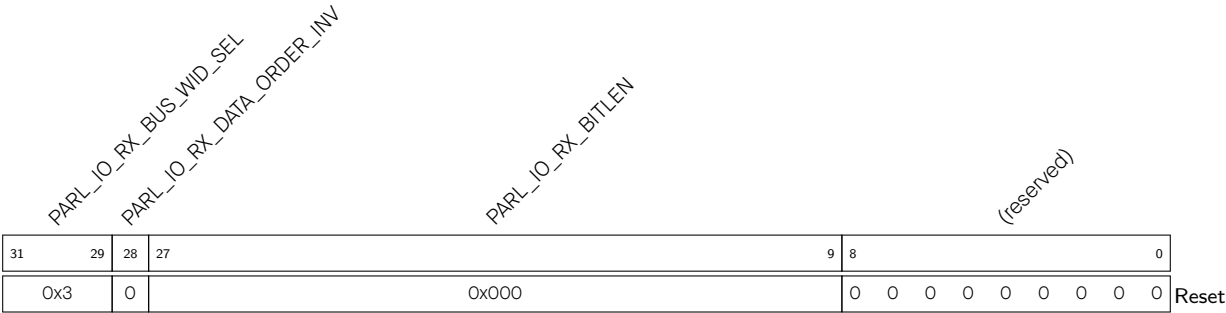
### 1: External Pulse Enable mode

## 2: Internal Software Enable mode

(R/W)



Register 53.2. PARL\_IO\_RX\_DATA\_CFG\_REG (0x0004)



- PARL\_IO\_RX\_BITLEN

Configures the expected bit number of RXD. (R/W)
- PARL\_IO\_RX\_DATA\_ORDER\_INV

Configures whether to invert the bit order of one byte sent from RX FIFO to GDMA. (R/W)
- PARL\_IO\_RX\_BUS\_WID\_SEL

Configures the RXD bus width.

0: 1 bit

1: 2 bits

2: 4 bits

3: 8 bits

4: 16 bits

5 ~ 15: Invalid and will incur error

(R/W)

Register 53.3. PARL\_IO\_RX\_GENRL\_CFG\_REG (0x0008)

|            |    |    |       |                        |  |  |  |  |  |  |   |                          |    |    |   |   |   |   |   |                      |   |   |   |   |   |   |   |            |   |       |  |  |  |  |  |
|------------|----|----|-------|------------------------|--|--|--|--|--|--|---|--------------------------|----|----|---|---|---|---|---|----------------------|---|---|---|---|---|---|---|------------|---|-------|--|--|--|--|--|
| (reserved) |    |    |       | PARL_IO_RX_EOF_GEN_SEL |  |  |  |  |  |  |   | PARL_IO_RX_TIMEOUT_THRES |    |    |   |   |   |   |   | PARL_IO_RX_GATING_EN |   |   |   |   |   |   |   | (reserved) |   |       |  |  |  |  |  |
| 31         | 30 | 29 | 28    |                        |  |  |  |  |  |  |   | 13                       | 12 | 11 |   |   |   |   |   |                      |   |   | 0 |   |   |   |   |            |   |       |  |  |  |  |  |
| 0          | 0  | 1  | 0xfff |                        |  |  |  |  |  |  | 0 | 0                        | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | Reset |  |  |  |  |  |

**PARL\_IO\_RX\_GATING\_EN** Configures whether to enable the clock gating of the RX output clock.

0: Disable

1: Enable

(R/W)

**PARL\_IO\_RX\_TIMEOUT\_THRES** Configures the threshold of the RX timeout counter. (R/W)

**PARL\_IO\_RX\_TIMEOUT\_EN** Configures whether to enable the timeout function to generate GDMA ERR EOF.

0: Disable

1: Enable

(R/W)

**PARL\_IO\_RX\_EOF\_GEN\_SEL** Configures the generation mechanism of GDMA SUC EOF.

0: Generate GDMA SUC EOF by the configured data bit length

1: Generate GDMA SUC EOF by the external enable signal

(R/W)

Register 53.4. PARL\_IO\_RX\_START\_CFG\_REG (0x000C)

|                  |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |       |  |  |  |  |  |  |
|------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|-------|--|--|--|--|--|--|
| PARL_IO_RX_START |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |       |  |  |  |  |  |  |
| 31               | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0          |       |  |  |  |  |  |  |
| 0                | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | Reset |  |  |  |  |  |  |

**PARL\_IO\_RX\_START** Configures whether to start RX data sampling.

0: No effect

1: Start

(R/W)

### Register 53.5. PARL\_IO\_TX\_DATA\_CFG\_REG (0x0010)

|                        |  |                           |  |    |  |       |  |                   |  |                     |  |       |  |
|------------------------|--|---------------------------|--|----|--|-------|--|-------------------|--|---------------------|--|-------|--|
| 31                     |  | 29                        |  | 28 |  | 27    |  | 9                 |  | 8                   |  | 0     |  |
| PARL_IO_TX_BUS_WID_SEL |  | PARL_IO_TX_DATA_ORDER_INV |  |    |  |       |  | PARL_IO_TX_BITLEN |  | (reserved)          |  |       |  |
| 0x3                    |  | 0                         |  |    |  | 0x000 |  |                   |  | 0 0 0 0 0 0 0 0 0 0 |  | Reset |  |

**PARL\_IO\_TX\_BITLEN** Configures the expected bit number of TXD. (R/W)

**PARL\_IO\_TX\_DATA\_ORDER\_INV** Configures whether to invert the bit order of one byte sent from TX FIFO to IO data.

0: No effect

1: Invert

(R/W)

**PARL\_IO\_TX\_BUS\_WID\_SEL** Configures the TXD bus width.

0: 1 bit

1: 2 bits

2: 4 bits

3: 8 bits

4: 16 bits

5 ~ 15: Invalid and will incur error

(R/W)

### Register 53.6. PARL\_IO\_TX\_START\_CFG\_REG (0x0014)

[illegible]

**PARL\_IO\_TX\_START** Configures whether to start TX data transmission.

0: No effect

1: Start

(R/W)

Register 53.7. PARL\_IO\_TX\_GENRL\_CFG\_REG (0x0018)

|  |    |                       |  |  |  |  |  |  |  |  |  |   |    |                                      |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
|--|----|-----------------------|--|--|--|--|--|--|--|--|--|---|----|--------------------------------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|
| PARL_IO_TX_VALID_OUTPUT_EN<br>PARL_IO_TX_GATING_EN |    | PARL_IO_TX_IDLE_VALUE |  |  |  |  |  |  |  |  |  |   |    | PARL_IO_TX_EOF_GEN_SEL<br>(reserved) |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |     |
|  |    |                       |  |  |  |  |  |  |  |  |  |   |    |                                      |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 31   | 30 | 29                    |  |  |  |  |  |  |  |  |  |   | 14 | 13                                   | 12 |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |
| 0  | 0  | 0x00                  |  |  |  |  |  |  |  |  |  | 0 | 0  | 0                                    | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0</ |

Reset

**PARL\_IO\_TX\_EOF\_GEN\_SEL** Configures the generation mechanism of TX EOF.

0: Generate TX EOF by the configured data bit length

1: Generate TX EOF by the GDMA EOF signal.

(R/W)

**PARL\_IO\_TX\_IDLE\_VALUE** Configures the data value on TX bus in idle state. (R/W)**PARL\_IO\_TX\_GATING\_EN** Configures whether to enable the clock gating of the TX output clock.

0: Disable

1: Enable

(R/W)

**PARL\_IO\_TX\_VALID\_OUTPUT\_EN** Configures whether to enable the output of TX data valid signal.

0: Disable

1: Enable

(R/W)

Register 53.8. PARL\_IO\_FIFO\_CFG\_REG (0x001C)

|                      |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|----------------------|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PARL_IO_RX_FIFO_SRST |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| PARL_IO_TX_FIFO_SRST |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                   | 30 | 29         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                    | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Reset

**PARL\_IO\_TX\_FIFO\_SRST** Configures whether to reset async FIFO in the TX unit.

0: No effect

1: Reset

(R/W)

**PARL\_IO\_RX\_FIFO\_SRST** Configures whether to reset async FIFO in the RX unit.

0: No effect

1: Reset

(R/W)

## Register 53.9. PARL\_IO\_REG\_UPDATE\_REG (0x0020)

PARL\_IO\_RX\_REG\_UPDATE

(reserved)

|    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| 31 | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |       |
| 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PARL\_IO\_RX\_REG\_UPDATE** Configures whether to update RX register configuration.

0: No effect

1: Update

(WT)

## Register 53.10. PARL\_IO\_ST\_REG (0x0024)

PARL\_IO\_TX\_READY

(reserved)

|    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| 31 | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |       |
| 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PARL\_IO\_TX\_READY** Represents whether TX is ready to transmit data.

0: Not ready

1: Ready

(RO)

## Register 53.11. PARL\_IO\_INT\_ENA\_REG (0x0028)

(reserved)

 PARL\_IO\_TX\_EOF\_INT\_ENA  
 PARL\_IO\_RX\_FIFO\_WOVF\_INT\_ENA  
 PARL\_IO\_TX\_FIFO\_EMPTY\_INT\_ENA

|    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| 31 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

**PARL\_IO\_TX\_FIFO\_EMPTY\_INT\_ENA** Write 1 to enable [TX\\_FIFO\\_EMPTY\\_INT](#). (R/W)**PARL\_IO\_RX\_FIFO\_WOVF\_INT\_ENA** Write 1 to enable [RX\\_FIFO\\_WOVF\\_INT](#). (R/W)**PARL\_IO\_TX\_EOF\_INT\_ENA** Write 1 to enable [TX\\_EOF\\_INT](#). (R/W)

## Register 53.12. PARL\_IO\_INT\_RAW\_REG (0x002C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PARL_IO_TX_EOF_INT_RAW<br>PARL_IO_RX_FIFO_WOVF_INT_RAW<br>PARL_IO_TX_FIFO_EMPTY_INT_RAW |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3   | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0   | 0 | 0 | Reset |

**PARL\_IO\_TX\_FIFO\_EMPTY\_INT\_RAW** The raw interrupt status of [TX\\_FIFO\\_EMPTY\\_INT](#). (R/WTC/SS)

**PARL\_IO\_RX\_FIFO\_WOVF\_INT\_RAW** The raw interrupt status of [RX\\_FIFO\\_WOVF\\_INT](#). (R/WTC/SS)

**PARL\_IO\_TX\_EOF\_INT\_RAW** The raw interrupt status of [TX\\_EOF\\_INT](#). (R/WTC/SS)

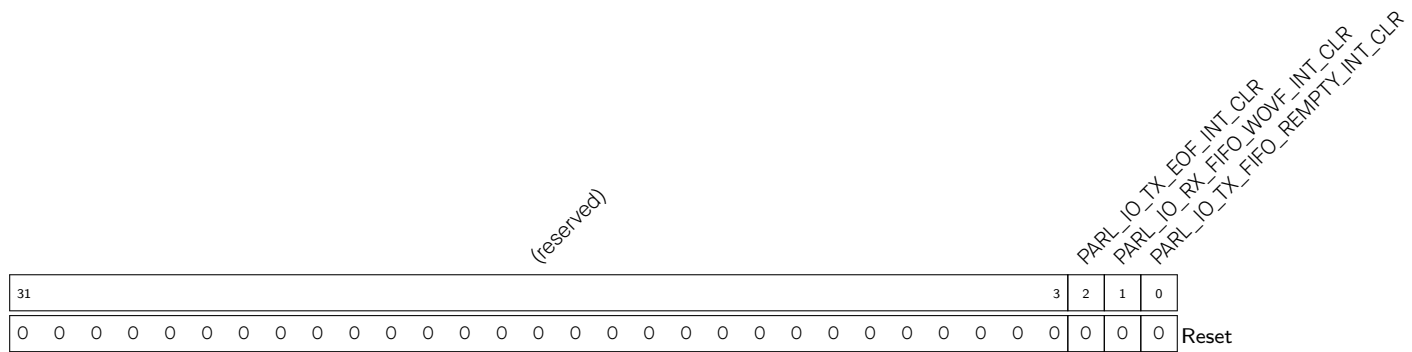
## Register 53.13. PARL\_IO\_INT\_ST\_REG (0x0030)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PARL_IO_TX_EOF_INT_ST<br>PARL_IO_RX_FIFO_WOVF_INT_ST<br>PARL_IO_TX_FIFO_EMPTY_INT_ST |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 3  | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | Reset |

**PARL\_IO\_TX\_FIFO\_EMPTY\_INT\_ST** The masked interrupt status of [TX\\_FIFO\\_EMPTY\\_INT](#). (RO)

**PARL\_IO\_RX\_FIFO\_WOVF\_INT\_ST** The masked interrupt status of [RX\\_FIFO\\_WOVF\\_INT](#). (RO)

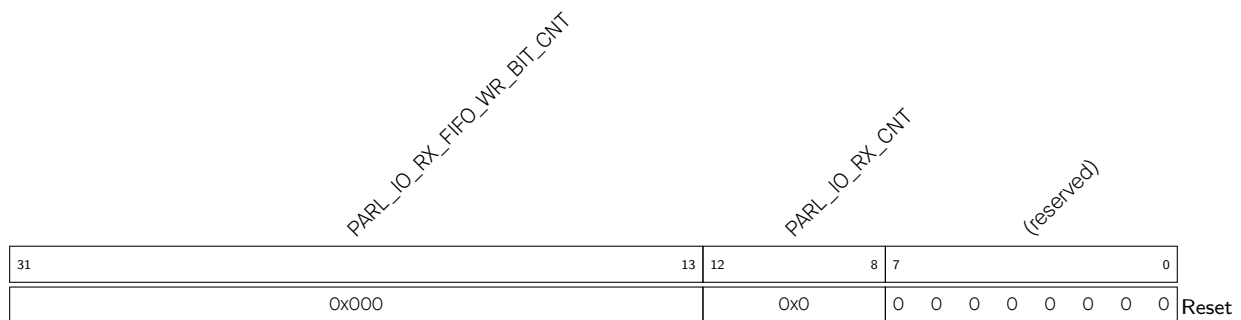
**PARL\_IO\_TX\_EOF\_INT\_ST** The masked interrupt status of [TX\\_EOF\\_INT](#). (RO)

**Register 53.14. PARL\_IO\_INT\_CLR\_REG (0x0034)**

**PARL\_IO\_TX\_FIFO\_EMPTY\_INT\_CLR** Write 1 to clear [TX\\_FIFO\\_EMPTY\\_INT](#). (WT)

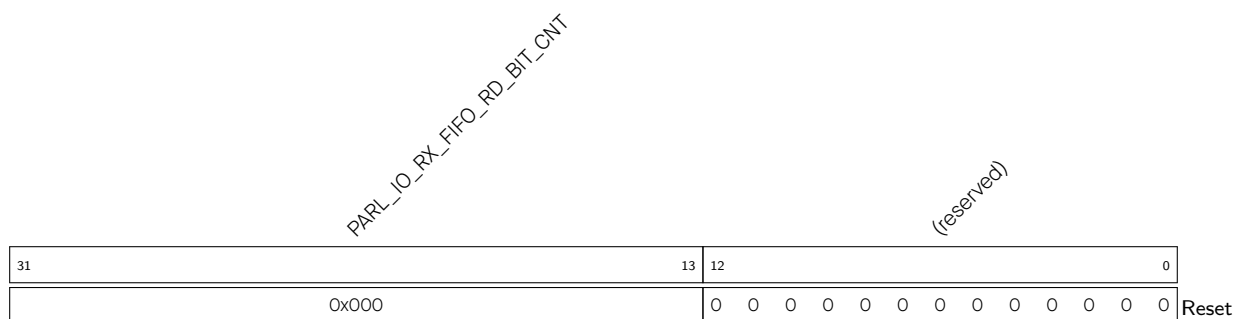
**PARL\_IO\_RX\_FIFO\_WOVF\_INT\_CLR** Write 1 to clear [RX\\_FIFO\\_WOVF\\_INT](#). (WT)

**PARL\_IO\_TX\_EOF\_INT\_CLR** Write 1 to clear [TX\\_EOF\\_INT](#). (WT)

**Register 53.15. PARL\_IO\_RX\_STO\_REG (0x0038)**

**PARL\_IO\_RX\_CNT** Represents the clock cycle number of reading the RX FIFO. (RO)

**PARL\_IO\_RX\_FIFO\_WR\_BIT\_CNT** Represents the bit number currently written into the RX FIFO. (RO)

**Register 53.16. PARL\_IO\_RX\_ST1\_REG (0x003C)**

**PARL\_IO\_RX\_FIFO\_RD\_BIT\_CNT** Represents the bit number currently read from the RX FIFO. (RO)

Register 53.17. PARL\_IO\_TX\_STO\_REG (0x0040)

|                            |  |  |  |  |  |  |  |  |  |            |  |  |    |  |  |     |  |  |   |  |  |   |  |  |   |  |  |   |  |  |       |  |  |
|----------------------------|--|--|--|--|--|--|--|--|--|------------|--|--|----|--|--|-----|--|--|---|--|--|---|--|--|---|--|--|---|--|--|-------|--|--|
| PARL_IO_TX_FIFO_RD_BIT_CNT |  |  |  |  |  |  |  |  |  |            |  |  |    |  |  |     |  |  |   |  |  |   |  |  |   |  |  |   |  |  |       |  |  |
| PARL_IO_TX_CNT             |  |  |  |  |  |  |  |  |  | (reserved) |  |  |    |  |  |     |  |  |   |  |  |   |  |  |   |  |  |   |  |  |       |  |  |
| 31                         |  |  |  |  |  |  |  |  |  |            |  |  | 13 |  |  | 12  |  |  | 6 |  |  | 5 |  |  | 0 |  |  |   |  |  |       |  |  |
| 0x000                      |  |  |  |  |  |  |  |  |  |            |  |  |    |  |  | 0x0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | 0 |  |  | Reset |  |  |

**PARL\_IO\_TX\_CNT** Represents the cycle number of reading the TX FIFO. (RO)

**PARL\_IO\_TX\_FIFO\_RD\_BIT\_CNT** Represents the bit number currently read from the TX FIFO. (RO)

Register 53.18. PARL\_IO\_RX\_CLK\_CFG\_REG (0x0044)

|                      |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|----------------------|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| PARL_IO_RX_CLK_O_INV |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| PARL_IO_RX_CLK_I_INV |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| (reserved)           |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31                   | 30 | 29 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |       |
| 0                    | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**PARL\_IO\_RX\_CLK\_I\_INV** Configures whether to invert the RX input Core clock.

0: No effect

1: Invert

(R/W)

**PARL\_IO\_RX\_CLK\_O\_INV** Configures whether to invert the RX output Core clock.

0: No effect

1: Invert

(R/W)



## Register 53.19. PARL\_IO\_TX\_CLK\_CFG\_REG (0x0048)

|                      |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| PARL_IO_TX_CLK_O_INV |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | PARL_IO_TX_CLK_I_INV |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31                   | 30 | 29 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0                    | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PARL\_IO\_TX\_CLK\_I\_INV** Configures whether to invert the TX input Core clock.

0: No effect

1: Invert

(R/W)

**PARL\_IO\_TX\_CLK\_O\_INV** Configures whether to invert the TX output Core clock.

0: No effect

1: Invert

(R/W)

## Register 53.20. PARL\_IO\_CLK\_REG (0x0120)

|                |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |
|----------------|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|---|
| PARL_IO_CLK_EN |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | 0 |
| 31             | 30 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |   |
| 0              | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |   |

**PARL\_IO\_CLK\_EN** Register clock gating.

0: Enable the register clock only when reading or writing registers

1: Always enable the register clock

(R/W)

## Register 53.21. PARL\_IO\_VERSION\_REG (0x03FC)

|            |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|----|--|--|--|----|--|--|--|---|--|--|--|-----------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |    |  |  |  |    |  |  |  |   |  |  |  |           |  |  |  |  |  |  |  |  |  |  |  |  |  |  | PARL_IO_DATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  | 28 |  |  |  | 27 |  |  |  | 0 |  |  |  |           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  | 0  |  |  |  | 0  |  |  |  | 0 |  |  |  | 0x2212260 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**PARL\_IO\_DATE** Version control register. (R/W)

## Chapter 54

### BitScrambler

The ESP32-P4 has an extensive amount of DMA-capable peripherals. These can move data from memory to an external device, and vice versa, without any interference from the CPU. This only works if the external device needs or emits the data in question in the same format as the software expects it: if not, the CPU needs to rewrite the format of the data. Examples include a need to swap bytes, reverse bytes, and shift the data left or right.

As bitwise operations tend to be fairly CPU-expensive and the purpose of DMA is to not use the CPU in the transfer, ESP32-P4 includes two BitScramblers, which are dedicated peripherals to change the format of data in between memory and the peripheral. A BitScrambler is capable of performing the aforementioned operations, but as a flexible programmable state machine, it is capable of more advanced things as well. One of the two BitScramblers is dedicated to memory-to-peripheral (or memory-to-memory) transfers, the other one is dedicated to peripheral-to-memory transfers.

#### 54.1 Introduction

In ESP32-P4, a DMA-capable peripheral is one that can read data directly from memory and/or write data directly to memory using a DMA channel. The format this data is read/written in is dependent on the peripheral and generally has only a small amount of flexibility. For most DMA-capable peripherals in ESP32-P4, it is possible to attach a BitScrambler to any of these paths for additional flexibility.

When a BitScrambler is attached to a peripheral, it gets the chance to modify any data that flows down a DMA channel associated with that peripheral. Data written to the DMA channel will appear on the BitScrambler input, and what the BitScrambler writes to its output will flow down the DMA channel. The BitScrambler contains instruction memory where instructions on how to route the data between input and output can be stored. As such, by writing an appropriate BitScrambler program, the way the data is rewritten by the BitScrambler can be controlled.

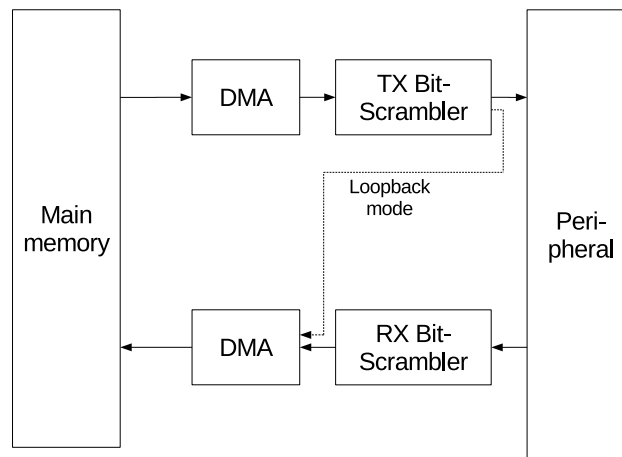


Figure 54.1-1. BitScrambler System Context Diagram

## 54.2 Feature List

The BitScrambler has the following features:

- Two BitScramblers, one for RX (peripheral-to-memory), one for TX (memory-to-peripheral)
- Support for memory-to-memory transfers
- Processing up to 32 bits per DMA clock period
- Data path controlled by a BitScrambler program stored in instruction memory
- Input registers able to read 0, 8, 16, or 32 bits per clock cycle
- Output registers:
  - Able to write 0, 8, 16, or 32 bits per clock cycle
  - Data sources for output register bits: 64 bits of input data, two counters, LUT RAM data, data output of last cycle, comparators
  - With some restrictions, each of the 32 output register bits can come from any bit on the data sources
- 8 x 257-bit instruction memory, for storing eight instructions, controlling control flow and the data path
- 2048 bytes of lookup table (LUT) memory, configurable as various word widths

## 54.3 Architectural Overview

The BitScrambler can be separated into a data path, a control path, and the registers that the CPU can use to program them. The data path moves bits between the incoming DMA stream, internal registers, and the outgoing DMA stream. The control path parses the instructions in the instruction memory to control the data path, as well as handle program flow.

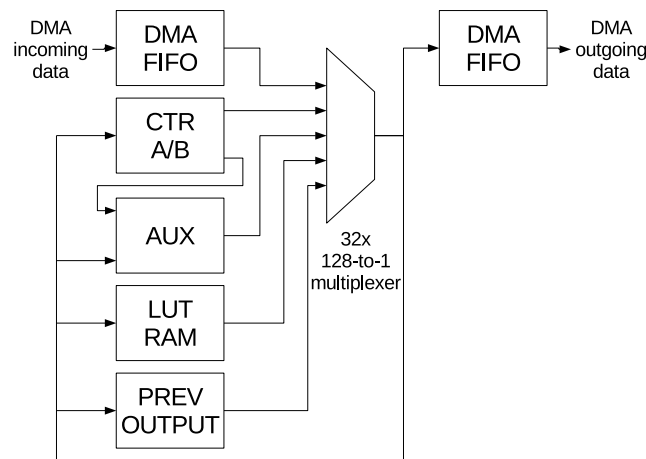


Figure 54.3-1. BitScrambler Data Path Diagram

### 54.3.1 Data Path

The data path of the BitScrambler is intended to take data from the incoming DMA stream, process it according to the program code stored in instruction memory, and write it to the outgoing DMA stream. Data is read from the incoming DMA stream into a 64-bit register. At the end of an instruction cycle, as specified in the instruction, N bits (with N being 0, 8, 16, or 32) are read from the DMA stream. The data in the register is then shifted toward the LSB of the register with the least significant N bits disappearing. Finally, the read data appears as the N most significant bits. Optionally, on startup, the BitScrambler will automatically read the first 64 bits into this register.

On the other side of the BitScrambler, data is deposited into a 32-bit output register. At the end of the instruction cycle, depending on what the instruction specifies, the least significant 0, 8, 16, or 32 bits will be written to the outgoing DMA stream.

The BitScrambler derives its name from the fact that it can put input bits in any random position in the output, and this is achieved by 32 x 128-to-1 multiplexers. For each of the 32 output register bits, there is one multiplexer that selects the input signals from one of the data sources, dependent on the output of the BitScrambler control path. These data sources are:

- 64 bits, shifted in from the input FIFO (i.e., the left DMA FIFO block in Figure 54.3-1). As described before, data from the incoming DMA stream is deposited here. In order to facilitate iterating over input bits in a loop, an instruction can enable relative addressing. In this addressing mode, any mux sourcing a bit from the input FIFO register will actually get the bit offset by the counter A register (i.e., CTR A in Figure 54.3-1).
- 32 bits that were sent to the output in the last cycle (i.e., PREV OUTPUT block in Figure 54.3-1). Data sent to the output register will appear on this register one clock cycle later. This allows the BitScrambler to 'remember' data over multiple clock cycles: by outputting a bit to the output register, even if that bit subsequently is not sent to the output FIFO, the next clock cycle can still access it by selecting from this register. Bits can be remembered longer-term by selecting bits from this register for output again, which makes them appear here in the subsequent cycle.
- 8, 16, or 32 bits that are the output of LUT RAM. The address used to select the data is the most significant bits of the output data of the last cycle. The LUT RAM is a part of the BitScrambler that takes an address, looks it up in its memory, and outputs the data located at that specific address. The LUT

RAM can be filled when the BitScrambler is initialized, but the BitScrambler itself does not have the ability to modify it. Depending on requirements, the LUT RAM can be initialized in the following modes:

- 512 x 32-bit words
- 1024 x 16-bit words
- 2048 x 8-bit words

The LUT RAM can be used to do translations of data, e.g. using a calibration curve for a given sensor. It can also be used to implement mathematical functions, with the address input split into two or more input variables and the data output used as the output of the function; the memory should be loaded with the output of the function for each of the input values.

- 32 bits from 2 x 16-bit counters (i.e., CTR A/B block in Figure 54.3-1). This register contains two 16-bit counters, named 'A' and 'B'. These can be loaded, incremented and decremented via control path instructions.
- 30 bits from comparators between counter B and the previous data on the output (PREV OUT in Figure 54.3-1; the 30 bits described here are part of the AUX block there). These allow the result of comparisons being used for output or for program flow. This can be useful in e.g. decoding run-length encoded streams, or generating PWM signals.
- 2 bits, one fixed-high, one fixed-low (i.e., part of AUX in Figure 54.3-1). These are useful if a protocol needs an always-high or always-low bit in the output that does not depend on the input data.

Note that some sources cannot be accessed at the same time. Specifically, a given instruction cannot source data from both the high 32 bits of the input FIFO source register as well as the counter registers. When data is read from the LUT, for a LUT that is set to a width of N, the top N bits of both the input FIFO register as well as the top N bits of the counter register become unavailable.

### 54.3.2 Control Path

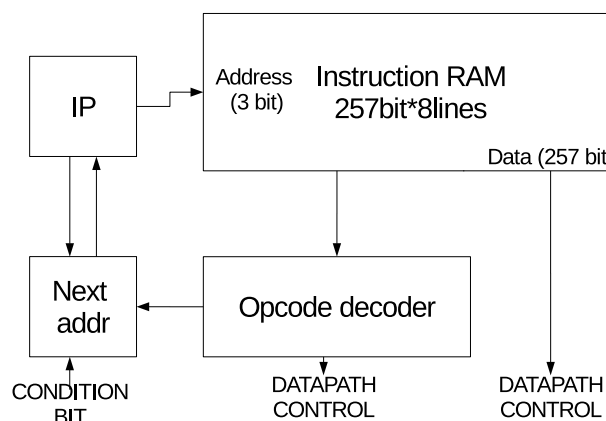


Figure 54.3-2. BitScrambler Control Path Diagram

The BitScrambler behavior is governed by a program stored in program RAM. The program RAM has space for up to eight instructions, each being 257 bits in size. An instruction configures the data path for the clock cycle the instruction runs in, as well as contains opcodes that control program flow.

A BitScrambler program is similar to a microprocessor program, in that each cycle the BitScrambler will execute the next instruction in instruction memory, unless the opcode tells it to specifically jump to another location.

Concretely, this behaviour is implemented using an instruction pointer (IP, see Figure 54.3-2), which points to the currently executing instruction. Opcodes can also affect the counter registers.

The bits of the instruction that configure the data path consist of settings for the 32 muxes, as well as some bits to select the availability of the counter bits or LUT output. It also can put the muxes into relative mode, where if they get a bit from the DMA FIFO, the position of that bit is offset by counter B.

## 54.4 Functional Description

The BitScrambler is a flexible device, with its behavior controlled by the program loaded into it as well as the configuration registers that set several global BitScrambler behaviors as well. As such, a BitScrambler program consists of the contents of the 257-bit x 8 instruction RAM as well as the settings for various configuration registers. Both are described below.

### 54.4.1 Instructions

The 257 bits that make up an instruction are structured as shown in Table 54.4-1.

**Table 54.4-1. Instruction Structure**

| Bit       | Field          | Bit       | Field           |
|-----------|----------------|-----------|-----------------|
| 0 - 6     | CTL_MUX_SEL_0  | 133 - 139 | CTL_MUX_SEL_19  |
| 7 - 13    | CTL_MUX_SEL_1  | 140 - 146 | CTL_MUX_SEL_20  |
| 14 - 20   | CTL_MUX_SEL_2  | 147 - 153 | CTL_MUX_SEL_21  |
| 21 - 27   | CTL_MUX_SEL_3  | 154 - 160 | CTL_MUX_SEL_22  |
| 28 - 34   | CTL_MUX_SEL_4  | 161 - 167 | CTL_MUX_SEL_23  |
| 35 - 41   | CTL_MUX_SEL_5  | 168 - 174 | CTL_MUX_SEL_24  |
| 42 - 48   | CTL_MUX_SEL_6  | 175 - 181 | CTL_MUX_SEL_25  |
| 49 - 55   | CTL_MUX_SEL_7  | 182 - 188 | CTL_MUX_SEL_26  |
| 56 - 62   | CTL_MUX_SEL_8  | 189 - 195 | CTL_MUX_SEL_27  |
| 63 - 69   | CTL_MUX_SEL_9  | 196 - 202 | CTL_MUX_SEL_28  |
| 70 - 76   | CTL_MUX_SEL_10 | 203 - 209 | CTL_MUX_SEL_29  |
| 77 - 83   | CTL_MUX_SEL_11 | 210 - 216 | CTL_MUX_SEL_30  |
| 84 - 90   | CTL_MUX_SEL_12 | 217 - 223 | CTL_MUX_SEL_31  |
| 91 - 97   | CTL_MUX_SEL_13 | 224 - 249 | OPCODE          |
| 98 - 104  | CTL_MUX_SEL_14 | 250 - 251 | CTL_READ_IN     |
| 105 - 111 | CTL_MUX_SEL_15 | 252 - 253 | CTL_WR_OUT      |
| 112 - 118 | CTL_MUX_SEL_16 | 254       | CTL_MUX_REL     |
| 119 - 125 | CTL_MUX_SEL_17 | 255       | CTL_CTR_SRC_SEL |
| 126 - 132 | CTL_MUX_SEL_18 | 256       | CTL_LUT_SRC_SEL |

The meanings of these fields are as follows:

- CTL\_MUX\_SEL\_n: This 7-bit field selects the source of bit n in the output register. See Table 54.4-3 for details.
- OPCODE: These bits encode an opcode. For the bit pattern of this field, please refer to Table 54.4-4.

- CTL\_READ\_IN: This selects the number of bits that are read from the input FIFO at the end of the instruction:
  - 0: Do not read any data
  - 1: Read 8 bits
  - 2: Read 16 bits
  - 3: Read 32 bits
- CTL\_WR\_OUT: This selects the number of bits that are written from the output register to the output FIFO at the end of the instruction:
  - 0: Do not write any data
  - 1: Write 8 bits
  - 2: Write 16 bits
  - 3: Write 32 bits
- CTL\_MUX\_REL, CTL\_CTR\_SRC\_SEL and CTR\_LUT\_SRC\_SEL: Select which bits are available to select using the CTL\_MUX\_SEL bits.
  - CTRL\_CTR\_SRC\_SEL (Control Counter Source Select) makes the bits from counter A and B available
  - CTL\_LUT\_SRC\_SEL (Control LUT Source Select) makes the output value of the LUT RAM available. See Table 54.4-3 for details.
  - When CTL\_MUX\_REL (Control Mux Relative) is 1, the BitScrambler applies the value of counter A as an offset to any CTL\_MUX\_SEL\_n value that is 63 or below. The exact behaviour depends on CTR\_SRC\_SEL, as detailed in Table 54.4-2.

**Table 54.4-2. Effective CTL\_MUX\_SEL\_n values when CTL\_MUX\_REL is 1**

| Condition  | Effective value of CTL_MUX_SEL     |
|--|------------------------------------|
| CTL_MUX_SEL_n >= 64                              | CTL_MUX_SEL (unchanged)            |
| CTL_MUX_SEL_n < 64 and CTL_CTR_SRC_SEL = 0       | (CTL_MUX_SEL_n + CTRA) & 63        |
| CTL_MUX_SEL_n < 31 and CTL_CTR_SRC_SEL = 1       | (CTL_MUX_SEL_n + CTRA) & 31        |
| 32 <= CTL_MUX_SEL_n < 64 and CTL_CTR_SRC_SEL = 1 | ((CTL_MUX_SEL_n + CTRA) & 31) + 32 |

Of these fields, most are data path configuration items. The field that affects the control path is OPCODE, although CTL\_MUX\_REL, CTL\_CTR\_SRC\_SEL, and CTR\_LUT\_SRC\_SEL may influence how some of the opcodes work by adjusting the source selection for the IF/IFN opcodes.

CTL\_MUX\_SEL\_n: These fields, one for each bit in the output register, select the source for that particular bit. The specific bit chosen is partially dependent on the settings of the CTL\_MUX\_REL, CTL\_CTR\_SRC\_SEL and CTR\_LUT\_SRC\_SEL. Given CTL\_MUX\_SRC\_n has value N, the bit is selected as described in Table 54.4-3. Note that the source selection for IF/IFN opcodes is affected in the same way.

Table 54.4-3. CTL\_MUX\_SEL Values

| Bit    | Description   |
|--------|---|
| 0-31   | The bit is sourced from bit N in the incoming FIFO register.  |
| 32-63  | The source of the bit depends on the setting of CTL_CTR_SRC_SEL and CTL_LUT_SRC_SEL:<br>If CTL_CTR_SRC_SEL = 0: the bit is sourced from bit N in the incoming FIFO register.<br>If CTL_CTR_SRC_SEL = 1: the bit is sourced from bit (N-32) of the counter registers. Specifically, if N is 32 to 47, the bit is sourced from bit (N-32) of counter A and if N is 48 to 63, the bit is sourced from bit (N-48) of counter B.<br>If CTL_LUT_SRC_SEL = 1: Depending on the width of the LUT (8, 16, or 32 bits), a read of the top 8, 16, or 32 bits will return data from the LUT rather than what CTL_CTR_SRC_SEL selects. Specifically, given a LUT width of N, 63 will return LUT output bit (N-1), 62 will return LUT output bit (N-2) and so on. |
| 64     | CounterB[7:0] =< last[7:0]  |
| 65     | CounterB[7:0] > last[7:0]   |
| 66     | CounterB[7:0] = last[7:0]   |
| 67     | CounterB[7:0] =< last[15:8]   |
| 68     | CounterB[7:0] > last[15:8]  |
| 69     | CounterB[7:0] = last[15:8]  |
| 70     | CounterB[7:0] =< last[23:16]  |
| 71     | CounterB[7:0] > last[23:16]   |
| 72     | CounterB[7:0] = last[23:16]   |
| 73     | CounterB[7:0] =< last[31:24]  |
| 74     | CounterB[7:0] > last[31:24]   |
| 75     | CounterB[7:0] = last[31:24]   |
| 76     | CounterB[15:8] =< last[7:0]   |
| 77     | CounterB[15:8] > last[7:0]  |
| 78     | CounterB[15:8] = last[7:0]  |
| 79     | CounterB[15:8] =< last[15:8]  |
| 80     | CounterB[15:8] > last[15:8]   |
| 81     | CounterB[15:8] = last[15:8]   |
| 82     | CounterB[15:8] =< last[23:16]   |
| 83     | CounterB[15:8] > last[23:16]  |
| 84     | CounterB[15:8] = last[23:16]  |
| 85     | CounterB[15:8] =< last[31:24]   |
| 86     | CounterB[15:8] > last[31:24]  |
| 87     | CounterB[15:8] = last[31:24]  |
| 88     | CounterB[15:0] =< last[15:0]  |
| 89     | CounterB[15:0] > last[15:0]   |
| 90     | CounterB[15:0] = last[15:0]   |
| 91     | CounterB[15:0] =< last[31:16]   |
| 92     | CounterB[15:0] > last[31:16]  |
| 93     | CounterB[15:0] = last[31:16]  |
| 94     | Always 0  |
| 95     | Always 1  |
| 96-127 | The bits selected here are the same as the bits on the output register at the end of the previous cycle.  |



The BitScrambler recognizes six opcodes, which are encoded in the opcode fields as shown in Table 54.4-4.

**Table 54.4-4. Instruction Opcode**

| Bit   | 25 | 24 | 23  | 22 | 21 | 20      | 19 | 18 | 17 | 16 | 15      | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6   | 5 | 4       | 3 | 2 | 1 | 0 |
|-------|----|----|-----|----|----|---------|----|----|----|----|---------|----|----|----|----|----|---|---|---|-----|---|---------|---|---|---|---|
| LOOP  | 1  | c  | tgt |    |    | end_val |    |    |    |    |         |    |    |    |    |    |   |   |   |     |   | ctr_add |   |   |   |   |
| ADD   | 0  | c  | h   | l  | 0  | 0       | 0  | 0  | 0  | 0  | ctr_add |    |    |    |    |    |   |   |   |     |   |         |   |   |   |   |
| IF    | 0  | 0  | tgt |    |    | 0       | 0  | 0  | 0  | 1  | 0       | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | src |   |         |   |   |   |   |
| IFN   | 0  | 0  | tgt |    |    | 0       | 0  | 0  | 1  | 0  | 0       | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | src |   |         |   |   |   |   |
| LDCTD | 0  | c  | h   | l  | 0  | 0       | 0  | 0  | 1  | 1  | ctr_set |    |    |    |    |    |   |   |   |     |   |         |   |   |   |   |
| LDCTI | 0  | c  | h   | l  | 0  | 0       | 0  | 1  | 0  | 0  | 0       | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0   | 0 | 0       | 0 | 0 | 0 | 0 |

The fields are defined as follows:

- c: Configures which counter to use.
  - 0: counter A
  - 1: counter B
- end\_val, ctr\_add, ctr\_set: 16-bit (or 5-bit) value. Please refer to the instruction descriptions below for the meanings of these fields.
- tgt: The location of an instruction. Range: 0 ~ 7.
- h: 1 if the upper 8 bits need to be written back to a counter.
- l: 1 if the lower 8 bits need to be written back to a counter.

Note that if an opcode does not specify H or L, it is assumed that the full 16 bits need to be written back and the h and l bits will both be 1.

These six opcodes affect the state of the BitScrambler as follows:

**Table 54.4-5. LOOP Opcode**

| LOOPc end_val, ctr_add, tgt  |   |
|--|---|
| Loop on counter indicated by c, add ctr_add to the counter, and loop back to tgt until the counter reaches end_val. When that happens, reset the counter and fall through. |   |
| Argument   | c: Either A or B, indicates counter to use<br>tgt: 3-bit target instruction addresses<br>end_val: 16-bit value to compare the counter to<br>ctr_add: 5-bit signed value to add to the counter |
| Pseudo-code  | <pre> if ((unsigned)ctrC &lt; end_val) begin     IP &lt;= tgt     ctr_c &lt;= ctr_c + sign_extend(ctr_add) end else begin     IP &lt;= IP + 1     ctr_c &lt;= 0 end           </pre>          |

Table 54.4-6. ADD Opcode

| ADDc[H L] ctr_add  |   |
|--|---|
| Add immediate value to counter indicated by c, and optionally write back only upper or lower 8 bits. |   |
| Argument   | <p>c: Either A or B, indicate counter to use</p> <p>ctr_add: 16-bit value to add to counter</p> <p>If opcode is ADDcH, only most significant 8 bits are written back</p> <p>If opcode is ADDcL, only least-significant 8 bits are written back</p> <p>If opcode is ADDc, all 16 bits will be written back (h=1, l=1).</p> |
| Pseudo-code  | <pre> tmp &lt;= ctr_c + ctr_add if (h) begin     ctr_c[15:8] &lt;= tmp[15:8] end if (l) begin     ctr_c[7:0] &lt;= tmp[7:0] end IP &lt;= IP + 1 </pre>  |
| Note   | The NOP (no operation) pseudo-op is encoded as 'ADDA 0'.  |

Table 54.4-7. IF Opcode

| IF ctl_cond_src, tgt                                   |  |
|--|--|
| Jump to target if the indicated mux source bit is set. |  |
| Argument   | <p>ctl_cond_src: Mux source (see <a href="#">CTR_MUX_SRC sources</a>)</p> <p>tgt: 3-bit target instruction addresses</p> |
| Pseudo-code  | <pre> if (ctl_cond_src) begin     IP &lt;= tgt end else begin     IP &lt;= IP + 1 end </pre>                             |
| Note   | The JMP (always jump) pseudo-op is implemented as an 'IF 95,tgt' opcode, using the always-1 bit from the AUX bits.       |

Table 54.4-8. IFN Opcode

| IFN ctl_cond_src, tgt  |  |
|--|--|
| Jump to target if the indicated mux source bit is NOT set (note: same as IF but condition is negated). |  |
| Argument   | <p>ctl_cond_src: Mux source (see <a href="#">CTR_MUX_SRC sources</a>)</p> <p>tgt: 3-bit target instruction addresses</p> |
| Pseudo-code  | <pre> if (ctl_cond_src) begin     IP &lt;= IP + 1 end else begin     IP &lt;= tgt end </pre>                             |

**Table 54.4-9. LDCTD Opcode**

| LDCTDc[H L] ctr_set   |  |
|---|--|
| Load counter direct (from immediate), and optionally only load high or low 8 bits of counter. |  |
| Argument  | c: Either A or B, indicate counter to use<br>ctr_set: 16-bit value to set the counter to<br>h: If opcode is LDCTDcH, only most significant 8 bits are set<br>l: If opcode is LDCTDcL, only least-significant 8 bits are set<br>If opcode is LDCTDc, all 16 bits are set (h=1, l=1) |
| Pseudo-code   | <pre> if (h) begin     ctr_c[15:8] &lt;= ctr_set[15:8] end if (l) begin     ctr_c[7:0] &lt;= ctr_set[7:0] end IP &lt;= IP + 1 </pre>   |

**Table 54.4-10. LDCTI Opcode**

| LDCTIc[H L]  |   |
|--|---|
| Load counter indirect (from most significant 16 bits of mux output), and optionally only load high or low 8 bits of counter. |   |
| Argument   | c: Either A or B, indicate counter to use<br>h: If opcode is LDCTIcH, only the most significant 8 bits are set<br>l: If opcode is LDCTIcL, only the least significant 8 bits are set<br>If opcode is LDCTIc, all 16 bits are set (h=1, l=1) |
| Pseudo-code  | <pre> if (h) begin     ctr_c[15:8] &lt;= mux_out[31:24] end if (l) begin     ctr_c[7:0] &lt;= mux_out[23:16] end IP &lt;= IP + 1 </pre>   |

## 54.4.2 Configuration Registers

The BitScrambler is configured using a set of registers. Specifically, these registers are used to write a program into BitScrambler, write its LUT RAM, configure its behaviour, and start and stop BitScrambler operation. They are also used to attach a BitScrambler to a peripheral DMA path.

The ESP32-P4 has two BitScramblers: one can be placed in the TX path (where data is sent from the memory to a peripheral) while the other can be placed in a RX path (where data is sent from the peripheral to memory). The configuration registers for the two BitScramblers are the same, with the only difference being the TX path BitScrambler registers are prefixed by BITSCRAMBLER\_TX\_ while the RX path BitScrambler uses BITSCRAMBLER\_RX\_ prefixes.

**Note:**

For convenience, in this section we will refer to the TX path BitScrambler only; to get the RX path BitScrambler descriptions, simply swap the prefixes.

When modifying the input or output of a peripheral, the BitScrambler needs to be attached to the DMA path of that peripheral. To do this, write the appropriate value for the peripheral into the `HP_SYSTEM_BITSCRAMBLER_PERI_TX_SEL` or `HP_SYSTEM_BITSCRAMBLER_PERI_RX_SEL` field of the `HP_SYSTEM_BITSCRAMBLER_PERI_SEL_REG` register.

The BitScrambler can also run in memory-to-memory mode. For this, the `BITSCRAMBLER_LOOP_MODE` bit in `BITSCRAMBLER_SYS_REG` needs to be set to one. In this mode, the TX BitScrambler is put into loopback mode while the RX BitScrambler is unused and unavailable. The BitScrambler still needs to be attached to a peripheral (although the peripheral does not need to be configured); the DMA path for this peripheral will be unusable.

Neither the program memory nor the LUT RAM are accessible to the main processor directly. Rather, they need to be written indirectly, by setting an address in one register and then writing the data in a second register.

Specifically, for the LUT RAM, the address is written in the `BITSCRAMBLER_TX_LUT_IDX` field of `BITSCRAMBLER_TX_LUT_CFG0_REG` and the data is written to or read from `BITSCRAMBLER_TX_LUT_CFG1_REG`. The width of the LUT, as visible to the BitScrambler, can be configured using the `BITSCRAMBLER_TX_LUT_MODE` field. Note that regardless of the width the LUT is configured to have on the BitScrambler side, the main processor always writes the memory in 32-bit wide words.

Similarly, the instruction memory is written by setting the address up in `BITSCRAMBLER_TX_INST_CFG0_REG` and writing the data to or reading it from `BITSCRAMBLER_TX_INST_CFG1_REG`. As the BitScrambler instructions are 257 bits, one instruction needs to be written as 9 32-bit words (with the 257th bit being in the LSB of the 9th word). To achieve that purpose, the `BITSCRAMBLER_TX_INST_CFG0_REG` register is divided into two fields. The position of the instruction is written into the `BITSCRAMBLER_TX_INST_IDX` field while the word offset within the instruction is written to `BITSCRAMBLER_TX_INST_POS`.

As the BitScrambler has the ability to generate more or less data than it gets on the input, a BitScrambler-controlled DMA stream can end in one or two ways. The first is that the receiver (either memory in case of the RX BitScrambler, or the peripheral in case of the TX BitScrambler) stops accepting data because it is configured to only receive a limited number of bytes. This case is pretty simple: the BitScrambler will simply halt as it cannot write any more data. The other way is that the transmitter (the peripheral for the RX BitScrambler and the memory for the TX BitScrambler) stops sending data. This is a more complicated situation, as the BitScrambler may or may not be processing some data that needs to be written to the output.

In order to allow the BitScrambler to send out the data it is still processing, two methods have been devised to handle a certain amount of data after the input data stream has ended. Both depend on setting `BITSCRAMBLER_RX_TAILING_BITS_REG` to a certain value N:

- EOF-on-N-reads: After the input data stream ends, the BitScrambler reads N dummy bytes from the input. The value of these bytes is zero. After the Nth byte is read, the BitScrambler halts and the DMA stream ends.
- EOF-on-N-writes: After the input data stream ends, the BitScrambler is allowed to write N more bytes to

the output. During this time, any reads on the input stream return zero-value dummy bytes. After the N'th byte is written, the BitScrambler halts and the DMA stream ends.

To configure either mode, set the option bits as follows:

**Table 54.4-11. Settings for EOF modes**

| Register                                   | EOF-on-N-reads | EOF-on-N-writes |
|--|----------------|-----------------|
| <a href="#">BITSCRAMBLER_TX_RD_DUMMY</a>   | 1              | 1               |
| <a href="#">BITSCRAMBLER_TX_FETCH_MODE</a> | 0              | 0               |
| <a href="#">BITSCRAMBLER_TX_EOF_MODE</a>   | 1              | 0               |
| <a href="#">BITSCRAMBLER_TX_HALT_MODE</a>  | 1              | 1               |

## 54.5 Programming Procedures

Note that these instructions are written for a TX BitScrambler, which is in the memory-to-peripheral path, or memory-to-memory path if in loopback mode. For the peripheral-to-memory path, the RX BitScrambler is used. Unless otherwise indicated, you can exchange "TX" for "RX" in these instructions to configure the RX BitScrambler.

1. Attach the BitScrambler to a peripheral by configuring [HP\\_SYSTEM\\_BITSCRAMBLER\\_PERI\\_TX\\_SEL](#) field in [HP\\_SYSTEM\\_BITSCRAMBLER\\_PERI\\_SEL\\_REG](#) register. Note that this step is required even in loopback mode.
2. Enable the BitScrambler by setting the [BITSCRAMBLER\\_TX\\_ENA](#) field in the [BITSCRAMBLER\\_TX\\_CTRL\\_REG](#) register.
3. Configure loopback mode if required. If loopback mode is needed, set [BITSCRAMBLER\\_LOOP\\_MODE](#) in the [BITSCRAMBLER\\_SYS\\_REG](#) register. Otherwise, clear it.
4. Load program into BitScrambler. For each instruction and each 32-bit word within the instruction, set the [BITSCRAMBLER\\_TX\\_INST\\_IDX](#) and [BITSCRAMBLER\\_TX\\_INST\\_POS](#) fields in the [BITSCRAMBLER\\_TX\\_INST\\_CFG0\\_REG](#) register, then write the word in the [BITSCRAMBLER\\_TX\\_INST\\_CFG1\\_REG](#) register. Note that the 257'th bit is written as bit 0 into [BITSCRAMBLER\\_TX\\_INST\\_CFG1\\_REG](#).
5. Load LUT into BitScrambler, if needed. Similar to loading the program, the LUT is loaded in 32-bit words by first writing the word address to the [BITSCRAMBLER\\_TX\\_LUT\\_CFG0\\_REG](#) and then writing the word itself to [BITSCRAMBLER\\_TX\\_LUT\\_CFG1\\_REG](#). After loading the LUT, configure its width by setting [BITSCRAMBLER\\_TX\\_LUT\\_MODE](#) in [BITSCRAMBLER\\_TX\\_LUT\\_CFG0\\_REG](#).
6. Configure BitScrambler. Dependent on what the BitScrambler program expects, you may need to set or clear the various bits in the [BITSCRAMBLER\\_TX\\_CTRL\\_REG](#) register. You may also need to set [BITSCRAMBLER\\_TX\\_TAILING\\_BITS\\_REG](#) to an applicable value.
7. Start the BitScrambler by clearing the [BITSCRAMBLER\\_TX\\_HALT](#) bit in the [BITSCRAMBLER\\_TX\\_CTRL\\_REG](#) register.
8. Start DMA transaction. Please refer to Chapter 3 *GDMA Controller (GDMA-AHB, GDMA-AXI)* for more information about DMA subsystem and refer to the peripheral chapter if loopback mode is not used.
9. Wait until DMA transaction is done.

10. Halt the BitScrambler by setting the [BITSCRAMBLER\\_TX\\_HALT](#) in the [BITSCRAMBLER\\_TX\\_CTRL\\_REG](#) register.
11. Wait for halt state. The BitScrambler is halted when the [BITSCRAMBLER\\_TX\\_IN\\_IDLE](#) bit in the [BITSCRAMBLER\\_TX\\_STATE\\_REG](#) register is set.
12. Reset the FIFO by writing a 1 and then a 0 to the [BITSCRAMBLER\\_TX\\_FIFO\\_RST](#) bit in the [BITSCRAMBLER\\_TX\\_CTRL\\_REG](#) register.
13. The BitScrambler is ready for a new transaction with the current program and LUT configuration. Simply start from step 7 to do this.

## 54.6 Register Summary

The addresses in this section are relative to the Bit-scrambler base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

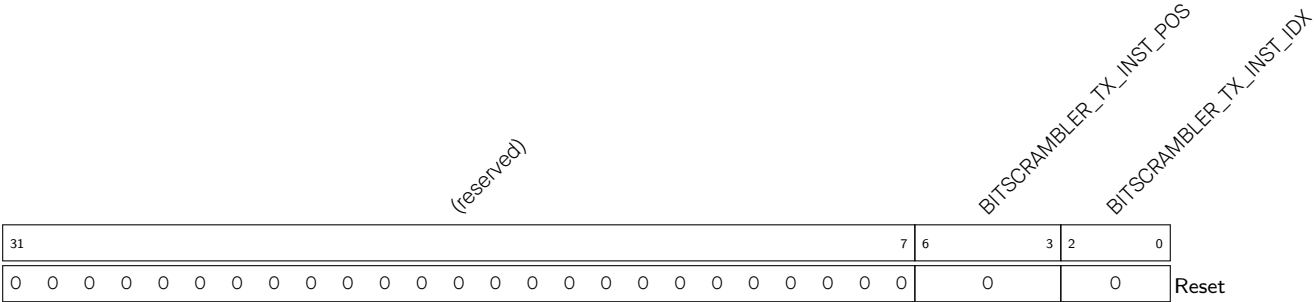
| Name   | Description  | Address | Access |
|--|--|---------|--------|
| <b>Control and configuration registers</b>       |  |         |        |
| <a href="#">BITSCRAMBLER_TX_INST_CFG0_REG</a>    | BitScrambler TX core instruction memory address selection register | 0x0000  | R/W    |
| <a href="#">BITSCRAMBLER_TX_INST_CFG1_REG</a>    | BitScrambler TX core instruction memory access register            | 0x0004  | R/W    |
| <a href="#">BITSCRAMBLER_RX_INST_CFG0_REG</a>    | BitScrambler RX core instruction memory address selection register | 0x0008  | R/W    |
| <a href="#">BITSCRAMBLER_RX_INST_CFG1_REG</a>    | BitScrambler RX core instruction memory access register            | 0x000C  | R/W    |
| <a href="#">BITSCRAMBLER_TX_LUT_CFG0_REG</a>     | BitScrambler TX core LUT memory address selection register         | 0x0010  | R/W    |
| <a href="#">BITSCRAMBLER_TX_LUT_CFG1_REG</a>     | BitScrambler TX core LUT memory access register                    | 0x0014  | R/W    |
| <a href="#">BITSCRAMBLER_RX_LUT_CFG0_REG</a>     | BitScrambler RX core LUT memory address selection register         | 0x0018  | R/W    |
| <a href="#">BITSCRAMBLER_RX_LUT_CFG1_REG</a>     | BitScrambler RX core LUT memory access register                    | 0x001C  | R/W    |
| <b>Configuration registers</b>                   |  |         |        |
| <a href="#">BITSCRAMBLER_TX_TAILING_BITS_REG</a> | BitScrambler TX core extra data length register                    | 0x0020  | R/W    |
| <a href="#">BITSCRAMBLER_RX_TAILING_BITS_REG</a> | BitScrambler RX core extra data length register                    | 0x0024  | R/W    |
| <a href="#">BITSCRAMBLER_TX_CTRL_REG</a>         | BitScrambler TX core control register                              | 0x0028  | varies |
| <a href="#">BITSCRAMBLER_RX_CTRL_REG</a>         | BitScrambler RX core control register                              | 0x002C  | varies |
| <a href="#">BITSCRAMBLER_SYS_REG</a>             | Loopback control register  | 0x00F8  | R/W    |
| <b>Status registers</b>                          |  |         |        |
| <a href="#">BITSCRAMBLER_TX_STATE_REG</a>        | BitScrambler TX core status register                               | 0x0030  | varies |
| <a href="#">BITSCRAMBLER_RX_STATE_REG</a>        | BitScrambler RX core status register                               | 0x0034  | varies |
| <b>Version register</b>                          |  |         |        |
| <a href="#">BITSCRAMBLER_VERSION_REG</a>         | Version control register   | 0x00FC  | R/W    |

## 54.7 Registers

The addresses in this section are relative to the Bit-scrambler base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

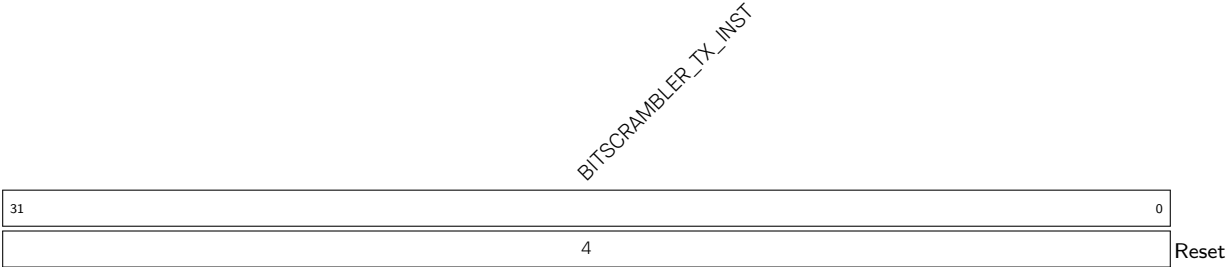
Register 54.1. BITSCRAMBLER\_TX\_INST\_CFG0\_REG (0x0000)



**BITSCRAMBLER\_TX\_INST\_IDX** Configures the index of the BitScrambler instruction to be accessed via [BITSCRAMBLER\\_TX\\_INST\\_CFG1\\_REG](#). (R/W)

**BITSCRAMBLER\_TX\_INST\_POS** Configures the offset into the 257-bit BitScrambler instruction (in 32-bit increments) to be accessed via [BITSCRAMBLER\\_TX\\_INST\\_CFG1\\_REG](#). (R/W)

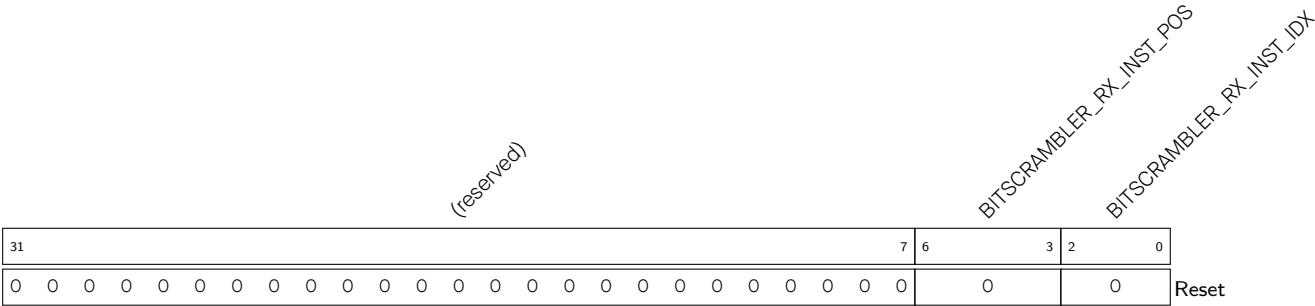
Register 54.2. BITSCRAMBLER\_TX\_INST\_CFG1\_REG (0x0004)



**BITSCRAMBLER\_TX\_INST** Configures the instruction to be accessed at the address specified by [BITSCRAMBLER\\_TX\\_INST\\_CFG0\\_REG](#). (R/W)

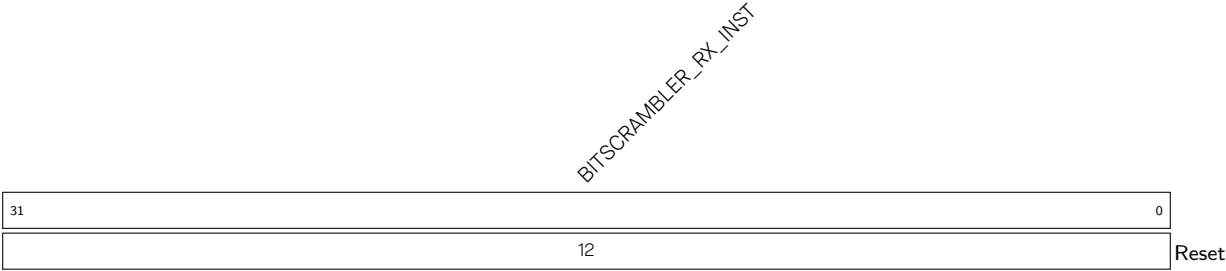


Register 54.3. BITSCRAMBLER\_RX\_INST\_CFG0\_REG (0x0008)



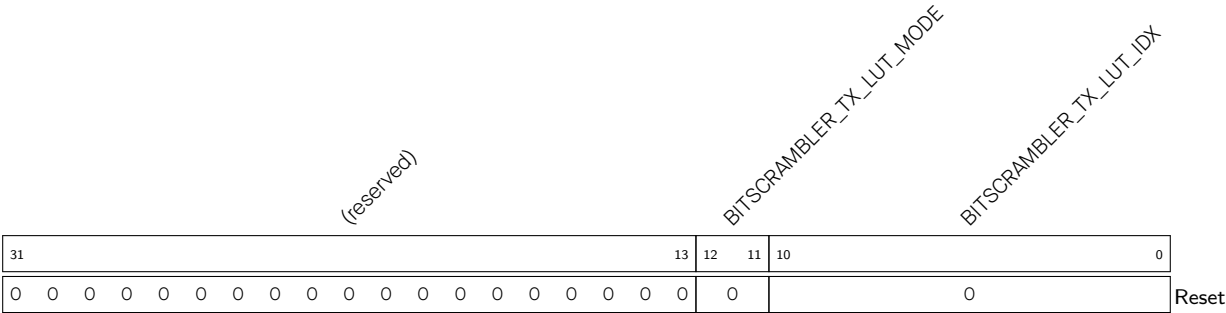
- BITSCRAMBLER\_RX\_INST\_IDX** Configures the index of the BitScrambler instruction to be accessed via [BITSCRAMBLER\\_RX\\_INST\\_CFG1\\_REG](#). (R/W)
- BITSCRAMBLER\_RX\_INST\_POS** Configures the offset into the 257-bit BitScrambler instruction (in 32-bit increments) to be accessed via [BITSCRAMBLER\\_RX\\_INST\\_CFG1\\_REG](#). (R/W)

Register 54.4. BITSCRAMBLER\_RX\_INST\_CFG1\_REG (0x000C)



- BITSCRAMBLER\_RX\_INST** Configures the instruction to be accessed at the address specified by [BITSCRAMBLER\\_RX\\_INST\\_CFG0\\_REG](#). (R/W)

Register 54.5. BITSCRAMBLER\_TX\_LUT\_CFG0\_REG (0x0010)



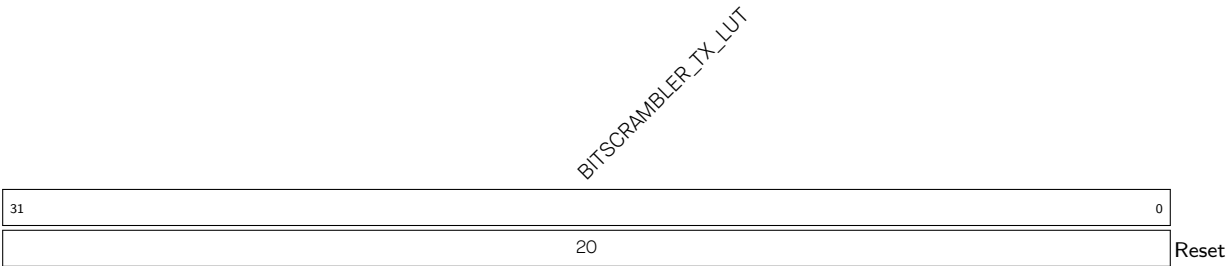
**BITSCRAMBLER\_TX\_LUT\_IDX** Configures the position (in 32-bit increments) into LUT RAM to be accessed via [BITSCRAMBLER\\_TX\\_LUT\\_CFG1\\_REG](#). (R/W)

**BITSCRAMBLER\_TX\_LUT\_MODE** Configures the word size of LUT RAM for Bitscrambler programs.

- 0: 1 Byte
- 1: 2 Bytes
- 2: 4 Bytes
- 3: Reserved

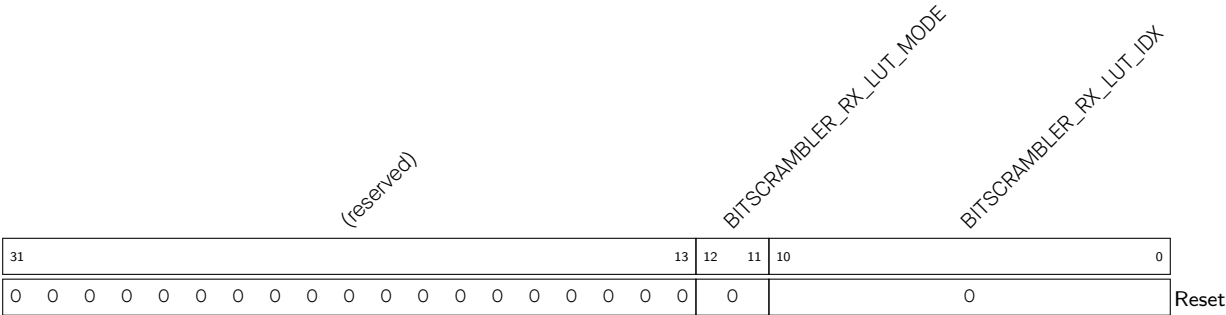
(R/W)

Register 54.6. BITSCRAMBLER\_TX\_LUT\_CFG1\_REG (0x0014)



**BITSCRAMBLER\_TX\_LUT** Configures the LUT entry to be accessed at the position specified by [BITSCRAMBLER\\_TX\\_LUT\\_CFG0\\_REG](#). (R/W)

Register 54.7. BITSCRAMBLER\_RX\_LUT\_CFG0\_REG (0x0018)



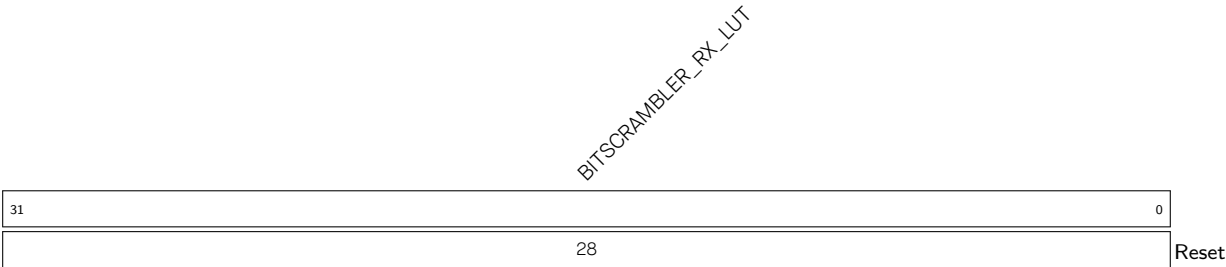
**BITSCRAMBLER\_RX\_LUT\_IDX** Configures the position (in 32-bit increments) into LUT RAM to be accessed via [BITSCRAMBLER\\_RX\\_LUT\\_CFG1\\_REG](#). (R/W)

**BITSCRAMBLER\_RX\_LUT\_MODE** Configures the word size of LUT RAM for BitScrambler programs.

- 0: 1 byte
- 1: 2 bytes
- 2: 4 bytes
- 3: Reserved

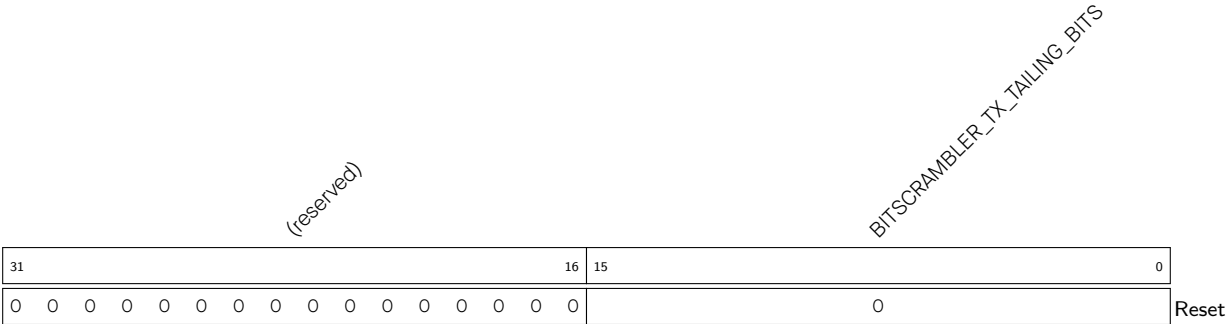
(R/W)

Register 54.8. BITSCRAMBLER\_RX\_LUT\_CFG1\_REG (0x001C)



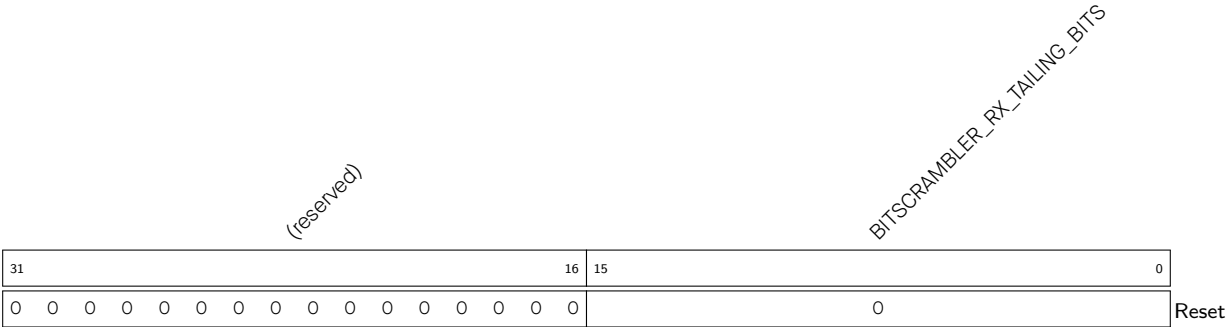
**BITSCRAMBLER\_RX\_LUT** Configures the LUT entry to be accessed at the position specified by [BITSCRAMBLER\\_RX\\_LUT\\_CFG0\\_REG](#). (R/W)

Register 54.9. BITSCRAMBLER\_TX\_TAILING\_BITS\_REG (0x0020)



**BITSCRAMBLER\_TX\_TAILING\_BITS** Configures the length of extra data after getting EOF for the TX BitScrambler core. Measurement unit: bit. (R/W)

Register 54.10. BITSCRAMBLER\_RX\_TAILING\_BITS\_REG (0x0024)



**BITSCRAMBLER\_RX\_TAILING\_BITS** Configures the length of extra data after getting EOF for the BitScrambler RX core. Measurement unit: bit. (R/W)

## Register 54.11. BITSCRAMBLER\_TX\_CTRL\_REG (0x0028)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | BITSCRAMBLER_TX_FIFO_RST<br>BITSCRAMBLER_TX_RD_DUMMY<br>BITSCRAMBLER_TX_HALT_MODE<br>BITSCRAMBLER_TX_FETCH_MODE<br>BITSCRAMBLER_TX_COND_MODE<br>BITSCRAMBLER_TX_EOF_MODE<br>BITSCRAMBLER_TX_PAUSE<br>BITSCRAMBLER_TX_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**BITSCRAMBLER\_TX\_ENA** Configures whether to enable BitScrambler TX core.

0: Disable

1: Enable

(R/W)

**BITSCRAMBLER\_TX\_PAUSE** Configures whether to pause BitScrambler TX core. A paused core can be un-paused to resume execution.

0: Not pause

1: Pause

(R/W)

**BITSCRAMBLER\_TX\_HALT** Configures whether to halt BitScrambler TX core. Halting the BitScrambler TX core will flush the FIFOs and cannot be resumed; a FIFO reset and a restart is needed.

0: Not halt

1: Halt (R/W)

**BITSCRAMBLER\_TX\_EOF\_MODE** Configures BitScrambler TX core EOF signal generating mode.

This is combined with [BITSCRAMBLER\\_TX\\_TAILING\\_BITS](#) for use.

0: Data written to the output FIFO are counted to generate delayed EOF

1: Data read from the input FIFO are counted to generate delayed EOF

(R/W)

**BITSCRAMBLER\_TX\_COND\_MODE** Configures BitScrambler TX LOOP instruction condition mode.

0: Use the less than operator to get the condition

1: Use not equal operator to get the condition

(R/W)

**BITSCRAMBLER\_TX\_FETCH\_MODE** Configures BitScrambler TX core fetch instruction mode.

0: Prefetch by reset

1: Fetch by instructions

(R/W)

**BITSCRAMBLER\_TX\_HALT\_MODE** Configures BitScrambler TX core halt mode when [BITSCRAMBLER\\_TX\\_HALT](#) is set

0: Wait for write data back done

1: Ignore write data back

(R/W)

Continued on the next page...

**Register 54.11. BITSCRAMBLER\_TX\_CTRL\_REG (0x0028)**

Continued from the previous page...

**BITSCRAMBLER\_TX\_RD\_DUMMY** Configures BitScrambler TX core read data mode when EOF received.

0: Wait read data

1: Ignore read data

(R/W)

**BITSCRAMBLER\_TX\_FIFO\_RST** Configures whether to reset BitScrambler TX FIFO.

0: Not reset

1: Reset

(WT)

## Register 54.12. BITSCRAMBLER\_RX\_CTRL\_REG (0x002C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | BITSCRAMBLER_RX_FIFO_RST<br>BITSCRAMBLER_RX_RD_DUMMY<br>BITSCRAMBLER_RX_HALT_MODE<br>BITSCRAMBLER_RX_FETCH_MODE<br>BITSCRAMBLER_RX_COND_MODE<br>BITSCRAMBLER_RX_EOF_MODE<br>BITSCRAMBLER_RX_PAUSE<br>BITSCRAMBLER_RX_ENA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   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|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 9  | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**BITSCRAMBLER\_RX\_ENA** Configures whether to enable BitScrambler RX core.

0: Disable

1: Enable

(R/W)

**BITSCRAMBLER\_RX\_PAUSE** Configures whether to pause BitScrambler RX core. A paused core can be un-paused to resume execution.

0: Not pause

1: Pause

(R/W)

**BITSCRAMBLER\_RX\_HALT** Configures whether to halt BitScrambler RX core. Halting the BitScrambler RX core will flush the FIFOs and cannot be resumed; a FIFO reset and a restart is needed.

0: Not halt

1: Halt

(R/W)

**BITSCRAMBLER\_RX\_EOF\_MODE** Configures BitScrambler RX core EOF signal generating mode.

This is combined with [BITSCRAMBLER\\_RX\\_TAILING\\_BITS](#) for use.

0: Data written to the output FIFO are counted to generate delayed EOF

1: Data read from the input FIFO are counted to generate delayed EOF

(R/W)

**BITSCRAMBLER\_RX\_COND\_MODE** Configures BitScrambler RX LOOP instruction condition mode.

0: Use the less than operator to get the condition

1: Use not equal operator to get the condition

(R/W)

**BITSCRAMBLER\_RX\_FETCH\_MODE** Configures BitScrambler RX core fetch instruction mode

0: Prefetch by reset

1: Fetch by instructions

(R/W)

Continued on the next page...

Register 54.12. BITSCRAMBLER\_RX\_CTRL\_REG (0x002C)

Continued from the previous page...

**BITSCRAMBLER\_RX\_HALT\_MODE** Configures BitScrambler RX core halt mode when **BITSCRAMBLER\_RX\_HALT** is set

0: Wait for write data back done

1: Ignore write data back

(R/W)

**BITSCRAMBLER\_RX\_RD\_DUMMY** Configures BitScrambler RX core read data mode when EOF received.

0: Wait read data

1: Ignore read data

(R/W)

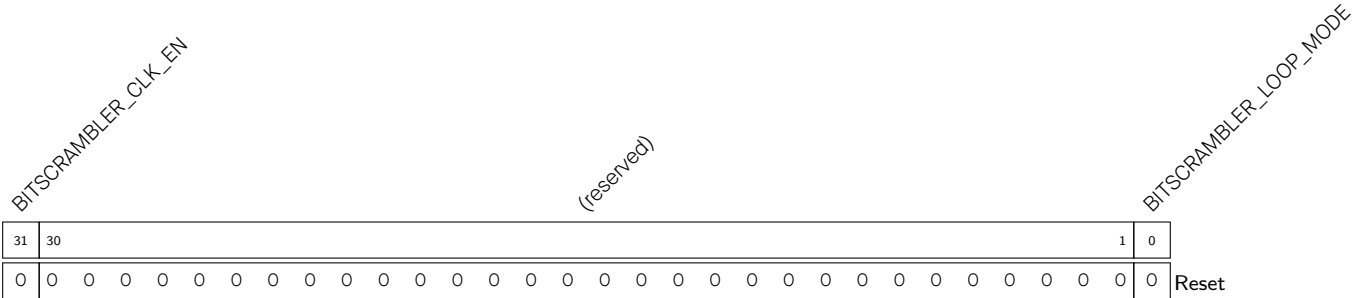
**BITSCRAMBLER\_RX\_FIFO\_RST** Configures whether to reset BitScrambler RX FIFO.

0: Not reset

1: Reset

(WT)

Register 54.13. BITSCRAMBLER\_SYS\_REG (0x00F8)



**BITSCRAMBLER\_LOOP\_MODE** Configures whether to enable BitScrambler TX to DMA RX loopback mode

0: Disable

1: Enable

(R/W)

**BITSCRAMBLER\_CLK\_EN** Reserved. (R/W)



Register 54.14. BITSCRAMBLER\_TX\_STATE\_REG (0x0030)

|                               |    |                             |    |  |  |  |  |  |  |  |  |            |    |   |   |                            |   |   |   |                          |   |                         |   |                        |   |                         |   |   |   |       |
|-------------------------------|----|-----------------------------|----|--|--|--|--|--|--|--|--|------------|----|---|---|----------------------------|---|---|---|--------------------------|---|-------------------------|---|------------------------|---|-------------------------|---|---|---|-------|
| BITSCRAMBLER_TX_EOF_TRACE_CLR |    | BITSCRAMBLER_TX_EOF_GET_CNT |    |  |  |  |  |  |  |  |  | (reserved) |    |   |   | BITSCRAMBLER_TX_FIFO_EMPTY |   |   |   | BITSCRAMBLER_TX_IN_PAUSE |   | BITSCRAMBLER_TX_IN_WAIT |   | BITSCRAMBLER_TX_IN_RUN |   | BITSCRAMBLER_TX_IN_IDLE |   |   |   |       |
| 31                            | 30 | 29                          | 16 |  |  |  |  |  |  |  |  |            | 15 | 5 |   |                            |   | 4 | 3 | 2                        | 1 | 0                       |   |                        |   |                         |   |   |   |       |
| 0                             | 0  | 0                           |    |  |  |  |  |  |  |  |  | 0          | 0  | 0 | 0 | 0                          | 0 | 0 | 0 | 0                        | 0 | 0                       | 0 | 0                      | 0 | 0                       | 0 | 0 | 1 | Reset |

**BITSCRAMBLER\_TX\_IN\_IDLE** Represents whether BitScrambler TX core is halted.

0: Not halted

1: Halted

(RO)

**BITSCRAMBLER\_TX\_IN\_RUN** Represents whether BitScrambler TX core is running.

0: Not running

1: Running

(RO)

**BITSCRAMBLER\_TX\_IN\_WAIT** Represents whether BitScrambler TX core is waiting for write back done.

0: Not waiting

1: Waiting

(RO)

**BITSCRAMBLER\_TX\_IN\_PAUSE** Represents whether BitScrambler TX core is paused.

0: Not paused

1: Paused

(RO)

**BITSCRAMBLER\_TX\_FIFO\_EMPTY** Represents whether BitScrambler TX FIFO is empty

0: Not empty

1: Empty

(RO)

**BITSCRAMBLER\_TX\_EOF\_GET\_CNT** Represents byte count of BitScrambler TX core after EOF is received. (RO)

**BITSCRAMBLER\_TX\_EOF\_OVERLOAD** Represents whether BitScrambler TX core tries to process more than one EOF.

0: Not try to process more than one EOF

1: Try to process more than one EOF

(RO)

**BITSCRAMBLER\_TX\_EOF\_TRACE\_CLR** Configures whether to clear [BITSCRAMBLER\\_TX\\_EOF\\_OVERLOAD](#) and [BITSCRAMBLER\\_TX\\_EOF\\_GET\\_CNT](#).

0: Not clear

1: Clear

(WT)

Register 54.15. BITSCRAMBLER\_RX\_STATE\_REG (0x0034)

|   |    |    |                            |  |  |  |  |  |  |  |  |  |  |   |            |   |   |   |   |  |   |   |   |   |   |   |   |   |   |       |
|---|----|----|----------------------------|--|--|--|--|--|--|--|--|--|--|---|------------|---|---|---|---|--|---|---|---|---|---|---|---|---|---|-------|
| BITSRAMBLER_RX_EOF_TRACE_CLR<br>BITSRAMBLER_RX_EOF_OVERLOAD |    |    | BITSRAMBLER_RX_EOF_GET_CNT |  |  |  |  |  |  |  |  |  |  |   | (reserved) |   |   |   |   | BITSRAMBLER_RX_FIFO_FULL<br>BITSRAMBLER_RX_IN_PAUSE<br>BITSRAMBLER_RX_IN_WAIT<br>BITSRAMBLER_RX_IN_RUN<br>BITSRAMBLER_RX_IN_IDLE |   |   |   |   |   |   |   |   |   |       |
| 31  | 30 | 29 | 16                         |  |  |  |  |  |  |  |  |  |  |   | 15         | 5 |   |   |   |  | 4 | 3 | 2 | 1 | 0 |   |   |   |   |       |
| 0   | 0  | 0  |                            |  |  |  |  |  |  |  |  |  |  | 0 | 0          | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Reset |

**BITSCRAMBLER\_RX\_IN\_IDLE** Represents whether BitScrambler TX core is halted.

0: Not halted

1: Halted

(RO)

**BITSCRAMBLER\_RX\_IN\_RUN** Represents whether BitScrambler TX core is running.

0: Not running

1: Running

(RO)

**BITSCRAMBLER\_RX\_IN\_WAIT** Represents whether BitScrambler TX core is waiting for write back done.

0: Not waiting

1: Waiting

(RO)

**BITSCRAMBLER\_RX\_IN\_PAUSE** Represents whether BitScrambler TX core is paused.

0: Not paused

1: Paused

(RO)

**BITSCRAMBLER\_RX\_FIFO\_FULL** Represents whether BitScrambler RX FIFO is full.

0: Not full

1: Full

(RO)

**BITSCRAMBLER\_RX\_EOF\_GET\_CNT** Represents byte count of BitScrambler TX core after EOF is received. (RO)

**BITSCRAMBLER\_RX\_EOF\_OVERLOAD** Represents whether BitScrambler RX core tries to process more than one EOF.

0: Not try to process more than one EOF

1: Try to process more than one EOF

(RO)

**BITSCRAMBLER\_RX\_EOF\_TRACE\_CLR** Configures whether to clear [BITSRAMBLER\\_RX\\_EOF\\_OVERLOAD](#) and [BITSRAMBLER\\_RX\\_EOF\\_GET\\_CNT](#).

0: Not clear

1: Clear

(WT)

Register 54.16. BITSCRAMBLER\_VERSION\_REG (0x00FC)



**BITSCRAMBLER\_BITSCRAMBLER\_VER** Version control register. (R/W)

## Part VIII

# Analog Signal Processing

This part describes components related to analog-to-digital conversion, voltage comparison, on-chip sensors, and features such as temperature and touch sensing, demonstrating the system's capabilities in handling analog signals.

## Chapter 55

### Touch Sensor (TOUCH)

ESP32-P4 has 14 capacitive touch sensor units, each of which can be connected to an external touch panel via a touch pin (GPIO pin) to constitute a touch sensor system. The ESP32-P4 touch sensor system is mainly used in human-computer interactions to detect finger touch or proximity. It also features moisture resistance and waterproof design.

#### 55.1 Terminology

To better illustrate the functions of capacitive touch sensors, the following terms are used in this section.

|                            |  |
|----------------------------|--|
| <b>Touch Sensor</b>        | Touch-related internal sensing circuitry.  |
| <b>Touch Pin</b>           | Pins with touch sensing feature.   |
| <b>Touch Panel</b>         | The external device connected to touch sensor via channel (touch pin) to detect finger touch.    |
| <b>Touch Sensor System</b> | Capacitive touch sensing system, consisting of touch sensor, touch pin, traces, and touch panel. |

**Note:**

In subsequent description, “touch panel is sampled/scanned/measured” indicates the same action to touch pin, i.e. “touch pin is sampled/scanned/measured”.

#### 55.2 Feature List

The ESP32-P4 touch sensor has the following features:

- Detection of 14 capacitive touch pins
- Sampling triggered by software or dedicated hardware timer
- Two sampling methods:
  - Pulses from the touch pins used as clock signals to count the sampling period
  - Pulses from the touch pins used as digital signals; sample the rising edge of the digital signal with the system clock to count the sampling period
- Scan mode, supporting sequential sampling of multiple touch pins by configuring the Touch FSM.
- Timeout mechanism to monitor channel abnormality
- Frequency hopping to increase the anti-interference of detection
- Proximity sensing mode with up to three configurable channels

- Configuration of individual touch sensors to operate normally in sleep mode
- Wake-up by touch sensor
- Moisture resistance
- Waterproof design

## 55.3 Architectural Overview

### 55.3.1 Touch Panel

A touch panel consists of the following components:

- Electrode: Changes in capacitance when touched by a finger.
- Substrate: The base material on which the protective cover, electrode, and the electrode's connector to the channel are built.
- Protective cover: To physically separate the other components from the external environment.

When developing applications using the touch sensing feature, users should decide on the placement, the material, or the arrangement of the touch panels during mechanical design. For more information about the design guidelines, please refer to [Touch Sensor Application Note](#). Touch panel can be connected to ESP32-P4 touch sensor via touch pin (channel). See Figure 55.3-1.

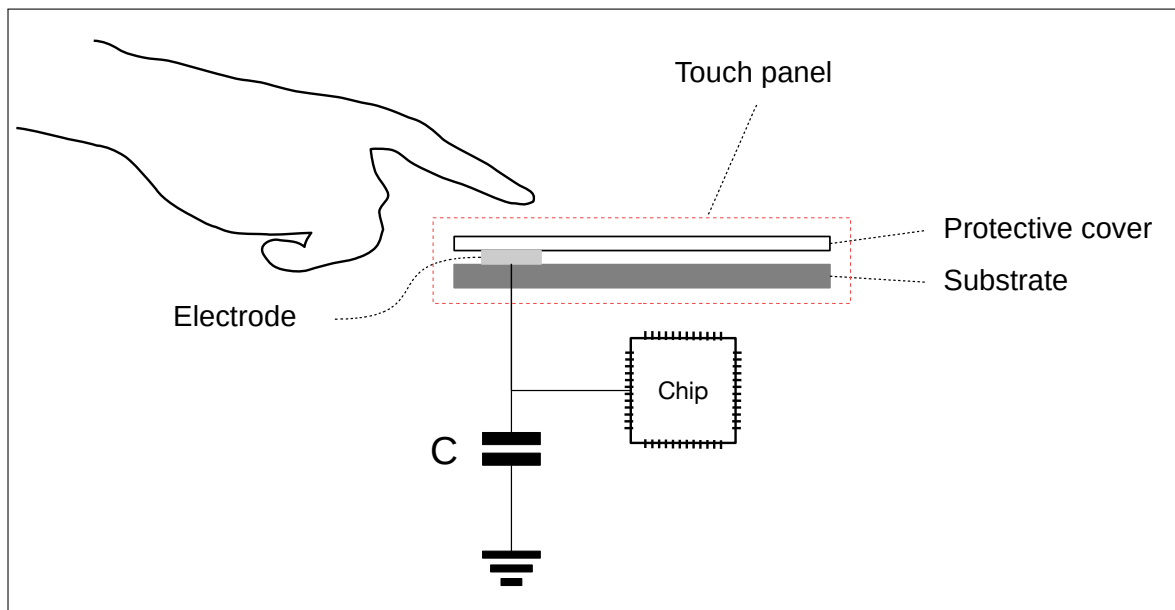


Figure 55.3-1. Touch Sensor System

When users touch the protective cover, the capacitance of the electrode increases. If the electrode is connected to one of the ESP32-P4 touch sensors via a channel, the touch sensor will be able to detect the electrode's change in capacitance. If the change of capacitance exceeds the configurable threshold, the touch sensor will trigger an interrupt.

### 55.3.2 Capacitive Touch Pin

ESP32-P4 provides 14 capacitive touch pins labeled as T1 ~ T14, each connected to the chip's pin to monitor finger touch from the external environment. The mapping between the touch sensors and the chip pins is shown in Table 55.3-1.

Table 55.3-1. ESP32-P4 Capacitive Touch Pins

| Capacitive Touch Pin | Connected GPIO Pin |
|----------------------|--------------------|
| T1                   | GPIO2              |
| T2                   | GPIO3              |
| T3                   | GPIO4              |
| T4                   | GPIO5              |
| T5                   | GPIO6              |
| T6                   | GPIO7              |
| T7                   | GPIO8              |
| T8                   | GPIO9              |
| T9                   | GPIO10             |
| T10                  | GPIO11             |
| T11                  | GPIO12             |
| T12                  | GPIO13             |
| T13                  | GPIO14             |
| T14                  | GPIO15             |

### 55.3.3 Touch Sensor

The touch sensor charges and discharges the touch pin with a fixed current source, and each charge and discharge generates a pulse signal, the TOUCH\_OUT signal. The touch sensor detects the capacitance change of the touch pin. If the touch pin is touched or approached by a finger, the touch pin's capacitance increases and the charging and discharging time is extended. By measuring the time required for charging and discharging the touch pin a fixed number of times, it can be inferred whether the touch pin has been touched or not.

Figure 55.3-2 illustrates the internal structure of the touch sensors. Each of the touch sensors has a set of input and output signals, some of which are connected to the Touch FSM (see Section 55.4.1). Table 55.3-2 shows the output signals of the touch sensor and their functions.

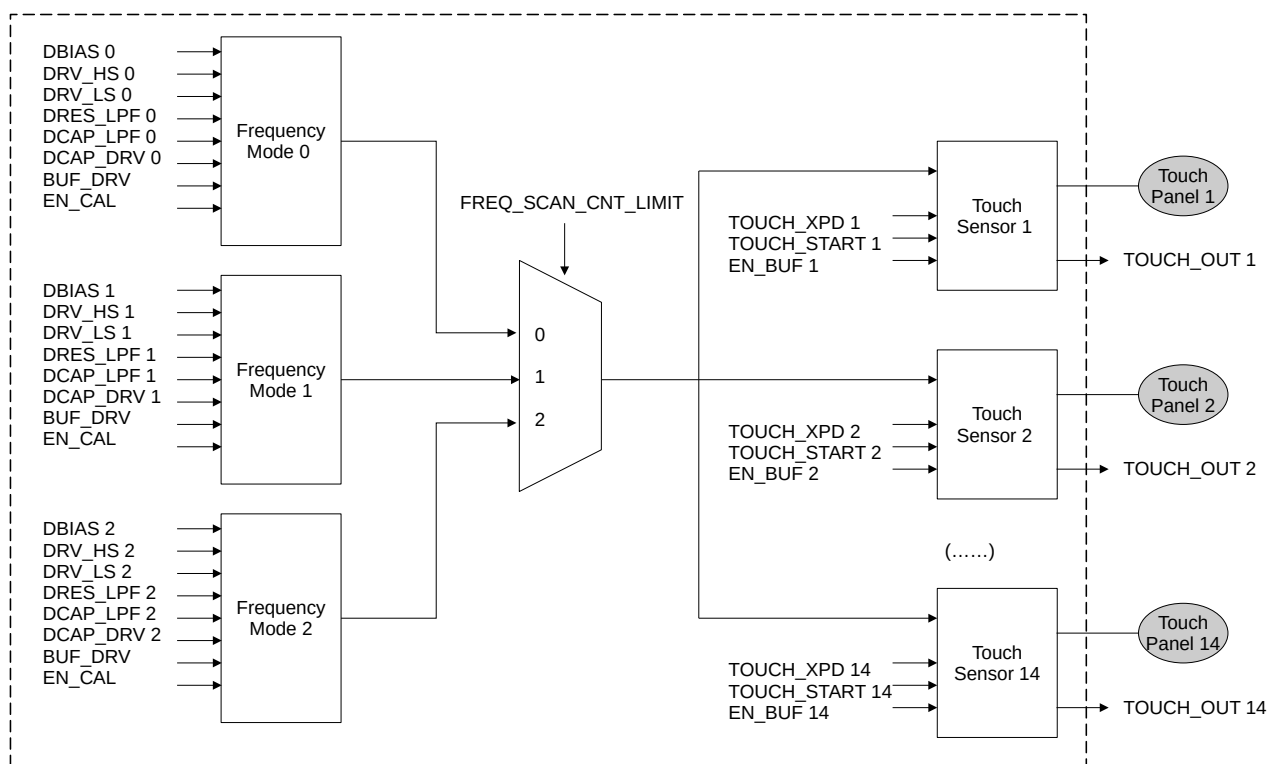


Figure 55.3-2. Touch Sensor Internal Structure

Table 55.3-2. Capacitive Touch Sensor Output Signal

| Signal      | Source    | Function   |
|-------------|-----------|--|
| TOUCH_XPD   | Touch FSM | Controls the power-up and power-down of the touch sensor   |
| TOUCH_START | Touch FSM | Controls the touch sensor to initiate a measurement. The measurement ends when the Touch FSM pulls down the TOUCH_START signal   |
| DBIAS       | Touch FSM | The FSM selects different DBIAS based on the frequency mode to adjust the voltage of the touch sensor's internal LDO, which affects the charging and discharging speed of the touch sensor   |
| DRV_HS      | Touch FSM | The FSM selects different DRV_HS based on the frequency mode to adjust the high-speed driving capability of the touch sensor   |
| DRV_LS      | Touch FSM | The FSM selects different DRV_LS based on the frequency mode to adjust the low-speed driving capability of the touch sensor  |
| DRES_LPF    | Touch FSM | The FSM selects different DRES_LPF based on the frequency mode to adjust the RC low-pass filter, which can be configured as 0 k $\Omega$ , 3 k $\Omega$ , 4.5 k $\Omega$ , or 7.5 k $\Omega$ |
| DCAP_LPF    | Touch FSM | The FSM selects different DCAP_LPF based on the frequency mode to adjust the RC low-pass filter with an adjustment range of 0-2.54 pF and a step of 20 fF                                    |
| DCAP_DRV    | Touch FSM | Used to adjust the internal capacitance connected to touch channels during measurement, usually set to 0   |
| EN_CAL      | Touch FSM | Used to disconnect from the touch pins and to test the capacitance in the touch sensor (the touch panel needs to be disabled)  |



| Signal    | Source       | Function  |
|-----------|--------------|---|
| BUF_DRV   | Touch FSM    | Adjusts the driving capability of TOUCH_BUFF  |
| EN_BUF    | Touch FSM    | Enables TOUCH_BUFF, a software-configurable touch panel, to mitigate the effects of water droplets on the sensor for moisture tolerance |
| TOUCH_OUT | Touch sensor | The Touch FSM counts the pulses in the TOUCH_OUT signal and measures the time it takes to generate N pulses                             |

## 55.4 Functional Description

### 55.4.1 Touch FSM

The Touch FSM performs a measurement by selecting a touch sensor and controlling the necessary signals to and from a touch sensor. Figure 55.4-1 shows the internal structure and operating mechanism of the Touch FSM. The Touch FSM is clocked by LP\_DYN\_FAST\_CLK. For more information on LP\_DYN\_FAST\_CLK, see Chapter 9 *Reset and Clock*.

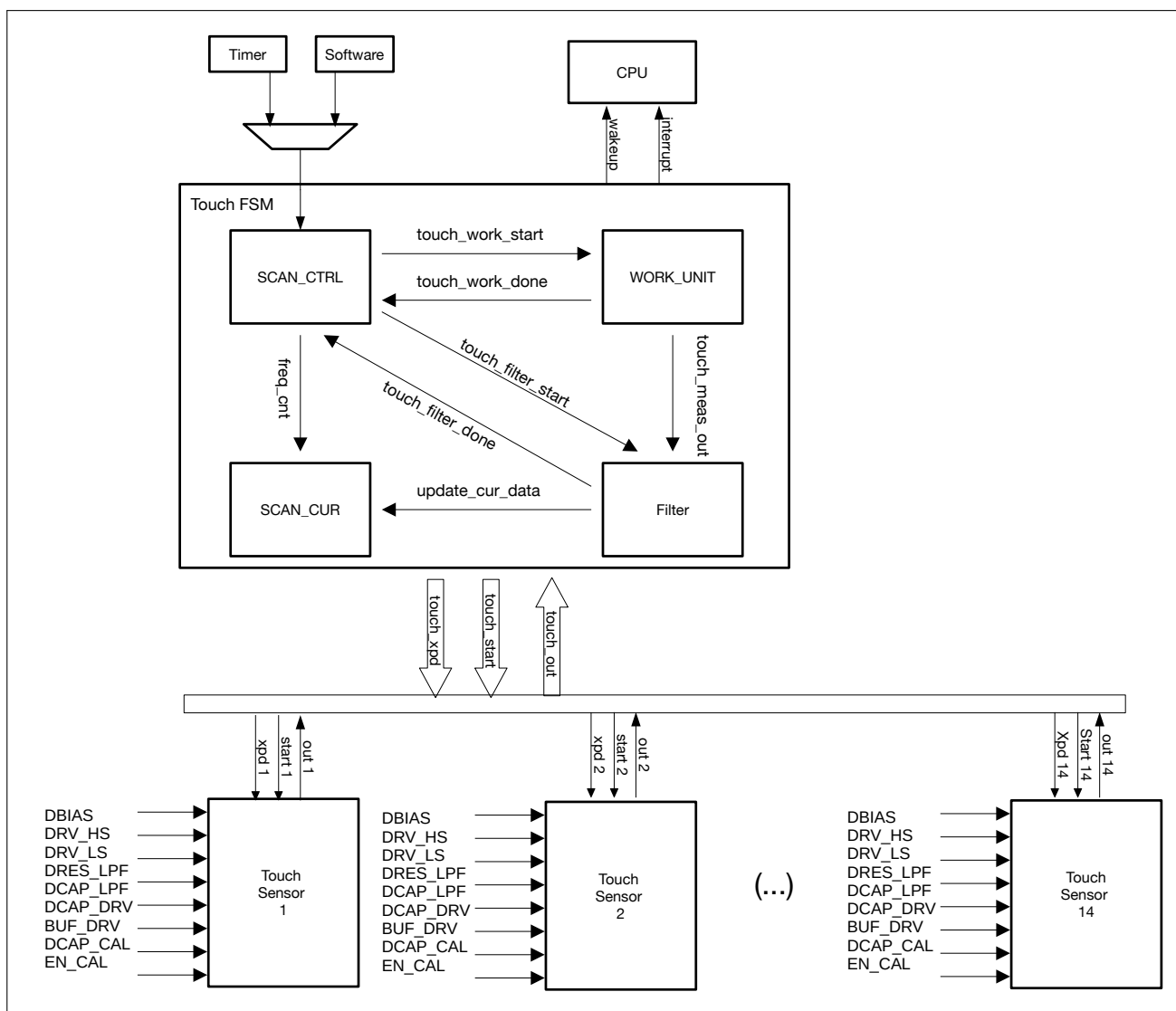


Figure 55.4-1. Touch FSM Structure and Mechanism

The following introduces the modules in the Touch FSM.

- **SCAN\_CTRL**: Select the touch pin to measure, set the parameters such as hopping frequency, and controls the start and end of measurement for each touch sensor in scan mode.
- **WORK\_UNIT**: Sample the selected touch sensors during a measurement.
- **Filter**: If enabled, each touch sensor can filter a series of measurements via an infinite impulse response (IIR) filter. The filtered value will be returned as the sampled value. See Section 55.4.3.1 for details.
- **SCAN\_CUR**: Cache the parameters of different touch sensors at different frequency modes during the measurement to be used for the next measurement.

## 55.4.2 Sampled Signal Preprocessing

The core mechanism of the touch sensor is to reflect whether the touch panel is touched or not based on the change of the output pulse wave, i.e., the TOUCH\_OUT signal, through detecting the change of capacitance on the touch panel. Therefore, the sampling of the TOUCH\_OUT signal is critical. Figure 55.4-2 shows the preprocessing of the TOUCH\_OUT signal.

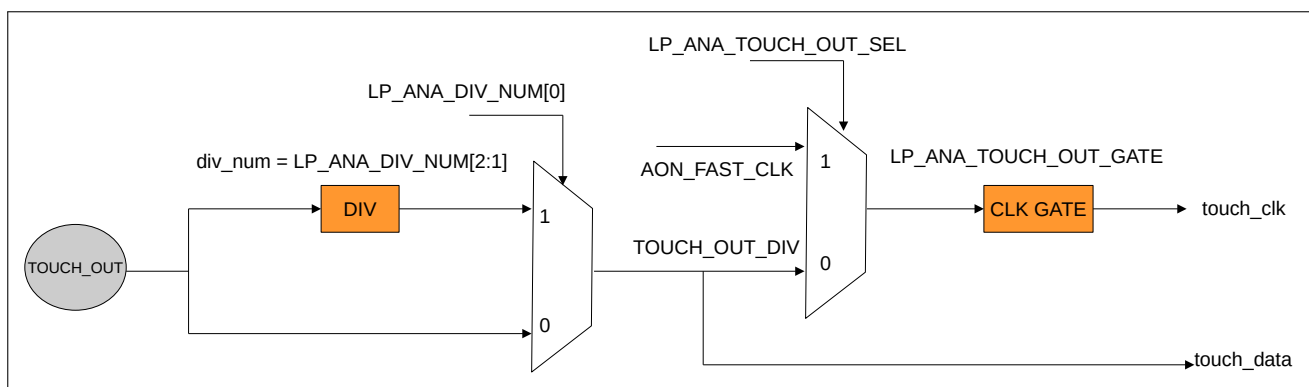


Figure 55.4-2. TOUCH\_OUT Signal Preprocessing

The frequency of TOUCH\_OUT might be much higher than the sampling frequency. Therefore, in order to improve the accuracy of the signal sampling, users can divide the TOUCH\_OUT signal by configuring `LP_ANA_DIV_NUM $n$` .  $n$  in this field represents different frequency modes in frequency hopping (refer to Section 55.4.2.4) with the value 0-2. The lowest bit configures whether to enable or disable frequency division. Set the lowest bit to 0 to disable frequency division, and set it to 1 to enable division. The highest two bits indicate the frequency division coefficient with a value of 0/1/2/3, corresponding to the 0/2/4/6 divisions.

If the frequency is still higher than twice the sampling frequency after frequency division, set `LP_ANA_TOUCH_OUT_SEL` to 1 to directly use the divided TOUCH\_OUT signal as a clock. Set `LP_ANA_TOUCH_OUT_GATE` to configure whether to enable this clock.

### 55.4.2.1 Measurement Process

Depending on whether frequency hopping is enabled, a measurement of a touch pin can be divided into the following two processes:

- Frequency hopping not enabled:

1. The Touch FSM selects the touch sensor to be measured. The relevant signals are routed to that touch sensor.
  2. The Touch FSM drives the START signal to the touch sensor to initiate the measurement. Internally, the Touch FSM starts a touch counter to time the duration of the measurement.
  3. A pulse counter in the Touch FSM is incremented on each pulse received from the touch sensor's TOUCH\_OUT signal.
  4. When the pulse counter reaches the count threshold set in [LP\\_ANA\\_TOUCH\\_MEAS\\_NUM0](#), the measurement is complete. The START signal is de-asserted, and the touch counter is stopped. The value of the stopped touch counter x LP\_DYN\_SLOW\_CLK cycles indicates the time taken to charge and discharge the touch pin for [LP\\_ANA\\_TOUCH\\_MEAS\\_NUM0](#) cycles.
- Frequency hopping enabled:
    1. The Touch FSM selects the touch sensor to be measured. The relevant signals are routed to that touch sensor.
    2. Set [LP\\_ANA\\_FREQ\\_SCAN\\_EN](#) to 1 to enable frequency hopping, configure [LP\\_ANA\\_FREQ\\_SCAN\\_CNT\\_LIMIT](#) to set the number of frequency modes supported for frequency hopping (up to three), and configure the parameters required for each frequency mode and the number of pulses for sampling the TOUCH\_OUT signal.
    3. The Touch FSM drives the START signal to the touch sensor to initiate the measurement. Internally, the Touch FSM starts a touch counter to time the duration of the measurement.
    4. A pulse counter in the Touch FSM is incremented on each pulse received from the touch sensor's TOUCH\_OUT signal.
    5. When the pulse counter reaches the count threshold set in [LP\\_ANA\\_TOUCH\\_MEAS\\_NUM0](#) of the corresponding frequency mode, the measurement is complete. The value of the stopped touch counter indicates the time taken to charge and discharge the touch pin [LP\\_ANA\\_TOUCH\\_MEAS\\_NUM0](#) cycles with the current frequency.
    6. The sampling frequency counter is incremented by 1 and the touch counter is cleared. The next frequency mode will be sampled after a small delay. When the samplings are finished for all frequency modes, the START signal is de-asserted, and the touch counter is cleared.

The sampled value (measured value) is the value of the touch counter indicated as touch\_raw\_data. The value of touch\_raw\_data can be read from [RTC\\_TOUCH\\_PADn\\_DATA](#). Note that the value returned by [RTC\\_TOUCH\\_PADn\\_DATA](#) may also be the filtered touch\_raw\_data, i.e., touch\_smooth\_data and benchmark. Configure [LP\\_ANA\\_TOUCH\\_DATA\\_SEL](#) and [LP\\_ANA\\_TOUCH\\_FREQ\\_SEL](#) to select the type of the return value. For more information on the sampled value types and how to judge touch actions based on the data, refer to Section [55.4.3.1](#).

**Note:**

Note that if the pulse does not reach the set threshold for a long time while the touch counter has reached the timeout threshold set in [LP\\_ANA\\_TOUCH\\_TIMEOUT\\_NUM](#) with [LP\\_ANA\\_TOUCH\\_TIMEOUT\\_EN](#) set as 1, the [RTC\\_TOUCH\\_TIMEOUT\\_INT\\_RAW](#) timeout interrupt will be triggered, indicating a circuit abnormality.

### 55.4.2.2 Trigger Source of Measurement

The Touch FSM initiates a measurement by sending a START signal. The START signal can either be triggered by software, or by a dedicated hardware timer known as the “touch timer”. The use of a touch timer allows periodic measurements to be taken without software intervention.

The touch timer is clocked by LP\_DYN\_SLOW\_CLK and should be configured with a period in number of LP\_DYN\_SLOW\_CLK cycles. The START signal is generated when the touch timer expires. The touch timer is reset when the measurement completes and restarts counting until the next expiration.

- To trigger the START signal by software:
  - Set [LP\\_ANA\\_TOUCH\\_START\\_FORCE](#) to 1 to trigger the START signal by software.
  - Software sets [LP\\_ANA\\_TOUCH\\_START\\_EN](#) to 1 and generates the START signal to initiate a measurement.
- To trigger the START signal by the touch timer:
  - Clear [LP\\_ANA\\_TOUCH\\_START\\_FORCE](#).
  - Configure the wait time before the timer sends the START signal (unit: LP\_DYN\_SLOW\_CLK cycle) via [PMU\\_TOUCH\\_WAIT\\_CYCLES](#).
  - Configure the wait time after the timer receives the DONE signal upon the completion of the touch sensor sampling (unit: LP\_DYN\_SLOW\_CLK cycle) via [PMU\\_TOUCH\\_SLEEP\\_CYCLES](#).
  - Set [PMU\\_TOUCH\\_SLEEP\\_TIMER\\_EN](#) to 1 to enable the touch timer.
- To force exit the current measurement cycle of the touch timer by software, there are two approaches:
  1. Generate the end signal of the touch sensor to exit the current measurement cycle of the touch timer.
    - Set [LP\\_ANA\\_TOUCH\\_DONE\\_FORCE](#) to 1 to select the DONE signal to be triggered by software.
    - Software sets [LP\\_ANA\\_TOUCH\\_DONE\\_EN](#) to 1 to generate the DONE signal to end a measurement.
  2. Use the software to directly force the touch timer to exit the current measurement cycle.
    - Set [PMU\\_TOUCH\\_FORCE\\_DONE](#) to generate the DONE signal and force the touch timer to exit the current measurement cycle.

**Note:**

The touch timer waits for a period of time before generating the START signal and after receiving the DONE signal, so the interval between two consecutive measurements is ([PMU\\_TOUCH\\_WAIT\\_CYCLES](#) + [PMU\\_TOUCH\\_SLEEP\\_CYCLES](#)) and the timing clock is LP\_DYN\_SLOW\_CLK.

### 55.4.2.3 Scan Mode

Scan mode involves the Touch FSM taking measurements of multiple touch sensors in sequential order. On every START signal, a new touch sensor is selected for measurement, thus allowing multiple touch pins to be monitored. The scan process is illustrated in Figure 55.4-3.

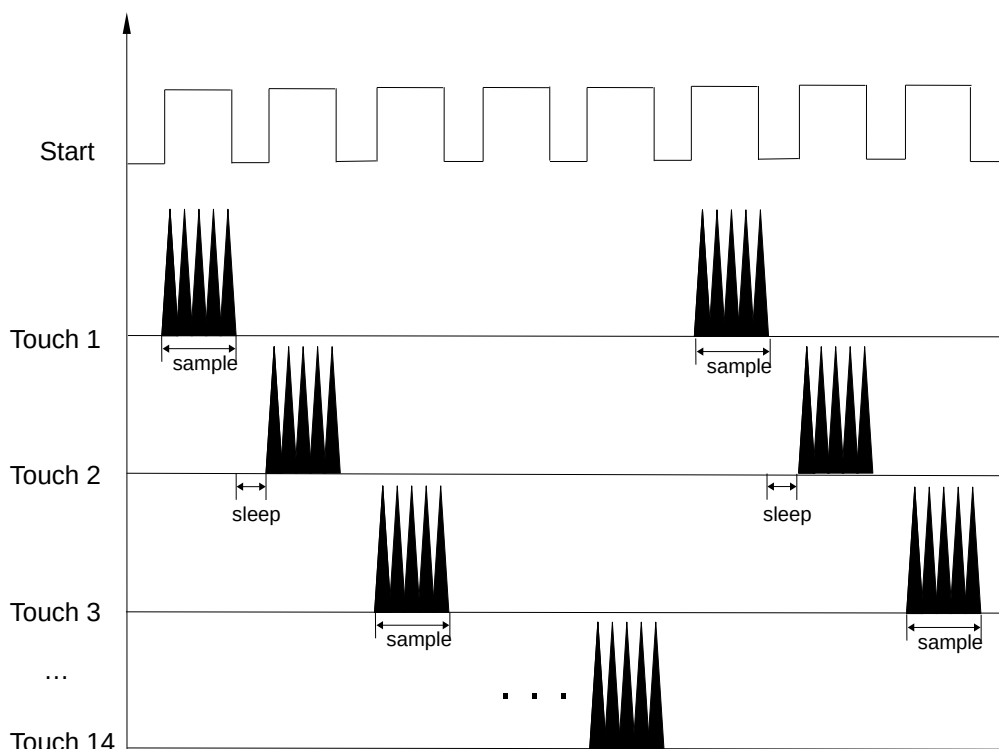


Figure 55.4-3. Timing Diagram of Scan Mode

To enable the scan mode, specify the bit map of the enabled touch pins in [LP\\_ANA\\_TOUCH\\_SCAN\\_PAD\\_MAP](#). The Touch FSM will select one touch pin from the bit map of the enabled touch pins in turn to measure per START signal, i.e., only one measurement is conducted per START signal. As multiple START signals are generated, the Touch FSM will cycle through the enabled touch pins in sequential order.

When measuring for different touch sensors, the sleep interval between two measurements is  $PMU\_TOUCH\_WAIT\_CYCLES + PMU\_TOUCH\_SLEEP\_CYCLES$  with the clock cycle of  $LP\_DYN\_SLOW\_CLK$ .

**Note:**

- After the touch sensor receives the START signal from the touch timer, it waits a short period before starting the measurement to ensure the stability of the sampling signal. The wait time is configured by [LP\\_ANA\\_TOUCH\\_XPD\\_WAIT](#). The timing clock is  $AON\_FAST\_CLK$ .
- If the touch timer is used to generate the START signal, the scanning can be conducted without software intervention.

#### 55.4.2.4 Frequency Hopping

When frequency hopping is enabled, the Touch FSM can measure the touch sensor at different frequency modes. Up to three frequency modes are supported, each corresponding to a set of configuration parameters. When a START signal is generated, the measurement will be carried out for each frequency mode sequentially, and the DONE signal will be generated when the measurements are completed for all frequency modes. Frequency hopping can be enabled together with the scan mode. In such case, users can monitor the touch condition of multiple touch sensors under different frequency modes by generating multiple START

signals. The scanning process is shown in Figure 55.4-4.

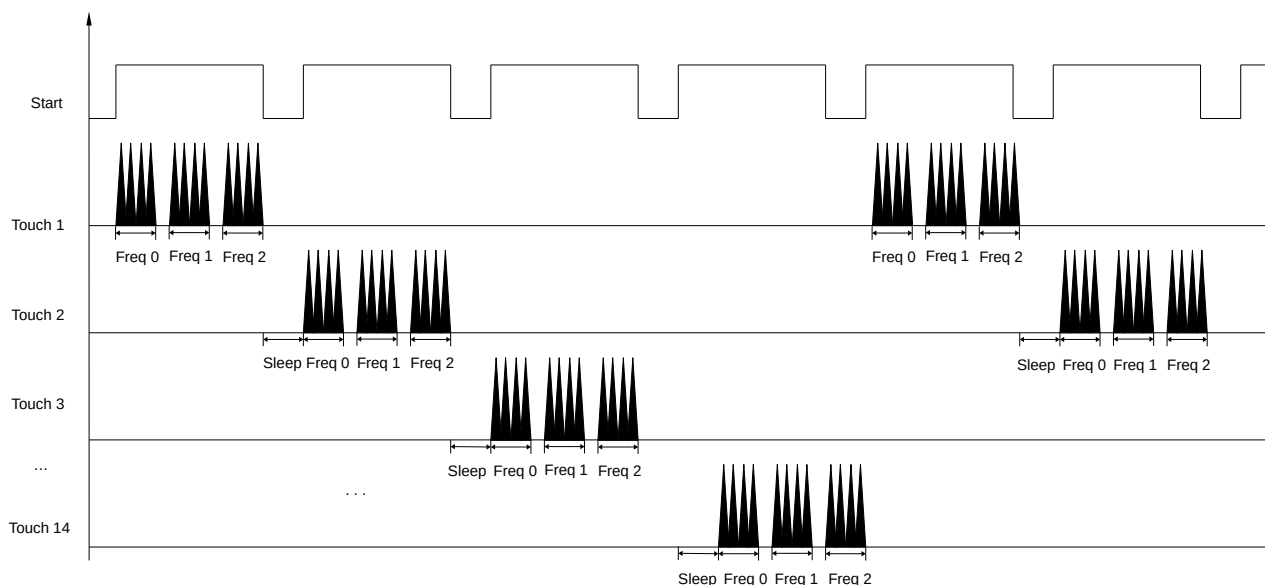


Figure 55.4-4. Touch Sensor Frequency Hopping Sequence Timing

Set `LP_ANA_FREQ_SCAN_EN` to 1 to enable frequency hopping, configure `LP_ANA_FREQ_SCAN_CNT_LIMIT` to select the maximum number of frequency mode supported, and configure the following analog parameter registers to adjust the sampling performance of the touch sensor at different frequency modes:

- `LP_ANA_TOUCH_FREQ $n$ _DBIAS` ( $n = 0-2$ )
- `LP_ANA_TOUCH_FREQ $n$ _DRV_HS` ( $n = 0-2$ )
- `LP_ANA_TOUCH_FREQ $n$ _DRV_LS` ( $n = 0-2$ )
- `LP_ANA_TOUCH_FREQ $n$ _DRES_LPF` ( $n = 0-2$ )
- `LP_ANA_TOUCH_FREQ $n$ _DCAP_LPF` ( $n = 0-2$ )

Upon each START signal, the Touch FSM measures consecutively for frequency mode 0, 1, and 2. A START signal triggers a maximum of three measurement operations. When the measurements are completed for all frequency modes, the START signal is de-asserted until the next measurement. Therefore, the Touch FSM performs measurements on the enabled touch sensors in sequence upon multiple START signals.

**Note:**

- When the same touch sensor is measured at different frequency modes, the wait time between measurements can be configured by `LP_ANA_TOUCH_XPD_WAIT` (count clock: `AON_FAST_CLK`).
- After receiving the START signal from the touch timer, the touch sensor waits for a short period of time before starting measuring to ensure the stability of the sampling signal. The wait time can be configured by `LP_ANA_TOUCH_XPD_WAIT` (count clock: `AON_FAST_CLK`).
- If a touch timer is used to generate the START signal, the scanning can be conducted without software intervention.

## 55.4.3 Touch Detection

### 55.4.3.1 Sampled Value

As introduced in Section 55.4.2.1, the sampled value of a measurement can be read from [RTC\\_TOUCH\\_PAD \$n\$ \\_DATA](#). However, the specific type of sampled value stored in [RTC\\_TOUCH\\_PAD \$n\$ \\_DATA](#) is determined together by [LP\\_ANA\\_TOUCH\\_DATA\\_SEL](#) and [LP\\_ANA\\_TOUCH\\_FREQ\\_SEL](#). The following three sampled value types are supported:

1. **touch\_raw\_data**: When the measurement is completed, the touch counter's value indicates the time taken to charge and discharge the touch pin a fixed number of times in LP\_DYN\_SLOW\_CLK cycles. After the IIR filter is turned on, the data is the filtered data.
2. **touch\_smooth\_data**: A series of moving averages generated by the touch\_raw\_data values sampled from a single touch sensor filtered by an IIR filter.

touch\_smooth\_data is less prone to noise spikes or outlier samples, thus often used for hardware touch detection. If frequency hopping is enabled, each touch pin will have a separate set of smooth\_touch\_data at different frequency modes and do not affect each other. The IIR filter that generates touch\_smooth\_data is configured via [LP\\_ANA\\_TOUCH\\_SMOOTH\\_LVL](#). See Table 55.4-1 for more information.

Table 55.4-1. touch\_smooth\_data Calculation

| <a href="#">LP_ANA_TOUCH_SMOOTH_LVL</a> | Type    | Formula  |
|---|---------|--|
| 0                                       | —       | touch_raw_data   |
| 1                                       | IIR 1/2 | $1/2 \text{ touch\_raw\_data} + 1/2 \text{ touch\_smooth\_data}$ |
| 2                                       | IIR 1/4 | $1/4 \text{ touch\_raw\_data} + 3/4 \text{ touch\_smooth\_data}$ |
| 3                                       | IIR 1/8 | $1/8 \text{ touch\_raw\_data} + 7/8 \text{ touch\_smooth\_data}$ |

3. **benchmark**: Also generated from the touch\_raw\_data values by IIR filtering. However, the moving average window for benchmark is much wider.

The benchmark value is usually used to represent the stable reading of a touch pin without the effect from a touch action. The touch detection is based on the benchmark value. Each touch sensor has a separate set of benchmark values at different frequency modes with a default value of 0xFFFF. The IIR filter that generates benchmark is configured via [LP\\_ANA\\_TOUCH\\_FILTER\\_MODE](#). Refer to Table 55.4-2 for more information.

In addition to the IIR filtering, users can also update the benchmark value directly by software. Configure [LP\\_ANA\\_TOUCH\\_BENCHMARK\\_SW](#) and [LP\\_ANA\\_TOUCH\\_UPDATE\\_BENCHMARK\\_SW](#) sequentially to update the benchmark value. This is generally used for software debugging.

Table 55.4-2. benchmark Algorithm

| <a href="#">LP_ANA_TOUCH_FILTER_MODE</a> | Type     | Formula   |
|--|----------|---|
| 0  | IIR 1/4  | $1/4 \text{ touch\_raw\_data} + 3/4 \text{ benchmark}$    |
| 1  | IIR 1/8  | $1/8 \text{ touch\_raw\_data} + 7/8 \text{ benchmark}$    |
| 2  | IIR 1/16 | $1/16 \text{ touch\_raw\_data} + 15/16 \text{ benchmark}$ |
| 3  | IIR 1/32 | $1/32 \text{ touch\_raw\_data} + 31/32 \text{ benchmark}$ |

Table 55.4-2. benchmark Algorithm

| LP_ANA_TOUCH_FILTER_MODE | Type      | Formula   |
|--------------------------|-----------|---|
| 4                        | IIR 1/64  | $1/64 \text{ touch\_raw\_data} + 63/64 \text{ benchmark}$         |
| 5                        | IIR 1/128 | $1/128 \text{ touch\_raw\_data} + 127/128 \text{ benchmark}$      |
| 6                        | IIR 1/256 | $1/256 \text{ touch\_raw\_data} + 255/256 \text{ benchmark}$      |
| 7                        | JITTER    | $\text{touch\_raw\_data} \pm \text{LP\_ANA\_TOUCH\_JITTER\_STEP}$ |

### 55.4.3.2 Hardware Touch Detection

In hardware touch detection, the touch sensor can detect finger touch or release and trigger an interrupt. To use hardware touch detection, the following key parameters need to be defined:

- **finger\_threshold:** The threshold value used to determine a touch or a touch interruption. `finger_threshold` is configured via `LP_ANA_TOUCH_PADx_THy`, where `x` (1-14) represents the touch pin index and `y` (0-2) represents the frequency mode configured in hopping frequency.
- **noise\_threshold:** Indicates the maximum threshold of the upward and downward fluctuation of `touch_smooth_data`. `noise_threshold` is configured via `LP_ANA_TOUCH_NOISE_THRES`.
- **hysteresis:** Used to avoid touch misjudgments caused by fluctuations of `touch_smooth_data` around touch thresholds. The hysteresis value is configured via `LP_ANA_TOUCH_HHYSTERESIS`.

The `finger_threshold` and `noise_threshold` values are not absolute thresholds, but offsets from the benchmark value, while the hysteresis value is an offset from `finger_threshold`. This prevents from misdiagnosing the gradual or slow changes of `touch_raw_data` caused by environmental factors such as temperature, power, or noise as a touch action.

After a series of calculations and comparisons based on the above parameters, the touch sensor will output the touch results detected on the touch pins via interrupts. Each touch sensor corresponds to a control register `LP_ANA_TOUCH_OUTEN` to configure whether to output the detection result.

### 55.4.4 Proximity Mode

When an object such as a finger is close to, but not touching, a touch pin, a small change in capacitance occurs on the touch pin, which is much smaller than the change caused by a physical touch. Proximity mode allows for the detection of these small changes.

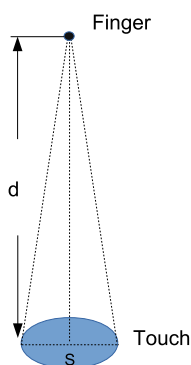


Figure 55.4-5. Sensing Area



- The maximum detection distance “d” is 16 cm and the sensing area “S” is 20 cm<sup>2</sup>, where “d” is positively correlated with “S” as shown in Figure 55.4-5.
- Up to three touch pins can be configured to operate simultaneously in proximity mode.
- Frequency hopping is also supported in proximity mode.

In proximity mode, a touch sensor samples for a fixed number of times and accumulates the sample values. If the final cumulative value exceeds the configured threshold, a proximity object is considered to be detected and an interrupt will be triggered. Note that since the sample values are accumulated, the values introduced in Section 55.4.3.1, i.e., touch\_raw\_data, touch\_smooth\_data, and benchmark, will not be generated in proximity mode.

To operate in proximity mode:

- Configure a touch sensor to operate in proximity mode by setting [LP\\_ANA\\_TOUCH\\_APPROACH\\_PADO](#), [LP\\_ANA\\_TOUCH\\_APPROACH\\_PAD1](#), or [LP\\_ANA\\_TOUCH\\_APPROACH\\_PAD2](#).
- Configure [LP\\_ANA\\_TOUCH\\_APPROACH\\_LIMIT](#) to adjust the number of samplings to generate the cumulative value. The touch sensor contains an internal sample counter to record the number of samplings.
- Set the threshold value via [LP\\_ANA\\_TOUCH\\_PADx\\_THy](#), where **x** (1-14) represents the touch pin index and **y** (0-2) represents the frequency mode configured in hopping frequency.
- When the sample counter reaches the number of samplings configured in [LP\\_ANA\\_TOUCH\\_APPROACH\\_MEAS\\_NUMn](#):
  - If the cumulative value exceeds the threshold value, an interrupt will be triggered.
  - The sample counter and the cumulative value are reset to 0. The touch sensor restarts accumulating the sample values.

### 55.4.5 Sleep Mode

To reduce power consumption, the touch sensor also supports sleep mode. In sleep mode, users can designate one touch sensor to operate actively (hereinafter referred to as the sleeping touch sensor) to monitor whether a touch occurs in real time, while the remaining 13 touch sensors are all powered down in sleep mode. Once the sleeping touch sensor detects a touch or a touch release, it will generate an interrupt to wake up the rest of the touch sensors. The sleeping touch sensor also supports frequency hopping and proximity mode. There is a separate set of threshold parameters for the sleeping touch sensor, which can be configured as follows:

- Configure [LP\\_ANA\\_TOUCH\\_SLP\\_PAD](#) to select a particular touch sensor as the sleeping touch sensor.
- Configure [LP\\_ANA\\_TOUCH\\_SLP\\_TH0](#), [LP\\_ANA\\_TOUCH\\_SLP\\_TH1](#), and [LP\\_ANA\\_TOUCH\\_SLP\\_TH2](#) to set the touch threshold for the sleeping touch sensor at different frequency modes.
- Configure [LP\\_ANA\\_TOUCH\\_SLP\\_APPROACH\\_EN](#) to enable the proximity mode for the sleeping touch sensor.
- Configure [LP\\_ANA\\_TOUCH\\_SLP\\_CHANNEL\\_CLR](#) to clear the intermediate data for the sleeping touch sensor, such as benchmark, touch\_raw\_data, and the number of sampling.

**Note:**

The configuration for the noise\_threshold, hysteresis, touch\_smooth\_data, and benchmark values are the same for the sleeping touch sensor in sleep mode as in the normal mode.

## 55.4.6 Moisture Tolerance

If there are water droplets on the touch pads and the droplets are large enough to physically bridge two more adjacent touch pads, the adjacent touch pads may be electrically coupled. Coupled touch pads can cause false touch detection due to capacitance changes caused by the coupling. If a water droplet is connected across the touch pad and ground, a large parasitic capacitance will be introduced, also leading to false detection. The moisture tolerance feature can mitigate the impact of water droplets.

To configure moisture tolerance:

- Configure [LP\\_ANA\\_TOUCH\\_SHIELD\\_PAD\\_EN](#) to enable moisture tolerance.
- Configure [LP\\_ANA\\_TOUCH\\_BUFSEL](#) to select a touch pin to be used for moisture tolerance.

**Note:**

The moisture tolerance feature only works at frequencies below 10 MHz. Therefore, when the frequency is higher than 10 MHz, please disable the moisture tolerance feature.

## 55.4.7 Water Rejection

If the sensor array becomes wet, i.e., the majority of the sensor pads are soaked by water, most (if not all) of the touch pads will become unusable due to the possible false touch detections. ESP32-P4 supports the water rejection feature to shut down the sensor array if it is detected to be wet.

Configure [LP\\_ANA\\_TOUCH\\_OUT\\_RING](#) to select one of the touch pins to be used for the water rejection feature.

## 55.5 Interrupts

ESP32-P4's touch sensor can generate the LP\_TOUCH\_INTR signal that will be sent to the [Interrupt Matrix](#).

There are several internal interrupt sources from touch sensor that can generate the LP\_TOUCH\_INTR signal. The interrupt sources from touch sensor are listed with their trigger conditions and the resulted interrupt signal in Table [55.5-1](#).

Table 55.5-1. Touch Sensor's Internal Interrupt Sources

| Internal Interrupt Source    | Trigger Condition   | Interrupt Signal |
|------------------------------|---|------------------|
| TOUCH_APPROACH_LOOP_DONE_INT | Completion of proximity mode cumulative sampling  | LP_TOUCH_INTR    |
| TOUCH_TIMEOUT_INT            | Timeout for the TOUCH_OUT signal sampling   |                  |
| TOUCH_INACTIVE_INT           | Touch release detected  |                  |
| TOUCH_ACTIVE_INT             | Touch detected  |                  |
| TOUCH_DONE_INT               | Completion of sampling an individual touch pin at a certain frequency mode for comparison |                  |
| TOUCH_SCAN_DONE_INT          | Completion of sampling selected touch pins for comparison at all frequency modes          |                  |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [55.6 Register Summary](#).

## 55.6 Register Summary

### 55.6.1 Interrupt and Status Register Summary

The addresses in this section are relative to Touch Sensor base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                     | Description                            | Address | Access   |
|--|--|---------|----------|
| <b>Interrupt Register</b>                |  |         |          |
| <a href="#">RTC_TOUCH_INT_RAW_REG</a>    | Touch sensor interrupt raw register    | 0x0000  | R/SS/WTC |
| <a href="#">RTC_TOUCH_INT_ST_REG</a>     | Touch sensor interrupt status register | 0x0004  | RO       |
| <a href="#">RTC_TOUCH_INT_ENA_REG</a>    | Touch sensor interrupt enable register | 0x0008  | R/WTC    |
| <a href="#">RTC_TOUCH_INT_CLR_REG</a>    | Touch sensor interrupt clear register  | 0x000C  | WT       |
| <b>Status Register</b>                   |  |         |          |
| <a href="#">RTC_TOUCH_CHN_STATUS_REG</a> | Scan mode status register              | 0x0010  | RO       |
| <a href="#">RTC_TOUCH_STATUS_1_REG</a>   | Touch pin 1 status register            | 0x0018  | RO       |
| <a href="#">RTC_TOUCH_STATUS_2_REG</a>   | Touch pin 2 status register            | 0x001C  | RO       |
| <a href="#">RTC_TOUCH_STATUS_3_REG</a>   | Touch pin 3 status register            | 0x0020  | RO       |
| <a href="#">RTC_TOUCH_STATUS_4_REG</a>   | Touch pin 4 status register            | 0x0024  | RO       |
| <a href="#">RTC_TOUCH_STATUS_5_REG</a>   | Touch pin 5 status register            | 0x0028  | RO       |
| <a href="#">RTC_TOUCH_STATUS_6_REG</a>   | Touch pin 6 status register            | 0x002C  | RO       |
| <a href="#">RTC_TOUCH_STATUS_7_REG</a>   | Touch pin 7 status register            | 0x0030  | RO       |
| <a href="#">RTC_TOUCH_STATUS_8_REG</a>   | Touch pin 8 status register            | 0x0034  | RO       |
| <a href="#">RTC_TOUCH_STATUS_9_REG</a>   | Touch pin 9 status register            | 0x0038  | RO       |
| <a href="#">RTC_TOUCH_STATUS_10_REG</a>  | Touch pin 10 status register           | 0x003C  | RO       |
| <a href="#">RTC_TOUCH_STATUS_11_REG</a>  | Touch pin 11 status register           | 0x0040  | RO       |
| <a href="#">RTC_TOUCH_STATUS_12_REG</a>  | Touch pin 12 status register           | 0x0044  | RO       |
| <a href="#">RTC_TOUCH_STATUS_13_REG</a>  | Touch pin 13 status register           | 0x0048  | RO       |
| <a href="#">RTC_TOUCH_STATUS_14_REG</a>  | Touch pin 14 status register           | 0x004C  | RO       |
| <a href="#">RTC_TOUCH_STATUS_15_REG</a>  | Sleep mode touch pin status register   | 0x0050  | RO       |

| Name   | Description                       | Address | Access |
|--|-----------------------------------|---------|--------|
| <a href="#">RTC_TOUCH_STATUS_16_REG</a>      | Proximity mode status register    | 0x0054  | RO     |
| <a href="#">RTC_TOUCH_STATUS_17_REG</a>      | Frequency hopping status register | 0x0058  | RO     |
| <a href="#">RTC_TOUCH_CHN_TMP_STATUS_REG</a> | Touch status register             | 0x005C  | RO     |
| <b>Version Control Register</b>              |                                   |         |        |
| <a href="#">RTC_TOUCH_DATE_REG</a>           | Version control register          | 0x0100  | R/W    |

## 55.6.2 Configuration Register Summary

The addresses in this section are relative to LP Analog Peripheral base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name  | Description  | Address | Access |
|---|--|---------|--------|
| <b>Configuration Register</b>                           |  |         |        |
| <a href="#">LP_ANA_TOUCH_APPROACH_WORK_MEAS_NUM_REG</a> | Configuration register for the number of measurements in proximity mode        | 0x00FC  | R/W    |
| <a href="#">LP_ANA_TOUCH_SCAN_CTRL1_REG</a>             | Scan mode configuration register 1   | 0x0100  | R/W    |
| <a href="#">LP_ANA_TOUCH_SCAN_CTRL2_REG</a>             | Scan mode configuration register 2   | 0x0104  | R/W    |
| <a href="#">LP_ANA_TOUCH_WORK_REG</a>                   | Sample preprocessing register  | 0x0108  | varies |
| <a href="#">LP_ANA_TOUCH_WORK_MEAS_NUM_REG</a>          | Configuration register for number of measurements at different frequency modes | 0x010C  | R/W    |
| <a href="#">LP_ANA_TOUCH_FILTER1_REG</a>                | Touch detection configuration register 1                                       | 0x0110  | R/W    |
| <a href="#">LP_ANA_TOUCH_FILTER2_REG</a>                | Touch detection configuration register 2                                       | 0x0114  | R/W    |
| <a href="#">LP_ANA_TOUCH_FILTER3_REG</a>                | Touch detection configuration register 3                                       | 0x0118  | varies |
| <a href="#">LP_ANA_TOUCH_SLPO_REG</a>                   | Sleep mode configuration register 1  | 0x011C  | varies |
| <a href="#">LP_ANA_TOUCH_SLP1_REG</a>                   | Sleep mode configuration register 2  | 0x0120  | R/W    |
| <a href="#">LP_ANA_TOUCH_CLR_REG</a>                    | Status clear register  | 0x0124  | WT     |
| <a href="#">LP_ANA_TOUCH_APPROACH_REG</a>               | Proximity mode configuration register  | 0x0128  | R/W    |
| <a href="#">LP_ANA_TOUCH_FREQ0_SCAN_PARA_REG</a>        | Analog parameter configuration register for touch sensor for frequency mode 0  | 0x012C  | R/W    |
| <a href="#">LP_ANA_TOUCH_FREQ1_SCAN_PARA_REG</a>        | Analog parameter configuration register for touch sensor for frequency mode 1  | 0x0130  | R/W    |

| Name   | Description   | Address | Access |
|--|---|---------|--------|
| <a href="#">LP_ANA_TOUCH_FREQ2_SCAN_PARA_REG</a> | Analog parameter configuration register for touch sensor for frequency mode 2 | 0x0134  | R/W    |
| <a href="#">LP_ANA_TOUCH_ANA_PARA_REG</a>        | Touch sensor analog parameter configuration register                          | 0x0138  | R/W    |
| <a href="#">LP_ANA_TOUCH_MUX0_REG</a>            | DEBUG mode selection configuration register                                   | 0x013C  | R/W    |
| <a href="#">LP_ANA_TOUCH_MUX1_REG</a>            | DEBUG mode function configuration register                                    | 0x0140  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD1_TH0_REG</a>        | Touch threshold configuration register for touch pin 1 for frequency mode 0   | 0x0150  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD1_TH1_REG</a>        | Touch threshold configuration register for touch pin 1 for frequency mode 1   | 0x0154  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD1_TH2_REG</a>        | Touch threshold configuration register for touch pin 1 for frequency mode 2   | 0x0158  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD2_TH0_REG</a>        | Touch threshold configuration register for touch pin 2 for frequency mode 0   | 0x015C  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD2_TH1_REG</a>        | Touch threshold configuration register for touch pin 2 for frequency mode 1   | 0x0160  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD2_TH2_REG</a>        | Touch threshold configuration register for touch pin 2 for frequency mode 2   | 0x0164  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD3_TH0_REG</a>        | Touch threshold configuration register for touch pin 3 for frequency mode 0   | 0x0168  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD3_TH1_REG</a>        | Touch threshold configuration register for touch pin 3 for frequency mode 1   | 0x016C  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD3_TH2_REG</a>        | Touch threshold configuration register for touch pin 3 for frequency mode 2   | 0x0170  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD4_TH0_REG</a>        | Touch threshold configuration register for touch pin 4 for frequency mode 0   | 0x0174  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD4_TH1_REG</a>        | Touch threshold configuration register for touch pin 4 for frequency mode 1   | 0x0178  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD4_TH2_REG</a>        | Touch threshold configuration register for touch pin 4 for frequency mode 2   | 0x017C  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD5_TH0_REG</a>        | Touch threshold configuration register for touch pin 5 for frequency mode 0   | 0x0180  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD5_TH1_REG</a>        | Touch threshold configuration register for touch pin 5 for frequency mode 1   | 0x0184  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD5_TH2_REG</a>        | Touch threshold configuration register for touch pin 5 for frequency mode 2   | 0x0188  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD6_TH0_REG</a>        | Touch threshold configuration register for touch pin 6 for frequency mode 0   | 0x018C  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD6_TH1_REG</a>        | Touch threshold configuration register for touch pin 6 for frequency mode 1   | 0x0190  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD6_TH2_REG</a>        | Touch threshold configuration register for touch pin 6 for frequency mode 2   | 0x0194  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD7_TH0_REG</a>        | Touch threshold configuration register for touch pin 7 for frequency mode 0   | 0x0198  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD7_TH1_REG</a>        | Touch threshold configuration register for touch pin 7 for frequency mode 1   | 0x019C  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD7_TH2_REG</a>        | Touch threshold configuration register for touch pin 7 for frequency mode 2   | 0x01A0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD8_TH0_REG</a>        | Touch threshold configuration register for touch pin 8 for frequency mode 0   | 0x01A4  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD8_TH1_REG</a>        | Touch threshold configuration register for touch pin 8 for frequency mode 1   | 0x01A8  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD8_TH2_REG</a>        | Touch threshold configuration register for touch pin 8 for frequency mode 2   | 0x01AC  | R/W    |

| Name                                       | Description  | Address | Access |
|--|--|---------|--------|
| <a href="#">LP_ANA_TOUCH_PAD9_TH0_REG</a>  | Touch threshold configuration register for touch pin 9 for frequency mode 0  | 0x01B0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD9_TH1_REG</a>  | Touch threshold configuration register for touch pin 9 for frequency mode 1  | 0x01B4  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD9_TH2_REG</a>  | Touch threshold configuration register for touch pin 9 for frequency mode 2  | 0x01B8  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD10_TH0_REG</a> | Touch threshold configuration register for touch pin 10 for frequency mode 0 | 0x01BC  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD10_TH1_REG</a> | Touch threshold configuration register for touch pin 10 for frequency mode 1 | 0x01C0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD10_TH2_REG</a> | Touch threshold configuration register for touch pin 10 for frequency mode 2 | 0x01C4  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD11_TH0_REG</a> | Touch threshold configuration register for touch pin 11 for frequency mode 0 | 0x01C8  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD11_TH1_REG</a> | Touch threshold configuration register for touch pin 11 for frequency mode 1 | 0x01CC  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD11_TH2_REG</a> | Touch threshold configuration register for touch pin 11 for frequency mode 2 | 0x01D0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD12_TH0_REG</a> | Touch threshold configuration register for touch pin 12 for frequency mode 0 | 0x01D4  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD12_TH1_REG</a> | Touch threshold configuration register for touch pin 12 for frequency mode 1 | 0x01D8  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD12_TH2_REG</a> | Touch threshold configuration register for touch pin 12 for frequency mode 2 | 0x01DC  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD13_TH0_REG</a> | Touch threshold configuration register for touch pin 13 for frequency mode 0 | 0x01E0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD13_TH1_REG</a> | Touch threshold configuration register for touch pin 13 for frequency mode 1 | 0x01E4  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD13_TH2_REG</a> | Touch threshold configuration register for touch pin 13 for frequency mode 2 | 0x01E8  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD14_TH0_REG</a> | Touch threshold configuration register for touch pin 14 for frequency mode 0 | 0x01EC  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD14_TH1_REG</a> | Touch threshold configuration register for touch pin 14 for frequency mode 1 | 0x01F0  | R/W    |
| <a href="#">LP_ANA_TOUCH_PAD14_TH2_REG</a> | Touch threshold configuration register for touch pin 14 for frequency mode 2 | 0x01F4  | R/W    |
| <a href="#">LP_ANA_DATE_REG</a>            | Version control register   | 0x03FC  | R/W    |

## 55.7 Registers

## 55.7.1 Interrupt and Status Registers

The addresses in this section are relative to Touch Sensor base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

### Register 55.1. RTC\_TOUCH\_INT\_RAW\_REG (0x0000)

Register 0x00000000: RTC\_TOUCH\_SCAN\_DONE\_INT\_RAW

|            |   |   |   |   |   |                                      |                           |                            |                          |                        |                             |
|------------|---|---|---|---|---|--------------------------------------|---------------------------|----------------------------|--------------------------|------------------------|-----------------------------|
| 31         | 6 | 5 | 4 | 3 | 2 | 1                                    | 0                         |                            |                          |                        |                             |
| (reserved) |   |   |   |   |   | RTC_TOUCH_APPROACH_LOOP_DONE_INT_RAW | RTC_TOUCH_TIMEOUT_INT_RAW | RTC_TOUCH_INACTIVE_INT_RAW | RTC_TOUCH_ACTIVE_INT_RAW | RTC_TOUCH_DONE_INT_RAW | RTC_TOUCH_SCAN_DONE_INT_RAW |

**RTC\_TOUCH\_SCAN\_DONE\_INT\_RAW** The raw interrupt status of [TOUCH\\_SCAN\\_DONE\\_INT](#).  
(R/SS/WTC)

**RTC\_TOUCH\_DONE\_INT\_RAW** The raw interrupt status of [TOUCH\\_DONE\\_INT](#). (R/SS/WTC)

**RTC\_TOUCH\_ACTIVE\_INT\_RAW** The raw interrupt status of **TOUCH\_ACTIVE\_INT**. (R/SS/WTC)

**RTC\_TOUCH\_INACTIVE\_INT\_RAW** The raw interrupt status of **TOUCH\_INACTIVE\_INT**. (R/SS/WTC)

**RTC\_TOUCH\_TIMEOUT\_INT\_RAW** The raw interrupt status of [TOUCH\\_TIMEOUT\\_INT](#). (R/SS/WTC)

**RTC\_TOUCH\_APPROACH\_LOOP\_DONE\_INT\_RAW** The raw interrupt status of [TOUCH\\_APPROACH\\_LOOP\\_DONE\\_INT](#). (R/SS/WTC)



### Register 55.2. RTC\_TOUCH\_INT\_ST\_REG (0x0004)

Diagram illustrating the structure of the RTC\_CR register (32 bits):

- Bits 31 to 6: (reserved)
- Bit 5: RTC\_TOUCH\_APPROACH\_LOOP\_DONE\_INT\_ST
- Bit 4: RTC\_TOUCH\_TIMEOUT\_INT\_ST
- Bit 3: RTC\_TOUCH\_INACTIVE\_INT\_ST
- Bit 2: RTC\_TOUCH\_ACTIVE\_INT\_ST
- Bit 1: RTC\_TOUCH\_DONE\_INT\_ST
- Bit 0: RTC\_TOUCH\_SCAN\_DONE\_INT\_ST

Reset

**RTC\_TOUCH\_SCAN\_DONE\_INT\_ST** The masked interrupt status of [TOUCH\\_DONE\\_INT](#). (RO)

**RTC\_TOUCH\_DONE\_INT\_ST** The masked interrupt status of [TOUCH\\_DONE\\_INT](#). (RO)

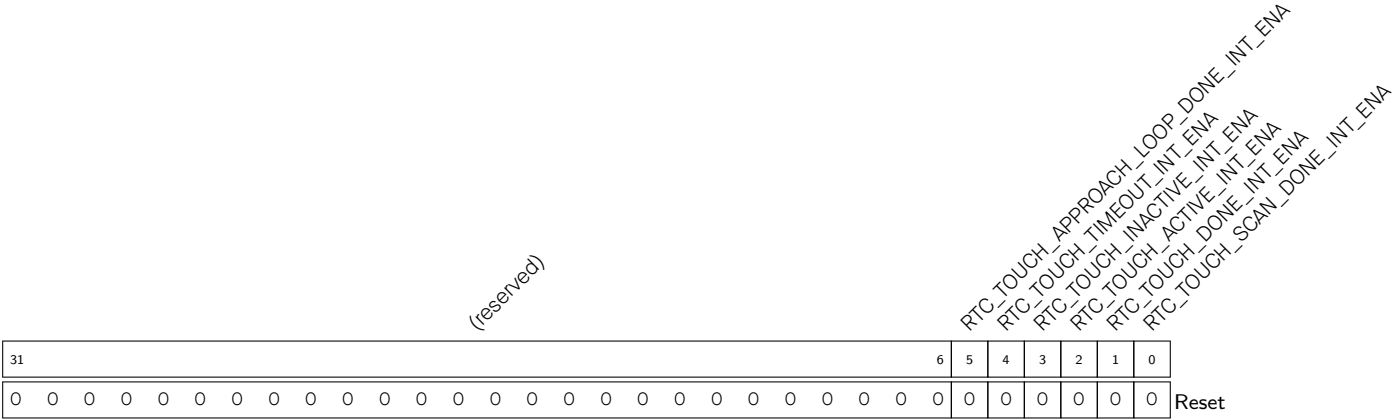
**RTC\_TOUCH\_ACTIVE\_INT\_ST** The masked interrupt status of [TOUCH\\_ACTIVE\\_INT](#). (RO)

**RTC\_TOUCH\_INACTIVE\_INT\_ST** The masked interrupt status of [TOUCH\\_INACTIVE\\_INT](#). (RO)

**RTC\_TOUCH\_TIMEOUT\_INT\_ST** The masked interrupt status of [TOUCH\\_TIMEOUT\\_INT](#). (RO)

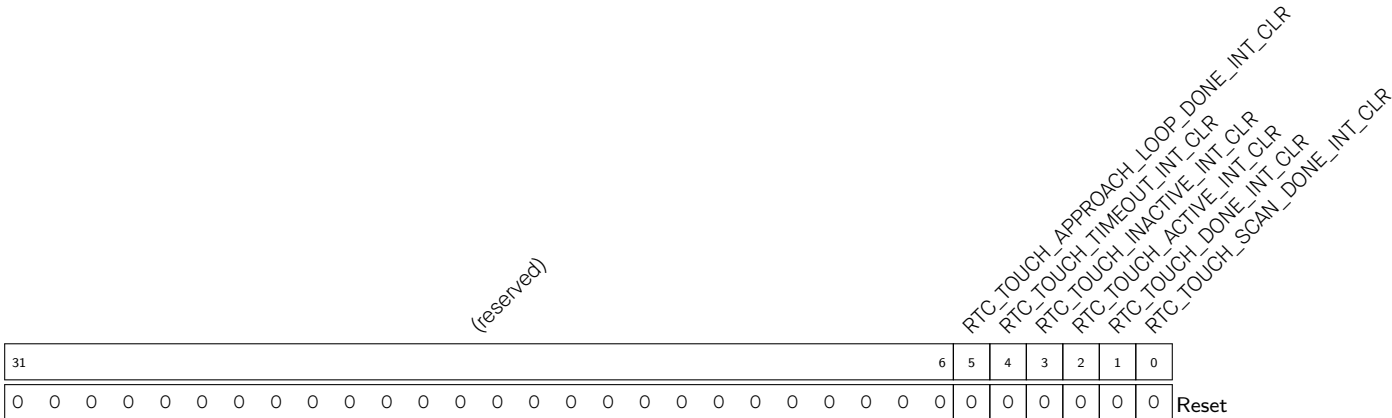
**RTC\_TOUCH\_APPROACH\_LOOP\_DONE\_INT\_ST** The masked interrupt status of [TOUCH\\_APPROACH\\_LOOP\\_DONE\\_INT](#). (RO)

Register 55.3. RTC\_TOUCH\_INT\_ENA\_REG (0x0008)



- RTC\_TOUCH\_SCAN\_DONE\_INT\_ENA Write 1 to enable TOUCH\_DONE\_INT. (R/W)
- RTC\_TOUCH\_DONE\_INT\_ENA Write 1 to enable TOUCH\_DONE\_INT. (R/W)
- RTC\_TOUCH\_ACTIVE\_INT\_ENA Write 1 to enable TOUCH\_ACTIVE\_INT. (R/W)
- RTC\_TOUCH\_INACTIVE\_INT\_ENA Write 1 to enable TOUCH\_INACTIVE\_INT. (R/W)
- RTC\_TOUCH\_TIMEOUT\_INT\_ENA Write 1 to enable TOUCH\_TIMEOUT\_INT. (R/W)
- RTC\_TOUCH\_APPROACH\_LOOP\_DONE\_INT\_ENA Write 1 to enable TOUCH\_APPROACH\_LOOP\_DONE\_INT. (R/W)

#### Register 55.4. RTC\_TOUCH\_INT\_CLR\_REG (0x000C)



**RTC\_TOUCH\_SCAN\_DONE\_INT\_CLR** Write 1 to clear **TOUCH\_DONE\_INT**. (WT)

**RTC\_TOUCH\_DONE\_INT\_CLR** Write 1 to clear **TOUCH\_DONE\_INT**. (WT)

**RTC\_TOUCH\_ACTIVE\_INT\_CLR** Write 1 to clear **TOUCH\_ACTIVE\_INT**. (WT)

**RTC\_TOUCH\_INACTIVE\_INT\_CLR** Write 1 to clear **TOUCH\_INACTIVE\_INT**. (WT)

**RTC\_TOUCH\_TIMEOUT\_INT\_CLR** Write 1 to clear **TOUCH\_TIMEOUT\_INT**. (WT)

RTC\_TOUCH\_APPROACH\_LOOP\_DONE\_INT\_CLR Write 1 to clear TOUCH\_APPROACH\_LOOP\_DONE\_INT.  
(WT)

Register 55.5. RTC\_TOUCH\_CHN\_STATUS\_REG (0x0010)

|            |   |   |   |   |   |   |   |   |   |                     |    |     |    |    |                     |      |   |   |   |                      |   |   |   |   |   |   |   |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---------------------|----|-----|----|----|---------------------|------|---|---|---|----------------------|---|---|---|---|---|---|---|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   | RTC_TOUCH_SCAN_CURR |    |     |    |    | RTC_TOUCH_MEAS_DONE |      |   |   |   | RTC_TOUCH_PAD_ACTIVE |   |   |   |   |   |   |   |   |   |   |       |
| 30         |   |   |   |   |   |   |   |   |   |                     | 20 | 19  | 16 | 15 | 14                  |      |   |   |   |                      |   |   |   |   |   |   |   |   |   |   | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                   | 0  | 0   | 0  | 0  | 0                   | 0    | 0 | 0 | 0 | 0                    | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0     |
|            |   |   |   |   |   |   |   |   |   |                     |    | 0x0 |    |    | 0                   | 0x00 |   |   |   |                      |   |   |   |   |   |   |   |   |   |   | Reset |

**RTC\_TOUCH\_PAD\_ACTIVE** Indicates whether the touch pin detects a touch. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.

0: No touch detected

1: Touch detected

(RO)

**RTC\_TOUCH\_MEAS\_DONE** Indicates whether the touch pins have been measured at all frequency modes.

0: Not completed

1: Completed

(RO)

**RTC\_TOUCH\_SCAN\_CURR** Indicates the index number of the currently scanned touch pin. (RO)

Register 55.6. RTC\_TOUCH\_STATUS\_*n*\_REG (*n*: 1-14) (0x0018+0x4\**n*)

|            |   |   |   |   |   |   |   |   |    |                                   |    |    |     |    |   |      |  |  |  |                                 |  |  |  |  |  |  |  |  |   |       |  |
|------------|---|---|---|---|---|---|---|---|----|-----------------------------------|----|----|-----|----|---|------|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|---|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |    | RTC_TOUCH_PAD <sub>n</sub> NN_CNT |    |    |     |    | RTC_TOUCH_PAD <sub>n</sub> DEBOUNCE_CNT |      |  |  |  | RTC_TOUCH_PAD <sub>n</sub> DATA |  |  |  |  |  |  |  |  |   |       |  |
| 31         |   |   |   |   |   |   |   |   | 23 | 22                                | 19 | 18 | 16  | 15 |   |      |  |  |  |                                 |  |  |  |  |  |  |  |  | 0 |       |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0x0                               |    |    | 0x0 |    |   | 0x00 |  |  |  |                                 |  |  |  |  |  |  |  |  |   | Reset |  |

**RTC\_TOUCH\_PAD<sub>*n*</sub>DATA** Indicates the touch\_raw\_data, touch\_smooth\_data, or benchmark sampled by touch pin *n*. (RO)

**RTC\_TOUCH\_PAD<sub>*n*</sub>DEBOUNCE\_CNT** Indicates the cumulative number of consecutive touch or touch release detection by touch pin *n*. (RO)

**RTC\_TOUCH\_PAD<sub>*n*</sub>NN\_CNT** Indicates the cumulative number of consecutive instances where *touch\_smooth\_data* < *benchmark* – *passive\_noise\_threshold* has been detected by touch pin *n*. (RO)

**Register 55.7. RTC\_TOUCH\_STATUS\_15\_REG (0x0050)**

|                     |  |  |  |  |  |  |  |  |  |                      |  |  |  |                            |  |  |  |                    |  |  |  |    |  |  |  |    |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |
|---------------------|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|----------------------------|--|--|--|--------------------|--|--|--|----|--|--|--|----|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|
| (reserved)          |  |  |  |  |  |  |  |  |  | RTC_TOUCH_SLP_NN_CNT |  |  |  | RTC_TOUCH_SLP_DEBOUNCE_CNT |  |  |  | RTC_TOUCH_SLP_DATA |  |  |  |    |  |  |  |    |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |
| 31                  |  |  |  |  |  |  |  |  |  | 23                   |  |  |  | 19                         |  |  |  | 18                 |  |  |  | 16 |  |  |  | 15 |  |  |  |       |  |  |  |  |  |  |  | 0 |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  | 0x0                  |  |  |  | 0x0                        |  |  |  | 0x00               |  |  |  |    |  |  |  |    |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |

**RTC\_TOUCH\_SLP\_DATA** Indicates the touch\_smooth\_data or benchmark sampled by touch pin in sleep mode. (RO)

**RTC\_TOUCH\_SLP\_DEBOUNCE\_CNT** Indicates the cumulative number of consecutive touch or touch release detection by touch pin in sleep mode. (RO)

**RTC\_TOUCH\_SLP\_NN\_CNT** Indicates the cumulative number of consecutive instances where *touch\_smooth\_data < benchmark - passive\_noise\_threshold* has been detected by touch pin in sleep mode. (RO)

**Register 55.8. RTC\_TOUCH\_STATUS\_16\_REG (0x0054)**

|                            |    |  |  |  |  |  |  |                             |    |  |  |  |  |    |   |                             |  |  |  |   |   |  |  |                             |  |  |  |  |  |  |  |       |
|----------------------------|----|--|--|--|--|--|--|-----------------------------|----|--|--|--|--|----|---|-----------------------------|--|--|--|---|---|--|--|-----------------------------|--|--|--|--|--|--|--|-------|
| RTC_TOUCH_SLP_APPROACH_CNT |    |  |  |  |  |  |  | RTC_TOUCH_APPROACH_PADO_CNT |    |  |  |  |  |    |   | RTC_TOUCH_APPROACH_PAD1_CNT |  |  |  |   |   |  |  | RTC_TOUCH_APPROACH_PAD2_CNT |  |  |  |  |  |  |  |       |
| 31                         | 24 |  |  |  |  |  |  | 23                          | 16 |  |  |  |  | 15 | 8 |                             |  |  |  | 7 | 0 |  |  |                             |  |  |  |  |  |  |  |       |
| 0x0                        |    |  |  |  |  |  |  | 0x0                         |    |  |  |  |  |    |   | 0x0                         |  |  |  |   |   |  |  | 0x0                         |  |  |  |  |  |  |  | Reset |

**RTC\_TOUCH\_APPROACH\_PAD2\_CNT** Indicates the cumulative number of samplings of touch pin 2 in proximity mode. (RO)

**RTC\_TOUCH\_APPROACH\_PAD1\_CNT** Indicates the cumulative number of samplings of touch pin 1 in proximity mode. (RO)

**RTC\_TOUCH\_APPROACH\_PADO\_CNT** Indicates the cumulative number of samplings of touch pin 0 in proximity mode. (RO)

**RTC\_TOUCH\_SLP\_APPROACH\_CNT** Indicates the cumulative number of samplings of the sleeping touch pin in proximity mode. (RO)

**Register 55.9. RTC\_TOUCH\_STATUS\_17\_REG (0x0058)**

|            |   |   |   |   |    |    |    |                   |   |  |  |                 |    |    |  |                  |   |  |    |                  |   |  |  |                    |   |   |   |                    |   |  |  |  |       |  |  |  |
|------------|---|---|---|---|----|----|----|-------------------|---|--|--|-----------------|----|----|--|------------------|---|--|----|------------------|---|--|--|--------------------|---|---|---|--------------------|---|--|--|--|-------|--|--|--|
| (reserved) |   |   |   |   |    |    |    | RTC_FREQ_SCAN_CNT |   |  |  | RTC_TOUCH_DBIAS |    |    |  | RTC_TOUCH_DRV_HS |   |  |    | RTC_TOUCH_DRV_LS |   |  |  | RTC_TOUCH_DRES_LPF |   |   |   | RTC_TOUCH_DCAP_LPF |   |  |  |  |       |  |  |  |
| 31         |   |   |   |   | 25 | 24 | 23 | 22                |   |  |  |                 | 18 | 16 |  |                  |   |  | 12 | 12               |   |  |  |                    | 9 | 8 | 7 | 6                  |   |  |  |  | 0     |  |  |  |
| 0          | 0 | 0 | 0 | 0 | 0  | 0  | 0  | 0                 | 0 |  |  |                 | 0  |    |  |                  | 0 |  |    |                  | 0 |  |  |                    | 0 |   |   |                    | 0 |  |  |  | Reset |  |  |  |

**RTC\_TOUCH\_DCAP\_LPF** Indicates the DCAP\_LPF value of the current touch pin. (RO)

**RTC\_TOUCH\_DRES\_LPF** Indicates the DRES\_LPF value of the current touch pin. (RO)

**RTC\_TOUCH\_DRV\_LS** Indicates the DRV\_LS value of the current touch pin. (RO)

**RTC\_TOUCH\_DRV\_HS** Indicates the DRV\_HS value of the current touch pin. (RO)

**RTC\_TOUCH\_DBIAS** Indicates the DBIAS value of the current touch pin. (RO)

**RTC\_FREQ\_SCAN\_CNT** Indicates the SCAN\_CNT value of the current touch pin. (RO)

**Register 55.10. RTC\_TOUCH\_CHN\_TMP\_STATUS\_REG (0x005C)**

|            |    |      |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |    |   |  |  |  |  |  |  |  |  |  |  |  |       |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------|----|------|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|----|---|--|--|--|--|--|--|--|--|--|--|--|-------|--|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved) |    |      |  |  |  |  |  |  |  |  |  |  |  |  |  | RTC_TOUCH_PAD_ACTIVE_STATUS |    |   |  |  |  |  |  |  |  |  |  |  |  |       |  | RTC_TOUCH_PAD_INACTIVE_STATUS |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31         | 30 | 29   |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                          | 14 | 0 |  |  |  |  |  |  |  |  |  |  |  |       |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0          | 0  | 0x00 |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x00                        |    |   |  |  |  |  |  |  |  |  |  |  |  | Reset |  |                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**RTC\_TOUCH\_PAD\_INACTIVE\_STATUS** Indicates whether the touch pin detects the touch pad from being touched to being released. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.

0: Touch release detected

1: Touch release not detected

(RO)

**RTC\_TOUCH\_PAD\_ACTIVE\_STATUS** Indicates whether the touch pin detects the process of being touched. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.

0: Touch detected

1: Touch not detected

(RO)

Register 55.11. RTC\_TOUCH\_DATE\_REG (0x0100)

|                          |    |          |    |
|--------------------------|----|----------|----|
| RTC_CLK_EN<br>(reserved) |    | RTC_DATE |    |
| 31                       | 30 | 28       | 27 |
| 0                        | 0  | 0        | 0  |
| 0x2309130                |    |          |    |
| Reset                    |    |          |    |

**RTC\_CLK\_EN** Configures whether to enable the register read/write clock.

0: Disable

1: Enable

(R/W)

**RTC\_DATE** Version control register. (R/W)

## 55.7.2 Configuration Registers

The addresses in this section are relative to LP Analog Peripheral base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section *Programming Reserved Register Field*.

Register 55.12. LP\_ANA\_TOUCH\_APPROACH\_WORK\_MEAS\_NUM\_REG (0x00FC)

|            |    |                                 |     |                                 |     |                                 |     |
|------------|----|---------------------------------|-----|---------------------------------|-----|---------------------------------|-----|
| (reserved) |    | LP_ANA_TOUCH_APPROACH_MEAS_NUM0 |     | LP_ANA_TOUCH_APPROACH_MEAS_NUM1 |     | LP_ANA_TOUCH_APPROACH_MEAS_NUM2 |     |
| 31         | 30 | 29                              | 20  | 19                              | 10  | 9                               | 0   |
| 0          | 0  |                                 | 100 |                                 | 100 |                                 | 100 |
| Reset      |    |                                 |     |                                 |     |                                 |     |

**LP\_ANA\_TOUCH\_APPROACH\_MEAS\_NUM2** Configures the number of measurements for sampling frequency mode 2 in proximity mode. (R/W)

**LP\_ANA\_TOUCH\_APPROACH\_MEAS\_NUM1** Configures the number of measurements for sampling frequency mode 1 in proximity mode. (R/W)

**LP\_ANA\_TOUCH\_APPROACH\_MEAS\_NUM0** Configures the number of measurements for sampling frequency mode 0 in proximity mode. (R/W)

Register 55.13. LP\_ANA\_TOUCH\_SCAN\_CTRL1\_REG (0x0100)

|  |  |  |  |  |  |  |  |  |  |  |    |    |  |  |   |   |   |       |
|--|--|--|--|--|--|--|--|--|--|--|----|----|--|--|---|---|---|-------|
| LP_ANA_TOUCH_XPD_WAIT  |  |  |  |  |  |  |  |  |  |  |    |    |  |  |   |   |   |       |
| LP_ANA_TOUCH_SCAN_PAD_MAP                                      |  |  |  |  |  |  |  |  |  |  |    |    |  |  |   |   |   |       |
| LP_ANA_TOUCH_INACTIVE_CONNECTION<br>LP_ANA_TOUCH_SHIELD_PAD_EN |  |  |  |  |  |  |  |  |  |  |    |    |  |  |   |   |   |       |
| 31   |  |  |  |  |  |  |  |  |  |  | 17 | 16 |  |  | 2 | 1 | 0 |       |
| 0x04   |  |  |  |  |  |  |  |  |  |  |    | 0  |  |  |   | 0 | 0 | Reset |

**LP\_ANA\_TOUCH\_SHIELD\_PAD\_EN** Configures whether to enable the moisture tolerance feature.  
0: Disable  
1: Enable  
(R/W)

**LP\_ANA\_TOUCH\_INACTIVE\_CONNECTION** Configures whether to power up the touch pins involved in the measurement in scan mode.  
0: Not power up  
1: Power up  
(R/W)

**LP\_ANA\_TOUCH\_SCAN\_PAD\_MAP** Configures which touch pins to use in scan mode for measurement. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.  
0: No effect  
1: Enable the touch pin  
(R/W)

**LP\_ANA\_TOUCH\_XPD\_WAIT** Configures the power-up wait time after initiating a measurement.  
(R/W)



**Register 55.14. LP\_ANA\_TOUCH\_SCAN\_CTRL2\_REG (0x0104)**

|            |    |                            |    |                     |     |                       |    |                         |  |                          |   |  |  |  |  |            |   |
|------------|----|----------------------------|----|---------------------|-----|-----------------------|----|-------------------------|--|--------------------------|---|--|--|--|--|------------|---|
| (reserved) |    | LP_ANA_FREQ_SCAN_CNT_LIMIT |    | LP_ANA_FREQ_SCAN_EN |     | LP_ANA_TOUCH_OUT_RING |    | LP_ANA_TOUCH_TIMEOUT_EN |  | LP_ANA_TOUCH_TIMEOUT_NUM |   |  |  |  |  | (reserved) |   |
| 31         | 30 | 29                         | 28 | 27                  | 26  | 23                    | 22 | 21                      |  | 6                        | 5 |  |  |  |  |            | 0 |
| 0          | 0  |                            | 3  | 0                   | 0xf |                       | 0  |                         |  | 0xffff                   |   |  |  |  |  | 0          | 0 |

Reset

**LP\_ANA\_TOUCH\_TIMEOUT\_NUM** Configures the number of measurement timeouts. (R/W)

**LP\_ANA\_TOUCH\_TIMEOUT\_EN** Configures whether to enable the measurement timeout.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_TOUCH\_OUT\_RING** Configures which touch pins to be used for water rejection. Configurable values are 1-14. Other values are invalid. (R/W)

**LP\_ANA\_FREQ\_SCAN\_EN** Configures whether to enable frequency hopping.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_FREQ\_SCAN\_CNT\_LIMIT** Configures the number of frequency hops.

0: 1

1: 2

2: 3

3: Invalid

(R/W)

**Register 55.15. LP\_ANA\_TOUCH\_WORK\_REG (0x0108)**

|            |    |   |   |                       |    |            |    |                      |  |                 |    |                 |    |                 |  |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|------------|----|---|---|-----------------------|----|------------|----|----------------------|--|-----------------|----|-----------------|----|-----------------|--|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (reserved) |    |   |   | LP_ANA_TOUCH_OUT_GATE |    | (reserved) |    | LP_ANA_TOUCH_OUT_SEL |  | LP_ANA_DIV_NUM0 |    | LP_ANA_DIV_NUM1 |    | LP_ANA_DIV_NUM2 |  | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         | 28 |   |   | 27                    | 26 | 25         | 24 | 22                   |  | 21              | 19 |                 | 18 | 16              |  | 15         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0  | 0 | 0 | 0                     | 0  | 0          | 0  | 0x0                  |  | 0x0             |    | 0x0             |    | 0               |  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**LP\_ANA\_DIV\_NUM2** Configures the enabling of the TOUCH\_OUT signal division and the coefficient for sampling frequency mode 0.

bit[0]: Configures whether to enable division.

0: Disable

1: Enable

bit[1-2]: Configures the TOUCH\_OUT signal division coefficient.

0: 0

1: 2

2: 4

3: 6

Other values: Invalid

(R/W)

**LP\_ANA\_DIV\_NUM1** Configures the enabling of the TOUCH\_OUT signal division and the coefficient for sampling frequency mode 1. For detailed configuration, refer to [LP\\_ANA\\_DIV\\_NUM2](#). (R/W)

**LP\_ANA\_DIV\_NUM0** Configures the enabling of the TOUCH\_OUT signal division and the coefficient for sampling frequency mode 2. For detailed configuration, refer to [LP\\_ANA\\_DIV\\_NUM2](#). (R/W)

**LP\_ANA\_TOUCH\_OUT\_SEL** Configures whether to use the TOUCH\_OUT signal for clock or data.

0: TOUCH\_OUT signal is used as data

1: TOUCH\_OUT signal is used as clock

(R/W)

**LP\_ANA\_TOUCH\_OUT\_GATE** Configures whether to enable gating after enabling the TOUCH\_OUT signal division.

0: Disable

1: Enable

(R/W)

Register 55.16. LP\_ANA\_TOUCH\_WORK\_MEAS\_NUM\_REG (0x010C)

|            |    |     |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |                        |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |                        |  |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |   |
|------------|----|-----|------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----|------------------------|--|----|---|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|---|
| (reserved) |    |     | LP_ANA_TOUCH_MEAS_NUM0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     | LP_ANA_TOUCH_MEAS_NUM1 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     | LP_ANA_TOUCH_MEAS_NUM2 |  |    |   |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |   |
| 31         | 30 | 29  |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     | 20                     | 19 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |     |                        |  | 10 | 9 |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  | 0 |
| 0          | 0  | 100 |                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 100 |                        |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 100 |                        |  |    |   |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |   |

- LP\_ANA\_TOUCH\_MEAS\_NUM2 Configures the number of measurements for sampling frequency mode 2 in normal operation. (R/W)
- LP\_ANA\_TOUCH\_MEAS\_NUM1 Configures the number of measurements for sampling frequency mode 1 in normal operation. (R/W)
- LP\_ANA\_TOUCH\_MEAS\_NUM0 Configures the number of measurements for sampling frequency mode 0 in normal operation.(R/W)

**Register 55.17. LP\_ANA\_TOUCH\_FILTER1\_REG (0x0110)**

|                             |    |    |                             |    |    |                       |    |    |                        |   |   |                          |   |   |                          |   |   |                         |   |   |                          |  |  |                       |  |  |                         |  |  |                                     |  |  |
|-----------------------------|----|----|-----------------------------|----|----|-----------------------|----|----|------------------------|---|---|--------------------------|---|---|--------------------------|---|---|-------------------------|---|---|--------------------------|--|--|-----------------------|--|--|-------------------------|--|--|-------------------------------------|--|--|
| LP_ANA_TOUCH_DEBOUNCE_LIMIT |    |    | LP_ANA_TOUCH_APPROACH_LIMIT |    |    | LP_ANA_TOUCH_NN_LIMIT |    |    | LP_ANA_TOUCH_FILTER_EN |   |   | LP_ANA_TOUCH_FILTER_MODE |   |   | LP_ANA_TOUCH_JITTER_STEP |   |   | LP_ANA_TOUCH_SMOOTH_LVL |   |   | LP_ANA_TOUCH_NOISE_THRES |  |  | LP_ANA_TOUCH_NN_THRES |  |  | LP_ANA_TOUCH_HYSTERESIS |  |  | LP_ANA_TOUCH_NN_DISUPDATE_BENCHMARK |  |  |
| 31                          | 29 | 28 | 21                          | 20 | 17 | 16                    | 15 | 13 | 12                     | 9 | 8 | 7                        | 6 | 5 | 4                        | 3 | 2 | 1                       | 0 | 0 | Reset                    |  |  |                       |  |  |                         |  |  |                                     |  |  |
| 3                           |    |    | 80                          |    |    | 5                     |    |    | 0                      |   |   | 0                        |   |   | 1                        |   |   | 0                       |   |   | 0                        |  |  | 0                     |  |  | 0                       |  |  | 0                                   |  |  |

**LP\_ANA\_TOUCH\_NN\_DISUPDATE\_BENCHMARK\_EN** Configures whether to turn off the benchmark data correction.

0: Do not turn off

1: Turn off

(R/W)

**LP\_ANA\_TOUCH\_HYSTERESIS** Configures the sampling hysteresis. (R/W)

**LP\_ANA\_TOUCH\_NN\_THRES** Configures the out-of-phase noise\_threshold. (R/W)

**LP\_ANA\_TOUCH\_NOISE\_THRES** Configures the noise\_threshold. (R/W)

**LP\_ANA\_TOUCH\_SMOOTH\_LVL** Configures the IIR filter module for touch\_smooth\_data.(R/W)

**LP\_ANA\_TOUCH\_JITTER\_STEP** Configures the jitter step in filter module 7 for generating benchmark data. (R/W)

**LP\_ANA\_TOUCH\_FILTER\_MODE** Configures the filter module for generating benchmark data. (R/W)

**LP\_ANA\_TOUCH\_FILTER\_EN** Configures whether to enable the filter module for generating benchmark data.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_TOUCH\_NN\_LIMIT** Configures the number of consecutive sampling instances where the sampling value exceeds the out-of-phase noise\_threshold. (R/W)

**LP\_ANA\_TOUCH\_APPROACH\_LIMIT** Configures the number of sampling in proximity mode. (R/W)

**LP\_ANA\_TOUCH\_DEBOUNCE\_LIMIT** Configures the number of consecutive sampling for detecting touch state changes. (R/W)

LP\_ANA\_TOUCH\_BYPASS\_IN\_THRES  
LP\_ANA\_TOUCH\_BYPASS\_NOISE\_THRES

LP\_ANA\_TOUCH\_OUTEN

(reserved)

0: Disable

(R/W)

0: Disable

1: Enable

0: Disable

1: Enable

(reserved)

LP\_ANA\_TOUCH\_UPDATE\_BENCHMARK\_SW

LP\_ANA\_TOUCH\_BENCHMARK\_SW

LP\_ANA\_TOUCH\_UPDATE\_BENCHMARK\_SW Write 1 to enable the software to write the benchmark data. (WT)

**Register 55.20. LP\_ANA\_TOUCH\_SLP0\_REG (0x011C)**

|            |   |   |   |   |   |   |   |   |   |   |    |                      |    |    |    |                              |   |   |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |       |
|------------|---|---|---|---|---|---|---|---|---|---|----|----------------------|----|----|----|------------------------------|---|---|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |    | LP_ANA_TOUCH_SLP_PAD |    |    |    | LP_ANA_TOUCH_SLP_CHANNEL_CLR |   |   |  | LP_ANA_TOUCH_SLP_TH0 |  |  |  |  |  |  |  |  |  |  |  |  |       |
| 31         |   |   |   |   |   |   |   |   |   |   | 21 | 20                   | 17 | 16 | 15 |                              |   |   |  |                      |  |  |  |  |  |  |  |  |  |  |  |  | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0                    | 0  | 0  | 0  | 0xf                          | 0 | 0 |  |                      |  |  |  |  |  |  |  |  |  |  |  |  | Reset |

**LP\_ANA\_TOUCH\_SLP\_TH0** Configures the touch threshold for sampling frequency mode 0 in sleep mode. (R/W)

**LP\_ANA\_TOUCH\_SLP\_CHANNEL\_CLR** Write 1 to clear the benchmark data in sleep mode. (WT)

**LP\_ANA\_TOUCH\_SLP\_PAD** Configures which touch sensor to enter sleep mode. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.

0: No effect

1: Selects the touch sensor to enter sleep mode

(R/W)

**Register 55.21. LP\_ANA\_TOUCH\_SLP1\_REG (0x0120)**

|                      |  |  |  |  |  |  |  |  |  |  |    |    |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|----------------------|--|--|--|--|--|--|--|--|--|--|----|----|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| LP_ANA_TOUCH_SLP_TH1 |  |  |  |  |  |  |  |  |  |  |    |    |  |  |  | LP_ANA_TOUCH_SLP_TH2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31                   |  |  |  |  |  |  |  |  |  |  | 16 | 15 |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0                    |  |  |  |  |  |  |  |  |  |  |    |    |  |  |  | 0                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**LP\_ANA\_TOUCH\_SLP\_TH2** Configures the touch threshold for sampling frequency mode 2 in sleep mode. (R/W)

**LP\_ANA\_TOUCH\_SLP\_TH1** Configures the touch threshold for sampling frequency mode 1 in sleep mode. (R/W)

**Register 55.22. LP\_ANA\_TOUCH\_CLR\_REG (0x0124)**

|            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |                          |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  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| 31         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                      |  |  |  |  |  |  |  | 15                       |  |  |  |  |  |  |  | 14 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  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| 0          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                       |  |  |  |  |  |  |  | 0                        |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  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|  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |

**LP\_ANA\_TOUCH\_CHANNEL\_CLR** Write 1 to independently clear the touch state of the 14 touch sensors. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid. (WT)

**LP\_ANA\_TOUCH\_STATUS\_CLR** Write 1 to clear the touch state. (WT)

**Register 55.23. LP\_ANA\_TOUCH\_APPROACH\_REG (0x0128)**

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                              |  |  |  |  |  |  |  |  |  |  |  |                            |    |  |  |  |  |  |  |  |  |  |  |                            |   |   |   |  |  |  |  |  |  |  |  |                            |  |  |   |   |  |  |  |  |  |  |  |       |  |  |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|------------------------------|--|--|--|--|--|--|--|--|--|--|--|----------------------------|----|--|--|--|--|--|--|--|--|--|--|----------------------------|---|---|---|--|--|--|--|--|--|--|--|----------------------------|--|--|---|---|--|--|--|--|--|--|--|-------|--|--|--|
| (reserved)                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_SLP_APPROACH_EN |  |  |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_APPROACH_PAD2 |    |  |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_APPROACH_PAD1 |   |   |   |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_APPROACH_PADO |  |  |   |   |  |  |  |  |  |  |  |       |  |  |  |
| 31                                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 13                           |  |  |  |  |  |  |  |  |  |  |  | 12                         | 11 |  |  |  |  |  |  |  |  |  |  |                            | 8 | 7 | 4 |  |  |  |  |  |  |  |  |                            |  |  | 3 | 0 |  |  |  |  |  |  |  |       |  |  |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                            |  |  |  |  |  |  |  |  |  |  |  | 0xf                        |    |  |  |  |  |  |  |  |  |  |  | 0xf                        |   |   |   |  |  |  |  |  |  |  |  | 0xf                        |  |  |   |   |  |  |  |  |  |  |  | Reset |  |  |  |

**LP\_ANA\_TOUCH\_APPROACH\_PADO** Configure the first touch pin used in proximity mode. Configurable values are 1-14. Other values are invalid. (R/W)

**LP\_ANA\_TOUCH\_APPROACH\_PAD1** Configure the second touch pin used in proximity mode. Configurable values are 1-14. Other values are invalid. (R/W)

**LP\_ANA\_TOUCH\_APPROACH\_PAD2** Configure the third touch pin used in proximity mode. Configurable values are 1-14. Other values are invalid. (R/W)

**LP\_ANA\_TOUCH\_SLP\_APPROACH\_EN** Configures whether to enable proximity mode.

0: Disable

1: Enable

(R/W)

**Register 55.24. LP\_ANA\_TOUCH\_FREQ<sub>n</sub>\_SCAN\_PARA\_REG (n: 0-2) (0x012C+0x4\*n)**

|            |  |  |  |  |  |  |  |  |  |                                       |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|---------------------------------------|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_FREQ <sub>n</sub> _DBIAS |  |  |  |  |  |  |  | LP_ANA_TOUCH_FREQ <sub>n</sub> _DRV_HS |  |    |  |  |  |  |  | LP_ANA_TOUCH_FREQ <sub>n</sub> _DRV_LS |  |  |  |    |  |  |  | LP_ANA_TOUCH_FREQ <sub>n</sub> _DRES_LPF |  |  |  |  |  |    |  | LP_ANA_TOUCH_FREQ <sub>n</sub> _DCAP_LPF |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  | 23                                    |  |  |  |  |  |  |  |  |  | 22 |  |  |  |  |  |  |  |  |  | 18 |  |  |  |  |  |  |  |  |  | 17 |  |  |  |  |  |  |  |  |  | 13 |  |  |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  |  |  | 9 |  |  |  |  |  |  |  |  |  | 8 |  |  |  |  |  |  |  |  |  | 7 |  |  |  |  |  |  |  |  |  | 6     |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  | 0                                     |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |

**LP\_ANA\_TOUCH\_FREQ<sub>0</sub>\_DCAP\_LPF** Configures the touch sensor low-pass filter for sampling frequency mode *n*. The adjustment range is 0-2.54 pF, and the step is 20 fF. (R/W)(R/W)

**LP\_ANA\_TOUCH\_FREQ<sub>0</sub>\_DRES\_LPF** Configures the touch sensor low-pass filter for sampling frequency mode *n*.

0: 0 kΩ

1: 3 kΩ

2: 4.5 kΩ

3: 7.5 kΩ

(R/W)

**LP\_ANA\_TOUCH\_FREQ<sub>0</sub>\_DRV\_LS** Configures the value of DRV\_LS of the touch sensor for sampling frequency mode *n*. (R/W)

**LP\_ANA\_TOUCH\_FREQ<sub>0</sub>\_DRV\_HS** Configures the value of DRV\_HS of the touch sensor for sampling frequency mode *n*. (R/W)

**LP\_ANA\_TOUCH\_FREQ<sub>0</sub>\_DBIAS** Configures whether to enable the moisture tolerance function and configures the internal voltage of the touch sensor for sampling frequency mode *n*.

bit[0]: Configures whether to enable the moisture tolerance function for sampling frequency mode *n*.

0: Disable

1: Enable

bit[1-4]: Configures the internal voltage of the touch sensor for sampling frequency mode *n*.

(R/W)



### Register 55.25. LP\_ANA\_TOUCH\_ANA\_PARA\_REG (0x0138)

|   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                             |  |  |  |                           |  |   |  |                            |  |  |  |   |  |   |  |   |  |
|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-----------------------------|--|--|--|---------------------------|--|---|--|----------------------------|--|--|--|---|--|---|--|---|--|
| (reserved)                                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_TOUCH_DCAP_CAL |  |  |  | LP_ANA_TOUCH_TOUCH_EN_CAL |  |   |  | LP_ANA_TOUCH_TOUCH_BUF_DRV |  |  |  |   |  |   |  |   |  |
| 31  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 11                          |  |  |  | 10                        |  |   |  | 4                          |  |  |  | 3 |  | 2 |  | 0 |  |
| 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                           |  |  |  | 0                         |  | 0 |  | Reset                      |  |  |  |   |  |   |  |   |  |

**LP\_ANA\_TOUCH\_TOUCH\_BUF\_DRV** Configures the value of BUF\_DRV. (R/W)

**LP\_ANA\_TOUCH\_TOUCH\_EN\_CAL** Configures whether to enable the touch sensor internal capacitance test mode.

0: Disable

1: Enable

(R/W)

**LP\_ANA\_TOUCH\_TOUCH\_DCAP\_CAL** Configures the internal capacitance connected to the touch pins. The default value is 0, and the adjustment range is 0-127 pF with a step of 1. (R/W)

**Register 55.26. LP\_ANA\_TOUCH\_MUX0\_REG (0x013C)**

|                          |    |    |    |    |                     |    |    |    |   |   |   |                       |   |   |   |                       |   |   |   |            |   |   |   |
|--------------------------|----|----|----|----|---------------------|----|----|----|---|---|---|-----------------------|---|---|---|-----------------------|---|---|---|------------|---|---|---|
| LP_ANA_TOUCH_START_FORCE |    |    |    |    | LP_ANA_TOUCH_BUFSEL |    |    |    |   |   |   | LP_ANA_TOUCH_FREQ_SEL |   |   |   | LP_ANA_TOUCH_DATA_SEL |   |   |   | (reserved) |   |   |   |
| 31                       | 30 | 29 | 28 | 27 | 26                  | 12 | 11 | 10 | 9 | 8 | 7 |                       |   |   |   |                       |   |   |   |            |   |   |   |
| 0                        | 0  | 1  | 0  | 0  |                     | 0  |    |    | 0 | 0 |   | 0                     | 0 | 0 | 0 | 0                     | 0 | 0 | 0 | 0          | 0 | 0 | 0 |

Reset

**LP\_ANA\_TOUCH\_DATA\_SEL** Configures the type of the return value.

- 0/1: touch\_raw\_data
  - 2: benchmark
  - 3: touch\_smooth\_data
- (R/W)

**LP\_ANA\_TOUCH\_FREQ\_SEL** Configures the corresponding sampling frequency mode of the return value.

- 0: 0
  - 1: 1
  - 2: 2
  - 3: Invalid
- (R/W)

**LP\_ANA\_TOUCH\_BUFSEL** Configures whether to enable a touch pin to be used for moisture tolerance. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_ANA\_TOUCH\_DONE\_EN** Configures whether to enable software to trigger the DONE signal that enables the measurement.

- 0: Disable
  - 1: Enable
- (R/W)

**LP\_ANA\_TOUCH\_DONE\_FORCE** Configures whether to generate the DONE signal to end the current measurement operation.

- 0: Not generate
  - 1: Generate
- (R/W)

**LP\_ANA\_TOUCH\_FSM\_EN** Configures the control source to power up and activate touch pins.

- 0: Controlled by software
  - 1: Controlled by hardware
- (R/W)

Continued on the next page...

Register 55.26. LP\_ANA\_TOUCH\_MUX0\_REG (0x013C)

Continued from the previous page...

**LP\_ANA\_TOUCH\_START\_EN** Configures whether to enable software to trigger the START signal to start the measurement.  
0: Disable  
1: Enable  
(R/W)

**LP\_ANA\_TOUCH\_START\_FORCE** Configures whether to generate the DONE signal to start a measurement.  
0: Not generate  
1: Generate  
(R/W)

Register 55.27. LP\_ANA\_TOUCH\_MUX1\_REG (0x0140)

|            |    |                  |  |  |  |  |  |  |  |  |  |                    |    |    |  |  |  |  |  |  |  |       |  |  |   |
|------------|----|------------------|--|--|--|--|--|--|--|--|--|--------------------|----|----|--|--|--|--|--|--|--|-------|--|--|---|
| (reserved) |    | LP_ANA_TOUCH_XPD |  |  |  |  |  |  |  |  |  | LP_ANA_TOUCH_START |    |    |  |  |  |  |  |  |  |       |  |  |   |
| 31         | 30 | 29               |  |  |  |  |  |  |  |  |  |                    | 15 | 14 |  |  |  |  |  |  |  |       |  |  | 0 |
| 0          | 0  | 0                |  |  |  |  |  |  |  |  |  | 0                  |    |    |  |  |  |  |  |  |  | Reset |  |  |   |

**LP\_ANA\_TOUCH\_START** Configures whether to activate the 14 touch pins. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.  
0: No effect  
1: Activate  
(R/W)

**LP\_ANA\_TOUCH\_XPD** Configures whether to power up the 14 touch pins. Bit 1-14 corresponds to touch pin 1-14 respectively. Other bits are invalid.  
0: Not power up  
1: Power up  
(R/W)

Register 55.28. LP\_ANA\_TOUCH\_PAD $n$ \_THO\_REG ( $n$ : 1-14) (0x0150+0xC\* $n$ )

|                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LP_ANA_TOUCH_PAD <sup>n</sup> _TH0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 16                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 15                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0x00                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LP\_ANA\_TOUCH\_PAD $n$ \_THO** Configures the touch threshold for touch sensor  $n$  for sampling frequency mode 0. (R/W)

Register 55.29. LP\_ANA\_TOUCH\_PAD $n$ \_TH1\_REG ( $n$ : 1-14) (0x0154+0xC\* $n$ )

|                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                                 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------------|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|---|
| LP_ANA_TOUCH_PAD <sup>n</sup> _TH1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)                      |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |   |
| 31                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                              | 15 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       | 0 |
| 0x00                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |   |

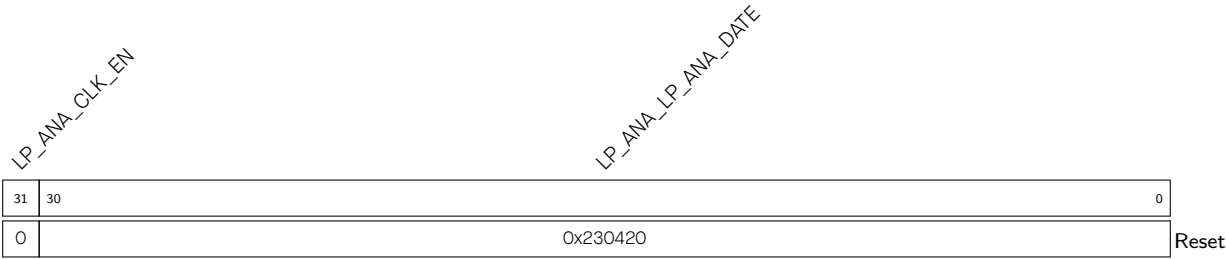
**LP\_ANA\_TOUCH\_PAD $n$ \_TH1** Configures the touch threshold of touch sensor  $n$  for sampling frequency mode 1. (R/W)

Register 55.30. LP\_ANA\_TOUCH\_PAD $n$ \_TH2\_REG ( $n$ : 1-14) (0x0158+0xC\* $n$ )

|                                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
|------------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|---------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|-------|
| LP_ANA_TOUCH_PAD <sup>n</sup> _TH2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | (reserved)                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |       |
| 31                                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16 | 15                              |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |       |
| 0x00                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   | Reset |

**LP\_ANA\_TOUCH\_PAD $n$ \_TH2** Configures the touch threshold of touch sensor  $n$  for sampling frequency mode 2. (R/W)

Register 55.31. LP\_ANA\_DATE\_REG (0x03FC)



- LP\_ANA\_LP\_ANA\_DATE Version control register. (R/W)
- LP\_ANA\_CLK\_EN Configures whether to enable the clock for accessing the registers.

0: Disable

1: Enable

(R/W)

## Chapter 56

# Temperature Sensor (TSENS)

## 56.1 Overview

ESP32-P4 provides a temperature sensor for real-time monitoring of temperature changes within the chip. The sensor converts analog voltage to digital values and provides compensation for temperature offsets.

## 56.2 Features

The temperature sensor has the following features:

- Software-triggered temperature measurement, which once triggered, the sensor continuously measures temperature. Software can read the data at any time.
- Hardware-triggered automatic temperature monitoring, supporting two wake-up modes
- Configurable temperature offset based on the application scenario for improved accuracy
- Configurable temperature measurement range
- Support for Event Task Matrix (ETM)-related events and tasks

## 56.3 Architecture

Figure [56.3-1](#) shows the internal structure of the temperature sensor.

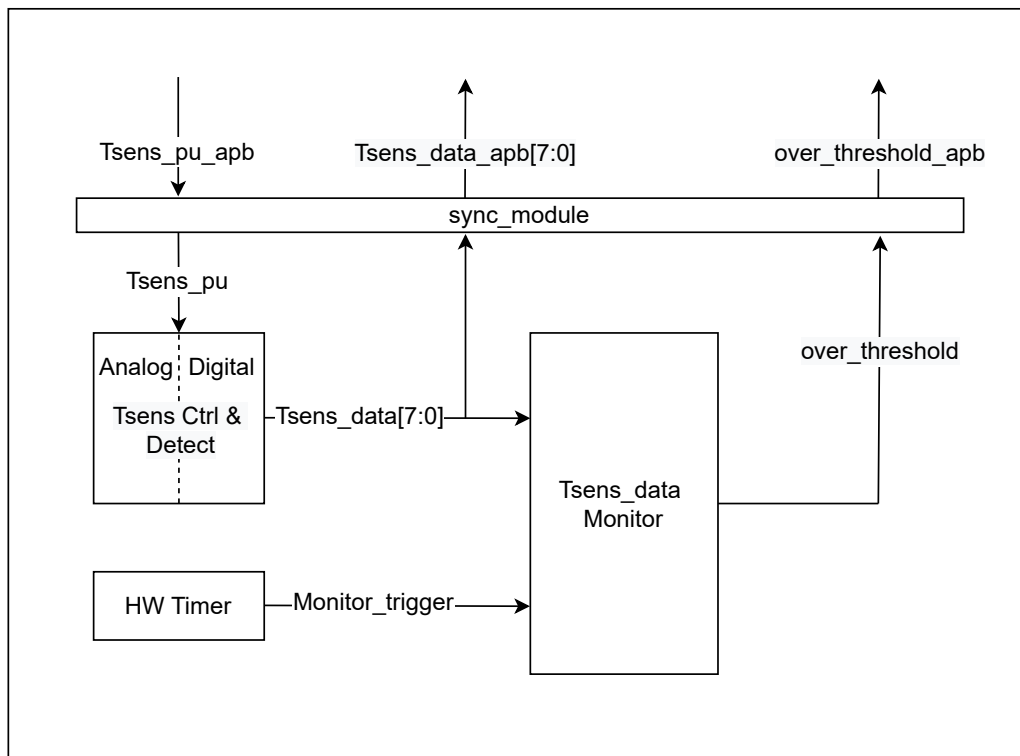


Figure 56.3-1. Temperature Sensor Architecture

As Figure 56.3-1 shows, the temperature sensor module contains the following major blocks:

- Tsens Ctrl & Detect: temperature sensor
- HW Timer: triggers automatic temperature monitoring
- Tsens\_data Monitor: monitors whether the temperature is outside the threshold range
- sync\_module: Synchronization block between APB clock domain and temperature sensor clock domain

## 56.4 Functional Description

### 56.4.1 Temperature Sensor Power Up

The temperature sensor can be powered up by setting the `TSENS_POWER_UP` register.

### 56.4.2 Temperature Sensor Clock

The temperature sensor has only one clock source: `LP_PERI_CLK`, and there is no frequency divider inside the module.

### 56.4.3 Wake-Up Modes for Automatic Temperature Monitoring

There are two wake-up modes for temperature monitoring, selected by `TSENS_WAKEUP_MODE`:

- Absolute value mode:

- Monitors the absolute value of the current temperature. Configure [TSENS\\_WAKEUP\\_TH\\_LOW](#) and [TSENS\\_WAKEUP\\_TH\\_HIGH](#) to set the temperature thresholds. Wake-up will be triggered if the sampled value is above the high threshold or below the low threshold.
- Change value mode:
  - Monitors the temperature changes inside the chip. If the temperature increment of two consecutive samplings exceeds the high threshold configured in [TSENS\\_WAKEUP\\_TH\\_HIGH](#), or the temperature decrement of two consecutive samplings exceeds the low threshold configured in [TSENS\\_WAKEUP\\_TH\\_LOW](#), a wake-up will be triggered. For example, when [TSENS\\_WAKEUP\\_TH\\_LOW](#) is set to 8, and the two consecutive sampling values are 28 and 19, resulting in a temperature decrement of 9, a wake-up will be triggered.

#### 56.4.4 Temperature Measurement Range and Offset

The temperature sensor is designed with five measurement ranges, as displayed in Table 56.4-1, to enhance accuracy. Each range has its own measurement errors, but users can select particular offsets to obtain calibrated data, so there is no need to be concerned about the errors.

**Table 56.4-1. Temperature Measurement Range and Offset**

| Temperature Measurement Range (°C) | Temperature Offset |
|------------------------------------|--------------------|
| 50 ~ 125                           | -2                 |
| 20 ~ 100                           | -1                 |
| -10 ~ 80                           | 0                  |
| -30 ~ 50                           | 1                  |
| -40 ~ 20                           | 2                  |

#### 56.4.5 Data Conversion

The sensor output value (*VALUE*) is stored in [TSENS\\_OUT](#). To calculate the actual temperature *T* (°C) based on *VALUE*, use the following equation:

$$T = 0.4386 * VALUE - 27.88 * offset - 20.52$$

where *offset* is the temperature offset displayed in Table 56.4-1.

### 56.5 Event Task Matrix Feature

The temperature sensor on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows the temperature sensor's ETM tasks to be triggered by any peripherals' ETM events, or temperature sensor's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to the temperature sensor. For more information, please refer to Chapter 12 [Event Task Matrix \(ETM\)](#).

The temperature sensor can receive the following ETM tasks:

- [TMPSNSR\\_TASK\\_START\\_SAMPLE](#): The temperature sensor starts sampling when this task is triggered.
- [TMPSNSR\\_TASK\\_STOP\\_SAMPLE](#): The temperature sensor stops sampling when this task is triggered.

The temperature sensor can generate the following ETM events:



- `TMPSNSR_EVT_OVER_LIMIT`: Generated when the temperature is beyond the threshold.

In practical applications, the temperature sensor's ETM events can trigger its own ETM tasks. For example, the `TMPSNSR_EVT_OVER_LIMIT` event can trigger the `TMPSNSR_TASK_STOP_SAMPLE` task.

## 56.6 Interrupts

ESP32-P4's Temperature Sensor can generate the following interrupt signal that will be sent to the [Interrupt Matrix](#).

- `LP_TSENS_INTR`

There is one internal interrupt source from the Temperature Sensor that can generate the above interrupt signal:

- `TSENS_COCPU_TSENS_WAKE_INT`: Triggered when the temperature sample value exceeds the threshold.

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter [11 Interrupt Matrix](#) > Section [11.2 Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [56.8 Register Summary](#).

## 56.7 Programming Procedure

The temperature sensor can be started by software as follows:

1. Set `TSENS_POWER_UP` to power up the temperature sensor.
2. Set `LPPERI_CK_EN_LP_TSENS` to enable the temperature sensor clock.
3. Wait for `TSENS_XPD_WAIT` clock cycles till the temperature sensor releases from reset and starts measuring the temperature.
4. Wait for 100  $\mu$ s (so that the output value gradually approaches the actual temperature) and then read the data from `TSENS_OUT`.

To enable hardware-triggered automatic temperature monitoring, add the following programming steps before powering up the sensor:

1. Configure `TSENS_SAMPLE_RATE` to set sampling rate.
2. Configure `TSENS_WAKEUP_MODE` to select wake-up mode for temperature monitoring.
3. Configure `TSENS_WAKEUP_TH_HIGH/LOW` to set the high and low temperature monitoring thresholds.
4. Set `TSENS_WAKEUP_EN` to start temperature monitoring.
5. Set `TSENS_SAMPLE_EN` to enable automatic temperature monitoring.

In automatic temperature monitoring mode, the output value will not be saved. Nevertheless, users can get the value at any moment by accessing `TSENS_OUT`.

## 56.8 Register Summary

The addresses in this section are relative to Temperature Sensor base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                   | Description  | Address | Access   |
|--|--|---------|----------|
| <b>Control Registers</b>               |  |         |          |
| <a href="#">TSENS_CTRL_REG</a>         | Temperature sensor control register 1.                   | 0x0000  | varies   |
| <a href="#">TSENS_CTRL2_REG</a>        | Temperature sensor control register 2.                   | 0x0004  | R/W      |
| <b>Interrupt Registers</b>             |  |         |          |
| <a href="#">TSENS_INT_RAW_REG</a>      | Raw register of temperature sensor interrupt.            | 0x0008  | R/WTC/SS |
| <a href="#">TSENS_INT_ST_REG</a>       | State register of temperature sensor interrupt.          | 0x000C  | RO       |
| <a href="#">TSENS_INT_ENA_REG</a>      | Enable register of temperature sensor interrupt.         | 0x0010  | R/WTC    |
| <a href="#">TSENS_INT_CLR_REG</a>      | Clear register of temperature sensor interrupt.          | 0x0014  | WT       |
| <a href="#">TSENS_INT_ENA_W1TS_REG</a> | <a href="#">TSENS_INT_ENA_REG</a> configuration register | 0x001C  | WT       |
| <a href="#">TSENS_INT_ENA_W1TC_REG</a> | <a href="#">TSENS_INT_ENA_REG</a> configuration register | 0x0020  | WT       |
| <b>Wake-up Control Registers</b>       |  |         |          |
| <a href="#">TSENS_WAKEUP_CTRL_REG</a>  | Temperature sensor wake-up control registers.            | 0x0024  | varies   |
| <a href="#">TSENS_SAMPLE_RATE_REG</a>  | Hardware automatic sampling control registers.           | 0x0028  | R/W      |

## 56.9 Registers

The addresses in this section are relative to Temperature Sensor base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

**Register 56.1. TSENS\_CTRL\_REG (0x0000)**

|            |  |  |  |  |  |  |  |  |  |                |  |  |  |  |  |  |  |  |  |               |    |     |  |  |  |  |  |  |  |              |  |    |    |  |  |  |  |  |  |            |  |  |    |   |   |   |     |  |  |                 |  |  |  |  |  |  |       |  |  |            |  |  |  |  |  |  |  |  |  |           |  |  |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--|--|----------------|--|--|--|--|--|--|--|--|--|---------------|----|-----|--|--|--|--|--|--|--|--------------|--|----|----|--|--|--|--|--|--|------------|--|--|----|---|---|---|-----|--|--|-----------------|--|--|--|--|--|--|-------|--|--|------------|--|--|--|--|--|--|--|--|--|-----------|--|--|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  |  |  | TSENS_POWER_UP |  |  |  |  |  |  |  |  |  | TSENS_CLK_DIV |    |     |  |  |  |  |  |  |  | TSENS_IN_INV |  |    |    |  |  |  |  |  |  | (reserved) |  |  |    |   |   |   |     |  |  | TSENS_SAMPLE_EN |  |  |  |  |  |  |       |  |  | (reserved) |  |  |  |  |  |  |  |  |  | TSENS_OUT |  |  |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  |  |  | 23             |  |  |  |  |  |  |  |  |  | 22            | 21 | 14  |  |  |  |  |  |  |  |              |  | 13 | 12 |  |  |  |  |  |  |            |  |  | 10 | 9 | 8 | 7 | 0   |  |  |                 |  |  |  |  |  |  |       |  |  |            |  |  |  |  |  |  |  |  |  |           |  |  |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  |  |  | 0              |  |  |  |  |  |  |  |  |  | 0             | 0  | 0x6 |  |  |  |  |  |  |  |              |  | 0  | 0  |  |  |  |  |  |  |            |  |  | 0  | 0 | 0 | 0 | 0x0 |  |  |                 |  |  |  |  |  |  | Reset |  |  |            |  |  |  |  |  |  |  |  |  |           |  |  |  |  |  |  |  |  |  |

**TSENS\_OUT** Stores the temperature sensor output value. (RO)

**TSENS\_SAMPLE\_EN** Configures whether to enable automatic temperature monitoring.

0: Disable

1: Enable

(R/W)

**TSENS\_IN\_INV** Configures whether to invert temperature sensor data.

0: No effect

1: Invert

(R/W)

**TSENS\_CLK\_DIV** Configures the clock division of the temperature sensor, which affects the frequency of temperature data generation by the analog circuits. (R/W)

**TSENS\_POWER\_UP** Configures whether to power up temperature sensor.

0: No effect

1: Power up

(R/W)

Register 56.2. TSENS\_CTRL2\_REG (0x0004)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |               |     |                 |    |                |  |  |  |  |  |  |  |  |       |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|---------------|-----|-----------------|----|----------------|--|--|--|--|--|--|--|--|-------|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | TSENS_CLK_INV |     | TSENS_XPD_FORCE |    | TSENS_XPD_WAIT |  |  |  |  |  |  |  |  |       |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 15 | 14            | 13  | 12              | 11 |                |  |  |  |  |  |  |  |  |       |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 1             | 0x0 | 0x2             |    |                |  |  |  |  |  |  |  |  | Reset |  |   |

**TSENS\_XPD\_WAIT** Configures the wait time (in clock cycles) for the sensor to release from reset.  
(R/W)

**TSENS\_XPD\_FORCE** Configures whether to enable force power up/down the temperature sensor.

- 0: Disable force power up function
- 1: Disable force power down function
- 2: Enable force power up temperature sensor
- 3: Enable force power down temperature sensor

(R/W)

**TSENS\_CLK\_INV** Configures the phase of the temperature sensor clock. (R/W)

Register 56.3. TSENS\_INT\_RAW\_REG (0x0008)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                |   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--------------------------------|---|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | TSENS_COCPU_TSENS_WAKE_INT_RAW |   |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                              | 0 |   |   |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                              | 0 | 0 | 0 | Reset |

**TSENS\_COCPU\_TSENS\_WAKE\_INT\_RAW** The raw interrupt status of the [TSENS\\_COCPU\\_TSENS\\_WAKE\\_INT](#). (R/WTC/SS)

### Register 56.4. TSENS\_INT\_ST\_REG (0x000C)

Diagram illustrating the structure of the TSENS\_COCPU\_TSENS\_WAKE\_INT\_ST register:

- Bits 31 down to 1 are reserved (indicated by a diagonal line and the text "(reserved)").
- Bit 0 is the Reset bit.

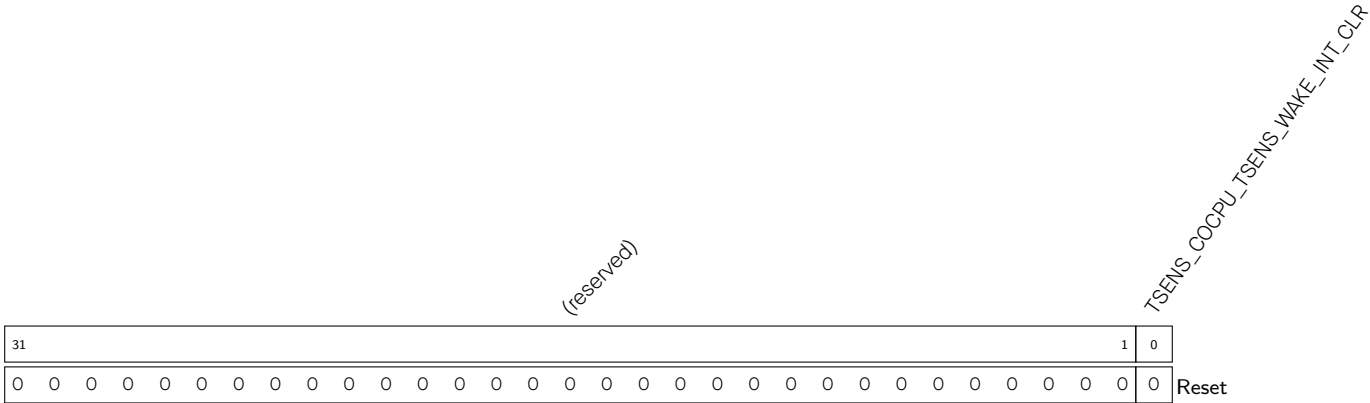
**TSENS\_COCPU\_TSENS\_WAKE\_INT\_ST** The masked interrupt status of the [TSENS\\_COCPU\\_TSENS\\_WAKE\\_INT](#). (RO)

### Register 56.5. TSENS\_INT\_ENA\_REG (0x0010)

Diagram of the TSENS\_C0CPU\_TSENS\_WAKE\_INT\_ENA register. The register is 32 bits wide. Bit 31 is labeled '31'. Bit 0 is labeled '0'. The register is divided into two sections: 'TSENS\_C0CPU\_TSENS\_WAKE\_INT\_ENA' (bits 0-31) and '(reserved)' (bits 32-63). The 'Reset' value for bit 0 is 0.

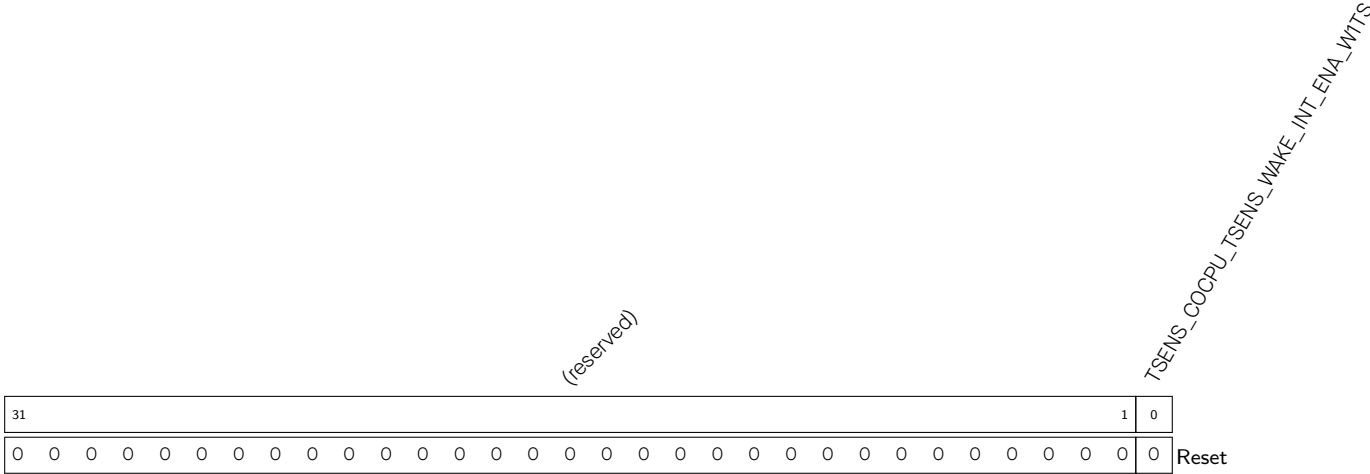
**TSENS\_COCPU\_TSENS\_WAKE\_INT\_ENA** Write 1 to enable [TSENS\\_COCPU\\_TSENS\\_WAKE\\_INT](#).  
(R/WTC)

Register 56.6. TSENS\_INT\_CLR\_REG (0x0014)



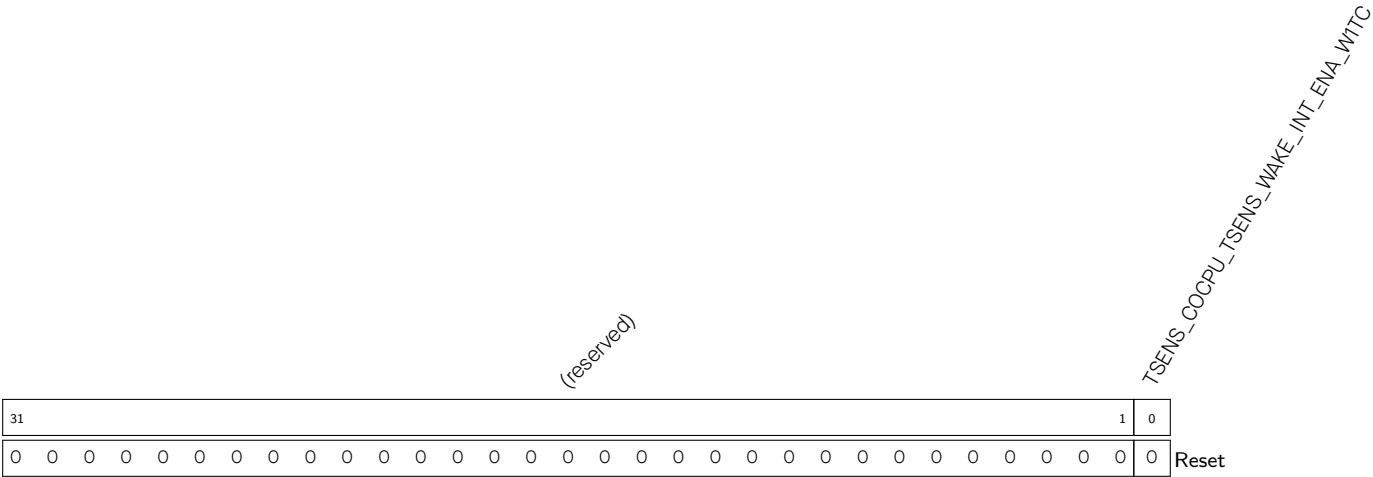
TSENS\_COCPU\_TSENS\_WAKE\_INT\_CLR Write 1 to clear TSENS\_COCPU\_TSENS\_WAKE\_INT. (WT)

Register 56.7. TSENS\_INT\_ENA\_WITS\_REG (0x001C)



TSENS\_COCPU\_TSENS\_WAKE\_INT\_ENA\_WITS Write 1 to set TSENS\_INT\_ENA\_REG. (WT)

Register 56.8. TSENS\_INT\_ENA\_W1TC\_REG (0x0020)



TSENS\_COCPU\_TSENS\_WAKE\_INT\_ENA\_W1TC Write 1 to clear TSENS\_INT\_ENA\_REG. (WT)

Register 56.9. TSENS\_WAKEUP\_CTRL\_REG (0x0024)

|                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|----------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| TSENS_WAKEUP_MODE          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TSENS_WAKEUP_TH_HIGH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | TSENS_WAKEUP_TH_LOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| TSENS_WAKEUP_EN            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| TSENS_WAKEUP_OVER_UPPER_TH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | (reserved)           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**TSENS\_WAKEUP\_TH\_LOW** Configures the low threshold for temperature monitoring wake-up function. (R/W)

**TSENS\_WAKEUP\_TH\_HIGH** Configures the high threshold for temperature monitoring wake-up function. (R/W)

**TSENS\_WAKEUP\_OVER\_UPPER\_TH** Represents whether the temperature output value exceeds the threshold.

0: The temperature output value is below the low threshold.

1: The temperature output value is above the high threshold.

(RO)

**TSENS\_WAKEUP\_EN** Configures whether to enable temperature monitoring wake-up function.

0: Disable

1: Enable

(R/W)

**TSENS\_WAKEUP\_MODE** Selects the wake-up mode for temperature monitoring. Valid only when [TSENS\\_WAKEUP\\_EN](#) = 1.

0: Absolute value mode

1: Change value mode

(R/W)

Register 56.10. TSENS\_SAMPLE\_RATE\_REG (0x0028)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----|-------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    | TSENS_SAMPLE_RATE |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 16 | 15                |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0x14              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| Reset      |   |   |   |   |   |   |   |   |   |   |   |   |   |   |    |                   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**TSENS\_SAMPLE\_RATE** Configures the sampling rate for hardware-triggered temperature monitoring. The sampling period = configured value × sensor's working clock cycle. (R/W)



## Chapter 57

### ADC Controller (ADC)

#### 57.1 Overview

ESP32-P4 integrates two 12-bit successive approximation ADCs (SAR ADCs) for measuring analog signals from up to 14 pins. Figure 57.1-1 shows the basic architecture of the SAR ADC module on ESP32-P4.

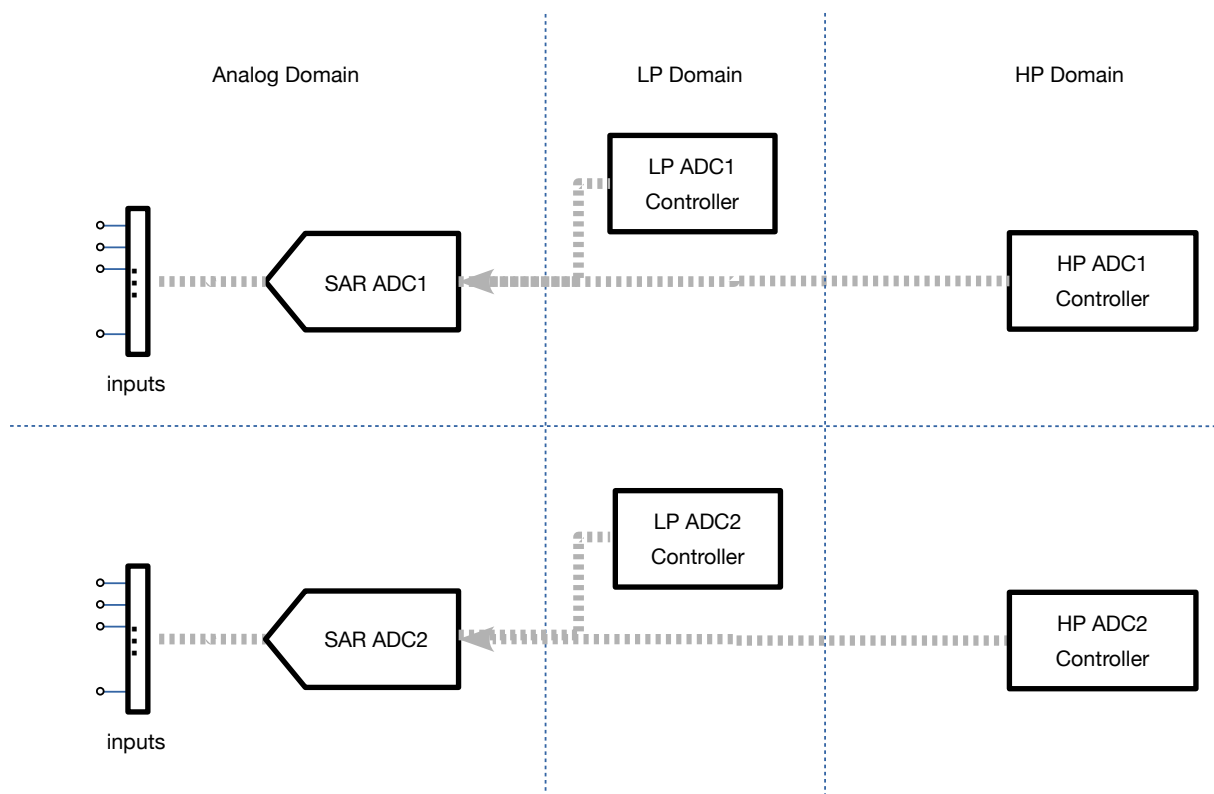


Figure 57.1-1. SAR ADC Simplified Architecture

As the figure shows, the SAR ADCs are managed by four dedicated controllers:

- Two HP (high-performance) controllers: HP ADC1 Controller and HP ADC2 Controller, designed for multi-channel sampling mode, supporting continuous transfer of conversion results to memory via the GDMA interface.
- Two LP (low-power) controllers: LP ADC1 Controller and LP ADC2 Controller, supporting operation in sleep mode and one-shot sampling mode.

## 57.2 Terminology

The following terms related to SAR ADC are defined in the context of the *ESP32-P4 Technical Reference Manual* to help readers better understand this document:

|                                     |   |
|-------------------------------------|---|
| <b>SAR ADC:</b>                     | Including analog ADC circuit and digital ADC controller. The HP ADC and LP ADC in the following text share the analog ADC circuit, but have their own controllers, namely the HP ADC controllers and LP ADC controllers. The SAR ADC mentioned in the text refers to both HP ADC and LP ADC.  |
| <b>HP ADC:</b>                      | High-performance ADC, supporting multi-channel sampling, GDMA data transfer, etc., not available in sleep mode.   |
| <b>LP ADC:</b>                      | Low-power ADC, supporting one-shot sampling mode, can be used in sleep mode.  |
| <b>One-shot sampling mode:</b>      | In this mode, LP ADC samples one channel at a time.   |
| <b>Multi-channel sampling mode:</b> | In this mode, HP ADC sequentially samples a group of channels or continuously samples a single channel.   |
| <b>Dual HP ADC sampling:</b>        | It means two HP ADCs sample either simultaneously or alternatively.   |
| <b>Conversion result:</b>           | The conversion result is the binary digital value obtained after the analog-to-digital conversion process. It is sometimes written as conversion data.  |
| <b>Filtered data:</b>               | Filtered data is the result of processing conversion data through a filter.   |
| <b>Sampling:</b>                    | The term typically refers to the entire process of sampling analog inputs, converting the sampled data, and transferring the conversion results to memory. In certain contexts and stages of the process, sampling may also refer to the SAR ADC capturing data points from an analog signal. |

## 57.3 Features

The SAR ADCs have the following features:

- Support HP ADC<sub>x</sub> controllers and LP ADC<sub>x</sub> controllers to get control of SAR ADC<sub>x</sub> via software, <sub>x</sub> = 1, 2
- 12-bit resolution
- Analog inputs sampling from up to 14 pins
- HP ADC<sub>x</sub> controllers:
  - Provide multi-channel sampling control module, supporting multi-channel sampling mode, with configurable channel sampling sequence
  - Provide mode control module, supporting dual HP ADC sampling
  - Provide two filters with configurable filter coefficients

- Provide two threshold monitors that can trigger an interrupt when the filtered data is above a high threshold or below a low threshold
- Support continuous transfer of conversion results to memory via the GDMA interface
- LP ADC~~x~~ controllers:
  - Support one-shot sampling mode
  - Support sampling in sleep mode (e.g., Deep-sleep)
- Support for several Event Task Matrix (ETM) related events and tasks

## 57.4 Architecture

The major components of SAR ADCs and their interconnections are shown in Figure 57.4-1.

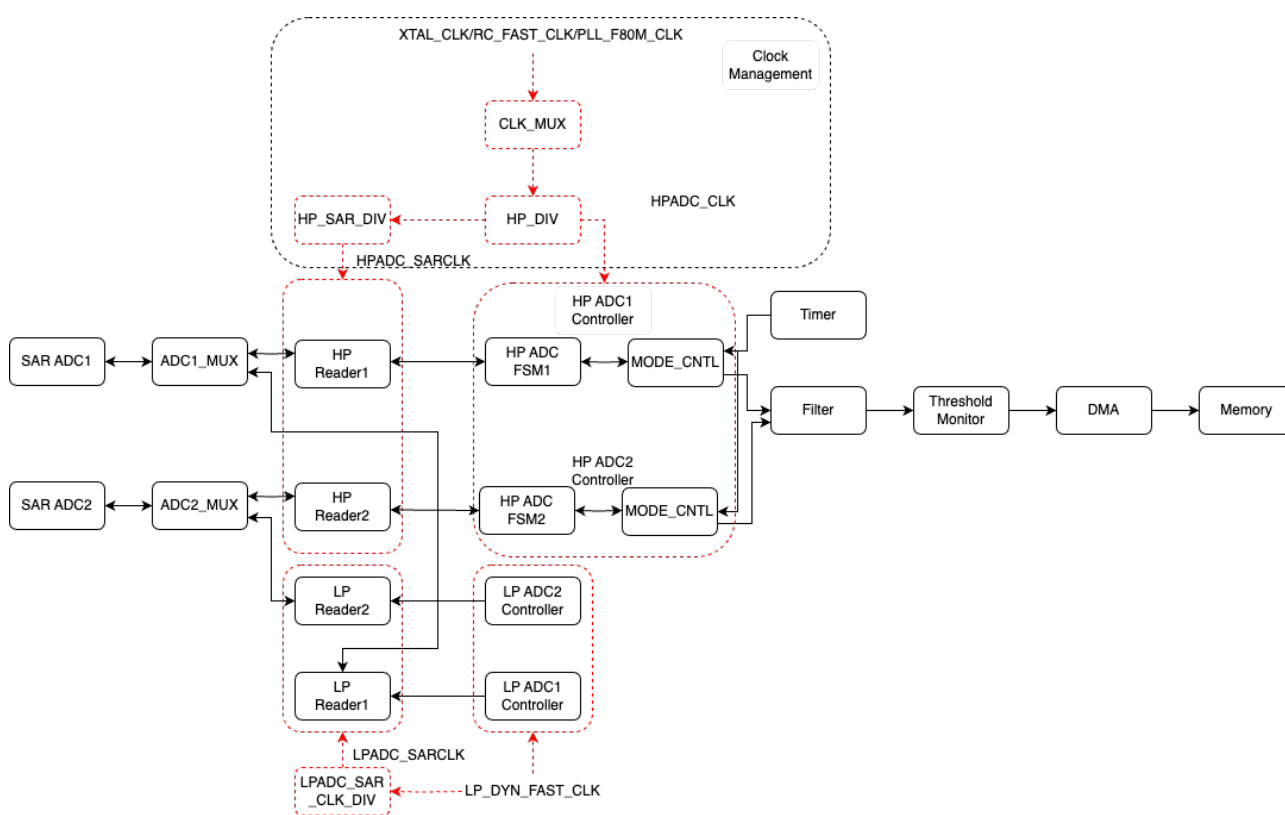


Figure 57.4-1. SAR ADC Architecture

- →: clock signals
- : clock divider, clock mux, and the blocks the clock works for

As Figure 57.4-1 shows, the SAR ADC module contains the following major functional blocks:

- SAR ADC1: Samples analog inputs from up to 8 pins
- SAR ADC2: Samples analog inputs from up to 6 pins
- Clock Management: Selects clock source and division
- Timer: Dedicated timer for the HP ADC~~x~~ controllers to generate sampling enable signal.
- HP ADC FSM~~x~~: FSM1 and FSM2 that can:

- receive the sampling enable signal from the timer.
  - determine the conversion rules defined in the patterns for HP ADC<sub>x</sub>.
  - drive the HP Reader<sub>x</sub> module to read conversion data.
  - transfer conversion data to the filter.
- Filter: Filter0 and filter1, used for filtering conversion results in multi-channel sampling mode.
  - Threshold Monitor: Threshold monitor 0 and threshold monitor 1 that trigger an interrupt when the filtered data is above a high threshold or below a low threshold.
  - MODE\_CNTL: Used for filtering the sampling signal triggered by the timer, supporting dual HP ADC sampling mode.
  - HP Reader<sub>x</sub>: HP reader 1 and HP reader 2, driven by HP ADC FSM<sub>x</sub> to read data from HP ADC<sub>x</sub>.
  - LP Reader<sub>x</sub>: LP reader 1 and LP reader 2, driven by LP ADC<sub>x</sub> Controller to read data from LP ADC<sub>x</sub>.
  - LP ADC<sub>x</sub> Controller: LP ADC1 Controller and LP ADC2 Controller. The controllers provide sampling enable signal, drive the LP Reader<sub>x</sub> module to read the conversion results of LP ADC<sub>x</sub>, and store the conversion results.

## 57.5 Functional Description

### 57.5.1 SAR ADC Power Up

The SAR ADCs can be powered up by setting [PMU\\_XPD\\_PERIF\\_I2C](#) and [PMU\\_PERIF\\_I2C\\_RST](#). The ADC sampling can be conducted immediately after power-up. Users need not be concerned about wait time, as it has been accounted for in the hardware design.

### 57.5.2 SAR ADC Channels

The SAR ADCs have 14 channels that are connected to 14 pins on the chip. To sample an analog signal, the SAR ADCs must first select the analog pin to measure via an internal multiplexer.

Table [57.5-1](#) shows the pins used as SAR ADC channels.

**Table 57.5-1. SAR ADC Channels and Chip Pins**

| Chip Pins | SAR ADC Channel | SAR ADC Selection |
|-----------|-----------------|-------------------|
| GPI016    | 0               | SAR ADC1          |
| GPI017    | 1               |                   |
| GPI018    | 2               |                   |
| GPI019    | 3               |                   |
| GPI020    | 4               |                   |
| GPI021    | 5               |                   |
| GPI022    | 6               |                   |
| GPI023    | 7               |                   |
| GPI049    | 0               |                   |
| GPI050    | 1               |                   |

SAR ADC2

| Chip Pins | SAR ADC Channel | SAR ADC Selection |
|-----------|-----------------|-------------------|
| GPIO51    | 2               |                   |
| GPIO52    | 3               |                   |
| GPIO53    | 4               |                   |
| GPIO54    | 5               |                   |

### 57.5.3 SAR ADC Clock

The clock for the HP ADC<sub>x</sub> Controller has three possible sources, selected by [HP\\_SYS\\_CLKRST\\_ADC\\_CLK\\_SRC\\_SEL](#):

- XTAL\_CLK
- RC\_FAST\_CLK
- PLL\_F80M\_CLK

The following clocks can be divided from the HP ADC<sub>x</sub> Controller's clock:

- HPADC\_SARCLK: It is the operating clock of HP ADC<sub>x</sub> and HP Reader<sub>x</sub>.
- HPADC\_CLK: It is the operating clock of HP ADC FSM<sub>x</sub>.

The frequency of HPADC\_SARCLK can affect the sampling accuracy. If the HPADC\_SARCLK frequency is higher than 5 MHz, the sampling accuracy will decrease. HPADC\_SARCLK is divided from HPADC\_CLK via a dedicated divider. The division is set in [ADC\\_SAR\\_CLK\\_DIV](#).

It takes 25 HPADC\_SARCLK clock cycles to complete one sampling, so the maximum sampling rate is limited by the frequency of HPADC\_SARCLK.

The LP ADC<sub>x</sub> Controller is clocked from LP\_DYN\_FAST\_CLK.

The following clocks can be divided from the LP ADC<sub>x</sub> Controller's clock:

- LPADC\_SARCLK: It is the operating clock of LP ADC<sub>x</sub> and LP Reader<sub>x</sub>. The division set in [LPADC\\_SAR1\\_CLK\\_DIV](#) and [LPADC\\_SAR2\\_CLK\\_DIV](#) should be at least 2. The frequency of LPADC\_SARCLK should not exceed 5 MHz.
- LPADC\_CLK: It is the operating clock of LP ADC FSM<sub>x</sub>.

For more information about clocks, please refer to Chapter 9 [Reset and Clock](#).

### 57.5.4 SAR ADC Conversion and Attenuation

The SAR ADCs can measure analog voltages from 0 mV to  $V_{ref}$ .  $V_{ref}$  is the SAR ADCs' internal reference voltage. The conversion result (*data*) is a 12-bit digital value, which is the raw data. To calculate the voltage  $V_{data}$  based on the raw data, the following formula can be used:

$$V_{data} = \frac{V_{ref}}{4095} \times data$$

To convert voltages larger than  $V_{ref}$ , apply attenuation to the input signals. The attenuation can be configured to 0 dB, 2.5 dB, 6 dB, or 12 dB.

### 57.5.5 HP ADC FSM

In multi-channel sampling mode HP ADC FSM (hereinafter referred to as FSM) generates all types of signals used in the sampling process. Figure 57.5-1 illustrates how the FSM works.

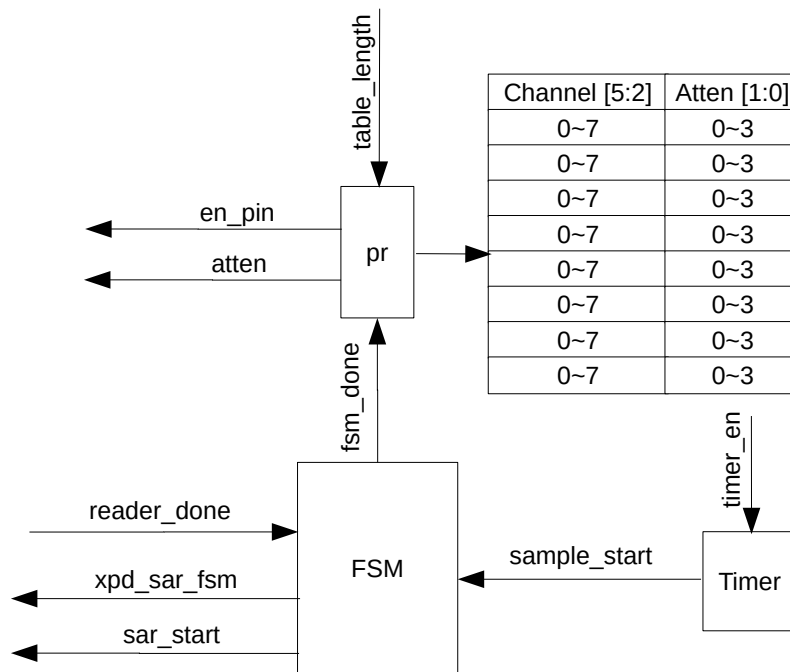


Figure 57.5-1. HP ADC FSM Block Diagram

Wherein:

- Timer: a dedicated timer for the HP ADC controller to generate **sample\_start** signal.
- pr: a pointer to the pattern table that defines the conversion rules for HP ADC. FSM sends out corresponding signals based on the conversion rules.

Set [ADC\\_TIMER\\_EN](#) to enable the timer. The timeout event of this timer triggers a **sample\_start** signal. This signal drives the FSM module to start sampling. When the FSM module receives the **sample\_start** signal, it starts the following operations:

- Powers up HP ADC.
- Determines the conversion rules (selected sample channels and attenuations) defined in the patterns that the current pr points to.
- Outputs the **en\_pin** and **atten** signals corresponding to the conversion rules to the analog side.
- Initiates the **sar\_start** signal and starts sampling.

When FSM receives the **reader\_done** signal from HP Reader, it starts the following operations:

- Stops sampling.
- Transfers the conversion result to the filter. Then the threshold monitor transfers the filtered result to memory via GDMA (see Figure 57.4-1).

- Updates `pr` and waits for the next sampling. The pointer `pr` counts cyclically between 0 and `ADC_SAR1/2_PATT_LEN` (`table_length`).

### 57.5.6 HP ADC Pattern Table

HP ADC FSM1/2 each contain a pattern table configured by `ADC_SARx_PATT_TAB $m$ _REG`, with  $m$  indicating registers 1 ~ 4. Each register contains four patterns and each pattern is 6 bits wide, as below shows.

|                 |  |  |  |  |  |  |  |        |  |  |  |  |  |      |  |        |  |  |  |      |  |  |  |        |  |      |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|--------|--|--|--|--|--|------|--|--------|--|--|--|------|--|--|--|--------|--|------|--|--|--|--|--|--------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | cmd0   |  |  |  |  |  | cmd1 |  |        |  |  |  | cmd2 |  |  |  |        |  | cmd3 |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 24     |  |  |  |  |  |      |  | 23     |  |  |  |      |  |  |  | 18     |  |      |  |  |  |  |  | 17     |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 6 |  |  |  |  |  |  |  | 5 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000 |  |  |  |  |  |      |  | 0x0000 |  |  |  |      |  |  |  | 0x0000 |  |      |  |  |  |  |  | 0x0000 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

`cmd  $n$`  ( $n = 0 - 3$ ) represents patterns 0 ~ 3.

Figure 57.5-2. `ADC_SARx_PATT_TAB1_REG` Contains Patterns 0 - 3

|            |  |  |  |  |  |  |  |        |  |  |  |  |  |        |  |  |  |  |  |        |  |  |  |  |  |        |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|--------|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  | cmd4   |  |  |  |  |  | cmd5   |  |  |  |  |  | cmd6   |  |  |  |  |  | cmd7   |  |  |  |  |  |
| 3124       |  |  |  |  |  |  |  | 2318   |  |  |  |  |  | 1712   |  |  |  |  |  | 116    |  |  |  |  |  | 50     |  |  |  |  |  |
| 00000000   |  |  |  |  |  |  |  | 0x0000 |  |  |  |  |  | 0x0000 |  |  |  |  |  | 0x0000 |  |  |  |  |  | 0x0000 |  |  |  |  |  |

`cmd  $n$`  ( $n = 4 - 7$ ) represents patterns 4 ~ 7.

Figure 57.5-3. `ADC_SARx_PATT_TAB2_REG` Contains Patterns 4 - 7

|                 |  |  |  |  |  |  |  |        |  |  |  |  |  |      |  |        |  |  |  |       |  |  |  |        |  |       |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|--------|--|--|--|--|--|------|--|--------|--|--|--|-------|--|--|--|--------|--|-------|--|--|--|--|--|--------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | cmd8   |  |  |  |  |  | cmd9 |  |        |  |  |  | cmd10 |  |  |  |        |  | cmd11 |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 24     |  |  |  |  |  |      |  | 23     |  |  |  |       |  |  |  | 18     |  |       |  |  |  |  |  | 17     |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 6 |  |  |  |  |  |  |  | 5 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000 |  |  |  |  |  |      |  | 0x0000 |  |  |  |       |  |  |  | 0x0000 |  |       |  |  |  |  |  | 0x0000 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

`cmd  $n$`  ( $n = 8 - 11$ ) represents patterns 8 ~ 11.

Figure 57.5-4. `ADC_SARx_PATT_TAB3_REG` Contains Patterns 8 - 11

|                 |  |  |  |  |  |  |  |        |  |  |  |  |  |       |  |        |  |  |  |       |  |  |  |        |  |       |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|--------|--|--|--|--|--|-------|--|--------|--|--|--|-------|--|--|--|--------|--|-------|--|--|--|--|--|--------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | cmd12  |  |  |  |  |  | cmd13 |  |        |  |  |  | cmd14 |  |  |  |        |  | cmd15 |  |  |  |  |  |        |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 24     |  |  |  |  |  |       |  | 23     |  |  |  |       |  |  |  | 18     |  |       |  |  |  |  |  | 17     |  |  |  |  |  |  |  | 12 |  |  |  |  |  |  |  | 11 |  |  |  |  |  |  |  | 6 |  |  |  |  |  |  |  | 5 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000 |  |  |  |  |  |       |  | 0x0000 |  |  |  |       |  |  |  | 0x0000 |  |       |  |  |  |  |  | 0x0000 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

`cmd  $n$`  ( $n = 12 - 15$ ) represents patterns 12 ~ 15.

Figure 57.5-5. `ADC_SARx_PATT_TAB4_REG` Contains Patterns 12 - 15

Each pattern is 6 bits wide, consisting of two fields where conversion rules are stored. Figure 57.5-6 shows the pattern format and is followed by the descriptions of each field.

| ch_sel |   | atten |   |
|--------|---|-------|---|
| 5      | 2 | 1     | 0 |
| xx     |   | x     | x |

Figure 57.5-6. Pattern Structure

**atten** Configures attenuation:

- 0: 0 dB
- 1: 2.5 dB
- 2: 6 dB
- 3: 12 dB

**ch\_sel** Configures channel. For HP ADC1, values 0-7 correspond to channels 0-7 individually, for HP ADC2, values 2-7 correspond to channels 0-5 individually.

### 57.5.7 HP ADC Pattern Configuration Example for Multi-channel Sampling

Assuming you want to implement the following sequence of HP ADC1 multi-channel sampling:

- Sample channel 2 of HP ADC1 with attenuation of 12 dB;
- Sample channel 0 of HP ADC1 with attenuation of 2.5 dB.

Then, the detailed configuration is as follows:

- Configure the first pattern (cmd0) of `ADC_SAR1_PATT_TAB1_REG[5:0]`:

| ch_sel |   | atten |   |
|--------|---|-------|---|
| 5      | 2 | 1     | 0 |
| 2      |   | 3     |   |

Figure 57.5-7. cmd0 configuration

**atten** write 3 to this field, to set the attenuation to 12 dB.

**ch\_sel** write 2 to this field, to select channel 2.

- Configure the second pattern (cmd1) of `ADC_SAR1_PATT_TAB1_REG[11:6]`:

| ch_sel |   | atten |   |
|--------|---|-------|---|
| 5      | 2 | 1     | 0 |
| 0      |   | 1     |   |

Figure 57.5-8. cmd1 Configuration

**atten** write 1 to this field, to set the attenuation to 2.5 dB.

**ch\_sel** write 0 to this field, to select channel 0.

- Configure `ADC_SAR1_PATT_LEN` to 1, i.e., set pattern table size to (this value + 1) = 2. Then patterns cmd0 and cmd1 will be used.
- Enable the timer so that the HP ADC1 Controller starts sampling the two channels periodically.



## 57.5.8 Dual HP ADC Sampling Control

`ADC_WORK_MODE` controls how two HP ADCs work together:

- 0: Single HP ADC sampling, i.e., only one HP ADC samples. When a sampling request is triggered by the timer, `ADC_SAR_SEL` controls which FSM receives the sampling request:
  - 0: HP ADC FSM1, i.e., using HP ADC1 for sampling.
  - 1: HP ADC FSM2, i.e., using HP ADC2 for sampling.
- 1: Dual HP ADC simultaneous sampling. When a sampling request is triggered by the timer, both HP ADC FSM1 and HP ADC FSM2 receive the sampling request.
- 2: Dual HP ADC alternative sampling. When an odd number of sampling requests are triggered by the timer, HP ADC FSM1 receives the sampling request. When an even number of sampling requests are triggered by the timer, HP ADC FSM2 receives the sampling request.

## 57.5.9 HP ADC Filters

The HP ADC<sub>x</sub> controllers provide two filters for filtering conversion results in multi-channel sampling mode. Both filters can be configured to any HP ADC channel, but cannot be configured to the same channel. If the two filters are configured to the same channel, the first one takes effect.

The filtered data is determined by the following equation:

$$data_{cur} = \frac{(k-1)data_{prev}}{k} + \frac{data_{in}}{k} + 0.5$$

- $data_{cur}$ : the filtered data
- $data_{in}$ : the conversion result
- $data_{prev}$ : the last filtered data
- $k$ : the filter coefficient

The filters are configured as follows:

- Configure `ADC_FILTER_CHANNELx` to select the HP ADC channel for filter  $x$ ,  $x=0, 1$ .
- Configure `ADC_FILTER_FACTORx` to set the coefficient  $k$  for filter  $x$ ,  $x=0, 1$ .

## 57.5.10 HP ADC Threshold Monitors

The HP ADC<sub>x</sub> controllers provide two threshold monitors to monitor the filtered data in multi-channel sampling mode. When the data is above the high threshold, a high threshold interrupt is triggered; when the data is below the low threshold, a low threshold interrupt is triggered. Both monitors can be configured to any HP ADC channel, but cannot be configured to the same channel.

Threshold monitors are configured as follows:

- Set `ADC_THRESx_EN` to enable threshold monitor  $x$  ( $x=0, 1$ ).
- Configure `ADC_THRESx_LOW` to set a low threshold.
- Configure `ADC_THRESx_HIGH` to set a high threshold.

- Configure `ADC_THRESx_CHANNEL` to select the channel to monitor.

### 57.5.11 HP ADC GDMA Support

When HP ADC converts data on multiple channels, it is necessary to enable GDMA so that the data can be transferred to memory continuously.

GDMA support is triggered by the timer in the HP ADC<sub>x</sub> controllers. Users can switch the GDMA data path to the HP ADC controller by configuring `ADC_APB_ADC_TRANS`. For specific GDMA configuration, please refer to Chapter 3 *GDMA Controller (GDMA-AHB, GDMA-AXI)*.

The HP ADC eventually passes 32-bit data to GDMA. The data format is shown in Figure 57.5-9.

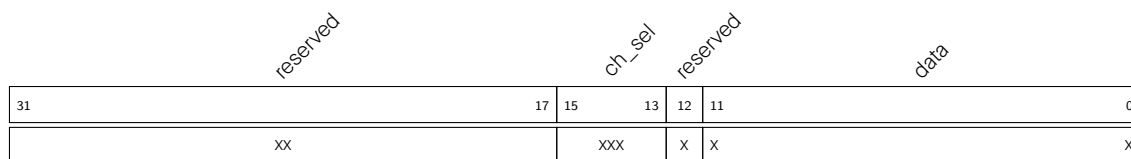


Figure 57.5-9. GDMA Data Format

**data** 12-bit HP ADC conversion result

**ch\_sel** 3-bit channel information

### 57.5.12 LP ADC Wake-Up Modes for Automatic Monitoring

The LP ADC<sub>x</sub> controllers support automatic monitoring of the conversion data. A dedicated timer generates LP ADC sampling signals periodically based on the value of `LPADC_ADCx_HW_READ_RATE_I`. Then the conversion data is fed into a threshold monitor (not the HP ADC threshold monitors). If the data exceeds the threshold, an interrupt will be generated.

There are two wake-up modes for automatic monitoring, selected by `LPADC_SARx_WAKEUP_MODE`:

- 0: Absolute value mode  
Monitors the absolute value of the conversion data. Configure `LPADC_SARx_WAKEUP_TH_LOW` and `LPADC_SARx_WAKEUP_TH_HIGH` to set the thresholds. Wake-up will be triggered if the data is above the high threshold or below the low threshold.
- 1: Change value mode  
Monitors the changes of the conversion data. If the increment of two consecutive samplings exceeds the high threshold configured in `LPADC_SARx_WAKEUP_TH_HIGH`, or the decrement of two consecutive samplings exceeds the low threshold configured in `LPADC_SARx_WAKEUP_TH_LOW`, a wake-up will be triggered. For example, when `LPADC_SARx_WAKEUP_TH_LOW` is set to 8, and the two consecutive conversion results are 28 and 19, resulting in a decrement of 9, a wake-up will be triggered.

## 57.6 Event Task Matrix Feature

The SAR ADC on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows SAR ADC's ETM tasks to be triggered by any peripherals' ETM events, or SAR ADC's ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM tasks and events related to SAR ADC. For more information, please refer to Chapter 12 *Event Task Matrix (ETM)*.

The SAR ADC can receive the following ETM tasks:

- ADC\_TASK\_SAMPLEO: LP ADC starts one-shot sampling when this task is triggered.
- ADC\_TASK\_STARTO: HP ADC starts multi-channel sampling when this task is triggered.
- ADC\_TASK\_STOPO: SAR ADC stops sampling when this task is triggered.

The SAR ADC can generate the following ETM events:

- ADC\_EVT\_CONV\_CMPLTO: Generated each time SAR ADC completes a sampling in either one-shot sampling mode or multi-channel sampling mode.
- ADC\_EVT\_EQ\_ABOVE\_THRESH<sub>x</sub>: Generated when the HP ADC's filtered data is above the threshold. <sub>x</sub> = 0, 1, representing threshold monitor 0, 1.
- ADC\_EVT\_EQ\_BELOW\_THRESH<sub>x</sub>: Generated when the HP ADC's filtered data is below the threshold. <sub>x</sub> = 0, 1, representing threshold monitor 0, 1.
- ADC\_EVT\_STARTEDO: Generated when SAR ADC begins sampling; one-shot sampling will not trigger this event.
- ADC\_EVT\_STOPPEDO: Generated when SAR ADC stops sampling, one-shot sampling will not trigger this event.

In practical applications, SAR ADC's ETM events can trigger its own ETM tasks. For example, the ADC\_EVT\_EQ\_ABOVE\_THRESH<sub>x</sub> event can trigger the ADC\_TASK\_STOPO task.

## 57.7 Interrupts

ESP32-P4's SAR ADC can generate the following interrupt signals that will be sent to the [Interrupt Matrix](#).

- ADC\_INTR
- LP\_ADC\_INTR

The following internal interrupt sources from SAR ADC can generate the interrupt signal ADC\_INTR:

- ADC\_SAR<sub>x</sub>\_DONE\_INT: Triggered when HP ADC<sub>x</sub> completes one sampling.
- ADC\_THRES<sub>x</sub>\_HIGH\_INT: Triggered when the filtered data is above the high threshold.
- ADC\_THRES<sub>x</sub>\_LOW\_INT: Triggered when the filtered data is below the low threshold.

The following internal interrupt sources from SAR ADC can generate the interrupt signal LP\_ADC\_INTR:

- LPADC\_COCPU\_SARADC<sub>x</sub>\_DONE\_INT: Triggered when LP ADC<sub>x</sub> completes one sampling.
- LPADC\_COCPU\_SARADC<sub>x</sub>\_ERROR\_INT: Triggered when sampling error occurs.
- LPADC\_COCPU\_SARADC<sub>x</sub>\_WAKE\_INT: Triggered when LP ADC<sub>x</sub> generates a wake-up event (such as conversion data exceeding the threshold).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section [57.9 Register Summary](#).

## 57.8 Programming Procedure

### 57.8.1 HP ADC Multi-Channel Sampling Mode

The multi-channel sampling mode can be configured with the following procedure:

1. Set [PMU\\_XPD\\_PERIF\\_I2C](#) and [PMU\\_PERIF\\_I2C\\_RST](#) to power up HP ADC.
2. Configure [HP\\_SYS\\_CLKRST\\_ADC\\_CLK\\_SRC\\_SEL](#) to select HP ADC clock source.
3. Configure [HP\\_SYS\\_CLKRST\\_ADC\\_CLK\\_DIV\\_NUM](#) and [HP\\_SYS\\_CLKRST\\_ADC\\_SARx\\_CLK\\_DIV\\_NUM](#) to set clock division.
4. Set [HP\\_SYS\\_CLKRST\\_ADC\\_CLK\\_EN](#) to enable HP ADC clock.
5. Set [LPADC\\_SARx\\_DIG\\_FORCE](#) to enable the sampling channel.
6. Configure the pattern table as described in Section [57.5.6 HP ADC Pattern Table](#).
7. Configure channels and filtering coefficients as described in Section [57.5.9 HP ADC Filters](#).
8. Configure threshold monitoring as described in Section [57.5.10 HP ADC Threshold Monitors](#), as needed.
9. Set [ADC\\_APB\\_ADC\\_TRANS](#) to use GDMA.
10. Configure [ADC\\_TIMER\\_TARGET](#) to set trigger target for HP ADC timer.
11. Set [ADC\\_TIMER\\_EN](#) to enable the timer.

The timer timeout will trigger HP ADC FSM to start sampling according to the pattern table. The conversion result will be automatically stored in memory. When the sampling reaches the specified limit in [ADC\\_APB\\_ADC\\_EOF\\_NUM](#), it will terminate.

Once sampling is complete, an [ADC\\_SARx\\_DONE\\_INT\\_RAW](#) interrupt will be generated.

### 57.8.2 LP ADC One-shot Sampling Mode

The one-shot sampling mode can be configured with the following procedure:

1. Set [PMU\\_XPD\\_PERIF\\_I2C](#) and [PMU\\_PERIF\\_I2C\\_RSTB](#) to power up LP ADC.
2. Configure [LPPERI\\_LPADC\\_FUNC\\_DIV\\_NUM](#) and [LPPERI\\_LPADC\\_SARx\\_DIV\\_NUM](#) to set the frequency of [LPADC\\_CLK](#) and [LPADCx\\_SARCLK](#).
3. Configure [LPADC\\_SARx\\_EN\\_PAD](#) and [LPADC\\_SARx\\_ATTEN](#) to select sampling channels and attenuation.
4. Set [LPADC\\_SAR\\_MEASx\\_START\\_SAR](#) to enable the one-shot sampling mode of LP ADCx.

Once sampling is complete, an [LPADC\\_COCPU\\_SARADCx\\_INT\\_RAW](#) interrupt is generated. Software can read the conversion result from [LPADC\\_SAR\\_MEASn\\_DATA\\_SAR](#).

### 57.8.3 LP ADC Automatic Monitoring

The configuration process for the automatic monitoring of the LP ADC controller is as follows:

1. Configure [LPADC\\_ADCx\\_HW\\_READ\\_RATE\\_I](#) to set the sampling rate.
2. Configure [LPADC\\_SARx\\_WAKEUP\\_MODE](#) to select the wake-up mode.

3. Configure `LPADC_SARx_WAKEUP_TH_HIGH` and `LPADC_SARx_WAKEUP_TH_LOW` to set the high and low thresholds.
4. Set `LPADC_SARx_WAKEUP_EN` to enable automatic monitoring.
5. Set `LPADC_ADCx_HW_READ_EN_I` to enable periodic monitoring.

During the automatic monitoring process, the conversion data will not be stored, but software can always read the last conversion data from `LPADC_SAR_MEASn_DATA_SAR`.

## 57.9 Register Summary

### 57.9.1 HP ADC Register Summary

The addresses in the table below are relative to the base address of HP ADC (written as ADC Controller) in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                    | Description                                   | Address | Access   |
|---|---|---------|----------|
| <b>HP ADC Configuration Registers</b>   |   |         |          |
| <a href="#">ADC_CTRL_REG</a>            | Configuration register for HP ADC Controller  | 0x0000  | R/W      |
| <a href="#">ADC_CTRL2_REG</a>           | Configuration register for HP ADC Controller. | 0x0004  | R/W      |
| <a href="#">ADC_FILTER_CTRL1_REG</a>    | Configuration register 1 for HP ADC filter.   | 0x0008  | R/W      |
| <a href="#">ADC_SAR1_PATT_TAB1_REG</a>  | Pattern table register 1 for HP ADC1.         | 0x0018  | R/W      |
| <a href="#">ADC_SAR1_PATT_TAB2_REG</a>  | Pattern table register 2 for HP ADC1.         | 0x001C  | R/W      |
| <a href="#">ADC_SAR1_PATT_TAB3_REG</a>  | Pattern table register 3 for HP ADC1.         | 0x0020  | R/W      |
| <a href="#">ADC_SAR1_PATT_TAB4_REG</a>  | Pattern table register 4 for HP ADC1.         | 0x0024  | R/W      |
| <a href="#">ADC_SAR2_PATT_TAB1_REG</a>  | Pattern table register 1 for HP ADC2.         | 0x0028  | R/W      |
| <a href="#">ADC_SAR2_PATT_TAB2_REG</a>  | Pattern table register 2 for HP ADC2.         | 0x002C  | R/W      |
| <a href="#">ADC_SAR2_PATT_TAB3_REG</a>  | Pattern table register 3 for HP ADC2.         | 0x0030  | R/W      |
| <a href="#">ADC_SAR2_PATT_TAB4_REG</a>  | Pattern table register 4 for HP ADC2.         | 0x0034  | R/W      |
| <a href="#">ADC_FILTER_CTRL0_REG</a>    | Configuration register 0 for HP ADC filter.   | 0x003C  | R/W      |
| <a href="#">ADC_THRES0_CTRL_REG</a>     | Filtered data threshold control register 0.   | 0x0044  | R/W      |
| <a href="#">ADC_THRES1_CTRL_REG</a>     | Filtered data threshold control register 1.   | 0x0048  | R/W      |
| <a href="#">ADC_THRES_CTRL_REG</a>      | Filter configuration register.                | 0x004C  | R/W      |
| <a href="#">ADC_INT_ENA_REG</a>         | Enable register of HP ADC interrupts.         | 0x0050  | R/W      |
| <a href="#">ADC_INT_RAW_REG</a>         | Raw register of HP ADC interrupts.            | 0x0054  | R/WTC/SS |
| <a href="#">ADC_INT_ST_REG</a>          | State register of HP ADC interrupts.          | 0x0058  | RO       |
| <a href="#">ADC_INT_CLR_REG</a>         | Clear register of HP ADC interrupts.          | 0x005C  | WT       |
| <a href="#">ADC_DMA_CONF_REG</a>        | GDMA configuration register for HP ADC.       | 0x0060  | R/W      |
| <b>HP ADC Version Control Registers</b> |   |         |          |
| <a href="#">ADC_CTRL_DATE_REG</a>       | HP ADC version control register               | 0x03FC  | RO       |

### 57.9.2 LP ADC Register Summary

The addresses in the table below are relative to LP ADC's base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

The abbreviations given in Column **Access** are explained in Section *Access Types for Registers*.

| Name                                   | Description                      | Address | Access |
|--|----------------------------------|---------|--------|
| <b>LP ADC Configuration Registers</b>  |                                  |         |        |
| <a href="#">LPADC_READER1_CTRL_REG</a> | LP ADC1 Reader control register. | 0x0000  | R/W    |

| Name                                     | Description   | Address | Access   |
|--|---|---------|----------|
| <a href="#">LPADC_MEAS1_CTRL2_REG</a>    | LP ADC1 configuration registers.                          | 0x000C  | varies   |
| <a href="#">LPADC_MEAS1_MUX_REG</a>      | LP or HP ADC controller selection register for SAR ADC1.  | 0x0010  | R/W      |
| <a href="#">LPADC_ATTEN1_REG</a>         | LP ADC1 attenuation registers.                            | 0x0014  | R/W      |
| <a href="#">LPADC_READER2_CTRL_REG</a>   | LP ADC2 Reader control register.                          | 0x0024  | R/W      |
| <a href="#">LPADC_MEAS2_CTRL2_REG</a>    | SAR ADC2 configuration registers.                         | 0x0030  | varies   |
| <a href="#">LPADC_MEAS2_MUX_REG</a>      | LP or HP controller selection register for SAR ADC2.      | 0x0034  | R/W      |
| <a href="#">LPADC_ATTEN2_REG</a>         | LP ADC2 attenuation registers.                            | 0x0038  | R/W      |
| <b>LP ADC Power Control Registers</b>    |   |         |          |
| <a href="#">LPADC_FORCE_WPD_SAR_REG</a>  | LP ADC Controllers power control registers.               | 0x003C  | R/W      |
| <b>LP ADC Interrupt Registers</b>        |   |         |          |
| <a href="#">LPADC_COCPU_INT_RAW_REG</a>  | Raw register of LP ADC interrupts.                        | 0x0048  | R/WTC/SS |
| <a href="#">LPADC_INT_ENA_REG</a>        | Enable register of LP ADC interrupts.                     | 0x004C  | R/WTC    |
| <a href="#">LPADC_INT_ST_REG</a>         | Status register of LP ADC interrupts.                     | 0x0050  | RO       |
| <a href="#">LPADC_INT_CLR_REG</a>        | Clear register of LP ADC interrupts.                      | 0x0054  | WT       |
| <a href="#">LPADC_INT_ENA_W1TS_REG</a>   | <a href="#">LPADC_INT_ENA_REG</a> configuration register. | 0x0058  | WT       |
| <a href="#">LPADC_INT_ENA_W1TC_REG</a>   | <a href="#">LPADC_INT_ENA_REG</a> configuration register. | 0x005C  | WT       |
| <b>LP ADC Wake-up Control Registers</b>  |   |         |          |
| <a href="#">LPADC_WAKEUP1_REG</a>        | LP ADC1 wake-up configuration registers.                  | 0x0060  | varies   |
| <a href="#">LPADC_WAKEUP2_REG</a>        | LP ADC2 wake-up configuration registers.                  | 0x0064  | varies   |
| <a href="#">LPADC_WAKEUP_SEL_REG</a>     | Wake-up source selection register.                        | 0x0068  | R/W      |
| <a href="#">LPADC_SAR1_HW_WAKEUP_REG</a> | LP ADC1 automatic monitoring configuration registers.     | 0x006C  | R/W      |
| <a href="#">LPADC_SAR2_HW_WAKEUP_REG</a> | LP ADC2 automatic monitoring configuration registers.     | 0x0070  | R/W      |

## 57.10 Registers

### 57.10.1 HP ADC Registers

The addresses in the following section are relative to the base address of HP ADC (written as ADC Controller) provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).



**Register 571. ADC\_CTRL\_REG (0x0000)**

|            |    |                    |    |                    |    |            |    |                       |    |                       |    |                   |    |                   |  |                 |   |                   |   |             |   |               |   |          |       |
|------------|----|--------------------|----|--------------------|----|------------|----|-----------------------|----|-----------------------|----|-------------------|----|-------------------|--|-----------------|---|-------------------|---|-------------|---|---------------|---|----------|-------|
| (reserved) |    | ADC_XPD_SAR2_FORCE |    | ADC_XPD_SAR1_FORCE |    | (reserved) |    | ADC_SAR2_PATT_P_CLEAR |    | ADC_SAR1_PATT_P_CLEAR |    | ADC_SAR2_PATT_LEN |    | ADC_SAR1_PATT_LEN |  | ADC_SAR_CLK_DIV |   | ADC_SAR_CLK_GATED |   | ADC_SAR_SEL |   | ADC_WORK_MODE |   | reserved |       |
| 31         | 30 | 29                 | 28 | 27                 | 26 | 25         | 24 | 23                    | 22 | 21                    | 18 |                   | 17 | 14                |  | 13              | 6 |                   | 5 | 4           | 3 | 2             | 1 | 0        | Reset |
| 0          | 0  | 0                  | 0  | 0                  | 0  | 0          | 0  | 0                     | 0  | 15                    |    | 15                |    | 4                 |  | 1               |   | 0                 | 0 | 0           | 0 |               |   |          |       |

**ADC\_WORK\_MODE** Configures dual HP ADC sampling.

- 0: Single HP ADC sampling
  - 1: Dual HP ADC simultaneous sampling
  - 2: Dual HP ADC alternative sampling.
- (R/W)

**ADC\_SAR\_SEL** Configures which HP ADC to use for single HP ADC sampling.

- 0: Use HP ADC1
  - 1: Use HP ADC2
- (R/W)

**ADC\_SAR\_CLK\_GATED** Enable HP ADC clock gate when HP ADC is in idle.

- 0: Disable
  - 1: Enable
- (R/W)

**ADC\_SAR\_CLK\_DIV** Configures HP ADC clock division. Division = configured value + 1. (R/W)

**ADC\_SAR1\_PATT\_LEN** Configures how many pattern table entries will be used for HP ADC1.

- 0: Use only cmd0
  - 1: Use cmd0 and cmd1
  - n: Use cmd0 to cmdn, the maximum n is 7
- (R/W)

**ADC\_SAR2\_PATT\_LEN** Configures how many pattern table entries will be used for HP ADC2.

- 0: Use only cmd0
  - 1: Use cmd0 and cmd1
  - n: Use cmd0 to cmdn, the maximum n is 7
- (R/W)

**ADC\_SAR1\_PATT\_P\_CLEAR** Clears the pointer of pattern table for HP ADC1 Controller.

- 0: No effect
  - 1: Clear
- (R/W)

**ADC\_SAR2\_PATT\_P\_CLEAR** Clears the pointer of pattern table for HP ADC2 Controller.

- 0: No effect
  - 1: Clear
- (R/W)

Continued on the next page...

**Register 57.1. ADC\_CTRL\_REG (0x0000)**

Continued from the previous page...

**ADC\_XPD\_SAR1\_FORCE** Keep HP ADC1 powered on forcefully.

0: No effect

1: Power on forcefully

(R/W)

**ADC\_XPD\_SAR2\_FORCE** Keep HP ADC2 powered on forcefully.

0: No effect

1: Power on forcefully

(R/W)

**Register 57.2. ADC\_CTRL2\_REG (0x0004)**

|                 |  |  |  |  |  |  |  |              |  |  |  |                  |    |  |  |            |    |  |  |                              |    |     |   |                  |  |   |  |                    |  |       |  |   |  |
|-----------------|--|--|--|--|--|--|--|--------------|--|--|--|------------------|----|--|--|------------|----|--|--|------------------------------|----|-----|---|------------------|--|---|--|--------------------|--|-------|--|---|--|
| (reserved)      |  |  |  |  |  |  |  | ADC_TIMER_EN |  |  |  | ADC_TIMER_TARGET |    |  |  | (reserved) |    |  |  | ADC_SAR2_INV<br>ADC_SAR1_INV |    |     |   | ADC_MAX_MEAS_NUM |  |   |  | ADC_MEAS_NUM_LIMIT |  |       |  |   |  |
| 31              |  |  |  |  |  |  |  | 25           |  |  |  | 24               | 23 |  |  |            | 12 |  |  |                              | 11 | 10  | 9 | 8                |  |   |  | 1                  |  |       |  | 0 |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0            |  |  |  | 10               |    |  |  | 0          |    |  |  | 0                            | 0  | 255 |   |                  |  | 0 |  |                    |  | Reset |  |   |  |

**ADC\_MEAS\_NUM\_LIMIT** Configures whether to enable the limitation of HP ADC's maximum conversion times.

0: Disable

1: Enable

(R/W)

**ADC\_MAX\_MEAS\_NUM** Configures the HP ADC's maximum conversion times. (R/W)**ADC\_SAR1\_INV** Configures whether to invert the data of HP ADC1.

0: Do not invert.

1: Invert the date.

(R/W)

**ADC\_SAR2\_INV** Configures whether to to invert the data of HP ADC2.

0: Do not invert.

1: Invert the date.

(R/W)

**ADC\_TIMER\_TARGET** Configures HP ADC timer target. (R/W)**ADC\_TIMER\_EN** Configures whether to enable HP ADC timer trigger.

0: Disable

1: Enable

(R/W)

### Register 57.3. ADC\_FILTER\_CTRL1\_REG (0x0008)

[illegible]

**ADC\_FILTER\_FACTOR1** Configures the filter coefficient  $k$  for HP ADC filter 1.

0:  $k=0$  (i.e., the filter is disabled)

1:  $k=2$ 

2:  $k=4$

3:  $k=8$ 

4:  $k=16$

5:  $k=32$

6:  $k=64$ 

(R/W)

**ADC\_FILTER\_FACTOR0** Configures the filter coefficient  $k$  for HP ADC filter 0 (same as above). (R/W)

### Register 57.4. ADC\_SAR1\_PATT\_TAB1\_REG (0x0018)

Diagram of the SAR1\_PATT\_TAB1 register. The register is 32 bits wide, divided into a 9-bit reserved field (bits 31-24) and a 23-bit data field (bits 23-0). The data field contains the value 0x0000. The label 'SAR1\_PATT\_TAB1' is placed above the data field.

**ADC\_SAR1\_PATT\_TAB1** Configures entries 0 ~ 3 for HP ADC FSM1. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

### Register 57.5. ADC\_SAR1\_PATT\_TAB2\_REG (0x001C)

|                 |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
|-----------------|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|
| (reserved)      |  |  |  |  |  |  |  | ADC_SAR1_PATT_TAB2 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |
| 31              |  |  |  |  |  |  |  | 24                 |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000             |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |

**ADC\_SAR1\_PATT\_TAB2** Configures entries 4 ~ 7 for HP ADC FSM1. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

**Register 57.6. ADC\_SAR1\_PATT\_TAB3\_REG (0x0020)**

|            |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |        |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
|------------|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--------|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|
| (reserved) |  |  |  |  |  |  |  | ADC_SAR1_PATT_TAB3 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |        |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 31         |  |  |  |  |  |  |  | 24                 |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |        |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |
| 0          |  |  |  |  |  |  |  | 0                  |  |  |  |  |  |  |  | 0  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  | 0x0000 |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |

**ADC\_SAR1\_PATT\_TAB3** Configures entries 8 ~ 11 for HP ADC FSM1. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

**Register 57.7. ADC\_SAR1\_PATT\_TAB4\_REG (0x0024)**

|                 |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
|-----------------|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|
| (reserved)      |  |  |  |  |  |  |  | ADC_SAR1_PATT_TAB4 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
| 31              |  |  |  |  |  |  |  | 24                 |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000             |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |

**ADC\_SAR1\_PATT\_TAB4** Configures entries 12 ~ 15 for HP ADC FSM1. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

**Register 57.8. ADC\_SAR2\_PATT\_TAB1\_REG (0x0028)**

|                 |  |  |  |  |  |  |  |                    |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
|-----------------|--|--|--|--|--|--|--|--------------------|--|--|--|--|--|--|--|----|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|---|
| (reserved)      |  |  |  |  |  |  |  | ADC_SAR2_PATT_TAB1 |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |   |
| 31              |  |  |  |  |  |  |  | 24                 |  |  |  |  |  |  |  | 23 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  | 0 |
| 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  | 0x0000             |  |  |  |  |  |  |  |    |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |   |

**ADC\_SAR2\_PATT\_TAB1** Configures entries 0 ~ 3 for HP ADC FSM2. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

(reserved)

ADC\_SAR2\_PATT\_TAB2

**ADC\_SAR2\_PATT\_TAB2** Configures entries 4 ~ 7 for HP ADC FSM2. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

(reserved)

ADC\_SAR2\_PAT\_TAB3

**ADC\_SAR2\_PATT\_TAB3** Configures entries 8 ~ 11 for HP ADC FSM2. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

(reserved)

ADC\_SAR2\_PATT\_TAB4

**ADC\_SAR2\_PATT\_TAB4** Configures entries 12 ~ 15 for HP ADC FSM2. Each entry is 6-bit wide. See Section [57.5.6 HP ADC Pattern Table](#). (R/W)

**Register 57.12. ADC\_FILTER\_CTRL0\_REG (0x003C)**

|                  |    |   |   |   |   |   |   |            |    |    |  |  |  |  |  |                     |    |    |  |  |  |  |  |                     |    |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
|------------------|----|---|---|---|---|---|---|------------|----|----|--|--|--|--|--|---------------------|----|----|--|--|--|--|--|---------------------|----|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|--|
| ADC_FILTER_RESET |    |   |   |   |   |   |   | (reserved) |    |    |  |  |  |  |  | ADC_FILTER_CHANNEL0 |    |    |  |  |  |  |  | ADC_FILTER_CHANNEL1 |    |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 31               | 30 |   |   |   |   |   |   | 24         | 23 | 19 |  |  |  |  |  |                     | 18 | 14 |  |  |  |  |  |                     | 13 | 0 |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |
| 0                | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0xd        |    |    |  |  |  |  |  | 0xd                 |    |    |  |  |  |  |  | 0                   | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |  |

Reset

**ADC\_FILTER\_CHANNEL0** Configures the ADC channel for filter 0. Value 0 ~ 7 corresponds to channel 0 ~ 7 in HP ADC1, value 10 ~ 15 corresponds to channel 0 ~ 5 in HP ADC2. (R/W)

**ADC\_FILTER\_CHANNEL1** Configure the ADC channel for filter 1. Same as above. (R/W)

**ADC\_FILTER\_RESET** Configures whether to reset the filter.

0: No effect

1: Reset

(R/W)

**Register 57.13. ADC\_THRES0\_CTRL\_REG (0x0044)**

|            |    |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  |        |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    |                    |   |   |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
|------------|----|----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--------|-----------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|----|--------------------|---|---|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|
| (reserved) |    | ADC_THRES0_LOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |        | ADC_THRES0_HIGH |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | ADC_THRES0_CHANNEL |   |   |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
| 31         | 30 |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 18     | 17              |  |  |  |  |  |  |  |  |  |  |  |  |  |  |    | 5                  | 4 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |
| 0          | 0  |                |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x1fff |                 |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 13 |                    |   |   |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |

Reset

**ADC\_THRES0\_CHANNEL** Configures the ADC channel for threshold monitor 0. Value 0 ~ 7 corresponds to channel 0 ~ 7 in HP ADC1, value 10 ~ 15 corresponds to channel 0 ~ 5 in HP ADC2. (R/W)

**ADC\_THRES0\_HIGH** Configures the high threshold for HP ADC threshold monitor 0. (R/W)

**ADC\_THRES0\_LOW** Configures the low threshold for HP ADC threshold monitor 0. (R/W)

Register 57.14. ADC\_THRES1\_CTRL\_REG (0x0048)

|            |    |                |  |  |  |  |  |  |  |  |        |                 |    |  |  |  |  |  |  |  |    |                    |  |   |   |  |  |   |       |
|------------|----|----------------|--|--|--|--|--|--|--|--|--------|-----------------|----|--|--|--|--|--|--|--|----|--------------------|--|---|---|--|--|---|-------|
| (reserved) |    | ADC_THRES1_LOW |  |  |  |  |  |  |  |  |        | ADC_THRES1_HIGH |    |  |  |  |  |  |  |  |    | ADC_THRES1_CHANNEL |  |   |   |  |  |   |       |
| 31         | 30 |                |  |  |  |  |  |  |  |  |        | 18              | 17 |  |  |  |  |  |  |  |    |                    |  | 5 | 4 |  |  | 0 |       |
| 0          | 0  |                |  |  |  |  |  |  |  |  | 0x1fff |                 |    |  |  |  |  |  |  |  | 13 |                    |  |   |   |  |  |   | Reset |

**ADC\_THRES1\_CHANNEL** Configures the ADC channel for threshold monitor 1. Value 0 ~ 7 corresponds to channel 0 ~ 7 in HP ADC1, value 10 ~ 15 corresponds to channel 0 ~ 5 in HP ADC2. (R/W)

**ADC\_THRES1\_HIGH** Configures the high threshold for HP ADC threshold monitor 1. (R/W)

**ADC\_THRES1\_LOW** Configures the low threshold for HP ADC threshold monitor 1. (R/W)

Register 57.15. ADC\_THRES\_CTRL\_REG (0x004C)

|               |    |    |   |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|---------------|----|----|---|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC_THRES0_EN |    |    |   |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ADC_THRES1_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | ADC_THRES_ALL_EN |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31            | 30 | 29 |   | 28 | 27 | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |               | 0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                  |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0             | 0  | 0  | 0 | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0             | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ADC\_THRES\_ALL\_EN** Configures whether to enable the threshold monitoring for all configured channels.  
 0: Disable  
 1: Enable  
 (R/W)

**ADC\_THRES1\_EN** Configures whether to enable threshold monitor 1.  
 0: Disable  
 1: Enable  
 (R/W)

**ADC\_THRES0\_EN** Configures whether to enable threshold monitor 0.  
 0: Disable  
 1: Enable  
 (R/W)

**Register 57.16. ADC\_INT\_ENA\_REG (0x0050)**

|  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| ADC_SAR1_DONE_INT_ENA<br>ADC_SAR2_DONE_INT_ENA<br>ADC_THRES0_HIGH_INT_ENA<br>ADC_THRES1_HIGH_INT_ENA<br>ADC_THRES0_LOW_INT_ENA<br>ADC_THRES1_LOW_INT_ENA<br><br>(reserved) |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0 |   |       |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**ADC\_THRES1\_LOW\_INT\_ENA** Enable bit of [ADC\\_THRES1\\_LOW\\_INT](#). (R/W)

**ADC\_THRES0\_LOW\_INT\_ENA** Enable bit of [ADC\\_THRES0\\_LOW\\_INT](#). (R/W)

**ADC\_THRES1\_HIGH\_INT\_ENA** Enable bit of [ADC\\_THRES1\\_HIGH\\_INT](#). (R/W)

**ADC\_THRES0\_HIGH\_INT\_ENA** Enable bit of [ADC\\_THRES0\\_HIGH\\_INT](#). (R/W)

**ADC\_SAR2\_DONE\_INT\_ENA** Enable bit of [ADC\\_SAR2\\_DONE\\_INT](#). (R/W)

**ADC\_SAR1\_DONE\_INT\_ENA** Enable bit of [ADC\\_SAR1\\_DONE\\_INT](#). (R/W)

**Register 57.17. ADC\_INT\_RAW\_REG (0x0054)**

|  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|
| <div>ADC_SAR1_DONE_INT_RAW<br/>ADC_SAR2_DONE_INT_RAW<br/>ADC_THRES0_HIGH_INT_RAW<br/>ADC_THRES1_HIGH_INT_RAW<br/>ADC_THRES0_LOW_INT_RAW<br/>ADC_THRES1_LOW_INT_RAW</div> |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0          |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |

**ADC\_THRES1\_LOW\_INT\_RAW** Raw bit of [ADC\\_THRES1\\_LOW\\_INT](#). (R/WTC/SS)

**ADC\_THRES0\_LOW\_INT\_RAW** Raw bit of [ADC\\_THRES0\\_LOW\\_INT](#). (R/WTC/SS)

**ADC\_THRES1\_HIGH\_INT\_RAW** Raw bit of [ADC\\_THRES1\\_HIGH\\_INT](#). (R/WTC/SS)

**ADC\_THRES0\_HIGH\_INT\_RAW** Raw bit of [ADC\\_THRES0\\_HIGH\\_INT](#). (R/WTC/SS)

**ADC\_SAR2\_DONE\_INT\_RAW** Raw bit of [ADC\\_SAR2\\_DONE\\_INT](#). (R/WTC/SS)

**ADC\_SAR1\_DONE\_INT\_RAW** Raw bit of [ADC\\_SAR1\\_DONE\\_INT](#). (R/WTC/SS)



## Register 57.18. ADC\_INT\_ST\_REG (0x0058)

|  |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|--|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| <div>ADC_APB_SARADC1_DONE_INT_ST<br/>ADC_APB_SARADC2_DONE_INT_ST<br/>ADC_THRES0_HIGH_INT_ST<br/>ADC_THRES1_HIGH_INT_ST<br/>ADC_THRES0_LOW_INT_ST<br/>ADC_THRES1_LOW_INT_ST</div> |    |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31   | 30 | 29 | 28 | 27 | 26 | 25 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0          |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ADC\_THRES1\_LOW\_INT\_ST** Status bit of [ADC\\_THRES1\\_LOW\\_INT](#). (RO)

**ADC\_THRES0\_LOW\_INT\_ST** Status bit of [ADC\\_THRES0\\_LOW\\_INT](#). (RO)

**ADC\_THRES1\_HIGH\_INT\_ST** Status bit of [ADC\\_THRES1\\_HIGH\\_INT](#). (RO)

**ADC\_THRES0\_HIGH\_INT\_ST** Status bit of [ADC\\_THRES0\\_HIGH\\_INT](#). (RO)

**ADC\_APB\_SARADC2\_DONE\_INT\_ST** Status bit of [ADC\\_SAR2\\_DONE\\_INT](#). (RO)

**ADC\_APB\_SARADC1\_DONE\_INT\_ST** Status bit of [ADC\\_SAR1\\_DONE\\_INT](#). (RO)

## Register 57.19. ADC\_INT\_CLR\_REG (0x005C)

|  |    |    |    |    |    |            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |       |
|--|----|----|----|----|----|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-------|
| <div> <div>ADC_APB_SARADC1_DONE_INT_CLR</div> <div>ADC_APB_SARADC2_DONE_INT_CLR</div> <div>ADC_THRES0_HIGH_INT_CLR</div> <div>ADC_THRES1_HIGH_INT_CLR</div> <div>ADC_THRES0_LOW_INT_CLR</div> <div>ADC_THRES1_LOW_INT_CLR</div> </div> |    |    |    |    |    | (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 31   | 30 | 29 | 28 | 27 | 26 | 25         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 0     |
| 0  | 0  | 0  | 0  | 0  | 0  | 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Reset |

**ADC\_THRES1\_LOW\_INT\_CLR** Clear bit of [ADC\\_THRES1\\_LOW\\_INT](#). (WT)

**ADC\_THRES0\_LOW\_INT\_CLR** Clear bit of [ADC\\_THRES0\\_LOW\\_INT](#). (WT)

**ADC\_THRES1\_HIGH\_INT\_CLR** Clear bit of [ADC\\_THRES1\\_HIGH\\_INT](#). (WT)

**ADC\_THRES0\_HIGH\_INT\_CLR** Clear bit of [ADC\\_THRES0\\_HIGH\\_INT](#). (WT)

**ADC\_APB\_SARADC2\_DONE\_INT\_CLR** Clear bit of [ADC\\_SAR2\\_DONE\\_INT](#). (WT)

**ADC\_APB\_SARADC1\_DONE\_INT\_CLR** Clear bit of [ADC\\_SAR1\\_DONE\\_INT](#). (WT)

### Register 57.20. ADC\_DMA\_CONF\_REG (0x0060)

|    |    |    |   |   |   |   |   |   |   |   |   |   |    |    |   |   |     |   |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |       |
|----|----|----|---|---|---|---|---|---|---|---|---|---|----|----|---|---|-----|---|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|-------|
| 31 | 30 | 29 |   |   |   |   |   |   |   |   |   |   | 16 | 15 |   |   |     |   |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |       |
| 0  | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0  | 0 | 0 | 255 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  | Reset |

**ADC\_APB\_ADC\_EOF\_NUM** Configures the number of samples. When the sampling reaches the configured number, the EOF flag bit sent to GDMA will be pulled high. (R/W)

**ADC\_APB\_ADC\_RESET\_FSM** Configures whether to reset the status of HP ADC controller.

0: No effect

1: Reset

(R/W)

**ADC\_APB\_ADC\_TRANS** Configures whether to let HP ADC controller use GDMA.

0: No effect

1: HP ADC controller uses DMA

(R/W)

### Register 57.21. ADC\_CTRL\_DATA\_REG (0x03FC)

Diagram illustrating the structure of the `ADC_CTRL` register:

- Bit 31: (reserved)
- Bits 30-0: `ADC_CTRL_DATE`
- Bit 0: `Reset`

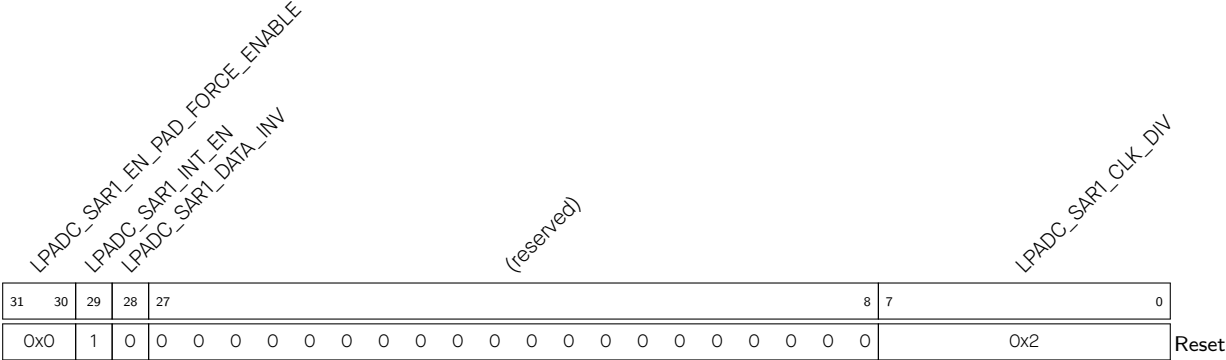
**ADC\_CTRL\_DATE** HP ADC version control register. (RO)

## 57.10.2 LP ADC Registers

The addresses in the following section are relative to LP ADC's base address provided in Table 6.3-2 in Chapter 6 *System and Memory*.

For how to program reserved fields, please refer to Section [Programming Reserved Register Field](#).

Register 57.22. LPADC\_READER1\_CTRL\_REG (0x0000)



**LPADC\_SAR1\_CLK\_DIV** Configures the division of LP ADC1’s clock LPADC\_SARCLK. (R/W)

**LPADC\_SAR1\_DATA\_INV** Configures whether to to invert the data of LP ADC1.

0: Do not invert the data.

1: Invert the data.

(R/W)

**LPADC\_SAR1\_INT\_EN** Enables LP ADC1 to send out interrupt. (R/W)

**LPADC\_SAR1\_EN\_PAD\_FORCE\_ENABLE** Configures whether to use software to force enable [LPADC\\_SAR1\\_EN\\_PAD](#).

2: Force off

3: Force enable

Other values: Hardware control (enabled during sampling)

(R/W)

Register 57.23. LPADC\_MEAS1\_CTRL2\_REG (0x000C)

|                         |     |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |    |    |    |                         |    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |       |   |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |
|-------------------------|-----|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|----|----|----|-------------------------|----|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|-------|---|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|
| LPADC_SAR1_EN_PAD_FORCE |     |  |  |  |  |  |  |  |  |  | LPADC_SAR1_EN_PAD |  |  |  |  |  |  |  |    |    |    | LPADC_MEAS1_START_FORCE |    |  |  |  |  |  |  |  |  |  | LPADC_MEAS1_START_SAR |  |  |  |  |  |  |       |   |  |  | LPADC_MEAS1_DONE_SAR |  |  |  |  |  |  |  |  |  |  | LPADC_MEAS1_DATA_SAR |  |  |  |  |  |  |  |  |  |  |
| 31                      | 30  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  | 19 | 18 | 17 | 16                      | 15 |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |       | 0 |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |
| 0                       | 0x0 |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  | 0  | 0  | 0  | 0x00                    |    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  | Reset |   |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |

**LPADC\_MEAS1\_DATA\_SAR** Stores LP ADC1's conversion data in one-shot sampling mode. (RO)

**LPADC\_MEAS1\_DONE\_SAR** Indicates whether LP ADC1 conversion is done. (RO)

**LPADC\_MEAS1\_START\_SAR** Configures whether to start LP ADC1 by software.

0: No effect

1: Start LP ADC1 by software

Valid only when [LPADC\\_MEAS1\\_START\\_FORCE](#) = 1.

(R/W)

**LPADC\_MEAS1\_START\_FORCE** Configures whether to use software to enable LP ADC1 sampling.

0: Select FSM to start LP ADC1 sampling

1: Select software to start LP ADC1 sampling

(R/W)

**LPADC\_SAR1\_EN\_PAD** Configures the sampling channel for LP ADC1. Value 0 ~ 7 corresponds to channel 0 ~ 7. (R/W)

**LPADC\_SAR1\_EN\_PAD\_FORCE** Configures whether to use software to select the sampling channel for LP ADC1.

0: No effect

1: Use software to control

(R/W)

LPADC\_SAR1\_DIG\_FORCE

(reserved)

LPADC\_SAR1\_ATTEN

Register 57.26. LPADC\_READER2\_CTRL\_REG (0x0024)

|                   |    |    |     |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     |                                |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |
|-------------------|----|----|-----|----|----|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----|--------------------------------|--|--|--|--|--|--|--|---------------------|--|--|--|--|--|--|--|
| (reserved)        |    |    |     |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     | (reserved)                     |  |  |  |  |  |  |  | LPADC_SAR2_CLK_DIV  |  |  |  |  |  |  |  |
| LPADC_SAR2_INT_EN |    |    |     |    |    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |     | LPADC_SAR2_EN_PAD_FORCE_ENABLE |  |  |  |  |  |  |  | LPADC_SAR2_DATA_INV |  |  |  |  |  |  |  |
| 31                | 30 | 29 | 28  | 27 | 26 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 8 | 7   |                                |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |
| 0                 | 1  | 0  | 0x0 | 0  | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x2 | Reset                          |  |  |  |  |  |  |  |                     |  |  |  |  |  |  |  |

**LPADC\_SAR2\_CLK\_DIV** Configures the division of LP ADC2’s clock LPADC\_SARCLK. (R/W)

**LPADC\_SAR2\_EN\_PAD\_FORCE\_ENABLE** Configures whether to use software to force enable [LPADC\\_SAR2\\_EN\\_PAD](#).  
2: Force off  
3: Force enable  
Other values: Hardware control (enabled during sampling)  
(R/W)

**LPADC\_SAR2\_DATA\_INV** onfigures whether to to invert the data of LP ADC2.  
0: Do not invert the data.  
1: Invert the data.  
(R/W)

**LPADC\_SAR2\_INT\_EN** Enable LP ADC2 to send out interrupt. (R/W)

Register 57.27. LPADC\_MEAS2\_CTRL2\_REG (0x0030)

|                         |     |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  |    |    |    |                         |    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |       |   |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |
|-------------------------|-----|--|--|--|--|--|--|--|--|--|-------------------|--|--|--|--|--|--|--|----|----|----|-------------------------|----|--|--|--|--|--|--|--|--|--|-----------------------|--|--|--|--|--|--|-------|---|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|----------------------|--|--|--|--|--|--|--|--|--|--|
| LPADC_SAR2_EN_PAD_FORCE |     |  |  |  |  |  |  |  |  |  | LPADC_SAR2_EN_PAD |  |  |  |  |  |  |  |    |    |    | LPADC_MEAS2_START_FORCE |    |  |  |  |  |  |  |  |  |  | LPADC_MEAS2_START_SAR |  |  |  |  |  |  |       |   |  |  | LPADC_MEAS2_DONE_SAR |  |  |  |  |  |  |  |  |  |  | LPADC_MEAS2_DATA_SAR |  |  |  |  |  |  |  |  |  |  |
| 31                      | 30  |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  | 19 | 18 | 17 | 16                      | 15 |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  |       | 0 |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |
| 0                       | 0x0 |  |  |  |  |  |  |  |  |  |                   |  |  |  |  |  |  |  | 0  | 0  | 0  | 0x00                    |    |  |  |  |  |  |  |  |  |  |                       |  |  |  |  |  |  | Reset |   |  |  |                      |  |  |  |  |  |  |  |  |  |  |                      |  |  |  |  |  |  |  |  |  |  |

**LPADC\_MEAS2\_DATA\_SAR** Stores LP ADC2's conversion data in one-shot sampling mode. (RO)

**LPADC\_MEAS2\_DONE\_SAR** Indicates whether LP ADC2 conversion is done. (RO)

**LPADC\_MEAS2\_START\_SAR** Configures whether to start LP ADC2 by software.

0: No effect

1: Start LP ADC2 by software

Valid only when [LPADC\\_MEAS2\\_START\\_FORCE](#) = 1.

(R/W)

**LPADC\_MEAS2\_START\_FORCE** Configures whether to use software to enable LP ADC2 sampling.

0: Select FSM to start LP ADC2 sampling

1: Select software to start LP ADC2 sampling

(R/W)

**LPADC\_SAR2\_EN\_PAD** Configures the sampling channel for LP ADC2. Value 2 ~ 7 corresponds to channel 0 ~ 5. (R/W)

**LPADC\_SAR2\_EN\_PAD\_FORCE** Configures whether to use software to select the sampling channel for LP ADC1.

0: No effect

1: Use software to control

(R/W)

LPADC\_SAR2\_LP\_FORCE

(reserved)

Reset

0: Do not disable HP ADC2 Controller.

(R/W)

LPADC\_SAR2\_ATTEN

Reset

0: 0 dB

2: 6 dB

(R/W)



### Register 57.30. LPADC\_FORCE\_WPD\_SAR\_REG (0x003C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |     |                      |       |  |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|-----|----------------------|-------|--|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_FORCE_XPD_SAR2 |     | LPADC_FORCE_XPD_SAR1 |       |  |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 4 | 3                    | 2   | 1                    | 0     |  |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0x0 | 0x0                  | Reset |  |

**LPADC\_FORCE\_XPD\_SAR1** Configures the power control for LP ADC1.

3: Software control, force on.

2: Software control, force off.

1/0: Hardware control.

(R/W)

**LPADC\_FORCE\_XPD\_SAR2** Configures the power control for LP ADC2.

3: Software control, force on.

2: Software control, force off.

1/0: Hardware control.

(R/W)

Register 57.31. LPADC\_COCPU\_INT\_RAW\_REG (0x0048)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_WAKE_INT_RAW  |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_WAKE_INT_RAW  |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_ERROR_INT_RAW |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_ERROR_INT_RAW |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_INT_RAW       |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_INT_RAW       |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5 | 4 | 3                                 | 2 | 1 | 0     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | Reset |

LPADC\_COCPU\_SARADC1\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC1\_DONE\_INT. (R/WTC/SS)

LPADC\_COCPU\_SARADC2\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC2\_DONE\_INT. (R/WTC/SS)

LPADC\_COCPU\_SARADC1\_ERROR\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC1\_ERROR\_INT. (R/WTC/SS)

LPADC\_COCPU\_SARADC2\_ERROR\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC2\_ERROR\_INT. (R/WTC/SS)

LPADC\_COCPU\_SARADC1\_WAKE\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC1\_WAKE\_INT. (R/WTC/SS)

LPADC\_COCPU\_SARADC2\_WAKE\_INT\_RAW Raw bit of LPADC\_COCPU\_SARADC2\_WAKE\_INT. (R/WTC/SS)

Register 57.32. LPADC\_INT\_ENA\_REG (0x004C)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                                   |   |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|-----------------------------------|---|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_WAKE_INT_ENA  |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_WAKE_INT_ENA  |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_ERROR_INT_ENA |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_ERROR_INT_ENA |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_INT_ENA       |   |   |       |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC1_INT_ENA       |   |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6                                 | 5 | 4 | 3     |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                                 | 0 | 0 | 0     |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 2                                 | 1 | 0 | Reset |

- LPADC\_COCPU\_SARADC1\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC1\_DONE\_INT. (R/WTC)
- LPADC\_COCPU\_SARADC2\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC2\_DONE\_INT. (R/WTC)
- LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC1\_ERROR\_INT. (R/WTC)
- LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC2\_ERROR\_INT. (R/WTC)
- LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC1\_WAKE\_INT. (R/WTC)
- LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ENA Enable bit of LPADC\_COCPU\_SARADC2\_WAKE\_INT. (R/WTC)

### Register 57.33. LPADC\_INT\_ST\_REG (0x0050)

Diagram of the LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ST register. The register is 32 bits wide. Bits 31-6 are reserved. Bits 5-0 are status bits for LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ST, LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ST, LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ST, LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ST, LPADC\_COCPU\_SARADC1\_INT\_ST, and LPADC\_COCPU\_SARADC2\_INT\_ST. The register is reset to 0.

**LPADC\_COCPU\_SARADC1\_INT\_ST** Status bit of [LPADC\\_COCPU\\_SARADC1\\_DONE\\_INT](#). (RO)

**LPADC\_COCPU\_SARADC2\_INT\_ST** Status bit of [LPADC\\_COCPU\\_SARADC2\\_DONE\\_INT](#). (RO)

LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ST Status bit of LPADC\_COCPU\_SARADC1\_ERROR\_INT.  
(RO)

LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ST Status bit of LPADC\_COCPU\_SARADC2\_ERROR\_INT.  
(RO)

LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ST Status bit of LPADC\_COCPU\_SARADC1\_WAKE\_INT. (RO)

LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ST Status bit of LPADC\_COCPU\_SARADC2\_WAKE\_INT.  
(RO)

Register 57.34. LPADC\_INT\_CLR\_REG (0x0054)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |  |   |   |   |   |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
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| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_COCPU_SARADC2_WAKE_INT_CLR<br>LPADC_COCPU_SARADC1_WAKE_INT_CLR<br>LPADC_COCPU_SARADC2_ERROR_INT_CLR<br>LPADC_COCPU_SARADC1_ERROR_INT_CLR<br>LPADC_COCPU_SARADC2_INT_CLR<br>LPADC_COCPU_SARADC1_INT_CLR |   |   |   |   |   |       |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 6 | 5  | 4 | 3 | 2 | 1 | 0 | Reset |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0  | 0 | 0 | 0 | 0 | 0 |       | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

- LPADC\_COCPU\_SARADC1\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC1\_DONE\_INT. (WT)
- LPADC\_COCPU\_SARADC2\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC2\_DONE\_INT. (WT)
- LPADC\_COCPU\_SARADC1\_ERROR\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC1\_ERROR\_INT. (WT)
- LPADC\_COCPU\_SARADC2\_ERROR\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC2\_ERROR\_INT. (WT)
- LPADC\_COCPU\_SARADC1\_WAKE\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC1\_WAKE\_INT. (WT)
- LPADC\_COCPU\_SARADC2\_WAKE\_INT\_CLR Clear bit of LPADC\_COCPU\_SARADC2\_WAKE\_INT. (WT)

### Register 57.35. LPADC\_INT\_ENA\_W1TS\_REG (0x0058)

[illegible]

LPADC\_COCPU\_SARADC1\_INT\_ENA\_W1TS Write 1 to enable LPADC\_COCPU\_SARADC1\_INT\_ENA.  
(WT)

LPADC\_COCPU\_SARADC2\_INT\_ENA\_W1TS Write 1 to enable LPADC\_COCPU\_SARADC2\_INT\_ENA.  
(WT)

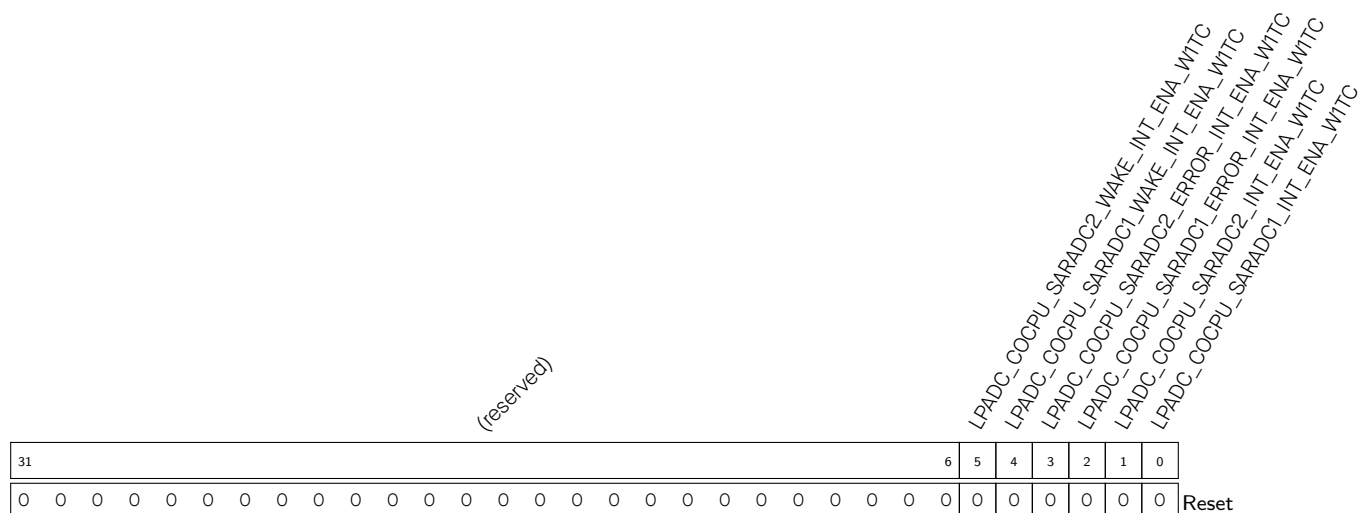
LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ENA\_W1TS Write 1 to enable  
LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ENA\_W1TS Write 1 to enable  
LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ENA\_W1TS Write 1 to enable  
LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ENA\_W1TS Write 1 to enable  
LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ENA. (WT)

### Register 57.36. LPADC\_INT\_ENA\_W1TC\_REG (0x005C)



LPADC\_COCPU\_SARADC1\_INT\_ENA\_W1TC Write 1 to clear LPADC\_COCPU\_SARADC1\_INT\_ENA.  
(WT)

LPADC\_COCPU\_SARADC2\_INT\_ENA\_W1TC Write 1 to clear LPADC\_COCPU\_SARADC2\_INT\_ENA.  
(WT)

LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ENA\_W1TC Write 1 to clear  
LPADC\_COCPU\_SARADC1\_ERROR\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ENA\_W1TC Write 1 to clear  
LPADC\_COCPU\_SARADC2\_ERROR\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ENA\_W1TC Write 1 to clear  
LPADC\_COCPU\_SARADC1\_WAKE\_INT\_ENA. (WT)

LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ENA\_W1TC Write 1 to clear  
LPADC\_COCPU\_SARADC2\_WAKE\_INT\_ENA. (WT)

Register 57.37. LPADC\_WAKEUP1\_REG (0x0060)

|                                 |    |    |    |    |    |                           |  |  |  |  |  |                          |    |    |    |   |       |
|---------------------------------|----|----|----|----|----|---------------------------|--|--|--|--|--|--------------------------|----|----|----|---|-------|
| LPADC_SAR1_WAKEUP_MODE          |    |    |    |    |    | LPADC_SAR1_WAKEUP_TH_HIGH |  |  |  |  |  | LPADC_SAR1_WAKEUP_TH_LOW |    |    |    |   |       |
| LPADC_SAR1_WAKEUP_EN            |    |    |    |    |    | (reserved)                |  |  |  |  |  | (reserved)               |    |    |    |   |       |
| LPADC_SAR1_WAKEUP_OVER_UPPER_TH |    |    |    |    |    |                           |  |  |  |  |  |                          |    |    |    |   |       |
| 31                              | 30 | 29 | 28 | 26 | 25 |                           |  |  |  |  |  | 14                       | 13 | 12 | 11 |   |       |
| 0                               | 0  | 0  | 0  | 0  | 0  | 0xfff                     |  |  |  |  |  | 0                        | 0  |    |    | 0 | Reset |

**LPADC\_SAR1\_WAKEUP\_TH\_LOW** Configures the low threshold for LP ADC1's wake-up function.  
(R/W)

**LPADC\_SAR1\_WAKEUP\_TH\_HIGH** Configures the high threshold for LP ADC1's wake-up function.  
(R/W)

**LPADC\_SAR1\_WAKEUP\_OVER\_UPPER\_TH** Indicates whether the wake-up event is triggered by the conversion data exceeding high threshold. (RO)

**LPADC\_SAR1\_WAKEUP\_EN** Configures whether to enable wake-up function for LP ADC1.  
0: Disable  
1: Enable  
(R/W)

**LPADC\_SAR1\_WAKEUP\_MODE** Selects the wake-up mode for automatic monitoring. Valid only when [LPADC\\_SAR1\\_WAKEUP\\_EN](#)=1.  
0: Absolute value mode  
1: Change value mode  
(R/W)



Register 57.38. LPADC\_WAKEUP2\_REG (0x0064)

|                        |    |    |    |    |   |   |       |    |  |  |  |  |  |  |  |  |                           |    |    |    |  |  |  |  |  |  |  |  |       |   |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|------------------------|----|----|----|----|---|---|-------|----|--|--|--|--|--|--|--|--|---------------------------|----|----|----|--|--|--|--|--|--|--|--|-------|---|--|--|--|--------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| LPADC_SAR2_WAKEUP_MODE |    |    |    |    |   |   |       |    |  |  |  |  |  |  |  |  | LPADC_SAR2_WAKEUP_TH_HIGH |    |    |    |  |  |  |  |  |  |  |  |       |   |  |  |  | LPADC_SAR2_WAKEUP_TH_LOW |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| LPADC_SAR2_WAKEUP_EN   |    |    |    |    |   |   |       |    |  |  |  |  |  |  |  |  | (reserved)                |    |    |    |  |  |  |  |  |  |  |  |       |   |  |  |  | (reserved)               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| (reserved)             |    |    |    |    |   |   |       |    |  |  |  |  |  |  |  |  |                           |    |    |    |  |  |  |  |  |  |  |  |       |   |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                     | 30 | 29 | 28 | 26 |   |   | 25    | 14 |  |  |  |  |  |  |  |  |                           | 13 | 12 | 11 |  |  |  |  |  |  |  |  |       | 0 |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0                      | 0  | 0  | 0  | 0  | 0 | 0 | 0xfff |    |  |  |  |  |  |  |  |  | 0                         | 0  | 0  |    |  |  |  |  |  |  |  |  | Reset |   |  |  |  |                          |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LPADC\_SAR2\_WAKEUP\_TH\_LOW** Configures the low threshold for LP ADC2's wake-up function.  
(R/W)

**LPADC\_SAR2\_WAKEUP\_TH\_HIGH** Configures the high threshold for LP ADC2's wake-up function.  
(R/W)

**LPADC\_SAR2\_WAKEUP\_OVER\_UPPER\_TH** Indicates whether the wake-up event is triggered by the conversion data exceeding high threshold. (RO)

**LPADC\_SAR2\_WAKEUP\_EN** Configures whether to enable wake-up function for LP ADC2.  
0: Disable  
1: Enable  
(R/W)

**LPADC\_SAR2\_WAKEUP\_MODE** Selects the wake-up mode for automatic monitoring. Valid only when [LPADC\\_SAR2\\_WAKEUP\\_EN](#)=1.  
0: Absolute value mode  
1: Change value mode  
(R/W)

Register 57.39. LPADC\_WAKEUP\_SEL\_REG (0x0068)

|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |
|------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|----------------------|---|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | LPADC_SAR_WAKEUP_SEL |   |
| 31         |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | 1                    | 0 |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0                    | 0 |
|            |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |                      |   |

**LPADC\_SAR\_WAKEUP\_SEL** Enables the wake-up function for LP ADC1 or LP ADC2. 0: LP ADC1.  
1: LP ADC2.  
(R/W)

### Register 57.40. LPADC\_SAR1\_HW\_WAKEUP\_REG (0x006C)

|                               |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                           |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |                         |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|-------------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------------------------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|-------|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|---|--|--|--|--|--|--|--|--|--|--|--|--|--|--|--|
| (reserved)                    |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LPADC_ADC1_HW_READ_RATE_I |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | LPADC_ADC1_HW_READ_EN_I |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31                            |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 17                        |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 16                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1     |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0x64                      |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0                       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | Reset |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |   |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

**LPADC\_ADC1\_HW\_READ\_EN\_I** Configures whether to enable automatic monitoring for LP ADC1.

0: Disable

1: Enable

(R/W)

**LPADC\_ADC1\_HW\_READ\_RATE\_I** Configures the sampling rate for hardware-triggered automatic monitoring for LP ADC1. The sampling period = configured value × LP ADC1's working clock cycle. (R/W)

### Register 57.41. LPADC\_SAR2\_HW\_WAKEUP\_REG (0x0070)

|                           |    |    |   |   |
|---------------------------|----|----|---|---|
| 31                        | 17 | 16 | 1 | 0 |
| (reserved)                |    |    |   |   |
| LPADC_ADC2_HW_READ_RATE_1 |    |    |   |   |
| LPADC_ADC2_HW_READ_EN_1   |    |    |   |   |
| 0x64                      |    |    |   |   |
| 0 Reset                   |    |    |   |   |

**LPADC\_ADC2\_HW\_READ\_EN\_I** Configures whether to enable automatic monitoring for LP ADC2.

0: Disable

1: Enable

(R/W)

**LPADC\_ADC2\_HW\_READ\_RATE\_I** Configures the sampling rate for hardware-triggered automatic monitoring for LP ADC2. The sampling period = configured value × LP ADC2's working clock cycle. (R/W)

## Chapter 58

# Analog Voltage Comparator

## 58.1 Introduction

ESP32-P4 integrates two analog voltage comparators, i.e., analog voltage comparator [0](#) and analog voltage comparator [1](#). These comparators rely on special pads that support voltage comparison functionality to monitor voltage changes on these pads. Each analog voltage comparator has two pads associated with it, for the main voltage and the reference voltage respectively. The voltage comparison result generated by the analog voltage comparator can be used as Event Task Matrix (ETM) events to drive ETM tasks of other peripherals or trigger interrupts.

**Note:**

The information provided in this chapter applies to both analog voltage comparator [0](#) and analog voltage comparator [1](#). Unless otherwise indicated, the analog voltage comparator in this chapter refer to both analog voltage comparator [0](#) and analog voltage comparator [1](#).

## 58.2 Feature List

The analog voltage comparator has the following features:

- Voltage comparison
  - Configurable voltage comparison mode
  - Configurable reference voltage
- Interrupt upon changes of voltage comparison result
- ETM event generation

## 58.3 Architectural Overview

Figure [58.3-1](#) shows the structure of the analog voltage comparator.

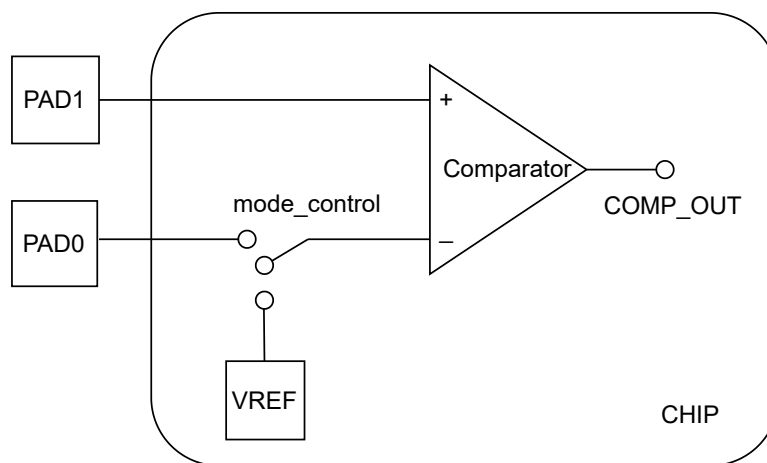


Figure 58.3-1. Analog Voltage Comparator Architecture

As shown in the figure above, the analog voltage comparator consists of:

- Two pad interfaces:
  - PAD1: Main voltage interface
  - PADO: External reference voltage interface
- VREF: Internal reference voltage interface
- mode\_control: Register-controlled switch for selecting the reference voltage source
- COMP\_OUT: Comparator voltage comparison result, which is an on-chip internal signal that cannot be directly accessed externally
  - If the main voltage is higher than the reference voltage, the COMP\_OUT signal is high.
  - If the main voltage is lower than the reference voltage, the COMP\_OUT signal is low.

## 58.4 Functional Description

The analog voltage comparator has the following functions:

- **Voltage comparison**

The analog voltage comparator relies on a specialized pads that support voltage comparison. For more information about general-purpose pads, please refer to Chapter 8 [GPIO Matrix and IO MUX](#). Table below shows the mapping between the PAD of analog voltage comparator *0* and GPIO pins.

Table 58.4-1. Mapping Between PAD and GPIO

| Analog Voltage Comparator          | PADO   | PAD1   |
|------------------------------------|--------|--------|
| Analog voltage comparator <i>0</i> | GPIO51 | GPIO52 |
| Analog voltage comparator <i>1</i> | GPIO53 | GPIO54 |

The comparison mode and reference voltage are configurable. For detailed configuration procedures, see Section 58.7 [Programming Procedures](#).

The voltage comparison results are output as the COMP\_OUT signal.

- **Voltage comparison mode control**

The analog voltage comparator compares the main voltage with the reference voltage, which can either be internal or external. There are two voltage comparison modes depending on the reference voltage selection:

- Comparing the main voltage with the external reference voltage.
- Comparing the main voltage with the internal reference voltage.

The voltage comparison mode can be configured through `LPSYSREG_MODE_COMP $n$`  ( $n = 0 \sim 1$ ).

- **Reference voltage configuration**

The internal reference voltage range is  $0 \sim (0.7 \times VDD\_IO\_6)$  V with a step of  $0.1 \times VDD\_IO\_6$  V, where `VDD_IO_6` is the supply voltage of the analog voltage comparator which is equal to the power supply voltage of the chip (usually 3.3 V). The internal reference voltage value can be configured through `LPSYSREG_DREF_COMP $n$`  ( $n = 0 \sim 1$ ).

The external reference voltage is accessed directly from the pad with an input range of  $0 \sim 0.7 \times VDD\_IO\_6$  V, same as the internal reference voltage, requiring no additional configuration.

- **Voltage comparison interrupt processing**

The voltage comparison result, i.e., the `COMP_OUT` signal, can be either high or low. Whenever the output value changes, a corresponding interrupt signal is generated.

## 58.5 Event Task Matrix Feature

The analog voltage comparator on ESP32-P4 supports the Event Task Matrix (ETM) function, which allows analog voltage comparator ETM events to trigger any peripherals' ETM tasks. This section introduces the ETM events related to analog voltage comparator. For more information, please refer to [Chapter 12 Event Task Matrix \(ETM\)](#).

The analog voltage comparator can generate the following ETM events:

- `GPIO_EVT_ZERO_DET_POS $n$` : Indicates that the `COMP_OUT` signal changes from low level to high level, i.e., the main voltage changes from below to above the reference voltage.
- `GPIO_EVT_ZERO_DET_NEG $n$` : Indicates that the `COMP_OUT` signal changes from high level to low level, i.e., the main voltage changes from higher to lower than the reference voltage.

The analog voltage comparator does not support any ETM tasks.

## 58.6 Interrupts

ESP32-P4's analog voltage comparator can generate the `GPIO_PAD_COMP_INT` interrupt signal that will be sent to the [Interrupt Matrix](#).

There are several internal interrupt sources from analog voltage comparator that can generate the above interrupt signal. The interrupt sources from analog voltage comparator are listed with their trigger conditions and the resulted interrupt signal(s) in [Table 58.6-1](#).

Table 58.6-1. Analog Voltage Comparator's Internal Interrupt Sources

| Internal Interrupt Source                 | Trigger Condition  | Interrupt Signal  |
|---|--|-------------------|
| GPIO_COMP $n$ _ALL_INT ( $n = 0 \sim 1$ ) | Any COMP_OUT signal transition occurs                    | GPIO_PAD_COMP_INT |
| GPIO_COMP $n$ _NEG_INT ( $n = 0 \sim 1$ ) | The COMP_OUT signal changes from high level to low level | GPIO_PAD_COMP_INT |
| GPIO_COMP $n$ _POS_INT ( $n = 0 \sim 1$ ) | The COMP_OUT signal changes from low level to high level | GPIO_PAD_COMP_INT |

**Note:**

For definitions of *interrupt*, *interrupt signal*, *interrupt source*, and their correlations, please refer to Chapter 11 [Interrupt Matrix](#) > Section 11.2 [Interrupt Terminology in ESP32-P4](#).

Each interrupt source can be configured by a common set of registers that are described in Section [Interrupt Configuration Registers](#). The specific registers can be found in Section 8.19.1 [HP GPIO Matrix Register Summary](#).

## 58.7 Programming Procedures

The programming procedure for the analog voltage comparator is as follows:

**Note:**

For more information about the register fields mentioned in this section, refer to Chapter 3 [System Registers](#) [to be added later].

1. Enable the comparator by setting LPSYSREG\_XPD\_COMP $n$  ( $n = 0 \sim 1$ ) to 1.
2. Disable normal digital pad functions (including IE, OE, WPU, and WPD) for PAD1, and if using the external reference voltage, also for PADO. For detailed configuration, see Chapter 8 [GPIO Matrix and IO MUX](#).
3. Configure the comparison mode by setting LPSYSREG\_MODE\_COMP $n$  ( $n = 0 \sim 1$ ):
  - 0: Configures to compare the main voltage with the internal reference voltage;
  - 1: Configures to compare the main voltage with the external reference voltage.
4. Configure the internal reference voltage through LPSYSREG\_DREF\_COMP $n$  ( $n = 0 \sim 1$ ), which offers a voltage range of  $0 \sim (0.7 \times VDD\_IO\_6)$  V with a step of  $0.1 \times VDD\_IO\_6$  V.

# Part IX

## Appendix

This part contains the following information starting from the next page:

- [\*Related Documentation and Resources\*](#)
- [\*Glossary\*](#)
- [\*Programming Reserved Register Field\*](#)
- [\*Interrupt Configuration Registers\*](#)
- [\*Revision History\*](#)

## Related Documentation and Resources

### Related Documentation

- [ESP32-P4 Series Datasheet](#) – Specifications of the ESP32-P4 hardware.
- [ESP32-P4 Hardware Design Guidelines](#) – Guidelines on how to integrate the ESP32-P4 into your hardware product.
- [Certificates](#)  
<https://espressif.com/en/support/documents/certificates>
- [Documentation Updates and Update Notification Subscription](#)  
<https://espressif.com/en/support/download/documents>

### Developer Zone

- [ESP-IDF Programming Guide for ESP32-P4](#) – Extensive documentation for the ESP-IDF development framework.
- [ESP-IDF](#) and other development frameworks on GitHub.  
<https://github.com/espressif>
- [ESP32 BBS Forum](#) – Engineer-to-Engineer (E2E) Community for Espressif products where you can post questions, share knowledge, explore ideas, and help solve problems with fellow engineers.  
<https://esp32.com/>
- [The ESP Journal](#) – Best Practices, Articles, and Notes from Espressif folks.  
<https://blog.espressif.com/>
- See the tabs *SDKs and Demos*, *Apps*, *Tools*, *AT Firmware*.  
<https://espressif.com/en/support/download/sdks-demos>

### Products

- [ESP32-P4 Series SoCs](#) – Browse through all ESP32-P4 SoCs.  
<https://espressif.com/en/products/socs?id=ESP32-P4>
- [ESP32-P4 Series DevKits](#) – Browse through all ESP32-P4-based devkits.  
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## Glossary

### Abbreviations for Peripherals

|                 |   |
|-----------------|---|
| 2D-DMA          | 2D-DMA Controller   |
| ADC             | ADC Controller  |
| AES             | AES (Advanced Encryption Standard) Accelerator                |
| DMA             | DMA (Direct Memory Access) Controller                         |
| DSA             | Digital Signature Algorithm                                   |
| ECC             | ECC (Elliptic Curve Cryptography) Accelerator                 |
| ECDSA           | Elliptic Curve Digital Signature Algorithm                    |
| eFuse           | eFuse Controller  |
| EMAC            | Ethernet Media Access Controller                              |
| ETM             | Event Task Matrix   |
| HMAC            | HMAC (Hash-based Message Authentication Code) Accelerator     |
| I2C             | I2C (Inter-Integrated Circuit) Controller                     |
| I2S             | I2S (Inter-IC Sound) Controller                               |
| I3C             | I3C (Improved Inter-Integrated Circuit) Controller            |
| ISP             | Image Signal Processor  |
| LCD_CAM         | LCD and Camera Controller                                     |
| LEDC            | LED PWM (Pulse Width Modulation) Controller                   |
| MCPWM           | Motor Control PWM (Pulse Width Modulation)                    |
| PARLIO          | Parallel IO Controller  |
| PCNT            | Pulse Count Controller  |
| PIE             | Processor Instruction Extensions                              |
| PMS             | Permission Control  |
| PPA             | Pixel-Processing Accelerator                                  |
| RMT             | Remote Control Peripheral                                     |
| RNG             | Random Number Generator                                       |
| RSA             | RSA (Rivest Shamir Adleman) Accelerator                       |
| SDHOST          | SD/MMC Host Controller  |
| SHA             | SHA (Secure Hash Algorithm) Accelerator                       |
| SPI             | SPI (Serial Peripheral Interface) Controller                  |
| TIMG            | Timer Group   |
| TOUCH           | Touch Sensor  |
| TRACE           | RISC-V Trace Encoder  |
| TSENS           | Temperature Sensor  |
| TWAI            | Two-Wire Automotive Interface                                 |
| UART            | UART (Universal Asynchronous Receiver-Transmitter) Controller |
| ULP Coprocessor | Ultra-low-power Coprocessor                                   |
| USB OTG         | USB On-The-Go   |
| USB_SERIAL_JTAG | USB Serial/JTAG Controller                                    |
| VAD             | Voice Activity Detection                                      |
| VDMA            | VDMA Controller   |
| WDT             | Watchdog Timers   |

XTS\_AES External Memory Encryption and Decryption

## Abbreviations Related to Registers

|        |   |
|--------|---|
| REG    | <b>Register.</b>  |
| SYSREG | <b>System registers</b> are a group of registers that control system reset, memory, clocks, software interrupts, power management, clock gating, etc.   |
| ISO    | <b>Isolation.</b> If a peripheral or other chip component is powered down, the pins, if any, to which its output signals are routed will go into a floating state. ISO registers isolate such pins and keep them at a certain determined value, so that the other non-powered-down peripherals/devices attached to these pins are not affected. |
| NMI    | <b>Non-maskable interrupt</b> is a hardware interrupt that cannot be disabled or ignored by the CPU instructions. Such interrupts exist to signal the occurrence of a critical error.   |
| W1TS   | Abbreviation added to names of registers/fields to indicate that such register/field should be used to set a field in a corresponding register with a similar name. For example, the register <code>GPIO_ENABLE_W1TS_REG</code> should be used to set the corresponding fields in the register <code>GPIO_ENABLE_REG</code> .                   |
| W1TC   | Same as <i>W1TS</i> , but used to clear a field in a corresponding register.  |

## Access Types for Registers

Sections *Register Summary* and *Register Description* in TRM chapters specify access types for registers and their fields.

Most frequently used access types and their combinations are as follows:

- |          |              |               |
|----------|--------------|---------------|
| • RO     | • R/W/SS     | • R/WS/SS/SC  |
| • WO     | • R/W/SS/SC  | • R/SS/WTC    |
| • WT     | • R/WC/SS    | • R/SC/WTC    |
| • R/W    | • R/WC/SC    | • R/SS/SC/WTC |
| • R/W1   | • R/WC/SS/SC | • RF/WF       |
| • WL     | • R/WS/SC    | • R/SS/RC     |
| • R/W/SC | • R/WS/SS    | • varies      |

Descriptions of all access types are provided below.

- R **Read.** User application can read from this register/field; usually combined with other access types.
- RO **Read only.** User application can only read from this register/field.
- HRO **Hardware Read Only.** Only hardware can read from this register/field; used for storing default settings for variable parameters.
- W **Write.** User application can write to this register/field; usually combined with other access types.
- WO **Write only.** User application can only write to this register/field.
- W1 **Write Once.** User application can write to this register/field only once; only allowed to write 1; writing 0 is invalid.
- SS **Self set.** On a specified event, hardware automatically writes 1 to this register/field; used with 1-bit fields.
- SC **Self clear.** On a specified event, hardware automatically writes 0 to this register/field; used with 1-bit and multi-bit fields.
- SM **Self modify.** On a specified event, hardware automatically writes a specified value to this register/field; used with multi-bit fields.
- SU **Self update.** On a specified event, hardware automatically updates this register/field; used with multi-bit fields.
- RS **Read to set.** If user application reads from this register/field, hardware automatically writes 1 to it.
- RC **Read to clear.** If user application reads from this register/field, hardware automatically writes 0 to it.
- RF **Read from FIFO.** If user application writes new data to FIFO, the register/field automatically reads it.
- WF **Write to FIFO.** If user application writes new data to this register/field, it automatically passes the data to FIFO via APB bus.
- WS **Write any value to set.** If user application writes to this register/field, hardware automatically sets this register/field.

- W1S **Write 1 to set.** If user application writes 1 to this register/field, hardware automatically sets this register/field.
- W0S **Write 0 to set.** If user application writes 0 to this register/field, hardware automatically sets this register/field.
- WC **Write any value to clear.** If user application writes to this register/field, hardware automatically clears this register/field.
- W1C **Write 1 to clear.** If user application writes 1 to this register/field, hardware automatically clears this register/field.
- W0C **Write 0 to clear.** If user application writes 0 to this register/field, hardware automatically clears this register/field.
- WT **Write 1 to trigger an event.** If user application writes 1 to this field, this action triggers an event (pulse in the APB bus) or clears a corresponding WTC field (see WTC).
- WTC **Write to clear.** Hardware automatically clears this field if user application writes 1 to the corresponding WT field (see WT).
- W1T **Write 1 to toggle.** If user application writes 1 to this field, hardware automatically inverts the corresponding field; otherwise - no effect.
- W0T **Write 0 to toggle.** If user application writes 0 to this field, hardware automatically inverts the corresponding field; otherwise - no effect.
- WL **Write if a lock is deactivated.** If the lock is deactivated, user application can write to this register/field.
- varies **The access type varies.** Different fields of this register might have different access types.

## Programming Reserved Register Field

### Introduction

A field in a register is reserved if the field is not open to users, or produces unpredictable results if configured to values other than defaults.

### Programming Reserved Register Field

The reserved fields should not be modified. It is not possible to write only part of a register since registers must always be written as a whole. As a result, to write an entire register that contains reserved fields, you can choose one of the following two options:

1. Read the value of the register, modify only the fields you want to configure and then write back the value so that reserved fields are untouched.

OR

2. Modify only the fields you want to configure and write back the default value of the reserved fields. The default value of a field is provided in the "Reset" line of a register diagram. For example, the default value of Field\_A in [Register X](#) is 1.

**Register 58.1. Register X (Address)**

|            |   |   |   |   |   |   |   |   |   |   |   |         |  |    |    |            |    |   |   |   |   |   |   |   |   |   |   |         |   |         |   |       |
|------------|---|---|---|---|---|---|---|---|---|---|---|---------|--|----|----|------------|----|---|---|---|---|---|---|---|---|---|---|---------|---|---------|---|-------|
| (reserved) |   |   |   |   |   |   |   |   |   |   |   | Field_C |  |    |    | (reserved) |    |   |   |   |   |   |   |   |   |   |   | Field_B |   | Field_A |   |       |
| 31         |   |   |   |   |   |   |   |   |   |   |   | 20      |  | 19 | 16 |            | 15 | 2 |   |   |   |   |   |   |   |   |   |         |   | 1       | 0 |       |
| 0          | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0000    |  | 0  | 0  | 0          | 0  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0       | 0 | 0       | 1 | Reset |

Suppose you want to set Field\_A, Field\_B, and Field\_C of [Register X](#) to 0x0, 0x1, and 0x2, you can:

- Use option 1 and fill in the reserved fields with the value you have just read. Suppose the register reads as 0x0000\_0003. Then, you can modify the fields you want to configure, thus writing 0x0002\_0002 to the register.
- Use option 2 and fill in the reserved fields with their defaults, thus writing 0x0002\_0002 to the register.

## Interrupt Configuration Registers

Generally, the peripherals' internal interrupt sources can be configured by the following common set of registers:

- **RAW** (Raw Interrupt Status) register: This register indicates the raw interrupt status. Each bit in the register represents a specific internal interrupt source. When an interrupt source triggers, its RAW bit is set to 1.
- **ENA** (Enable) register: This register is used to enable or disable the internal interrupt sources. Each bit in the ENA register corresponds to an internal interrupt source.

By manipulating the ENA register, you can mask or unmask individual internal interrupt source as needed. When an internal interrupt source is masked (disabled), it will not generate an interrupt signal, but its value can still be read from the RAW register.

- **ST** (Status) register: This register reflects the status of enabled interrupt sources. Each bit in the ST register corresponds to a specific internal interrupt source. The ST bit being 1 means that both the corresponding RAW bit and ENA bit are 1, indicating that the interrupt source is triggered and not masked. The other combinations of the RAW bit and ENA bit will result in the ST bit being 0.

The configuration of ENA/RAW/ST registers is shown in Table 58.7-4.

- **CLR** (Clear) register: The CLR register is responsible for clearing the internal interrupt sources. Writing 1 to the corresponding bit in the CLR register clears the interrupt source.

Table 58.7-4. Configuration of ENA/RAW/ST Registers

| ENA Bit Value | RAW Bit Value | ST Bit Value |
|---------------|---------------|--------------|
| 0             | Ignored       | 0            |
| 1             | 0             | 0            |
|               | 1             | 1            |

## Revision History

| Date       | Version | Release notes       |
|------------|---------|---------------------|
| 2025-06-04 | v0.1    | Preliminary release |



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